MVME135/D2

MVME135, MVME135-1 MVME135A, MVME136, AND MVME136A 32-Bit Microcomputers User's Manual

MOTOROLA

MOTOROLA

MVME135/L3

SEPTEMBER 1987

MVME135/135-1/MVME136

CUSTOMER LETTER

This letter is directed to customers using MVME135Bug, Revision 1.0, and to software designers writing code for the MC68681 DUART on the MVME135. The purpose is to clarify an error in the data sheet on the MC68681 which defines the reset condition of the Interrupt Status Register (ISR) as $00. Two potential situations exist that can cause this register to not be read as $00 after a power-up or reset condition.

The first case involves bits two and six of the ISR, the Delta Break bits for each serial port. Due to an anomaly in the chip circuitry, either of these bits may be set after a power-up condition. This anomaly has been verified by both vendors of the chip (Motorola and Signetics) and should not be considered fatal faults in the part, as their power-up conditions will not affect normal operation of these bits. The proper initialization sequence for these bits is to write all port control registers to desired values, then issue a "Reset Channel x Break Change Interrupt" command for each channel. At this point, the state of these bits will be valid and further operations of these bits will be accurate.

The second case involves bit three of the ISR, the Counter/Timer Ready bit. This bit may be set after a power-up or reset condition and prior to being read by software in the ISR. The reason for this is that the MC68681 powers up in the free running timer mode, and the timer may reach the end of a count-down sequence, setting the Counter/Timer Ready bit at any time after release of the reset line. This status condition is normal to the device and will not affect normal operation of the part. The proper initialization sequence for the MC68681 timer is to initialize the desired timer modes, then perform a read of the Stop Counter command address to clear ISR bit three. At this point, further setting of the bit will be due to normal counter/timer operation and may be considered valid.

Due to operation of the ISR in the MC68681 as described above, intermittent failures of the MVME135Bug, Revision 1.0, confidence test at test $A0 may be observed. These failures are related to the ISR not containing $00 after reset. As described, this is not a fatal error, and the MVME135Bug will operate normally after exiting the confidence test. Future releases of the MVME135Bug will correct for the operation of the MC68681 and will not demonstrate this error.

We apologize for any inconvenience this may cause.

2217B-1 PRINTED IN USA 6/88I MPS 2M

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS MAIL PERMIT NO. 2565 PHOENIX, ARIZONA

POSTAGE WILL BE PAID BY ADDRESSEE

MOTOROLA INC.

Computer Group, Microcomputer Division, DW164
2900 South Diablo Way
Tempe, AZ 85282-9741

ENTS

ın. Please use this form.

e _____

ephone Number _____

air the product

_____

manual?

☐ Other _____

od ☐ Fair ☐ Poor

Presentation: ☐ Excellent ☐ Very Good ☐ Good ☐ Fair ☐ Poor

What features of the manual are most useful (tables, figures, appendixes, index, etc.)?

Is the information easy to understand? ☐ Yes ☐ No If you checked no, please explain:

Is the information easy to find? ☐ Yes ☐ No If you checked no, please explain:

Technical Accuracy: ☐ Excellent ☐ Very Good ☐ Good ☐ Fair ☐ Poor

If you have found technical or typographical errors, please list them here.

Page Number	Description of Error

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Field Service Division for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

PREFACE

This manual provides general information, hardware preparation, installation instructions, functional description, and support information for the MVME135/MVME136 Monoboard Series of 32-Bit Microcomputers.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system or in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this manual, you should be faimilar with the publications listed in the *Related Documentation* paragraph in Chapter 1 of this manual.

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL ENVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES NECESSARY TO CORRECT THE INTERFERENCE.

Second Edition

First Edition April 1987

MVME135, MVME135-1, MVME135A, MVME136, AND MVME136A 32-BIT MICROCOMPUTERS USER'S MANUAL

(MVME135/D2)

The information in this document has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, Motorola reserves the right to make changes to any products herein to improve reliability, function, or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights or the rights of others.

TABLE OF CONTENTS

Page

CHAPTER 1 - GENERAL INFORMATION

1.1 INTRODUCTION 1-1
1.2 FEATURES 1-1
1.3 SPECIFICATIONS 1-2
1.3.1 Cooling Requirements 1-4
1.3.2 FCC Compliance 1-4
1.4 GENERAL DESCRIPTION 1-5
1.5 MVME135/136 CONFIGURATIONS 1-5
1.6 REFERENCE DOCUMENTATION 1-6
1.7 MANUAL TERMINOLOGY 1-7

CHAPTER 2 - HARDWARE PREPARATION AND INSTALLATION

2.1 INTRODUCTION 2-1
2.2 UNPACKING INSTRUCTIONS 2-1
2.3 HARDWARE PREPARATION 2-1
2.3.1 VMEbus Lock For VSBbus (J1) 2-4
2.3.2 Bus Grant/Request Level Select (J2) 2-4
2.3.3 Factory Test Jumper (J5) 2-6
2.3.4 RAM Acknowledge Mode (J6) 2-6
2.3.5 ROM Size Select (J7) 2-7
2.3.6 DRAM Address Multiplex Select (J8) 2-8
2.3.7 Local/VMEbus Timeout Disable (J11) 2-8
2.3.8 DRAM Cycle Start Mode Select (J12) 2-9
2.3.9 External Timer Select (J13,J14) 2-10
2.4 SERIAL PORT CABLING 2-11
2.4.1 DB-9 To DB-25 Cable Connection 2-11
2.5 VME CHASSIS INSTALLATION 2-12

CHAPTER 3 - OPERATING INSTRUCTIONS

3.1 INTRODUCTION 3-1
3.2 FRONT PANEL 3-1
3.2.1 LED Indicators 3-1
3.2.2 ABORT Switch (S1) 3-1
3.2.3 RESET Switch (S2) 3-1
3.2.4 Mapping Switch (S3) 3-3
3.2.5 System Configuration Switch (S4) 3-10
3.3 MEMORY MAP AND MAP DECODER 3-11
3.3.1 MVME135/135-1/135A Main Memory Map 3-12
3.3.2 MVME136/135A Main Memory Map 3-13

TABLE OF CONTENTS (cont.)

Page

CHAPTER 4 - FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION 4-1
4.2 GENERAL DESCRIPTION 4-1
4.2.1 Data Bus Structure 4-1
4.2.2 Memory Map 4-1
4.2.3 Timing 4-1
4.2.4 MVME135/135-1/136 DRAM Cycle Times 4-1
4.2.5 MVME135A/136A DRAM Cycle Times 4-4
4.2.6 ROM/PROM/EPROM/EEPROM Cycle Times 4-4
4.2.7 VMEbus Cycle Times 4-5
4.2.8 VMEbus Arbitration Time 4-5
4.3 MC68Ø2Ø MPU 4-6
4.4 MC68881 FPCP 4-6
4.5 MC68851 PMMU 4-6
4.6 DEBUG MONITOR FIRMWARE 4-7
4.7 VME SUBSYSTEM BUS (VSBbus) 4-7
4.8 DYNAMIC RAM 4-7
4.9 FUNCTION CODE ASSIGNMENTS 4-8
4.1Ø MVME135/136 USE OF CPU SPACE 4-8
4.1Ø.1 MC68851 Breakpoint Support 4-9
4.1Ø.2 MC68851 Breakpoint Operation 4-1Ø
4.1Ø.3 MC68851 Breakpoint Architecture 4-11
4.1Ø.4 MC68851 Acknowledge Cycle Operation 4-12
4.1Ø.5 Access Level Control 4-12
4.1Ø.6 Coprocessor Communications 4-13
4.11 INTERRUPT HANDLER 4-14
4.12 ONBOARD ROM/PROM/EPROM 4-17
4.13 DUAL SERIAL PORTS 4-17
4.14 MVME135/136 TIMER 4-17
4.15 LOCAL CONTROL/STATUS REGISTERS 4-18
4.15.1 Status Register Format And Functions 4-19
4.15.2 Control Register Format And Functions 4-21
4.16 MULTIPROCESSOR CONTROL/STATUS REGISTERS (MPCSR) .. 4-27
4.16.1 Base Address Selection 4-32
4.17 VSBbus CONTROL/STATUS REGISTER 4-33
4.17.1 VSBbus Control/Status Format and Functions 4-33
4.18 CONFIGURING A VME SUBSYSTEM BUS 4-37

CHAPTER 5 - SUPPORT INFORMATION

5.1 INTRODUCTION 5-1
5.2 INTERCONNECTION SIGNALS 5-1
5.2.1 Connector P1 Interconnect Signals 5-1

TABLE OF CONTENTS (cont.)

		Page
5.2.2	Connector P2 Interconnect Signals	5-6
5.2.3	Connector J3 Interconnect Signals	5-13
5.2.4	Connector J4 Interconnect Signals	5-15
5.2.5	Connector J9 Interconnect Signals	5-19
5.2.6	Connector J1Ø Interconnect Signals	5-2Ø
5.3	PARTS LIST	5-21
5.4	SCHEMATIC DIAGRAMS	5-43

APPENDIX A - MVME135/135-1/136 PAL2 SOURCE LISTING A-1

APPENDIX B - MVME135A/136A PAL2 SOURCE LISTING B-1

APPENDIX C - MVME135/136 LOCAL MEMORY MAP C-1

LIST OF ILLUSTRATIONS

FIGURE 2-1.	Jumper, Connector, And Switch Location Diagram	2-2
FIGURE 3-1.	MVME135/136 Front Panel	3-2
FIGURE 3-2.	MVME135/135-1/136 Slave Access Addressing	3-4
FIGURE 3-3.	MVME135A/136A Slave Access Addressing	3-7
FIGURE 4-1.	MVME135/135-1/136 Block Diagram	4-2
FIGURE 4-2.	MVME135A/136A Block Diagram	4-3
FIGURE 4-3.	CPU Space Type Field Encoding	4-9
FIGURE 4-4.	Breakpoint Acknowledge Cycle Address Encoding	4-1Ø
FIGURE 4-5.	Breakpoint Registers	4-11
FIGURE 4-6.	Breakpoint Acknowledge Data Register Format	4-11
FIGURE 4-7.	Breakpoint Acknowledge Control Register Format	4-12
FIGURE 4-8.	ALC Interface Logical Address Bus Encoding	4-13
FIGURE 4-9.	Coprocessor Interface Address Bus Encoding	4-14
FIGURE 4-1Ø.	Serial Port Interconnections	4-17
FIGURE 4-11.	D16/D32 Default Data Segmentation	4-27
FIGURE 4-12.	MPCSR And DRAM Address Mapping	4-35
FIGURE 5-1.	MVME135/136 Parts Location Diagram	5-33
FIGURE 5-2.	1Mb DRAM Mezzanine Board Parts Location Diagram	5-38
FIGURE 5-3.	4Mb DRAM Mezzanine Board Parts Location Diagram	5-4Ø
FIGURE 5-4.	MVME135/136 By-Pass Board Parts Location Diagram	5-42
FIGURE 5-5.	MVME135/136 Schematic Diagram	5-45

Page

FIGURE 5-6. 1Mb DRAM Mezzanine Schematic Diagram 5-97
FIGURE 5-7. 4Mb DRAM Mezzanine Schematic Diagram 5-113
FIGURE 5-8. PMMU By-Pass Board Schematic Diagram 5-131

LIST OF TABLES

TABLE 1-1. MVME135/136 Specifications 1-2
TABLE 1-2. MVME135/136 Configurations 1-6
TABLE 2-1. Jumper Block Placements 2-3
TABLE 3-1. MVME135/136 Front Panel LED Status 3-3
TABLE 3-2. Function Code Assignments 3-11
TABLE 3-3. MVME135/135-1/136 Main Memory Map 3-12
TABLE 3-4. MVME135A/136A Main Memory Map 3-13
TABLE 4-1. MVME135/136 Timing 4-3
TABLE 4-2. Function Code Assignments 4-9
TABLE 4-3. ALC Interface Registers Map 4-13
TABLE 4-4. MC68851 Coprocessor Interface Register Map 4-14
TABLE 4-5. MC68881 Coprocessor Interface Register Map 4-15
TABLE 4-6. Interrupt Handler Priority Assignments 4-15
TABLE 4-7. Multiprocessor Control/Status Registers 4-28
TABLE 4-8. Mapping On The VMEbus 4-30
TABLE 5-1. Connector P1 Interconnect Signals 5-1
TABLE 5-2. Connector P2 Interconnect Signals 5-6
TABLE 5-3. Connector J3 Interconnect Signals 5-13
TABLE 5-4. Connector J4 Interconnect Signals 5-15
TABLE 5-5. Connector J9 Interconnect Signals 5-19
TABLE 5-6. Connector J10 Interconnect Signals 5-20
TABLE 5-7. MVME135/136 Parts List 5-21
TABLE 5-8. 1Mb DRAM Mezzanine Board Parts List 5-37
TABLE 5-9. 4Mb DRAM Mezzanine Board Parts List 5-39
TABLE 5-10. PMMU By-Pass Board Parts List 5-41

CHAPTER 1 - GENERAL INFORMATION

1.1 INTRODUCTION

This user's manual provides general information, preparation and installation instructions, operating instructions, functional description, and support information for the MVME135/MVME136 series of 32-bit microcomputers (refer to section 1.5 for the different module configurations). Unless otherwise specified, these microcomputers are referred to as the MVME135/136 throughout the contents of this user's manual.

1.2 FEATURES

The features of the MVME135/136 include:

- MC68Ø2Ø Virtual Memory Microprocessor with 32-bit address and data at 16.67 MHz or 2Ø.ØØ MHz.
- 1Mb of shared local DRAM with no wait cycles, 32-bit wide; accessible from the VMEbus with optional parity (MVME135, MVME135-1, and MVME136 versions only).
- 4Mb of shared local DRAM with one wait cycle, 32-bit wide; accessible from the VMEbus with optional parity (MVME135A version only).
- 4Mb of shared local DRAM with two wait cycles, 32-bit wide; accessible from the VMEbus with optional parity (MVME136A version only). Parity does not add any additional wait cycles for this version.
- On-board socket for MC68881 Floating Point Coprocessor (FPCP) at 16.67 MHz or 2Ø.ØØ MHz.
- On-board socket for MC68851 Demand Paged Memory Management Unit (PMMU) at 16.67 MHz (MVME136 and MVME136A versions only).
- Multi-master VME Subsystem Bus (VSBbus) interface; 32-bit secondary bus support.
- VMEbus interface; 32-bit address and data.
- VMEbus Interrupt Handler.
- Z8Ø36A Programmable Timer Module.
- Periodic tick interrupt (level 6).
- Watchdog reset (momentary local reset, local reset and hold, or a system level reset may be software selected).
- VSBbus can eliminate "software holes" in VMEbus memory map caused by exception tables and stacks.

- Single level system controller capability (level is jumper selectable).
- High level multiprocessor control and status registers used for inter-processor signaling and communication.
- Round Robin requesting provides fairness of VMEbus mastership for systems with multiple MVME135/136s (software selectable).
- Two front panel RS-232C serial ports with level translators; eliminating the need for a transition board between the MVME135/136 and a terminal or modem.
- Two on-board ROM sockets for a capacity of 128Kb (configured for Industry Standard JEDEC 28-pin ROM/PROM/EPROM devices; user provided).

1.3 SPECIFICATIONS

General specifications for the MVME135/136 are provided in the following table. Sections 1.2.2 and 1.2.3 detail cooling requirements and FCC compliance, respectively.

TABLE 1-1. MVME135/136 SPECIFICATIONS

Characteristic	Specification
Microprocessor	MC68Ø2Ø 32-bit microprocessor
Clock signal:	
MVME135/135A/136/136A	16.67 MHz CPU clock frequency
MVME135-1	2Ø.ØØ MHz CPU clock frequency
Power requirements:	
MVME135/135-1/135A	+5 Vdc, 6.75 A maximum (5.6 A typical) +12 Vdc, 5Ø mA maximum (1Ø mA typical) -12 Vdc, 9Ø mA maximum (3Ø mA typical)
MVME136/136A	+5 Vdc, 7.ØØ A maximum (5.8 A typical) +12 Vdc, 5Ø mA maximum (1Ø mA typical) -12 Vdc, 9Ø mA maximum (3Ø mA typical)
	NOTE: Backplane Connectors -- The P2 backplane is not only necessary for 32-bit operation but is also used to connect +5 V to the MVME135/136 module for current distribution. The module draws 5.6 A under typical operation and should not be operated without a P2 backplane.

TABLE 1-1. MVME135/136 SPECIFICATIONS (cont.)

Characteristic	Specification
Addressing:	
System Size (Total on-/off-board)	32-bits = 4 gigabytes linear address space
ROM/EPROM	Two EPROM/ROM sockets for 16Kb or 32Kb devices using +5 Vdc only (JEDEC standard 28-pin devices; user supplied).
Serial I/O ports	Two multi-protocol serial communications channels with RS-232C interface (connection made via two DB-9 connectors from the front panel).
Timer	A Z8Ø36A programmable timer module with three independent 16-bit timers.
Interrupts	Any seven possible VMEbus interrupts can be received by the MVME135/136. VSBbus has interrupt capability, as do most on-board devices.
On-board memory	
MVME135/135-1	1Mb, Ø wait state without parity and 1 wait state with parity.
MVME136	1Mb, 1 wait state without parity and 2 wait states with parity. The MC68851 Paged Memory Management Unit (PMMU) adds 1 wait state to local memory accesses.
MVME135A	4Mb, 1 wait state with or without parity.
MVME136A	4Mb, 2 wait states with or without parity. The MC68851 Paged Memory Management Unit (PMMU) adds 1 wait state to local memory accesses.
Temperatures:	
Operating	Ø to 5Ø degrees C (inlet air temperature with forced air cooling)
Storage	-4Ø to 85 degrees C
Relative humidity	5% to 95% (non-condensing)
Physical size (PCB):	(not including the front panel)
Height x width	6.3Ø inches (16.ØØ cm) x 9.19 inches (23.34 cm)
Thickness	Ø.Ø62 inch (Ø.157 cm)

TABLE 1-1. MVME135/136 SPECIFICATIONS (cont.)

Characteristic	Specification
Part projections:	
Component side	Ø.5Ø inch (1.27 cm) maximum
Solder side	Ø.Ø67 inch (Ø.17 cm) maximum
Connectors:	
VMEbus/VSBbus	DIN triple row, 96-pin male (P1, P2)
RS-232C	DB-9, 9-pin female (J9, J1Ø)

1.3.1 Cooling Requirements

Motorola VMEmodules are specified, designed, and tested to operate reliably with an incoming air temperature range from Ø degrees C to 5Ø degrees C (32 degrees F to 122 degrees F) with forced air cooling. Temperature qualification is performed in a standard Motorola VMEsystem 1ØØØ chassis. Twenty-five watt load boards are inserted in the two card slots, one on each side, adjacent to the board under test to simulate a high power density system configuration. An assembly of three axial fans, rated at 1ØØ CFM per fan, is placed directly under the MVME card cage. The incoming air temperature is measured between the fan assembly and the card cage where the incoming airstream first encounters the board under test. Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 1Ø CFM flowing over the module. Less air flow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions it may be possible to operate the module reliably at higher than 5Ø degrees C with increased air flow. It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume of air flowing over a module.

1.3.2 FCC Compliance

The MVME135/136 module is tested in an FCC-compliant chassis, and meets the requirements for Class A equipment. FCC compliance was achieved under the following conditions:

1. Shielded cables on all external I/O ports.
2. Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
3. Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
4. Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented; failure to do so could compromise the FCC compliance of the equipment containing the modules.

1.4 GENERAL DESCRIPTION

The MVME135/136 is a high performance MC68Ø2Ø microprocessor-based module implemented on a VME double-high, single-wide form-factor. The MVME135/136 incorporates an MC68Ø2Ø, a 32-bit address and data microprocessor, a high level multiprocessor CSR, and 1Mb or 4Mb of fast DRAM. Other main features provided include a Demand Paged Memory Management Unit (PMMU), a Floating Point Coprocessor (FPCP), and interfaces to the VMEbus and the VSBbus.

The MVME135/136 is designed for those applications which require fast on-board RAM and a secondary bus (VSBbus). The features of the MVME135/136 include high performance and an elegant architecture. The MVME135/136 is especially suited to applications requiring multiple processors where the efficiency of inter-processor communication is important.

The 135bug resident debug package (refer to Motorola publication MVME135BUG) is the firmware package designed for use with the MVME135/136 module. 135bug provides a powerful system debugging tool for VMEmodule systems. This firmware features a one line assembler/disassembler, provisions for upload/download, and disk bootstrap commands. 135bug is available as an EPROM-based resident package which is plugged into IC sockets U54 and U56 on the MVME135/136.

1.5 MVME135/136 CONFIGURATIONS

There are five module configurations available in the MVME135/136 series of 32-bit microcomputers. These configurations are listed in the following table.

TABLE 1-2. MVME135/136 CONFIGURATIONS

Module Designation	CPU Clock Cycle (MHz)	On-Board Memory	MC68881 (FPCP)	MC68851 (PMMU)
MVME135	16.67	1Mb	Yes	No
MVME135-1	20.00	1Mb	Yes	No
MVME135A	16.67	4Mb	Yes	No
MVME136	16.67	1Mb	Yes	Yes
MVME136A	16.67	4Mb	Yes	Yes

1.6 REFERENCE DOCUMENTATION

The following publications may provide additional helpful information. If not shipped with this product, they may be purchased from Motorola's Literature Distribution Center, 616 West 24th Street, Tempe, Arizona 85282; telephone (602) 994-6561.

DOCUMENT TITLE	MOTOROLA PUBLICATION NUMBER
MC68020 32-Bit Microprocessor U.M.	MC68020UM/AD
MC68851 Paged Memory Management Unit U.M.	MC68851UM/AD
MC68881 Floating-Point Coprocessor U.M.	MC68881UM/AD
MVME204-1/-2 Dual Ported Dynamic Memory U.M.	MVME204
MVME204-2F Dual Ported Dynamic Memory U.M.	MVME204F
MVME224-1/-2 4/8Mb Dynamic Memory U.M.	MVME224
MVSB2400 VSBchip U.M.	MVSB2400
VME System Architecture Guide	MVMESYSAM/D
VME Subsystem Bus (VSBbus) Specification (Rev A.1)	MVMESB
135bug Diagnostic/Debug Package U.M.	MVME135BUG

NOTE: Although not shown in the above list, each Motorola MCD manual publication number is suffixed with characters which represent the revision level of the document, such as "D2" (the second revision of a manual); a supplement bears the same number as the manual but has a suffix such as "A1" (the first supplement to the manual).

U.M. denotes User's Manual.

Additional publications that may provide helpful information are listed below.

ANSI/IEEE Standard 1Ø14-1987 Versatile Backplane Bus: VMEbus	Institute of Electrical and Electronics Engineers, Inc. 345 East 47th Street New York, New York 1ØØ17
Zilog Z-CIO (Z8Ø36) Counter/Timer and Parallel I/O Unit Technical Manual	Zilog Incorporation 1315 Del Avenue Campbell, California 95ØØ8 (4Ø8) 37Ø-8ØØØ

1.7 MANUAL TERMINOLOGY

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

CHAPTER 2 - HARDWARE PREPARATION AND INSTALLATION

2.1 INTRODUCTION

This chapter provides the unpacking, hardware preparation, and installation instructions for the MVME135/136.

2.2 UNPACKING INSTRUCTIONS

> **NOTE**
>
> If shipping carton is damaged upon receipt, request that the carrier's agent be present during unpacking/inspection of equipment.

Carefully unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the shipping carton and packing materials for storing or reshipping of the equipment.

> **CAUTION**
>
> AVOID TOUCHING AREAS OF INTEGRATED CIRCUITS; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

Inspect for any shipping damage. If no damage exists, then the module can be prepared for operation according to the following sections of this chapter.

2.3 HARDWARE PREPARATION

This section describes the hardware preparation for the MVME135/136 prior to installation. Observance of this description will ensure the user that all components are properly configured for operation.

Jumper blocks are used to select the various functions and options of the module. Before the module is installed, the user should verify the jumper block configurations and alter the jumpers, as required, for the user's particular system operation. The MVME135/136 has been factory tested and is shipped with factory-installed jumper configurations that are illustrated in Figure 2-1.

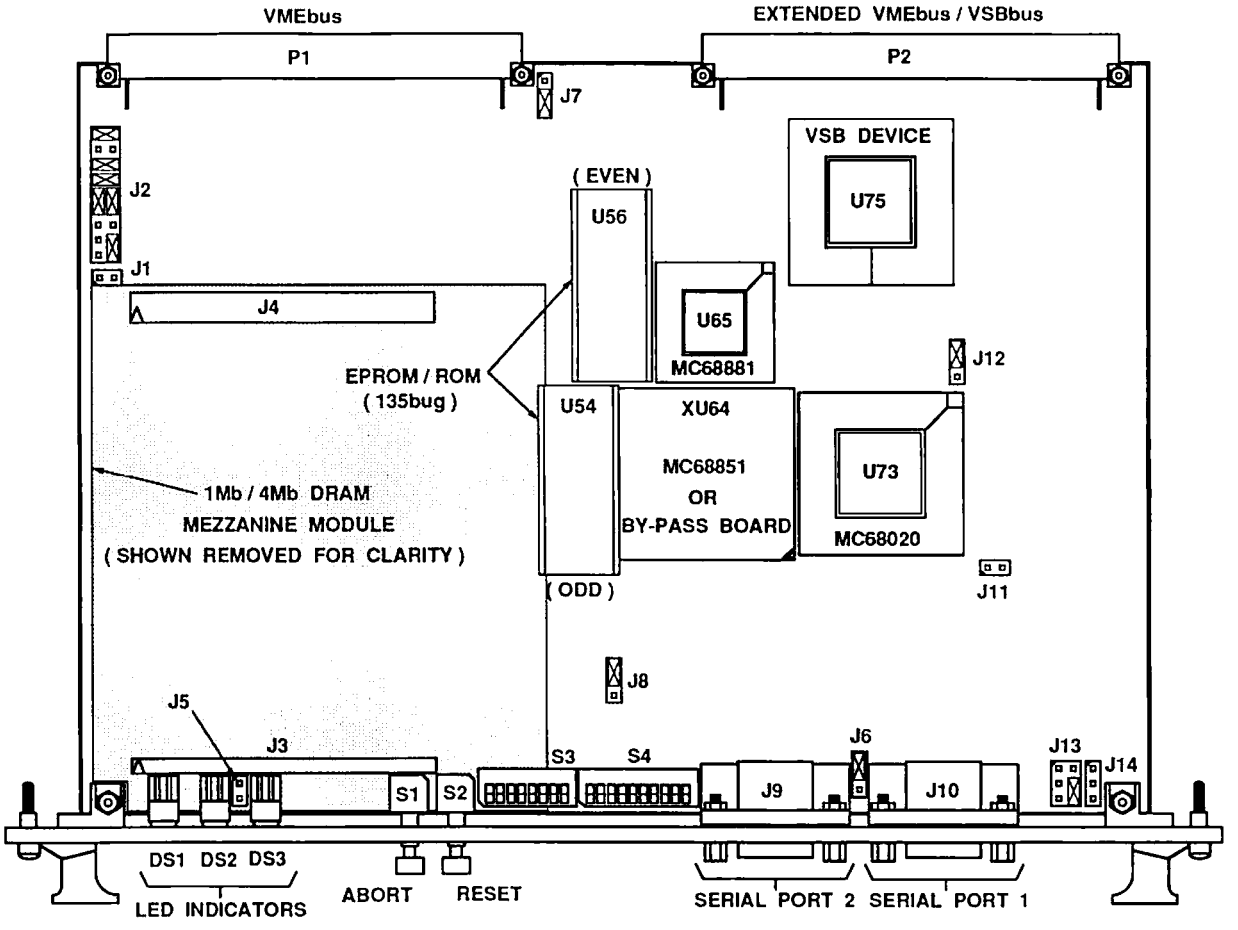


FIGURE 2-1. JUMPER, CONNECTOR, AND SWITCH LOCATION DIAGRAM

Table 2-1 lists the jumper blocks by designation, function, and factory-installed configuration. A more detailed description of these jumper blocks is provided in the following sections.

Four switches (S1, S2, S3, and S4) are located on the MVME135/136's front panel. Switches S1 and S2 are push-buttons and switches S3 and S4 are eight- and ten-positions DIP-type devices, respectively. Three LED indicators (**FAIL**, **HALT**, and **RUN**) are located on the front panel. Refer to Chapter 3 for more detailed information regarding the front panel and the use of these switches and indicators.

The following table lists and describes the MVME135/136 jumper blocks.

TABLE 2-1. JUMPER BLOCK PLACEMENTS

Jumper	Function	Factory Configuration
J1	VMEbus Lock for VSBbus (Disabled)	No jumper installed.
J2	Bus Grant/Request Level Select	J2 (1-2)(5-6)(7-8)(9-11) (1Ø-12)(16-18)
J3	Mezzanine Memory Connect	27-pin connector
J4	Mezzanine Memory Connect	56-pin connector
J5	Factory Test Jumper	No jumper installed.
J6	RAM Acknowledge Mode	J6 (1-2)
J7	ROM Size Select	J7 (2-3)
J8	DRAM Address MUX Timing Select	J8 (1-2)
J9	Serial Port 2 (B) Connect	Front Panel Host Connector
J1Ø	Serial Port 1 (A) Connect	Front Panel Terminal Connector
J11	Timeout Disable (Local and VMEbus)	No jumper installed.
J12	DRAM Cycle Start Mode Select	J12 (1-2)
J13/J14	External Timer Select (Optional)	J13 (4-6)

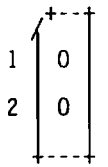
2

2.3.1 VMEbus Lock For VSBbus (J1)

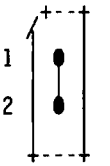
Jumper block J1 allows the RMC* (Read Modify Cycle) signal from the MC68Ø2Ø processor to be asserted on the reserved bus pin P2-B3. This option is provided for users that require access locking of the slave ports that may have a dual bus interface. Normal bus locking occurs on VMEbus without this jumper for single ported VMEbus slave modules. Since this lock feature is not part of the VMEbus specification and since it utilizes a reserved bus pin, use of this feature is recommended only when no other method will suffice. Therefore, J1 is normally not installed.

VMEmodules MVME2Ø4-x and MVME214 have a similar jumper option to allow their use with the lock feature described above. This jumper does not need to be installed if the system software executes only TAS (Test And Set) RMC instruction cycles.

Jumper Block J1
VMEbus Lock (Disabled)
No Jumper Installed
(Factory Setting)



Jumper Block J1
VMEbus Lock (Enabled)
Jumper Installed



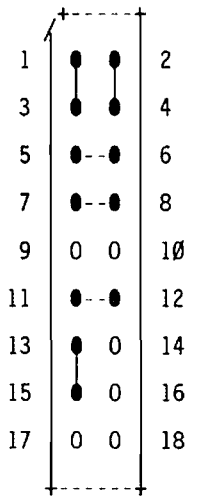
2.3.2 Bus Grant/Request Level Select (J2)

The VMEbus has four prioritized bus request levels (BRØ* through BR3*), each having an associated bus grant daisy-chain. Level 3 has the highest priority while level Ø has the lowest. Jumper block J2 allows the user to select the desired priority level for VMEbus accesses.

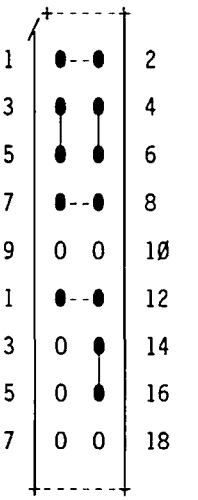
The following configurations illustrate the proper jumpering for each bus arbitration level. If the MVME135/136 is the system controller, then the level 3 configuration is recommended.

NOTE: No other configurations will work properly.

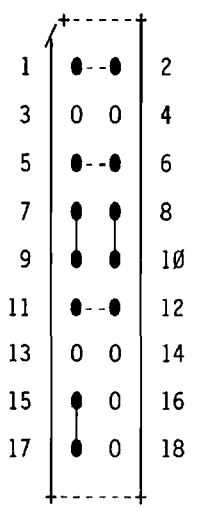
Jumper Block J2
Bus Grant/Request Level Ø



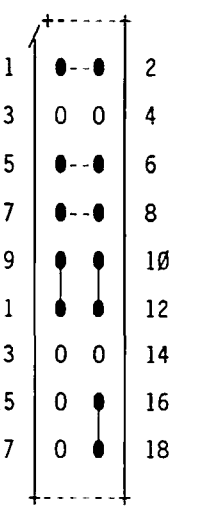
Jumper Block J2
Bus Grant/Request Level 1



Jumper Block J2
Bus Grant/Request Level 2



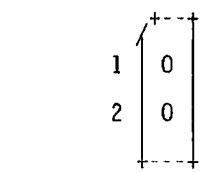
Jumper Block J2
Bus Grant/Request Level 3
(Factory Setting)



2.3.3 Factory Test Jumper (J5)

This jumper block is provided for factory testing purposes only. No jumper cap is installed across jumper J5 pins 1 and 2.

Jumper Block J5
Factory Test Jumper
No Jumper Installed
(Factory Setting)



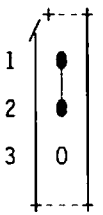
2.3.4 RAM Acknowledge Mode (J6)

The MVME135/136's on-board memory is designed to operate with no wait states when memory speeds are adequate or if parity operation is not required. Jumper block J6 allows for the insertion of one wait state. Parity operation requires that a jumper cap be installed between jumper J6 pins 2 and 3. For optimum performance, care should be taken to ensure that a jumper cap is installed at jumper J6 pins 1 and 2 when parity is not required.

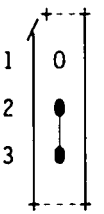
The other case where a jumper cap must be installed at pins 2 and 3 is to accommodate slower DRAM devices. Note that the MVME135A and MVME136A versions utilize slower 1M-bit DRAMs, therefore, jumper J6 is configured for 1 wait state operation. For no wait state operation at 16.67 MHz, a 70-nanosecond memory mezzanine module is required. No wait state operation at 20 MHz requires a 60-nanosecond memory mezzanine module. Upgrading a 16.67 MHz MVME135/136 multiprocessor to a 20 MHz unit requires a 20 MHz oscillator (Y2) and an 80-nanosecond ten tap delay line (DL4).

The MVME135-1 multiprocessor is pre-configured for 20 MHz from the factory. User upgrading of a MVME135 multiprocessor to a MVME135-1 configuration is not recommended.

Jumper Block J6
No Wait State Operation
MVME135/135-1/136 Versions
(Factory Setting)
Parity Mode - NOT Allowed



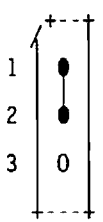
Jumper Block J6
One Wait State Operation
MVME135A/136A Versions
(Factory Setting)
Parity Mode - All Versions



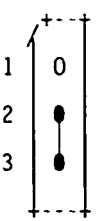
2.3.5 ROM Size Select (J7)

The MVME135/136 accepts two EPROM/ROM devices (28-pin compatible JEDEC units). Jumper block J7 configures sockets U54 (odd byte) and U56 (even byte) for either 32K x 8 (27256) or 64K x 8 (27512) size EPROMs/ROMs. These two device sizes are the only ones supported. These ROM sockets are usually occupied by 135bug, a powerful debug package resident in two 27512 EPROM devices (optional), therefore, a jumper cap is normally installed at jumper J7 pins 2 and 3. The MVME135/135A/136/136A versions (16.67 MHz) require that the EPROM/ROM device access times be no greater than 300 nanoseconds. The MVME135-1 version (20 MHz) requires device times to be 250 nanoseconds or faster.

Jumper Block J7
ROM Size Select
27256 Devices (64Kb)



Jumper Block J7
ROM Size Select
27512 Devices (128Kb)
(Factory Setting)

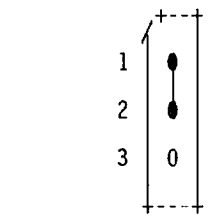


2

2.3.6 DRAM Address Multiplex Select (J8)

The MVME135/136 design requires high performance memory devices. These devices have timing requirements that differ from typical performance DRAMs. Jumper block J8 allows the flexibility to accept timing from a wider variety of DRAM devices and is factory configured.

Jumper Block J8
Normal High Performance
DRAM Multiplex Timing
(Factory Setting)



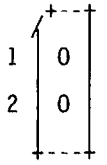
2.3.7 Local/VMEbus Timeout Disable (J11)

Jumper block J11 performs a hardware enable/disable of the local and VMEbus timeout. This jumper is typically used when debugging a new design or isolating a problem where bus errors occur due to accesses to non-existent memory space. Installing a jumper cap across jumper J11 pins 1 and 2 will prevent the cycle from being terminated by a bus error when a slave does not respond. This allows ease in debug since the hung access will remain as long as the cycle is not terminated by a normal acknowledge.

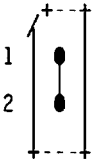
When 135bug is installed, the MVME135/136 will not come up if a jumper cap is installed at J11 pins 1 and 2. This is due to the fact that as a course of normal operation, 135bug initiates bus cycles that may be terminated by a timeout. These cycles include searching for on-board coprocessors (FPCP or PMMU) or sizing of system memory.

If the MVME135/136 is set as the system controller, then VMEbus timeout is not affected by jumper J11, and J11 only controls the local bus timeout. The MVME135/136 will not cause a VMEbus timeout if not set as the system controller, that function is provided to the module that has been configured as VMEbus system controller.

Jumper Block J11
Timeout (Enabled)
No Jumper Installed
(Factory Setting)



Jumper Block J11
Timeout (Disabled)
Jumper Installed



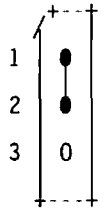
2.3.8 DRAM Cycle Start Mode Select (J12)

The MVME135/136 memory circuit has been designed with the flexibility to operate in synchronous or asynchronous modes. This approach allows for performance gains to local memory when timing strobes are synchronous to the CPU clock. This is the case when operating with a MC68Ø2Ø alone or with the combination of a MC68Ø2Ø and a MC68851 PMMU.

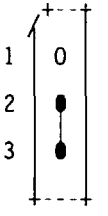
The asynchronous mode allows for timing strobes that do not have any relationship to the MC68Ø2Ø clock. The case where this jumper is installed would be when a Memory Management Board is used (M68KVMMB851).

NOTE: Use of the Memory Management Board is not planned for the MVME135/136. Therefore, jumper block J12 is normally installed in the synchronous mode.

Jumper Block J12
Synchronous Mode Select
(Factory Setting)



Jumper Block J12
Asynchronous Mode Select



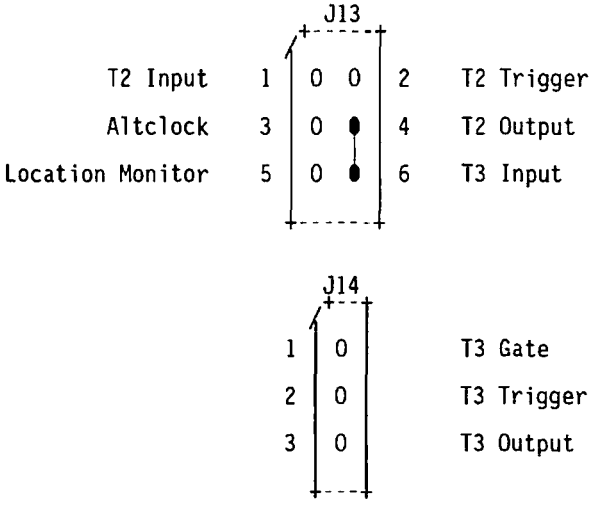
2

2.3.9 External Timer Select (J13,J14)

Jumper blocks J13 and J14 provide the means to access timers 2 and 3 of the Z8Ø36 timer. These jumper blocks are designed to allow an alternate clock source and to allow cascading of the counters. The alternate clock is 125 KHz, derived from the 4 MHz clock that drives the clock input of the Z8Ø36 (divide by 32). The factory setting for J13 and J14 links timers 2 and 3 for diagnostics purposes. Also, the timer 3 output is used as the watch dog timer signal when the system software configures the Z8Ø36 to perform the watch dog timer function. Location monitor 2 is also accessible as an input clock source to the Z8Ø36. This could be set up to count events or perform synchronizing functions.

Some of the jumper pins are not intended to be jumper configured. These provide external access to timer 2's trigger and timer 3's output, trigger, and gate signals. These signals can be connected to other circuitry via wire-wrap or jumper clip connections. Refer to the Zilog Z-CIO (Z8Ø36) Counter/Timer And Parallel I/O Unit Technical Manual for details regarding timer functionality.

Jumper Blocks J13 and J14
External Timer I/O Select
(Optional)
(Factory Setting)



2.4 SERIAL PORT CABLING

2.4.1 DB-9 To DB-25 Cable Connection

The following diagrams indicate the recommended cable connections for connecting the MVME135/136 serial ports to a terminal or modem interface.

135Bug expects the terminal to be attached to serial port one. Serial port 2 may be used as another terminal interface, or as a connection to a host system for upload/download using S-Record format.

Connection To A Terminal

DB-9 Connector		DB-25 Connector
2	to	2
3	to	3
8	to	4
7	to	5
4	to	8
5	to	7
1	to	20
6	to	6

Connection To A Modem

DB-9 Connector		DB-25 Connector
3	to	2
2	to	3
7	to	4
8	to	5
6	to	6
5	to	7
1	to	8
4	to	20

2.5 VME CHASSIS INSTALLATION

When the MVME135/136 has been prepared (configured by the user) as desired, it is ready for system use and can then be installed in a VMEmodule chassis. The following general procedure is recommended for installation of the MVME135/136.

a. Turn all equipment **OFF**.

> **CAUTION**
>
> INSERTING OR REMOVING THE MODULE WHILE POWER IS APPLIED COULD RESULT IN DAMAGE TO MODULE PARTS. AVOID TOUCHING AREAS OF INTEGRATED CIRCUITS; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

b. The MVME135/136 may be installed into any double-high slot on a VMEmodule chassis. Make certain that the intended slot does not have I/O cabling on P2, since that could potentially damage the MVME135/136 VSBbus interface.

c. Using a firm grip on the module, slide the unit into the card slide until the P1 and P2 connectors of the unit align and seat into the backplane sockets. Use a firm, steady pushing motion to install the unit snuggly into the backplane.

d. Turn chassis power **ON**.

CHAPTER 3 - OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides necessary information to use the MVME135/136 in a system configuration. This includes switches, operating controls, indicators, and memory map details found on the MVME135/136 microcomputer.

3.2 FRONT PANEL

The MVME135/136's front panel is illustrated in Figure 3-1. As shown, the red and green LED indicators (**FAIL**, **HALT**, and **RUN**) are located on the front panel. Located below the LED indicators are the two pushbutton switches **ABORT** (S1) and **RESET** (S2). The next two slots are cutouts for accessing the eight-position DIP switch S3 and the ten-position DIP switch S4. This is followed by the slots for the two DB-9 connectors for Serial Ports 1 and 2.

3.2.1 LED Indicators

The MVME135/136 has three LED indicators: **FAIL**, **HALT**, and **RUN**. They are described below. Table 3-1 provides the MVME135/136 module status for all possible combinations of these LEDs.

The **FAIL** indicator (DS1) is a discrete red LED that indicates the status of the BDFAIL software bit.

The **HALT** indicator (DS2) is a discrete red LED that indicates when the halt line of the MPU is asserted. The **HALT** indicator may flicker as a result of normal CPU operation.

The **RUN** indicator (DS3) is a discrete green LED that indicates when the MC68Ø2Ø address strobe is active.

3.2.2 ABORT Switch (S1)

The **ABORT** switch is a momentary type switch that when pressed, causes a Group 3 Level 7 interrupt to the MC68Ø2Ø processor. The 135bug MVME135/136 Debug Monitor, treats **ABORT** as a low level reset. The result being a display of the MC68Ø2Ø registers and/or return of the program control to 135bug.

3.2.3 RESET Switch (S2)

The **RESET** switch is a momentary type switch that when pressed, causes a reset to occur locally. If the MVME135/136 is the system controller (see S4-1), a VMEbus system reset will also occur.

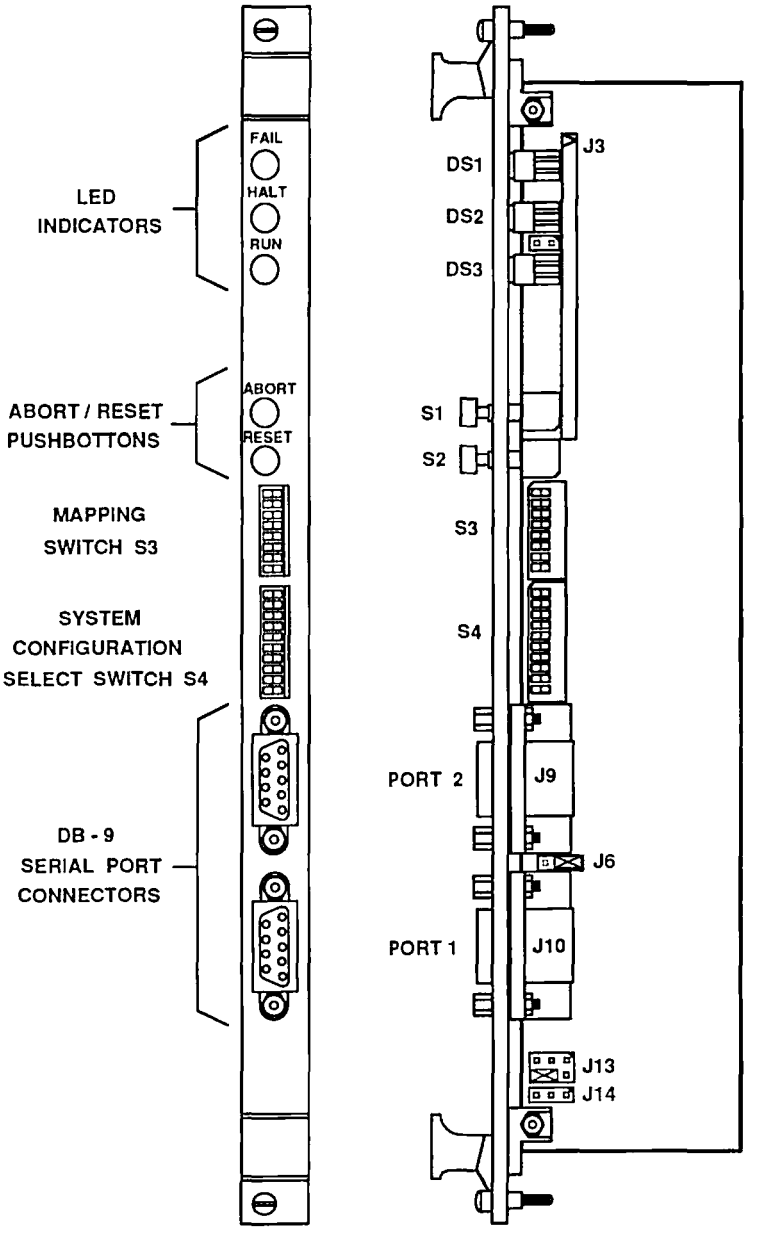


FIGURE 3-1. MVME135/136 FRONT PANEL

TABLE 3-1. MVME135/136 FRONT PANEL LED STATUS

FAIL DS1 Red	HALT DS2 Red	RUN DS3 Green	MVME135/136 Status
OFF	OFF	OFF	No power is applied to the module, or the MPU is not the current local bus master.
OFF	OFF	ON	Normal operation.
OFF	ON	OFF	MPU is halted.
OFF	ON	ON	MPU is running and encountering VMEbus deadlocks and/or PMMU relinquish-and-retry. The frequency of VMEbus deadlocks and/or PMMU relinquish-and-retry determines the intensity of the HALT LED.
ON	OFF	OFF	MPU is not the current local bus master. Also, [BRDFAIL] has not been cleared since reset or has been set by software. The FAIL indicator is also ON if the MVME135/136 is the system controller and SYSFAIL* is detected low on VMEbus.
ON	OFF	ON	[BRDFAIL] has not been cleared since reset or has been set by software. The FAIL indicator is also ON if the MVME135/136 is the system controller and SYSFAIL* is detected low on VMEbus.
ON	ON	OFF	MPU is halted and [BRDFAIL] has not been cleared since reset or has been set by software. The FAIL indicator is also ON if the MVME135/136 is the system controller and SYSFAIL* is detected low on VMEbus.
ON	ON	ON	MPU is running and encountering VMEbus deadlocks and/or PMMU relinquish-and-retry. The frequency of VMebus deadlocks and/or PMMU relinquish-and-entry determines the intensity of the HALT LED. Also, [BRDFAIL] has not been cleared since reset or has been set by software.

3.2.4 Mapping Switch (S3)

Switch S3 is the slave resource mapping switch. It is an eight-position piano type DIP switch that maps the memory and MPCSR on the VMEbus. Mapping options for the MVME135/135-1/136 occurs on 1Mb boundaries. Mapping is possible from ØMb to 32Mb. Mapping options for the MVME135A/136A occur on 4Mb boundaries. Mapping is therefore, possible from ØMb to 128Mb for the MVME135A/136A. However, each switch setting defines 4Mb rather than 1Mb.

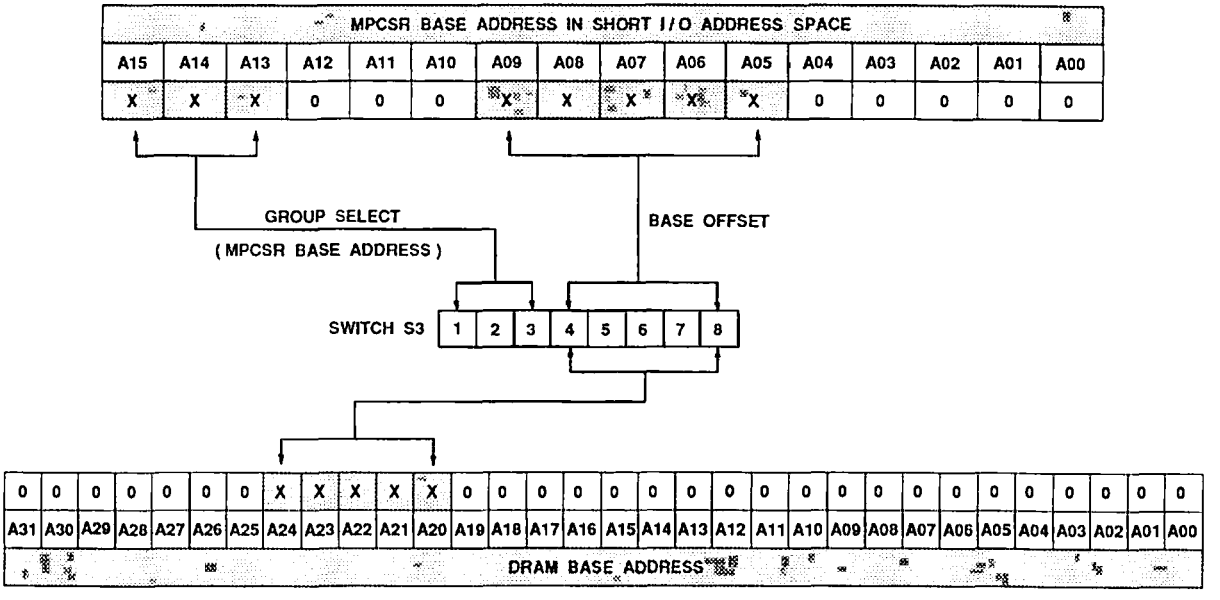
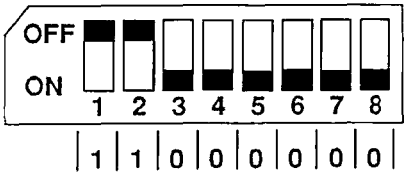


FIGURE 3-2. MVME135/135-1/136 SLAVE ACCESS ADDRESSING

The following illustrations provide various examples of MPCSR and DRAM base addressing (MVME135/135-1/136 versions only).

Example 1: (MVME135/135-1/136 versions only).



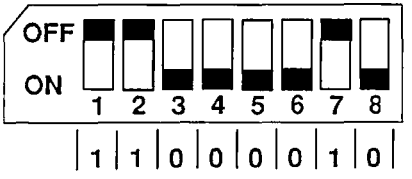
Switch S3
Mapping Switch
(Factory Configuration)

(NOTE: ON is Ø, OFF is 1)

MPCSR (Located In VMEbus Short I/O Space $FFFF XXXX)
Base Addr = 1 1 Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø ØØØØ = $CØØØ

DRAM
Base Addr = ØØØØ Ø Ø Ø Ø Ø Ø Ø Ø ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ = $ØØØØ ØØØØ

Example 2: (MVME135/135-1/136 versions only).



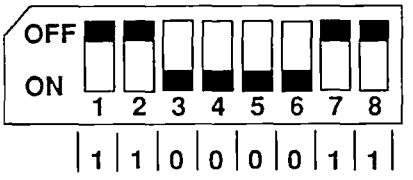
Switch S3
Mapping Switch

(NOTE: ON is Ø, OFF is 1)

MPCSR
Base Addr = 1 1 Ø Ø Ø Ø Ø Ø 1 Ø Ø Ø ØØØØ = $CØ4Ø

DRAM
Base Addr = ØØØØ Ø Ø Ø Ø Ø Ø 1 Ø ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ = $ØØ2Ø ØØØØ

Example 3: (MVME135/135-1/136 versions only).



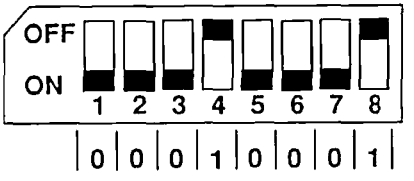
Switch S3
Mapping Switch

(NOTE: ON is Ø, OFF is 1)

MPCSR
Base Addr = 1 1 Ø Ø Ø Ø Ø Ø Ø 1 1 Ø ØØØØ = $CØ6Ø

DRAM
Base Addr = ØØØØ Ø Ø Ø Ø Ø Ø 1 1 ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ = $ØØ3Ø ØØØØ

Example 4: (MVME135/135-1/136 versions only).



Switch S3
Mapping Switch

(NOTE: ON is Ø, OFF is 1)

MPCSR
Base Addr = Ø Ø Ø Ø Ø Ø 1 Ø Ø Ø 1 Ø ØØØØ = $Ø22Ø

DRAM
Base Addr = ØØØØ Ø Ø Ø 1 Ø Ø Ø 1 ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ = $Ø11Ø ØØØØ

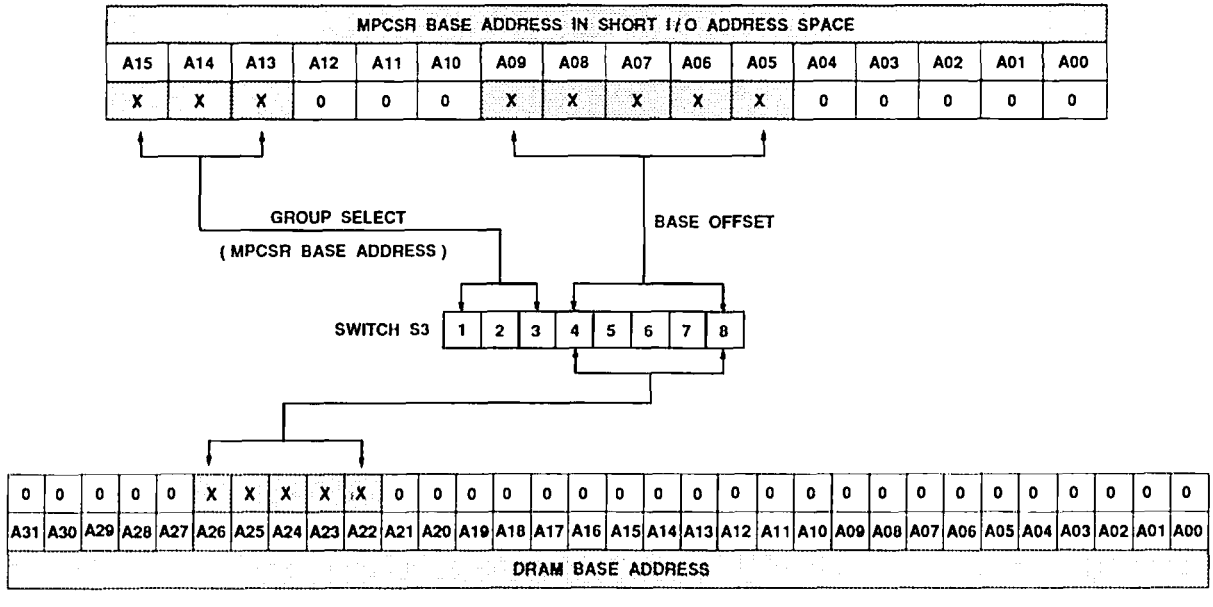
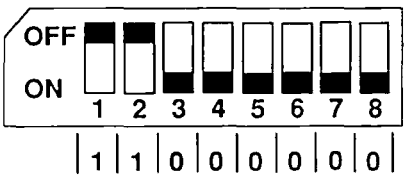


FIGURE 3-3. MVME135A/136A SLAVE ACCESS ADDRESSING

The following illustrations provide various examples of MPCSR and DRAM base addressing (MVME135A/136A versions only).

Example 1: (MVME135A/136A versions only).



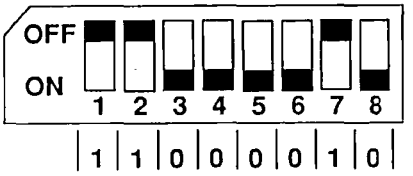
Switch S3
Mapping Switch
(Factory Configuration)

(NOTE: ON is Ø, OFF is 1)

MPCSR (Located In VMEbus Short I/O Space $FFFF XXXX)
Base Addr = 1 1 Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø ØØØØ = $CØØØ

DRAM
Base Addr = ØØØØ Ø Ø Ø Ø Ø Ø Ø Ø ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ = $ØØØØ ØØØØ

Example 2: (MVME135A/136A versions only).



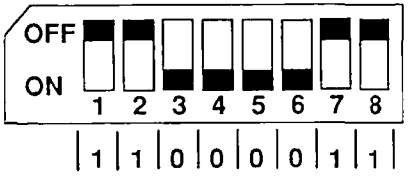
Switch S3
Mapping Switch

(NOTE: ON is Ø, OFF is 1)

MPCSR
Base Addr = 1 1 Ø Ø Ø Ø Ø Ø Ø 1 Ø Ø ØØØØ = $CØ4Ø

DRAM
Base Addr = ØØØØ Ø Ø Ø Ø 1 Ø Ø Ø ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ = $ØØ8Ø ØØØØ

Example 3: (MVME135A/136A versions only).



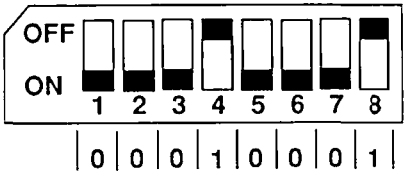
Switch S3
Mapping Switch

(NOTE: ON is Ø, OFF is 1)

MPCSR
Base Addr = 1 1 Ø Ø Ø Ø Ø Ø Ø 1 1 Ø ØØØØ = $CØ6Ø

DRAM
Base Addr = ØØØØ Ø Ø Ø Ø 1 1 Ø Ø ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ = $ØØCØ ØØØØ

Example 4: (MVME135A/136A versions only).



Switch S3
Mapping Switch

(NOTE: ON is Ø, OFF is 1)

MPCSR
Base Addr = Ø Ø Ø Ø Ø Ø 1 Ø Ø Ø 1 Ø ØØØØ = $Ø22Ø

DRAM
Base Addr = ØØØØ Ø 1 Ø Ø Ø 1 Ø Ø ØØØØ ØØØØ ØØØØ ØØØØ ØØØØ = $Ø44Ø ØØØØ

3.2.5 System Configuration Switch (S4)

Switch S4 is a ten-position piano type DIP switch that provides the following functions as defined by 135bug (refer to the 135bug manual for a more detailed description). Note that S4-1 and S4-2 are implemented in hardware and that the other eight positions are implemented in the 135bug monitor.

Switch S4
System Configuration Select
(Factory Configuration)

(NOTE: ON is Ø, OFF is 1)

S4-1Ø: OFF= Autoboot enabled.
ON = Autoboot disabled.

S4-9 : OFF= MP bits enabled.
ON = MP bits disabled.

S4-8 : OFF= VSBbus disabled.
ON = VSBbus enabled.

S4-7 : OFF= VSB not system controller.
ON = VSB is system controller.

S4-6 : OFF= 24-bit VMEbus addr width.
ON = 32-bit VMEbus addr width.

S4-5 : OFF= 16-bit VMEbus data width.
ON = 32-bit VMEbus data width.

S4-4 : ON = { 135bug executes locally,
S4-3 : ON DRAM mapped at $Ø.

S4-4 : OFF= { 135bug executes locally,
S4-3 : ON DRAM mapped at $FFXØØØØØ.

S4-4 : ON = { 135bug executes over the
S4-3 : OFF VMEbus BASE.

S4-4 : OFF= { 135bug executes in first
S4-3 : OFF off-board VMEbus memory.

S4-2 : OFF= RESET/ABORT disabled.
ON = RESET/ABORT enabled.

S4-1 : OFF= VME not system controller.
ON = VME is system controller.

3.3 MEMORY MAP AND MAP DECODER

At the beginning of each MPU cycle, the map decoder determines what kind of cycle takes place and which device or function is selected within that cycle type. Cycle types are determined by the function code lines FC2 through FCØ, which are driven by the MC68Ø2Ø MPU. The cycle types and the devices that respond are listed in Table 3-2.

TABLE 3-2. FUNCTION CODE ASSIGNMENTS

FC2	FC1	FCØ	Cycle Type	Responding Board Devices/Functions
Ø	Ø	Ø	Reserved	None (causes local timeout).
Ø	Ø	1	User Data	All except the interrupt handler, MC68851, and MC68881.
Ø	1	Ø	User Program	All except the interrupt handler, MC68851, and MC68881.
Ø	1	1	Reserved	None (causes local timeout).
1	Ø	Ø	Reserved	None (causes local timeout).
1	Ø	1	Supervisory Data	All except the interrupt handler, MC68851, and MC68881.
1	1	Ø	Supervisory Program	All except the interrupt handler, MC68851, and MC68881.
1	1	1	CPU (IACK)	VMEbus interrupt and the local interrupt handler.
1	1	1	CPU Coprocessor	MC68851 and MC68881.

3.3.1 MVME135/135-1/136 Main Memory Map

The memory map of devices that respond in User Data, User Program, Supervisory Data, and Supervisory Program spaces is shown in the following table.

TABLE 3-3. MVME135/135-1/136 MAIN MEMORY MAP

Physical Address Range (Hexadecimal)	Devices Accessed	Port Size	Size (Bytes)	Notes
00000000 - 000FFFFF	VMEbus A32/A24/VSB or Optionally On-board DRAM	D32/D16	1Mb	1
00100000 - 00FFFFFF	VMEbus A32/A24/VSB	D32/D16	15Mb	---
01000000 - FFDFFFFF	VMEbus/A32/VSB	D32	4Gb	---
FFE00000 - FFEFFFFF	On-board DRAM	D32	1Mb	---
FFF00000 - FFF1FFFF	On-board ROM/PROM/EPROM	D16	128Kb	---
FFF20000 - FFF9FFFF	Not Used	N/A	512Kb	---
FFFA0000 - FFFAFFFF	MVSB2400 (VSB) Gate Array	D16	64Kb	---
FFFB0000 - FFFB002F	Z8036 Timer (STAT1, CNT1)	D08	64Kb	---
FFFB0030 - FFFB0031	Not Used	N/A	2b	---
FFFB0032	STAT2	D08	1b	---
FFFB0033 - FFFB0037	Not Used	N/A	4b	---
FFFB0038	CNT2	D08	1b	---
FFFB0039	CNT3	D08	1b	---
FFFB003A	CNT4	D08	1b	---
FFFB003B	CNT5	D08	1b	---
FFFB003C - FFFB003F	Not Used	N/A	4b	---
FFFB0040 - FFFB004F	MC68681 Serial Controller	D08	16b	---
FFFB0050 - FFFB005F	Not Used	N/A	16b	---
FFFB0060 - FFFB007F	MPCSR Registers	D08	32b	---
FFFB0080 - FFFBFFFF	Not Used	N/A	64Kb	---
FFFC0000 - FFFEFFFF	Reserved	N/A	128Kb	---
FFFF0000 - FFFFFFFF	VMEbus A16 Short I/O Space	D16	64Kb	---

NOTES: When the option 0 bit (OPT0) in Control Register 5 (CNT5) is set, then local DRAM appears in this address space. When OPT0 is cleared, this address space is decoded as VMEbus A32/A24 or VSB (refer to section 4.15.2).

3.3.2 MVME135A/136A Main Memory Map

The memory map of devices that respond in User Data, User Program, Supervisory Data, and Supervisory Program spaces is shown in the following table.

TABLE 3-4. MVME135A/136A MAIN MEMORY MAP

Physical Address Range (Hexadecimal)	Devices Accessed	Port Size	Size (Bytes)	Notes
00000000 - 003FFFFF	VMEbus A32/A24/VSB or Optionally On-board DRAM	D32/D16	4Mb	1
00400000 - 00FFFFFF	VMEbus A32/A24/VSB	D32/D16	12Mb	---
01000000 - FFDFFFFF	VMEbus/A32/VSB	D32/D16	4Gb	---
FF800000 - FFBFFFFF	On-board DRAM	D32	4Mb	---
FFC00000 - FFEFFFFF	Not Used	N/A	3Mb	---
FFF00000 - FFF1FFFF	On-board ROM/PROM/EPROM	D16	128Kb	---
FFF20000 - FFF9FFFF	Not Used	N/A	1Mb	---
FFFA0000 - FFFAFFFF	MVSB2400 (VSB) Gate Array	D16	64Kb	---
FFFB0000 - FFFB002F	Z8036 Timer (STAT1, CNT1)	D08	64Kb	---
FFFB0030 - FFFB0031	Not Used	N/A	2b	---
FFFB0032	STAT2	D08	1b	---
FFFB0033 - FFFB0037	Not Used	N/A	4b	---
FFFB0038	CNT2	D08	1b	---
FFFB0039	CNT3	D08	1b	---
FFFB003A	CNT4	D08	1b	---
FFFB003B	CNT5	D08	1b	---
FFFB003C - FFFB003F	Not Used	N/A	4b	---
FFFB0040 - FFFB004F	MC68681 Serial Controller	D08	16b	---
FFFB0050 - FFFB005F	Not Used	N/A	16b	---
FFFB0060 - FFFB007F	MPCSR Registers	D08	32b	---
FFFB0080 - FFFBFFFF	Not Used	N/A	64Kb	---
FFFC0000 - FFFEFFFF	Reserved	N/A	128Kb	---
FFFF0000 - FFFFFFFF	VMEbus A16 Short I/O Space	D16	64Kb	---

NOTES: When the option 0 bit (OPT0) in Control Register 5 (CNT5) is set, then local DRAM appears in this address space. When OPT0 is cleared, this address space is decoded as VMEbus A32/A24 or VSB (refer to section 4.15.2).

CHAPTER 4 - FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides the overall block diagram level description for the MVME135/136 module. The general description provides an overview of the module, followed by a detailed description of each section of the module. The simplified block diagram for the MVME135/135-1/136 is illustrated in Figure 4-1 and for the MVME135A/136A in Figure 4-2.

4.2 GENERAL DESCRIPTION

The MVME135/136 is a MC68Ø2Ø microprocessor-based module. The module incorporates an MC68Ø2Ø, a 32-bit address and data microprocessor, a high level multiprocessor CSR, and 1Mb (MVME135/135-1/136 versions) or 4Mb (MVME135A/136A versions) of fast DRAM. Other features include a Paged Memory Management Unit (PMMU), a Floating Point Coprocessor (FPCP), an A32/D32 VMEbus interface, a secondary bus interface (VSBbus), two RS-232C serial ports, two 16-bit timers, two 28-pin ROM/PROM/EPROM sockets, VMEbus system controller functions, a seven-level VMEbus interrupt handler, and a dual ported, high-level communication interface called the Multiprocessor Control and Status Registers (MPCSR).

4.2.1 Data Bus Structure

The data bus structure on the MVME135/136 module is arranged to accommodate the 8-bit, 16-bit, 32-bit, and 16/32-bit ports that reside on the module. The 8-bit ports are connected to data lines D24 through D31 of the local bus, the 16-bit ports are connected to data lines D16 through D31 of the local bus, and the 32-bit ports are connected to data lines DØØ through D31 of the local bus.

4.2.2 Memory Map

The operation of the map decoder and tables providing the main memory maps of the MVME135/136 modules are provided in Chapter 3.

4.2.3 Timing

General characteristics of the MVME135/136 module timing are given in the following sections and Table 4-1.

4.2.4 MVME135/135-1/136 DRAM Cycle Times

MPU accesses to the on-board DRAM require a minimum of three MPU clock cycles. A clock cycle at 16.67 MHz is 6Ø nanoseconds and at 2Ø.ØØ MHz is 5Ø nanoseconds.

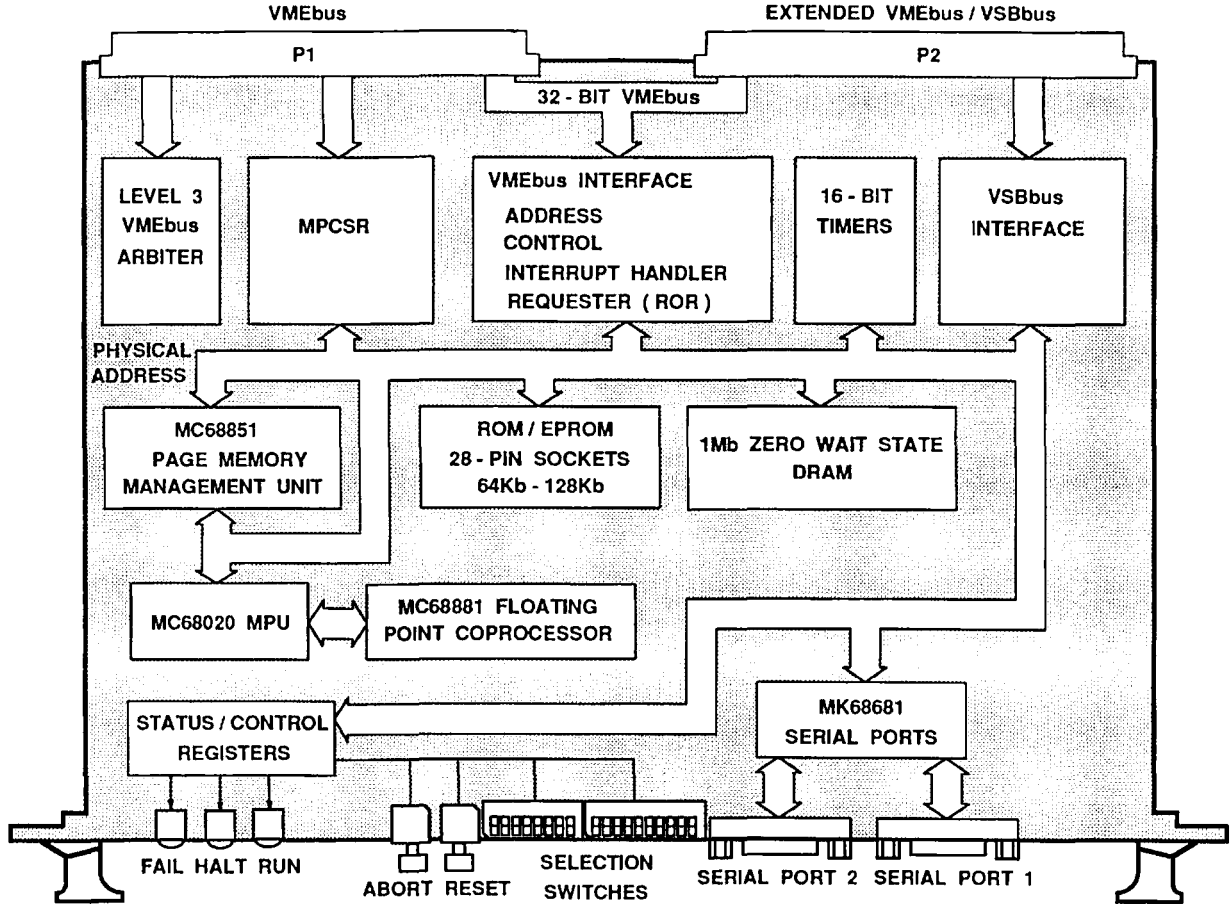


FIGURE 4-1. MVME135/135-1/136 BLOCK DIAGRAM

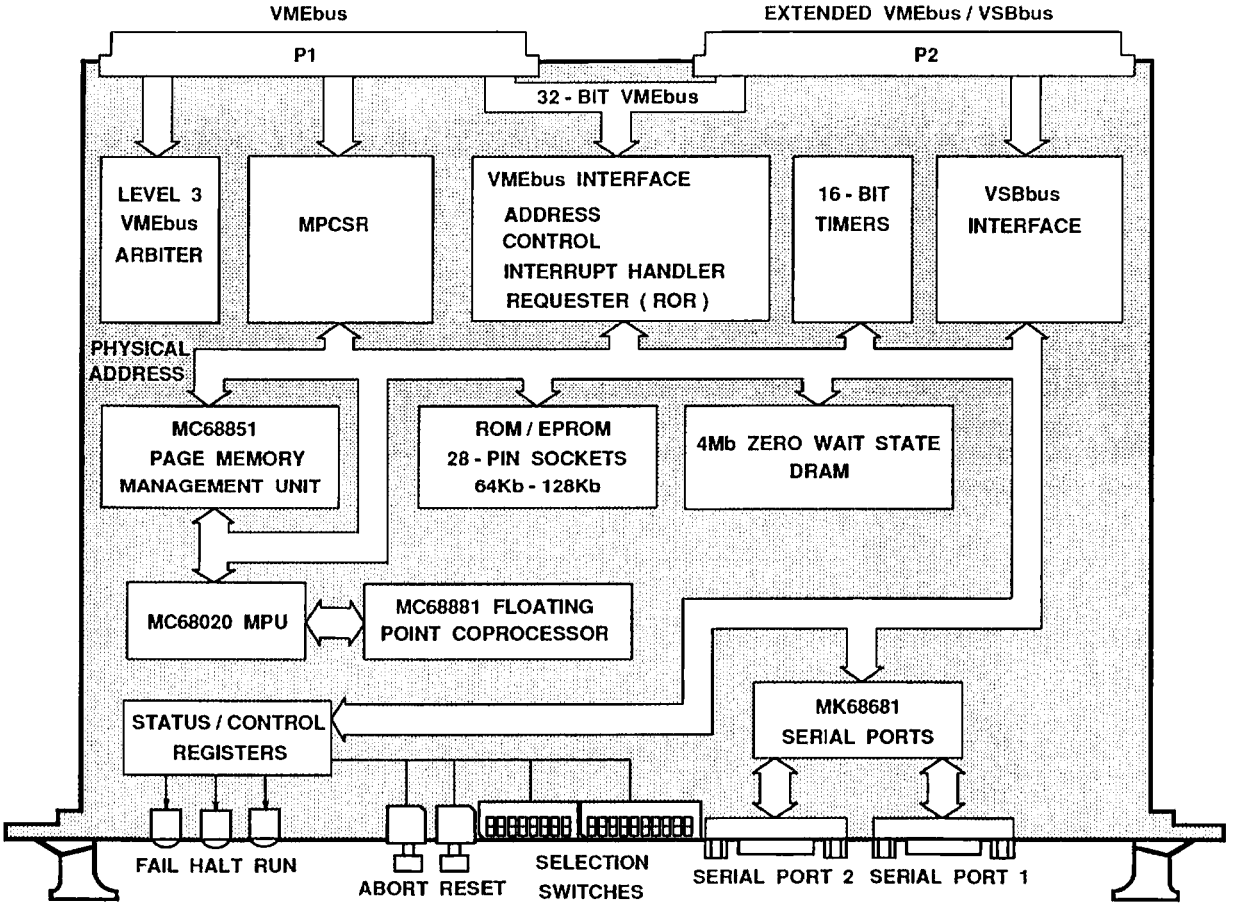


FIGURE 4-2. MVME135A/136A BLOCK DIAGRAM

The addition of the PMMU adds one wait cycle (three minimum + one wait cycle). Parity adds one wait cycle to the total number of MPU clock cycles, (four total for the MVME135/135-1 and five total for the MVME136).

4.2.5 MVME135A/136A DRAM Cycle Times

MPU accesses to the on-board DRAM require four MPU clock cycles (three minimum + one wait cycle) for slower memories. A clock cycle at 16.67 MHz is 60 nanoseconds.

The addition of a PMMU adds one wait cycle (three minimum + one wait cycle). Parity does not add additional wait cycles on the MVME135A/136A.

TABLE 4-1. MVME135/136 TIMING

ACCESS SEQUENCE	MVME135 (16.67 MHz)		MVME135-1 (20.00 MHz)		MVME135A (16.67 MHz)		MVME136 (16.67 MHz)		MVME136A (16.67 MHz)	
	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ
MPU TO LOCAL DRAM (NO PARITY)	3	3	3	3	4	4	4	4	5	5
MPU TO LOCAL DRAM (PARITY ENABLED)	4	4	4	4	4	4	5	5	5	5
MPU TO LOCAL ROM/ PROM/EPROM	--	8	--	8	--	9	--	9	--	9
VMEbus TO LOCAL DRAM	11	10	11	11	11	10	12	11	12	11
MPU TO GLOBAL DRAM OVER VSB (MVME204-2F)	8	8	9	9	8	8	9	9	9	9
MPU TO GLOBAL DRAM OVER VMEbus (MVME204-2F)	9	10	12	14	9	10	10	11	10	11
ACCESS SEQUENCE	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ
	MVME135 (16.67 MHz)		MVME135-1 (20.00 MHz)		MVME135A (16.67 MHz)		MVME136 (16.67 MHz)		MVME136A (16.67 MHz)	
ALL TIMES ARE TOTAL NUMBER OF MC68020 CLOCK CYCLES.										

4.2.6 ROM/PROM/EPROM/EEPROM Cycle Times

All ROM/PROM/EPROM/EEPROM accesses require eight MPU clock cycles when NO PMMU is installed, and nine MPU clock cycles to complete when the PMMU is installed.

4.2.7 VMEbus Cycle Times

The following formula assumes that the MVME135/136 module is the current VMEbus master and that all slaves have released DTACK* and BERR*. The time from the activation of DSØ*/DS1* to the activation of DTACK* is Tac in nanoseconds, T is the MPU clock period in nanoseconds, and N is the total number of MPU clock periods required to complete a VMEbus cycle. N must always be rounded up to the next integer.

For read accesses	N = 5 + [Tac / T]	typical
For write accesses	N = 6 + [Tac / T]	typical

The following formula assumes that the MVME135/136 module is NOT the current VMEbus master, but that it is the system controller. Also, it assumes that all previous slaves have released DTACK* and/or BERR* when the MVME135/136 module receives VMEbus mastership. The delay from BR3* low (driven by MVME135/136) to BBSY* high and AS* high is Tr. The time from the activation of DSØ*/DS1* to the activation of DTACK* is Tac in nanoseconds, T is the MPU clock period in nanoseconds, and N is the total number of MPU clock periods required to complete a VMEbus cycle. N must always be rounded to to the next integer.

For read accesses	N = 6 + [Tac + Tr) T]	typical
For write accesses	N = 7 + [Tac + Tr) T]	typical

The following formula assumes that the MVME135/136 module is NOT the current VMEbus master, and it is NOT the system controller. Also, it assumes that all previous slaves have released DTACK* and/or BERR* when the MVME135/136 receives VMEbus mastership. The delay from BRX* low (driven by MVME135/136) to BGXIN* low and AS* high is Tg. The time from the activation of DSØ*/DS1* to the activation of DTACK* is Tac in nanoseconds, T is the MPU clock period in nanoseconds, and N is the total number of MPU clock periods required to complete a VMEbus cycle. N must always be rounded to to the next integer.

For read accesses	N = 6 + [Tac + Tg) T]	typical
For write accesses	N = 7 + [Tac + Tg) T]	typical

4.2.8 VMEbus Arbitration Time

When the MVME135/136 module is configured as the system controller and is not requesting VMEbus mastership, the delay from BBSY* high and BR3* low to BG3OUT* low is 35 nanoseconds typical and 5Ø nanoseconds maximum.

When the MVME135/136 module is not configured as the system controller and is not requesting VMEbus mastership, the delay from BGXIN* low to BGXOUT* low is 45 nanoseconds typical and 60 nanoseconds maximum.

4.3 MC68020 MPU

The MC68020 is the main microprocessor of the MVME135/136. The MVME135/135A/136/136A versions utilize the MC68020 operating at a fixed operating speed of 16.67 MHz. On the MVME135-1 version, the fixed operating frequency is 20.00 MHz.

The MC68020 is a full 32-bit microprocessor with 32-bit registers, 32-bit data, and 32-bit addresses. Its advanced architecture, enhanced addressing modes, and on-chip cache are advancements over its predecessors in the MC68000 family of chips. The 32-bit data and address architecture of the MC68020 fully supports applications in environments based on an asynchronous, non-multiplexed bus such as the VMEbus. The microprocessor includes control inputs and an internal multiplexer that enable it to perform automatic port sizing during each bus cycle. Use of this mechanism facilitates the transfer of one, two, or four byte operands to and from external devices of any data port width effectively eliminating all alignment restrictions. Refer to the MC68020UM/AD User's Manual for a detailed description of its operation.

4.4 MC68881 FPCP

The MVME135/135A/136/136A versions are equipped with a 16.67 MHz MC68881 Floating-Point Coprocessor. On the MVME135-1 version, the MC68881 operates at 20.00 MHz. The MC68881 extends the main MPU integer data processing capabilities. It does this by providing a very high performance binary floating-point arithmetic unit and a set of floating-point data registers that are utilized in a manner analogous to the use of the integer data registers. The MC68881 instruction set is a natural extension to that of all earlier members of the M68000 family, and supports all of the addressing modes of the host MPU. Refer to the MC68881UM/AD User's Manual for a detailed description of its operation.

4.5 MC68851 PMMU

Memory management for the MVME136 and MVME136A is provided by a 16.67 MHz MC68851. The MC68851 is a high performance Paged Memory Management Unit (PMMU) designed to efficiently support a demand paged virtual memory environment with the MC68020 32-bit microprocessor. The PMMU is optimized for very fast logical-to-physical address translations, to provide a comprehensive access control and protection mechanism, and to provide extensive support for paged virtual systems. Operating as a coprocessor to the

MC68Ø2Ø, the PMMU provides a logical extension to the program control and processing abilities of the main processor. It does this by providing a set of translation, protection, and breakpoint registers that control operation of the memory management mechanism. These registers are utilized in a manner similar to the use of any internal processor register.

4.6 DEBUG MONITOR FIRMWARE

The MVME135bug Debug Monitor firmware package is optionally available for use with any of the MVME135/136 modules. This firmware offers 32 debug capability, upload/download, disk bootstrap commands, a one line assembler/disassembler with full MC68881 support, as well as a full set of on-board diagnostics. Refer to the 135bug Diagnostic/Debug Package User's Manual for a detailed description of its operation.

4.7 VME SUBSYSTEM BUS (VSBbus)

The VME Subsystem Bus (VSBbus is a subset of the VMEbus) is a local extension bus. It allows a processor board to access additional memory and I/O over a local bus, removing traffic from the global bus and improving the total throughput of the system. The VSBbus interface occupies 64 I/O pins on connector P2 and utilizes the multiplexing of address and data in order to accommodate full 32-bit functionality, along with appropriate control signals, within the 64-pin allotment.

On the MVME135/136 modules, VSBbus is implemented through the use of the MVSB24ØØ. The MVSB24ØØ is a 132-pin gate array subset of the VSBbus specification in a PGA package. The MVSB24ØØ provides most of the functionality required to support a master VSBbus interface using one VLSI device and a few external gates, and contains most of the bus drivers for the VSBbus and all of the address and data multiplexing circuits. Refer to the MVSB24ØØ VSBchip User's Manual for a detailed description of its operation. Although the MVSB24ØØ VSBchip has a slave mode, the MVME135/136 does not support VSBbus slave accesses.

4.8 DYNAMIC RAM

The MVME135/136's dynamic random access memory uses 256K x 1 or 1M x 1 dynamic RAMs surface mounted on a mezzanine board, providing a total of 1Mb to 4Mb of local DRAM with optional parity. It is accessible from the MC68Ø2Ø, the refresh circuitry, and the VMEbus, each of which requests and is granted use of the DRAM by an on-board arbiter.

The on-board DRAM is designed to operate at zero wait cycles at both 16.67 MHz and 2Ø.ØØ MHz without parity and a bypass board installed

in the PMMU socket. Memory management, parity and the processor clock frequency all affect the speed of the local DRAM and VMEbus accesses.

Because the local address and data buses are used to access the on-board DRAM, any device that uses the DRAM must become the local bus master. An on-board arbiter handles this using the MC68Ø2Ø arbitration logic to transfer local bus mastership from the current master to the next. During normal operation, the MC68Ø2Ø is the local master. When the VMEbus requires use of the DRAM, the arbiter requests, and is granted the local bus by the MC68Ø2Ø. At this time, memory timing circuitry executes one DRAM cycle (read or write) and relinquishes the local bus mastership, after which, the MC68Ø2Ø resumes local bus mastership. If a refresh cycle is required, the current bus cycle is stretched, eliminating the need for the refresh circuitry to obtain local bus mastership.

The user can select the address at which the on-board DRAM appears from the VMEbus by setting S3 (an 8-position DIP switch). This switch is used not only to determine the address of the DRAM, but is also used to determine the location at which the Multiprocessing Control/Status Register (MPCSR) is located. This mapping is explained in detail in section 4.16 and mapping examples are provided in section 3.2.4.

On-board DRAM responds to a VMEbus access only when address modifier lines AMØ through AM5 indicate extended or standard, privileged or non-privileged data or program space.

4.9 FUNCTION CODE ASSIGNMENTS

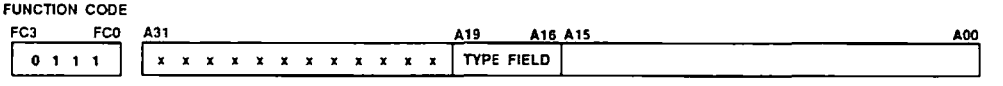
Decoding logic on the MVME135/136 module determines the supervisor or user processor state and type of address space assignments controlled, for each cycle, by the collective state of the MC68Ø2Ø Function Code pins (FC2, FC1, and FCØ). In addition to the standard supervisor or user processor state and type of address space, the MVME135/136 modules use the CPU space assignment to implement coprocessor, interrupt handling, and other functions. Refer to Table 4-2 for the function code assignments.

4.1Ø MVME135/136 USE OF CPU SPACE

The MVME135/136 devices and functional blocks respond to four types of CPU space accesses (FC2-FCØ = 111): breakpoint (MC68851), access level (MC68851), coprocessor (MC68851 and MC68881), and interrupt acknowledge. The type of access determined by A19 through A16 is illustrated in Figure 4-3.

TABLE 4-2. FUNCTION CODE ASSIGNMENTS

FC2	FC1	FC0	CYCLE TYPE	RESPONDING MVME135/136 MODULE DEVICES/FUNCTIONS
0	0	0	RESERVED	NONE (CAUSES LOCAL TIMEOUT).
0	0	1	USER DATA	ALL EXCEPT THE INTERRUPT HANDLER, THE MC68851, AND THE MC68881.
0	1	0	USER PROGRAM	ALL EXCEPT THE INTERRUPT HANDLER, THE MC68851, AND THE MC68881.
0	1	1	RESERVED	NONE (CAUSES LOCAL TIMEOUT).
1	0	0	RESERVED	NONE (CAUSES LOCAL TIMEOUT).
1	0	1	SUPERVISORY DATA	ALL EXCEPT THE INTERRUPT HANDLER, THE MC68851, AND THE MC68881.
1	1	0	SUPERVISORY PROGRAM	ALL EXCEPT THE INTERRUPT HANDLER, THE MC68851, AND THE MC68881.
1	1	1	CPU (IACK)	THE LOCAL HANDLER AND THE VMEbus INTERRUPT.
1	1	1	CPU COPROCESSOR	THE MC68851 AND MC68881.



CPU SPACE TYPE FIELD (A19 - A16)	CPU SPACE TRANSACTION
0 0 0 0	BREAKPOINT ACKNOWLEDGE
0 0 0 1	ACCESS LEVEL CONTROL
0 0 1 0	COPROCESSOR COMMUNICATIONS
1 1 1 1	INTERRUPT ACKNOWLEDGE

FIGURE 4-3. CPU SPACE TYPE FIELD ENCODING

4.10.1 MC68851 Breakpoint Support

In order to simplify debugging and emulation for system developers, the designers of the MC68851 took full advantage of an MC68020 extension to the M68000 family instruction set, the BreaKPoinT instruction BKPT, and the supporting breakpoint acknowledge bus cycle. The three low order bits of the instruction are used as immediate data that can be transmitted by the breakpoint acknowledge bus cycle to an external device to signal that the processor has encountered a breakpoint and requires further direction. Since the three low order bits represent data, the processor can respond to

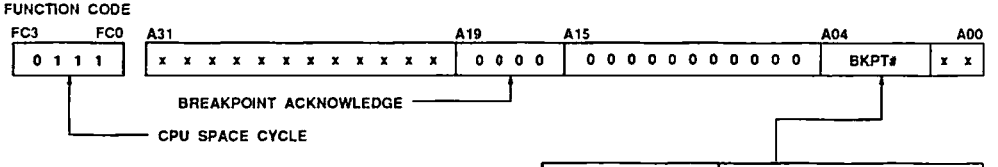
eight opcodes ($4848 to $484F) thus providing a means of initiating eight different types of breakpoint processing.

4.10.2 MC68851 Breakpoint Operation

During MVME135/136 operation after the processor fetches a breakpoint opcode, it performs a breakpoint acknowledge cycle in which, it sets the function code lines to indicate CPU space and sets address lines A16 through A19 to indicate the breakpoint acknowledge type of CPU space. It also decodes the three low order bits of the opcode and places the obtained breakpoint number on address lines A2 through A4.

On decoding the address lines when it begins its acknowledge cycle, the MC68851 has two options. It can force the processor to initiate illegal instruction exception processing by asserting the BERR signal or it can obtain from one of its eight breakpoint register pairs a replacement opcode corresponding to the breakpoint number, place this opcode on the processor data bus and assert the DSACK signal.

The processor then replaces the breakpoint opcode in its instruction pipeline with the new opcode supplied by the MC68851 and continues execution. The systems programmer has full discretion to design the actions initiated by execution of the replacement opcode. The breakpoint acknowledge cycle address bus decoding by the MC68851 is illustrated in Figure 4-4. The bits marked "x" are zero filled by the CPU and ignored by the MC68851.



BKPT#	BREAKPOINT SELECTED
0 0 0	BREAKPOINT REGISTER #0
0 0 1	BREAKPOINT REGISTER #1
0 1 0	BREAKPOINT REGISTER #2
0 1 1	BREAKPOINT REGISTER #3
1 0 0	BREAKPOINT REGISTER #4
1 0 1	BREAKPOINT REGISTER #5
1 1 0	BREAKPOINT REGISTER #6
1 1 1	BREAKPOINT REGISTER #7

FIGURE 4-4. BREAKPOINT ACKNOWLEDGE CYCLE ADDRESS ENCODING

4.10.3 MC68851 Breakpoint Architecture

For each of the eight breakpoint opcodes recognized by the MC68020, the MC68851 has a pair of registers: a breakpoint acknowledge control register and a breakpoint acknowledge data register. Figure 4-5 illustrates these and the breakpoint opcode to which each pair corresponds.

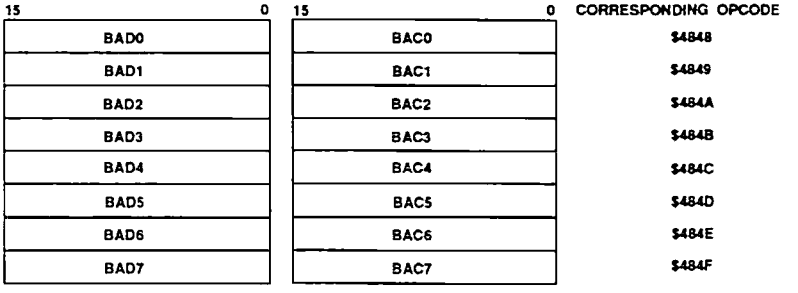


FIGURE 4-5. BREAKPOINT REGISTERS

Each of the breakpoint acknowledge data registers, BAD0 through BAD7, can be loaded with a replacement opcode for transfer to the MC68020 during the MC68851 acknowledge cycle. Using the PMOVE instruction, the 16-bit value for a legal MC68020 opcode may be written to (or read from) any BADx register in the format illustrated in Figure 4-6.

FIGURE 4-6. BREAKPOINT ACKNOWLEDGE DATA REGISTER FORMAT

The manner in which the data in a BADx register is actually used is controlled by data written in the corresponding breakpoint acknowledge control register - BACx- in the format illustrated in Figure 4-7.

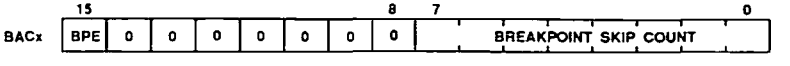


FIGURE 4-7. BREAKPOINT ACKNOWLEDGE CONTROL REGISTER FORMAT

4.10.4 MC68851 Acknowledge Cycle Operation

Bit 15 of a BACx register acts as a BreakPoint Enable (BPE) control field. During the MC68851 acknowledge cycle, when the breakpoint register pair corresponding to the transmitted breakpoint number has been selected, the BPE bit, if clear, disables transmission of the replacement opcode currently in BADx by causing the MC68851 to assert the BERR signal and thereby forcing the processor to initiate exception processing. The BPE bit in all eight registers is cleared by a reset cycle.

Bits 0 through 7 of a BACx register are used as a breakpoint skip count field whose value specifies the number of times that, in response to repeated processor breakpoint acknowledge cycles causing selection of that particular BACx register (and the corresponding BADx register), the MC68851 will transmit the current replacement opcode before forcing the processor to initiate exception processing by asserting the BERR signal. A reset cycle does not clear the skip count field in any of the eight acknowledge control registers. Refer to the MC68851 User's Manual for a more detailed description of the MC68851 breakpoint registers and functions.

4.10.5 Access Level Control

For communications between the MC68020 and the MC68851 during the Access Level Control (ACL) type of CPU space operations, the PMMU has an interface that includes a register set and support for a communications protocol. The protocol includes electrical and command level mechanisms that enable the MC68851 to extend the means of protection offered by the main processor.

Although not part of the MC68851 programming model, the Access Level Control Registers (ALCR) operate as communication ports, each register handling a specific control function. To use the function associated with a register, the processor accesses the register by encoding the address bus fields illustrated in Figure 4-8. Bits positions marked with an "x" are zero filled by the MC68020 and ignored by the PMMU.

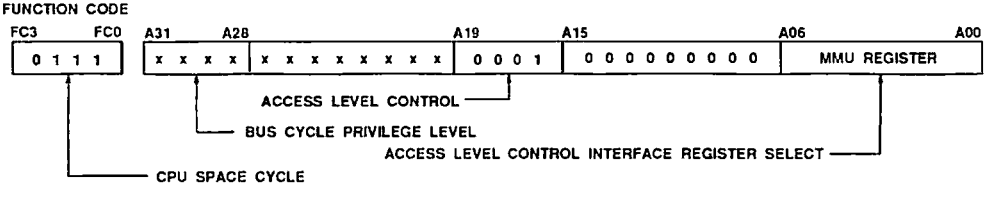


FIGURE 4-8. ALC INTERFACE LOGICAL ADDRESS BUS ENCODING

The MMU register (ALCR select) field, AØ through A15, is decoded by the MC68851 to select the appropriate ALCR. Although the MC68851 decodes the full address range specified on AØ through A15, the ALCRs occupy only the lower 128 bytes of this range. Table 4-3 provides a map of the MC68851 access control interface registers as they appear in the CPU address space. Refer to the MC68851 User's Manual for a more detailed description of the MC68851 access level control registers and functions.

TABLE 4-3. ALC INTERFACE REGISTERS MAP

REGISTER SELECT BUS	MC68851 ACCESS LEVEL INTERFACE REGISTER 31 23 0		
0 0 0 0 0 0 0	CL	READ	(UNUSED, RESERVED)
0 0 0 0 1 0 0	ACCESS STATUS	READ	(UNUSED, RESERVED)
0 0 0 1 0 0 0	IAL	WRITE	(UNUSED, RESERVED)
0 0 0 1 1 0 0	DAL	WRITE	(UNUSED, RESERVED)

1 0 0 0 0 x x	FUNCTION CODE 0 DESCRIPTOR ADDRESS	WRITE
1 0 0 0 1 x x	FUNCTION CODE 1 DESCRIPTOR ADDRESS (USER DATA)	WRITE
1 0 0 1 0 x x	FUNCTION CODE 2 DESCRIPTOR ADDRESS (USER PROGRAM)	WRITE
1 0 0 1 1 x x	FUNCTION CODE 3 DESCRIPTOR ADDRESS (USER RESERVED)	WRITE
1 0 1 0 0 x x	FUNCTION CODE 4 DESCRIPTOR ADDRESS (SUPERVISOR DATA)	WRITE
1 0 1 0 1 x x	FUNCTION CODE 5 DESCRIPTOR ADDRESS (SUPERVISOR PROGRAM)	WRITE
1 0 1 1 0 x x	FUNCTION CODE 6 DESCRIPTOR ADDRESS	WRITE
1 0 1 1 1 x x	FUNCTION CODE 7 DESCRIPTOR ADDRESS (CPU SPACE)	WRITE

4.10.6 Coprocessor Communications

Both the MC68851 and the MC68881 contain a set of Coprocessor Interface Registers (CIRs) by which the main processor and coprocessor communicate. These registers are not related to the programming model implemented by these coprocessors.

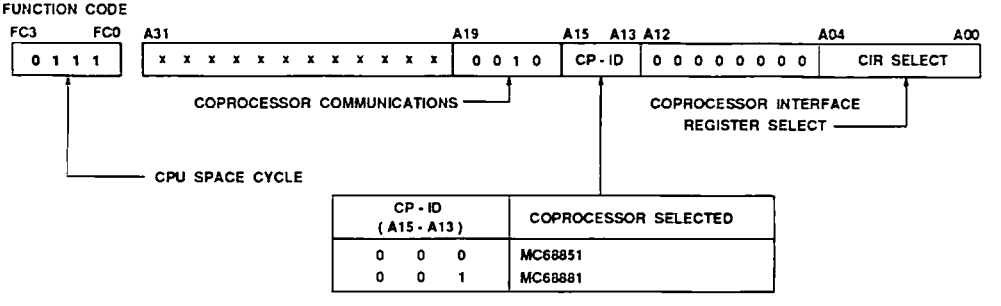


FIGURE 4-9. COPROCESSOR INTERFACE ADDRESS BUS ENCODING

Part of the CPU space accessed via the MC68Ø2Ø address bus is dedicated to coprocessor functions. Figure 4-9 illustrates the required address bus encoding for coprocessor accesses in the CPU space. The bit positions marked with an "x" are ignored by the MC68851 and MC68881 and are zero filled by the MC68Ø2Ø.

Table 4-4 identifies locations and characteristics of the MC68851 coprocessor interface registers in the CUP space, that are used for communications between the MC68Ø2Ø and the MC68851. Table 4-5 identifies the locations and characteristics of the MC68881 coprocessor interface registers in the CPU space that are used for communications between the MC68Ø2Ø and the MC68881. For a more detailed description of the MC68851 and MC68881 coprocessor registers and functions, refer to the MC68851 User's Manual and the MC68881 User's Manual.

TABLE 4-4. MC68851 COPROCESSOR INTERFACE REGISTER MAP

A04 - A00 (IN BINARY)	MC68851 ACCESS LEVEL INTERFACE REGISTER 31 15 0	
0 0 0 0 x	RESPONSE (READ)	
0 0 0 1 x	CONTROL (WRITE)	
0 0 1 0 x	SAVE (READ)	
0 0 1 1 x	RESTORE (READ/WRITE)	
0 1 0 0 x	OPERATION WORD (WRITE)	
0 1 0 1 x	COMMAND (WRITE)	
0 1 1 0 x	(RESERVED)	
0 1 1 1 x	CONDITION (WRITE)	
1 0 0 x x	OPERAND	(READ/WRITE)
1 0 1 x x	REGISTER SELECT (READ)	(RESERVED)
1 1 0 x x	INSTRUCTION ADDRESS	(READ/WRITE)
1 1 1 x x	OPERAND ADDRESS	(WRITE)

4.11 INTERRUPT HANDLER

The MVME135/136 module allows interrupts to the on-board CPU from up to 16 sources. The interrupt handler preprocesses interrupt sources into three groups of seven interrupts corresponding to the seven MC68Ø2Ø interrupt levels. The groups are labeled Group 1, Group 2, and Group 3. Interrupt service priority is determined by the interrupt level and the group number. Interrupts of different levels are processed according to the standard interrupt processing discipline. Interrupts of the same level are processed according to the group number.

TABLE 4-5. MC68881 COPROCESSOR INTERFACE REGISTER MAP

A04 - A00 (IN BINARY)	MC68881 ACCESS LEVEL INTERFACE REGISTER 31 15 0	
0 0 0 0 x	RESPONSE (READ)	
0 0 0 1 x	CONTROL (WRITE)	
0 0 1 0 x	SAVE (READ)	
0 0 1 1 x	RESTORE (READ/WRITE)	
0 1 0 0 x	OPERATION WORD (WRITE)	
0 1 0 1 x	COMMAND (WRITE)	
0 1 1 0 x	(RESERVED)	
0 1 1 1 x	CONDITION (WRITE)	
1 0 0 x x	OPERAND	(READ/WRITE)
1 0 1 x x	REGISTER SELECT (READ)	(RESERVED)
1 1 0 x x	INSTRUCTION ADDRESS	(WRITE)
1 1 1 x x	OPERAND ADDRESS	(READ/WRITE)

The interrupt handler processes Group 2 and Group 3 interrupts differently from Group 1 interrupts which are reserved for VMEbus interrupts. If the interrupt being acknowledged is a Group 2 or 3 interrupt, the interrupt handler fetches the appropriate exception vector number from PROM and sends it to the CPU via the local bus. If the interrupt being acknowledged is a Group 1 interrupt, the exception vector number is fetched from the VMEbus where it will be placed by the interrupting device. Table 4-6 describes the interrupt assignments.

TABLE 4-6. INTERRUPT HANDLER PRIORITY ASSIGNMENTS

INTERRUPT LEVEL	PRIORITY WITHIN A PARTICULAR INTERRUPT LEVEL DETERMINES THE SERVICE ORDER (HIGHEST)	(MIDDLE)	(LOWEST)
	GROUP 3 (VECTOR #)	GROUP 2 (VECTOR #)	GROUP 1
7	ABORT* (\$40)	ACFIRQ* (\$41)	VMEbus IRQ7*
6	TMRIRQ* (\$42)	SFIRQ* (\$43)	VMEbus IRQ6*
5	SIOIRQ* (\$44)	SIGHP* (\$45)	VMEbus IRQ5*
4	UNASSIGNED	VSBIRQ* (\$47)	VMEbus IRQ4*
3	UNASSIGNED	UNASSIGNED	VMEbus IRQ3*
2	LMIRQ* (\$4A)	SIGLP* (\$4B)	VMEbus IRQ2*
1	UNASSIGNED	UNASSIGNED	VMEbus IRQ1*

WITHIN A GROUP x, INTERRUPT PRIORITY DECREASES WITH DECREASING LEVEL.
WITHIN A PARTICULAR INTERRUPT LEVEL, INTERRUPT PRIORITY DECREASES FROM LEFT TO RIGHT.

ABORT* **< Abort Pushbutton IRQ>**

ABORT* is the interrupt caused by the ABORT pushbutton.

ACFIRQ* **< VMEbus AC Power Fail IRQ>**

ACFIRQ* is the interrupt caused by the ACFAIL* line being asserted on the VMEbus.

TMRIRQ* **< Timer IRQ>**

TMRIRQ* is the local timer chip's interrupt. This will also be the broadcast IRQ caused by a transition on the IRQ1* line of the VMEbus similar to the MVME13Ø, provided that the Z8Ø36 timer chip is preconfigured to assert TMRIRQ* upon receipt of a broadcast IRQ input.

SFIRQ* **< VMEbus System Fail IRQ>**

SFIRQ* is the interrupt caused by the SYSFAIL* line of the VMEbus being asserted. This interrupt is maskable using the SYSFIEN bit of < CNT3> .

SIOIRQ* **< Dual Channel Serial Port IRQ>**

SIOIRQ* is the interrupt from the local serial port chip, the MC68681. The SIOIRQ* interrupt is handled the same as all other local interrupts, where the vector is supplied by a PROM.

SIGHP* **< MPCSR High Priority IRQ>**

SIGHP* is the signal high priority interrupt from the MPCSR. This interrupt is maskable using the SHPIEN bit of < CNT3> .

VSBIRQ* **< VSBbus IRQ>**

VSBIRQ* is an interrupt from the secondary bus, VSBbus. This interrupt is maskable using the VSBIEN bit of < CNT1> .

LMIRQ* **< Location Monitor IRQ>**

LMIRQ* is the interrupt caused from the location monitor indicating there was a VME access to the Short I/O broadcast area. This interrupt is maskable using the LMIEN bit of < CNT3> .

SIGLP* **< MPCSR Low Priority IRQ>**

SIGLP* is the signal low priority interrupt from the MPCSR. This interrupt is maskable using the SLPIEN bit of < CNT3> .

IRQ1*-IRQ7* **< VMEbus IRQ7*-IRQ1*>**

Interrupts IRQ1* through IRQ7* are the VMEbus interrupts. These interrupts are individually maskable using the VBIMSK1 through VMIMSK7 bits of < CNT2> .

4.12 ONBOARD ROM/PROM/EPROM

The MVME135/136 module has two 28-pin JEDEC sockets that are organized as a single bank. This bank appears as a 16-bit word port to the MC68Ø2Ø and can be configured for 32K x 8 or 64K x 8 ROM/PROM/EPROMs with an access time of 25Ø nanoseconds or faster, providing a total of 128Kb of non-volatile storage. If 32K x 8 devices are used, they will appear twice in the 128Kb ROM/PROM/EPROM address space.

4.13 DUAL SERIAL PORTS

For its two asynchronous serial ports, the MVME135/136 module uses the MC68681 to provide the timing and control necessary to support two independent communications channels.

Both serial ports utilize standard RS-232C drivers and receivers. Signals are available through DB-9 connectors located on the MVME135/136 module's front panel. Both ports are configured as a 9-wire DTE interface as illustrated in Figure 4-1Ø.

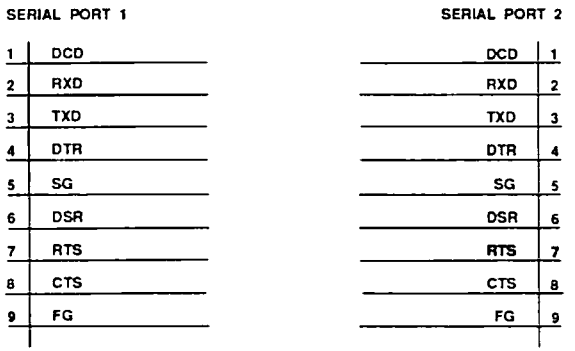


FIGURE 4-1Ø. SERIAL PORT INTERCONNECTIONS

4.14 MVME135/136 TIMER

Timer functions for the MVME135/136 modules are provided by a Z8Ø36 Counter/Timer and Parallel I/O Unit. This device offers two independent 8-bit, double-buffered, bidirectional I/O ports, three independent 16-bit counter/timers, and a 4-bit special purpose I/O port. The latter is used in conjunction with one counter/timer to implement a watchdog timer and also provide a means for software selection of a reset type. The function of each of the timers is described below.

Timer #1 - User Programmable Timer

This programmable timer is not utilized by the MVME135/136 hardware or on-board firmware and is therefore, available to the user.

Timer #2 - Periodic Tick Timer

When enabled, this timer causes a local Group 3 interrupt on Level 6 when it times out. Group 3, Level 6 is the highest local interrupt except for ABORT. Timer periods range from 1 to 10 milliseconds and are software selectable.

Timer #3 - Watchdog Timer

This time is capable of generating three types of reset (two local and one global). The watchdog timer must be periodically serviced by software to prevent timeout so that the module is not reset.

When a reset does occur, a bit indicating this condition is set in the local Control/Status Register (CSR) to provide for software recovery, if needed. A corresponding bit is also set in the Multiprocessing Control/Status Register (MPCSR) to provide other bus masters with the reset indication.

Because system controller functions are independent of local reset, the MVME135/136 modules will not assert the SYSRESET signal on the VMEbus when either of the local reset options is chosen. Two types of local reset are available from the watchdog reset timer and are enabled via bits 6 and 7 (WD0, WD1) of Local Control Register #5. They are a Momentary Reset of sufficient duration to reset all hardware on the module, and a Reset And Hold. The momentary reset option allows the MC68020 microprocessor and other devices to come back up and operate. The reset and hold option keeps the module in local reset until a SYSRESET is asserted on the VMEbus, or until another VMEbus master clears the R&H bit in the MPCSR. Both options are software selectable.

The global reset option for the watchdog timer will cause a 200 millisecond minimum reset pulse to appear on the VMEbus SYSRESET line. This option is also software selectable.

4.15 LOCAL CONTROL/STATUS REGISTERS

The MVME135/136 Control/Status Registers (CSR) use the two Z8036 8-bit parallel ports to provide local and system side information to the on-board MPU and control of various local and system level functions.

Switch S4 is a 10-position switch, settable from the front panel. Switch positions 1 and 2 are control functions (refer to section 3.2.5 for a brief description of these switch functions). Switch positions 3 through 10 are readable and constitute STAT1 (Status Register 1) as defined below. In the following text, PA is physical address, RC is reset condition, (res) is reserved, and NA is not available for use.

4.15.1 Status Register Format And Functions

The following text describes the format and functions of the Status Registers.

<STAT1> Physical Address: $FFFB000D (Read Only) RC = None

D07	D06	D05	D04	D03	D02	D01	D00
GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
S4-3	S4-4	S4-5	S4-6	S4-7	S4-8	S4-9	S4-10

GP7-GP0 < General Purpose User Status Bits>

GP0 through GP7 are front panel selectable user status bits (S4-3 through S4-10) used for software steering. Access to this register will read Port A of the timer. 135bug configures Port A of the timer as an input port and uses these general purpose bits to perform various optional switching functions. For a complete description of 135bug's use of these switches, refer to the 135bug Diagnostic/Debug Package User's Manual.

If firmware other than 135bug is used, the resident firmware must configure Port A of the timer before reading STAT1, otherwise, the data will not be a valid representation of the switch settings. Refer to the Zilog Z-CIO (Z8036) Counter/Timer and Parallel I/O Unit Technical Manual for information on programming the timer registers.

<STAT2> Physical Address: $FFFB0032 (Read Only) RC = Not Valid

D07	D06	D05	D04	D03	D02	D01	D00
RAMERR*	RMCERR*	ABORT*	SYSFAIL*	VBER*	VSBERR*	MMUBER*	LCLERR*

Data bits 00, 01, 02, 03, 06, and 07 will clear automatically when read. These six data bits will indicate the bus error that is the most recent only. The contents of this register is invalid after

power-up reset, and should be read once by the system software to initialize the bus error status bits to their inactive state.

RAMERR* < Local DRAM Parity Error>

RAMERR*, when low, indicates that the bus error was caused by a local DRAM memory read where a single-bit error had been detected. The board must be properly configured for parity operation. Refer to the descriptions of jumper J6 and parity enable, sections 2.3.4 and 4.15.2, respectively.

RMCERR* < Read-Modify-Write Cycle Error>

The shared memory architecture of the MVME135/136 module requires that during a slave access to the on-board DRAM, the MC68Ø2Ø must give up the local bus. A lockup condition occurs when another bus master has possession of the VMEbus and is trying to access the MVME135/136 DRAM and the MVME135/136 has just begun an access to a memory location that resides in VMEbus mapped memory space.

Normally, this situation is handled by circuitry on the MVME135/136 that detects the lockup and asserts BERR* and HALT* to the local MC68Ø2Ø causing a retry. The MC68Ø2Ø terminates the cycle, and then arbitrates the local bus away allowing the slave access to complete. After the slave access has completed and the MC68Ø2Ø becomes the local bus master, the retry cycle then completes, all transparent to the system software.

RMCERR* indicates that the lockup condition described above has occurred while the local MC68Ø2Ø was executing a TAS (Test And Set) cycle. The MC68Ø2Ø will not do a retry, while it is performing a locked cycle (RMC* asserted). When this situation is detected, a bus error is asserted to the MC68Ø2Ø, and the RMCERR* status bit is asserted.

During the bus error handling routine, the system software must examine STAT2. If RMCERR* is asserted, the processor retry flag should be set before returning from exception processing. This in effect causes a software retry for the lockup condition when RMC* type cycles are involved.

ABORT* < ABORT Pushbutton Status>

The system software can monitor the status of the MVME135/136 ABORT pushbutton via the ABORT status flag. Pressing the ABORT pushbutton will cause a level seven interrupt. During abort interrupt handling, 135bug monitors this status flag before returning from exception to ensure that the abort interrupt is seen only once.

SYSFAIL* < VMEbus System Failure Status>

A system failure, communicated to this module via the VMEbus SYSFAIL* signal, will set the SYSFAIL* flag = Ø. If the SYSFIEN* bit is set when a system failure occurs, the MVME135/136 interrupt handler will assert SFIRQ* to the processor.

VBER* < VMEbus Bus Error>

VBER* = Ø, if a VMEbus reference made by this MVME135/136 caused a bus error (i.e., only VMEbus bus errors made by this MVME135/136 when it is VMEbus master will be logged).

VSBERR* < VSBbus Bus Error>

VSBERR* = Ø, if a VSBbus reference made by this MVME135/136 caused a bus error. VSBERR* will be asserted.

MMUBER* < MMU Bus Error>

MMUBER* = Ø, when the bus error signal from the MMU device has been asserted. The MMU will assert BERR* and HALT* to the MC68Ø2Ø during Relinquish and Retry operations, in which it forces the current logical bus master to terminate the current bus cycle, release the logical bus, and retry the bus cycle when it is once again logical bus master. The concurrent assertion of HALT* and BERR* by the MMU constitutes the Retry phase of the Relinquish and Retry cycle. The MMUBER* status bit will only indicate true MMU cycle faults, not Relinquish and Retry cycle types.

LCLERR* < Local Timeout Error>

LCLERR*, when low, indicates that a reference to a locally mapped device caused a timeout bus error. This signal is also asserted if an access attempt is made to local coprocessors such as the MC68881 or MC68851 that is not installed in the module.

4.15.2 Control Register Format And Functions

The following text describes the format and functions of the Control Registers.

<CNTl> Physical Address: $FFFBØØØE (Read/Write) RC = None

D07	D06	D05	D04	D03	D02	D01	D00
BRIRQI*	WWP	PAREN*	VSBIEN	NA	NA	NA	NA

Access to this register will read the B port of the timer. Data bit Ø7 should always be programmed as an input. Data bits Ø5 and Ø6 are

used for testing and use of parity on the local DRAM. They must be programmed as outputs to be used. Data bit Ø4 is a mask for the VSBbus interrupt and must be programmed as an output to be used.

BRIRQI* **< Broadcast Interrupt Input>**

BRIRQI* is actually an input to the Z8Ø36 timer from the VMEbus IRQ1*. This is provided to allow the user that has several MVME135/136's to interrupt all of these processors with a single VMEbus interrupt. IRQ1* cannot be used as a VMEbus interrupt if BRIRQI* is used to interrupt the MVME135/136 through the Timer and therefore must be masked at CNT2. The VMEbus interrupter that causes BRIRQI* by asserting VMEbus IRQ1* must also negate this level. This interrupt must not be acknowledged on the VMEbus in this mode. If normal VMEbus IRQ1* operation is desired, then the Timer input must be programmed to not recognize the BRIRQI* interrupt. The Timer I/O pin connected to VMEbus IRQ1* must never be programmed as an output (Timer port B, bit 7).

WWP **< Write Wrong Parity>**

WWP*, when high, forces parity to be written incorrectly to local DRAM. This facilitates testing of on-board parity circuitry.

PAREN* **< Parity Enable>**

PAREN*, when low, enables parity error reporting by allowing bus errors to the local processor on read cycles where parity faults are detected. Parity should not be enabled, unless a jumper cap is installed across jumper J6 pins 2 and 3.

VSBIEN **< VSBbus Interrupt Enable>**

VSBIEN, when high, enables the MVME135/136 to be interrupted by the VSBIRQ* interrupt signal. VSBIRQ* is the interrupt signal from the VSBbus.

<CNT2> Physical Address: $FFFBØØ38 (Read/Write) RC = 11111111

D07	D06	D05	D04	D03	D02	D01	D00
VBIMSK7	VBIMSK6	VBIMSK5	VBIMSK4	VBIMSK3	VBIMSK2	VBIMSK1	VMSK*

CNT2 indicates which VMEbus interrupt this module's interrupt handler will respond to. If VBIMSKx = 1, then the module will not respond to the VMEbus IRQx. VMSK is a DRAM mask bit. When active it will not allow slave access to the local DRAM.

VBIMSK7-1 < VMEbus Interrupt Mask Bits>

The MVME135/136 Interrupt Handler will respond to the VMEbus interrupts that have their corresponding bit positions set in CNT2 as follows:

1. VBIMSKx = Ø, acknowledge VMEbus VBIRQx*.
2. VBIMSKx = 1, mask VMEbus VBIRQx*.

After reset, all CNT2 bits power up = 1, masking all VMEbus interrupts and allowing slave access to local DRAM from VMEbus.

VMSK* < VMEbus Access Mask>

VMSK*, when low, disallows any local DRAM access from VMEbus. This feature allows the MVME135/136 local memory to become completely private to the MC68Ø2Ø CPU.

<CNT3> Physical Address: $FFFBØØ39 (Read/Write) RC = 11111111

D07	D06	D05	D04	D03	D02	D01	D00
BUSY	ALLIEN*	SYSFIEN*	SHPIEN*	SLPIEN*	LMIEN*	BRIRQ0*	VSBIRQ0*

BUSY < MVME135/136 Module Busy>

Software steering bit that shows the module's system readiness. BUSY is used by 135bug as a status flag during diagnostic operation. BUSY is imaged in a read only register in the MPCSR (refer to section 4.16).

ALLIEN* < All Interrupt Enable>

When ALLIEN* = Ø, all MVME135/136 interrupts are enabled to the Interrupt Handler. When ALLIEN = 1, all interrupts are disabled allowing vector table initialization.

SYSFIEN* < SYSFAIL Interrupt Enable>

SYSFIEN is used to enable SYSFIRQ to the local interrupt handler when a system failure occurs. Refer to the SYSFAIL status register bit for more details regarding SYSFAIL*. When SYSFIEN = 1 (power up case), the SYSFIRQ* is disabled. When SYSFIEN = Ø and VMEbus SYSFAIL* is asserted, SYSFIRQ will be asserted to the MVME135/136 Interrupt Handler.

SHPIEN* < Signal High Priority Interrupt Enable>

SHPIEN*, when low, enables an interrupt to occur when SIGHP is set

in the MPCSR (refer to section 4.16). SHPIEN*, when high, prevents SIGHP from being set in the MPCSR. This restriction applys only to Artwork Revisions A-C. Artwork Revision E allows SIGHP to be set independent of the state of SHPIEN*.

SLPIEN* < Signal Low Priority Interrupt Enable>

SLPIEN*, when low, enables an interrupt to occur when SIGLP is set in the MPCSR (refer to section 4.16). SLPIEN*, when high, prevents SIGLP from being set in the MPCSR. This restriction applys only to Artwork Revisions A through C. Artwork Revision E allows SIGLP to be set independent of the state of SLPIEN*.

LMIEN* < Location Monitor Interrupt Enable>

LMIEN*, when low, enables an interrupt to occur from location monitor zero, in the MPCSR (refer to section 4.16).

BRIRQO* < Broadcast Interrupt Output>

BRIRQO*, when low, asserts VMEbus IRQ1*. This is not intended to cause a VMEbus interrupt. This bit is intended for use as a broadcast mechanism that is compatible with the MVME13Ø, where VMEbus IRQ1* is connected to bit 7 of Timer Port B and causes a timer interrupt. The MVME135/136 is also capable of being interrupted in this way. Refer to the BRIRQI* description under CNT1.

VSBIRQO* < VSBbus Interrupt Output>

VSBIRQO*, when low, asserts VSBIRQ* low on VSBbus, allowing the MVME135/136 to generate VSBbus interrupts for diagnostics applications.

<CNT4> Physical Address: $FFFBØØ3A (Read/Write) RC = 1-------

D07	D06	D05	D04	D03	D02	D01	D00
GLBRES*	NA	NA	NA	NA	NA	NA	NA

GLBRES* < Global Reset>

GLBRES*, when low, will cause a 2ØØ millisecond system reset. This will happen whether the MVME135/136 is the system controller or not. The data in this register is undefined when read.

<CNT5> Physical Address: $FFFB00 3B (Read/Write) RC = 11111111

D07	D06	D05	D04	D03	D02	D01	D00
WD0	WD1	LTMO	VTMO	OPT0	32/24*	32/16*	BDFAIL

WDØ,WD1 < Watch Dog Timer Control Bits>

When the watch dog timer times out, the following function occurs.

WD1	WDØ	Function
Ø	Ø	Momentary System Reset.
Ø	1	Momentary Local Reset.
1	Ø	Local Reset and Hold.
1	1	Watchdog Timer Disabled.

LTMO < Local Timeout Enabled>

When set, the local timeout generator is enabled.

VTMO < VMEbus Timeout Enabled>

When set, the VMEbus timeout generator is enabled.

OPTØ < Local DRAM Address Ø>

When set, local DRAM is mapped at ØØØØØØØØ (hex). The local DRAM always appears at FFEØØØØØ (hex) for the MVME135/135-1/136 versions and at FF8ØØØØØ (hex) for the MVME135A/136A versions.

32/24* < VMEbus Address Size Select>

This bit provides a software selectable 32- and 24-bit address option for VMEbus references. The appropriate address modifiers are generated for 32- or 24-bit address VMEbus accesses. 32/24* = 1 indicates 32-bit address option; 32/24* = Ø indicates a 24-bit address space. Refer to the following memory map chart for the affect of the 32/24* bit on the MVME135/136 VMEbus memory map.

If 32/24* = Ø:

ØØØØØØØØ-ØØFFFFFF A 24-bit address modifier is generated.

Ø1ØØØØØØ-FFDFFFFF A 32-bit address modifier is generated. (MVME135/135A/135-1/136 versions)

Ø1ØØØØØØ-FF7FFFFF A 32-bit address modifier is generated. (MVME136A version)

If 32/24* = 1:

00000000-FFDFFFFF	A 32-bit address modifier is generated. (MVME135/135A/135-1/136 versions)
00000000-FF7FFFFF	A 32-bit address modifier is generated. (MVME136A version)

Either with 32/24* set or cleared:

FFE00000-FFFEFFFF	Local address space. (MVME135/135A/135-1/136 versions)
FF800000-FFFEFFFF	Local address space. (MVME136A version)
FFFF0000-FFFFFFFF	A 16-bit address modifier is generated (VMEbus short I/O).

32/16* **< VMEbus Data Size Select>**

This bit provides a software selectable 32- or 16-bit VMEbus data width. This bit should be used with care because when 32/16* = 0, all memory references to VMEbus are forced to be 16 bits. When 32/16* = 1, all memory references to the VMEbus can be 32 bits.

The memory map can be customized in hardware by the user to segment D16 and D32 address space. This is performed by programming PAL2 (U60) for the particular application. The default memory map for D32 and D16 data space is illustrated in Figure 4-11. Refer to Appendix A for the description and equations for PAL2 (for the MVME135/135-1/136 versions only). Refer to Appendix B for the description and equations for PAL2 (for the MVME135A/136A versions only).

BDFAIL **< Board or System Failure>**

If this bit is = 1 (and the ISF bit in the MPCSR is clear), then the SYSFAIL* line on VMEbus will be asserted. The "FAIL" LED will be illuminated, whenever BDFAIL is set.

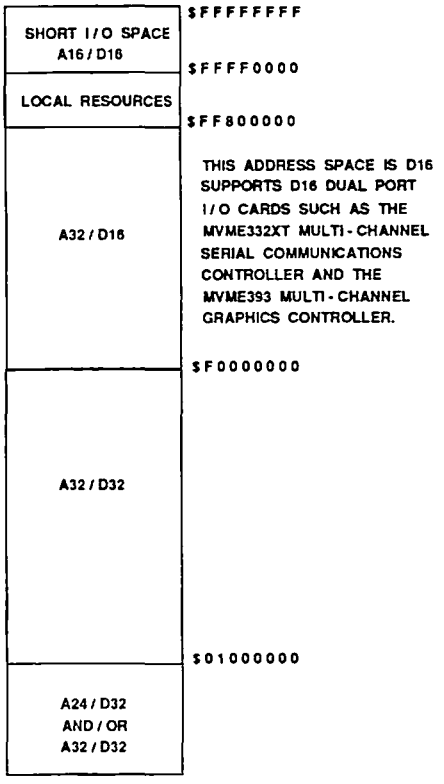


FIGURE 4-11. D16/D32 DEFAULT DATA SEGMENTATION

4.16 MULTIPROCESSOR CONTROL/STATUS REGISTERS (MPCSR)

The MVME135/136 modules are designed for multiprocessor applications providing a number of hardware features for this type of environment. These include global access to and control of the status of several module functions, as well as the ability to generate virtual interrupts to selected boards, and/or simultaneous interrupts to multiple boards. Their design does not define or limit in any way the architecture of a multiprocessor application, but, rather, eases its development, particularly from the point of view of software. The registers provided to facilitate use of a MVME135/136 module in any multiprocessor environment (the MPCSR), is illustrated in Table 4-7. The MPCSR is dual ported between the local MC68Ø2Ø microprocessor and VMEbus. The MPCSR may be accessed by the local processor at $FFFBØØ6Ø to 7F, or from the MPCSR VMEbus mapped location.

TABLE 4-7. MULTIPROCESSOR CONTROL/STATUS REGISTERS

ADDRESS OFFSET	D07	D06	D05	D04	D03	D02	D01	D00
1	ID BYTE							
3	BSY	SCON	FAIL	WDT	UNDEFINED			
5	KING* @	LM2*	LM1*	LM0*	ISF	LKTR @@	UNDEFINED	
7	R&H	UNDEFINED			RONR	UNDEFINED		
9	H&H	UNDEFINED						
B	SIGLP	UNDEFINED						
D	SIGHP	UNDEFINED						
F	UNDEFINED							
11	MP0	UNDEFINED						
13	MP1	UNDEFINED						
15	MP2	UNDEFINED						
17	MP3	UNDEFINED						
19	MP COMM BYTE							
1B								
1D								
1F								

@ ALSO DESIGNATED LM3*.
@@ LKTR IS READ ONLY FROM VMEbus AND IS READ/WRITE FROM THE LOCAL BUS.

ID < ID Byte>

This byte is the image of the mapping switch used to map the MPCSR and DRAM on the VMEbus. This byte allows the local processor to identify where other bus masters will be accessing its memory. The MPCSR will be at xxxyyyyy on the VMEbus, where "xxx" is the group base address and "yyyyy" is the base offset within the group. The module ID can be read visually from the board by looking at the 8-bit mapping switch S3. Refer to the Local DRAM and MPCSR Mapping examples in section 3.2.4.

BSY < Busy Bit>

This bit will come up asserted and is typically used to indicate that the MVME135/136 is not ready to operate at the system level. This will be the case while the MVME135/136 is executing confidence tests and during initialization of local resources. This bit is read only and is an image of the local busy bit located in CNT3. The function of this bit is determined only by the resident firmware/system software.

SCON < System Controller Bit>

This bit is the image of the local control bit that establishes the module as the VME system controller. This bit is active high, read only.

FAIL < Fail Bit>

This bit enables another VMEbus master to determine if the MVME135/136 has indicated a local failure. This bit is the image of the local BDFAIL bit. It will also be able to determine if the module is asserting the SYSFAIL* line on the VMEbus by setting or clearing the ISF bit, and monitoring for the SYSFAIL interrupt. This bit is read only.

WDT < Watchdog Timer Bit>

This status bit indicates whether a watchdog reset has occurred on the module. This bit is read only, and is cleared when read.

KING(LM3*) < KING Bit>

This bit will come up asserted and will indicate that the module has not been disqualified as the system initializer. The location monitor can clear this bit on all modules in the group at the same time.

LMØ*-LM2* < Location Monitor Bits>

The local processor can be interrupted by a broadcast cycle. This cycle can be recognized by all MVME135/136s in the system. This is accomplished with a location monitor that will detect a VMEbus cycle to the A16 (Short I/O) addresses determined by the VMEbus mapping switch. There is an enable bit in the local CSR (CNT3) that will allow the MVME135/136 to mask the location monitor interrupt. LMØ* is the only location monitor bit that can cause an interrupt. The MPCSR resides on odd addresses in the VMEbus Short I/O space. The VMEbus base address in this space will be mappable as shown in Table 4-8. Locally the address of the MPCSR is FFFBØØ6Ø-FFFBØØ7F.

Location monitor examples:

For MPCSR mapped at ØØØØ in VMEbus Short I/O. (Group Ø)

VME word access to Ø3EØ - will clear LMØ* and cause a location monitor interrupt, if the system software has setup the proper enables and lowered the processor mask.
VME word access to Ø3E2 - will clear LM1*.
VME word access to Ø3E4 - will clear LM2*.
VME word access to Ø3E6 - will clear LM3* (KING bit).

TABLE 4-8. MAPPING ON THE VMEbus

SWITCH S3 SETTINGS ID BYTE (IN MPCSR) 1 2 3	4 5 6 7 8	MPCSR BASE ADDRESS (VME SHORT I/O SPACE)	DRAM BASE ADDRESS (MVME135/135-1/136)	DRAM BASE ADDRESS (MVME136A)
0 0 0	0 0 0 0 0	$0000	$00000000	$00000000
0 0 0	0 0 0 0 1	$0020	$00100000	$00400000
0 0 0	0 0 0 1 0	$0040	$00200000	$00800000
		UP TO 31 DIFFERENT MPCSR START ADDRESSES FOR EACH GROUP		
0 0 0	1 1 1 0 0	$0380	$01C00000	$07000000
0 0 0	1 1 1 0 1	$03A0	$01D00000	$07400000
0 0 0	1 1 1 1 0	$03C0	$01E00000	$07800000
0 0 0	1 1 1 1 1	RESERVED FOR BROADCAST, GROUP 0		
0 0 1	0 0 0 0 0	$2000	$00000000	$00000000
0 0 1	0 0 0 0 1	$2020	$00100000	$00400000
0 0 1	0 0 0 1 0	$2040	$00200000	$00800000
0 0 1	1 1 1 0 0	$2380	$01C00000	$07000000
0 0 1	1 1 1 0 1	$23A0	$01D00000	$07400000
0 0 1	1 1 1 1 0	$23C0	$01E00000	$07800000
0 0 1	1 1 1 1 1	RESERVED FOR BROADCAST, GROUP 1		
0 1 0	0 0 0 0 0	$4000	$00000000	$00000000
0 1 0	0 0 0 0 1	$4020	$00100000	$00400000
0 1 0	0 0 0 1 0	$4040	$00200000	$00800000
0 1 0	1 1 1 0 0	$4380	$01C00000	$07000000
0 1 0	1 1 1 0 1	$43A0	$01D00000	$07400000
0 1 0	1 1 1 1 0	$43C0	$01E00000	$07800000
0 1 0	1 1 1 1 1	RESERVED FOR BROADCAST, GROUP 2		
0 1 1	0 0 0 0 0	$6000	$00000000	$00000000
0 1 1	0 0 0 0 1	$6020	$00100000	$00400000
0 1 1	0 0 0 1 0	$6040	$00200000	$00800000
0 1 1	1 1 1 0 0	$6380	$01C00000	$07000000
0 1 1	1 1 1 0 1	$63A0	$01D00000	$07400000
0 1 1	1 1 1 1 0	$63C0	$01E00000	$07800000
0 1 1	1 1 1 1 1	RESERVED FOR BROADCAST, GROUP 3		
		:	:	:
		:	:	:
		:	:	:
		:	:	:
		:	:	:

NOTE: SETTING S3-4 THROUGH S3-8 TO 1 (ALL OFF) IS NOT ALLOWED.
THIS ADDRESS SPACE FOR EACH GROUP IS USED AS BROADCAST ADDRESSES FOR LOCATION MONITORS.

ISF < Inhibit SYSFAIL Bit>

If the module has a BDFAIL asserted locally and ISF is not active, then the module is asserting SYSFAIL* on the VMEbus. Another bus master can force the MVME135/136 to negate the SYSFAIL* line by setting the ISF bit in the MPCSR. This is helpful to prevent interrupts after a module has been diagnosed as failed.

LKTR < VMEbus Locked Transfer>

LKTR when asserted will cause the next VMEbus access to lock possession of VMEbus to this MVME135/136 module. The normal release on request functioning of the MVME135/136 requester is disabled and release of VMEbus mastership will not occur until LKTR is negated. LKTR is intended to allow the system software to execute routines over VMEbus in a deterministic amount of time. If LKTR is asserted, the MVME135/136 module is not contending for VMEbus ownership with other VMEbus masters. LKTR, when set, does not immediately lock the VMEbus, unless VMEbus mastership has already occurred from previous VMEbus cycles and was not requested away by another VMEbus master. LKTR should be used with extreme care since other bus masters will not be able to obtain VMEbus ownership until the local CPU has cleared the LKTR bit.

LKTR is Read/Write from the local processor over the locally mapped address location, and is read only from the VMEbus mapped location. When LKTR is cleared, the MVME135/136 VMEbus requester operates in Release-On-Request mode, holding VMEbus mastership only until another VMEbus master requests the VMEbus. Release-On-Request operation is more efficient because the total number of VMEbus arbitration cycles is reduced.

R&H < Reset and Hold Bit>

Another VMEbus master will be able to place the module in reset by asserting this bit location. The module will remain in reset until the location is cleared or a system reset occurs. When R&H is set, a minimum of 5 microseconds may elapse before the module is placed in reset. When R&H is cleared, .5 seconds minimum will elapse before the module completes reset. To prevent memory corruption, it is recommended that HALT and HOLD be asserted before R&H is asserted.

RONR < Request On No Request>

RONR, when set, forces the MVME135/136 requester to wait to request the VMEbus until the request level that it is using has been negated. This causes all MVME135/136 modules that are on the same VMEbus request level, and have RONR asserted to share the available VMEbus bandwidth equally. The effect of RONR operation is like round robin arbitration. However, RONR allows round robin operation with a single level VMEbus arbiter, and does not limit the number of masters equally sharing the bus to the number of arbitration levels of the system bus (VMEbus).

When RONR is negated, strict priority determined by the MVME135/136's position in the VMEbus daisy-chain will determine the bus bandwidth obtained. MVME135/136's or other VMEbus masters that are nearer to the VMEbus arbiter will obtain most of the

available bus bandwidth. RONR may be used when it is important for all of the MVME135/136 modules to have fair access to VMEbus. Other bus masters that are not equipped with the RONR feature may starve the VME135 from access to the VMEbus, since the MVME135/136 is attempting to be fair and the other bus masters are not.

It may be necessary to experiment with different configurations of VMEbus arbitration levels and implementations of RONR operation with other VMEbus masters. Also, experimentation with the system configuration with respect to position within the VMEbus arbitration daisy-chain is recommended.

H&H < Halt and Hold Bit>

This bit enables another VMEbus master to place the module in halt by setting this bit. This ability is provided to allow upload and download of the DRAM with the local processor operation suspended.

SIGLP < Signal Low Priority>

The local processor may be interrupted by asserting this bit location. There is a control bit in the local control registers that will allow this interrupt to occur (SLPIEN in < CNT3>). This is a level 2 interrupt to the local processor.

SIGHP < Signal High Priority>

The local processor may be interrupted by asserting this bit location. There is a control bit in the local CSR that will allow this interrupt to occur (SHPIEN in < CNT3>). This signal is a higher priority locally (level 5) than SIGLP.

MPØ-MP3 < Multi-Processor Bits>

These are read/write bits in the most significant bit of each byte they occupy. They may be used as semaphores or as handshake bits for passing information through the MP COMMunication (MP COMM) channel described below.

MP COMM < Multi-Processor Communication Byte>

This is a byte wide communications path that allows interaction to be accomplished between bus masters independently of DRAM.

4.16.1 Base Address Selection

The MVME135/136 modules have an 8-position switch (S3) for locating the MPCSRs, as well as the local DRAM, in the VMEbus address space. A total of eight groups is accommodated and within each group a unique base address for up to 31 processor modules can be selected. The 32nd address range for each group is reserved for location monitor accesses capable of broadcasting an interrupt to all processor

boards within that group. Figure 4-12 illustrates the MPCSR and DRAM mapping capability provided by switch S3 and gives an example of the addresses selected by a specific setting of the switch. Refer to Table 4-8 for a listing of the MPCSR and DRAM base addresses that can be selected by switch S3. Note that using a S3 base offset setting to obtain a unique address for a processor module results in the same DRAM address regardless of the S3 group setting. Therefore, for a system, the maximum number of processor modules each having DRAM with a unique VMEbus address is 31.

4.17 VSBbus CONTROL/STATUS REGISTER

There are three registers in the VSBchip. They are the control and status register, the decode address register, and the block transfer count/extended address register. This register is referred to as the VSBCSR.

VSBbus Register	Function
Ø	Control and Status
* 1	Block Transfer/Extended Address
* 2	Decode Address

* Not used and should not be accessed on the MVME135/136.

4.17.1 VSBbus Control/Status Register Format And Functions

This register controls those functions which if asserted could drastically affect the functioning of the MVME135/136. Altering any of these bits should be done with care. These bits select the VSBchip, enable the VSBbus System Controller function, enable block transfer, set the MC68Ø2Ø mode, enable external decoding, make the bus read only, enable the bus timeout timer, and enable the bus fairness mode.

The status register reflects only the latest BERR condition. When a new BERR condition occurs, any previously set bits may change. This register is cleared upon reading or when a reset condition occurs. The following text describes this register.

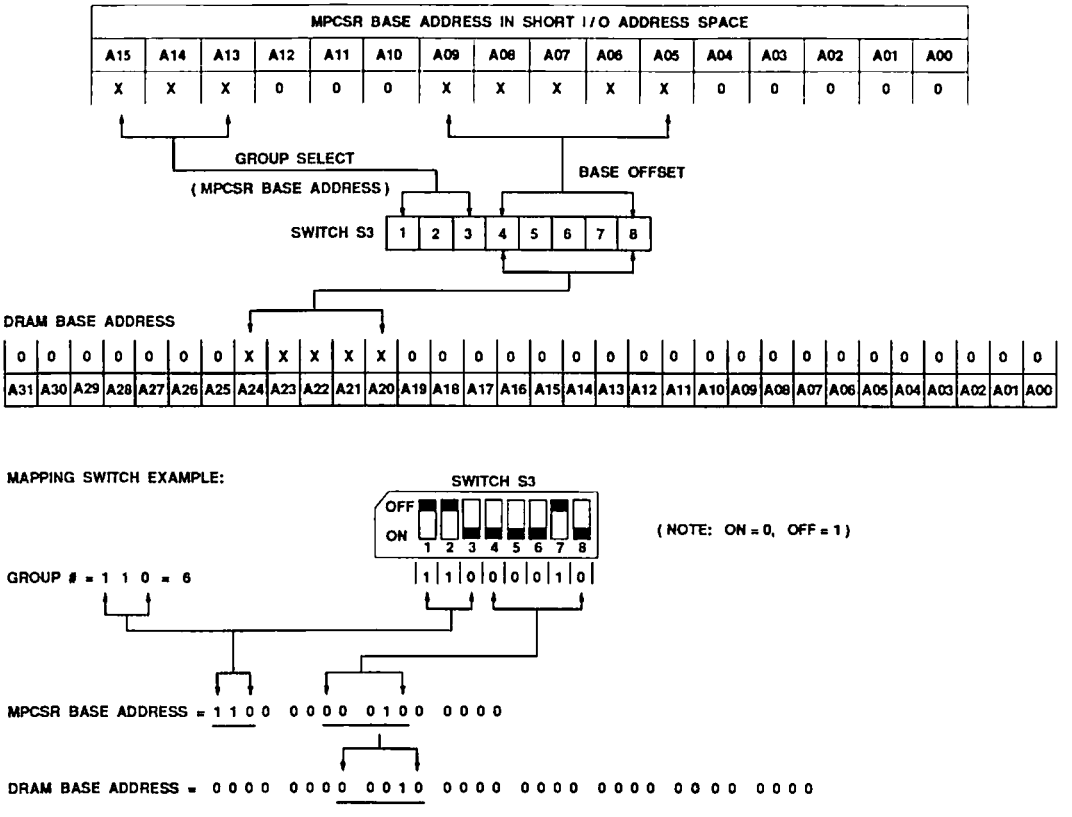


FIGURE 4-12. MPCSR AND DRAM ADDRESS MAPPING

<VSBCSR> Physical Address: $FFFA0000 (Read/Write) RC = FFFF

D31	D25	D15	D11	D00
NA	NA	STATUS	CONTROL	

Bit 00 SCON* < VSBbus System Controller>

SCON* selects the VSBchip as the System Controller. VSBbus SCON* does not affect VMEbus system controller selection.

Bit 01 Not Used

Bit 02 BLOCKEN* < Block Transfer Enable>

BLOCKEN* is used to enable a master block transfer. This bit should never be written to zero on the MVME135/136.

Bit 03 10* < 010 Processor Select>

10*, when asserted, selects the MC68010 mode and when negated selects the MC68020 mode. This bit should never be written to zero on the MVME135/136.

Bit 04 VSBDEN < VSBbus Decode Enable>

VSBDEN, when asserted allows the AS* signal to generate the PAS* signal without waiting for QAS*, thus allowing decode on VSBbus slaves to determine which bus (VSBbus or VMEbus) will be used. If a VSBbus slave is not found, the cycle is automatically directed to VMEbus.

Bit 05 READONLY* < VSBbus Read Only>

READONLY* prevents writes from occurring on the VSBbus from this master. Write cycles are automatically directed to VMEbus for cache monitoring, when READONLY* is asserted.

Bit 06 VSBEN* < VSBbus Enable>

VSBEN* enables the master mode if the VSBbus device SLAVE* pin is negated. On the MVME135/136, the SLAVE* pin is pulled high. Therefore, slave accesses to the MVME135/136 over VSBbus cannot occur.

Bit 07 Not Used

Bit 08 ENT00* < Enable Timeout Option 0>
Bit 09 ENT01* < Enable Timeout Option 1>

The VSBchip implements the bus timer function with various timeout periods. The timeout period may be chosen to be 64 microseconds,

128 microseconds, 256 microseconds, or infinite by setting bits Ø8 and Ø9 in the control register. The timeout counter is started when PAS* is asserted and is disabled when PAS* is negated. If the counter times out before the PAS* signal is negated the ERR* signal is asserted and the BUSTIMEOUT* bit is set in the status register. The times given are for CLK equal to 16.67 MHz.

ENTO1*	ENTOØ*	Timeout Period
1	1	Infinite
1	Ø	256 microseconds
Ø	1	128 microseconds
Ø	Ø	64 microseconds

Bit 1Ø ROBIN* < Round Robin Fairness Requester>

ROBIN* enables the fairness mode in the bus requester when asserted. Bus bandwidth is shared equally among VSBbus masters that all have fairness mode. When ROBIN* is negated, the bus bandwidth is prioritized by a daisy-chain scheme where the modules closest to the system controller will receive most of the available bus bandwidth.

Bit 11 WRERROR* < Write Error Status Bit>

WRERROR* reports the fact that a write to a read only bus was attempted.

Bit 12 BUSTIMEOUT* < VSBbus Timeout>

BUSTIMEOUT* reports the fact that a VSBbus timeout has occurred.

Bit 13 ASACKØ* < Address And Size Status Ø>

ASACKØ* reports the status of the bus ASACKØ* line at the time of the last bus error. Together with ASACK1*, it indicates the response and size of the slave module accessed. Refer to the following chart.

ASACK1*	ASACKØ*	Status
1	1	No Slave Response
1	Ø	8-Bit Slave Response
Ø	1	16-Bit Slave Response
Ø	Ø	32-Bit Slave Response

Bit 14 ASACK1* < Address And Size Status 1>

ASACK1* reports the status of the bus ASACK1* line at the time of the last bus error. Together with ASACKØ*, it indicates the response and size of the slave module accessed. Refer to the chart above.

Bit 15 ERR* < VSBbus Error Status>

ERR*, when asserted, reports that a bus error has occurred. This bit indicates status only for VSBbus cycles that are terminated with a VSBbus error.

4.18 CONFIGURING A VME SUBSYSTEM BUS

The MVME135/136 module gains much of its power and flexibility by use of the VME Subsystem Bus (VSBbus). VSBbus is implemented in a gate array device and performs almost all VSBbus requirements.

VSBbus on the MVME135/136 is a master only, multiple master interface, meaning that the MVME135/136 cannot be accessed over VSBbus. However, multiple MVME135/136s can be used on a single subsystem and share VSBbus slave resources. VSBbus can be implemented with a 64-pin ribbon cable. In this configuration, only two MVME135/136s may share VSBbus with up to four VSBbus slave devices. It is important to note that when a ribbon cable is used, at least one of the slave devices must connect VSB BGIN* to VSB BG* (P2 A31 to P2 C32).

VSBbus backplanes are available in varied configurations, typically up to six slots. These backplanes plug into P2 connectors on the VME P2 backplane. VSBbus backplanes are needed for applications requiring more than two VSBbus masters. The backplane will require jumpering for configuring VSB BGIN* to BG* for each slot where a VSBbus master such as the MVME135/136 is installed.

Socketed signal terminators (R2Ø and R21) are provided on the MVME135/136 module. If a ribbon cable is used, these terminators do not require reconfiguration and should remain installed in the module.

If a VSBbus backplane is used that provides proper VSBbus signal termination, R2Ø and R21 must be removed. Also, if more than two MVME135/136s are installed in single subsystem, then the terminators should only be installed in the modules that reside at each end of the subsystem bus. Proper VSBbus signal termination is essential for reliable VSBbus operation. Refer to the VME Subsystem Bus (VSBbus) Specification for more detailed information on VSBbus configuration and signal terminators.

CHAPTER 5 - SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the connector pin signal descriptions, parts list with associated parts location diagram, and the schematic diagram for the different versions of the MVME135/136 module, the 1Mb and 4Mb DRAM mezzanine board, and the PMMU by-pass board.

5.2 INTERCONNECTION SIGNALS

The MVME135/136 module interconnects with VMEbus through connector P1. Connector P2 interconnects the MVME135/136 module with the extended VMEbus and the secondary extension bus, VSBbus.

5.2.1 Connector P1 Interconnect Signals

Connector P1 is a standard DIN triple row, 96-pin male connector. All Motorola VMEbus specifications are met by the MVME135/136 module. The pin connections, VMEbus signal mnemonics, and signal descriptions for the P1 connector are provided in Table 5-1. Refer to the ANSI/IEEE Standard 1014-1987 (Versatile Backplane Bus: VMEbus) for a complete description of the VMEbus signals.

TABLE 5-1. CONNECTOR P1 INTERCONNECT SIGNALS

Pin Number	Signal Mnemonic	Signal Name and Description
A1-A8	D00-D07	DATA BUS (bits 0-7) - Eight of 16 three-state bidirectional data lines that provide the data path between the data transfer bus master and slave.
A9	GND	GROUND
A10	SYSCLK	SYSTEM CLOCK - A constant 16 MHz clock signal that is independent of processor speed or timing and is used as a timing reference.
A11	GND	GROUND
A12	DS1*	DATA STROBE 1 - A three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines D08 through D15 and data lines D24 through D31 for 32-bit data transfers.

TABLE 5-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A13	DSØ*	DATA STROBE Ø - A three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines DØØ through DØ7 and data lines D16 through D23 for 32-bit data transfers.
A14	WRITE*	WRITE - A three-state driven signal that specifies that the data transfer cycle in progress is either a read or a write. A high level indicates a read operation; a low level indicates a write operation.
A15	GND	GROUND
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - An open-collector driven signal generated by a data transfer bus slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
A17	GND	GROUND
A18	AS*	ADDRESS STROBE - The falling edge of this signal is used to indicate that a valid address is on the address bus. AS* is an active low, TTL three-state signal.
A19	GND	GROUND
A2Ø	IACK*	INTERRUPT ACKNOWLEDGE - An open-collector driven input signal that indicates a VME interrupt acknowledge cycle. The VME system controller has been interrupted on one of seven levels and is now acknowledging the interrupt.
A21	IACKIN*	INTERRUPT ACKNOWLEDGE IN - The IACKIN* and IACKOUT* lines form a daisy-chained acknowledge signal. The IACKIN* input signal is connected directly to IACKOUT* on the MVME135/136.
A22	IACKOUT*	INTERRUPT ACKNOWLEDGE OUT - See IACKIN* (pin A21).

TABLE 5-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A23	AM4	ADDRESS MODIFIER (bit 4) - One of four input lines that provide additional information about the address bus, such as size, cycle type, and/or data transfer bus master identification.
A24-A27	AØ7-AØ4	ADDRESS BUS (bits Ø7-Ø4) - Four of 31 three-state input lines that specify an address in the memory map.
A28-A3Ø	AØ3-AØ1	ADDRESS BUS (bits Ø3-Ø1) - Three of 31 three-state input lines that specify an address in the memory map. During an interrupt acknowledge cycle, address bus lines AØ1 through AØ3 are used to indicate the interrupt level that is being acknowledged.
A31	-12V	-12 Vdc POWER - Used by system logic circuits.
A32	+15V	+5 Vdc POWER - Used by system logic circuits.
B1	BBSY*	VMEbus BUSY - An open-collector driven signal generated by the current Data Transfer Bus (DTB) master to indicate that it is using the bus.
B2	NC	NOT CONNECTED.
B3	ACFAIL*	SYSTEM AC POWER FAIL - An open-collector driven signal which indicates that the AC input to the power supply is not being provided or the required input voltage level is not being met.
B4	BGØIN*	BUS GRANT IN (level Ø) - The "bus grant in" and "bus grant out" form a daisy-chained bus grant. A grant received at the jumpered level indicates the module may become the bus master. The remaining three "bus grant in" lines are connected directly to their respective "bus grant out" lines.
B5	BGØOUT*	BUS GRANT OUT (level Ø) - see BGØIN* (pin B4).
B6	BG1IN*	BUS GRANT 1 IN - Same as BGØIN on pin B4.
B7	BG1OUT*	BUS GRANT 1 OUT - Same as BGØOUT on pin B5.

TABLE 5-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
B8	BG2IN*	BUS GRANT 2 IN - Same as BGØIN on pin B4.
B9	BG2OUT*	BUS GRANT 2 OUT - Same as BGØOUT on pin B5.
B1Ø	BG3IN*	BUS GRANT 3 IN - Same as BGØIN on pin B4.
B11	BG3OUT*	BUS GRANT 3 OUT - Same as BGØOUT on pin B5.
B12	BRØ*	BUS REQUEST (level Ø) - One of four open-collector driven signals that are generated by requesters. These signals indicate that a data transfer bus master in the daisy-chain requires access to the bus.
B13	BR1*	BUS REQUEST (level 1) - Same as BRØ* on pin B12.
B14	BR2*	BUS REQUEST (level 2) - Same as BRØ* on pin B12.
B15	BR3*	BUS REQUEST (level 3) - Same as BRØ* on pin B12.
B16-B19	AMØ-AM3	ADDRESS MODIFIER (bits Ø-3) - Same as AM4 on pin A23.
B2Ø	GND	GROUND
B21,B22	NC	NOT CONNECTED
B23	GND	GROUND
B24-B3Ø	IRQ7*-IRQ1*	INTERRUPT REQUEST (bits 7-1)- These signals are generated by an interrupter and carry the prioritized interrupt requests. Level 7 is the highest priority and level 1 the lowest.
B31	+5VSTDBY	+5Vdc STANDBY - This line supplies +5 Vdc to devices requiring battery backup.
B32	+5V	+5 Vdc POWER - Used by system logic circuits.
C1-C8	DØ8-D15	DATA BUS (bits 8-15) - Eight of 16 three-state bidirectional data lines that provide the data path between the data transfer bus master and slave.

TABLE 5-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C9	GND	GROUND
C1Ø	SYSFAIL*	SYSTEM FAILURE - An open-collector driven signal that indicates a failure has occurred in the system. SYSFAIL* may be generated by any module on the VMEbus.
C11	BERR*	BUS ERROR - An open-collector driven signal generated by a slave. BERR* indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
C12	SYSRESET*	SYSTEM RESET - An open-collector driven signal which, when low, will cause the system to be reset.
C13	LWORD*	LONGWORD - A three-state driven signal specifying that the cycle is a byte/word transfer (when high) or a longword transfer (when low).
C14	AM5	ADDRESS MODIFIER (bit 5) - Same as AM4 on pin A23.
C15-C3Ø	A23-AØ8	ADDRESS BUS (bits 23-Ø8) - 16 of 31 three-state input lines that specify an address in the memory map.
C31	+12V	+12 Vdc POWER - Used by system logic circuits.
C32	+5V	+5 Vdc POWER - Used by system logic circuits.

5.2.2 Connector P2 Interconnect Signals

Connector P2 is a standard DIN triple row, 96-pin male connector. Table 5-2 lists the extended VMEbus and the VSBbus signals.

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS

Pin Number	Signal Mnemonic	Signal Name and Description
A1	MADØØ	VSBbus MULTIPLEXED ADDRESS/DATA (bit ØØ) - One of 32 multiplexed address/data lines that are controlled by the three-state drivers on the master and slave devices and are use to broadcast or receive addresses and data over the VSBbus. All lines are active high, TTL three-state signals.
A2	MADØ2	VSBbus MULTIPLEXED ADDRESS/DATA (bit Ø2) - Same as MADØØ on pin A1.
A3	MADØ4	VSBbus MULTIPLEXED ADDRESS/DATA (bit Ø4) - Same as MADØØ on pin A1.
A4	MADØ6	VSBbus MULTIPLEXED ADDRESS/DATA (bit Ø6) - Same as MADØØ on pin A1.
A5	MADØ8	VSBbus MULTIPLEXED ADDRESS/DATA (bit Ø8) - Same as MADØØ on pin A1.
A6	MAD1Ø	VSBbus MULTIPLEXED ADDRESS/DATA (bit 1Ø) - Same as MADØØ on pin A1.
A7	MAD12	VSBbus MULTIPLEXED ADDRESS/DATA (bit 12) - Same as MADØØ on pin A1.
A8	MAD14	VSBbus MULTIPLEXED ADDRESS/DATA (bit 14) - Same as MADØØ on pin A1.
A9	MAD16	VSBbus MULTIPLEXED ADDRESS/DATA (bit 16) - Same as MADØØ on pin A1.
A1Ø	MAD18	VSBbus MULTIPLEXED ADDRESS/DATA (bit 18) - Same as MADØØ on pin A1.
A11	MAD2Ø	VSBbus MULTIPLEXED ADDRESS/DATA (bit 2Ø) - Same as MADØØ on pin A1.
A12	MAD22	VSBbus MULTIPLEXED ADDRESS/DATA (bit 22) - Same as MADØØ on pin A1.

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A13	MAD24	VSBbus MULTIPLEXED ADDRESS/DATA (bit 24) - Same as MADØØ on pin A1.
A14	MAD26	VSBbus MULTIPLEXED ADDRESS/DATA (bit 26) - Same as MADØØ on pin A1.
A15	MAD28	VSBbus MULTIPLEXED ADDRESS/DATA (bit 28) - Same as MADØØ on pin A1.
A16	MAD3Ø	VSBbus MULTIPLEXED ADDRESS/DATA (bit 3Ø) - Same as MADØØ on pin A1.
A17	GND	GROUND
A18	MIRQ*	VSBbus INTERRUPT REQUEST - This signal, when low, indicates that a secondary master or slave device is attempting to interrupt the primary master. This line is an active low, TTL open-collector signal.
A19	MDS*	VSBbus DATA STROBE - The falling edge of MDS* indicates that a valid data transfer will occur on the bus (MADØØ to MAD31) at this time. During write cycles, write data is valid at the falling edge of MDS*. This line is an active low, TTL three-state signal.
A2Ø	MWRITE*	VSBbus WRITE - This signal, when low, indicates that a write operation is to be performed and when high, indicates that a read operation will occur. MWRITE is valid when MAS* is asserted on the bus. This line is an active low, TTL three-state signal.
A21	SPACEØ	VSBbus SPACE SELECT Ø (bit Ø) - One of two signals that are driven by the active master and used to select either one of three address spaces (i.e., the System Address Space, the I/O Address Space, or the Alternate Address Space), or to initiate an interrupt acknowledge, or an arbitration cycle.
A22	SPACE1	VSBbus SPACE SELECT 1 (bit 1) - Same as SPACEØ on pin A21.

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A23	MBLOK*	VSBbus LOCK - This signal, when low, indicates the bus is locked and that no other master can obtain possession of the bus. MBLOK* is also used in certain modes to indicate that a block transfer cycle is in progress. This line is an active low, TTL three-state signal.
A24	MERR*	VSBbus ERROR - This signal, when low, is issued by the selected slave module to indicate a fault condition while attempting a data transfer operation. This would typically be the result of a parity error detected on a slave device. This line is an active low, TTL open-collector signal.
A25-3Ø	GND	GROUND
A31	MBGIN*	VSBbus GRANT IN - This input signal is generated by the arbiter or a requester. The "bus grant in" and "bus grant out" signals form a bus grant daisy-chain. MBGIN* indicates to the module receiving it, that it may use the VSBbus.
A32	MBR*	VSBbus REQUEST - This signal is an output from the requester and an input to the arbiter when system controller and to the requester at all times. MBR* is used by the arbiter to determine when another master needs the bus. MBR* is used by the requester to release the bus (ROR). This line is an active low, TTL three-state signal.
B1	+5V	+5 Vdc POWER - Used by system logic circuits.
B2	GND	GROUND
B3	P2B3	VMEbus RESERVED PIN - Optionally used by the MVME135/136 and MVME2Ø4-x system combination as a lock signal for VMEbus via jumper J1.
B4-B11	A24-A31	ADDRESS BUS (bits 24-31) - These are the eight optional three-state driven address lines which specify the extended VME memory address.
B12	GND	GROUND

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
B13	+5V	+5 Vdc POWER - Used by system logic circuits.
B14-B21	D16-D23	DATA BUS (bits 16-23) - Eight of the 16 bidirectional three-state driven data lines which provide the expanded data path between the DTB master and slave for the optional expanded data bus configuration.
B22	GND	GROUND
B23-B3Ø	D24-D31	DATA BUS (bits 24-31) - Eight of the 16 bidirectional three-state driven data lines which provide the expanded data path between the DTB master and slave for the optional expanded data bus configuration.
B31	GND	GROUND
B32	+5V	+5 Vdc POWER - Used by system logic circuits.
C1	MADØ1	VSBbus MULTIPLEXED ADDRESS/DATA (bit Ø1) - Same as MADØØ on pin A1.
C2	MADØ3	VSBbus MULTIPLEXED ADDRESS/DATA (bit Ø3) - Same as MADØØ on pin A1.
C3	MADØ5	VSBbus MULTIPLEXED ADDRESS/DATA (bit Ø5) - Same as MADØØ on pin A1.
C4	MADØ7	VSBbus MULTIPLEXED ADDRESS/DATA (bit Ø7) - Same as MADØØ on pin A1.
C5	MADØ9	VSBbus MULTIPLEXED ADDRESS/DATA (bit Ø9) - Same as MADØØ on pin A1.
C6	MAD11	VSBbus MULTIPLEXED ADDRESS/DATA (bit 11) - Same as MADØØ on pin A1.
C7	MAD13	VSBbus MULTIPLEXED ADDRESS/DATA (bit 13) - Same as MADØØ on pin A1.
C8	MAD15	VSBbus MULTIPLEXED ADDRESS/DATA (bit 15) - Same as MADØØ on pin A1.

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C9	MAD17	VSBbus MULTIPLEXED ADDRESS/DATA (bit 17) - Same as MADØØ on pin A1.
C1Ø	MAD19	VSBbus MULTIPLEXED ADDRESS/DATA (bit 19) - Same as MADØØ on pin A1.
C11	MAD21	VSBbus MULTIPLEXED ADDRESS/DATA (bit 21) - Same as MADØØ on pin A1.
C12	MAD23	VSBbus MULTIPLEXED ADDRESS/DATA (bit 23) - Same as MADØØ on pin A1.
C13	MAD25	VSBbus MULTIPLEXED ADDRESS/DATA (bit 25) - Same as MADØØ on pin A1.
C14	MAD27	VSBbus MULTIPLEXED ADDRESS/DATA (bit 27) - Same as MADØØ on pin A1.
C15	MAD29	VSBbus MULTIPLEXED ADDRESS/DATA (bit 29) - Same as MADØØ on pin A1.
C16	MAD31	VSBbus MULTIPLEXED ADDRESS/DATA (bit 31) - Same as MADØØ on pin A1.
C17-C2Ø	GND	GROUND
C21	MSIZØ	VSBbus SIZE (bit Ø) - One of two lines which in conjunction with MADØØ and MADØ1, determine the active portion of the data bus. This line is an active low, TTL three-state signal.
C22	MAS*	VSBbus ADDRESS STROBE - The falling edge of MAS* indicates that a valid address is present on the MADØØ to MAD31 bus. This line is an active low, TTL three-state signal.
C23	MSIZ1	VSBbus SIZE (bit 1) - Same as MSIZØ on pin C21.
C24	GND	GROUND
C25	MACK*	VSBbus DATA TRANSFER ACKNOWLEDGE - This signal is issued by a slave device to complete the handshake for a data transfer operation. This line is an active low, TTL three-state signal.

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C26	AC	VSBbus ADDRESS CYCLE COMPLETE - This signal is issued by a slave device to indicate that address decoding has been completed. All slave devices must allow AC to go high after the decode interval has elapsed regardless of whether the device is selected by the current address on the bus. AC is an active high, TTL open-collector signal.
C27	ASACK1*	VSBbus ADDRESS/SIZE ACKNOWLEDGE (bit 1) - One of two lines that are driven by VSBbus slave devices and are used to perform several functions. The slave device that is selected by address decoding must drive at least one ASACK* signal to control switching and multiplexed address/data bus from address to data. Secondly, ASACKØ* and ASACK1* are encoded to indicate to the master the size of the data bus for the slave module. Finally, ASACK* can be gated with signal AC on the master device. The condition of AC active and ASACK* inactive, while MAS* is asserted, is defined to indicate that no VSBbus slave module has decoded the address being driven at that time or that there are no VSBbus slave modules installed. This provides the VSBbus master the opportunity to switch to the VMEbus when VSBbus slaves are not responding. ASACKØ* and ASACK1* are active low, TTL open-collector signals.
C28	ASACKØ*	VSBbus ADDRESS/SIZE ACKNOWLEDGE (bit Ø) - Same as ASACK1* on pin C27.
C29	MCACHE*	VSBbus CACHEABLE - This signal is issued by a slave device at the same time that ASACKØ* and ASACK1* are issued to indicate that the current transfer is cacheable. MCACHE* remains inactive to indicate that the transfer is non-cacheable. This line is an active low, TTL open-collector signal.
C3Ø	WAIT*	VSBbus HOLD THIS CYCLE - This signal is an input line used only in the master mode to indicate that this VSBbus cycle should not be terminated until the signal is negated. The DSACK1* and DSACKØ* lines are not asserted until this line is negated.

TABLE 5-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C31	MBBSY*	VSBbus BUSY - This signal is driven by the current master to indicate that it is using the bus. When the master releases this line, the resultant rising edge causes the arbiter to sample the bus request line and grant the bus to the requester. This line is an active low, TTL open-collector signal.
C32	MBG*	VSBbus GRANT OUT - This line is the output of the on chip requester. MBG* is asserted whenever the module receives a bus request and is the system controller and does not need the bus or when it is not the system controller and it receives a bus grant in and it does not need the bus. This line is an active low, TTL open-collector signal.

5.2.3 Connector J3 Interconnect Signals

Connector J3 is a 27-pin, single-row connector used for connecting the MVME135/136 to the 1Mb or 4Mb DRAM mezzanine module. Table 5-3 list the pin connection, signal mnemonic, and signal description for the connector.

TABLE 5-3. CONNECTOR J3 INTERCONNECT SIGNALS

Pin Number	Signal Mnemonic	Signal Name and Description
1-1Ø	LDØØ-LD1Ø	LOCAL DATA BUS (bits ØØ-1Ø) - Eleven of 32 local data lines that are connected directly to the MC68Ø2Ø microprocessor.
12	GND	GROUND
13	+5V	+5 Vdc POWER - Used by system logic circuits.
14	WR1*	DRAM WRITE ENABLE BYTE 1 - This signal, when asserted, causes data to be written into local data bits LDØ8 through LD15.
15	WRØ*	DRAM WRITE ENABLE BYTE Ø - This signal, when asserted, causes data to be written into local data bits LDØØ through LDØ7.
16	CAS3*	DRAM COLUMN ADDRESS STROBE BYTE 3 - This signal, when asserted, strobes column addresses to local DRAMs connected to data bits LD24 through LD31.
17	WR2*	DRAM WRITE ENABLE BYTE 2 - This signal, when asserted, causes data to be written into local data bits LD16 through LD23.
18	CASØ*	DRAM COLUMN ADDRESS STROBE BYTE Ø - This signal, when asserted, strobes column addresses to local DRAMs connected to data bits LDØØ through LDØ7.
19	CAS1*	DRAM COLUMN ADDRESS STROBE BYTE 1 - This signal, when asserted, strobes column addresses to local DRAMs connected to data bits LDØ8 through LD15.
2Ø	CAS2*	DRAM COLUMN ADDRESS STROBE BYTE 2 - This signal, when asserted, strobes column addresses to local DRAMs connected to data bits LD16 through LD23.

TABLE 5-3. CONNECTOR J3 CONNECTIONS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
21	WR3*	DRAM WRITE ENABLE BYTE 3 - This signal, when asserted, causes data to be written into local data bits LD24 through LD31.
22	GND	GROUND
23	+5V	+5 Vdc POWER - Used by system logic circuits.
24	REFRAS	DRAM REFRESH ROW ADDRESS STROBE - REFRAS is logically OR'ed with NORMRAS, with timing to perform CAS before RAS refresh.
25	NORMRAS	NORMAL DRAM CYCLE ROW ADDRESS STROBE - This DRAM address multiplexed control signal is used as a timing strobe for normal memory cycles.
26	ROWADDR*	ROW ADDRESS SELECT - This signal is used to switch from row to column addresses on the DRAM Mezzanine.
27	MEZZERR*	MEZZANINE ERROR - This signal is asserted when the mezzanine parity detection circuitry has detected a single-bit error.

5.2.4 Connector J4 Interconnect Signals

Connector J4 is a 57-pin, double-row connector used for connecting the MVME135/136 to the 1Mb or 4Mb DRAM mezzanine module. Table 5-4 list the pin connection, signal mnemonic, and signal description for the connector.

TABLE 5-4. CONNECTOR J4 INTERCONNECT SIGNALS

Pin Number	Signal Mnemonic	Signal Name and Description
1	LD16	LOCAL DATA BUS (bit 16) - One of 32 local data lines that are connected directly to the MC68Ø2Ø microprocessor.
2	LD24	LOCAL DATA BUS (bit 24) - Same as LD16 on pin 1.
3	LD17	LOCAL DATA BUS (bit 17) - Same as LD16 on pin 1.
4	LD25	LOCAL DATA BUS (bit 25) - Same as LD16 on pin 1.
5	LD18	LOCAL DATA BUS (bit 18) - Same as LD16 on pin 1.
6	LD26	LOCAL DATA BUS (bit 26) - Same as LD16 on pin 1.
7	LD19	LOCAL DATA BUS (bit 19) - Same as LD16 on pin 1.
8	LD27	LOCAL DATA BUS (bit 27) - Same as LD16 on pin 1.
9	+5V	+5 Vdc POWER - Used by system logic circuits.
1Ø	GND	GROUND
11	LD2Ø	LOCAL DATA BUS (bit 2Ø) - Same as LD16 on pin 1.
12	LD28	LOCAL DATA BUS (bit 28) - Same as LD16 on pin 1.
13	LD21	LOCAL DATA BUS (bit 21) - Same as LD16 on pin 1.
14	LD29	LOCAL DATA BUS (bit 29) - Same as LD16 on pin 1.
15	LD22	LOCAL DATA BUS (bit 22) - Same as LD16 on pin 1.
16	LD3Ø	LOCAL DATA BUS (bit 3Ø) - Same as LD16 on pin 1.
17	LD23	LOCAL DATA BUS (bit 23) - Same as LD16 on pin 1.
18	LD31	LOCAL DATA BUS (bit 31) - Same as LD16 on pin 1.

TABLE 5-4. CONNECTOR J4 CONNECTIONS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
19	LD15	LOCAL DATA BUS (bit 15) - Same as LD16 on pin 1.
2Ø	LD14	LOCAL DATA BUS (bit 14) - Same as LD16 on pin 1.
21	LD12	LOCAL DATA BUS (bit 12) - Same as LD16 on pin 1.
22	LD13	LOCAL DATA BUS (bit 13) - Same as LD16 on pin 1.
23	LD11	LOCAL DATA BUS (bit 28) - Same as LD16 on pin 1.
24	GND	GROUND
25	+5V	+5 Vdc POWER - Used by system logic circuits.
26	NC	NOT CONNECTED.
27	PA21	PHYSICAL ADDRESS (bit 21) - One of 2Ø physical address lines used to address memory locations contained on the MVME135/136 DRAM mezzanine module.
28	NC	NOT CONNECTED.
29	PA19	PHYSICAL ADDRESS (bit 19) - Same as PA21 on pin 27.
3Ø	PA2Ø	PHYSICAL ADDRESS (bit 2Ø) - Same as PA21 on pin 27.
31	PA17	PHYSICAL ADDRESS (bit 17) - Same as PA21 on pin 27.
32	PA18	PHYSICAL ADDRESS (bit 18) - Same as PA21 on pin 27.
33	PA16	PHYSICAL ADDRESS (bit 16) - Same as PA21 on pin 27.
34	GND	GROUND
35	+5V	+5 Vdc POWER - Used by system logic circuits.
36	NC	NOT CONNECTED.

TABLE 5-4. CONNECTOR J4 CONNECTIONS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
37	PAØ3	PHYSICAL ADDRESS (bit Ø3) - Same as PA21 on pin 27.
38	PAØ2	PHYSICAL ADDRESS (bit Ø2) - Same as PA21 on pin 27.
39	PAØ5	PHYSICAL ADDRESS (bit Ø5) - Same as PA21 on pin 27.
4Ø	PAØ4	PHYSICAL ADDRESS (bit Ø4) - Same as PA21 on pin 27.
41	PAØ7	PHYSICAL ADDRESS (bit Ø7) - Same as PA21 on pin 27.
42	PAØ6	PHYSICAL ADDRESS (bit Ø6) - Same as PA21 on pin 27.
43	PA12	PHYSICAL ADDRESS (bit 12) - Same as PA21 on pin 27.
44	PA13	PHYSICAL ADDRESS (bit 13) - Same as PA21 on pin 27.
45	PA1Ø	PHYSICAL ADDRESS (bit 1Ø) - Same as PA21 on pin 27.
46	PA11	PHYSICAL ADDRESS (bit 11) - Same as PA21 on pin 27.
47	PAØ8	PHYSICAL ADDRESS (bit Ø8) - Same as PA21 on pin 27.
48	PAØ9	PHYSICAL ADDRESS (bit Ø9) - Same as PA21 on pin 27.
49	PA15	PHYSICAL ADDRESS (bit 15) - Same as PA21 on pin 27.
5Ø	PA14	PHYSICAL ADDRESS (bit 14) - Same as PA21 on pin 27.
51	+5V	+5 Vdc POWER - Used by system logic circuits.

TABLE 5-4. CONNECTOR J4 CONNECTIONS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
52	GND	GROUND
53	PWRITE	PHYSICAL WRITE - PWRITE controls the parity generate/detect mode on the DRAM mezzanine module.
54	NC	NOT CONNECTED.
55	PAREN*	DRAM PARITY ENABLE - This signal, when asserted, allows the DRAM mezzanine module to report parity errors on detection via the MEZZERR* signal.
56	WWP*	WRITE WRONG PARITY - This signal, when asserted, forces the DRAM mezzanine module into a diagnostic mode where parity is intentionally written incorrectly for testing purposes.

5.2.5 Connector J9 Interconnect Signals

Connector J9 is a standard RS-232C DB-9 9-pin female connector. Table 5-5 list the pin connection, signal mnemonic, and signal description for the connector.

TABLE 5-5. CONNECTOR J9 INTERCONNECT SIGNALS

Pin Number	Signal Mnemonic	Signal Name and Description
1	DCDB	DATA CARRIER DETECT (channel B) - DCDB is sent by the modem to the terminal to indicate that a valid carrier is being received.
2	RXDB	RECEIVE DATA (channel B) - Data to be transmitted is furnished on this line to the modem from the terminal.
3	TXDB	TRANSMIT DATA (channel B) - Data that is demodulated from the receiver line is presented to the terminal by the modem.
4	DTRB	DATA TERMINAL READY (channel B) - This signal from the terminal to the modem indicates that the terminal is ready to send or receive data.
5	SG	SIGNAL GROUND
6	DSRB	DATA SET READY (channel B) - DSRB is a function supplied by the modem to the terminal to indicate that the modem is ready to transmit data.
7	RTSB	REQUEST TO SEND (channel B) - RTSB is supplied by the terminal to the modem when it is required to transmit a message. With RTSB off, the modem carrier remains off. When RTSB is turned on, the modem immediately turns on the carrier.
8	CTSB	CLEAR TO SEND (channel B) - CTSB is a function supplied to the terminal by the modem, and indicates that it is permissible to begin transmission of a message. When using a modem, CTSB follows the off-to-on transition of RTSB after a time delay.
9	FG	NOT CONNECTED.

5.2.6 Connector J1Ø Interconnect Signals

Connector J1Ø is a standard RS-232C DB-9 9-pin female connector. Table 5-6 list the pin connection, signal mnemonic, and signal description for the connector.

TABLE 5-6. CONNECTOR J1Ø INTERCONNECTION SIGNALS

Pin Number	Signal Mnemonic	Signal Name and Description
1	DCDA	DATA CARRIER DETECT (channel A) - DCDA is sent by the modem to the terminal to indicate that a valid carrier is being received.
2	RXDA	RECEIVE DATA (channel A) - Data to be transmitted is furnished on this line to the modem from the terminal.
3	TXDA	TRANSMIT DATA (channel A) - Data that is demodulated from the receiver line is presented to the terminal by the modem.
4	DTRA	DATA TERMINAL READY (channel A) - This signal from the terminal to the modem indicates that the terminal is ready to send or receive data.
5	SG	SIGNAL GROUND
6	DSRA	DATA SET READY (channel A) - DSRA is a function supplied by the modem to the terminal to indicate that the modem is ready to transmit data.
7	RTSA	REQUEST TO SEND (channel A) - RTSA is supplied by the terminal to the modem when it is required to transmit a message. With RTSB off, the modem carrier remains off. When RTSB is turned on, the modem immediately turns on the carrier.
8	CTSA	CLEAR TO SEND (channel A) - CTSA is a function supplied to the terminal by the modem, and indicates that it is permissible to begin transmission of a message. When using a modem, CTSB follows the off-to-on transition of RTSB after a time delay.
9	FG	NOT CONNECTED.

5.3 PARTS LIST

The reference designation, part number, and description for each component of the different versions of the MVME135/136 are listed in Table 5-7. The components for the 1Mb DRAM mezzanine module are listed in Table 5-8. The components for the 4Mb DRAM mezzanine module are listed in Table 5-9. The components for the PMMU by-pass board are listed in Table 5-10.

The parts location diagram (2 sheets) for the current five versions of the MVME135/136 is illustrated in Figure 5-1. Figures 5-2 and 5-3 illustrate the 1Mb and 4Mb DRAM mezzanine module, respectively. Figure 5-4 illustrates the PMMU by-pass board for those MVME135/136 versions not using the PMMU device.

These lists reflect the latest issue of all MVME135/136 hardware at the time of the printing of this user's manual.

TABLE 5-7. MVME135/136 PARTS LIST

Reference Designation	Motorola Part Number	Description
---	84-W844ØBØ1	Printed wiring board assembly, MVME135/136 (used on MVME135/135-1/136/136A only)
---	84-W844ØBØ1E	Printed wiring board assembly, MVME135/136 (used on MVME135A only)
C1-14, C18-21, C26-32, C34-39, C42,C43, C45-47	21NW9632AØ3	Capacitor, ceramic, axial, Ø.1 uF, 5Ø Vdc
C48-52,	21NW9632AØ3	Capacitor, ceramic, axial, Ø.1 uF, 5Ø Vdc (used on MVME135A only)
C15,C17	21NW96Ø4A11	Capacitor, ceramic, 47 uF, 5Ø Vdc
C16,C33, C44	23NW9618A71	Capacitor, electrolytic, 47 uF, 1Ø Vdc
C22-25	21NW97Ø2A21	Capacitor, ceramic, radial, Ø.1 uF, 5Ø Vdc
C4Ø	21NW9629AØ1	Capacitor, mica, radial, 5 pF, 5ØØ Vdc
C41	21NW96Ø4A4Ø	Capacitor, ceramic, radial, 1Ø pF, 5Ø Vdc

TABLE 5-7. MVME135/136 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
CR1	48NW96Ø7AØ1	Rectifier, 1N4ØØØ1 (used on MVME135A only)
DL1	51NW9615T55	IC, DS1ØØØ-1ØØ
DL2	Ø1NW98Ø4C45	Delay module, 5Ø nsec
DL3	Ø1NW9615U81	IC, DS1ØØØ-15Ø
DL4	Ø1NW98Ø4C8Ø	Delay module, 1ØØ nsec (used on MVME135/136/136A only)
DL4	Ø1NW98Ø4D19	Delay module, 8Ø nsec (used on MVME135-1 only)
DL4	Ø1NW98Ø4D53	Delay module, 125 nsec (used on MVME135A only)
---	Ø9NW9811A29	Socket, IC, DIL, 14-pin (1 req'd)(use at DL4)
DS1,DS2	48NW9612A49	LED, red
DS3	48NW9612A59	LED, green
J3	28NW98Ø2HØ8	Connector, single-row, 27-pin
J4	28NW98Ø2H1Ø	Connector, double-row, 56-pin
J7	28NW98Ø2D86	Connector, single-row, 3-pin
J8	28NW98Ø2D86	Connector, single-row, 3-pin (used on MVME135A only)
J9,J1Ø	28NW98Ø2G79	Connector, right-angle, 9-pin
P1,P2	28NW98Ø2E51	Connector, plug, 96-pin
---	Ø5NW9ØØ7A26	Eyelet, .Ø89"OD x .344 L (4 req'd)(used at P1 and P2)
R1,R5,R8, R11-15, R18,R19	51NW9626B56	Resistor network, nine 1ØK ohm

TABLE 5-7. MVME135/136 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
R2,R3	51NW9626A56	Resistor network, four 22 ohm
R4	51NW9626A69	Resistor network, seven 1K ohm
R6,R10	51NW9626A45	Resistor network, nine 2.2K ohm
R7	51NW9626B76	Resistor network, seven 680K ohm
R9	51NW9626B55	Resistor network, nine 4.7K ohm
R16,R22	06SW-124A41	Resistor, film, 1/4W, 5%, 470 ohm
R17	51NW9626A49	Resistor network, seven 10K ohm
R20,R21	51NW9626A75	Resistor network, eight 330/470 ohm
---	09-W4659B10	Socket, IC, SIL, 10-pin (2 req'd)(used at R20 and R21)
R23	51NW9626B04	Resistor network, seven 2K ohm
R24	51NW9626A84	Resistor network, five 330 ohm
R25	51NW9626A40	Resistor network, five 1K ohm (used on MVME135A only)
R26	51NW9626B56	Resistor network, nine 10K ohm (used on MVME135A only)
S1,S2	40NW9801B70	Switch, pushbutton, SPDT
---	38NW9404C11	Cap, switch, black (1 req'd)(used at S1)
---	38NW9404C12	Cap, switch, red (1 req'd)(used at S2)
S3	40NW9801B35	Switch, DIP, SPST, 8-position
S4	40NW9801B76	Switch, DIP, SPST, 10-position
U1,U3, U4,U55	51NW9615R38	IC, SN74LS794N

TABLE 5-7. VME135 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U2	51AW5238B01	IC, Programmed, PAL 33
U5-8	51NW9615M90	IC, 74F245PC
U9	51NW9615F79	IC, SN74S240N
U10	51NW9615B59	IC, MC7407P
U11	51NW9615E93	IC, SN74LS14N
U12,U13, U81,U82	51NW9615R36	IC, 74F543SPC
---	09-W4659B12	Socket, IC, SIL, 12-pin (2 req'd)(used at U13)
U14	51AW4804C27	IC, Programmed, PAL 13
U15	51AW5239B01	IC, Programmed, PAL 34 (used on MVME135/135-1/136/136A only)
U15	51AW5239B06	IC, Programmed, PAL 34 (used on MVME135A only)
U16	51AW5471B01	IC, Programmed, PAL 12
U17	51AW5243B02	IC, Programmed, PAL 32
U18	51AW5238B02	IC, Programmed, PAL 7
U19	51-W5552B06	IC, Programmed, PAL 10
U20,U27	51NW9615F38	IC, SN74LS393N
U21	51NW9615G81	IC, SN74LS132N
U22	51AW5120B85	IC, Programmed, PAL 22
U23,U88	51NW9615R55	IC, N74F38N
U24	51AW5240B03	IC, Programmed, PAL 31
---	09NW9811A78	Socket, IC, DIL, 20-pin (1 req'd)(used at U24)

TABLE 5-7. MVME135/136 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U25,U45, U47,U68	51NW9615R26	IC, SN74ALS645-1N
U26	51NW9615J39	IC, 74F74PC
U28	51AW5237BØ1	IC, Programmed, PAL 25
U29	51AW524ØBØ4	IC, Programmed, PAL 35
U3Ø	51AW5392BØ1	IC, Programmed, PAL 27
U31	51AW48Ø4B58	IC, Programmed, PAL 26
U32	51AW55Ø8BØ1	IC, Programmed, PAL 24
U33	51AW524ØBØ5	IC, Programmed, PAL 36
U34,U46, U87	51NW9615K47	IC, 74F244PC
---	Ø9-W4659B1Ø	Socket, IC, SIL, 1Ø-pin (1 req'd)(used at U87) (used on MVME135A only)
U35,U92	51NW9615FØ2	IC, SN74LS244N
U36	51AW5243BØ3	IC, Programmed, PAL 19
U37	51AW5241BØ2	IC, Programmed, PAL 18
U38	51NW9615K69	IC, 74F1ØPC
U39	51NW9615K65	IC, 74F11PC
U4Ø,U79	51NW9615J39	IC, 74F74PC
U41	51AW1Ø86X15	IC, Programmed
U42	51NW9615P17	IC, 74F1ØPC
U43	51AW5387BØ2	IC, Programmed, PAL 2Ø
U44	51AW5241BØ3	IC, Programmed, PAL 16

TABLE 5-7. MVME135/136 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U48	51AW48Ø4B57	IC, Programmed, PAL 14
---	Ø9-W4659B1Ø	Socket, IC, SIL, 1Ø-pin (2 req'd)(used at U48)
U49	51AW5389BØ1	IC, Programmed, PAL 17
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U49)
U5Ø	51AW4939BØ5	IC, Programmed, PAL 21
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U5Ø)
U51	51NW9615K71	IC, 74FØ4PC
U52	51NW9615K73	IC, 74FØØPC
U53	51NW9615C6Ø	IC, MC3456P
U57	51AW5Ø11B1Ø	IC, Programmed, PAL 3Ø
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U57)
U58	51AW5388BØ1	IC, Programmed, PAL 29
---	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U58) (used on MVME135/135-1/136/136A only)
---	Ø9-W4659B12	Socket, IC, SIL, 12-pin (1 req'd)(used at U58) (used on MVME135A only)
U59	51AW4697B68	IC, Programmed, PAL 8 (used on MVME135/135-1/136 only)
U59	51-W5388B25	IC, Programmed, PAL 8 (used on MVME135A/136A only)
---	Ø9-W4659B12	Socket, IC, SIL, 12-pin (2 req'd)(used at U59)

TABLE 5-7. MVME135/136 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U6Ø	51AW48Ø4C29	IC, Programmed, PAL 2 (used on MVME135/135-1/136 only)
U6Ø	51-W48Ø4C58	IC, Programmed, PAL 2 (used on MVME135A/136A only)
---	Ø9-W4659B1Ø	Socket, IC, SIL, 1Ø-pin (2 req'd)(used at U6Ø)
U61,U72	51NW9615K72	IC, 74FØ2PC
U62	51AW48Ø4C28	IC, Programmed, PAL 3
---	Ø9-W4659B1Ø	Socket, IC, SIL, 1Ø-pin (2 req'd)(used at U62)
U63,U74	51NW9615K7Ø	IC, 74FØ8PC
U64	Ø1-W3464BØ1	Printed wiring assembly, by-pass board (used on MVME135/135-1/135A only)
U64	51NW9615Y22	IC, XC68851RC16A (used on MVME136/136A only)
---	Ø9NW9811B14	Socket, IC, PGA, 144-pin (1 req'd)(used at XU64)
U65	51NW9615T12	IC, MC68881RC16B (used on MVME135/135A/136/136A only)
U65	51NW9615U64	IC, MC68881RC2ØB (used on MVME135-1 only)
---	Ø9NW9811A71	Socket, IC, PGA, 68-pin (1 req'd)(used at U65)
U66	51AW55Ø8BØ3	IC, Programmed, PAL 37 (used on MVME135/135-1 only)
U66	51-W55Ø8BØ5	IC, Programmed, PAL 37 (used on MVME135A/136/136A only)
---	Ø9-W4659B1Ø	Socket, IC, SIL, 1Ø-pin (2 req'd)(used at U66)

TABLE 5-7. MVME135/136 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U67	51AW524ØBØ2	IC, Programmed, PAL 23
---	Ø9-W4659B1Ø	Socket, IC, SIL, 1Ø-pin (2 req'd)(used at U67)
U69	51AW48Ø4C15	IC, Programmed, PAL 4
---	Ø9-W4659B1Ø	Socket, IC, SIL, 1Ø-pin (2 req'd)(used at U69)
U7Ø	51AW5243BØ1	IC, Programmed, PAL 15
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U7Ø)
U71	51AW4591C66	IC, Programmed, PAL 9
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U71)
U73	51NW9615R89	IC, MC68Ø2ØRC16BE (used on MVME135/135A/136/136A only)
U73	51NW9615T26	IC, MC68Ø2ØRC2ØBE (used on MVME135-1 only)
---	Ø9NW9811B12	Socket, IC, PGA, 124-pin (2 req'd)(used at U73)
U74	51NW9615K7Ø	IC, 74FØ8PC (used on MVME135A only)
U75	51NW9615W77	IC, XVSB24ØØ
---	Ø9NW9811B33	Socket, IC, PGA, 132-pin (1 req'd)(used at U75)
U76	51AW4939BØ3	IC, Programmed, PAL 8
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U76) (used on MVME135/135-1/136/136A only)

TABLE 5-7. MVME135/136 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
---	Ø9-W4659B1Ø	Socket, IC, SIL, 1Ø-pin (1 req'd)(used at U76) (used on MVME135A only)
U77,U78	51NW9615S83	IC, MC145406P
U8Ø	51AW48Ø4B55	IC, Programmed, PAL 5
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U8Ø)
U83	51AW4939BØ4	IC, Programmed, PAL 11
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U83)
U84	51-W5449B34	IC, Programmed, PAL 6
---	Ø9NW9811A78	Socket, IC, DIL, 2Ø-pin (1 req'd)(used at U84)
U85	51NW9615E96	IC, SN74LS245
U86	51AW48Ø4C31	IC, Programmed, PAL 1
---	Ø9-W4659B1Ø	Socket, IC, SIL, 1Ø-pin (2 req'd)(used at U86)
U89	51NW9615P22	IC, MC68681P
---	Ø9-W4659B2Ø	Socket, IC, SIL, 2Ø-pin (2 req'd)(used at U89)
U9Ø	51NW9615C21	IC, SN74LSØ4N
U91	51NW9615K66	IC, 74F32PC
U93	51NW9615N68	IC, Z8Ø36APS
---	Ø9-W4659B2Ø	Socket, IC, SIL, 2Ø-pin (2 req'd)(used at U93)
Y1	48AW1Ø15BØ9	Crystal oscillator, 16.Ø MHz

TABLE 5-7. MVME135/136 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
Y2	48AW1Ø15B18	Crystal oscillator, 16.667 MHz (used with MVME135/135A/136/136A only)
Y2	48AW1Ø15BØ3	Crystal oscillator, 2Ø.ØØ MHz (used with MVME135-1 only)
---	Ø9NW9811A29	Socket, IC, DIL, 14-pin (1 req'd)(used at Y2)
Y3	48AW96Ø6A54	Crystal oscillator, 3.6864 MHz
---	11NW92Ø1A26	Tape, foam, 1/2 x 1/16 (.5 inch req'd)(used at Y3)
---	47NW94Ø5A28	Jackpost, assembly (2 req'd)
---	29NW98Ø5B17	Jumper, insulated, shorting (1Ø req'd)[used at J2(1-2)(5-6)(7-8)(9-11) (1Ø-12)(16-18),J6(1-2),J7(2-3),J12(1-2), J13(4-6)]
---	29NW98Ø5B17	Jumper, insulated, shorting (1 req'd)[used at J8(1-2)] (used on MVME135A/136A only)
---	67NW9415A17	Kit, 6 component, ejector handle (1 req'd)
---	33-W5Ø89B35	Nameplate, MVME135 (1 req'd) (used on MVME135 only)
---	33-W4577BØ1	Nameplate, MVME135-1 (1 req'd) (used on MVME135-1 only)
---	33-W5686BØ1A	Nameplate, MVME135A (1 req'd) (used on MVME135A only)
---	33-W5Ø89B52	Nameplate, MVME136 (1 req'd) (used on MVME136/136A only)

TABLE 5-7. MVME135/136 PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
---	33-W5Ø89BØ1	Nameplate, Motorola logo (1 req'd)
---	64-W5164BØ1	Panel, front, MVME135
---	29NW98Ø5CØ7	Pin, Ø.Ø25-inch square, auto-insert (38 req'd)(used at E1,J1,J2,J6,J11,J12, J13,J14)
---	Ø1-W3443BØ1	Printed wiring board assembly, mezzanine, 1Mb, 7Ø nanosecond (1 req'd) (used with MVME135/136 only)
---	Ø1-W3443BØ2	Printed wiring board assembly, mezzanine, 1Mb, 6Ø nanosecond (1 req'd) (used with MVME135-1 only)
---	Ø1-W3486BØ1A	Printed wiring board assembly, mezzanine, 4Mb, 1ØØ nanosecond (1 req'd) (used with MVME135A/136A only)
---	42NW94Ø1B14	Screw, captive collar (2 req'd)
---	Ø3NW9ØØ4B48	Screw, captive, M2.5 (2 req'd)
---	Ø9-W4659B14	Socket, IC, SIL, 14-pin (2 req'd)(used at U54)
---	Ø9-W4659B14	Socket, IC, SIL, 14-pin (2 req'd)(used at U56)
---	43NW9ØØ2B43	Support, printed wiring board (3 req'd)(used with mezzanine board)

APPENDIX A - MVME135/135-1/136 PAL2 SOURCE LISTING

```
   U6Ø    DEVICE     'P16L8'  "16L8B ON MVME135..51AW48Ø4C29";

   PA22              "I"      PIN IN U6Ø 1;
   PA24              "I"      PIN 2;
   PA27              "I"      PIN 3;
   PA31              "I"      PIN 4;
   PA28              "I"      PIN 5;
   PA26              "I"      PIN 6;
   PA3Ø              "I"      PIN 7;
   PA25              "I"      PIN 8;
   PA29              "I"      PIN 9;
   PA23              "I"      PIN 11;
"!"UPPER1MB          "O"      PIN 12 = 'NEG';
"!"SEGMENT           "I/O"    PIN 13 = 'NEG,FEED<-PIN';
"!"VSBVME            "I/O"    PIN 14 = 'NEG,FEED<-PIN';
"!"<-24ADDR          "I/O"    PIN 15 = 'NEG,FEED<-PIN';
   OPTØ              "I/O"    PIN 16 = 'FEED<-PIN';
   PA2Ø              "I/O"    PIN 17 = 'FEED<-PIN';
   PA21              "I/O"    PIN 18 = 'FEED<-PIN';
"!"RAMSEL1           "O"      PIN 19 = 'NEG';

PALOW = !PA31 & !PA3Ø & !PA29 & !PA28 & !PA27 & !PA26 & !PA25 & !PA24;

PAHI  = PA31 & PA3Ø & PA29 & PA28 & PA27 & PA26 & PA25 & PA24;

EQUATIONS

!<-24ADDR = PALOW;

!VSBVME = !PA22;

!RAMSEL1 = PAHI & PA23 & PA22 & PA21 & !PA2Ø #
           OPTØ & PALOW & !PA23 & !PA22 & !PA21 & !PA2Ø;

!SEGMENT = PAHI & PA23 & PA22 & PA21 & PA2Ø;

!UPPER1MB = PAHI & PA23 & PA22 & PA21 & PA2Ø;

"CHECKSUM 2ACF"
"VSBVME MUST BE LOW TO DECODE VME ACCESSES."
"ADDED 2ND TERM TO SEGMENT...FXXXXXXX IS D16 ON VME.  6/26/87 JMS"
@INCLUDE 'U6Ø. INC';  "This line of source code is for"
                      "factory test, and must be deleted"
                      "or commented out when a custom"
                      "U6Ø is developed."

END PAL2
```

SIGNAL DESCRIPTIONS

The following outputs may be user customized to fit specific customer applications. These PAL equations may be changed if the customer has requirements for hardware configuration of VMEbus 32/24 address range or 32/16 data space. The target bus (VME or VSB) may also be hardware configured via this PAL. It should be noted that the granularity is limited to 1Mb boundaries. The number of PAL terms available may also limit the flexibility of the features provided by this PAL.

!ADDR23 - When low, indicates that 24-bit address modifier codes will be generated for VMEbus references that fall within this decoded address. The equation produces 24-bit address modifier codes when the physical address is $ØØØØØØØØ through ØØFFFFFF and VMEbus cycles occur (references to this address space may be VSB as well). Bit 2 of control register 5 will affect this bit. Refer to the description of CNT5 in the MVME135/136 hardware manual. This bit is provided as an aid to configure mixed A24 and A32 slaves in the same VME chassis.

!VSBVME - Used in conjunction with the VSBDEN bit in the VSBCSR. When VSBDEN is low, the target bus (VME or VSB) will depend upon this decode output, which when low the bus access will be explicitly VME or when high explicitly VSB. The output is currently programmed to alternate on 4Mb boundaries from VSBbus to VMEbus. Refer to the description of the VSBDEN bit in the MVME135/136 hardware manual under the VSBCSR description for further information.

!SEGMENT- When low, indicates that the decoded address space, for VMEbus references only, that will be forced to 16 bits. When !SEGMENT is high, the VMEbus data width is determined by CNT5 bit 1 (refer to the MVME135/136 hardware for CNT5 Bit 1). !SEGMENT is currently programmed to go low only for VMEbus short I/O bus cycles and memory mapped I/O bus cycles (see Figure 4-1Ø). If this bit is not used, it should be programmed to be a logic 1. This bit is provided as an aid to configure D16 and D32 slaves in the same VME chassis.

APPENDIX B - MVME135A/136A PAL2 SOURCE LISTING


```
   U60_4  DEVICE     'P16L8'  "16L8B ON MVME135..51AW480C58";

   PA22            "I"       PIN IN U60_4 1;
   PA24            "I"       PIN 2;
   PA27            "I"       PIN 3;
   PA31            "I"       PIN 4;
   PA28            "I"       PIN 5;
   PA26            "I"       PIN 6;
   PA30            "I"       PIN 7;
   PA25            "I"       PIN 8;
   PA29            "I"       PIN 9;
   PA23            "I"       PIN 11;
"!"UPPER1MB        "O"       PIN 12 = 'NEG';
"!"SEGMENT         "I/O"     PIN 13 = 'NEG,FEED_PIN';
"!"VSBVME          "I/O"     PIN 14 = 'NEG,FEED_PIN';
"!"_24ADDR         "I/O"     PIN 15 = 'NEG,FEED_PIN';
   OPT0            "I/O"     PIN 16 = 'FEED_PIN';
   PA20            "I/O"     PIN 17 = 'FEED_PIN';
   PA21            "I/O"     PIN 18 = 'FEED_PIN';
"!"RAMSEL1         "O"       PIN 19 = 'NEG';

PALOW = !PA31 & !PA30 & !PA29 & !PA28 & !PA27 & !PA26 & !PA25 & !PA24;

PAHI  = PA31 & PA30 & PA29 & PA28 & PA27 & PA26 & PA25 & PA24;

EQUATIONS

!_24ADDR = PALOW;

!VSBVME = !PA22;

!RAMSEL1 = PAHI & PA23 & !PA22 #
           OPT0 & PALOW & !PA23 & !PA22;

!SEGMENT = PAHI & PA23 & PA22 & PA21 & PA20:
           PA31 & PA30 & PA29 & PA28;

!UPPER1MB = PAHI & PA23 & PA22 & PA21 & PA20;

"CHECKSUM 2B9B"
"VSBVME MUST BE LOW TO DECODE VME ACCESSES."
"ADDED 2ND TERM TO SEGMENT...FXXXXXXX IS D16 ON VME. 6/26/87 JMS"
"PAL ALTERED TO ACCOMMODATE 4MB MEZZANINE ONLY. 6/26/87 JMS"
"CHANGED DECODING ON RAMSEL1 TO FF800000 - FFBFFFFF 7/8/87 JMS"
@INCLUDE 'U60_4.INC'; "This line of source code is for"
                      "factory test, and must be deleted"
                      "or commented out when a custom"
                      "U60 is developed."

END PAL2
```

B

SIGNAL DESCRIPTIONS

The following outputs may be user customized to fit specific customer applications. These PAL equations may be changed if the customer has requirements for hardware configuration of VMEbus 32/24 address range or 32/16 data space. The target bus (VME or VSB) may also be hardware configured via this PAL. It should be noted that the granularity is limited to half-Mb boundaries. The number of PAL terms available may also limit the flexibility of the features provided by this PAL.

!ADDR23 - When low, indicates that 24-bit address modifier codes will be generated for VMEbus references that fall within this decoded address. The equation produces 24-bit address modifier codes when the physical address is $ØØØØØØØØ through $ØØFFFFFF and VMEbus cycles occur (references to this address space may be VSBbus as well). Bit 2 of control register 5 will affect this bit. Refer to the description of CNT5 in the MVME135/136 hardware manual. This bit is provided as an aid to configure mixed A24 and A32 slaves in the same VME chassis.

!VSBVME - Used in conjunction with the VSBDEN bit in the VSBCSR. When VSBDEN is low, the target bus (VME or VSB) will depend upon this decode output, which when low the bus access will be explicitly VME or when high explicitly VSB. The output is currently programmed to alternate on 4Mb boundaries from VSBbus to VMEbus. Refer to the description of the VSBDEN bit in the MVME135/136 hardware manual under the VSBCSR description for further information.

!SEGMENT- When low, indicates that the decoded address space, for VMEbus references only, that will be forced to 16 bits. When !SEGMENT is high, the VMEbus data width is determined by CNT5 bit 1 (refer to the MVME135/136 hardware for CNT5 Bit 1). !SEGMENT is currently programmed to go low only for VMEbus short I/O bus cycles and memory mapped I/O bus cycles (see Figure 4-1Ø). If this bit is not used, it should be programmed to be a logic 1. This bit is provided as an aid to configure D16 and D32 slaves in the same VME chassis.

APPENDIX C - MVME135/136 LOCAL MEMORY MAP

LOCAL MEMORY MAP

Physical Address	Device
ØØØØØØØØ-FFDFFFFF	Off-board access, VSBbus/VMEbus: (4Gb minus 2Mb). An image of the local DRAM may appear here beginning at ØØØØØØØØ. VMEbus mastership must be gained to access this area except for ØØØØØØØØ to ØØØFFFFF in option Ø. (For MVME135/135-1/136 versions only)
ØØØØØØØØ-FF7FFFFF	Off-board access, VSBbus/VMEbus: (4Gb minus 4Mb). An image of the local DRAM may appear here beginning at ØØØØØØØØ. VMEbus mastership must be gained to access this area except for ØØØØØØØØ to ØØ3FFFFF in option Ø. (For MVME135A/136A version only)
FFEØØØØØ-FFEFFFFF	DRAM; (1Mb, see description for options Ø and 1 in section 4.15.2 (CNT5)). (For MVME135/135-1/136 versions only)
FF8ØØØØØ-FFBFFFFF	DRAM; (4Mb, see description for options Ø and 1 in section 4.15.2 (CNT5)). (For MVME135A/136A version only)
FFFØØØØØ-FFFEFFFF	Local resources; (1Mb minus 64Kb). SIO, ROM, LCLCSR, and MPCSR.
FFFFØØØØ-FFFFFFFF	Off-board access; VMEbus Short I/O; (64Kb) 16-bit address, R/W to the VMEbus, Short I/O address modifier will be generated.
Local resources:	
FFFØØØØØ-FFF1FFFF	EPROM; (128Kb = 2 x 27512 devices maximum).
FFF20000-FFF9FFFF	Not Used.
FFFAØØØØ-FFFAFFFF	VSBCSR; FFFAØØØØ to FFFAØØØ3 are the only valid addresses for the VSBCSR. Although VSB select will occur for any reference written in this 64Kb address space. Erroneous operation may result if access attempts occur to any VSBCSR address other than FFFAØØØX.

C

LOCAL MEMORY MAP (cont.)

Physical Address	Device
FFFB0000-FFFB002F	Timer, <STAT1>, <CNT1>.
FFFB0030	Not Used.
FFFB0031	Not Used.
FFFB0032	<STAT2>.
FFFB0033-FFFB0037	Not Used.
FFFB0038	<CNT2>.
FFFB0039	<CNT3>.
FFFB003A	<CNT4>.
FFFB003B	<CNT5>.
FFFB003C-FFFB003F	Not Used.
FFFB0040-FFFB004F	SIO.
FFFB0050-FFFB005F	Not Used.
FFFB0060-FFFB007F	MPCSR.
FFFB0080-FFFBFFFF	Not Used.
FFFC0000-FFFEFFFF	Not Used.