NUCLEAR DATA, INC.
Post Office Box 451
Palatine, Illinois 60067

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IM41-8001-01
SOFTWARE INSTRUCTION MANUAL
ND812 DIAGNOSTICS

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OPERATE - MEMORY REFERENCE INSTRUCTION TEST (ND41-8001)

I. INTRODUCTION

A. This program is designed to serve as a go-no go check of both classes of Operate Instructions and all forms of Single Word Memory Instructions using forward, reverse and indirect references.

B. PROGRAM AREA

$ØØØØ_8$ through $335Ø_8$.

C. STARTING ADDRESSES

$ØØØ2_8$ for a single step operation.
$ØØ21_8$ for repeat cycle.

D. EQUIPMENT CONFIGURATION

Minimum requirements are a ND-812 Central Processor equipped with an ASR33 Teletype. An optional peripheral is a high speed reader.

II. PROGRAM DESCRIPTION

The first half of this program tests operate instructions (using no memory reference instructions) starting with simple clear, complement, skip if zero, positive/negative, non-zero, etc. Tests for interfering instructions are included. MRI's beginning with jump, are tested individually to see if jump, load, store, add, subtract and jump to subroutine are performed correctly without interfering with the static registers.

The program stops on commission of an error. The address at which the program stopped can be referred to the DIAGNOSTIC STOP LIST for possible cause of failure.

On the completion of 4096 valid passes, the teletype prints "OPR-MRI OK".

III. OPERATOR OR USER CONTROL

Starting the program at $ØØØ2_8$ allows the user to single step seven basic instructions. Starting at location $ØØ21_8$ causes multiple passes if the Switch Register is non-zero.

This program can be chained to the Execute and Two-Word Instruction Test (ND41-8002) by changing the contents of location $333Ø_8$ (of this program) to $4ØØØ_8$. A non-zero Switch Register will also cause multiple passes in the "chained" mode if ND41-8002 is in core and location 72768 (of ND41-8002) has been modified for this mode.

After the commission of an error, the stop address should be referred to the DIAGNOSTIC STOP LIST. Depressing CONTINUE recovers the program from an error condition.

IV. OPERATION PROCEDURE

1. Load the Operate-Memory Reference Instruction Test Binary Loader (ND41-0005) for a detailed description of its use).

SINGLE STEP

2. Set Switch Register to $ØØØ2_8$.

3. Depress LOAD ADDRESS.

4. Depress START.

   Stop test. Program stops, PC is $ØØØ3_8$.

5. Depress CONTINUE.

   CLR J test. Program stops, PC is $ØØØ5_8$ and the J register is $ØØØØ_8$.

6. Set Switch Register to 7777_8.

7. Depress CONTINUE.

   LJSW test. Program stops, PC is $ØØØ7_8$ and the J register is 7777_8.

8. Depress CONTINUE.

   CLR J test. Program stops, PC is $ØØ11_8$ and the J register is $ØØØØ_8$.

9. Depress CONTINUE.

   CMP J test. Program stops, PC is $ØØ13_8$ and the J register is 7777_8.

10. Depress CONTINUE.

    CLR K test. Program stops, PC is 0015_8, J register is 7777_8 and the K register is $ØØØØ_8$.

11. Depress CONTINUE.

    CMP K test. Program stops, PC is $ØØ17_8$, J register is 7777_8 and the K register is 7777_8.

12. Depress CONTINUE.

    CMP J test. Program stops, PC is $ØØ21_8$, J register is $ØØØØ_8$ and the K register is 7777_8.

MULTIPLE PASS

13. If user just completed the single step procedure, depress CONTINUE. If not go to the next step.

14. Set Switch Register to $\emptyset\emptyset21_8$.

15. Depress LOAD ADDRESS.

16. Set Switch Register to any value for multiple passes and to zero for a single pass.

17. Depress START.

18. The test can be terminated by depressing STOP.

The following is a procedure for error analysis.

1. Place the SELECT REGISTER switch in the ADDRESS position and read the stop address from the SELECTED REGISTER lights.

2. Refer the stop address to the DIAGNOSTIC STOP LIST for cause of failure.

3. To recover from an error condition, depress CONTINUE.

V. ERROR DIAGNOSTICS

The program stops on commission of an error. The address at which the program stopped is indicated by the SELECTED REGISTER light when the SELECT REGISTER switch is pladed in the ADDRESS position. Refer to the DIAGNOSTIC STOP LIST (page 4) for cause of failure.

VI. COMMAND SUMMARY

None.

```
ND41-0001  DIAGNOSTIC STOP LIST                    8/15/70 -DB
OPERATE-MEMORY REFERENCE INSTRUCTION TEST SA=0002
PRINTS "OPR-MRI OK" EACH 4096 PASSES      SA=0021    5
```

STOP AT	INSTRUCTION TESTED	REGISTERS SHOULD BE : JR	KR	RR	SR	FL	OV	PR
0002	STOP	XXXX	XXXX	XXXX	XXXX	X	X	0003
0004	CLR J	0000	XXXX	XXXX	XXXX	X	X	0005
0006	LJSW	7777	XXXX	XXXX	XXXX	X	X	0007
0010	CLR J	0000	XXXX	XXXX	XXXX	X	X	0011
0012	CMP J	7777	XXXX	XXXX	XXXX	X	X	0013
0014	CLR K	7777	0000	XXXX	XXXX	X	X	0015
0016	CMP K	7777	7777	XXXX	XXXX	X	X	0017
0020	CMP J	0000	7777	XXXX	XXXX	X	X	0021

ABNORMAL STOPS :

STOP AT	INSTRUCTION TESTED	REGISTERS SHOULD BE : JR	KR	RR	SR	FL	OV	PR
0022	SIP 0 (SKIP)	XXXX	XXXX	XXXX	XXXX	X	X	0023
0025	IDLE	XXXX	XXXX	XXXX	XXXX	X	X	0026
0031	SIZ J	0000	0000	XXXX	XXXX	X	X	0032
0034	SNZ J	0000	0000	XXXX	XXXX	X	X	0035
0036	SIZ K	0000	0000	XXXX	XXXX	X	X	0037
0041	SNZ K	0000	0000	XXXX	XXXX	X	X	0042
0043	SIP J	0000	0000	XXXX	XXXX	X	X	0044
0046	SIN J	0000	0000	XXXX	XXXX	X	X	0047
0050	SIP K	0000	0000	XXXX	XXXX	X	X	0051
0053	SIN K	0000	0000	XXXX	XXXX	X	X	0054
0056	SIN J	7777	0000	XXXX	XXXX	X	X	0057
0061	SIP J	7777	0000	XXXX	XXXX	X	X	0062
0063	SNZ J	7777	0000	XXXX	XXXX	X	X	0064
0066	SIZ J	7777	0000	XXXX	XXXX	X	X	0067
0071	SNZ K	7777	0000	XXXX	XXXX	X	X	0072
0074	SIN K	7777	0000	XXXX	XXXX	X	X	0075
0100	SIN K	0000	7777	XXXX	XXXX	X	X	0101
0103	SIP K	0000	7777	XXXX	XXXX	X	X	0104
0105	SIZ J	0000	7777	XXXX	XXXX	X	X	0106
0110	SNZ J	0000	7777	XXXX	XXXX	X	X	0111
0113	SIN J	7777	7777	XXXX	XXXX	X	X	0114
0116	SIP J	7777	7777	XXXX	XXXX	X	X	0117
0121	SNZ J	7777	7777	XXXX	XXXX	X	X	0122

STOP AT	INSTRUCTION TESTED	REGISTERS SHOULD BE : JR	KR	RR	SR	FL	OV	PR
0124	SIZ J	7777	7777	XXXX	XXXX	X	X	0125
0126	SIN K	7777	7777	XXXX	XXXX	X	X	0127
0131	SIP K	7777	7777	XXXX	XXXX	X	X	0132
0133	SNZ K	7777	7777	XXXX	XXXX	X	X	0134
0136	SIZ K	7777	7777	XXXX	XXXX	X	X	0137
0141	CLR JK	0000	0000	XXXX	XXXX	X	X	0142
0143	SIZ K	0000	0000	XXXX	XXXX	X	X	0144
0146	CLR O	0000	0000	XXXX	XXXX	X	0	0147
0151	SNZ O	0000	0000	XXXX	XXXX	X	0	0152
0155	SIZ O	7777	7777	XXXX	XXXX	X	0	0156
0157	SIN J	7777	7777	XXXX	XXXX	X	0	0160
0161	SIN K	7777	7777	XXXX	XXXX	X	0	0162
0163	SIZ O	7777	7777	XXXX	XXXX	X	0	0164
0166	SNZ O (CMP O)	7777	7777	XXXX	XXXX	X	1	0167
0171	SIZ O	7777	7777	XXXX	XXXX	X	1	0172
0173	SIN J	7777	7777	XXXX	XXXX	X	1	0174
0175	SIN K	7777	7777	XXXX	XXXX	X	1	0176
0200	CLR JK O	0000	0000	XXXX	XXXX	X	0	0201
0202	SIZ K	0000	0000	XXXX	XXXX	X	0	0203
0204	SIZ O	0000	0000	XXXX	XXXX	X	0	0205
0210	CLR FLAG	0000	0000	XXXX	XXXX	0	0	0211
0213	SNZ FLAG	0000	0000	XXXX	XXXX	0	0	0214
0217	CMP FLAG	0000	0000	XXXX	XXXX	1	0	0220
0222	SIZ FLAG	0000	0000	XXXX	XXXX	1	0	0223
0227	SET FLAG	0000	0000	XXXX	XXXX	1	0	0230
0234	CLR JK O	7777	7777	XXXX	XXXX	1	1	0235
0237	SET FLAG	7777	7777	XXXX	XXXX	1	1	0240
0241	SET FLAG	7777	7777	XXXX	XXXX	1	1	0242
0243	SET FLAG	7777	7777	XXXX	XXXX	1	1	0244
0245	SET FLAG	7777	7777	XXXX	XXXX	1	1	0246
0251	CLR JK O	0000	0000	XXXX	XXXX	1	0	0252
0257	SET J	7777	0000	XXXX	XXXX	0	0	0260
0263	SET K	7777	7777	XXXX	XXXX	0	0	0264
0267	SET O	7777	7777	XXXX	XXXX	0	1	0270
0275	SFTZ 14 J	0000	0000	XXXX	XXXX	0	0	0276
0303	SFTZ 14 K	0000	0000	XXXX	XXXX	0	0	0304
0312	SFTZ 14 JK	0000	0000	XXXX	XXXX	0	0	0313
0321	ROTD 14 JK	0000	0000	XXXX	XXXX	0	0	0322
0330	ROTD 14 JK	0000	0000	XXXX	XXXX	0	0	0331

STOP AT	INSTRUCTION TESTED	REGISTERS SHOULD BE : JR	KR	RR	SR	FL	OV	PR
0337	ROTD 14 J	0000	0000	XXXX	XXXX	0	0	0340
0346	ROTD 14 K	0000	0000	XXXX	XXXX	0	0	0347
0353	INC J	0001	0000	XXXX	XXXX	0	0	0354
0356	INC J	0001	0000	XXXX	XXXX	0	0	0357
0362	SFTZ 01 J	0002	0000	XXXX	XXXX	0	0	0363
0365	SFTZ 01 J	0002	0000	XXXX	XXXX	0	0	0366
0371	SFTZ 01 J	0004	0000	XXXX	XXXX	0	0	0372
0374	SFTZ 01 J	0004	0000	XXXX	XXXX	0	0	0375
0400	SFTZ 01 J	0010	0000	XXXX	XXXX	0	0	0401
0403	SFTZ 01 J	0010	0000	XXXX	XXXX	0	0	0404
0407	SFTZ 01 J	0020	0000	XXXX	XXXX	0	0	0410
0412	SFTZ 01 J	0020	0000	XXXX	XXXX	0	0	0413
0416	SFTZ 01 J	0040	0000	XXXX	XXXX	0	0	0417
0421	SFTZ 01 J	0040	0000	XXXX	XXXX	0	0	0422
0425	SFTZ 01 J	0100	0000	XXXX	XXXX	0	0	0426
0430	SFTZ 01 J	0100	0000	XXXX	XXXX	0	0	0431
0434	SFTZ 01 J	0200	0000	XXXX	XXXX	0	0	0435
0437	SFTZ 01 J	0200	0000	XXXX	XXXX	0	0	0440
0443	SFTZ 01 J	0400	0000	XXXX	XXXX	0	0	0444
0446	SFTZ 01 J	0400	0000	XXXX	XXXX	0	0	0447
0452	SFTZ 01 J	1000	0000	XXXX	XXXX	0	0	0453
0455	SFTZ 01 J	1000	0000	XXXX	XXXX	0	0	0456
0461	SFTZ 01 J	2000	0000	XXXX	XXXX	0	0	0462
0464	SFTZ 01 J	2000	0000	XXXX	XXXX	0	0	0465
0470	SFTZ 01 J	4000	0000	XXXX	XXXX	0	0	0471
0473	SFTZ 01 J	4000	0000	XXXX	XXXX	0	0	0474
0477	SFTZ 01 J	0000	0000	XXXX	XXXX	0	0	0500
0502	SFTZ 01 J	0000	0000	XXXX	XXXX	0	0	0503
0504	SFTZ 01 J	0000	0000	XXXX	XXXX	0	0	0505
0511	INC K	0000	0001	XXXX	XXXX	0	0	0512
0514	INC K	0000	0001	XXXX	XXXX	0	0	0515
0520	SFTZ 01 K	0000	0002	XXXX	XXXX	0	0	0521
0523	SFTZ 01 K	0000	0002	XXXX	XXXX	0	0	0524
0527	SFTZ 01 K	0000	0004	XXXX	XXXX	0	0	0530
0532	SFTZ 01 K	0000	0004	XXXX	XXXX	0	0	0533
0536	SFTZ 01 K	0000	0010	XXXX	XXXX	0	0	0537
0541	SFTZ 01 K	0000	0010	XXXX	XXXX	0	0	0542
0545	SFTZ 01 K	0000	0020	XXXX	XXXX	0	0	0546
0550	SFTZ 01 K	0000	0020	XXXX	XXXX	0	0	0551
0554	SFTZ 01 K	0000	0040	XXXX	XXXX	0	0	0555
0557	SFTZ 01 K	0000	0040	XXXX	XXXX	0	0	0560

STOP AT	INSTRUCTION TESTED	REGISTERS SHOULD BE : JR	KR	RR	SR	FL	OV	PR
0563	SFTZ 01 K	0000	0100	XXXX	XXXX	0	0	0564
0566	SFTZ 01 K	0000	0100	XXXX	XXXX	0	0	0567
0572	SFTZ 01 K	0000	0200	XXXX	XXXX	0	0	0573
0575	SFTZ 01 K	0000	0200	XXXX	XXXX	0	0	0576
0601	SFTZ 01 K	0000	0400	XXXX	XXXX	0	0	0602
0604	SFTZ 01 K	0000	0400	XXXX	XXXX	0	0	0605
0610	SFTZ 01 K	0000	1000	XXXX	XXXX	0	0	0611
0613	SFTZ 01 K	0000	1000	XXXX	XXXX	0	0	0614
0617	SFTZ 01 K	0000	2000	XXXX	XXXX	0	0	0620
0622	SFTZ 01 K	0000	2000	XXXX	XXXX	0	0	0623
0626	SFTZ 01 K	0000	4000	XXXX	XXXX	0	0	0627
0631	SFTZ 01 K	0000	4000	XXXX	XXXX	0	0	0632
0635	SFTZ 01 K	0000	0000	XXXX	XXXX	0	0	0636
0640	SFTZ 01 K	0000	0000	XXXX	XXXX	0	0	0641
0642	SFTZ 01 K	0000	0000	XXXX	XXXX	0	0	0643
0644	SFTZ 01 K	0000	0000	XXXX	XXXX	0	0	0645
0652	NEG J	0000	0000	XXXX	XXXX	0	0	0653
0660	NEG K	0000	0000	XXXX	XXXX	0	0	0661
0667	LRFJ LJFR	0000	0000	0000	XXXX	0	0	0670
0700	LRFJ LJFR	0000	0000	7777	XXXX	0	0	0701
0707	LSFK LKFS	0000	0000	7777	0000	0	0	0710
0720	LSFK LKFS	0000	0000	7777	7777	0	0	0721
0726	EXJR	0000	0000	7777	7777	0	0	0727
0732	EXJR	0000	0000	0000	7777	0	0	0733
0737	EXKS	0000	0000	0000	7777	0	0	0740
0743	EXKS	0000	0000	0000	0000	0	0	0744
0752	EXJR EXKS	0000	0000	7777	7777	0	0	0753
0756	EXJR EXKS	0000	0000	0000	0000	0	0	0757
0764	LKFJ	0000	0000	0000	0000	0	0	0765
0771	LKFJ	0000	0000	0000	0000	0	0	0772
1017	SFTZ 02 JK	2525	2525	2525	2525	0	0	1020
1026	AJK J	0000	2525	2525	2525	0	0	1027
1036	AJK K	2525	0000	2525	2525	0	0	1037
1045	SJK J	0000	2525	2525	2525	0	0	1046
1052	SJK K	2525	0000	2525	2525	0	0	1053
1061	AND J	0000	2525	2525	2525	0	0	1062
1070	AND K	2525	0000	2525	2525	0	0	1071
1077	ADR J	0000	2525	2525	2525	0	0	1100
1106	ADR K	2525	0000	2525	2525	0	0	1107
1113	SBR J	0000	2525	2525	2525	0	0	1114
1120	SBR K	2525	0000	2525	2525	0	0	1121
1127	ADS J	0000	2525	2525	2525	0	0	1130
1136	ADS K	2525	0000	2525	2525	0	0	1137
1143	SBS J	0000	2525	2525	2525	0	0	1144
1150	SBS K	2525	0000	2525	2525	0	0	1151

STOP AT	INSTRUCTION TESTED		REGISTERS SHOULD BE : JR	KR	RR	SR	FL	OV	PR
1155	NAJK	J	5253	2525	2525	2525	0	1	1156
1161	NAJK	J	0000	2525	2525	2525	0	0	1162
1166	NAJK	K	2525	5253	2525	2525	0	1	1167
1172	NAJK	K	2525	0000	2525	2525	0	0	1173
1177	NSJK	J	0000	2525	2525	2525	0	0	1200
1204	NSJK	K	2525	0000	2525	2525	0	0	1205
1211	NADR	J	5253	2525	2525	2525	0	1	1212
1216	NADR	J	0000	2525	2525	2525	0	0	1217
1224	NADR	K	2525	5253	2525	2525	0	1	1225
1231	NADR	K	2525	0000	2525	2525	0	0	1232
1237	NSBR	J	0000	2525	2525	2525	0	0	1240
1245	NSBR	K	2525	0000	2525	2525	0	0	1246
1253	NADS	J	5253	2525	2525	2525	0	1	1254
1257	NADS	J	0000	2525	2525	2525	0	0	1260
1265	NADS	K	2525	5253	2525	2525	0	1	1266
1271	NADS	K	2525	0000	2525	2525	0	0	1272
1277	NSBS	J	0000	2525	2525	2525	0	0	1300
1305	NSBS	K	2525	0000	2525	2525	0	0	1306
1312	LRFJ		0000	0000	0000	0000	0	0	1313
1315	LSFK		0000	0000	0000	0000	0	0	1316
1321	LJFR		0000	0000	0000	0000	0	0	1322
1323	LKFS		0000	0000	0000	0000	0	0	1324
1333	LRFJ	LSFK	0000	0000	7777	7777	0	0	1334
1337	LRFJ	LSFK	0000	0000	7777	7777	0	0	1340
1344	LJFR	LKFS	0000	7777	7777	7777	0	0	1345
1347	LJFR	LKFS	0000	0000	7777	7777	0	0	1350
1355	LJST		0XXX	0000	7777	7777	0	0	1356
1360	LJST		0XXX	0000	7777	7777	0	0	1361
1365	LJST		2XXX	0000	7777	7777	0	1	1366
1370	LJST		4XXX	0000	7777	7777	0	1	1371
1375	LJST		4XXX	0000	7777	7777	1	0	1376
1400	LJST		0XXX	0000	7777	7777	1	0	1401
1405	LJST		6XXX	0000	7777	7777	1	1	1406
1410	LJST		4XXX	0000	7777	7777	1	1	1411
1416	RFOV		7777	0000	7777	7777	1	1	1417
1420	RFOV		7777	0000	7777	7777	1	1	1421
1427	RFOV		4000	0000	7777	7777	1	0	1430
1431	RFOV		4000	0000	7777	7777	1	0	1432
1440	RFOV		2000	0000	7777	7777	0	1	1441
1442	RFOV		2000	0000	7777	7777	0	1	1443
1446-65	JMP	.+21	0000	0000	7777	7777	0	0	1466
1467	JMP		0000	0000	7777	7777	0	0	1470

STOP AT	INSTRUCTION TESTED		REGISTERS SHOULD BE : JR	KR	RR	SR	FL	OV	PR
1471	JMP		0000	0000	7777	7777	0	0	1472
1477	LDJ		0000	0001	7777	7777	0	0	1500
1504	LDJ		0000	0002	7777	7777	0	0	1505
1511	LDJ		0000	0004	7777	7777	0	0	1512
1516	LDJ		0000	0010	7777	7777	0	0	1517
1523	LDJ		0000	0020	7777	7777	0	0	1524
1530	LDJ		0000	0040	7777	7777	0	0	1531
1535	LDJ		0000	0100	7777	7777	0	0	1536
1542	LDJ		0000	0200	7777	7777	0	0	1543
1547	LDJ		0000	0400	7777	7777	0	0	1550
1554	LDJ		0000	1000	7777	7777	0	0	1555
1561	LDJ		0000	2000	7777	7777	0	0	1562
1566	LDJ		0000	4000	7777	7777	0	0	1567
1570	JMP	.+16	0000	4000	7777	7777	0	0	1605
1612	LDJ		0000	0001	7777	7777	0	0	1613
1617	LDJ		0000	0002	7777	7777	0	0	1620
1624	LDJ		0000	0004	7777	7777	0	0	1625
1631	LDJ		0000	0010	7777	7777	0	0	1632
1636	LDJ		0000	0020	7777	7777	0	0	1637
1643	LDJ		0000	0040	7777	7777	0	0	1644
1650	LDJ		0000	0100	7777	7777	0	0	1651
1655	LDJ		0000	0200	7777	7777	0	0	1656
1662	LDJ		0000	0400	7777	7777	0	0	1663
1667	LDJ		0000	1000	7777	7777	0	0	1670
1674	LDJ		0000	2000	7777	7777	0	0	1675
1701	LDJ		0000	4000	7777	7777	0	0	1702
1706	LDJ		0000	0000	7777	7777	0	0	1707
1717	ADJ		0000	2525	7777	7777	0	0	1720
1723	ADJ		7777	0000	7777	7777	0	0	1724
1726	ADJ		7776	0000	7777	7777	0	1	1727
1733	ADJ		0000	0000	7777	7777	0	1	1734
1740	STJ		0000	0000	7777	7777	0	0	1741
1747	STJ		0000	0000	7777	7777	0	0	1750
1754	STJ		0000	0000	7777	7777	0	0	1755
1761	SBJ		0000	0000	7777	7777	0	0	1762
1764	DSZ		0000	0000	7777	7777	0	0	1765
1770	DSZ		0000	0000	7777	7777	0	0	1771
1772	ISZ		0000	0000	7777	7777	0	0	1773
1775	ISZ		0000	0000	7777	7777	0	0	1776
1777	DSZ		0000	0000	7777	7777	0	0	2000
2010	LDJ		0000	0000	7777	7777	0	0	2011

STOP AT	INSTRUCTION TESTED	REGISTERS SHOULD BE : JR	KR	RR	SR	FL	OV	PR
2021	ADJ	0000	2525	7777	7777	0	0	2022
2025	ADJ	7777	0000	7777	7777	0	0	2026
2030	ADJ	7776	0000	7777	7777	0	1	2031
2035	ADJ	0000	0000	7777	7777	0	1	2036
2042	STJ	0000	0000	7777	7777	0	0	2043
2051	STJ	0000	0000	7777	7777	0	0	2052
2056	STJ	0000	0000	7777	7777	0	0	2057
2063	SBJ	0000	0000	7777	7777	0	0	2064
2066	DSZ	0000	0000	7777	7777	0	0	2067
2072	DSZ	0000	0000	7777	7777	0	0	2073
2074	ISZ	0000	0000	7777	7777	0	0	2075
2077	ISZ	0000	0000	7777	7777	0	0	2100
2101	DSZ	0000	0000	7777	7777	0	0	2102
2107	STJ FIRST	0000	0000	7777	7777	0	0	2110
2112	STJ FIRST	0000	0000	7777	7777	0	0	2113
2117	STJ FIRST	0000	0000	7777	7777	0	0	2120
2123	STJ FIRST	0000	0000	7777	7777	0	0	2124
2132	STJ LAST	0000	0000	7777	7777	0	0	2133
2136	STJ LAST	0000	0000	7777	7777	0	0	2137
2140	STJ LAST	0000	0000	7777	7777	0	0	2141
2146	ADJ LAST	0000	0000	7777	7777	0	1	2147
2152	ADJ LAST	0000	0000	7777	7777	0	1	2153
2164	ADJ FIRST	0000	0000	7777	7777	0	1	2165
2175	LDJ@ LAST	0000	0000	7777	7777	0	0	2176
2201	FIRST INC	0000	0000	7777	7777	0	0	2202
2213	LDJ@ LAST	0000	0000	7777	7777	0	0	2214
2216	FIRST INC	0000	0000	7777	7777	0	0	2217
2226	LDJ@	0000	0000	7777	7777	0	0	2227
2234	ADJ@	0000	0000	7777	7777	0	0	2235
2242	ADJ@	0000	0000	7777	7777	0	0	2243
2251	ADJ@	0000	0000	7777	7777	0	1	2252
2255	ADJ@	7777	0000	7777	7777	0	0	2256
2261	ADJ@	0000	0000	7777	7777	0	1	2262
2267	SBJ@	0000	0000	7777	7777	0	0	2270
2274	STJ@	0000	0000	7777	7777	0	0	2275
2303	STJ@	0000	0000	7777	7777	0	0	2304
2310	STJ@	0000	0000	7777	7777	0	0	2311
2313	STJ@	0000	0000	7777	7777	0	0	2314
2333	LDJ@ LAST	0000	0000	7777	7777	0	0	2334
2336	FIRST INC	0000	0000	7777	7777	0	0	2337
2346	LDJ@ FIRST	0000	0000	7777	7777	0	0	2347

STOP AT	INSTRUCTION TESTED	REGISTERS SHOULD BE : JR	KR	RR	SR	FL	OV	PR
2351	LAST INC	0000	0000	7777	7777	0	0	2352
2361	LDJ@	0000	0000	7777	7777	0	0	2362
2367	ADJ@	0000	0000	7777	7777	0	0	2370
2375	ADJ@	0000	0000	7777	7777	0	1	2376
2404	ADJ@	0000	0000	7777	7777	0	1	2405
2410	ADJ@	7777	0000	7777	7777	0	1	2411
2422	SBJ@	0000	0000	7777	7777	0	0	2423
2432	STJ@	0000	0000	7777	7777	0	0	2433
2441	STJ@	0000	0000	7777	7777	0	0	2442
2446	STJ@	0000	0000	7777	7777	0	0	2447
2451	FIRST INC	0000	0000	7777	7777	0	0	2452
2454	LAST INC	0000	0000	7777	7777	0	0	2455
2457	SMJ	0000	0000	7777	7777	0	0	2460
2462	SMJ	0000	0000	7777	7777	0	0	2463
2465	SMJ	7777	0000	7777	7777	0	0	2466
2470	SMJ	7777	0000	7777	7777	0	0	2471
2477	SMJ	0000	0000	7777	7777	0	0	2500
2502	SMJ	0000	0000	7777	7777	0	0	2503
2505	SMJ	7777	0000	7777	7777	0	0	2506
2510	SMJ	7777	0000	7777	7777	0	0	2511
2513	SMJ@	0000	0000	7777	7777	0	0	2514
2516	SMJ@	0000	0000	7777	7777	0	0	2517
2521	SMJ@	7777	0000	7777	7777	0	0	2522
2524	SMJ@	7777	0000	7777	7777	0	0	2525
2533	SMJ@	0000	0000	7777	7777	0	0	2534
2536	SMJ@	0000	0000	7777	7777	0	0	2537
2541	SMJ@	7777	0000	7777	7777	0	0	2542
2544	SMJ@	7777	0000	7777	7777	0	0	2545
2550	DSZ@	0000	0000	7777	7777	0	0	2551
2554	DSZ@ (NO DEC)	0000	0000	7777	7777	0	0	2555
2556	ISZ@ (NO SKIP)	0000	0000	7777	7777	0	0	2557
2561	ISZ@ (NO INC)	0000	0000	7777	7777	0	0	2562
2564	ISZ@	0000	0000	7777	7777	0	0	2565
2572	ISZ@ (NO INC)	0000	0000	7777	7777	0	0	2573
2574	DSZ@ (NO SKIP)	0000	0000	7777	7777	0	0	2575
2577	DSZ@ (NO DEC)	0000	0000	7777	7777	0	0	2600
2606	DSZ@	0000	0000	7777	7777	0	0	2607
2612	DSZ@ (NO DEC)	0000	0000	7777	7777	0	0	2613
2614	ISZ@ (NO SKIP)	0000	0000	7777	7777	0	0	2615
2617	ISZ@ (NO INC)	0000	0000	7777	7777	0	0	2620
2622	ISZ@	0000	0000	7777	7777	0	0	2623

STOP AT	INSTRUCTION TESTED	REGISTERS SHOULD BE : JR	KR	RR	SR	FL	OV	PR
2630	ISZ@ (NO INC)	0000	0000	7777	7777	0	0	2631
2632	DSZ@ (NO SKIP)	0000	0000	7777	7777	0	0	2633
2635	DSZ@ (NO DEC)	0000	0000	7777	7777	0	0	2636
2643	ADDL 01	0000	0000	7777	7777	0	1	2644
2652	ADDL 00	0000	0000	7777	7777	0	0	2653
2656	SUBL 01	7777	0000	7777	7777	0	1	2657
2661	SUBL 01	0000	0000	7777	7777	0	1	2662
2666	SUBL 00	0000	0000	7777	7777	0	0	2667
2675	ADDL 77	0000	0000	7777	7777	0	1	2676
2704	SUBL 77	0000	0000	7777	7777	0	0	2705
2711	ANDL 00	0000	0000	7777	7777	0	0	2712
2721	ANDL 77	0000	0000	7777	7777	0	1	2722
2731	ANDL 01	0000	0000	7777	7777	0	1	2732
2736	ANDF 0000	0000	0000	7777	7777	0	0	2737
2745	ANDF 2525	0000	0000	7777	7777	0	0	2746
2754	ANDF 5252	0000	0000	7777	7777	0	0	2755
2762	ANDF 7777	0000	0000	7777	7777	0	0	2763
2777	JPS (FAILED)	7777	7777	7777	7777	0	1	3003
3000-1	JPS (FAILED)	7777	7777	7777	7777	0	1	3003
3005	JPS (JR)	0000	0000	7777	7777	0	0	3006
3007	JPS (KR)	0000	0000	7777	7777	0	0	3010
3011	JPS (OV)	0000	0000	7777	7777	0	0	3012
3017	JPS (PR)	0000	0000	7777	7777	0	0	3020
3024-5	JMP	0000	0000	7777	7777	0	0	3045
3031	JPS (JR)	0000	0000	7777	7777	0	0	3032
3033	JPS (KR)	0000	0000	7777	7777	0	0	3034
3035	JPS (OV)	0000	0000	7777	7777	0	0	3036
3042	JPS (PR)	0000	0000	7777	7777	0	0	3043
3044	JMP	0000	0000	7777	7777	0	0	3054
3051-3	JPS (FAILED)	7777	7777	7777	7777	0	1	3027
3062	JMP@ (FAILED)	7777	7777	7777	7777	1	1	3066
3070	JMP@ (JR)	0000	0000	7777	7777	1	0	3071
3072	JMP@ (KR)	0000	0000	7777	7777	1	0	3073
3074	JMP@ (OV)	0000	0000	7777	7777	1	0	3075
3076	JMP@ (FL)	0000	0000	7777	7777	1	0	3077
3104	JMP@ (FAILED)	7777	7777	7777	7777	1	1	3105
3107	JMP@ (JR)	0000	0000	7777	7777	1	0	3110
3111	JMP@ (KR)	0000	0000	7777	7777	1	0	3112
3113	JMP@ (OV)	0000	0000	7777	7777	1	0	3114
3115	JMP@ (FL)	0000	0000	7777	7777	1	0	3116
3122	JMP@ (FAILED)	0000	0000	7777	7777	0	0	3125

```
STOP AT TESTED                    REGISTERS SHOULD BE :
                                  JR    KR    RR    SR   FL OV   PR

3126     JMP@ (JR)                0000  0000  7777  7777  0  0  3127
3130     JMP@ (KR)                0000  0000  7777  7777  0  0  3131
3132     JMP@ (OV)                0000  0000  7777  7777  0  0  3133
3134     JMP@ (FL)                0000  0000  7777  7777  0  0  3135
3141     JMP@ (FAILED)            0000  0000  7777  7777  0  0  3142
3143     JMP@ (JR)                0000  0000  7777  7777  0  0  3144
3145     JMP@ (KR)                0000  0000  7777  7777  0  0  3146
3147     JMP@ (OV)                0000  0000  7777  7777  0  0  3150
3151     JMP@ (FL)                0000  0000  7777  7777  0  0  3152
3157-60  JPS@ (FAILED)            7777  7777  7777  7777  1  1  3166
3170     JPS@ (JR)                0000  0000  7777  7777  1  0  3171
3172     JPS@ (KR)                0000  0000  7777  7777  1  0  3173
3174     JPS@ (OV)                0000  0000  7777  7777  1  0  3175
3176     JPS@ (FL)                0000  0000  7777  7777  1  0  3177
3203     JPS@ (PR)                0000  0000  7777  7777  1  0  3204
3210-11  JPS@ (FAILED)            7777  7777  7777  7777  1  1  3213
3215     JPS@ (JR)                0000  0000  7777  7777  1  0  3216
3217     JPS@ (KR)                0000  0000  7777  7777  1  0  3220
3221     JPS@ (OV)                0000  0000  7777  7777  1  0  3222
3223     JPS@ (FL)                0000  0000  7777  7777  1  0  3224
3231     JPS@ (PR)                0000  0000  7777  7777  1  0  3232
3236-37  JPS@ (FAILED)            0000  0000  7777  7777  0  0  3245
3246     JPS@ (JR)                0000  0000  7777  7777  0  0  3247
3250     JPS@ (KR)                0000  0000  7777  7777  0  0  3251
3252     JPS@ (OV)                0000  0000  7777  7777  0  0  3253
3254     JPS@ (FL)                0000  0000  7777  7777  0  0  3255
3261-62  JPS@ (FAILED)            0000  0000  7777  7777  0  0  3264
3265     JPS@ (JR)                0000  0000  7777  7777  0  0  3266
3267     JPS@ (KR)                0000  0000  7777  7777  0  0  3270
3271     JPS@ (OV)                0000  0000  7777  7777  0  0  3272
3273     JPS@ (FL)                0000  0000  7777  7777  0  0  3274
3301     JPS@ (PR)                0000  0000  7777  7777  0  0  3302

3304     NO SWITCHES UP -SINGLE PASS CORRECT
3325-26  JMP@ RETEST      FAILED

END ND41-8001 STOP LIST
```

EXECUTE AND TWO-WORD INSTRUCTION TEST (ND41-8002)

I. INTRODUCTION

A. This program is designed to serve as a go-no go check of the Execute Instruction, all forms of Two-Word MRI's and combinations of Single and Two-Word MRI's with the Execute Instruction.

B. PROGRAM AREA

$4ØØØ_8$ through 7315_8.

C. STARTING ADDRESS

$4ØØØ_8$.

D. EQUIPMENT CONFIGURATION

Minimum requirements are a ND-812 Central Processor equipped with an ASR33 Teletype. An optional peripheral is a high speed reader.

II. PROGRAM DESCRIPTION

All forms of two-word MRI's are tested separately to verify that each step in the instruction is performed correctly. The second half of the program is the execute test that includes a stored execute test marker indicating the number of current tests. Execution of two-word operates, two single word MRI's and combinations of direct and indirect two-word instructions are tested.

The program stops on commission of an error. The address at which the program stopped and the status of the marker (location 5573_8) can be referred to the DIAGNOSTIC STOP LIST for possible cause of failure.

On completion of 4096 valid passes, the teletype prints "XCT - TWI OK".

III. OPERATOR OR USER CONTROL

Starting the program with a non-zero Switch Register causes multiple passes. A zero Switch Register allows only one pass.

This program can be chained to the Operate-Memory Reference Instruction Test (ND41-8001) by changing the contents of location 7276_8 (of this program) to $ØØ21_8$. A non-zero Switch Register will also cause multiple passes in the "chained" mode if ND41-8001 is in core and location $333Ø_8$ of ND41-8001 has been modified for this mode.

After the commission of an error, the stop address and marker status (location 5573_8) should be referred to the DIAGNOSTIC STOP LIST. To recover from an error condition, set Switch Register to stop address, depress LOAD ADDRESS, depress CONTINUE.

IV. OPERATION PROCEDURE

1. Load the Execute and Two-Word Instruction Test program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a detailed description of its use).

2. Set Switch Register to 4000_8.

3. Depress LOAD ADDRESS.

4. Set Switch Register to any value for multiple passes or to zero for single pass.

5. Depress START.

6. The test can be terminated by depressing STOP.

The following is a procedure for error analysis:

1. Place the SELECT REGISTER switch in the ADDRESS position and read the stop address from the SELECTED REGISTER lights.

2. Set Switch Register to 5573_8.

3. Depress NEXT WORD.

4. Refer stop addrsss and marker status the DIAGNOSTIC STOP LIST (Page 65).

5. To recover from an error condition, set Switch Register to stop address and depress CONTINUE.

V. ERROR DIAGNOSTICS

On commission of an error the program will stop. Refer to the DIAGNOSTIC STOP LIST (Page 65).

VI. COMMAND SUMMARY

None.

ND41-8002 DIAGNOSTIC STOP LIST 1/10/70 -DB
EXECUTE AND TWO-WORD INSTRUCTION TEST SA=4000

STOPPED ADDRESS	EXECUTE MARKER	INSTRUCTION TESTED	CAUSE OF STOP
4014	7777	TWLDJ	FAILED TO INCREMENT PROGRAM REGISTER
4012	7777	TWLDJ	EXTRA PROGRAM REGISTER INCREMENT
4014	7777	TWLDJ	FAILED TO LOAD J REGISTER
4017	7777	TWSTJ	FAILED TO INCREMENT PROGRAM REGISTER
4021	7777	TWSTJ	EXTRA PROGRAM REGISTER INCREMENT
4024	7777	TWSTJ	CHANGED CONTENTS OF J REGISTER
4030	7777	TWSTJ	FAILED TO STORE J REGISTER
4033	7777	TWLDJ	FAILED TO INCREMENT PROGRAM REGISTER
4035	7777	TWLDJ	EXTRA PROGRAM REGISTER INCREMENT
4040	7777	TWLDJ	FAILED TO LOAD J REGISTER
4043	7777	TWSTJ	FAILED TO INCREMENT PROGRAM REGISTER
4045	7777	TWSTJ	EXTRA PROGRAM REGISTER INCREMENT
4050	7777	TWSTJ	FAILED TO STORE J REGISTER
4053	7777	TWADJ	FAILED TO INCREMENT PROGRAM REGISTER
4055	7777	TWADJ	EXTRA PROGRAM REGISTER INCREMENT
4057	7777	TWADJ	CHANGED CONTENTS OF J REGISTER
4062	7777	TWSBJ	FAILED TO INCREMENT PROGRAM REGISTER
4064	7777	TWSBJ	EXTRA PROGRAM REGISTER INCREMENT
4067	7777	TWSBJ	FAILED TO SUBTRACT ZERO
4072	7777	TWLDJ	FAILED TO INCREMENT PROGRAM REGISTER
4074	7777	TWLDJ	EXTRA PROGRAM REGISTER INCREMENT
4076	7777	TWLDJ	FAILED TO LOAD J REGISTER
4102	7777	ANY ABOVE	CHANGED K REGISTER
4104	7777	ANY ABOVE	CHANGED OVERFLOW REGISTER
4106	7777	ANY ABOVE	CHANGED FLAG REGISTER
4112	7777	TWLDK	FAILED TO INCREMENT PROGRAM REGISTER
4114	7777	TWLDK	EXTRA PROGRAM REGISTER INCREMENT
4116	7777	TWLDK	CHANGED CONTENTS OF K REGISTER
4121	7777	TWSTK	FAILED TO INCREMENT PROGRAM REGISTER
4123	7777	TWSTK	EXTRA PROGRAM REGISTER INCREMENT
4126	7777	TWSTK	CHANGED CONTENTS OF K REGISTER
4131	7777	TWSTK	CHANGED J REGISTER
4135	7777	TWSTK	FAILED TO STORE K REGISTER
4141	7777	TWLDK	FAILED TO INCREMENT PROGRAM REGISTER
4143	7777	TWLDK	EXTRA PROGRAM REGISTER INCREMENT
4146	7777	TWLDK	FAILED TO LOAD K REGISTER
4151	7777	TWSTK	FAILED TO INCREMENT PROGRAM REGISTER
4153	7777	TWSTK	EXTRA PROGRAM REGISTER INCREMENT
4155	7777	TWSTK	CHANGED CONTENTS OF K REGISTER
4160	7777	TWSTK	CHANGED J REGISTER
4163	7777	TWSTK	FAILED TO STORE K REGISTER
4167	7777	TWADK	FAILED TO INCREMENT PROGRAM REGISTER
4171	7777	TWADK	EXTRA PROGRAM REGISTER INCREMENT

4173	7777	TWADK	CHANGED CONTENT OF K REGISTER
4176	7777	TWSBK	FAILED TO INCREMENT PROGRAM REGISTER
4200	7777	TWSBK	EXTRA PROGRAM REGISTER INCREMENT
4203	7777	TWSBK	CHANGED K REGISTER
4206	7777	TWLDK	FAILED TO INCREMENT PROGRAM REGISTER
4210	7777	TWLDK	EXTRA PROGRAM REGISTER INCREMENT
4212	7777	TWLDK	CHANGED K REGISTER
4215	7777	TWLDK	CHANGED J REGISTER
4217	7777	TWLDK	CHANGED O REGISTER
4221	7777	TWLDK	CHANGED FLAG REGISTER
4233	7777	TWDJ	FAILED TO LOAD J REGISTER
4243	7777	TWLDJ	FAILED TO LOAD J REGISTER
4256	7777	TWSTJ	FAILED TO STORE J REGISTER
4271	7777	TWSTJ	FAILED TO STORE J REGISTER
4302	7777	TWSTJ	CHANGED K REGISTER
4304	7777	TWSTJ	CHANGED FLAG REGISTER
4316	7777	TWADJ	FAILED TO ADD TO J REGISTER
4325	7777	TWADJ	FAILED TO ADD TO J REGISTER
4335	7777	TWSBJ	FAILED TO SUBTRACT FROM J REGISTER
4343	7777	TWSBJ	FAILED TO SUBTRACT FROM J REGISTER
4350	7777	TWSMJ	FAILED TO SKIP WHEN DIFFERENT
4354	7777	TWSMJ	SKIPPED WHEN SAME
4360	7777	TWSMJ	FAILED TO SKIP WHEN DIFFERENT
4364	7777	TWSMJ	SKIPPED WHEN SAME
4370	7777	TWSMJ	FAILED TO SKIP WHEN DIFFERENT
4374	7777	TWSMJ	FAILED TO SKIP WHEN DIFFERENT
4401	7777	TWSMJ	SKIPPED WHEN SAME
4406	7777	TWSMJ	SKIPPED WHEN SAME
4412	7777	TWSMJ	FAILED TO SKIP WHEN DIFFERENT
4415	7777	TWSMJ	FAILED TO SKIP WHEN DIFFERENT
4420	7777	TWSMJ	FAILED TO SKIP WHEN DIFFERENT
4423	7777	TWSMJ	FAILED TO SKIP WHEN DIFFERENT
4426	7777	TWSMJ	FAILED TO SKIP WHEN DIFFERENT
4431	7777	TWSMJ	FAILED TO SKIP WHEN DIFFERENT
4433	7777	TWSMJ	CHANGED K REGISTER
4435	7777	TWSMJ	CHANGED O REGISTER
4456	7777	TWSMK	FAILED TO SKIP WHEN DIFFERENT
4462	7777	TWSMK	SKIPPED WHEN SAME
4466	7777	TWSMK	FAILED TO SKIP WHEN DIFFERENT
4472	7777	TWSMK	SKIPPED WHEN SAME

4500	7777	TWLDK	FAILED TO LOAD K REGISTER
4503	7777	TWSMK	FAILED TO SKIP WHEN DIFFERENT
4510	7777	TWSMK	FAILED TO SKIP WHEN DIFFERENT
4515	7777	TWSMK	SKIPPED WHEN SAME
4523	7777	TWSMK	SKIPPED WHEN SAME
4527	7777	TWSMK	FAILED TO SKIP WHEN DIFFERENT
4532	7777	TWSMK	FAILED TO SKIP WHEN DIFFERENT
4535	7777	TWSMK	FAILED TO SKIP WHEN DIFFERENT
4540	7777	TWSMK	FAILED TO SKIP WHEN DIFFERENT
4543	7777	TWSMK	FAILED TO SKIP WHEN DIFFERENT
4546	7777	TWSMK	FAILED TO SKIP WHEN DIFFERENT
4555	7777	TWDSZ	SKIPPED DECREMENTING ZERO
4561	7777	TWDSZ	FAILED TO DECREMENT
4564	7777	TWISZ	FAILED TO SKIP WHEN ZERO
4567	7777	TWISZ	FAILED TO INCREMENT
4573	7777	TWISZ	SKIPPED INCREMENTING ZERO
4600	7777	TWISZ	FAILED TO INCREMENT
4603	7777	TWDSZ	FAILED TO SKIP WHEN ZERO
4606	7777	TWDSZ	FAILED TO DECREMENT
4617-22	7777	TWJMP	FAILED TO MODIFY PROGRAM REGISTER
4626	7777	TWJMP	CHANGED J REGISTER
4631	7777	TWJMP	CHANGED K REGISTER
4634	7777	TWJMP	CHANGED O REGISTER
4637	7777	TWJMP	CHANGED FLAG REGISTER
4646-50	7777	TWJPS	FAILED TO MODIFY PROGRAM REGISTER
4655	7777	TWJPS	CHANGED J REGISTER
4660	7777	TWJPS	CHANGED K REGISTER
4663	7777	TWJPS	CHANGED O REGISTER
4666	7777	TWJPS	CHANGED FLAG REGISTER
4673	7777	TWJPS	FAILED TO STORE PROGRAM REGISTER
4702	7777	TWLDJ@	EXTRA PROGRAM REGISTER INCREMENT
4704	7777	TWLDJ@	FAILED TO LOAD J REGISTER
4711	7777	TWLDJ@	EXTRA PROGRAM REGISTER INCREMENT
4714	7777	TWLDJ@	FAILED TO LOAD J REGISTER
4722	7777	TWLDJ@	EXTRA PROGRAM REGISTER INCREMENT
4725	7777	TWLDJ@	FAILED TO LOAD J REGISTER
4730	7777	TWLDJ@	CHANGED K REGISTER
4732	7777	TWLDJ@	CHANGED O REGISTER
4734	7777	TWLDJ@	CHANGED FLAG REGISTER
4745	7777	TWSTJ@	EXTRA PROGRAM REGISTER INCREMENT
4751	7777	TWSTJ@	FAILED TO STORE J REGISTER
4756	7777	TWSTJ@	EXTRA PROGRAM REGISTER INCREMENT
4761	7777	TWSTJ@	FAILED TO STORE J REGISTER

4766	7777	TWSTJ@	EXTRA PROGRAM REGISTER INCREMENT
4772	7777	TWSTJ@	FAILED TO STORE J REGISTER
4777	7777	TWSTJ@	EXTRA PROGRAM REGISTER INCREMENT
5003	7777	TWSTJ@	FAILED TO STORE J REGISTER
5010	7777	TWSTJ@	CHANGED K REGISTER
5012	7777	TWSTJ@	CHANGED O REGISTER
5014	7777	TWSTJ@	CHANGED FLAG REGISTER
5040	7777	TWADJ@	EXTRA PROGRAM REGISTER INCREMENT
5043	7777	TWADJ@	FAILED TO ADD ONE
5050	7777	TWADJ@	EXTRA PROGRAM REGISTER INCREMENT
5054	7777	TWADJ@	FAILED TO ADD TO J REGISTER
5057	7777	TWADJ@	CHANGED K REGISTER
5061	7777	TWADJ@	CHANGED FLAG REGISTER
5070	7777	TWADJ@	EXTRA PROGRAM REGISTER INCREMENT
5074	7777	TWADJ@	FAILED TO ADD TO J REGISTER
5102	7777	TWSBJ@	EXTRA PROGRAM REGISTER INCREMENT
5106	7777	TWSBJ@	FAILED TO SUBTRACT FROM J REGISTER
5113	7777	TWSBJ@	EXTRA PROGRAM REGISTER INCREMENT
5116	7777	TWSBJ@	FAILED TO SUBTRACT FROM J REGISTER
5121	7777	TWSBJ@	CHANGED K REGISTER
5123	7777	TWSBJ@	CHANGED FLAG REGISTER
5132	7777	TWLDK@	EXTRA PROGRAM REGISTER INCREMENT
5134	7777	TWLDK@	FAILED TO LOAD K REGISTER
5141	7777	TWLDK@	EXTRA PROGRAM REGISTER INCREMENT
5144	7777	TWLDK@	FAILED TO LOAD K REGISTER
5152	7777	TWLDK@	EXTRA PROGRAM REGISTER INCREMENT
5155	7777	TWLDK@	CHANGED J REGISTER
5161	7777	TWLDK@	FAILED TO LOAD K REGISTER
5163	7777	TWLDK@	CHANGED O REGISTER
5165	7777	TWLDK@	CHANGED FLAG REGISTER
5176	7777	TWSTK@	EXTRA PROGRAM REGISTER INCREMENT
5201	7777	TWSTK@	CHANGED J REGISTER
5205	7777	TWSTK@	FAILED TO STORE K REGISTER
5213	7777	TWSTK@	EXTRA PROGRAM REGISTER INCREMENT
5217	7777	TWSTK@	FAILED TO STORE K REGISTER
5225	7777	TWSTK@	EXTRA PROGRAM REGISTER INCREMENT
5231	7777	TWSTK@	FAILED TO STORE K REGISTER
5235	7777	TWSTK@	CHANGED O REGISTER
5237	7777	TWSTK@	CHANGED FLAG REGISTER
5263	7777	TWADK@	EXTRA PROGRAM REGISTER INCREMENT
5266	7777	TWADK@	FAILED TO ADD TO K REGISTER
5273	7777	TWADK@	EXTRA PROGRAM REGISTER INCREMENT
5276	7777	TWADK@	CHANGED J REGISTER
5303	7777	TWADK@	FAILED TO ADD TO K REGISTER
5305	7777	TWADK@	CHANGED FLAG REGISTER
5316	7777	TWADK@	EXTRA PROGRAM REGISTER INCREMENT
5322	7777	TWADK@	FAILED TO ADD TO K REGISTER
5330	7777	TWSBK@	EXTRA PROGRAM REGISTER INCREMENT
5334	7777	TWSBK@	FAILED TO SUBTRACT FROM K REGISTER

5342	7777	TWSBK@	EXTRA PROGRAM REGISTER INCREMENT
5345	7777	TWSBK@	FAILED TO SUBTRACT FROM K REGISTER
5347	7777	TWSBK@	CHANGED FLAG REGISTER
5360	7777	TWDSZ@	DECREMENTING ZERO SKIPPED
5363	7777	TWDSZ@	CHANGED J REGISTER
5366	7777	TWDSZ@	CHANGED K REGISTER
5370	7777	TWDSZ@	CHANGED O REGISTER
5372	7777	TWDSZ@	CHANGED FLAG REGISTER
5376	7777	TWDSZ@	FAILED TO DECREMENT
5405	7777	TWISZ@	FAILED TO SKIP ON ZERØ
5410	7777	TWISZ@	CHANGED J REGISTER
5413	7777	TWISZ@	CHANGED K REGISTER
5415	7777	TWISZ@	CHANGED O REGISTER
5417	7777	TWISZ@	CHANGED FLAG REGISTER
5422	7777	TWISZ@	FAILED TO INCREMENT
5431	7777	TWISZ@	INCREMENTING ZERO SKIPPED
5434	7777	TWISZ@	CHANGED J REGISTER
5437	7777	TWISZ@	CHANGED K REGISTER
5441	7777	TWISZ@	CHANGED O REGISTER
5443	7777	TWISZ@	CHANGED FLAG REGISTER
5456	7777	TWDSZ@	FAILED TO SKIP ON ZERO
5461	7777	TWDSZ@	CHANGED J REGISTER
5464	7777	TWDSZ@	CHANGED K REGISTER
5466	7777	TWDSZ@	CHANGED O REGISTER
5470	7777	TWDSZ@	CHANGED FLAG REGISTER
5473	7777	TWDSZ@	FAILED TO DECREMENT
5501-02	7777	TWJMP@	FAILED TO MODIFY PROGRAM REGISTER
5504-05	7777	TWJMP@	ILLEGAL TRANSFER OF CONTROL
5513	7777	TWJMP@	CHANGED J REGISTER
5516	7777	TWJMP@	CHANGED K REGISTER
5520	7777	TWJMP@	CHANGED O REGISTER
5522	7777	TWJMP@	CHANGED FLAG REGISTER
5530-31	7777	TWJPS@	FAILED TO MODIFY PROGRAM REGISTER
5534-35	7777	TWJPS@	ILLEGAL TRANSFER OF CONTROL
5544	7777	TWJPS@	CHANGED J REGISTER
5547	7777	TWJPS@	CHANGED K REGISTER
5551	7777	TWJPS@	CHANGED O REGISTER
5553	7777	TWJPS@	CHANGED FLAG REGISTER
5560	7777	TWJPS@	FAILED TO STORE PROGRAM REGISTER

EXECUTE	TEST	EXECUTE MARKER = 5573	
5562	7777	XCT	ILLEGAL TRANSFER OF CONTROL
5564-67	7777	XCT	ILLEGAL TRANSFER OF CONTROL
5571-72	7777	XCT	ILLEGAL TRANSFER OF CONTROL
5576	0000	MARKER	CHANGED OR NOT RESET START AT 4000
5601	0001	MARKER TEST	CHANGED OR NOT RESET START AT 4000
5607	0001	XCT SIZ J	SKIPPED ON NON-ZERO J REGISTER
5612	0001	XCT SIZ J	CHANGED J REGISTER
5616	0001	MARKER	INCORRECT MARKER = TEST IN ERROR
5621	0002	MARKER	INCORRECT MARKER = TEST IN ERROR
5625	0002	XCT SIZ J	FAILED TO SKIP ON ZERO J REGISTER
5627	0002	XCT SIZ J	CHANGED J REGISTER
5633	0002	MARKER	INCORRECT MARKER = TEST IN ERROR
5640	0003	XCT ISZ	SEQUENCE ERROR
5643	0003	XCT ISZ	CHANGED J REGISTER
5647	0003	MARKER	INCORRECT MARKER = TEST IN ERROR
5652	0004	MARKER	SEQUENCE ERROR
5655	0005	XCT XCT ISZ	FAILED OR MARKER INCORRECT
5661	0005	MARKER	INCORRECT MARKER = TEST IN ERROR
5665	0005	XCT LDJ	SKIPPED
5670	0005	XCT LDJ	FAILED TO LOAD J REGISTER
5673	0006	XCT XCT ISZ	FAILED OR MARKER INCORRECT
5700	0006	MARKER	SEQUENCE ERROR
5703	0007	XCT XCT XCT ISZ	FAILED OR MARKER INCORRECT
5707	0007	XCT XCT LDJ	FAILED OR MARKER INCORRECT
5714	0010	XCT XCT XCT ISZ	FAILED OR MARKER INCORRECT
5717	0010	XCT XCT SIZ J	SKIPPED ON NON-ZERO J REGISTER
5722	0010	XCT XCT SIZ J	FAILED TO SKIP ON ZERO J REGISTER
5726	0010	XCT XCT XCT LDJ	FAILED OR MARKER INCORRECT
5731	0010	XCT	CHANGED K REGISTER
5733	0010	XCT	CHANGED O REGISTER
5735	0010	XCT	CHANGED FLAG REGISTER
5740	0011	XCT XCT XCT ISZ	FAILED OR SEQUENCE INCORRECT
5744	0011	MARKER	SEQUENCE INCORRECT
5752	0011	XCT@ SIZ J	SKIPPED J NOT ZERO
5755	0011	XCT@ SIZ J	DIDN'T SKIP J = 0
5761	0011	MARKER	SEQUENCE INCORRECT
5764	0011	MARKER	SEQUENCE INCORRECT
5770	0012	XCT@ LDJ	SKIPPED OR MARKER INCORRECT
5773	0012	MARKER	SEQUENCE OR XCT@ LDJ INCORRECT
5777	0013	MARKER	SEQUENCE OR XCT@ ISZ INCORRECT
6003	0013	MARKER	INCORRECT -CHECK MARKER
6006	0013	XCT@	CHANGED K REGISTER

6010	0013	XCT@	CHANGED 0 REGISTER
6012	0013	XCT@	CHANGED FLAG REGISTER
6015	0014	MARKER	OUT OF SEQUENCE
6021	0014	MARKER	OUT OF SEQUENCE
6026-30	0014	XCT@ JMP	FAILED TO TRANSFER CONTROL
6032	0014	XCT@ JMP	ILLEGAL TRANSFER OF CONTROL
6034	0014	XCT@ JMP	FAILED
6043	0014	XCT@ JMP	CHANGED K REGISTER
6046	0014	XCT@ JMP	CHANGED J REGISTER
6050	0014	XCT@ JMP	CHANGED 0 REGISTER
6052	0014	XCT@ JMP	CHANGED FLAG REGISTER
6057	0014	XCT@ JMP	SEQUENCE INCORRECT CHECK MARKER
6070	0015	XCT@ SIZ J	SKIPPED -J NONZERO
6073	0015	XCT@ SIZ J	DIDN'T SKIP -J = 0
6077	0015	MARKER	SEQUENCE INCORRECT
6102	0016	XCT(5) ISZ	SKIPPED -SEQUENCE INCORRECT
6106	0016	XCT@ LDJ	SKIPPED
6111	0016	XCT@ LDJ	FAILED
6115	0017	XCT@ ISZ	SKIPPED SEQUENCE INCORRECT
6121	0017	XCT(5) LDJ	FAILED
6124	0017	XCT@ ISZ	CHANGED K REGISTER
6126	0017	XCT@ ISZ	CHANGED 0 REGISTER
6130	0017	XCT@ ISZ	CHANGED FLAG REGISTER
6136	0020	XCT(6) ISZ	SKIPPED -SEQUENCE INCORRECT
6142	0020	XCT LDJ@	SKIPPED
6145	0020	MARKER	OUT OF SEQUENCE
6151	0021	XCT ISZ@	FAILED OR SEQUENCE INCORRECT
6155	0021	XCT(6) LDJ	SKIPPED
6160	0022	XCT(6) ISZ	XCT ISZ SKIPPED OR SEQUENCE..
6164	0022	XCT LDJ@	SKIPPED
6167	0022	XCT LDJ@	FAILED TO LOAD
6173	0022	MARKER	SEQUENCE INCORRECT
6176	0023	XCT(7) ISZ	SKIPPED OR SEQUENCE INCORRECT
6201	0023	XCT ISZ	CHANGED K REGISTER
6203	0023	XCT ISZ	CHANGED 0 REGISTER
6205	0023	XCT ISZ	CHANGED FLAG REGISTER
6212-3	0023	XCT JMP@	FAILED
6214	0023	XCT JMP@	ILLEGAL TRANSFER OF CONTROL
6216-20	0023	XCT JMP@	ILLEGAL TRANSFER OF CONTROL
6222	0023	XCT JMP@	ILLEGAL TRANSFER OF CONTROL
6225	0023	XCT JMP@	JUMP DIRECT FAILED
6226	0023	XCT JMP@	ILLEGAL TRANSFER OF CONTROL
6230-1	0023	XCT JMP@	ILLEGAL TRANSFER OF CONTROL
6233-4	0023	XCT JMP@	ILLEGAL TRANSFER OF CONTROL

6236	0023	XCT JMP@	ILLEGAL TRANSFER OF CONTROL
6242	0023	XCT JMP@	CHANGED K REGISTER
6245	0023	XCT JMP@	CHANGED J REGISTER
6247	0023	XCT JMP@	CHANGED O REGISTER
6251	0023	XCT JMP@	CHANGED FLAG REGISTER
6255	0023	MARKER	SEQUENCE INCORRECT
6260	0024	XCT ISZ	SEQUENCE INCORRECT
6267	0024	XCT LDJ@	FAILED TO LOAD
6272	0025	XCT ISZ@	FAILED OR SEQUENCE INCORRECT
6276	0025	XCT ISZ@	MARKER INCORRECT
6301	0026	XCT XCT ISZ	SEQUENCE INCORRECT
6304	0026	XCT ISZ(@)	CHANGED K REGISTER
6306	0026	XCT ISZ(@)	CHANGED O REGISTER
6310	0026	XCT ISZ(@)	CHANGED FLAG REGISTER
6316	0026	XCT@ LDJ@	SKIPPED ?
6321	0026	XCT@ LDJ@	FAILED TO LOAD
6325	0027	XCT@ ISZ@	FAILED OR SEQUENCE INCORRECT
6331	0027	MARKER	SEQUENCE ?
6334	0030	XCT ISZ	SEQUENCE INCORRECT
6337	0030	XCT@	CHANGED K REGISTER
6341	0030	XCT@	CHANGED O REGISTER
6343	0030	XCT@	CHANGED FLAG REGISTER
6352	0030	XCT@ JMP@	NO TRANSFER OF CONTROL
6352	0030	XCT@ JMP@	ILLEGAL TRANSFER OF CONTROL
6354	0030	XCT@ JMP@	ILLEGAL TRANSFER OF CONTROL
6356	0030	XCT@ JMP@	ILLEGAL TRANSFER OF CONTROL
6361-2	0030	XCT@ JMP@	ILLEGAL TRANSFER OF CONTROL
6364	0030	XCT@ JMP@	ILLEGAL TRANSFER OF CONTROL
6366-7	0030	XCT@ JMP@	ILLEGAL TRANSFER OF CONTROL
6371-2	0030	XCT@ JMP@	ILLEGAL TRANSFER OF CONTROL
6374-5	0030	XCT@ JMP@	ILLEGAL TRANSFER OF CONTROL
6401	0030	XCT@ JMP@	CHANGED K REGISTER
6404	0030	XCT@ JMP@	CHANGED J REGISTER
6406	0030	XCT@ JMP@	CHANGED O REGISTER
6410	0030	XCT@ JMP@	CHANGED FLAG REGISTER
6414	0030	XCT@ JMP@	MARKER INCORRECT
6420	0031	XCT ISZ	SEQUENCE INCORRECT
6427-30	0031	XCT JPS	NO TRANSFER OF CONTROL
6432-3	0031	XCT JPS	ILLEGAL TRANSFER OF CONTROL
6435	0031	XCT JPS	ILLEGAL TRANSFER OF CONTROL
6442	0031	XCT JPS	CHANGED K REGISTER
6445	0031	XCT JPS	CHANGED J REGISTER
6447	0031	XCT JPS	CHANGED O REGISTER
6451	0031	XCT JPS	CHANGED FLAG REGISTER

6455	0031	XCT JPS	DIDN'T STORE PR
6461	0031	XCT JPS	SEQUENCE INCORRECT
6470-1	0032	XCT@ JPS	NO TRANSFER OF CONTROL
6474	0032	XCT@ JPS	ILLEGAL TRANSFER OF CONTROL
6476-7	0032	XCT@ JPS	ILLEGAL TRANSFER OF CONTROL
6504	0032	XCT@ JPS	CHANGED J REGISTER
6510	0032	XCT@ JPS	SEQUENCE INCORRECT
6515	0033	XCT@ JPS	FAILED TO STORE PR
6520	0033	XCT@ JPS	CHANGED K REGISTER
6522	0033	XCT@ JPS	CHANGED O REGISTER
6524	0033	XCT@ JPS	CHANGED FLAG REGISTER
6531-2	0033	XCT@ JPS@	NO TRANSFER OF CONTROL
6535	0033	XCT@ JPS@	ILLEGAL TRANSFER OF CONTROL
6537-40	0033	XCT@ JPS@	ILLEGAL TRANSFER OF CONTROL
6542	0033	XCT@ JPS@	ILLEGAL TRANSFER OF CONTROL
6547	0033	XCT@ JPS@	CHANGED J REGISTER
6553	0033	XCT@ JPS@	FAILED TO STORE PR
6557	0033	XCT@ JPS@	SEQUENCE INCORRECT
6562	0033	XCT@ JPS@	CHANGED K REGISTER
6564	0033	XCT@ JPS@	CHANGED O REGISTER
6566	0033	XCT@ JPS@	CHANGED FLAG REGISTER
6571	0034	MARKER	SEQUENCE INCORRECT
6577	0034	XCT TWLDJ	SKIPPED ?
6602	0034	XCT TWLDJ	FAILED
6605	0034	XCT TWLDJ	CHANGED K REGISTER
6607	0034	XCT TWLDJ	CHANGED O REGISTER
6611	0034	XCT TWLDJ	CHANGED FLAG REGISTER
6616	0035	XCT TWISZ	FAILED OR SEQUENCE INCORRECT
6622	0035	XCT XCT TWLDJ	FAILED OR OUT OF SEQUENCE
6625	0035	XCT TWISZ	CHANGED K REGISTER
6627	0035	XCT TWISZ	CHANGED O REGISTER
6631	0035	XCT TWISZ	CHANGED FLAG REGISTER
6634	0036	XCT XCT TWISZ	FAILED OR WRONG SEQUENCE
6636-7	0036	XCT TWJMP	FAILED

MEMORY ADDRESS TEST (ND41-8004)

I. INTRODUCTION

A. This program is designed to test the addressing circuitry of the memory system to verify that each word has a unique address. This is accomplished by setting the contents of a word equal to the address and then checking the contents forwards and backwards.

B. PROGRAM AREA

$ØØØ3_8$ through $Ø127_8$.

C. STARTING ADDRESS

$ØØØ3_8$.

D. EQUIPMENT CONFIGURATION

Minimum requirements are a ND-812 Central Processor equipped with an ASR33 Teletype. An optional peripheral is a high speed reader.

II. PROGRAM DESCRIPTION

The program starts by storing $Ø13Ø_8$ in location $Ø13Ø_8$, $Ø131_8$ into $Ø131_8$, etc. Storage continues until the maximum word is reached, then the program reads location $Ø13Ø_8$ and verifies that the contents is $Ø13Ø_8$. Each word is read and verified through the maximum (7777_8), then read and verified starting at the maximum word through location $Ø13Ø_8$.

If an error is encountered, the teletype prints the number in the location, the current address (preceded by an "@") and a "D" if the program was decrementing. The teletype prints a "$" every time 64 passes are completed without an error.

This program will destroy the Binary Loader. Location $Ø127_8$ can be changed to a value less than $76ØØ_8$ to save the loader.

III. OPERATOR OR USER CONTROL

Location $Ø127_8$ can be changed to a value less than $76ØØ_8$ to save the Binary Loader.

IV. OPERATIONAL PROCEDURE

1. Load the Memory Address Test program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a detailed description of its use).

2. Set Switch Register to $ØØØ3_8$.

3. Depress LOAD ADDRESS.

4. Depress START.

5. The test can be terminated by depressing STOP.

V. ERROR DIAGNOSTICS

If an error is encountered, the teletype prints the number in the location, the current address (preceded by an "@") and a "D" if the program was decrementing.

75ØØ @ 77ØØ D

In the above example location 77ØØ contained a 75ØØ, and the program was decrementing. The correct value in this example is $77ØØ_8$, as each location in memory contains the actual address.

VI. COMMAND SUMMARY

None.

HIGH-LOW SPEED READER TEST (ND41-8005)

I INTRODUCTION

A. This program is designed to test the high or low speed readers using a tape loop.

B. PROGRAM AREA

$ØØØ2_8$ through $ØØ36_8$.

C. STARTING ADDRESS

$ØØØ2_8$.

D. EQUIPMENT CONFIGURATION

Minimum requirements are a ND812 Central Processor equipped with an ASR33 Teletype. An optional peripheral is a high speed reader.

II PROGRAM DESCRIPTION

The program reads a sequence of 0 to 255 ramps from a tape loop (supplied with diagnostic software package) until terminated or an error is detected. Depress CONTINUE to recover from an error condition.

Switch Register Bit Ø set to "1" indicates the use of a high speed reader and "Ø" a low speed reader.

III OPERATOR CONTROL

Switch Register Bit Ø set to "1" indicates the use of a high speed read and "Ø" a low speed reader. Depress CONTINUE to recover from an error condition.

IV OPERATION PROCEDURE

1. Load the High-Low Speed Reader Test program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a detailed description of its use).

2. Remove program tape from reader and replace it with the tape loop supplied with the Diagnostic Software Package.

3. Set Switch Register to $ØØØ2_8$.

4. Depress LOAD ADDRESS.

5. Set Switch Register Bit Ø to "1" for high speed reader and "Ø" for low speed reader.

6. Depress START.

7. The test can be terminated by depressing STOP.

V ERROR DIAGNOSTICS

The program will stop when an error is encountered. If the program stops at location $\emptyset\emptyset25_8$ it indicates that the program misread a character. When stopped at $\emptyset\emptyset34_8$ it indicates a loss of sync. In either case, the K register will contain the correct or expected character and the J register will contain the actual character read. Depress CONTINUE to recover from an error condition.

VI COMMAND SUMMARY

None.

LOW SPEED PUNCH TEST (NDI-8006)

I INTRODUCTION

A. This program is designed to test the punched paper tape output of the ASR33 Teletype for missing or extra levels.

B. PROGRAM AREA

$ØØØ2_8$ through $ØØ54_8$.

C. STARTING ADDRESS

$ØØØ2_8$.

D. EQUIPMENT CONFIGURATION

Minimum requirements are a ND-812 Central Processor and ASR33 Teletype.

II PROGRAM DESCRIPTION

The program punches 25 blank frames of tape, then a 0-255 ramp and repeats the sequence. The low speed reader verifies the punched tape and stops on error. When an error is detected, the program stops and the K register contains the expected data for the frame just read and the R register contains the actual erroneous data. Depressing CONTINUE causes the program to recover from the error condition.

III OPERATOR OR USER CONTROL

Depressing CONTINUE will cause the program to recover from an error condition.

IV OPERATION PROCEDURE

1. Load the Low Speed Punch Test program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a detailed description of its use).
2. Remove program tape from reader and place blank tape in low speed punch.
3. Place the teletype to LOCAL and turn low speed punch ON.
4. Depress HERE IS to provide sufficient leader to reach the reader head on the low speed reader.
5. Place leader in low speed reader, turn reader ON and place teletype to LINE.
6. Set Switch Register to $ØØØ2_8$.

7. Depress LOAD ADDRESS.

8. Depress START.

9. The program will now punch a number of 0-255 ramp and then verify the punched paper tape. Detecting an error causes the program to stop, refer to ERROR DIAGNOSTICS for description of error.

10. This test can be terminated by depressing STOP.

V. ERROR DIAGNOSTICS

If an error is detected, the program stops with the correct or expected data for the frame just read in the K register and actual data in the R register. Depressing CONTINUE recovers this program from an error condition.

VI. COMMAND SUMMARY

None.

HIGH SPEED PUNCH TEST (ND41-8007)

I. INTRODUCTION

A. This program is designed to test the accuracy and registration of the high speed punch with the high speed reader.

B. PROGRAM AREA

$ØØØ2_8$ through $Ø114_8$.

C. STARTING ADDRESS

$ØØØ2_8$.

D. EQUIPMENT CONFIGURATION

ND-812 Central Processor, ASR33 Teletype, high speed reader and high speed punch.

II. PROGRAM DESCRIPTION

The program punches an incrementing complementry pattern on tape at pseudo random intervals which are generated by a random number generator. Punched data is verified by the high speed read and stops on error. When an error is detected, the program stops at location $Ø112_8$ with the K register containing the expected data for the frame just read and the J register contains the actual erroneous data. Depressing CONTINUE causes the program to recover from the error condition.

III. OPERATOR OR USER CONTROL

Depressing CONTINUE will cause the program to recover from an error condition.

IV. OPERATION PROCEDURE

1. Load the High Speed Punch Test program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a detailed description of its use).

2. Remove program tape from reader and place blank tape in high speed punch.

3. Turn high speed punch ON.

4. Depress the PAPER ADVANCE to provide sufficient leader to reach the reader head on the high speed reader.

5. Place leader in high speed reader, turn reader ON and teletype to LINE.

6. Set Switch Register to $\emptyset\emptyset\emptyset 2_8$.

7. Depress LOAD ADDRESS.

8. Depress START.

9. The program will punch random patterns on paper tape and verify the outputted data. Detection of an error causes the program to stop. Refer to the ERROR DIAGNOSTICS for description of error.

10. This test can be terminated by depressing STOP.

V. ERROR DIAGNOSTICS

When an error is detected, the program stops at location $\emptyset 112_8$ with the correct or expected data for the frame just read in the K register and the actual data in the J register. Depress CONTINUE to recover from this condition.

VI. COMMAND SUMMARY

None.

HIGH SPEED READER TEST (ND41-8008)

I. INTRODUCTION

A. This program is designed to test the high speed reader for accuracy and stopping ability with random length character blocks.

B. PROGRAM AREA

$ØØØ2_8$ through $Ø124_8$.

C. STARTING ADDRESS

$ØØØ2_8$.

D. EQUIPMENT CONFIGURATION

ND-812 Central Processor, ASR33 Teletype and high speed reader.

II. DESCRIPTION

The program reads a random number of characters from a tape loop consisting of a sequence of 0-255 ramps (supplied with diagnostic software package). The tape will stop for an interval that is determined by setting of Switch Register BITS 8 through 11. The minimum time interval is 24 milliseconds and the maximum interval is 350 milliseconds.

After the time delay, the program re-reads the last character to verify that no over shoots occurred and then reads new random numbers and repeats until an error is found. If an error is encountered, the program outputs the correct character, the actual character, and time delay and resumes program execution.

III. OPERATOR OR USER CONTROL

Switch Register BITS 8 through 11 determine the time delay between blocks. Minimum time interval is 24 milliseconds (BIT 11 set to "1") and 350 milliseconds maximum (BITS 8 through 11 set to "1").

IV. OPERATION PROCEDURE

1. Load the High Speed Reader Test program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a detailed description of its use).

2. Remove program tape from reader, place tape loop supplied with the Diagnostic Software Package in the high speed reader and turn high speed reader ON.

3. Set Switch Register to $ØØØ2_8$.

4. Depress LOAD ADDRESS.

5. Set the Switch Register to desired time delay (BITS 8 through 11).

6. Depress START.

7. This test will run until manually terminated. If an error is encountered, refer to ERROR DIAGNOSTICS for description of output data.

8. The test can be terminated by depressing STOP.

V. ERROR DIAGNOSTICS

When an error is encountered the program prints the correct or expected character, the actual character read, and the time delay in milliseconds.

```
1743    1740    48
```

The program automatically recovers from an error condition.

VI. COMMAND SUMMARY

None.

RANDOM ISZ-DSZ TEST (ND41-8013)

I. INTRODUCTION

A. This program is designed to test ISZ and DSZ Memory Reference Instruction using random or fixed addresses.

B. PROGRAM AREA

$ØØØØ_8$ through $Ø246_8$.

C. STARTING ADDRESS

$ØØ44_8$.

D. EQUIPMENT CONFIGURATION

Minimum requirements are a ND-812 Central Processor equipped with an ASR33 Teletype. An optional peripheral is a high speed reader.

II. PROGRAM DESCRIPTION

The program starts by reading the Switch Register to determine the instruction, method of addressing and random or fixed numbers. Then random reference and effective addresses are selected and the instruction is executed. If the addresses are fixed, the program continues to execute the instruction with the first selection of random addresses until an error is detected or the program is terminated. With the selection of random addresses, the program clears old locations and selects new random addresses for each test and continues until an error is detected or the program is terminated. Changing Switch Register BITS 1, 2 and 3 during a test can generate an error. Disregard this error and depress CONTINUE to recover from the error condition. When 4096 tests are completed without an error, a bell is rung by the teletype.

This program selects random addresses which interjects the possibility of destroying locations occupied by the Binary Loader. If the user wishes to alleviate this condition, he need only change location $Ø246_8$ of this program to a value less than $76ØØ_8$.

III. OPERATOR OR USER CONTROL

Switch Register BIT Ø set to "1" selects fixed addresses, set to "Ø" random addresses. BIT 1 set to "1" selects either direct or indirect addressing (as determined by BIT 2), set to "Ø" alternates direct and indirect addressing. BIT 2 set to "1" (if BIT 1 is "1") selects indirect addressing, set to "Ø" selects direct addressing. BIT 3 set to "1" selects an ISZ test, set to "Ø" a DSZ test.

Location $Ø246_8$ can be changed to a value less that $76ØØ_8$ to save the Binary Loader.

IV. OPERATION PROCEDURE

1. Load the Random ISZ-DSZ program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a detailed description of its use).

2. Set the Switch Register to $\emptyset\emptyset44_8$.

3. Depress LOAD ADDRESS.

4. Set the Switch Register to the test desired. (Switch Register BIT $\emptyset$ set to "1" selects fixed addresses, set to "$\emptyset$" random addresses. BIT 1 set to "1" selects either direct or indirect addressing (as determined by BIT 2), set to "$\emptyset$" alternates direct and indirect addressing. BIT 2 set to "1" (if BIT 1 is "1") selects indirect addressing, set to "$\emptyset$" selects direct addressing. BIT 3 set to "1" selects an ISZ test, set to "$\emptyset$" a DSZ test).

5. Depress START.

6. The test can be terminated by depressing STOP .

V. ERROR DIAGNOSTICS

Changing Switch Register BITS 1, 2 and 3 during a test can generate an error. Disregard this error and depress CONTINUE to recover from the error condition. When the program stops at location $\emptyset\emptyset43_8$, a detectable error has occurred. The R register contains the correct number before the test operation, the K register contains the address of the instruction tested, the J register contains the address of the memory location being tested, and the overflow light (if on) indicates the instruction was indirect. Depress CONTINUE to recover from this error condition.

If the program stops at location 0125_8, the JMP@ failed. To recover from this error condition, re-start the program from Step 2 of the Operation Procedure.

VI. COMMAND SUMMARY

None.

RANDOM ADJ-SBJ TEST (ND41-8014)

I. INTRODUCTION

A. This program is designed to test ADJand SBJ Memory Reference Instruction using random or fixed addresses.

B. PROGRAM AREA

$ØØØØ_8$ through $Ø24Ø_8$.

C. STARTING ADDRESS

$ØØ25_8$.

D. EQUIPMENT CONFIGURATION

Minimum requirements are a ND-812 Central Processor equipped with an ASR33 Teletype. An optional peripheral is a high speed reader.

II. PROGRAM DESCRIPTION

The program starts by reading the Switch Register to determine the instruction, method of addressing, and random or fixed numbers. Then random reference and effective addresses are selected and the instruction is executed. If the addresses are fixed, the program continues to execute the instruction with the first selection of random addresses until an error is detected or the program is terminated. With the selection of random addresses, the program clears old locations and selects new random addresses for each test and continues until an error is detected or the program is terminated. Changing Switch Register BITS 1,2 and 3 during a test can generate an error. Disregard this error and depress CONTINUE to recover from the error condition. When 4096 tests are completed without an error, a bell is rung by the teletype.

This program selects random addresses which interjects the possibility of destroying locations occupied by the Binary Loader. If the user wishes to alleviate this condition, he need only change location $Ø24Ø_8$ of this program to a value less than $76ØØ_8$.

III. OPERATOR OR USER CONTROL

Switch Register BIT Ø set to "1" selects fixed addresses, set to "Ø" random addresses. BIT 1 set to "1" selects either direct or indirect addressing (as determined by BIT 2), set to "Ø" alternates direct and indirect addressing. BIT 2 set to "1" (if BIT 1 is "1") selects indirect addressing, set to "Ø" selects direct addressing. BIT 3 set to "1" selects an ADJ test, set to "Ø" a SBJ test.

Location $Ø24Ø_8$ can be changed to a value less than $76ØØ_8$ to save the Binary Loader.

IV. OPERATION PROCEDURE

1. Load the Random ADJ-SBJ program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a detailed description of its use).

2. Set the Switch Register to $ØØ25_8$.

3. Depress LOAD ADDRESS.

4. Set the Switch Register to the test desired. (Switch Register BIT Ø set to "1" selects fixed addresses, set to "Ø" random addresses. BIT 1 set to "1" selects either direct or indirect addressing (as determined by BIT 2), set to "Ø" alternates direct and indirect addressing. BIT 2 set to "1" (if BIT 1 is "1") selects indirect addressing, set to "Ø" selects direct addressing. BIT 3 set to "1" selects an ADJ test, set to "Ø" a SBJ test).

5. Depress START.

6. The test can be terminated by depressing STOP.

V. ERROR DIAGNOSTICS

Changing Switch Register BITS 1, 2 and 3 during a test can generate an error. Disregard this error and depress CONTINUE to recover from the error condition.

When the program stops at location $ØØ24_8$ a detectable error has occurred. The K register contains operand 1, the R register operand 2, the J register the result and the overflow light (if on) indicates the instruction was indirect. Depress CONTINUE to recover from this error condition.

If the program stops at location $Ø117_8$, the JMP@ failed. To recover from this error condition, re-start the program from Step 2 of the Operation Procedure.

VI. COMMAND SUMMARY

None.

RANDOM LDJ-STJ TEST (ND41-8015)

I. INTRODUCTION

A. This program is designed to test LDJ and STJ Memory Reference Instruction using random or fixed addresses.

B. PROGRAM AREA

$ØØØØ_8$ through $Ø242_8$.

C. STARTING ADDRESS

$ØØ3Ø_8$.

D. EQUIPMENT CONFIGURATION

Minimum requirements are a ND-812 Central Processor equipped with an ASR33 Teletype. An optional peripheral is a high speed reader.

II. PROGRAM DESCRIPTION

The program starts by reading the Switch Register to determine the instruction, method of addressing, and random or fixed numbers. Then random reference and effective addresses are selected and the instruction is executed. If the addresses are fixed, the program continues to execute the instruction with the first selection of random addresses until an error is detected or the program is terminated. With the selection of random addresses, the program clears old locations and selects new random addresses for each test and continues until an error is detected or the program is terminated. Changing Switch Register BITS 1, 2 and 3 during a test can generate an error. Disregard this error and depress CONTINUE to recover from the error condition. When 4096 tests are completed without an error, a bell is rung by the teletype.

This program selects random addresses which interjects the possibility of destroying locations occupied by the Binary Loader. If the user wishes to alleviate this condition, he need only change location $Ø242_8$ of this program to a value less than $76ØØ_8$.

III. OPERATOR OR USER CONTROL

Switch Register BIT Ø set to "1" selects fixed addresses, set to "Ø" random addresses. BIT 1 set to "1" selects either direct or indirect addressing (as determined by BIT 2), set to "Ø" alternates direct and indirect addressing. BIT 2 set to "1" (if BIT 1 is "1") selects indirect addressing, set to "Ø" selects direct addressing. BIT 3 set to "1" selects an LDJ test, set to "Ø" an STJ test.

Location $Ø242_8$ can be changed to a value less than $76ØØ_8$ to save the Binary Loader.

IV. OPERATION PROCEDURE

1. Load the Random LDJ-STJ program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a detailed description of its use).

2. Set the Switch Register to $ØØ3Ø_8$.

3. Depress LOAD ADDRESS.

4. Set the Switch Register to the test desired. (Switch Register BIT Ø set to "1" selects fixed addresses, set to "Ø" random addresses. BIT 1 set to "1' selects either direct or indirect addressing (as determined by BIT 2), set to "Ø" alternates direct and indirect addressing. BIT 2 set to "1" (if BIT 1 is "1") selects indirect addressing, set to "Ø" selects direct addressing. BIT 3 set to "1" selects an LDJ test, set to "Ø" an STJ test).

5. Depress START.

6. The test can be terminated by depressing STOP.

V. ERROR DIAGNOSTICS

Changing Switch Register BITS 1, 2 and 3 during a test can generate an error. Disregard this error and depress CONTINUE to recover from the error condition. When the program stops at location $ØØ27_8$, a detectable error has occurred. The K register contains the correct number before the test operation, the J register contains the actual number, and the overflow light (if on) indicates the instruction was indirect. Depress CONTINUE to recover from this error condition.

If the program stops at location $Ø121_8$, the JMP@ failed. To recover from this error condition, re-start the program from Step 2 of the Operation Procedure.

VI. COMMAND SUMMARY

None.

RANDOM JMP-JPS TEST (ND41-8016)

I. INTRODUCTION

A. This program is designed to test JMP and JPS Memory Reference Instruction using random or fixed addresses.

B. PROGRAM AREA

$ØØØØ_8$ through $Ø25Ø_8$.

C. STARTING ADDRESS

$ØØ31_8$.

D. EQUIPMENT CONFIGURATION

Miminum requirements are a ND-812 Central Processor equipped with an ASR33 Teletype. An optional peripheral is a high speed reader.

II. PROGRAM DESCRIPTION

The program starts by reading the Switch Register to determine the instruction, method of addressing, and random or fixed numbers. Then random reference and effective addresses are selected and the instruction is executed. If the addresses are fixed, the program continues to execute the instruction with the first selection of random addresses until an error is detected or the program is terminated. With the selection of random addresses, the program clears old locations and selects new random addresses for each test and continues until an error is detected or the program is terminated. Changing Switch Register BITS 1, 2, and 3 during a test can generate as error. Disregard this error and depress CONTINUE to recover from the error condition. When 4096 tests are completed without an error, a bell is rung by the teletype.

This program selects random addresses which interjects the possibility of destroying locations occupied by the Binary Loader. If the user wishes to alleviate this condition, he need only change location $Ø1Ø1_8$ of this program to a value less than $76ØØ_8$.

III. OPERATOR OR USER CONTROL

Switch Register BIT Ø set to "1" selects fixed addresses, set to "Ø" random addresses. BIT 1 set to "1" selects either direct or indirect addressing (as determined by BIT 2), set to "Ø" alternates direct and indirect addressing. BIT 2 set to "1" (if BIT 1 is "1") selects indirect addressing, set to "Ø" selects direct addressing. BIT 3 set to "1" selects a JMP test, set to "Ø" a JPS test.

Location $Ø1Ø1_8$ can be changed to a value less than $76ØØ_8$ to save the Binary Loader.

IV. OPERATION PROCEDURE

1. Load the Random JMP-JPS program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a detailed description of its use).

2. Set the Switch Register to $ØØ31_8$.

3. Depress LOAD ADDRESS.

4. Set the Switch Register to the test desired. (Switch Register BIT Ø set to "1" selects fixed addresses, set to "Ø" random addresses. BIT 1 set to "1" selects either direct or indirect addressing (as determined by BIT 2), set to "Ø" alternates direct and indirect addressing. BIT 2 set to "1" (if BIT 1 is "1") selects indirect addressing, set to "Ø" selects direct addressing. BIT 3 set to "1" selects a JMP test, set to "Ø" a JPS test).

5. Depress START.

6. The test can be terminated by depressing STOP.

V. ERROR DIAGNOSTICS

Changing Switch Register BITS 1, 2 and 3 during a test can generate an error. Disregard this error and depress CONTINUE to recover from the error condition. When the program stops at location $ØØ3Ø_8$, a detectable error has occurred. The R register contains the correct number before the test operation, the K register contains the address of the instruction tested, the J register contains the address of the memory location being tested, and the overflow light (if on) indicates the instruction was indirect. Depress CONTINUE to recover from this error condition.

If the program stops at location $Ø232_8$, the JMP@ failed. To recover from this error condition, re-start the program from Step 2 of the Operation Procedure.

VI. COMMAND SUMMARY

None.

HARDWARE MULTIPLY AND DIVIDE TEST (ND41-8019)

I. INTRODUCTION

A. This program is designed to test the hardware multiply and divide features.

B. PROGRAM AREA

$Ø16Ø_8$ through $Ø522_8$.

C. STARTING ADDRESSES

$Ø2ØØ_8$ hardware divide.
$Ø4ØØ_8$ hardware multiply.

D. EQUIPMENT CONFIGURATION

Minimum requirements are a ND-812 Central Processor equipped with an ASR33 Teletype.

E. DEFINITIONS

None.

II. PROGRAM DESCRIPTION

Testing the hardware multiply feature is accomplished by generating two random numbers and storing them as Operand 1 and Operand 2. Next a software multiply is executed with Operand 1 and Operand 2, followed by a hardware multiply. The products are compared and if equal, two new random operands are generated. It is possible to fix the operands by placing Switch Register BIT Ø to "1". If an error is detected the difference is printed in the following format:

Oper 1	Oper 2	Software Product	Hardware Product
XXXX	YYYY	AAAAAAAA	BBBBBBBB

Random operands should be selected for the hardware divide test, as the old set used in the previous test run are added to provide the divisor for the current test run. At the start of a hardware divide test, two random numbers (Operand 1 and 2) are generated for the dividend and the operands used in the previous test are added to provide the divisor. A software divide is executed followed by a hardware divide. The quotients, remainders and overflow states are compared and if equal, new random numbers are generated for the next test run. If an error is detected, the difference is printed in the following format:

Divisor	Oper 1-Oper 2	Software Remainder	Software Quotient	Hardware Remainder	Hardware Quotient	Overflow
XXXX	YYYYZZZZ	AAAA	BBBB	CCCC	DDDD	O

The overflow indicates an attempt to divide by zero or the K register portion of the divisor is greater than the dividend.

III. OPERATOR OR USER CONTROL

$Ø2ØØ_8$ is the starting address for hardware divide and $Ø4ØØ_8$ is the hardware multiply starting address.

Switch Register BIT Ø set to "1" selects new random operands.

NOTE: The hardware division test should be run with random operands.

IV. OPERATION PROCEDURE

1. Load the Hardware Multiply and Divide Test program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a description of its use).
2. Set the Switch Register to $Ø2ØØ_8$ for divide or to $Ø4ØØ_8$ for multiply.
3. Depress LOAD ADDRESS.
4. Set Switch Register BIT Ø to specify random or fixed operands.
5. Depress START.
6. This test can be terminated by depressing STOP.

V. ERROR DIAGNOSTICS

It is assumed that the software multiply and divide are correct. If the user is not positive that the software functions are correct, the following addition and multiplication tables can be used to calculate the answer.

Addition

0	01	02	03	04	05	06	07
1	02	03	04	05	06	07	10
2	03	04	05	06	07	10	11
3	04	05	06	07	10	11	12
4	05	06	07	10	11	12	13
5	06	07	10	11	12	13	14
6	07	10	11	12	13	14	15
7	10	11	12	13	14	15	16

Multiplication

1	02	03	04	05	06	07
2	04	06	10	12	14	16
3	06	11	14	17	22	25
4	10	14	20	24	30	34
5	12	17	24	31	36	43
6	14	22	30	36	44	52
7	16	25	34	43	52	61

If an error is encountered during a hardware multiply test, the data is printed by the teletype in the following format:

Oper 1	Oper 2	Software Product	Hardware Product
1234	4567	Ø61312Ø4	Ø61312ØØ

```
  4567
  1234
 22734
 16145
 11356
  4567
Ø61312Ø4
```

During a hardware divide test, data is printed in the following format:

Divisor	Oper 1-Oper 2	Software Remainder	Software Quotient	Hardware Remainder	Hardware Quotient	Over-flow
1234	Ø61312Ø4	ØØØØ	4567	ØØØ4	4567	

```
        4567
1234⌐06131304
     5160
     7512
     6414
     10760
      7650
      10104
      10104
```

VI. COMMAND SUMMARY

None.

MULTIPLE FIELD RANDOM TWJPS-TWJPS@ AND INTERRUPT TEST - 8K/16K (ND41-8026)

I. INTRODUCTION

A. This program is designed to test TWJPS, TWJPS@ and interrupt with random effective and absolute addresses.

B. PROGRAM AREA

$ØØØØ_8$ through $Ø351_8$.

C. STARTING ADDRESS

$ØØ76_8$.

D. EQUIPMENT CONFIGURATION

Minimum requirements are an 8K or 16K ND-812 Central Processor equipped with an ASR-33 Teletype.

E. DEFINITIONS

None.

II. PROGRAM DESCRIPTION

This program starts by generating a 24-bit random number with the lower 12-bits (J register) representing the address selected for the TWJPS instruction in the "FROM" field. The lower 2-bits of the K register (upper 12-bits of random number) indicate the memory field selected as the "FROM FIELD". Another 24-bit random number is generated with the lower 12-bits selecting an effective address used for a TWJPS@ instruction. Still another 24-bit random number is generated with the lower 12-bits selecting an absolute address for destination within the "TO FIELD" and the lower 2-bits of the K register (upper 12-bits of random number) selecting the memory field designated as the "TO FIELD".

These above described numbers are loaded in the respective memory fields accompanied with a short program that tests the interrupt logic and the two-word instruction is executed. New random numbers are generated for each test and the teletype bell is rung when 4096 tests are successfully completed.

This program is designed to select random addresses that fall between locations $Ø352_8$ through 7573_8 in any memory field, consequently eliminating the possibility of destroying the Binary Loader (ND41-0005)

III. OPERATOR OR USER CONTROL

Switch Register BIT Ø is used to indicate the number of memory fields in which this test is to be run. BIT Ø set to "1" selects memory fields Ø and 1 (8K), and set to "Ø" selects memory fields Ø, 1, 2 and 3 (16K).

When Switch Register BIT 1 is set to "1", the first selection of random numbers is used for every test operation. With BIT 1 set to "Ø", new random numbers are generated for each test.

IV. OPERATION PROCEDURE

1. Load the Multiple Field Random TWJPS-TWJPS@ and Interrupt Test program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a description of its use.

2. Set the Switch Register to $ØØ76_8$.

3. Depress LOAD AR.

4. Select memory field and fixed or random numbers (BITS Ø and 1).

5. Depress START.

6. The program will begin execution and the teletype bell is rung every 4096 correct test operations. If the program stops, refer to the ERROR DIAGNOSTICS.

7. This test can be terminated by depressing STOP.

V. ERROR DIAGNOSTICS

The analysis of an error condition detected by this program requires the PROGRAM LISTING section and the knowledge of the subroutine which is randomly placed in memory and executed.

Commission of an error causes the processor to stop. If the stop address is between $ØØØØ_8$ and $Ø351_8$, refer to the Program Listing for the cause of failure. Any stop address that does not fall within these limits can indicate many different failures. The user should check the values for FROM (location $Ø162_8$), INDWRD (location $Ø163_8$), DEST ($Ø164_8$), FRMFLD ($Ø165_8$), TOFLD ($Ø166_8$) and write them on paper. These values can then be used in the following program to find the problem.

```
IN "FROM" FIELD:  FROM,    TWJPS (@)  ("TO" FIELD)
                           DEST  (INDWRD)
                           TWJMP   FØ      604
                           START           76

                  INDWRD, Ø    (DEST)

IN "TO" FIELD:    DEST,    Ø               Ø
                           IONN            1007
                           IDLE            1400
                           JMP@  DEST      6303
```

VI. COMMAND SUMMARY

None.

MULTIPLE FIELD RANDOM TWJPS-TWJPS@ AND INTERRUPT TEST - 12K (ND41-8028)

I. INTRODUCTION

A. This program is designed to test TWJPS, TWJPS@ and interrupt with random effective and absolute addresses.

B. PROGRAM AREA

$ØØØØ_8$ through $Ø351_8$.

C. STARTING ADDRESS

$ØØ76_8$.

D. EQUIPMENT CONFIGURATION

Minimum requirements are 12K ND-812 Central Processor equipped with an ASR-33 Teletype.

E. DFINITIONS

None.

II. PROGRAM DESCRIPTION

This program starts by generating a 24-bit random number with the lower 12-bits (J register) representing the address selected for the TWJPS instruction in the "FROM" field. The lower 2-bits of the K register (upper 12-bits of random number) indicate the memory field selected as the "FROM FIELD". Another 24-bit random number is generated with the lower 12-bits selecting an effective address used for a TWJPS@ instruction. Still another 24-bit random number is generated with the lower 12-bits selecting an absolute address for destination within the "TO FIELD" and the lower 2-bits of the K register (upper 12-bits of random number) selecting the memory field designated as the "TO FIELD".

These above described numbers are loaded in the respective memory fields accompanied with a short program that tests the interrupt logic and the two-word instruction is executed. New random numbers are generated for each test and the teletype bell is rung when 4096 tests are successfully completed.

This program is designed to select random addresses that fall between locations $Ø352_8$ through 7573_8 in any memory field, consequently eliminating the possibility of destroying the Binary Loader (ND41-0005).

III. OPERATOR OR USER CONTROL

Switch Register BIT Ø is used to indicate the number of memory fields in which this test is to be run. For this test, set BIT Ø to "1" to select memory fields Ø, 1 and 2 (12K).

When Switch Register BIT 1 is set to "1", the first selection of random numbers is used for every test operation. With BIT 1 set to "Ø", new random numbers are generated for each test.

IV. OPERATION PROCEDURE

1. Load the Multiple Field Random TWJPS-TWJPS@ and Interrupt Test program tape with the Binary Loader (refer to the Binary Loader (ND41-0005) for a description of its use.

2. Set the Switch Register to $ØØ76_8$.

3. Depress LOAD AR.

4. Select memory field and fixed or random numbers (BITS Ø and 1).

5. Depress START.

6. The program will begin execution and the teletype bell is rung every 4096 correct test operations. If the program stops, refer to the ERROR DIAGNOSTICS.

7. This test can be terminated by depressing STOP.

V. ERROR DIAGNOSTICS

The analysis of an error condition detected by this program requires the PROGRAM LISTING section and the knowledge of the subroutine which is randomly placed in memory and executed.

Commission of an error causes the processor to stop. If the stop address is between $ØØØØ_8$ and $Ø351_8$, refer to the Program Listing for the cause of failure. Any stop address that does not fall within these limits can indicate many different failures The user should check the values for FROM (location $Ø162_8$), INDWRD (location $Ø163_8$), DEST ($Ø164_8$), FRMFLD ($Ø165_8$), TOFLD ($Ø166_8$) and write them on paper. These values can then be used in the following program to find the problem.

```
IN "FROM" FIELD:    FROM,     TWJPS (@) ("TO" FIELD)
                              DEST (INDWRD)
                              TWJPS    FØ    604
                              START          76

                    INDWRD,   Ø    (DEST)

IN "TO" FIELD:      DEST,     Ø              Ø
                              IONN           1007
                              IDLE           1400
                              JMP@   DEST    6303
```

VI. COMMAND SUMMARY

None.

WORST CASE MEMORY EXERCISER (ND41-8036)

I. INTRODUCTION

A. PROGRAM SUMMARY

The Worst Case Memory Exerciser (ND41-8036) Program is designed as an in system test of the ND812 memory components in a manner which is particularly demanding of these components.

B. PROGRAM AREA

This program initially occupies locations $ØØØ2_8$ thru $Ø231_8$, Field Ø. During execution, it occupies the same locations in successive fields.

C. STARTING ADDRESS

The starting address is $ØØØ2_8$, Field Ø.

D. EQUIPMENT CONFIGURATION

The minimum equipment configuration required to properly execute this program is: a 4K ND812 Central Processor and a TC33ASR Teletype.

II. PROGRAM DESCRIPTION

This program retrieves a 12-bit word entered via the Switch Register. It fills a 4K area (the next higher field) of memory with the word, in a worst case pattern, word or complement, and then reads the pattern, checking for errors. If an error occurs, it signals the operator by halting. If no errors occur, the program updates the pattern by rotating the 12 bits one position and reiterates the write, read, check sequence of operations. Once 12 rotations are completed, the pattern is complemented and the write, read, check cycle with 12 rotations is reinitiated. After the check complement routine is completed, the program transposes itself to the next higher field and executes in that field, again operating upon the next higher field. If the highest field is the current one in which the program is running, it will transpose itself to the lowest field in a wrap-around manner.

This program is written primarily to check DATARAM, 12 and 24 bit memory stacks. If the Plessey stacks are to be checked, memory location $Ø153_8$ should be changed to read 1400. Also, a new version of the DATARAM 24 bit stack may be tested, requiring two changes in the program: location $Ø153_8$ to read 1400; location $Ø147_8$ to read 1400.

III. OPERATOR OR USER CONTROL

Once the program has been entered, using the procedures outlined in Section 4, the operator sets up the test word in the Switch Register. He depresses the RUN Switch and the program begins execution. The program will continue to run until an error occurs or if the operator manually stops the program by depressing the HALT Switch. The bit pattern may be changed while the program is running, but the change will only be sensed at the end of a pass, which may be as long as thirty seconds.

Approximate running time for the program should be from fifteen to thirty minutes. If no errors occur during this time, the test may be considered as having been withstood successfully.

IV. OPERATIONAL PROCEDURE

A. LOADING PROCEDURE

The Worst Case Memory Exerciser Program (ND41-8036) is entered in the following manner.

1. Set the Memory Field Switches, MFØ and MF1 in the down position.

2. Place the program tape leader (8-level punched only) over the reader head.

3. Turn the reader on.

4. Depress both the LOAD AR and NEXT WORD switches at the same time.

5. The hardware loader will load the program. Tape motion will stop automatically when the trailer (8-level punched only) punches are sensed. At this point, the J Register should read all zeros. If not, repeat steps 2 thru 4.

B. PROGRAM MODIFICATION

After the program has been loaded, it may be modified to test one of three types of core stacks. As it presently exists, it will test the DATARAM 12 and 24 bit stacks. To modify the program to test Plessey stacks, perform the following.

1. Set the Switch Register to $Ø153_8$ and depress the LOAD AR Switch.

2. Set the Switch Register to $14ØØ_8$ and depress the LOAD MR Switch.

3. The program is now modified to test Plessey core stacks.

To modify the program to test the newer version of the DATARAM 24-bit stacks, perform the following.

1. Set the Switch Register to $\emptyset153_8$ and depress the LOAD AR Switch.

2. Set the Switch Register to $14\emptyset\emptyset_8$ and depress the LOAD MR Switch.

3. Set the Switch Register to $\emptyset147_8$ and depress the LOAD AR Switch.

4. Set the Switch Register to $14\emptyset\emptyset_8$ and depress the LOAD MR Switch.

C. PROGRAM INITIALIZATION

The program is initialized in the following manner.

1. Set the Switch Register to the starting address $\emptyset\emptyset\emptyset2_8$ and depress the LOAD AR key.

2. Set the Switch Register to the pattern desired. (NOTE: The address $\emptyset\emptyset\emptyset2_8$ already contains a desireable pattern. In which case, this step may not be necessary.)

3. Depress the RUN Switch.

V. ERROR DIAGNOSTICS

A. ERROR INDICATORS

If the program halts during execution, verify the following registers for diagnosis.

1. J Register: If a bit was picked up erroneously, the corresponding bit position will be lit and all others will be off. If a bit was dropped, the corresponding bit position will be off and all other more significant bits (bits to the left of dropped bit) will be lit.

2. K Register: This register will contain the correct pattern.

3. ADDR Register: This register will contain the address in the next higher field at which the error occured. If the current field is Field 3, the error address will be in Field $\emptyset$.

B. RESTART PROCEDURE

1. After the error has been checked, depress the CONTINUE Switch.

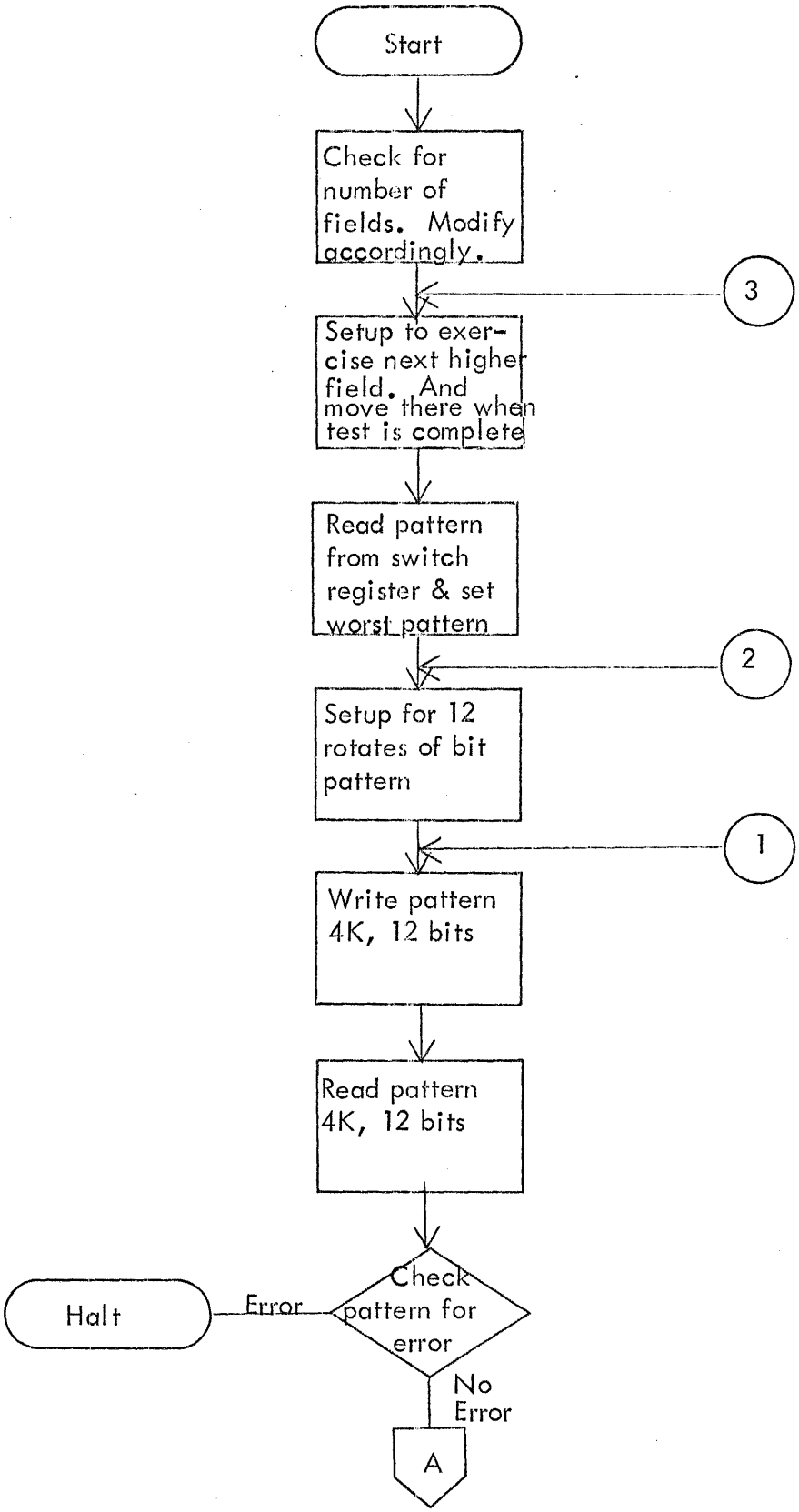
2. If the program is to be started anew, reload the program according to the procedure outlined in Section 4.

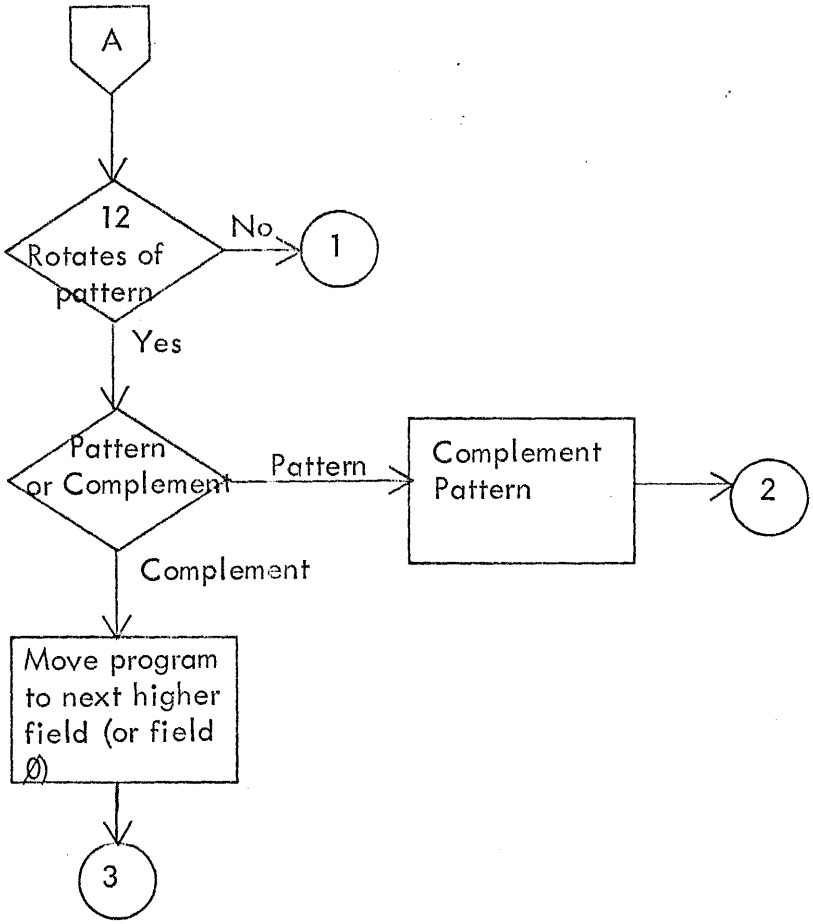
VI. COMMAND SUMMARY

None.

VII. FLOW CHARTS

Next Page.


Start
Check for number of fields. Modify accordingly.
3
Setup to exercise next higher field. And move there when test is complete
Read pattern from switch register & set worst pattern
2
Setup for 12 rotates of bit pattern
1
Write pattern 4K, 12 bits
Read pattern 4K, 12 bits
Check pattern for error
Error
Halt
No Error
A


A
12
Rotates of
pattern
No
1
Yes
Pattern
or Complement
Pattern
Complement
Pattern
2
Complement
Move program
to next higher
field (or field
Ø)
3