DIGITAL COMPUTER NEWSLETTER

The purpose of this newsletter is to provide a medium for the interchange among interested persons of information concerning recent developments in various digital computer projects. Distribution is limited to government agencies, contractors, and contributors.

OFFICE OF NAVAL RESEARCH · PHYSICAL SCIENCES DIVISION

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Approved by
The Under Secretary of the Navy
16 August 1954

COMPUTERS, U.S.A.

ABERDEEN PROVING GROUND COMPUTERS

The following statistics show the machine hours for the three high-speed computers for the "average" week for the period 0800 26 November 1954 to 0800 20 May 1955:

	ORDVAC	EDVAC	ENIAC
A. Engineering Time			
1. System Improvement	2.5	0.5	0.8
2. Engineering Servicing	39.4	36.9	60.0
Total Engineering	41.9	37.4	60.8
B. Chargeable Time			
1. Code Checking	33.4	32.1	1.5
2. Production	61.8	68.5	44.6
Total Chargeable Time	95.2	100.6	46.1
C. Non-Chargeable Time Due to			
1. Machine Causes	10.4	8.2	4.2
2. Non-Machine Causes	19.1	16.7	3.7
Total Non-Chargeable Time	29.5	24.9	7.9
D. Idle Time	1.1	1.3	51.8
E. Standby Time	0.3	2.8	1.4
GRAND TOTAL	168.0	168.0	168.0

The Bell Relay Calculators have been transferred from the Computing Laboratory, BRL to CONARC Board Number 4, Fort Bliss, Texas.

The CRC-105 Digital Differential Analyzer has been transferred from the Computing Laboratory, BRL to the Ballistic Measurements Laboratory, BRL.

THE BURROUGHS E101

The Burroughs E101 is a desk size, general purpose, low cost electronic computer. It is designed to be intermediate in both price and performance between a battery of desk top calculators on one hand, and a giant computing installation on the other. It combines the powerful features of the large-scale computers with the convenience and simplicity of manual methods.

The E101 uses the full keyboard of a Burroughs bookkeeping machine for data input, and the tabulating page printer of the same machine for data output. Its external program is embodied in the positions of pins inserted into the removable pinboard units. It stores constants intermediate results, and final answers on a magnetic drum.

An optional Punched Paper Tape Input Unit can be used both to bypass the keyboard for the entry of data, and to supplement the instructions in the pinboard program. Figure 1 shows this unit in position alongside the E101.

E101 specifications are as follows:

Input:	11-column full keyboard of Burroughs bookkeeping machine; optional Punched Tape Unit will read 5-, 6-, 7-, or 8- channel tape
Output:	24 digits per second semi-gang page printer; completely flexible format control on rolls or forms up to 18 inches wide; front feed insert for unit documents
Number System:	Pulse coded decimal, internal and external; word length of 12 digits (plus sign)
Storage:	Magnetic drum memory, 100 word capacity; 3600 rpm; programmed split-register storage
Programming:	Machine language of 28 single-address instructions; program controlled by placement of pins in 8 removable pinboards, providing 128 program steps; 2 automatic address-modification counters with programmed limits; unconditional transfer instructions; master or supplementary instructions can be read from tape
Speed:	Addition and subtraction at 20 per second, multiplication and division at 4 per second, including access times
Size:	All components completely self-contained in a single desk-size cabinet (on casters) 60 inches wide by 38 inches deep
Power:	Requires 220-volt, single phase, 3-wire line; dissipates about 2500 watts

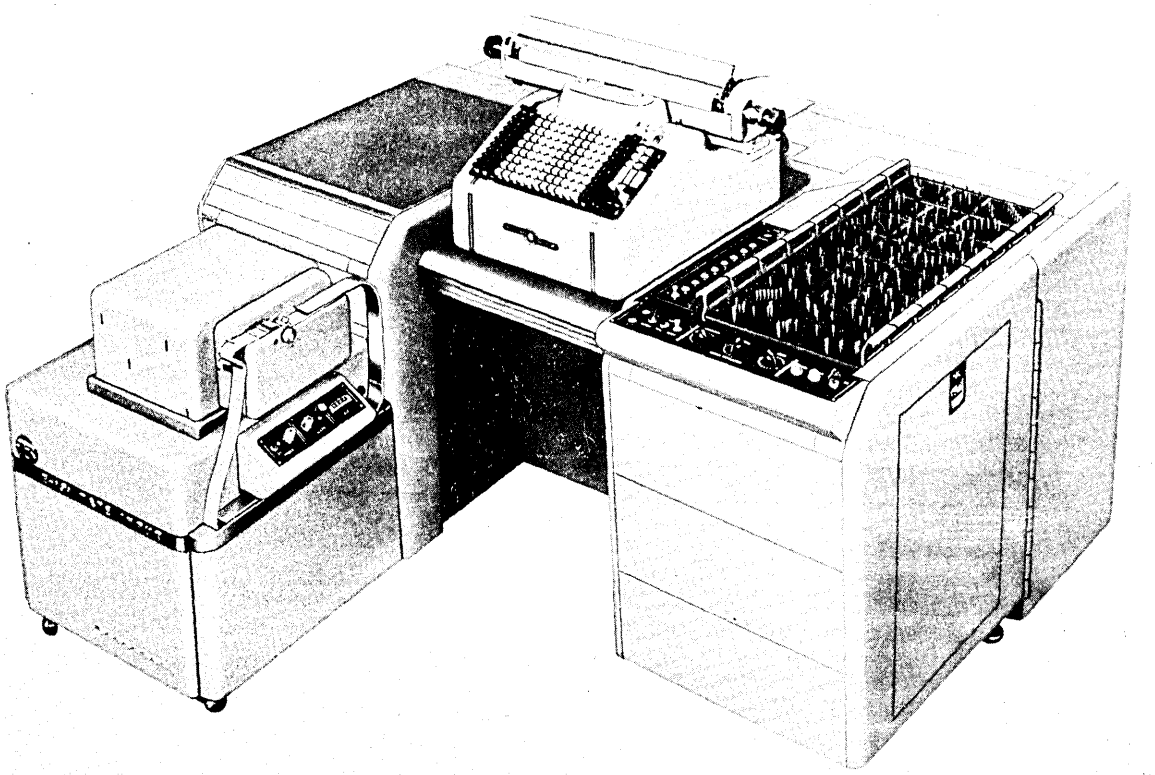

Figure 1. Burroughs E101

IBM—608

International Business Machines Corporation has announced a commercially-available transistorized computer called the 608, with several times the calculating speed and storage capacity of the experimental model the company demonstrated several months ago. Deliveries will begin early in 1956.

The new machine is the first completely transistorized computer available for commercial installation. It relies heavily on production techniques suitable for the large-scale manufacture of computing and data processing equipment combining transistors, printed circuitry and other forms of miniaturization. Use of these devices makes possible the fast, efficient assembly of modular components that can be used as "building blocks" in future machines.

It operates entirely on transistors—without the use of a single vacuum tube. Magnetic cores make up the machine's internal storage.

In the new calculator, a one-half reduction in computer-unit size and a 90% reduction in power requirements over a comparable vacuum tube model have been achieved.

More than 3,000 transistors are used in the 608. The "power" transistor, the 150x4, is a result of intensive reserach and development activity of the IBM Laboratories.

The capacity and speed of the 608 will enable it to tackle problems of greater size and complexity than those now handled by the IBM Types 604 and 607 Calculators.

"Pluggable" Components are mounted, along with related circuitry, on about 700 printed, wiring panels. These printed circuits are well adapted to the fast, automatic production techniques that have been set up by IBM to increase uniformity and quality.

The machine can perform 4,500 additions a second, a computing speed two and one-half times faster than IBM's Type 607 calculator. It can multiply two 9-digit numbers and come up with the 18-digit product in eleven milliseconds. It can divide an 18-digit number by a 9-digit number and produce the 9-digit quotient in just thirteen milliseconds. The calculating punch unit, used for both input and output, is designed to permit a card to be calculated and the results punched while it is passing through the machine at the rate of 155 per minute. This provides 50% greater card output than is now available in a machine such as the 607.

The three-dimensional array of magnetic cores in the "memory" section of the 608 provides more than twice the storage capacity of its predecessor.

Programming is handled by a flexibly wired control panel similar to those found in IBM machines currently in use. Up to eighty program steps form the basis of the machine's "logical" ability. The non-sequential arrangement of the steps allows the programmer to initiate or skip individual steps by simple control panel wiring. The program steps are supplemented by electronic selectors, coincidence switches and various test impulses that provide the programme with the tools for setting up machine logic directly on the control panel. External manual and visual controls permit the operator to test complicated calculating routines before proceeding with a problem.

THE INSTITUTE FOR ADVANCED STUDY

Electronic Computer Project

The mixing problem mentioned in an earlier report is now on the machine and is being "debugged". As an integral test calculation the well-known case of the lighter fluid on the heavier one is being undertaken at the present time. At the same time an attack has been made on the problem by analytical methods. It will be recalled that in the stable case in which the upper fluid is the lighter, the motion could be adequately represented by an approximate perturbation velocity potential which linearized the problem. This has no validity in the unstable case since the basic assumption of small velocities and displacements no longer holds.

The basic idea of the new approach to the problem of tne unstable case is to expand potentials, interface displacements, and all other relevant quantities as series of powers of the initial perturbation velocity at the interface. The calculation of the successive coefficients is rather complicated and so far has been carried only up to terms of the fourth order. The general character of the motion agrees with experiment as well as with other approximate theories.

As was mentioned previously a large—12,000 word—drum is on order to replace the present one. Virtually all the design considerations have been completed and a buffering register and major control components have been constructed. Other chasses in the unit are now being wired.

The tubes in the machine now have been in operation more than 15,000 hours. Random tests on some of them indicated the need for extensive tube replacement. In general, the main reason for this replacement was excessive interelectrode leakage, in particular heater-cathode leakage.

Work continues on higher speed arithmetic components. An extensive program on the possible use of large cathode tubes for restricted read-around, high density storage has been completed and has been written up for publication.

LIBRASCOPE COMPUTER

Librascope, Incorporated has under development a low-cost electronic, General-Purpose Digital Computer. The logical organization is based on work done by Dr. Stanley P. Frankel in the design of the "MINAC" Computer. Design aims are to handle large scale scientific and engineering calculations at medium speed, consistent with structural simplicity and a minimum number of components. The computer is a serial, one address, fixed binary point, stored program, magnetic drum machine.

While the command structure is relatively simple, having only 16 orders, the computer is fully automatic, executing internally stored programs capable of branching and self modification. Internal operations are in the binary system and word length is 30 bits plus a sign digit.

The magnetic drum has a capacity of 4096 words (numbers or instructions) organized into 64 channels of 64 words each. At a drum speed of 3500 R.P.M., maximum and average random access times are 17 and 8.5 milliseconds respectively. However, a system of optimum access programming is relatively easy to use, which reduces total search time per operation to two milliseconds.

The input-output system consists of a Flexowriter with paper tape punch and reader. Normal input is through the tape reader; however, the keyboard may be used as desired. Data are entered in hexadecimal or binary coded decimal form. In the latter case, as well as for output, the number base conversion is done by a programmed subroutine, permitting great flexibility for special applications. The format is coded and the computer has full control of all Flexowriter functions including the tape punch and reader.

A single address order structure is employed wherein the accumulator register supplies one operand and holds the result for all arithmetic operations.

There are six orders of arithmetic character; these are addition, subtraction, integral and fractional multiplication and extraction (selective erasure). Multiplication and division take one drum revolution (17 msec) for execution; all others one word time (0.26 msec).

A blocked state is entered by the computer after a spillover in addition, subtraction or division, or, if the "one-operation" mode is selected, after each operation. The break point order may put the computer in the blocked state dependent upon a six-bit code and settings of six corresponding switches, thus establishing a hierarchy of break point instructions. From the blocked state the computer may be filled manually, for example, with a program alteration or output subroutine.

Four orders are associated with program sequence control. The control transfer order and return address order facilitate the insertion of subroutines in the main computation scheme. The store address order permits alteration of address portions of instructions, for instance, within subroutines. Decision or branching is possible with the test (conditional control transfer) order wherein the sign of the accumulator content is tested. Two orders are available to record words from the accululator register into the main memory, one clearing the accumulator to zero. The three remaining orders are "bring" (clear and add), "input" and "output."

The entire computer contains approximately 100 tubes and 1200 germanium diodes. All circuits are conservatively designed and are conveniently packaged in plug-in units for ease of maintenance. The cabinet volume is about ten cubic feet and power required is less than 1500 watts from a 115-volt, 60-cycle, single-phase supply.

General Specifications

Number Base	2
Word Length	30 bits plus a sign digit
Number Range	-1 to +1
Negative No. Rep.	Complement
Mode of Operation	Serial
Storage	Magnetic Drum
Storage Capacity	4096 words
Clock Frequency	120 K. C.
Total Access Time	2 m.s. minimum 17 m.s. maximum
Transfer Time	1 m.s. minimum 17 m.s. maximum
Addition Time	.26 m.s. (excluding access time)
Multiplication Time	17 m.s. (excluding access time)
Division Time	17 m.s. (excluding access time)

NAREC

The Naval Research Laboratory's electronic digital computer has been operating since December 1952 with a 1536-word magnetic drum storage and since November 1954 with a 1024-word electrostatic storage. Since May 1953, half of the time has been devoted to engineering and development with the remaining time being made available for scheduled computational purposes. The development work is now expected to be completed by July 1956.

The most notable recent progress has been in the improved operation of the electrostatic storage. This system makes use of three standard three-inch cathode-ray tubes (3RP1) for each binary-digit position. Thus there are 45 chassis of three cathode-ray tubes each to store 1024 45-binary-digit words. This design was expected to reduce cathode-ray-tube replacement costs, and to improve read-around ratio and reliability by reducing the effect of storage surface blemishes. Recent experience has indicated that the results are as anticipated. Individual cathode-ray tubes within a group of the three tubes in a unit have become inoperative (such as filament burn-out) and the unit did not lose its data. When operating with electrostatic storage, there is at present a 10-usec action period followed by a 10-usec forced regeneration period. A test program for checking computer operation indicated that the machine performed more than 9,000 single-address orders per second.

Input has been provided in the form of a Ferranti photo-electric tape reader and the output consists of a Flexowriter, or high-speed punch (60 characters/sec). In July 1955, it is planned that the present 1536-word drum storage will be replaced by a 8192-word drum storage system.

NATIONAL BUREAU OF STANDARDS

Technical Advisory Committee for Mathematics

In its report of October 15, 1953 the Ad Hoc Committee, composed of representatives of professional scientific and engineering societies under the chairmanship of M. J. Kelly, appointed by Secretary Weeks to review the activities of the National Bureau of Standards, recommended the formation of a set of Technical Advisory Committees to advise the director of the Bureau of Standards and his staff on matters which the committees and the staff of the Bureau consider of importance. In accordance with this report known as the Kelly report, the Policy Committee of the Mathematical Societies of America, which was represented on the original Kelly Committee, nominated members for a Technical Advisory Committee for the Applied Mathematics Division of the National Bureau of Standards.

At present this committee consists of David Blackwell of Howard University, E. U. Condon, consulting physicist, Mark Kac of Cornell University, P.M. Morse of Massachusetts Institute of Technology, Mina Rees of Hunter College (Chairman) and A. H. Taub of the University of Illinois.

In meetings held on October 23, 1954 and on February 3, 1955, the Advisory Committee reviewed the program of the four sections of the Applied Mathematics Division, namely the Numerical Analysis Section, the Computation Laboratory, the Statistical Engineering Laboratory and the Mathematical Physics Section. At both meetings the needs for new computing equipment and methods for financing the acquisition of such equipment were discussed.

At the request of the Committee, the Applied Mathematics Division conducted a Bureau-wide survey in order to analyze the needs of NBS in the field of high-speed computation. This survey revealed that many important problems in various scientific and engineering areas require computation facilities not only in excess of the Bureau's existing machines but even many times more powerful than any existing machine. Accordingly, a preliminary systems study was carried out and tentative plans were devised for a powerful computer which could be realized physically by existing NBS computer circuitry and components. The proposed machine will be from 50 to 500 times faster than SEAC in solving a large class of scientific problems and thus would be capable of satisfying the advanced computational requirements of NBS.

The proposed general-purpose computer, the system plans for which were formulated by A. L. Leiner, W. A. Notz, J. L. Smith, and A. Weinberger of NBS, will have an all-parallel logical organization capable of being constructed from a slightly modified version of the time-tested circuitry used in SEAC and DYSEAC. Without increasing the pulse repetition frequency of 1 Mc/sec. used in the two earlier computers, an increase in speed of a factor of 100 can be achieved. The new computer will operate with 53-digit numbers in the binary system.

The arithmetic unit features a 53-stage adder with novel carry generating circuits in which the basic addition cycle for a complete word will be 1 microsecond. Multiplication is to be performed by repeated additions and subtractions, and the shifting will be arranged to skip over one, two, or three 0's or 1's in the permitted instances. Included will be instructions for both fixed-point and floating-point numbers.

The effective utilization of such an arithmetic unit depends on using a memory with a very short random-access time—of the order of 1 microsecond. The NBS diode-capacitor memory developed by A. W. Holt can be operated at these speeds. Such a fast memory would be backed up by a much larger but slower magnetic-core memory.

Average fixed-point operation times for the 3-address mode will be 8-1/2 microseconds for addition and 29 microseconds for multiplication, while average 3-address floating-point operation times will be 16 microseconds for addition and 25 microseconds for multiplication. Accumulations can be performed in an average time of 2 microseconds per word.

Two concurrent input-output trunks are to be provided, each of which could communicate with many different input-output units. Computations can proceed while either or both of the input-output trunks are in use, and automatic interlocks would prevent any logically inconsistent use of the memory for arithmetic references or input-output references. Extensions and modifications of the special supervisory control facilities incorporated in the DYSEAC system are also to be provided.

These preliminary specifications for the new NBS machine were presented to the Mathematical Technical Advisory Committee on April 30, 1955.

NAVAL PROVING GROUND CALCULATORS

Reassembly of the Naval Ordnance Research Calculator (NORC) at the Naval Proving Ground is essentially complete except for the checking out period.

A compiling routine for the automatic assembly of NORC programs was published in Naval Proving Ground Report No. 1374.

The Aiken Dahlgren Electronic Calculator (ADEC) continued on a three-shift operation while the Aiken Relay Calculator (ARDC) operated on one shift. A card-to-tape-to-card converter for ADEC which was built by the Technitrol Engineering Company has recently passed its acceptance tests and will be shipped to the Naval Proving Ground.

UNIVAC II

The new UNIVAC II magnetic core electronic computer, with double the speed and capacity of UNIVAC I has been announced by Remington Rand Inc.

Two major equipment improvements are involved. These are: (1) the replacement of the present 1000-word mercury delay line internal memory with a 2000-word magnetic core memory, and (2) increasing the input-output tape read and write speed to 20,000 characters per second. Present 60-word input-output buffers will be replaced with equivalent magnetic core buffers.

Other system improvements include installation of high-speed magnetic clutches in the Uniservo Units, thus reducing tape start-stop time to 15 ms. Present input-output synchronizers (SYI and SYO) are replaced by an Input Character Distributor and an Output Character Distributer capable of 40,000 character per second operating speed—double that required to accommodate the new 20,000 character per second tape read-write speed.

Design of the new 2000-word magnetic core internal memory and associated address decoding is such that it will accommodate up to four additional 2000-word memory units for a maximum of 10,000 words of high speed internal memory.

Present ten-word transfer instructions (Y and Z) are replaced with one-to-ten word transfer instructions, and the present Extract Function is extended to cover word transfers into and out of memory, thus achieving the equivalent of individual addressable characters. Contributing to the better than two-to-one internal computer speed-up is the elimination of the alpha-time portion of computer operation cycle.

An additional advantage achieved with the higher recording density (200 characters per inch) is the increase in information capacity of a reel of Univac tape to approximately 3,000,000 characters.

Below is given a comparison of UNIVAC I and the new UNIVAC II.

UNIVAC System Comparisons

Operating Area	UNIVAC I	UNIVAC II
1. CENTRAL COMPUTER		
(1) Memory	1,000 words of 12 characters each (alpha numeric)—12,000 character capacity. Mercury delay—line storage system.	2,000 words of 12 characters each (alpha numeric)—24,000 character capacity. Additional 2,000 word increments of memory up to 10,000 words, (120,000 characters) may be added. Magnetic core storage system.
(2) Instructions		All instructions now in UNIVAC I, plus:
	Extract order—transfers predetermined pattern of digits from memory to arithmetic unit.	Field selector—all instructions referring to memory operate under control of extract pattern.
	One, two and ten word transfers.	One to 10 word transfer order.
(3) Time	Transfer to registers, 425 micro-seconds. Addition, 525 microseconds.	Transfers to registers, 120 micro-seconds. Addition, 200 microseconds.
(4) Control	Four-stage cycle of operation.	Three stage cycle of operation.
2. TAPE UNITS (Metal)		
(1) Capacity	1,440,000 digits per 1,500 foot reel.	3,000,000 digits per 1,500 foot reel.
(2) Number of tape control units (Uniservos)	10	10 (more under consideration)
(3) Length of tape	1,500 feet	1,500 feet
(4) Density	128 characters per inch	200 characters per inch
(5) Speed	100 inches of tape read in and out per second or 12,800 characters per second.	100 inches of tape per second or 20,000 characters per second.
(6) Start and Stop time for tape feeding.	45 Milliseconds.	15 Milliseconds.
(7) Space between each block of 60 words.	2.4 inches	1 inch
(8) Time to read one block of 60 words.	100-104 milliseconds (200 instructions)	45-50 milliseconds (300 instructions)

Operating Area	UNIVAC I	UNIVAC II
(9) Blocks of 60 words per 1,500 foot reel of tape.	2,000	4,000
(10) Reading time	3-1/2 minutes (2,000 blocks)	3-1/2 minutes (4,000 blocks)

WHIRLWIND I

Applications

During the past three months, the Scientific and Engineering Computation Group, in conjunction with various departments at M.I.T., processed 66 problems for solution on Whirlwind I. These problems are described in the Project Whirlwind Summary Reports submitted to the Office of Naval Research and cover some 15 different fields of applications. The results of 22 of the problems have been or will be included in academic theses. Of these, 19 represent doctoral theses, two master's and one electrical engineering thesis. Thirty-seven of the problems have originated from research projects sponsored at M.I.T. by the Office of Naval Research.

Even though no major modifications were introduced into the comprehensive system of service routines, the development of new coding techniques by the S & EC Group was extended by the development of translation programs for M.I.T.'s Numerically Controlled Milling Machine. The new coding techniques are also useful to members of the Servomechanisms Laboratory in coding for the UNIVAC Scientific 1103 computer.

Academic

Course 6.535, Introduction to Digital Computer Coding and Logic, a discussion of selected topics in programming, logical design and applications of large scale digital computers, was offered at MIT during the spring of 1955. The course included the solution of a programming problem on a simplified single address computer simulated by Whirlwind I. Among the problems solved by the class members were the solution of simultaneous linear equations, integration of differential equations, and the economization of power series. The total enrollment was 55 seniors and graduate students (from both the engineering and industrial management curricula).

Project Whirlwind staff members have been participating in seminars on machine methods of computation, numerical analysis, and operations research.

Systems

A. Revisions in the Marginal Checking Procedures for the Drum Systems

The programmed-marginal-checking facilities have been expanded to include additional terminal equipment. Previously, this equipment was checked by taking manual margins during specially assigned maintenance periods. The marginal-checking equipment was modified to include the drum equipment in the daily programmed-marginal-checking routines. In the past, check program cycle for this type of terminal equipment has been long compared to the existing voltage variation cycle. It is now possible to select the marginal-checking equipment in a special mode which will hold a preset excursion for an amount of time determined by the program.

A consolidated test program containing nine routines has been written for the drum system. The proper choice of program techniques and assignment of variation lines has reduced the checking time enough to make it practical to include the program as a part of the daily marginal-checking routine. The drum system, containing approximately 5,500 cathodes, is now checked in one half of the hour scheduled for daily system maintenance.

B. Whirlwind Computer Reliability

The following data pertains to the most recent 13 and 33 weeks of operation:

	13 Week Period	33 Week Period
Total Computer operating time	1923 hours	4598 hours
Total lost time	65.2 hours	157.8 hours
Total number of failure incidents	170	410
Average uninterrupted operating time between incidents	10.9 hours	10.8 hours
Average time to locate and repair each failure	23 minutes	23.1 minutes
Percentage operating time usable	96.6%	96.6%

COMPUTERS, OVERSEAS

BESK (SWEDISH BOARD FOR COMPUTING MACHINERY, STOCKHOLM, SWEDEN)

The electronic computer BESK (parallel machine, Williams tube parallel storage, auxiliary magnetic drum storage), designed and built at the Board under Erik Stemme as chief engineer, was taken in use November 5, 1953, and has been in regular operation for problem solving since March 1, 1954. Customers are official, scientific, and military institutions, as well as industry.

"DEUCE" DIGITAL COMPUTER (ENGLISH ELECTRIC COMPANY)

Mode of Operation

The DEUCE operates in the binary notation. Word length is 32 binary digits. The time taken to pass a word from one location to another is known as a 'word time' or 'minor cycle.' A word may represent either an instruction or a number, the number varying in size from 0 up to 2^{31} (about 10^9), even if one digit is regarded as representing the sign.

Storage

The high-speed store of the DEUCE has a capacity of 402 words and is backed by a lower-speed store of capacity of 8,192 words arranged in such a way that it may be considered merely as an extension of the high-speed store.

The high speed store of the DEUCE consists of 12 mercury delay lines, each holding 32 words, and shorter lines, 2 of which hold 4 words, 3 of which hold 2 words and 4 of which are holding single words. The low speed or backing store is a magnetic drum, which has 256 tracks, each holding 32 words, and 16 reading and 16 writing heads. These heads may be moved into any of 16 positions. Transfers of information may take place between the drum and the high-speed store at any time, such transfers involving one track and one delay line at a time. The time required for such a transfer is about 10 milliseconds but if a head shift is involved a further 40 milliseconds may be required. This time is not wasted, however, as computation may proceed in the meantime. Accurate planning can, in many programs, virtually eliminate the time spent on magnetic transfers.

Terminal Equipment

The normal method of transferring information into and out of the DEUCE is by 80-column punched cards. A card reader is supplied which will sense 32 columns of each card at a maximum speed of 200 cards per minute. Instructions may be fed in binary form, while by suitable programs combinations of up to 32 decimal digits may be punched on a card and translated into binary form as the cards are read.

A separate card punch is provided which will punch a set of cards in the corresponding field of 32 columns. The punch will operate at a speed of 100 cards per minute, the cards being punched in sterling, decimal or binary forms.

Control Desk Facilities

The Control Desk of the DEUCE includes facilities to assist in the diagnosis of program and circuit faults.

Two Cathode Ray Tube monitors are provided in order that the contents of any delay line may be seen at will, while the current instruction being obeyed is shown on a row of lights. It is also possible to reduce the rate of program operation to 20 steps per second, or even to one at a time if desired.

Arrangements have been made to punch out each instruction as it is obeyed. The programmer is then free to take away a set of cards and scrutinize them without wasting machine time.

FINAC (INSTITUTO NAZIONALE PER LE APPLICAZIONE DEL CALCOLO, ROME)

The Installation of a Ferranti Mark 1* Computer has been completed. It will be officially named FINAC (Ferranti-Istituto Nazionale Applicazioni Calcolo).

During the first year, it is scheduled for a regular 8-hours-per-day schedule. It will be mainly devoted to partial differential equations, periodogram analysis and inversion of matrices.

The final acceptance test has started on June 20, 1955.

An extra high speed parallel output will be added about January, 1956. It will print 150 lines per minute, 64 characters each row (92 including spaces).

Courses on programming are given at the Institute.

G1 AND G2 (GOETTINGEN, GERMANY)

Up to the present, two computers G1 and G2 (G for Goettingen) have been completed by the "Arbeitsgruppe Numerische Rechenmaschinen" in Goettingen (Germany). Both computers are installed at the Max-Planck-Institut fuer Physik (Prof. Heisenberg) in Goettingen; G1 was set up in September 1952 and G2 in January 1955.

G1 is a small and slow serial computer with a drum memory. It calculates in the binary system and has decimal input and output. The speed is about 3 operations per second. The G1 is controlled directly from 4 selectable punched tapes. To render this kind of control sufficiently flexible, all the contents of each single track on the drum can be shifted cyclically by one word length and also a conditional transfer of the control from one tape to another can be ordered. It is an advantage of this machine that programming is especially simple. It takes only a few hours for a mathematician to learn to run the machine and all students of the Institute are allowed to use the machine during the nighttime without any supervision being necessary. Often it is worth while to program and use the machine for problems that could be calculated on a desk-machine within 2 hours. The machine has 472 tubes and no crystal diodes.

During the last 2 years G1 has run about 21 hours each day. 85% of the scheduled time has been productive.

G2 is a medium speed serial computer with drum memory for 2048 words of 50 binary digits each. It calculates in the binary system with fixed point. Input and output are decimal. Output is by teleprinter, control from the drum memory. 2 orders can be stored in one word length. The speed is about 20 operations/sec. The G2 has 1200 tubes and no crystal diodes.

An I-register enables the user to modify an instruction just before execution by adding the content of the I-register to the address in the instruction without changing the instruction in the memory.

To facilitate the use of subroutines stored on punched tapes in a library, there are built in so called "tape instructions." Tape instructions are special symbols on the punched tape. During the reading in from the tape they call up subroutines that are permanently stored on the drum. 8 different tape instructions permit to add 7 constants or the content of the I-register to the addresses in the orders during the transfer from tape to drum. By this the allocation of the symbolic addresses in the library subroutines to the final addresses on the drum can be performed easily. Another tape instruction permits control of the computer directly from the keys of the teleprinter.

The instruction code consists of 32 instructions. Two of these serve the programming of calculations with floating point: 1) Shift the number in the multiplicand register to the left until the first binary one reaches the position in front of the point and write the number of shifts into the accumulator. 2) Multiply the content of the accumulator by 2^n ($-62 \leq n \leq +62$). For conditional transfer the execution of the next order can be suppressed conditioned by the sign of the number in the accumulator or by the content of the I-register or by the position of 2 manual switches on the control panel or by the reading of a marked number. Such marks for instance can be attached to last numbers of the rows of a matrix or in partial differential equations to the numbers at the boundary. The use of such marks often shortens the program appreciably.

NATIONAL PHYSICAL LABORATORY, CONTROL MECHANISMS AND ELECTRONICS DIVISION

The National Physical Laboratory has recently taken delivery of an English Electric DEUCE, which is now installed and working.

We are now constructing a new machine ACE 2. This is a very fast serial machine using mercury delay line store. It has special facilities for floating point working and for fast binary decimal and decimal binary conversion. It is a 4 address code machine (one is the address of the next instruction) and makes use of optimum coding.

The NPL are designing a machine, the TACT to be constructed by Northampton Polytechnic. This is quite a new type of machine, designed for extreme ease of programming.

The Laboratory, in conjunction with other Government departments, has set up a small team which is investigating the uses of high speed digital computors for clerical work.

T.R.E. COMPUTER, AT R.R.E. MALVERN

The T.R.E. computer has been in use for approximately 12 months to date. During this period, some improvements have been made, particularly in the C.R.T. deflection amplifiers.

Of the total hours during which the computer has been switched on, about 50% have been spent on useful computation, about 25% on development, and the remaining 25% on scheduled daily routine tests and maintenance, and extra unscheduled tests and maintenance.

The computer has been left working unattended for periods of up to 5 hours, then being switched off by a time switch. It is now fitted with a system for shutting down at the end of a problem.

The future program includes such items as the fitting of a large capacity magnetic drum store, a photo-electric tape reader, and, possibly, a higher speed output device.

COMPONENTS

COLEMAN ENGINEERING COMPANY, INC.

Coleman Engineering Company, Inc. now offers a 6-decade analog-to-digital converter, known by the trade-mark "Digitizer," to supplement its standard line of 3, 4 and 5-decade models. The New 6-decade standard version will accumulate a total of one million counts at the rate of 10, 40 or 100 counts per turn of the input shaft. This is the first time that a 6-decade instrument of this type has been available. (See Fig. 2.)

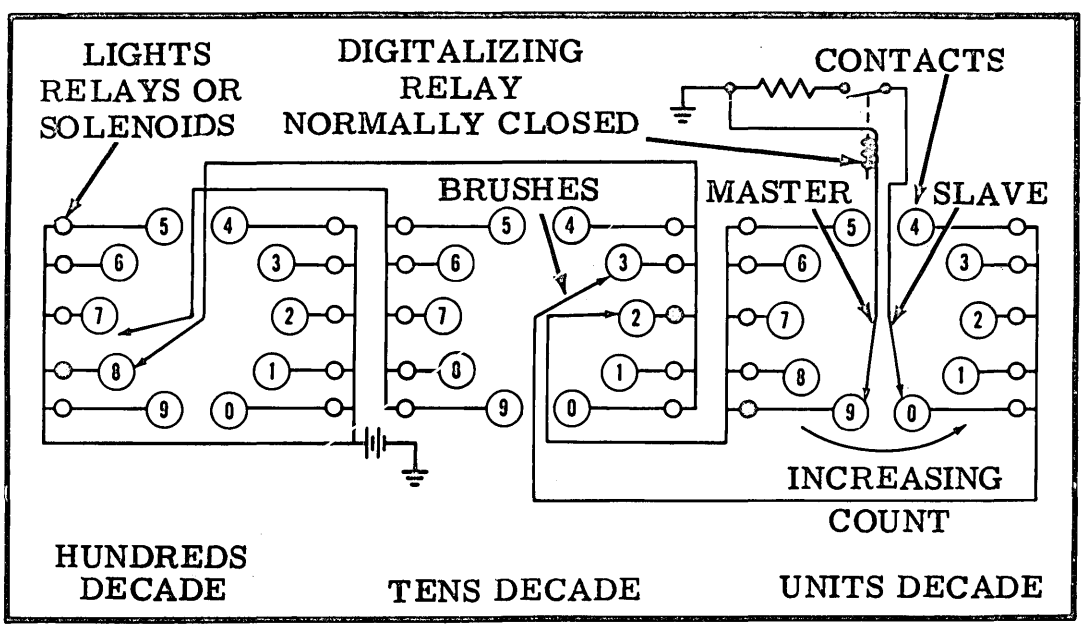

Figure 2 - Coleman Digitizer, schematic

This device is particularly well suited for installation on data reduction equipment, comparators, in automation systems, or to any systems which require a large number of shaft rotations to be expressed digitally.

"Digitizers" convert shaft rotations into discrete electrical contact setting through which various readout devices, such as punched card of perforated tape machines or electric printers can be actuated. This "Digitizer" can be operated for continuous readout with the brushes and contacts engaged or can be used in an "on demand" type readout system to eliminate wear on the brushes and contacts and greatly reduce the torque. With the brushes and contacts retracted during rotation, speeds upwards of 18,000 rpm at the units decade (corresponding to 3,000 digits per second) can be attained.

The torque to start rotation in this condition is less than .01 inch-ounces. The 6-decade "Digitizer" occupies a space approximately 7.4" by 5" by 1-1/8", including contact-retracting solenoids. The weight of the unit is approximately 3 pounds.

To illustrate the simplicity of design and the high degree of ruggedness and reliability, standard gearing is used throughout the "Digitizer." The backlash resulting from wear of these gears contributes in no way to the accuracy of the count, since the count changes at the unit decade and the dual brush system employed in this new "Digitizer" always has one of the two brushes in the proper position to read, regardless of backlash in the system.

IBM - "MAGNETIC DISC" MEMORY

International Business Machines Corporation has announced the development of a "random access" memory device of vast capacity for the storage of information in data processing machines.

The experimental unit, known as the IBM 305, stores 5-million characters, and, when combined in multiple units for use with a single electronic data processing system, will provide an information memory bin of almost unlimited capacity (see Fig. 3). The new equipment will be used with both punched card and magnetic tape-operated machines, and also will be the heart of a new line of IBM electronic data processing machines.

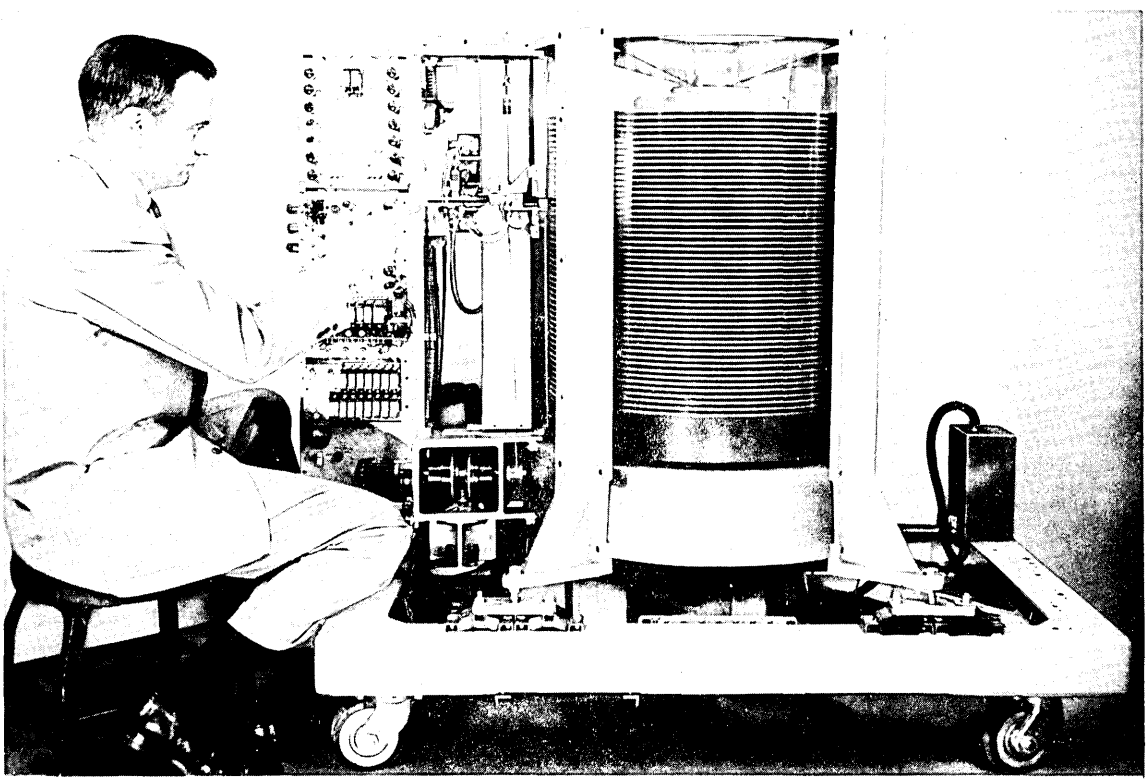

Figure 3 - IBM's new magnetic disc "memory"

The new memory unit is made up of a stack of magnetic discs, mounted on a vertical shaft, and slightly separated from one another. Data is stored as magnetized spots on the discs. At the side of the stack is a reading and writing arm which moves under electronic control directly to the "address" or location of the data desired.

The 305 was developed at IBM's Advanced Engineering Laboratory, San Jose, Calif.

NEW ELECTRODATA CORPORATION COMPONENTS

For use with the Datatron computer, ElectroData Corporation now has available DataReader magnetic tape units and an alphanumeric punch card converter.

Each DataReader holds 400,000 words of ten decimal digits and sign. Under computer control, the unit makes a two-way search for 20-word blocks, reads, or writes at the rate of 28,500 words per minute. It fills the 4000-word drum storage in 8-1/2 seconds. Two read-write heads record at a rate of 100 bits per inch in the non-return to zero system. Two 10-1/2 inch reels handle 2500 feet of tape moving at 60 inches per second and rewinding at 120 inches per second. Special features include self-checking, a preliminary "calibration" operation which rejects defective portions of tape, and vacuum servo control of tape movement.

The new punch card converter, operating on alphanumeric information, reads, punches, or operates line printers at the rate of the punch card machines. Reading speed available is 200 cards per minute, punching speed 100 cards per minute, and printing speed 150 lines per minute. Eight computer words of ten decimal digits and sign are contained on one card or line.

Card reading, punching or printing, and computation go on at the same time.

MEETINGS

INTERNATIONAL CONFERENCE ON ELECTRONIC DIGITAL COMPUTERS AND INFORMATION PROCESSING

An international conference on Electronic digital computers and information processing will be held on 25-27 October, 1955 at the Institut fur Praktische Mathematik (IPM), Technische Hochschule, Darmstadt, Germany.

The Conference is sponsored by the German professional societies in applied Mathematics (GAMM) and in communications engineering, (NTG - VDE).

Discussions will include machine logic and mathematical theory, engineering and development aspects and applications.

Further information on registration, which is open to all, may be obtained from --

Prof. Dr. A. Walther
Institut fur Praktische Mathematik (IPM)
Technische Hochschule
Darmstadt, Germany

INTERNATIONAL MEETING ON ANALOG COMPUTATION IN BRUSSELS

This meeting is being arranged by the Belgian Professional Societies in electrical engineering (SBE), communications engineering (SITEL), and mechanical engineering (SBM). The program contains paper and discussions of various analog methods and their applications to industry and science.

Further information may be obtained from --

P. Germain, Dr. Sc. Math.
Secretary,
Université Libre de Bruxelles
50 Av. Fr. Roosevelt
Brussels, Belgium

WISCONSIN MEETING: THE COMPUTING LABORATORY IN THE UNIVERSITY

The University of Wisconsin is holding a conference entitled "The Computing Laboratory in the University" for a two and one half day period beginning Wednesday morning, August 17, 1955. There will be a few addresses on the computing field in general, several short talks by the ablest users of computing equipment, and several panel discussions concerned with the role of computing in higher educational institutions. The meeting is planned so as to be of interest to administrators and educators in higher educational institutions and to those in governmental agencies and industries who are responsibly concerned with the employment of trained personnel. Inquiries concerning the conference may be addressed to the Director of the Numerical Analysis Laboratory, 206 North Hall, The University of Wisconsin, Madison 6, Wisconsin.

MISCELLANEOUS

COMPUTER SURVEY

The Ballistic Research Laboratories' Computing Laboratory has undertaken to conduct a complete survey of domestic, digital, electronic computing systems, either in current operation or in current or advanced stages of development. It is planned to include in a final report a complete description of digital computing systems, cross-indices on components thereof, glossaries and miscellaneous items pertaining to computing systems.

Government agencies, educational institutions, and manufacturers who own, operate or manufacture digital computing systems and have not been contacted or have not contributed to the survey are requested to contact the Director, Ballistic Research Laboratories, Aberdeen Proving Ground, Maryland, Attn: Mr. M. Weik, Computing Laboratory, for information and questionnaires.

NEW NCR RESEARCH CENTER

A new electronic engineering and research center will be constructed this summer in Hawthorne, Calif., by The National Cash Register Company as part of the Company's overall plan to consolidate and intensify its electronic engineering and research program on the West Coast.

The Company has also organized a special Electronic Applications Group, with headquarters in Dayton, to provide maximum technical assistance to customers and potential customers. This special group will conduct detailed surveys of possible electronic applications and carry out preliminary programming for these applications. It will also give courses in programming for customers' representatives and for other interested parties.

Named to direct the activities of this group of scientistis and technicians is Dr. A. D. Hestenes, who previously held positions with the Franklin Institute and the National Applied Mathematics Laboratories of the National Bureau of Standards.

SECOND ANNUAL ELECTRODATA CORPORATION SCHOLARSHIPS

Five graduate students, one each from Harvard, Louisiana State University, Oklahoma A & M College, the University of Southern California, and Washington University, are spending 10 weeks this summer at ElectroData Corporation's computing center in Pasadena.

Under the direction of Dr. Paul Brock, manager of the technical services department, they will undertake an intensive study program covering logical design and operation of digital

computing equipment, practical numerical analysis, theory of programming and coding, industrial and commercial applications of electronic computers, and the organization and management of a computer manufacturing facility. The students' fields of interest are accounting, economics, chemical engineering, electrical engineering, and mathematics.

ElectroData Corporation has made a $500 grant to each student's university, continuing a program established in the summer of 1954, when two graduate mathematicians from Purdue University spent 10 weeks at ElectroData on similar scholarships.

CONTRIBUTIONS WANTED FOR DIGITAL COMPUTER NEWSLETTER

The Office of Naval Research welcomes contributions to the Digital Computer NEWSLETTER.

The NEWSLETTER is published four times a year on the first of January, April, July and October and material should be in the hands of the editor at least one month before the publication date in order to be included in that issue.

Short technical articles on new machines, on new developments in digital techniques and components, on new types of problems solved and generally news items which may be of potential interest to government users are desired.

The NEWSLETTER is circulated to all interested military and government agencies, and to contractors of the Federal Government. In addition, it is being reprinted in the Journal of the Association for Computing Machinery.

Communications should be addressed to:

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