DIGITAL COMPUTER NEWSLETTER

The purpose of this newsletter is to provide a medium for the interchange among interested persons of information concerning recent developments in various digital computer projects. Distribution is limited to government agencies, contractors, and contributors.

OFFICE OF NAVAL RESEARCH · MATHEMATICAL SCIENCES DIVISION

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SPECIAL NOTICES

NEW CIRCULATION POLICY—DIGITAL COMPUTER NEWSLETTER

The NEWSLETTER IS circulated without charge to interested military and government agencies, and to the contractors of the Federal Government. Also for the many years it had been reprinted by the Association for Computing Machinery within their Journal and more recently in their Communications.

Recently the Association decided that the Communications could better serve its members by concentrating on ACM editorial material. Accordingly, effective with this issue, the NEWSLETTER will be available only by distribution from the Office of Naval Research.

Requests to receive the NEWSLETTER regularly should be submitted to:

Gordon D. Goldstein, Editor
Digital Computer Newsletter
Information Systems Branch
Office of Naval Research
Washington 25, D. C.

Contractors of the Federal Government should reference applicable contracts in their requests.

EDITORIAL POLICY—DIGITAL COMPUTER NEWSLETTER

The NEWSLETTER, although a U. S. Navy Department publication, welcomes contributions from any source. Page limitations do, however, prevent publication of some of the received material. Items which are not printed are kept on file and are made available to interested personnel within the Navy Department, and other government agencies.

Publication of information on commercial products does not—in any way—imply Navy approval of said products; nor does it mean that the Navy vouches for the accuracy of the statements made by the various contributors. Since we do not have space to print all of the worthwhile and newsworthy items, what does appear in each issue should be considered only as being representative of the state-of-the-art and not as the sole product or technique available.

G-20 REVISIONS—COMPUTER DIVISION BENDIX CORPORATION—LOS ANGELES, CALIFORNIA

A 40-percent increase in computing speed has been achieved as a result of experience with G-20 prototype models (see DCN April 1960). The clock frequency has been raised from 700 kilocycles to 1 megacycle and the fixed-point add time revised from 6 to 5 microseconds. Average rate for single word, fixed-point additions is now 83,000 per second, up from 60,000 per second.

Magnetic tape speeds have been doubled. Reading and writing operations are now performed at 120,000 alphanumeric characters per second. Searching is performed at double these speeds. The new fast tape handlers feature complete internal checking facilities and solid-state circuitry.

Printed output for the system will be accomplished with a new series of high-speed line printers. These units will operate at speeds up to 1500 lines per minute on numeric data and 1000 lines per minute on alphabetic data. These previously were 1250 and 600 lines, respectively.

The "organization chart" communications concept featured when the G-20 was introduced has been further refined. Both the accessory control buffers and the magnetic tape control units are now equipped with program controlled electronic switches that can connect them to either of two communication lines. Simultaneous data transfers can be made over multiple communication lines in a flexible and efficient manner.

Core memory for the storage of data and commands in the accessory control buffers has been increased from 1024 to 4096 characters. Facilities have been added for versatile data editing and control of data transfers.

The first G-20 system will be delivered to the Computation Laboratory at Carnegie Institute of Technology.

SWAC—UNIVERSITY OF CALIFORNIA AT LOS ANGELES—LOS ANGELES 24, CALIFORNIA

On September 2, 1959, the transfer of SWAC from its original site to new permanent quarters was begun. The machine had been built "in situ" and its removal entailed considerable disassembly. It was found possible to move the main frame in one piece by removing one wall of the building in which the computer was housed. Almost all of the power wiring had to be replaced. Much of the signal cabling between computer units was re-utilized, and most of the plug and receptacle connections were replaced by solder joints. These pluggable connections also proved satisfactory in subsequent operations.

Power equipment was completely reassembled, and new control cabinets were built. The drum was resurfaced, and new bearings installed, by the original builder, the Librascope Corp., Glendale, Calif. A new console was provided, and the manual controls were rearranged. Power was applied to the computer in its new location about June 1, 1960, and fully "debugged" operation began on August 18, 1960, when the drum retiming was completed.

It was hoped that the core memory could be installed during the move, but unexpected difficulties with the RCA core plate, and the diversion of all hands to the moving project at several critical points, prevented this. Finally, it was decided to abandon the core plates. Eight new core planes, of individually wired cores in a matrix of 48 by 64, have been obtained from RCA. These planes are directly inserted into the circuits of the memory logic, as previously built. They have two additional advantages: (a) the cores are faster by a factor of almost two, and (b) the array consists of 512 words, or twice the capacity of the original assembly.

The work of installing these cores is proceeding as a Senior Engineering project. Alterations in the SWAC logic, making it possible to address the extra words within the four-address structure, have been worked out.

The machine has not been operating long enough for definite figures to be quoted; however, the general impression is that the move has done SWAC no harm, and the move has been a benefit in disclosing many weak spots in the circuitry which have, of course, been repaired. A systematic replacement of the 6AG7 flip-flop tubes with 6197 computer-type pentodes has resulted in a large increase of reliability in the arithmetic section. Aging of the SWAC has resulted in a low but fairly steady failure rate of the pulse transformers, originally built by the National Bureau of Standards Institute for Numerical Analysis. Each failure has been replaced by a modern commercial transformer. Such systematic replacement policies should insure continued successful operation.

MICROCOMPUTER—HUGHES AIRCRAFT COMPANY— CULVER CITY, CALIFORNIA

At the Culver City Research and Development Laboratories of the Hughes Aircraft Company, work is well under way on the fabrication of a demonstration model of the Microcomputer. Completion is anticipated in the first quarter of 1961. This is a DDA computer for use with an inertial platform in ballistic missile applications. It is fabricated by use of thin-film techniques and "dot" components. Supplanting conventional fabrication techniques of phenolic boards with etched circuits and soldered-on components is a basic 3- by 2- by .040-in. fotoceram substrate wafer on which, by means of high vacuum deposition of thin metallic films, binary arrays of passive components (including 50-percent spares) and a universal interconnection method for several circuits are laid down. The specially packaged small "dot" components, diodes, and transistors, are imbedded in the wafer and appropriate component interconnections formed to complete the circuits. In the event of component failure, the circuits are repairable due to the unique Hughes interconnection method.

About 7000 components are required for the DDA computer. These, and the 50-percent spares of resistors and capacitors and a large built-in interconnection flexibility, are fitted into a space of slightly less than 20 cu in. This also includes cooling space and interwafer interconnections within the computer. The component density is well over 2,000,000 per cu ft. Power dissipation is reduced from around 40 w using conventional techniques to just under 10 w in the Microcomputer.

Nichrome resistors used in the computer circuits are currently yielding 3-percent tolerances. They have shown 0.3-percent stability when subjected to temperature changes from that of liquid solder, +225°C to liquid nitrogen - 190°C in less than a minute. After more than 350 hours of operation at 150°C the resistors have tolerance variances of 2 percent, or less. The ruggedness of these tiny circuits hold considerable promise for missile and space applications where small size, low power, and minimum performance degradation in environmental extremes are prime computer requirements.

The flexibility of the circuit fabrication also shows great promise in simplifying the logic design and reducing the programming effort required. Changes in the wired program and supporting logic are possible by severing old circuit interconnections and making new ones. The Hughes computer designers hail this flexibility as a significant step forward in the development of a true off-the-shelf DDA ballistic missile computer. With the appropriate logic/program/circuit changes a single basic computer can be quickly, easily and inexpensively be made to perform in a large number of different ballistic missile applications.

ILLIAC II—UNIVERSITY OF ILLINOIS—URBANA, ILLINOIS

The Digital Computer Laboratory of the University of Illinois has under construction a new computer. The work is being supported by the United States Atomic Energy Commission, the Office of Naval Research, and the University of Illinois.

Some specific details for the computer are:

Word length	52 binary digits
Mantissa	45 bits, including sign
Exponent (base 4)	7 bits
Range of each exponent x	$4^{-64} \leq x < 4^{64}$
Core storage unit capacity	8192 words
Magnetic drum-storage capacity	65,536 words
Fast access storage	10 words
Length of control group	13 bits
Length of short instruction	1 control group
Length of core storage address	1 control group
Length of long instruction	2 control groups

Approximate speeds expected are:

Floating add or subtract	1.5 to 2.5 microseconds*
Multiply	5 to 7 microseconds*
Divide	15 to 20 microseconds*
Core cycle time	1.8 to 2.0 microseconds
Initial access to drum	8.5 milliseconds average 17 microseconds maximum
Drum word rate during block transfer	7 microseconds per word
Block size	256 words

*Arithmetic operation times are initially expected to be 25 percent greater than listed here. After reliable operation is achieved, control modifications to reduce operation times to those listed will be made.

Some of the more unusual features of this high-speed computer, now under construction at the University's Digital Computer Laboratory, are:

1. Nonsaturating circuits using PNP germanium mesa transistors,

2. Use of selectors to control data paths. For example, shifting is achieved by choosing from control one of the signals, x, y, or z with each digit a'_i to be gated selected in accordance with the Boolean equation $a'_i = xa_{i-2} + ya_i + za_{i+2}$.

3. Use of stored carries and base-4 operation for increased arithmetic speed, particularly in multiplication.

4. A speed-independent control, having the property that the output of each logical circuit in the control, can react to an input change after an indefinitely long time without affecting the end result. Such a control will help to ensure correct operation, even when signal transmission times exceed circuit operation times.

5. Floating point operations, with facilities for floating addition of a single precision addend to a double precision augend in the accumulator, yielding a double precision sum in the accumulator.

6. Time-sharing of arithmetic operations with core memory accesses. An advanced control to read operands and instructions into fast access transistor registers in advance is required.

7. A compact order code, including short instructions, in which 4 bits select an index register containing the core memory address. Long instructions, with index registers employed in the conventional way for address modification, may also be used.

The faster portions of the computer are being constructed first. Each chassis used for the arithmetic unit has spaces for approximately 250 transistors; three chassis are used for two

base-4 sections of the arithmetic unit. Layout of each register is in the form of a narrow U, so that short distances between high- and low-order digits can be maintained. Wiring of chassis for the repetitive sections of the arithmetic unit is 70-percent completed. Logical design of the end connections and of the exponent arithmetic unit is virtually complete, with circuit layout underway. Final checks are being made on arithmetic control sequencing charts, and speed-independent controls corresponding to the more frequently used elementary sequences have been designed.

A 3-bit-per-word, 64-word, core memory test unit with dimensions approximating the final unit was constructed during the summer of 1960. Initially, the mean error-free time was approximately 30 minutes. After the addition of metal covers to shield the entire unit from external noise sources, an error-free run in excess of 100 hours has been achieved.

THE AMOS IV COMPUTER—NATIONAL BUREAU OF STANDARDS—WASHINGTON, D. C.

The National Bureau of Standards, in cooperation with the U. S. Weather Bureau, has developed a specialized digital computer for the Weather Bureau to use as a research tool in exploring the concept of the automatic weather station. The AMOS IV computer receives data from weather-sensing instruments and processes these data through such functions as sampling, comparing, selecting a maximum, and arithmetic operations. The results are transmitted via teletype to a central forecasting station and to other airport weather stations. Values of two quantities recently developed as aids to air safety—runway visual range and approach-light contact height— are given by the machine through automatic table look-up.

For a number of years, the Weather Bureau has been appraising the possibilities of an automatic weather station. Such stations could be widely distributed, and would be especially useful in relatively inaccessible locations that are important sources of early data on meteorological activity. The various developmental prototypes of this concept have been called AMOS (Automatic Meteorological Observation Station); the current version, containing transistorized packages, is AMOS IV. It is an outgrowth of previous work done by NBS for the Weather Bureau that resulted in a special computer for processing cloud-height signals from a ceilometer; the ceilometer was intended for use with the AMOS III.

Several of the input quantities to the AMOS computers, such as cloud height and precipitation, cannot be satisfactorily represented by instantaneous values but must be time-averaged. Varying amounts of data processing, therefore, must be associated with the different instruments measuring these quantities.

In the AMOS III concept, several complex units were required for these functions. Although many of the functions were similar, the hardware was not minimized because of a diversity of design that resulted from the isolated development of the individual units. Analysis of the over-all system indicated that a considerable reduction could be made in hardware and therefore in maintenance.

In AMOS IV, the automatic weather station is built around a single, small, general-purpose computer—designed especially for this application. The computer receives data from the input instruments at any desired interval.

These data are suitably processed and arranged in a specified order for teletype transmission in a variety of message formats and at various speeds. The computer also operates local and remote displays. Much latitude is available for research into the most desirable form of data processing because of the inherent flexibility of the internally programmed machine.

The computer continuously monitors new input data, while simultaneously processing data already entered and transmitting messages on command. Among the input quantities which the AMOS IV computer can handle are: temperature, dew point, wind speed and direction, atmospheric pressure, precipitation, transmissivity, and cloud height. Input data can be received directly from the instruments in the simplest possible form—such as analog voltage, current, or resistance; and pulse rate or contact closure. Information may also be received in coded

form— such as the Gray binary code frequently used with shaft-position encoders. The nature of the weather instruments and of the quantities measured limits the input data to 2 or 3 decimal digits for the most part; work size is therefore 3 digits plus sign. Double-precision methods are available for those few instances requiring greater accuracy. Communication with the machine is via electric typewriter or punched tape.

The computer circuitry is based on transistorized plug-in assemblies—designed at NBS for a variety of data-processing applications. These 50-kc packages perform flip-flop, analog switch, and gating circuitry functions, as well as other functions.

To store data, the machine uses a magnetic drum—operating at 1800 rpm—that carries 100 general storage channels of 100 words each, and the machine has space for 100 additional channels. Several dual-head channels are available for simultaneous read-in and read-out of incoming data, outgoing messages, etc. The magnetic drum provides the extensive storage capacity required for the table look-up involved in the calculations of runway visual range and approach light contact height. About 35 tables are stored on the drum; each table has about 90 three-digit values.

One set of these tables contains the data on runway visual range (RVR), i. e., the distance along the runway visible to a pilot from the point of touchdown—generally 1000 to 6500 feet, depending upon runway illumination (natural and artificial) and atmospheric conditions. The primary input for the RVR determination is a transmissometer reading. The computer continuously monitors this reading and "looks up" the proper corresponding value of RVR, which is then displayed locally and inserted into the teletype message.

The other set of tables contains the data on approach light contact height (ALCH), i. e., the height from which the pilot can identify the approach lights. ALCH is affected by background illumination level, atmospheric conditions, and the intensity of the approach lights which are set in accordance with prevailing conditions. If limiting conditions are indicated by either low clouds, as shown by the ceilometer, or by fog or snow, as sensed by the transmissometer, a value of ALCH based on the interfering factor is obtained. If both factors are present, two calculations are made; the machine then determines and displays the lower value. Since there is a statistical uncertainty in this type of information, two values of altitude are presented. The higher altitude is that at which the pilot has a 20-percent probability of seeing the approach lights; the lower altitude is that at which the probability is 90 percent.

TELEFILE —THE TELEREGISTER CORPORATION— STAMFORD, CONNECTICUT

Telefile is the trade name for a new (third generation) data-processing system created by the Teleregister Corporation. The first of four systems was shipped in October and November to its installation site at one of the largest savings banks in the east where this system will handle all of the bank's accounting functions. Two of the remaining systems will also serve banking institutions. The other Telefile, shipped in November, will handle reservations for one of the largest airlines.

The word "system" is appropriate because much more equipment than a single data processor is involved. Although the word "Telefile" is often used in reference to a single processor, it also may apply to a complete system because several processors and many other devices used for storage, data entry, data output, and communications usually are incorporated into a Telefile system and because the word is used in that sense collectively.

The data-processing industry refers to vacuum-tube computers that began with the Univac as first-generation data processors. The second-generation processors include recently introduced transistorized machines; these later machines are generally faster and have more parallel operations than those of the first generation.

The Telefile is transistorized. It belongs in a third generation because of its unique characteristics in comparison with second-generation processors. This chief difference is that Telefile data-processor design is subservient to a basic over-all system design philosophy.

This philosophy stemmed from a need for greater flexibility to obtain optimum combinations of equipment for a given application without closing the system to future expansion. This need has resulted in a modular design with a high degree of flexibility. The inclusion of on-line subsystems among the modules is an important factor controlling design concepts.

On-Line Systems. An on-line data-processing system must receive undisciplined information requests from a large number of sources, sometimes over great distances. It must process the information rapidly and send responses back to the sources very rapidly. "Real-time" is another name given to this type of system. These terms are in opposition to "off-line" processing which usually means the type of batched data handling common to industry.

Computers designed for on-line systems must meet special requirements not often found in commercial data-processing situations. Among these are high reliability, multiple inputs, large random access storage, ability to handle peak loads without wasting computing power. On-line computers must be able to change programs quickly from one type of transaction to another at random and to process off-line during nonpeak hours while handling the remaining on-line work load. They are further required to operate 24 hours per day, 7 days per week, year in and year out. The capability must exist for adding computing power and storage as the loads increase.

Detailed Characteristics.

1. Processor system-subsystem design concept
2. Multiple processors operating in several modes including multiplex, or singly, on-line or off-line, and maintenance
3. All processors capable of sharing on-line load through simultaneous computing in each processor
4. All processors having access to all storage, inputs and outputs at the same time
5. Large random access storage in several hierarchies of size and access time
6. Twenty-nine simultaneous input-output channels with each processor
7. Character addressable storage providing completely variable word length from 1 to 100 digits
8. High system reliability through provisions for multiple processor fallback
9. Computing power for on-line work can be increased or decreased in modules of one processor
10. Ability to handle on-line work with fewer processors during off-peak hours and switch remaining processors over to off-line work
11. Ability to maintain (either emergency or routine) any computer while others are handling the load
12. Ability to add storage or input-output capacity almost without limit, as requirements grow
13. Fast on-line program changes by surging programs into processor core storage from "limitless" drum program storage

Subsystem Design. The most important new characteristic listed above is the first: the processor system-subsystem design concept. Each processor in a Telefile system is a self-contained computer incorporating stored program, digit addressability and variable word-length features. Each processor has up to 29 channels which can be connected to either storage or input-output subsystems.

Each subsystem can operate independently from any of the processors because each is equipped with its own control register and associated logical elements. Subsystems take key instructions from a processor and proceed through a limited sequence of steps under their own control. A priority interrupt feature allows any subsystem, during this sequence, to stall the processor and communicate with it for a single pulse time. During this pulse time, a digit of data can be transferred between the core of the processor and the subsystem.

The technique can be likened to the organization of an office where the manager delegates responsibilities to specialized workers. Work flow is dependent on the manager who issues key instructions on disposition or handling of data and who receives results from the workers capable of performing limited operations. Both manager and processor function in the same manner; both have interruptions to maintain work flow and both handle simultaneous transfers and apply priorities in cases of conflict. Their own specialized work continues at the same time, slowed only by the short intervals required for the actual data transfers.

The subsystems available are: (a) large, medium-speed magnetic drums, (b) smaller, high-speed magnetic drums, (c) magnetic tapes, (d) large-size magnetic core, (e) large-size, medium-speed magnetic discs, (f) medium-size, high-speed magnetic discs, (g) on-line communications subsystems, (h) automatic typewriters, (i) low-speed, punched-tape readers and punches, (j) punched-card input and output, (k) and tab-drive output subsystems.

Modes of Operation. The processor in a system may be operated in any one of several modes under operator control from a master panel associated with each Telefile system. These modes include on-line processing, off-line processing, idling or standby, and maintenance. A simultaneous combination of modes can exist when more than one processor is contained in a system. For distinction, the following terms are used: "simplex mode" for a one-processor system, "duplex mode" for two "triplex mode" for three, and the like.

When two or more processors are used for on-line work in a system, they can be placed in a multiplex mode of operation. Each multiplexed processor is connected through a "seeker" arrangement to the on-line system to allow a nonbusy processor to handle the next transaction which arrives from any of the many on-line input sources. All processors share the same subsystem storages. The working core storage of 10,000 to 15,000 digits, however, is a separate part of each Telefile processor and is not shared. Thus, in this manner, system capabilities multiply almost directly as the number of processors while inputs and storages are shared.

Generally, in off-peak hours, only a single machine is needed to handle on-line loads. The other processors are then available for other work, such as mortgage processing. In this mode, the control panel is set to specify which subsystems are to be associated with each processor.

Programming Features. A completely new philosophy of programming has developed with the Telefile. It centers around on-line requirements, for which many programs required for processing a wide variety of transaction types in a completely random sequence must be brought into play rapidly.

The philosophy is based on large amounts of drum program storage available to be "surged" (a whole program at a time) as required, into the processor core storage. The core really becomes analogous to the operating or working registers in a standard first- or second-generation computer. A control program in the core determines which program is required for the transaction to be processed and causes all pertinent instructions to be surged into the core for execution.

In this technique, individual programs are stored independently. Large, practically unlimited, program storage permits "straight line" programming with no complicated "loops within loops" or other sophisticated methods. The net result is an over-all reduction in programming man-hours of better than 4 to 1. This is obviously an important advantage in large scale applications involving many man-years of programming effort. This facility also allows easy program changes when new routines or programs are added or old ones are replaced.

Programs are made up of any combination of flexible, single-address instructions which may provide for over 230 operations. Each instruction is made up of eight decimal digits: the first two are the order to be performed; the next two specify the length of the field, or the condition of the order; the last four provide the core location. Unless the program logic dictates otherwise, all instructions are executed sequentially.

Single-character core addressability permits efficient utilization of storage as well as flexibility in data handling. A single instruction will operate on data—ranging from 1 to 100 digits in length. Within the limits of practicality, there are no restrictions on the digit length of records, that is, the items of data to be processed. Instructions can be executed at a rate or more than 12,000 per second.

A number of control registers associated with each processor are used in the execution of program instructions. These include the instruction control register, the accumulator control register, the memory operand control register, and the quotient/multiplier control register. These program accessible control registers, effect over-all time savings, and facilitate programming. For example, the accumulator control register enables the program to define an accumulator of any length up to 100 decimal digits, located anywhere in the core memory. The other registers have the same facility.

Off-Line Capabilities. Telefile system design concepts, stemming primarily from special on-line requirements, have produced unusual capabilities for off-line processing. For example, the presence of large, random-access drum storage has provided an ability to sort faster than most magnetic-tape, general-purpose processors.

Large drum storage also allows various processing work to proceed simultaneously with magnetic-tape reading. The number of tape passes in a batch processing application is thus reduced by a significant ratio. Since tapes are, with the present state of the art, the least reliable form of storage, reduction in tape movement is a significant advantage.

Each drum is capable of storing up to 1,050,000 decimal digits. There is almost no limit to the number of such drums in any particular system. The drums, like the core, provide for digit accessibility on a completely random basis. Eight digits provide for the continuous addressing of every character on every drum. Any drum-stored information, from 1 to 10,000 decimal digits long, may be retrieved by a single instruction. This permits complete flexibility in the drum mapping of both data and programs.

The average access time to any unit of drum information is 17 milliseconds. Parallel processing of other information may be carried out in the central processor during this access time. Because of this access and simultaneous computation, the drums may be considered an extension of the core memory for all practical purposes. In this way, the solution of mass inventory-type problems demanding fast access to any record, in combination with the high-speed processing of that record, has been achieved.

Diagnostic Procedures. Reliability was a prime consideration in the design of the system. Checks and safeguards have been built into the circuitry to ensure accurate, dependable data processing. Errors in processing are detected by instructions provided for this purpose. If an error is detected, a branch to a diagnostic program is developed. This diagnostic routine will analyze the error and decide upon the proper procedure to follow. Program interrogated error check points include any malfunction in core memory, arithmetics, and peripheral equipment subsystems.

Central Processor. The processor consists of five standard 19-inch-wide racks of equipment, mounted in a ventilated cabinet. The center rack is a magnetic core memory. The associated logic circuits, arithmetics, registers, etc., are mounted in the two racks on each side of the memory. All circuitry is solid-state modularized on plug-in printed circuit transistor logic cards. A console associated with each processor displays the internal operations as an aid to the maintenance technician, and is used in the test and analysis of programs.

Peripheral Equipment. The Teleregister approach of not limiting the input-output region of the central processor to a single media such as magnetic tapes has led to the utilization of data-storage media of many different characteristics. Although a high-speed magnetic core memory is needed for efficient computation, it is not economically feasible to make available

an extremely large amount of this type of storage. Therefore, a variety of modular peripheral subsystems are tailored to meet the needs of the various system requirements for storage capacity and access time.

The peripheral equipment used in the various system options consists of storage and access devices along with the necessary electronic components to provide interconnection between these equipments and the processor. The following descriptions consider a complete subsystem as consisting of the device, and its associated electronics, as a single functional equipment.

Magnetic-Drum Subsystem. The magnetic-drum subsystem consists of drum units, drum control units, and, if more than one processor is used, a drum central unit. Each drum unit consists of a vertically mounted drum and read-write circuitry housed in a cabinet approximately 3-feet square by 7-feet high. Each magnetic drum has a storage capacity of 1,050,000 decimal digits. Digits are stored in specified locations on drums. Drums revolve at a speed of approximately 1800 rpm. Average access time to any digit of information on drums is 17 milliseconds. Drums, as well as other subsystems, can work in parallel with central processors.

The drum-system control unit consists of rack-mounted transistor logic cards that provide the necessary logic and solid-state switching circuits to automatically connect the proper drum to the processor on demand. If more than one processor is used in the system, a drum central unit is required. The drum central consists of rack-mounted, transistor logic cards; its function is to determine processor access to drum priority and to perform the switching function accordingly.

Magnetic Tapes. A single magnetic-tape subsystem consists of from 1 to 18 tape handlers with their associated electronics connected to the processor through a rack-mounted control unit. Multiple subsystems can be connected to a single processor. Both automatic and manual control of tape handlers is provided. A single magnetic tape provides storage capacity for approximately 4 million decimal digits of information. Each tape is 5/8-inch wide and 2400 feet in length. When running a tape, it passes the read-write head at a speed of 60 inches per second; therefore, 12,000 digits can be read or written per second.

Rewinding of tape occurs at a speed of 120 inches per second. Information on magnetic tape is grouped in blocks consisting of 303 digits. The first 300 digits are for information storage, the last three for end-of-block and parity codes. Each block is 1.5 inches in length with 1/2-inch guard space. When information is required, only a number of blocks forward or a number of blocks back can be addressed. There are approximately 14,400 blocks per tape.

Automatic Typewriters. The automatic typewriter subsystem consists of 1 to 12 Flexowriters connected to the processor through a single rack of electronics. The Flexowriter is the approximate size and appearance of an office typewriter. The electronics rack is a standard, 19-inch-wide rack, containing transistor logic cards mounted in a ventilated cabinet.

The prime function of an automatic typewriter is to enter control information into the system and receive control print outs. Flexoriters operate in two modes, edited and unedited. Edited operation is employed when information is normally entered or retrieved from the processor core-memory. Unedited operation is usually used in maintaining the processors or for anlayzing a program. Information can be entered into core-memory by direct key depression or by reading a punched paper tape via the paper tape read/punch attachment located at the left side of Flexowriters. Outputs from Flexowriters can be typed, punched, or both. Information transfer is at an average speed of 9.5 characters per second.

The typewriter subsystem acts in a completely independent manner. The processor can continue processing while the typewriter is transferring data at its relatively slow rate. The amount of buffering required is negligible because of the character transfer concept. When a character is to be transferred from or to any equipment the transfer takes place on an ask-receive basis. The automatic typewriter can be operated as a standard typewriter for functions as page headings and supplementary notes. When the processor wishes to connect to

the typewriter, the operator is signalled with a flashing light. The typewriter can be released at the convenienced of the operator.

Punched-Card Subsystem. The punched-card subsystem is used with an IBM 514 Reproducing Punch and/or 403, 407, or 408 Tabulator. These machines will be directly connected to the processor by a multiconductor cable. The cable can be disconnected for conventional utilization of these machines whenever necessary. The output from the IBM equipment will be printed reports or punched cards. Tab card information can also be entered into the system through the 514 Reproducing Punch. The reproducer is also used to create punched cards under Telefile control. The punched-card subsystem utilizes a high-speed core storage unit to buffer the information of one card to and from the processor.

Converter. The converter is a special piece of equipment that allows the following conversions of input-output media:

Input	Output
Paper Tape	Magnetic Tape
Punched Card (514)	Magnetic Tape
Magnetic Tape	Punched Card (514)
Magnetic Tape	Printer (403, 407, 408)

The equipment consists of translating and speed conversion units to enable the conversions. Monitoring and parity checks are carried throughout the equipment.

The magnetic-tape handler, punched-card equipment, and paper tape readers, are those used in the Telefile system and are interchangeable with the units directly connected to the data processor.

Local and Remote Input/Output Equipment. Present Telefile systems will incorporate specifically designed counter top keysets with self contained printers, with which the users' personnel can draw out information from the processors, and can update that information when necessary.

These devices may be located on the same premises with the processors or may be at any distance (one block to thousands of miles) and still operate on-line. This is accomplished over a private line network. Response time is 1 second on a trunk circuit, and around 4 seconds on tributary lines. Regular teletype machines operating over existing lines may be used instead of or in place of the special equipment.

Communications Equipment. When input/output equipment is installed in locations distant from the processor, special transmission equipment is located in the lines to relay the data messages to and from the processor.

Elaborate networks can be assembled to meet individual needs using a complete line of special purpose data transmission and switching equipment. Based on traffic load, required response time and over-all circuit economy 1000 bit/second trunks can be interconnected with slow speed tributary lines (75 bit/second) by means of switching and buffering equipments. Individual high- or low-speed lines are arranged for multistation operation; automatic switching is available to provide alternate routing fallback in the event of line or equipment failure. A network using all of these features is now being installed to serve one of the largest airlines.

COMPUTING CENTERS

ELECTRONIC DATA PROCESSING LABORATORY—THE AMERICAN UNIVERSITY—WASHINGTON 6, D. C.

The American University has opened its Electronic Data-Processing Laboratory at 1901 F Street, N.W. Administratively it is a part of the Center for Technology and Administration,

School of Government and Public Administration. At present the laboratory has in operation a Royal McBee RPC-9000 and a Librascope LGP-30. A Royal McBee RPC-4000 is to be added in the future.

The laboratory was established to:

1. Prepare and teach programming, systems, and executive orientation classes for Royal McBee Corporation.

2. Assist faculty and students in research on computer applications for government and business.

3. Give periodic seminars in ADPS, machine indexing, and research administration.

4. Conduct research in machine applications.

UNIVAC LARC—UNIVERSITY OF CALIFORNIA—BERKELEY, CALIFORNIA

Acceptance of the UNIVAC LARC* (see DCN October 1956 for preliminary data), the fastest and most advanced computer system in operation anywhere, was announced October 6, 1960, at the University of California's Lawrence Radiation Laboratory, Livermore, California. The Laboratory is operated for the U. S. Atomic Energy Commission by the University.

The LARC (Livermore Advanced Research Computer), which is many times faster than any existing computer system, was designed and built in Philadelphia by Remington Rand Univac, a division of the Sperry Rand Corporation, under contract with the Lawrence Radiation Laboratory.

The idea for the LARC originated in 1954, when Livermore scientists decided they wished to attack problems that were too large and too time-consuming for any existing computer system. The huge solid-state electronic digital computer which took 5 years to design and build will be used in a variety of AEC-supported research projects to solve problems of almost unbelievable complexity—problems that were unapproachable with existing computer systems.

Almost all the LARC's efforts will be devoted to nuclear weapons projects and fundamental studies of problems in nuclear physics of direct or potential application to the nation's weapons program. Among the more interesting projects which can be discussed is one involving the behavior of neutrons in reactors and nuclear weapons. Here, the LARC scientists will use the Monte Carlo technique to determine the behavior of large numbers of individual neutrons under a given set of circumstances.

For any specific problem, there are only certain things that can happen to a neutron. For instance, it may or may not strike a nucleus; it if does, it may combine with the nucleus, bounce off the nucleus, combine temporarily, and then be re-released, or cause the nucleus to fission. To decide which of these events will occur to an individual neutron, the LARC will perform operations that are similar to spinning a roulette wheel. The computer will generate a series of random numbers, each one of which is associated with one of the possible events. How many random numbers are associated with a specific event depends upon the probability of its happening. The computer will arbitrarily select a random number to determine the behavior of each individual neutron.

To apply this technique to a real problem, it is necessary for the LARC to follow the behavior of thousands of neutrons simultaneously. Final results will tell scientists, with a high degree of reliability, exactly what conditions are necessary for a nuclear device to explode or for a nuclear reactor to go critical.

Another important problem to be analyzed on the LARC is one advanced by Dr. Edward Teller, associate director of the Lawrence Radiation Laboratory. The physicist will provide

*For additional LARC information see the David Taylor Model Basin news item.

the LARC with the basic set of equations which according to work by Balacz Rozsnyai, represents the structure and properties of the atomic nucleus. Dr. Teller expects that it will be possible with the aid of the LARC to predict stability, charge distribution, and quadripole moments of nuclei. One of the many possible benefits to be reaped is a more fundamental understanding of how the process of nuclear fission takes place.

As time permits, other interesting problems will be attacked by the LARC. One of these involves the development of a system of weather prediction. Use of the computer would make it possible to treat the Earth's atmosphere as five separate layers, with simultaneous interaction between layers going on continuously. Data drawn from weather stations throughout the nation on wind velocity, temperature, pressure, and humidity could be recorded on magnetic tapes and fed into the LARC. From its computations, the LARC would then draw a weather map for each atmospheric layer. Such weather maps would be expected to provide a degree of reliability in weather prediction never before realized.

Also under consideration is the use of the LARC in an attempt to solve the famous many-body problem of astronomy. The problem—which has been studied by practically all of the great mathematicians of the past three centuries—concerns three or more astronomical bodies, each exerting a gravitational attraction upon the others. A general solution to the problem would enable scientists to predict the positions and motions of the bodies as a result of forces interacting between them.

LARC actually consists of two interconnected computers, one of which takes instructions from the other. The system is almost completely transistorized, containing some 80,000 transistors and 600 vacuum tubes in the computers and the input-output devices. Its high-speed magnetic core memory will store up to 97,500 words, or 11-digit numbers, while an additional 6 million words may be stored on high-speed drums.

The computer is capable of acting upon 76 different types of instructions. Its mechanical printer will print 720 lines per minute. But for much faster operation, the LARC is equipped to display results on the face of a cathode-ray tube. These results are automatically photographed and developed later. The photographic process will record up to 9,600 lines of output per minute, and can also be used to draw graphs of results, plotting an average of 120,000 points per minute.

A special building has been constructed for the LARC. In addition to the room housing the major units of the computer, the building contains a dust-free room for the magnetic drums, a room for motor generators, power supplies and cooling equipment, and a darkroom where films containing results will be processed.

BASE-LEVEL OPERATIONS SYSTEM—CHARLESTON AFB, SOUTH CAROLINA

A prototype program to cut costs and streamline airlift operations by means of an electronic computer is being conducted by the U. S. Air Force at the Charleston AFB—an aerial port of embarkation for MATS flights to Europe, Africa, and the Middle East, and one of the first USAF bases to have its own computer. The program which utilizes an IBM 7070 seeks to determine whether or not centralized computer systems can be operated economically at base level throughout the Air Force.

The computer processes data for a wide variety of base functions, including an up-to-the-minute supply inventory system, aircraft maintenance control, installation engineering, air operations planning, personnel accounting, and accounting finance operations. One of the most complex jobs assigned to the computer is the inventory control program. Details of more than 40,000 supply items have been stored in two large disk files. The supply program, which involves 85,000 separate instructions to the computer, is one of the largest single programs ever written for a business-type computer.

There is a remote inquiry station located in the base warehouse, a quarter of a mile away. Whenever items are requested, a punch card is punched and inserted into the remote inquiry unit. The computer then checks the inventory, withdraws a record of the items, updates the

balance, charges the proper account, and also prints out appropriate issue slips on an electric typewriter at the inquiry station. It has been estimated that more than 50,000 similar transactions are made each month at the base. When an item reaches a specified low level, the machine will refuse to authorize the issue, unless given a special priority number.

The system also has been programmed to handle security-classified materials. A special code, known only to those personnel who are responsible for the information, must be keyed into the machine along with other data. When this special code is not used, the machine prints a reject notice which informs the operator that the requested information is not authorized.

The computer will process daily records on aircraft maintenance—preparing reports on labor-and-material distribution, status of production, and other cost items for a work force of 1800 maintenance personnel. Such data will permit maintenance managers to recommend improvements in aircraft design.

Maintenance data will be incorporated into air-operations applications, thus providing current status of all aircraft at home and away. The computer will also be used to assist in scheduling aircraft, crews, passenger loads, and cargo-carrying capabilities on a day-to-day basis. Approximately 70 aircraft compose the MATS Wing at Charleston. The Wing aircraft transport nearly 8000 military passengers and 900 tons of cargo monthly between Charleston and U. S. military installations in Europe, Africa, Saudi Arabia, and the Caribbean area. Included in the Wing mission is the airlift support of the down-range missile tracking sites, extending from Cape Canaveral, Fla., to Ascension Island in the South Atlantic.

MANIAC III—UNIVERSITY OF CHICAGO, INSTITUTE FOR COMPUTER RESEARCH—CHICAGO, ILLINOIS

Maniac III (see DCN July 1960) has logged more than 400 hours of testing, during which its arithmetic and logical and indexing instructions have been checked as they have been installed. In addition, it has been used to test the individual planes of its core memory, prior to assembly. The programs for these tests were stored in the eight transistor storage registers which are associated with the computer. With the core plane testing completed, half of the core assembly has been installed in the computer and the memory is now in service for the remainder of testing, with 4000 words of storage available.

Testing time is now being shared with the programming staff which is doing the initial checking of the assembly program. Installation of the magnetic tape and high-speed printer control is in process.

LARC DELIVERY—DAVID TAYLOR MODEL BASIN—WASHINGTON, D. C.

The LARC Computer System* was delivered to the Applied Mathematics Laboratory of the David Taylor Model Basin (DTMB) on 28 October 1960 by the Remington Rand Univac Division of Sperry Rand Corporation, and it has been operated by the Navy since February 1961.

The configuration of the DTMB LARC System is as follows:

Computing Unit (C. U.)
Input-Output Processor (I. L. P.)
4 Read-Write, Magnetic-Tape Synchronizers
2 Read Drum Synchronizers
1 Write Drum Synchronizer
3 million 12-digit-word Drum Memory
Operator's Console
600-line-per-minute, On-Line Printer

The LARC is a multicomputer system (see DCN January 1958). Two main computers, the C. U. and the I. O. P., operate simultaneously, cooperating on the solution of a problem, and each is controlled by its own program written in its own language.

*For additional LARC information see University of California news item.

As much equipment as possible is operated simultaneously for speed and economy. All the peripheral equipment is controlled by synchronizers which permit two drums to be read, one to be written, four tapes to be read or written, and the On-Line-Printer to print, while the Input-Output Processor is carrying on some subsidiary program, such as editing and the Computing Unit is performing high-speed arithmetic operations without interruption.

The high-speed computational abilities are further exploited by having the C. U. process parts of five sequential instructions at once, and making each 2500-Word Memory unit independently accessible. Every instruction is automatically index-register or B-box modified; single (11-decimal digit) and double (22-decimal digit) precision as well as fixed-point and floating-point arithmetic are available.

Reliability is built into the system through extensive checking features; both the odd-even parity and complementary logic are extensively employed. The individual circuits are combined on 10,000 pluggable printed-circuit cards for ease of maintenance.

The performance test, devised by the Navy, was scheduled to run 3 days, 7 hours, and 20 minutes daily, with downtime limited to 45 minutes per day. To meet the performance test, the LARC on the third day processed 8 billion bits of information from the tape systems alone with no downtime in the 7-hour and 20-minute alloted time period to achieve a performance of one error per 1 billion bits of information. This involved 16 Uniservos with five of the 16 operating simultaneously.

Using 12 drums, a basic part of the system with three out of every 12 reading and writing continuously and simultaneously, the LARC processed 32 billion bits of information during the 7-hour and 20-minute period for a performance of one error in three billion bits of information. The 7-hour and 20-minute daily running time was established by setting test units for periods of 10-minute duration, 44 units to a day. Downtime, in this frame of reference, results from occurrence of an error necessitating a re-run of the 10-minute period.

LARC will be used in carrying out calculations involved in the solution of naval problems in the fields of engineering, research, management data analysis, and operations research.

Mathematicians at DTMB'S Applied Mathematics Laboratory have been utilizing high-speed computer devices for the past 9 years in solving naval engineering problems in the design of nuclear reactors for ships such as NAUTILUS and SEA WOLF; in the calculation of fallout patterns and propeller characteristics; in the analysis of collapse pressures of submarine hulls; in the calculation of phased material requirements in shipbuilding programs; and in many other applications.

Three-dimensional mathematical models of nuclear reactors will be constructed in the LARC which will enable the design engineer to study and compare varying designs in a highly compressed period of time. Other problems being considered for solution on the LARC system include: (a) the development of a digital method for spectrum analysis of ocean wave patterns, and (b) calculations related to the design of large arrays of transducers and the analysis of magnetic fields for minesweeping operations.

HIGH-SPEED INFORMATION RETRIEVAL—U. S. NAVAL ORDNANCE LABORATORY—SILVER SPRING, MARYLAND

Literature searches which have taken several librarians over a week to complete are being accomplished in 15 minutes at the Naval Ordnance Laboratory (NOL) in Silver Spring, Maryland. The system uses an IBM-704 computer and single roll of magnetic computer tape, containing information from thousands of library reference cards. Data on the master tape includes detailed and cross-referenced information on technical reports—representing defense projects in such fields as aeroballistics, chemistry, and physics. The computer scans the master tape at the rate of 1000 reports a second and produces a complete listing of those concerning a specific subject.

The new system represents a considerable savings of money, time, and effort for the Laboratory. Even with the cost of the computer being $300 an hour, the cost per query is calculated to be $1.25, only a quarter as much as that of a manual search.

Made once a day, the high-speed searches have utilized the computer from 5 to 15 minutes for as many as 50 queries.

Reports can be filed on the master tape in any sequence desired. For example, they can be arranged chronologically, listed by accession number, or grouped together according to their security classification. When a high-speed search is necessary, code words describing the desired subject are punched on IBM cards. These cards and a magnetic tape, containing programming instructions, are fed into the computer which searches the master tape for the relevant reports. Within seconds, these reports are recorded on an output tape—which is processed by a printer to produce a complete listing of all the reports on the specific subject.

The key to the tape is a subject code dictionary containing code terms which describe the reports registered on the master memory tape. Each report is represented by a single code group or a combination of these groups. Additional code terms are added to the dictionary from time to time to represent the expanding body of data on the master tape.

NOL's Library, in cooperation with the NOL Mathematics Department, is reasonsible for the operation of the new Information Retrieval System. Coding of new reports for recording on the magnetic tape is done by the Library staff while programming is the responsibility of the Mathematics Department.

COMPUTATION CENTER—U. S. NAVAL WEAPONS LABORATORY—DAHLGREN, VIRGINIA

IBM 7090 Installation. An IBM 7090 computer was installed in September 1960; second-shift operation began in February, and a third shift is planned within several months. An IBM 1401 has been installed as an input-output auxiliary to the 7090.

NORC Alphanumeric Compiler. Acquisition of the 20,000-word memory for the NORC computer made possible the preparation of an alphanumeric compiler which has been completed and used for compiling several major programs. This compiler, described in NWL Technical Memo E-32/59 (Revised), performs the following services: ordering the coding, converting coding to machine language, making up and assembling subroutines, and facilitating segmentation.

Space Surveillance System Commissioning. The U. S. Naval Space Surveillance System (NAVSPASUR) was commissioned on 1 February 1961, in a ceremony held at the U. S. Naval Weapons Laboratory. NAVSPASUR uses the facilities and staff of the Computation Center to process satellite observational data and produce output, such as orbital elements and ephemerides, for the North American Air Defense Command (NORAD). This new operating unit of the Navy, with headquarters located at the U. S. Naval Weapons Laboratory, is under the operational control of NORAD.

COMPUTER SYSTEMS AND APPLICATIONS—U. S. NAVY, BUREAU OF SHIPS—WASHINGTON 25, D. C.

The Bureau of Ships has four contracts for studies to apply the principles of Operations Research to production planning and control problems that require the use of electronic computers in naval shipyards. Mauchly Associates, Inc., Rensselaer Polytechnic Institute, Carnegie Institute of Technology, and M. I. T. are the contractors for this research.

Mauchly Associates, Inc., has successfully completed a feasibility study at Philadelphia Naval Shipyard. The critical Path Scheduling Method which contains many of the features of PERT was used to schedule, by computer, the overhaul of the Entemedor (SS340) in parallel

with conventional scheduling. Results to date have proven the feasibility of utilizing the Critical Path Technique for scheduling shipwork, and have indicated that many important improvements in scheduling and manpower utilization can be obtained.

Pilot projects are planned for utilizing the Critical Path Scheduling Method for computer scheduling of the construction of one ship and of the overhauls of a small group of ships.

WRUSS RETIREMENT—WESTERN RESERVE UNIVERSITY—CLEVELAND, OHIO

The Western Reserve University Searching Selector, a relay logical machine, has been retired from active operational service after having served a very important purppse. The principles and logic for information retrieval have been adequately demonstrated on an operational level. In its retirement the WRUSS will be used by students as an educational and experimental tool.

The Documentation Center is acquiring a GE-225 which is scheduled for installation during February 1961. The GE-225 is a transistorized general-purpose computer with an 18-microsecond access time and a total of 36-microsecond add time. The installation will contain 8192-word core memory and a dual-tape unit. A program to simulate the logic of the WRUSS for information retrieval is in preparation and will be available for use at the time of installation. Because of high-speed capabilities of the computer, the searching time of the operational phase of the Documentation Center will be reduced substantially. As a result, it is hoped that computer time will become available for other educational and research pursuits on the campus.

In the interim, searches are being conducted at G. E. in Phoenix on the NRC 304. This serves a dual purpose: (1) A large-volume search—too time-consuming for the WRUSS—is now being carried out. (2) A great deal is being learned about the simulation of the Searching Selector logic in a general-purpose computer.

COMPUTERS AND CENTERS, OVERSEAS

X1 INPUT-OUTPUT—N. V. ELECTROLOGICA—AMSTERDAM, HOLLAND

The X1 Computer (see DCN April 1959) is now equipped to handle the following input-output equipment:

1. Magnetic Tape—Up to sixteen 1/2-inch tape units, each with a tape speed of 30,000 digits per second.
2. High-Speed Printer—Mechanical type with a speed of 10 lines per minutes, 120 digits per line.
3. High-Speed Tape Punch—300 digits per second.
4. High-Speed Tape Reader—1000 digits per second.

FERRANTI COMPUTER MODELS—FERRANTI, LTD.—LONDON, ENGLAND

Since the Computer Department began just over 10 years ago, 52 machines have been delivered to customers and a further 31 have been ordered. The range includes:

Model	Application	Quantity
Pegasus 1	General-purpose computing system	25
Pegasus 2	A version of above for commercial data processing	12

Model	Application	Quantity
Mercury	High-speed machine mainly for scientific calculations	20
Perseus	Commercial data-processing system	2
Orion	Time-shared transistorized computing system for business or scientific uses	9
Atlas	High-speed transistorized computer	1
Sirius	Small transistorized machine, mainly for engineering calculations	2
Argus	Transistorized process-control computer	2 allocated
Apollo	Special-purpose computer for air-traffic control data processing	1
Mark I and I*	Early design of scientific computer, production discontinued	9

ORION—FERANTI, LTD.—LONDON, ENGLAND

The first machine is scheduled to be completed in early 1961. The Orion price is in the range of £120,000 - £400,000 depending on the peripheral equipment required. The machine is designed to be equally suitable for business and scientific applications. It enables a business to introduce automation of its work by stages, until eventually every aspect of its operations has been brought under an integrated system of control.

The outstanding design features of the computing system are: (a) its time-sharing mode of operations, (b) its reliability, relatively small size and low power consumption resulting from transistor and magnetic-core circuitry, (c) its ability to operate with a wide variety of peripheral units working at different speeds, (d) its avoidance of costly off-line electronic equipment and buffer storage, and (e) its large-capacity, quick-access working store. The description "high speed" is becoming meaningless nowadays, being a purely relative term, but the Orion is certainly fast by any standards (actually about four times as fast as the Mercury machine). Addition and subtraction operations, for example, are performed in about 50 microseconds—about 20,000 operations per second.

From the user's point of view, the Orion has the distinction of being a machine whose design has been guided by users—that is to say, by programming and applications experts rather than by electronics engineers. Naturally, the design of the "hardware" has been done by engineers, but the over-all organization of the machine, the planning of facilities, and the specification of operating requirements have been very much the concern of people who work with computers and are in constant touch with the problems of users. One of the early conclusions reached by the designers in planning the machine was that the requirements of business and scientific users of computers are not so incompatible as is generally thought. As a result, it has been possible to produce a machine equally suitable for business and scientific applications.

Another conclusion reached in the early stages of investigation was that most users need an expandable computing system. It can start as a basic electronic unit with the minimum of input and output equipment, and extra peripheral units can be added as increasing experience and the changing requirements of the user show them to be necessary.

With earlier computer designs, this problem was proving difficult and expensive to solve because it entailed extra electronic circuitry for controlling the additional peripheral units. In fact, it was rapidly being discovered that such auxiliary electronic equipment could become as big and extensive as the central computer itself. With Orion, however, the time-sharing mode of operating enables all the functions of controlling the peripheral units to be handled by

the central computing circuits. The design of the machine is such that the additional circuitry is small and easily incorporated.

Before going into details, it might be well to look at time-sharing in a general way. How does it operate, and what advantages does it offer? One usually says that it enables several computer programmes to be run "simultaneously" or "concurrently." These words are certainly true if one surveys what happens in a time-sharing computer over a period of the order of minutes. But, in fact, the individual mathematical and other operations can only be done on one programme at a time, since there is only one central arithmetic and control section. It is the time of this central section which is shared between the various programmes.

For example, a short sequence of operations might be done on Programme 1, then a short sequence on Programme 2, then perhaps another period on Programme 1, followed by a short sequence on Programme 3. These periods have different durations but are generally in the range of milliseconds to seconds; so that over a longer interval of, say, several minutes, the net effect is that all programmes have progressed simultaneously.

The advantage of time sharing is that it enables more computation to be performed in a given time by a given size of computer, because it ensures more efficient utilization of the actual computing circuits. In conventional computer systems some of the electronic circuits are not utilized to the full but are kept idle for quite lengthy periods. This is because the electronic circuits work very fast in relation to the speed of the electromechanical input and output equipment. A computer programme usually contains two main classes of operations: (a) transfer operations in which data are read from punched cards or tape into a store or written out from the store on to cards or tape and (b) computing operations in which arithmetical processes are performed by electronic circuits on the data in the store. These operations are interspersed according to the sequence laid down in the programme. The process of transferring numbers between the input or output equipment and the store generally takes much longer than the electronic operations performed on the numbers—perhaps 100 to 1000 times longer. As a result, some of the electronic circuits have to wait idle for comparatively long periods between bursts of activity. With the time-sharing technique these long periods are not idle but are filled with activity on other programmes. For example, while input data for Programme 1 is being read in, the computing circuits might be performing on Programme 2 data which has been previously read in and stored. If Programme 2 now calls for input data to be written out and Programme 1 is still reading in data, the computing circuits do not stop working but switch to operations on Programme 3. By the time Programme 3 calls for more data the reading-in or Programme 1 may be complete, so the computing circuits switch back and start performing operations on the Programme 1 data now available.

For this kind of procedure to work efficiently, it is necessary for the computing circuits—when they have to stop for a data transfer in one programme—to be able to start work "immediately" on the stored numbers of another programme. This means that each programme, as well as having its own input and output equipment, must also have its own section of the working store, and the method of storage must give quick access to the data. Furthermore, as the working store must handle not one but several programmes, its capacity must be appropriately large.

In the Orion these demands are met by a magnetic-core working store with a basic capacity of 4096 words, extendable to 32,000 words according to the number and scope of the programmes to be handled. Each computer word contains 48 binary digits, and all of the digits of a word are transferred into or out of the store in parallel in 12 microseconds.

The working store might be split into three independent sections for three different programmes—sorting and selecting data, printing output data, and checking data. The programmer, however, does not have to worry about the allocation of data to particular sections of the store. He only writes down the storage capacity required and the computer automatically reserves the actual storage locations and prints them out on a Flexowriter electric typewriter. This process is done by means of a special store programme. The reserve storage locations belonging to one programme cannot be accidentally used by the machine when working on another programme, because there is an electronic system of safeguards called "lockouts" to prevent this.

The programmer does not have to worry, either, about the actual sequence in which the time of the computing circuits is shared between the various programmes. This sequence is controlled automatically by a special "organization" programme, permanently stored in the machine which works on a system of priorities. Every time the operation of the central computing circuits is held up because a transfer of data has to take place, the organization programme surveys all the stored programmes and decides which one has the highest priority and should be worked on next. The priorities depend on the nature of the programmes and on the associated input and output equipment.

By suitable planning of the organization programme and the system of priorities, it is possible to deploy the facilities of the computer in a very efficient way on widely differing programmes and with widely differing types of input and output equipment. For example, it is possible to run scientific programmes, which tend to make more efficient use of the arithmetic circuits, at the same time as commercial data transcription programmes, which tend to make more efficient use of the peripheral units. High-speed output printers, which cannot be operated intermittently, can be given high priority in relation to other units not restricted in this way.

The advantages of time-sharing to a commercial user are bound up with the use made of peripheral equipments. To the scientific user, whose problems are mainly concerned with computation, the advantages are not so apparent. One of the most important advantages for the scientist, however, is that he can obtain his programme development time "free." Programme development usually involves short runs on the computer with lengthy periods for thought between. By keeping the programme under development permanently in the computer and interrupting the other main programme for a short period every few minutes to work on it, very little computer time is used but a great deal of development time is made available. The system of reservations and lockouts is such that even a completely untested programme can be run quite safely at the same time as a "production" programme without any possible danger of mutual interference.

The normal input units are 80-column, punched-card readers and 7-hole, punched-paper tape readers. For output data, there are corresponding card and tape punches and a high-speed xerographic printer with 240 characters per line. Mechanical output printers and tabulators are also available. Backing-up storage is provided by magnetic drums, each of 16,384-word capacity, while the job of file storage, as required for large batches of commercial data, is done by magnetic-tape stores. The magnetic-tape units operate at the high speed of 90,000 characters per second (continuous recording or reading) and up to four of them can be run simultaneously. This enables updating of files to be done on a daily basis.

Pure binary code is used for the number system within the machine and, as already mentioned, the arithmetic and control operations are performed by transistor and magnetic-core circuits. Each circuit element is called a "neuron"—its functional behaviour being roughly comparable with that of an animal nerve cell. In this mode of operation, the binary output state of a magnetic-core, 0 or 1, at any moment is determined on a statistical basis by the pattern of 0 and 1 input signals. The arithmetic unit built up from these logical elements works in semiparallel—that is, it does not handle all 48 binary digits of a word simultaneously but in two lots of 24 binary digits.

MATHEMATICS SECTION—NORWEGIAN DEFENCE RESEARCH ESTABLISHMENT—LILLESTRØM, NORWAY

The Mathematics Section of the Norwegian Defence Research Establishment, working with a Ferranti Mercury computer, has experienced a rapidly expanding increase in demand for electronic computation during the last year, both from defence and civilian institutions. Consequently, the number of scientists directly or indirectly connected with the computer shows a constantly growing trend. At present there are 10 programmers working with the Section and some 20 more doing regular programming jobs on their own.

The Section is working with several projects in the line of autocode programmes including one complete "Autocode for the Mercury Computer" which in its present state can tackle minor

problems only. It is intended, in its final shape, however, to cover most of the ALGOL language as well as some additional features. Also under development is a matrix interpretative scheme, and under consideration is an extension of the present Input Programme to include macro orders of arbitrary complexity.

The NDRE computer, a prototype Mercury, has shown an undesirably low efficiency for some time mainly because the original magnetic drums were inferior in construction to the later serial numbers. The old drums were replaced by new models in late November, and it is hoped that this will considerably improve operating statistics. Also at the same time, facilities for multichannel input/output were built into the computer.

DATA TRANSMISSION AND TRAFFIC SIMULATION—STANDARD TELECOMMUNICATION LABORATORIES, LTD. —LONDON, ENGLAND

Data Transmission. Data transmitted over ordinary telephone lines (in cooperation with the G. P. O.) are received and compared with a locally delayed version of what was sent. Errors cause an output five-hole paper tape to be punched at, for example, 200 characters per second, together with code symbols that indicate the repetition number of the data responsible for the error.

These tapes are processed by a STANTEC-ZEBRA computer to produce a paper tape of "plain language" statements describing the time of each error in its particular repetition. These paper tapes are again processed to give lists of special cases indicating the number of errors which would have been undetected, if the data transmission had been provided with various parity-error detecting schemes.

The results can be used to indicate a reasonable error-detecting scheme, thereby yielding statistical information about real noise.

Telephone Traffic Simulation. Computer Simulation of traffic flowing in a simplified 10,000 line T. D. M. exchange has shown that the traffic-carrying capacity is 15-percent greater than would be expected from a theoretical formula. This extra efficiency was expected. It is caused by the sequential-hunting rule and by the slight interdependence of the traffic flowing in various parts of the exchange; the formula assumes random hunting and independence of traffic.

The basic problem of hunting through two crossbar switches in series, each with limited availability, has also been successfully simulated. Results are in good agreement with other empirical methods of switch design, given in the standard text books.

COMPONENTS

CHARACTER RECOGNITION—RABINOW ENGINEERING COMPANY—WASHINGTON 12, D. C.

The Rabinow Engineering Company, 7212 New Hampshire Avenue, Washington 12, D. C., has been actively engaged in the character and pattern recognition field since the firm's organization. Although the first such machine was contructed by the company in 1957, Mr. Rabinow conceived and built a character reader in 1951 while at the National Bureau of Standards. This early machine used a mechanical scanning technique which employed a Nipkow disc and an optical mask. A symbol was chosen on the basis of best match—i.e., minimum transmission of light—as detected by a single photomultiplier tube. The machine was relatively slow, since each input character had to be compared against every character on the mask serially. The reader input consisted of numbers and letters of an ordinary commercial typewriter, while the output was a simple visual display.

The company's first machine used the same general principles as the early prototype, i.e., the mechanical scanning, optical-mask technique, but it was capable of a higher speed

of approximately 10 characters per second. This was, in part, due to the use of a split-field optical system in which the image was projected by a precision multifaced mirror to a bank of 16 photomultipliers. In this manner, parallel detection was possible. This device scanned a single printed line along the center of a standard IBM card.

The second machine to be designed was delivered in 1959. This machine was capable of reading 16 characters in a 5 by 7 font, as well as sensing a series of pencil marks recorded on the document by hand. Recognition of characters was accomplished by an electronic map-matching technique in which the output of a bank of photocells is sampled at proper intervals and the results are stored in a flip-flop matrix. These outputs are then compared electrically by a number of symbol detectors with an individual detector for each symbol. This action takes place in parallel, hence is extremely fast. The machine characteristics are as follows:

Input	Single line of typewritten characters plus mark sensing below the typewritten line
Output	Magnetic tape
Document Speed	10 lines per sec (10-inch paper) 18 lines per sec (6-inch paper)
Character Spacing	10 lines per in.

A third character reader, designed in 1959, was delivered to a major industrial customer in 1960. This device is a page reader and uses the combined movement of a rotating drum, which holds the document, and a moving head which carries a bank of 24 photocell detectors to scan each line in succession. A servosystem tracks the typewritten line and keeps the head in optimum position for reading. This machine has the following characteristics:

Input	Typewritten page (10 numbers, 26 letters, and 17 symbols in a 5 by 7 font)
Output	Magnetic tape
Format	20 lines per page; 100 characters per line
Document Speed	4.5 seconds (reading time plus paper handling)
Line Speed	6 lines per second.

A fourth type of reader, experimental in nature, was completed in 1960. This machine reads typewritten material where specially designed cut font characters are employed. A repertoire of 38 numbers, letters, and symbols is used. Only a single line is scanned, using a drum feed and fixed reading head. A scanning rate of 200 characters per second was achieved. Output of the machine was both electrical and visual. This machine was designed particularly with the idea of minimizing the costs of both the mechanical and electronic equipment.

At present the Rabinow Engineering Company is under contract to design and construct a reading machine for the Ryder Truck Lines Inc. This machine will read a line of numeric information off a trucker's waybill. Such information includes waybill number, charges, weight, destination code, etc. Carbon copies as well as originals, are to be read. The line scanned will contain space for a maximum of 80 typewritten characters and it is expected that approximately five documents will be handled per second. An electronic map-matching technique similar to that previously described, will be used, except for a much larger storage matrix. The output of the reader will be recorded on magnetic tape for insertion into a Remington Rand SS-80 computing machine system.

It should be pointed out that although each machine described above was designed for a particular purpose, the parameters of a reading system can cover a wide range. Thus, a variety of different fonts may be employed although those having maximum discrimination are to be preferred. Reading rates up to 2500 characters per second have been achieved. A variety of documents can be handled, from card stock to lightweight paper documents; In fact,

several feeders have been designed to handle multiple sheets of paper forms, glued or stapled. Finally, the outputs of such readers can be made suitable for different kinds of devices such as punched cards, magnetic-tape, or punched-paper tape equipment.

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