Copy _____

HIGH-SPEED BUFFER REGISTER, HSB-N
Technical Manual

PBC 1007

pb Packard Bell Computer

A SUBSIDIARY OF PACKARD BELL ELECTRONICS
1905 ARMACOST AVENUE • LOS ANGELES 25, CALIFORNIA

August 15, 1961

NOTICE

CONTENTS

Section			Page
I.	General		1-1
	A.	Introduction	1-1
	B.	Description	1-1
II.	Theory of Operation		2-1
	A.	General	2-1
	B.	PB 250 Computer Connections	2-1
	C.	Parallel Input and Output	2-3
	D.	Serial Level Input	2-3
	E.	Serial Pulse Input	2-5
	F.	High Speed Buffer (HSB-N) Logic	2-6
	G.	General Purpose Logic	2-7
III.	Maintenance		3-1
	A.	General	3-1
	B.	Installation	3-2
	C.	Troubleshooting Procedure	3-2
	D.	Marginal Checking	3-7

CONTENTS (Continued)

Section		Page
IV.	Parts List	4-1
	Appendices	
	A. Logic Layouts	A-1
	B. HSB-N Test Routine and Program Listing	B-1
	C. Modules Schematics	C-1

FIGURES

		Page
1-1.	High-Speed Buffer Register, HSB-N	1-2
1-2.	General Purpose Logic	1-3
1-3.	HSB-N Block Diagram	1-4
2-1.	Serial Input-Output (PB 250 Connections)	2-2
2-2.	Serial Input (Not PB 250 Connections)	2-4
3-1.	HSB-N Installation Drawing	3-3

TABLES

1-1.	Connectors	1-6
3-1.	Serial Input-Output Cable	3-4
3-2.	Control Pulse Cable	3-5
A-1.	Glossary of Terms	A-1
B-1.	Program Listing	B-3

I. GENERAL

A. INTRODUCTION

Model HSB-N High-Speed Buffer Register, see Figure 1-1, provides intermediate data storage during operation between the PB 250 Computer and asynchronous devices.

The HSB-N is a flip-flop shift register designed to accept parallel or serial information nonsynchronous with the PB 250 clock and transfer it into the PB 250 Computer by means of a block serial input command or to receive information from the PB 250 by means of a block serial output command and store it for transfer to external devices. The unit also contains some general purpose logic, see Figure 1-2, which can be patched for specific applications by two jumper plugs, see Figure 1-3. The HSB-N may be used as a buffer between the PB 250 and a core memory unit; digital to analog or analog to digital converters; or generally with other computers and systems operating at a clock rate different from the PB 250.

B. DESCRIPTION

The HSB-N measures 5-1/4 x 20-1/4 x 19 in. and is packaged in a modified MC-72 module case. The unit is adapted for 19 in. relay rack mounting and weighs 25 pounds. Power is supplied from the PB 250 Computer power supply (+6v, 0.2 amp, -12v, 1.8 amps maximum for 22 stages). The control logic is built up from 20 PBC 35-pin and 15-pin plug-in modules.

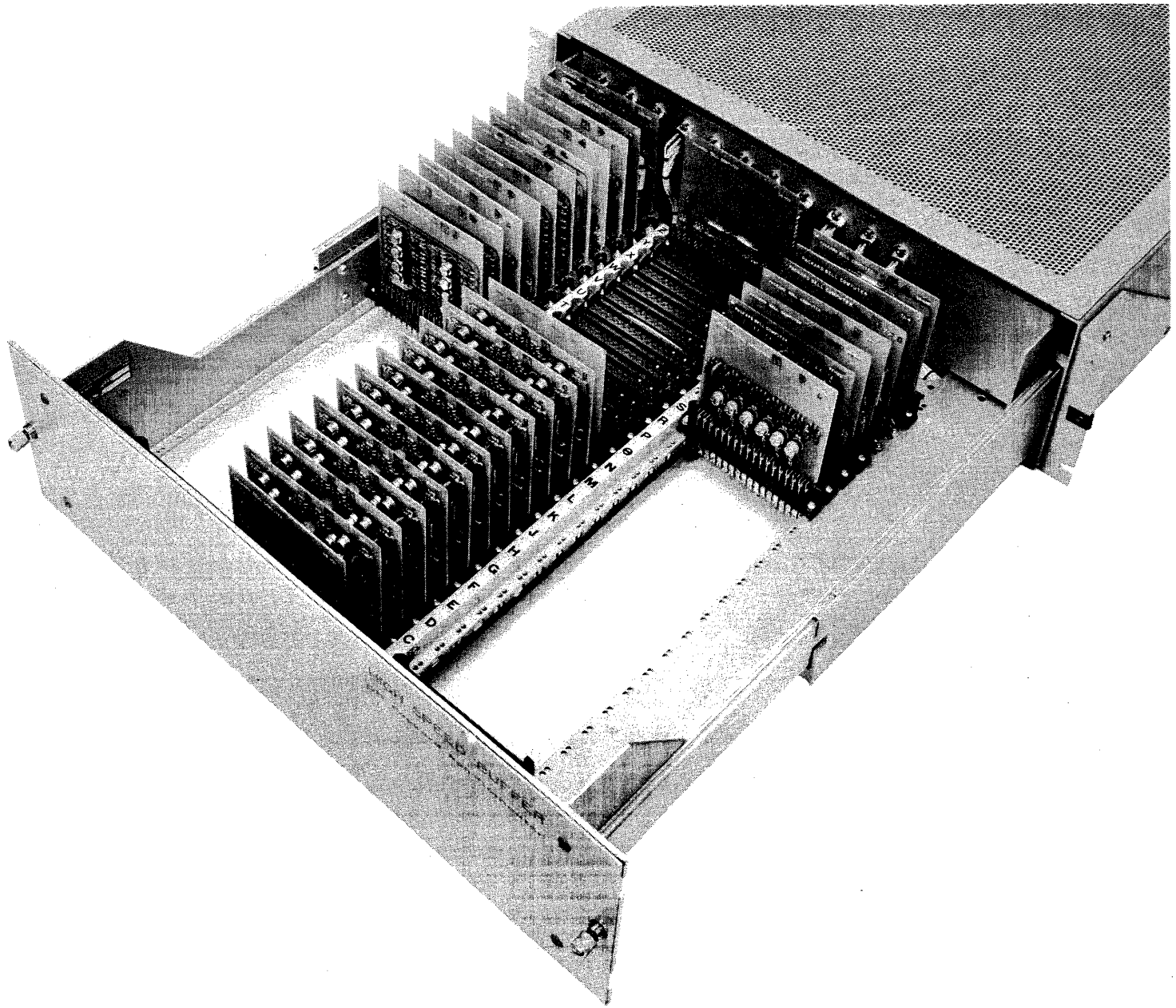


Figure 1-1. High-Speed Buffer Register

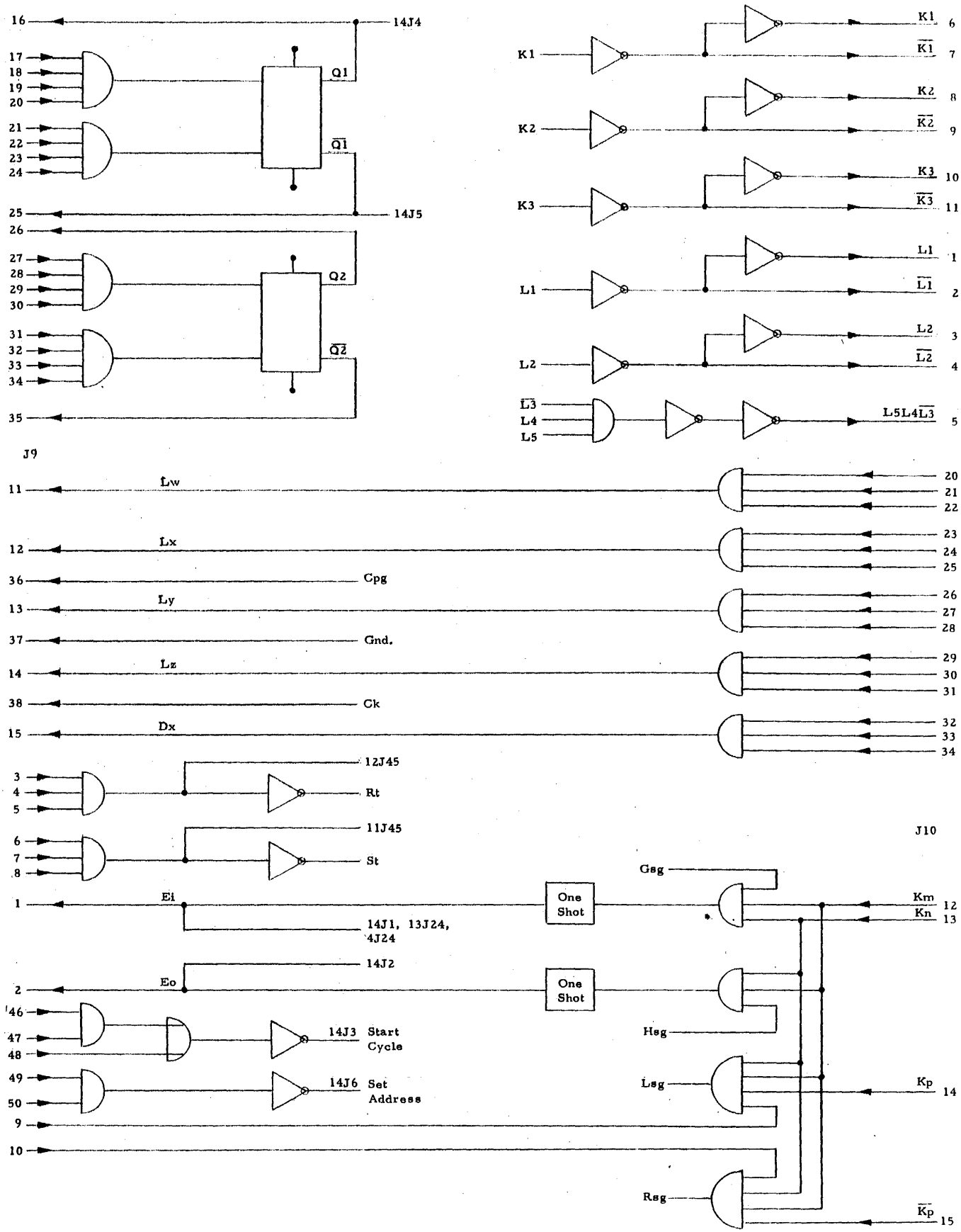


Figure 1-2. General Purpose Logic

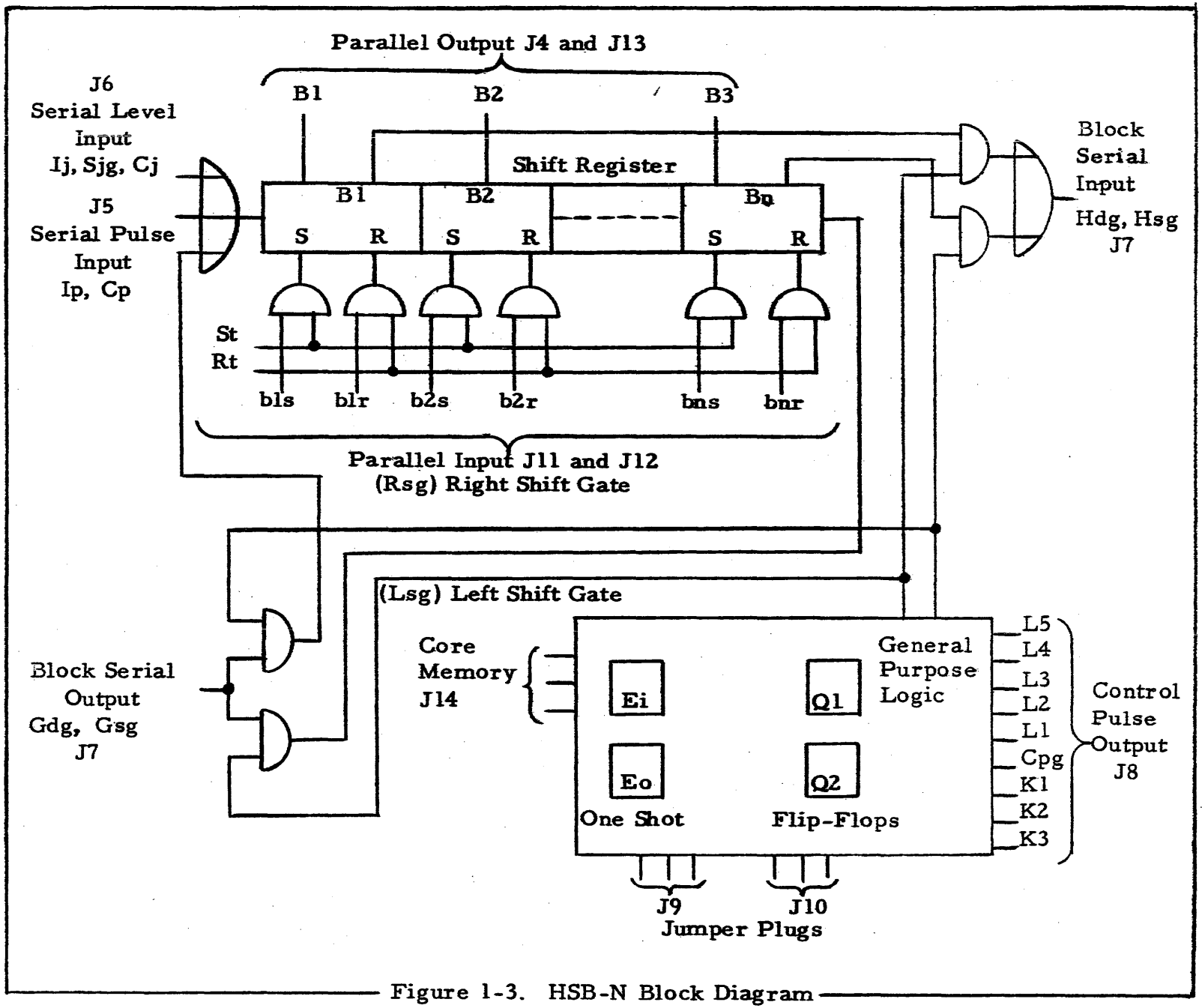


Figure 1-3. HSB-N Block Diagram

The shift register requires one 35-pin plug-in module for each two bits so that the maximum total number of modules for 44 bits, is 42 (31 modules for 22 bits). If the shift register is less than 44 bits long, a termination (jumper) module is installed after the last shift register module.

The connectors used in the HSB-N may be Cannon type or Amphenol equivalents. Table 1-1 lists the Cannon connectors used. An optional accessory to the HSB-N is a display front panel, containing indicator lights for 22 (IB 22) or 44 (IB 44) stages of the shift register.

Table 1-1 (Sheet 1 of 8)

CONNECTORS

J4 Parallel Output DC 37S			
Pin No.	Function	Pin No.	Function
1	B 23	13	B 35
2	B 24	14	B 36
3	B 25	15	B 37
4	B 26	16	B 38
5	B 27	17	B 39
6	B 28	18	B 40
7	B 29	19	B 41
8	B 30	20	B 42
9	B 31	21	B 43
10	B 32	22	B 44
11	B 33	23	Ground
12	B 34	24	Ei

Table 1-1 (Sheet 2 of 8)

CONNECTORS

J5 Serial Pulse Input DE 9P

Pin No.	Function
1	Cp
2	Ground
3	Ip
4	Ground

J6 Serial Level Input DA 15S

Pin No.	Function
1	Cj
2	Ground
3	Ij
4	Ground
5	Sjg

J7 Computer Serial Input-Output DA 15P

Pin No.	Function
1	Gsg
3	Gdg
5	Ck
6	Ground
7	Hsg
9	Hdg
11	K1
12	K2
13	K3

Table 1-1 (Sheet 3 of 8)

CONNECTORS

J8 Computer Control Pulse Output DB 25P	
Pin No.	Function
1	K1
2	K2
3	K3
4	L1
5	L2
6	L3
7	L4
8	L5
9	Cpg
10	Ground
11	Ground
12	+6v
13	-12v
23	Ground
24	1 vac
25	+50v

Table 1-1 (Sheet 4 of 8)

CONNECTORS

J9 General Purpose Logic DD 50S		J9 General Purpose Logic DD 50S	
Pin No.	Function	Pin No.	Function
1	Ei	22	Q1 reset in 2
2	Eo	23	Q1 reset in 3
3	Rt in 1	24	Q1 reset in 4
4	Rt in 2	25	$\overline{Q1}$ out
5	Rt in 3	26	Q2 out
6	St in 1	27	Q2 set in 1
7	St in 2	28	Q2 set in 2
8	St in 3	29	Q2 set in 3
9	Lsg in 1	30	Q2 set in 4
10	Rsg in 1	31	Q2 reset in 1
11	Lw out	32	Q2 reset in 2
12	Lx out	33	Q2 reset in 3
13	Ly out	34	Q2 reset in 4
14	Lz out	35	$\overline{Q2}$ out
15	Dx out	36	Cpg
16	Q1 out	37	Ground
17	Q1 set in 1	38	Ck
18	Q1 set in 2	46	Start cycle in 1
19	Q1 set in 3	47	Start cycle in 2
20	Q1 set in 4	48	Start cycle in 3
21	Q1 reset in 1	49	Set address in 1
		50	Set address in 2

Table 1-1 (Sheet 5 of 8)

CONNECTORS

J10 General Purpose Logic DC 37P		J10 General Purpose Logic DC 37P	
Pin No.	Function	Pin No.	Function
1	L1'	20	Lw in 1
2	L1	21	Lw in 2
3	L2'	22	Lw in 3
4	L2	23	Lx in 1
5	L3 L4 L5	24	Lx in 2
6	K1'	25	Lx in 3
7	K1	26	Ly in 1
8	K2'	27	Ly in 2
9	K2	28	Ly in 3
10	K3'	29	Lz in 1
11	K3	30	Lz in 2
12	Km in 1	31	Lz in 3
13	Kn in 1	32	Dx in 1
14	Kp in 1	33	Dx in 2
15	Kp in 1	34	Dx in 3

Table 1-1 (Sheet 6 of 8)

CONNECTORS

J11 Parallel Set Input DD 50P		J11 Parallel Set Input DD 50P	
Pin No.	Function	Pin No.	Function
1	b1s	24	b24s
2	b2s	25	b25s
3	b3s	26	b26s
4	b4s	27	b27s
5	b5s	28	b28s
6	b6s	29	b29s
7	b7s	30	b30s
8	b8s	31	b31s
9	b9s	32	b32s
10	b10s	33	b33s
11	b11s	34	b34s
12	b12s	35	b35s
13	b13s	36	b36s
14	b14s	37	b37s
15	b15s	38	b38s
16	b16s	39	b39s
17	b17s	40	b40s
18	b18s	41	b41s
19	b19s	42	b42s
20	b20s	43	b43s
21	b21s	44	b44s
22	b22s	45	St
23	b23s	46	Gnd

Table 1-1 (Sheet 7 of 8)

CONNECTORS

J12 Parallel Reset Input DD 50P		J12 Parallel Reset Input DD 50P	
Pin No.	Function	Pin No.	Function
1	b1r	24	b24r
2	b2r	25	b25r
3	b3r	26	b26r
4	b4r	27	b27r
5	b5r	28	b28r
6	b6r	29	b29r
7	b7r	30	b30r
8	b8r	31	b31r
9	b9r	32	b32r
10	b10r	33	b33r
11	b11r	34	b34r
12	b12r	35	b35r
13	b13r	36	b36r
14	b14r	37	b37r
15	b15r	38	b38r
16	b16r	39	b39r
17	b17r	40	b40r
18	b18r	41	b41r
19	b19r	42	b42r
20	b20r	43	b43r
21	b21r	44	b44r
22	b22r	45	Rt
23	b23r	46	Ground

Table 1-1 (Sheet 8 of 8)

CONNECTORS

J13 Parallel Output DC 37S		J13 Parallel Output DC 37S	
Pin No.	Function	Pin No.	Function
1	B1	13	B13
2	B2	14	B14
3	B3	15	B15
4	B4	16	B16
5	B5	17	B17
6	B6	18	B18
7	B7	19	B19
8	B8	20	B20
9	B9	21	B21
10	B10	22	B22
11	B11	23	Ground
12	B12	24	Ei

J14 Core Memory Coupling DE 9S	
Pin No.	Function
1	Ei
2	Eo
3	Start cycle
4	Read (Q1)
5	Write ($\overline{Q1}$)
6	Set address
7	Ground

II. THEORY OF OPERATION

A. GENERAL

The HSB-N register can shift left or right, as determined by the general purpose logic and control pulse codes or command line number. The length of the shift register can be any even number (N) of stages from 2 to 44. Stages 22 and 44 correspond to 1 and 2 words of the PB 250 respectively, but since block serial input and output are controlled by a mask, words can be assembled under control of the PB 250 program (see PB 250 Programming Manual).

B. PB 250 COMPUTER CONNECTIONS

The PB 250 Computer serial input-output connections are shown in Figure 2-1. Two cables connect the HSB-N to the PB 250. These cables contain serial data and mask inputs and outputs (Gdg, Gsg, Hdg, Hsg), the 2 mc computer clock (Ck), control pulse (Cpg), operand line code (L1 through L5), command line code (K1 through K3) and dc power (connectors J7 and J8). Data and mask are determined by the PB 250 program and the buffer register contents, but the direction of shift must be programmed by patching the general purpose logic on jumper plugs J9 and J10 (signals Lsg and Rsg, see Figure 1-2). Typical possibilities for this are: fixed shift direction, determined by grounding the Lsg or Rsg gate on J9; shift direction depending on the command line number out of which the BSO or BSI command is executed; shift direction controlled by flip-flops Q1 and Q2, which are turned on and off by PTU (Pulse to Specified Unit) commands with octal codes (operand lines) numbers 24 through 27. Description of the

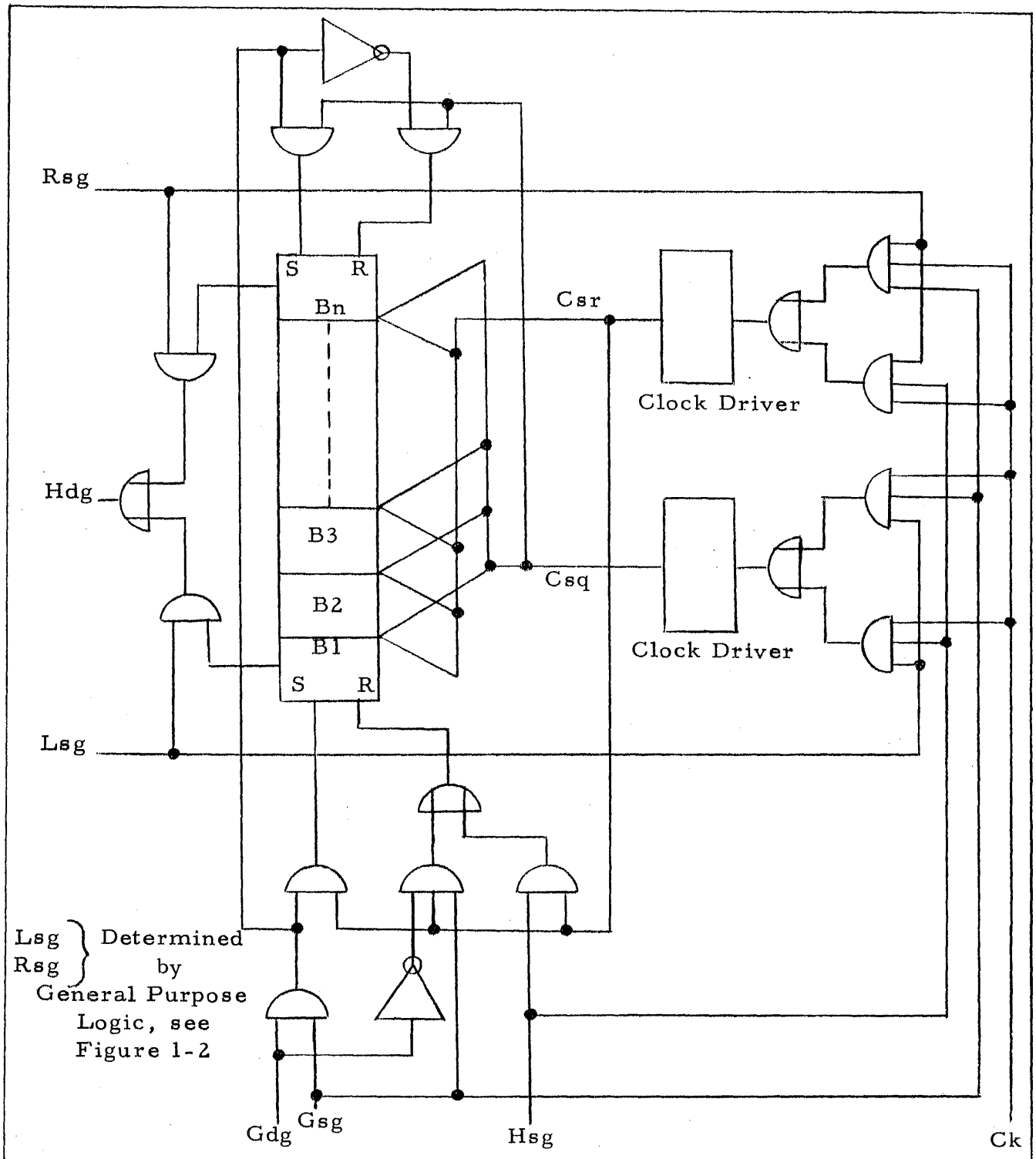


Figure 2-1. Serial Input-Output (PB 250 Connections)

functioning of the commands mentioned, is included in the PB 250 Reference Manual.

C. PARALLEL INPUT AND OUTPUT

Parallel inputs and outputs consist of individual "on" level inputs and a common "on" trigger, and individual "off" level inputs and a common "off" trigger.

The true ("1") outputs, see Figure 1-2, of all stages of the shift register (B1 through B44) are available on connectors J4 and J13. Each can be loaded by 750 ohms and 150 $\mu\mu$f to ground and supply up to 10 ma into a load returned to a voltage between -8 and -12v (typically diode AND gates of the negative true logic type returned to -12v). Parallel set and reset level inputs (bls, blr) combined with common set and reset trigger inputs (St, Rt) are available on connectors J11 and J12. The maximum load represented by each of these inputs is 5.6k ohms to $\approx$12v (one diode AND gate). Level input "true" should be -9 ± 3v, "false" 0 ± 0.5v. St and Rt can also be programmed by patching on J9 and J10 typically to the pulse output of a PTU command (Cpg gated by L's and K's). The requirements for the shape of external pulses to be used for St and Rt are: upper level 0 ± 0.5v, lower level -9 ± 3v, risetime of positive going (triggering) edge 0.5 μsec. maximum, duration at lower level 0.5 μsec. minimum, duration at upper level 0.5 μsec. minimum.

D. SERIAL LEVEL INPUT

The serial level input, see Figure 2-2, consists of a data line (Ij), a gate line (Sjg) and clock line (Cj) available on J6. Shift direction is to the right. Levels on Ij and Sjg should be 0 ± 0.5v for "false" and -9 ± 3v for "true". Clock pulse requirements are: upper ("false") level 0 ± 0.5v, duration at upper level 0.5 μsec. minimum, lower ("true") level -9 ± 3v,

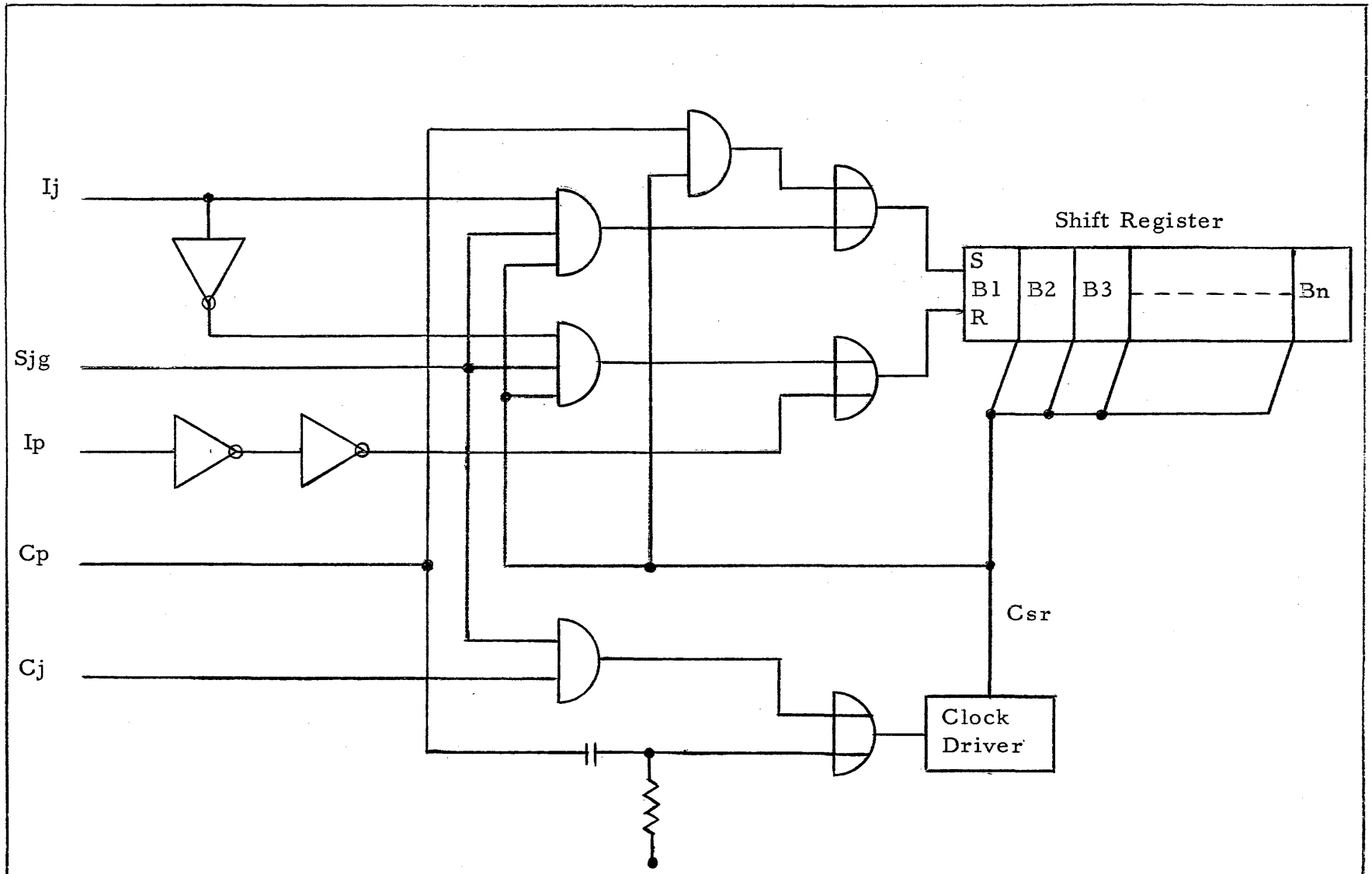


Figure 2-2. Serial Input (Not PB 250 Connections)

duration at lower level 0.5 μsec. minimum, risetime of positive going (triggering) edge 0.5 μsec. maximum. Ij and Sjg should change state only during the time Cj is at its upper ("false") level. The maximum load represented by Cj is 5.6k ohms -12v, Sjg 2.8k ohms to -12v, Ij 2.8k ohms to -6v.

E. SERIAL PULSE INPUT

Serial pulse inputs consist of bit reset pulses and clock pulses specifically adapted for connection to analog-to-digital converters M2 and M3. Shift direction is to the right.

The serial pulse input, see Figure 2-2, consists of a clock line (Cp) and a bit reset line (Ip) available on J5. This input is adapted to MULTIVERTER outputs, where Cp is the bit set and Ip the bit reset signal. Both signals should be negative pulses, upper level 0 ± 0.5v, lower level -9 ± 3v. Ip should have a duration at the lower level of 0.5 μsec. minimum, duration at upper level 0.5 μsec. minimum, risetime of positive going (triggering) edge 0.5 μsec. maximum. Cp should have a duration at the lower level of 1 μsec. minimum, duration at upper level 1 μsec. minimum, and the fall time of negative going (triggering) edge 0.5 μsec. maximum. The negative going edge of Cp should precede the positive going edge of Ip by 1 μsec. minimum. The negative going edge of Cp causes a right shift and sets the first stage (B1) of the shift register to "1". The positive going edge of Ip will then set the first stage to "0". The load represented by Ip is 5.6k to ground, by Cp 5.6k ohms to -12v and 100 μμf into 10k ohms to ground.

F. HIGH-SPEED BUFFER (HSB-N) LOGIC

$$\overline{sB1} = Csr\ (Gdg\ Gsg) + Ij\ Sjg\ Csr + Csq\ B2 + Cp\ Csr + bls\ St$$

B1

$$\underline{Rb1} = Csr\ (\overline{Gdg}\ Gsg) + Csr\ Hsg + \overline{Ij}\ Sjg\ Csr + Csq\ \overline{B2} + Ip + blr\ Rt$$

$$\overline{sB2} = Csr\ B1 + Csq\ (B3 \text{ or } X) + B2s\ St$$

B2

$$\underline{rB2} = Csr\ \overline{B1} + Csq\ (\overline{B3} \text{ or } \overline{X}) + b2r\ Rt$$

through

$$\overline{sB44} = Csr\ B43 + Csq\ (Gdg\ Gsg) + b44s\ St$$

B44

$$\underline{rB44} = Csr\ \overline{B43} + Csq\ \overline{(Gdg\ Gsg)} + b44r\ Rt$$

$$Csq = Lsg\ Ck\ (Hsg + Gsg)$$

$$Csr = Rsg\ Ck\ (Hsg + Gsg) + Cp + Cj\ Sjg$$

$$Hdg = [(B44 \text{ or } Y)\ Rsg + B1\ Lsg]$$

G. GENERAL PURPOSE LOGIC

	Lw	= 3 term AND gate
	Lx	= 3 term AND gate
	Ly	= 3 term AND gate
	Lz	= 3 term AND gate
	Dx	= 3 term AND gate
Q1	$\overline{sQ1}$	= 4 term AND gate
	$\overline{rQ1}$	= 4 term AND gate
Q2	$\overline{sQ2}$	= 4 term AND gate
	$\overline{rQ2}$	= 4 term AND gate
	Set address	= 2 term AND gate
	Start cycle	= 2 term AND gate OR 1 term
	St	= 3 term AND or external input
	Rt	= 3 term AND or external input
	Ei trigger	= Km Kn Gsg } One shots
	Eo trigger	= Km Kn Hsg }
	Rsg	= Km Kn $\overline{Kp}$ AND 1 term
	Lsg	= Km Kn Kp AND 1 term

III. MAINTENANCE

A. GENERAL

Most of the buffer logic and circuitry can be tested by means of a PB 250 program, which generates pseudo-random numbers, transfers them to the buffer (BSO command), reads them back into the computer (BSI command) and compares the number read back to the one generated. The program should have alternate modes of operation to either stop on error, or continue disregarding error (the second of these modes is used to trace malfunctions in the circuitry). Disconnect any equipment other than the PB 250 from the buffer during this test, in particular any serial pulse or serial level inputs. Tests of those inputs are best performed in connection with the system in which the buffer is used. This part of the logic contains only a small number of components and signals (Cp, Ip, Cj, Ij, Sjg) and is affected by the timing and levels of the external signals.

Whenever serial pulse input and serial level input are not used Cp and Sjg must be grounded (J5 pins 1 - 2, J6, pins 4 - 5). The shift direction in connection with the PB 250 must be selected; for right shift connect J9, pins 9 - 37; for left shift connect J9, pins 10 - 37.

The typical test routine, which is listed and described in Appendix B, does not utilize any part of the general purpose logic, serial pulse input or serial level input.

B. INSTALLATION

Refer to Figure 3-1 for details of the installation of the HSB-N. Note that connectors J16 and J17 are on the PB 250 Computer. Table 3-1 contains serial input-output cable information and Table 3-2 contains control pulse cable information.

C. TROUBLESHOOTING PROCEDURE

For signal flow, circuit details and test points refer to the applicable logic layout given in Appendix A, and proceed as follows:

1) Arrange the oscilloscope trigger so that the execute phase of the BSO and BSI commands can be displayed. Gsg, which represents the execute phase of the BSO command gated by the mask, or the cycle sync signal of the PB 250 in conjunction with a delayed sweep, can be used as sync.

2) Check to ensure that Gsg and Hsg are operating properly and trace the signals back to the computer.

3) Check to ensure that the shift clock (Csr for right shift, Csq for left shift) is operating during the time Gsg and Hsg are true and trace the signals through the clock driver input gates and to all clock driver outputs.

4) Check Gdg during the time Gsg is true (this represents the input signal to the buffer). Trace the signal into the shift register, starting at B1 for right shift, Bn for left shift, (n is the number of bits in the buffer).

5) Check Hdg during the time Hsg is true (this is the output signal from the buffer into the computer). Trace the signal back into the shift register, starting at Bn for right shift, B1 for left shift.

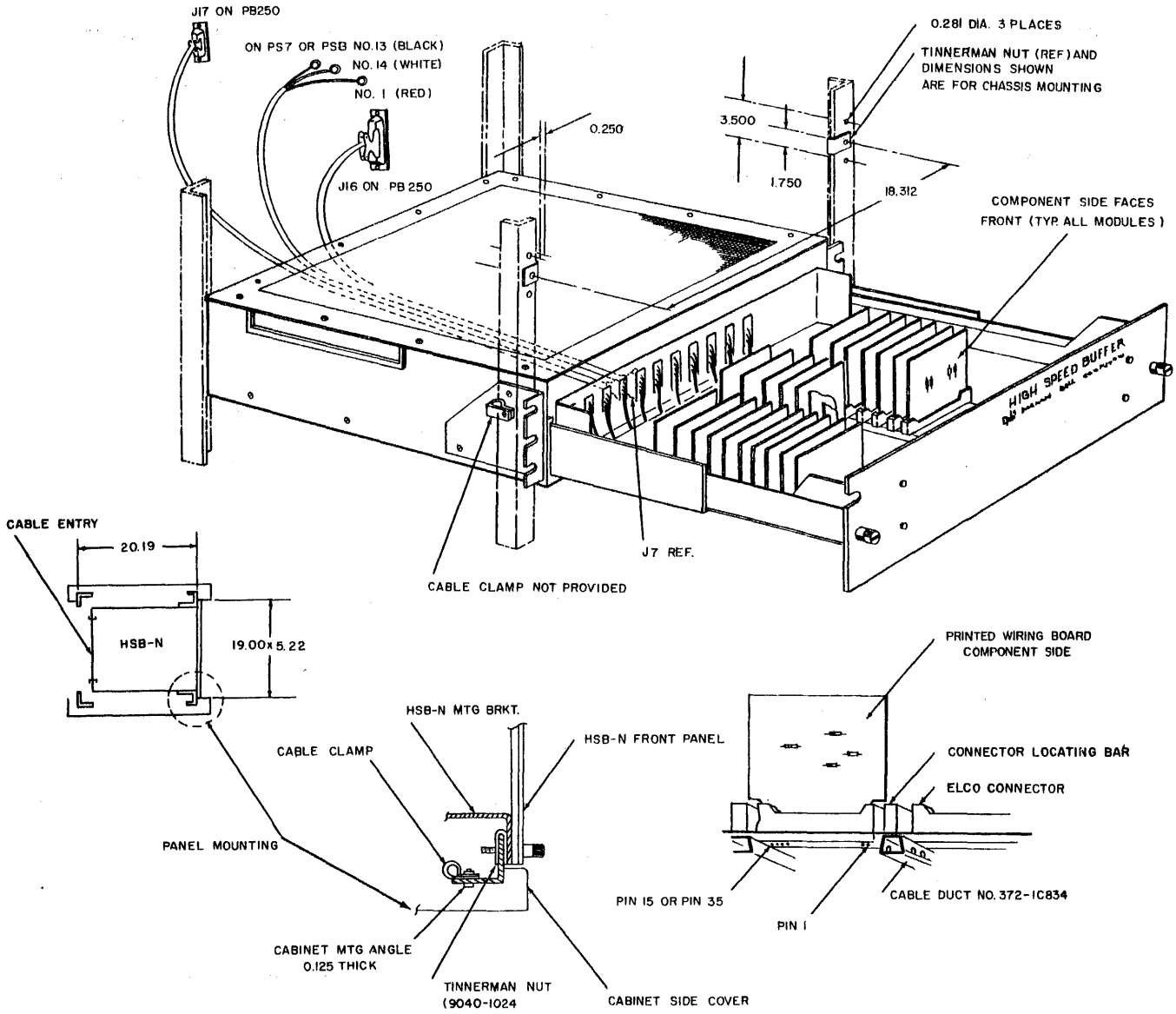


Figure 3-1. HSB-N Installation Drawing

Table 3-1

SERIAL INPUT-OUTPUT CABLE

HSB Plug J7 DA15S	Function	PB250 Plug J17 DE9S
Pin No.		Pin No.
1	Gsg	7
2		
3	Gdg	8
4	Ck Shield (Ground)	6
5	Ck	9
6	Shield Ground	
7	Hsg	4
8		
9	Hdg	5
10		
11	K1	3
12	K2	2
13	K3	1
14		
15		

Table 3-2 (Sheet 1 of 2)

CONTROL PULSE CABLE

HSB Plug J8 DB 25S	Function	PB 250 Plug J16 DA 15S
Pin No.		Pin No.
1	K1	3
2	K2	2
3	K3	1
4	L1	4
5	L2	5
6	L3	6
7	L4	7
8	L5	8
9	Cpg	12
10	Ground	13
11		
12	+6v	14
13	-12v	15
14		
15		
16		
17		
18		
19		

Table 3-2 (Sheet 2 of 2)

CONTROL PULSE CABLE

HSB Plug J8 DB 25S	Function	PB 250 Plug J16 DA 15S
Pin No.		Pin No.
20		
21		
22		
		PS7 Terminal Strip
		Terminal No.
23	Ground	13
24	1 vac	14
25	+50v	1

Even for an all "1" mask, Hsg and Gsg contain large "glitches", which do not normally interfere with the operation of the HSB-N, since they occur during the "off" time of the clock.

D. MARGINAL CHECKING

The HSB-N receives its power from the PB 250 Computer power supply, and takes part in any marginal voltage tests. Note that the HSB-N is not affected by the marginal clock tests of the computer, since the HSB-N has its own clock shaper.

IV. PARTS LIST

Item	Description	Part No.	Quantity
1	Assembly, Cable (Block Serial Input-Output)	124-1D4886	1
2	Assembly, Cable (Control Pulse and Power)	124-1D5887	1
3	Assembly, Cable, HSB-N	123-1J5184	1
4	Assembly, Chassis, HSB-N	123-1J5171	1
5	Assembly, Module, CD-100	124-1D2692	4
6	Assembly, Module, DG-100	124-1D2334	1
7	Assembly, Module, DG-102	124-1D2336	5
8	Assembly, Module, EF-101	124-1C4625	3
9	Assembly, Module, GD-100	124-1D2492	2
*10	Assembly, Module, SR-100	124-1C4613	$\frac{n}{2}$
11	Assembly, Module, T1-4	124-1C1005	2
*12	Assembly, Module, Terminal, HSB	124-1C1542	1
13	Assembly, Module, TF-100	124-1D2433	1
14	Assembly, Module, TO-3	124-1C416	1

Item 10, n = number of bits; Item 12, if n = 44, qty of item is 0

Item	Description	Part No.	Quantity
15	Assembly, Module, XCG-100	124-1D2689	1
16	Cable, Coaxial, Microdot, No. 95-3920		AR
17	Capacitor,	217-A3204-101	
18	Cord, Lacing, Nylon; Type P, Waxed, Class 2, per MIL-T-713 (0.050 wide)		AR
19	Nut, Plain, Hexagon, No. 4-40, Cad. Pl.		2
20	Panel, Front, HSB-N	634-1D5176	1
*21	Pin, Polarizing	644-1A3110	38 + n
22	Resistor, 10k, ±5 %, 1/4w	727-1A3100-103	1
23	Screw, 4-40, Mach, Pan Hd		2
24	Screw, Front Panel	760-1C816-1	4
25	Sleeving, Plastic, 16 gage (per MIL-I-631C)		AR
26	Strip, Power, Junction	124-1C5175	1
27	Washer, Flat, No. 4, Cad. Pl.		2
28	Washer, Lock, No. 4, Int. Tooth		2

Item 21, n = number of bits

Item	Description	Part No.	Quantity
29	Washer, Lock No. 6, Int. Tooth		4
30	Wire, Solid, Uninsulated, 16 gage		AR
31	Wire, Stranded, Vinyl, Insulated 18 gage		AR

APPENDIX A

Logic Layouts

APPENDIX A

Appendix A contains logic layouts for the High-Speed Buffer. A glossary of terms is provided in Table A-1. An index of the various functions and their location in the appendix is as follows:

HSB-N INDEX

Function	Page No.	Function	Page No.
B1, B2	A-13	Ei, Eo	A-9
B3, B4	A-14	Gdg	A-7
B5, B6	A-15	Gdg, Gsg; $\overline{\text{Gdg, Gsg}}$	A-7
B7, B8	A-16	Gsg	A-7
B9, B10	A-17	Hdg	A-8
B11, B12	A-18	Hsg	A-8
B13, B14	A-19	Ij	A-6
B15, B16	A-20	Ip	A-6
B17, B18	A-21	K1', $\overline{\text{K1}}$	A-10
B19, B20	A-22	K2', $\overline{\text{K2}}$	A-10
B21, B22	A-23	K3', $\overline{\text{K3}}$	A-10
B23, B24	A-24	L1', $\overline{\text{L1}}$	A-11
B25, B26	A-25	L2', $\overline{\text{L2}}$	A-11
B27, B28	A-26	L5, L4, $\overline{\text{L3}}$	A-11
B29, B30	A-27	Lsg	A-9
B31, B32	A-28	Lw	A-10
B33, B34	A-29	Lx	A-10
B35, B36	A-30	Ly	A-11
B37, B38	A-31	Lz	A-11
B39, B40	A-32	Q1	A-12
B41, B42	A-33	Q2	A-12
B43, B44	A-34	Rsg	A-9
Cj	A-6	Rt	A-5
Ck	A-8	Set address	A-9
Cp	A-6	Sjg	A-6
Csq	A-4	St	A-5
Csr	A-4	Start cycle	A-9
Dx	A-10		

Table A-1. (Sheet 1 of 2)

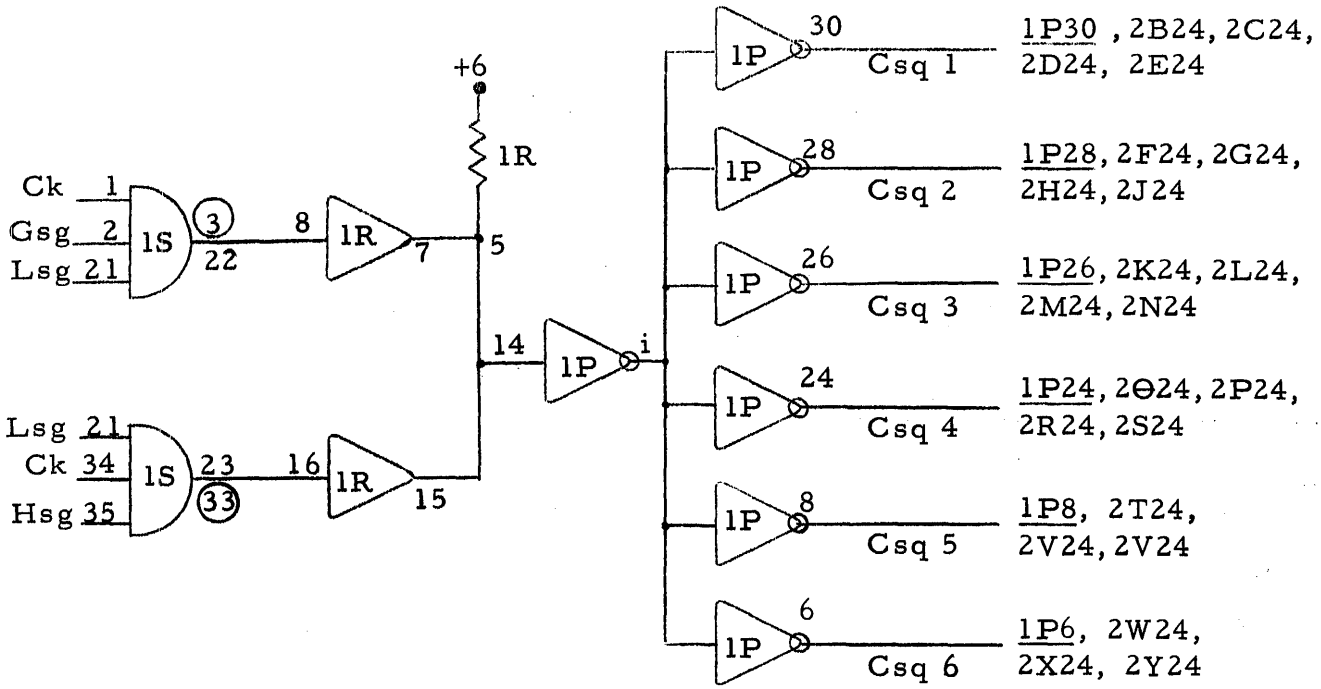
GLOSSARY OF TERMS

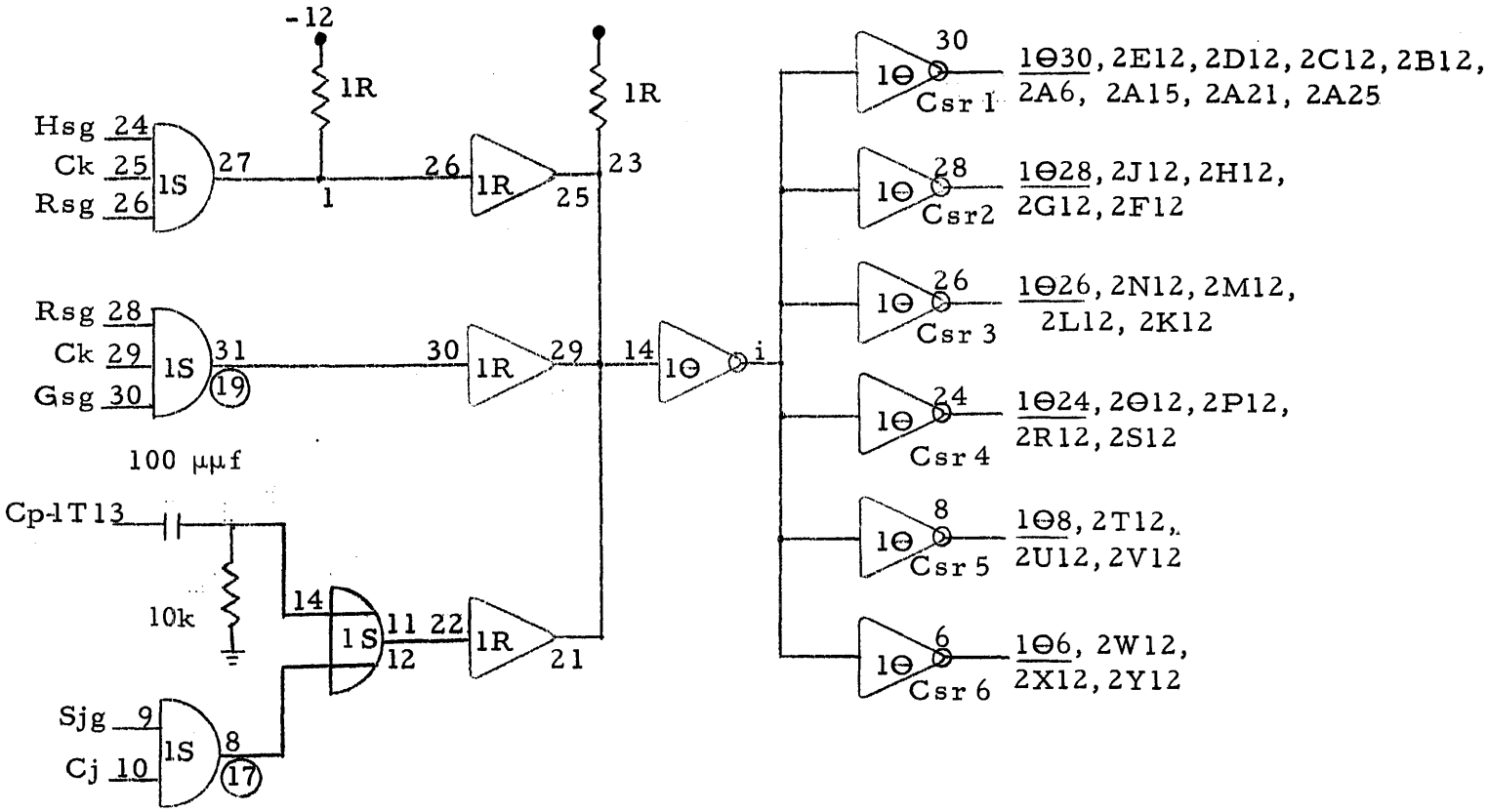
Function	Term
B1, B2 - - - B44	Register stages
b1r - - - - - b44r	Parallel input reset terms
b1s - - - - - b44s	Parallel input set terms
Cj	Serial level clock
Ck	Computer clock
Cp	Serial pulse train clock
Cpg	Control pulse
Csq	Buffer clock left shift
Csr	Buffer clock right shift
Ei	End of input pulse
Eo	End of output pulse
Gdg	Serial output data (from PB 250)
Gsg	Serial output mask (from PB 250)
Hdg	Serial input data (to PB 250)
Hsg	Serial input mask (to PB 250)
Ij	Serial level data
Ip	Serial pulse data (zero bit)
K1 - - - K3	Command line code
L1 - - - L5	Operand line code

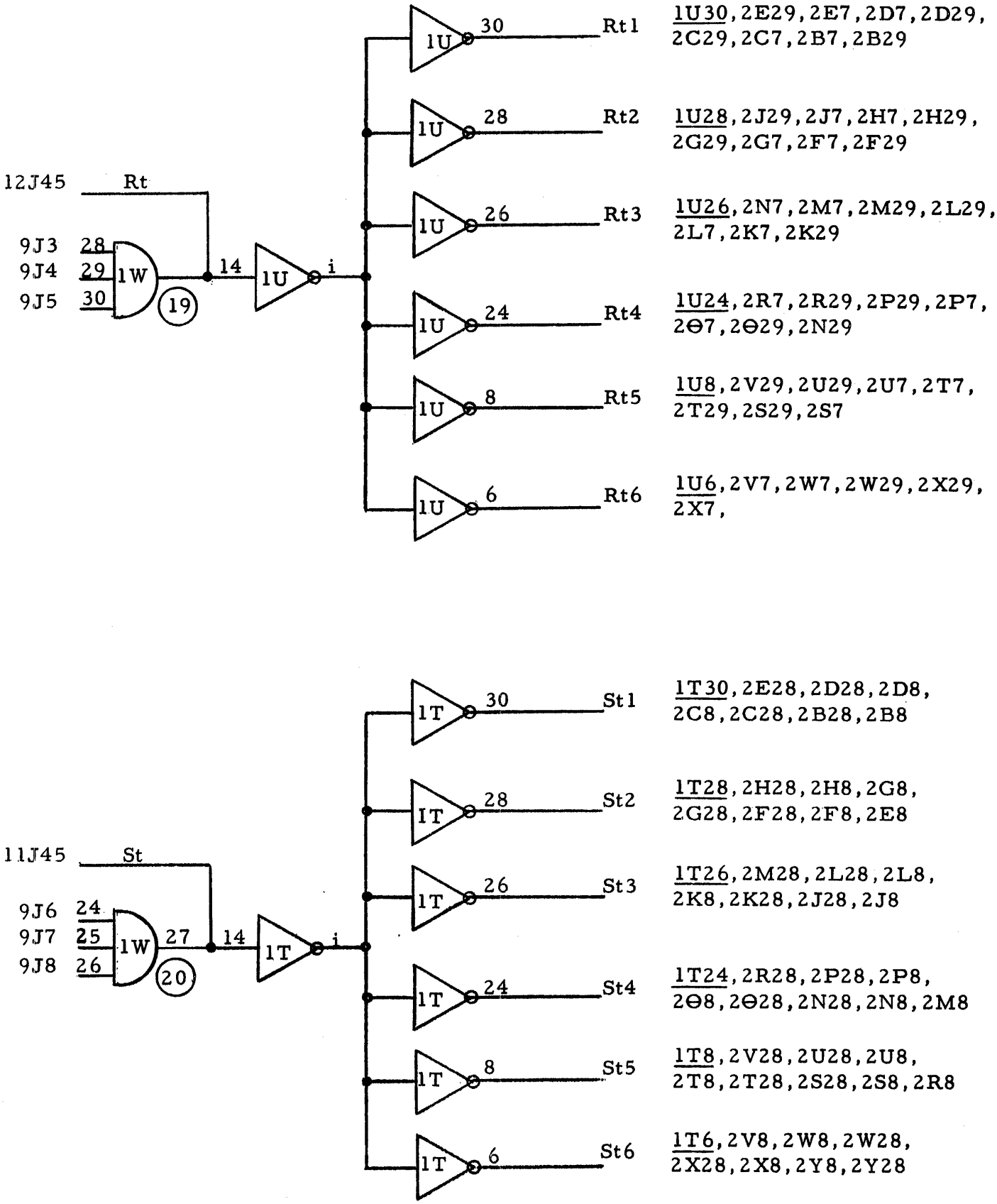
Table A-1. (Sheet 2 of 2)

GLOSSARY OF TERMS

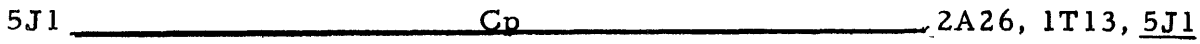
Function	Term
Lsg	Shift left gate
Q1	Interlock flip-flop
Q2	Interlock flip-flop
Rsg	Shift right gate
Rt	Reset transfer
Sjg	Serial level gate
St	Set transfer
X	(Gdg Gsg) bus line
Y	Bn bus line


+6
1R
Ck 1
Gsg 2
Lsg 21
1S
3
22
8
1R
7
5
14
1P
i
Lsg 21
Ck 34
Hsg 35
1S
23
33
16
1R
15
1P 30
Csq 1
1P30 , 2B24, 2C24, 2D24, 2E24
1P 28
Csq 2
1P28, 2F24, 2G24, 2H24, 2J24
1P 26
Csq 3
1P26, 2K24, 2L24, 2M24, 2N24
1P 24
Csq 4
1P24, 2Θ24, 2P24, 2R24, 2S24
1P 8
Csq 5
1P8, 2T24, 2V24, 2V24
1P 6
Csq 6
1P6, 2W24, 2X24, 2Y24

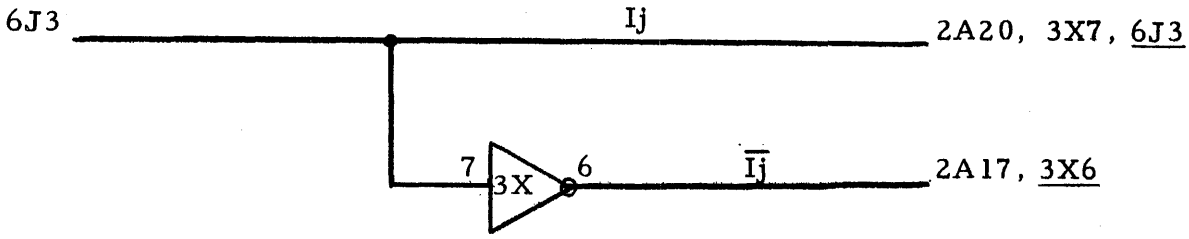

-12
1R
Hsg 24
Ck 25
Rsg 26
1S
27
1
26
1R
25
23
1R
Rsg 28
Ck 29
Gsg 30
1S
31
19
30
1R
29
14
1Θ
i
100 μμf
Cp-1T13
10k
14
1S
11 22
12
1R
21
Sjg 9
Cj 10
1S
8
17
1Θ 30
Csr 1
1Θ30, 2E12, 2D12, 2C12, 2B12, 2A6, 2A15, 2A21, 2A25
1Θ 28
Csr2
1Θ28, 2J12, 2H12, 2G12, 2F12
1Θ 26
Csr 3
1Θ26, 2N12, 2M12, 2L12, 2K12
1Θ 24
Csr 4
1Θ24, 2Θ12, 2P12, 2R12, 2S12
1Θ 8
Csr 5
1Θ8, 2T12, 2U12, 2V12
1Θ 6
Csr 6
1Θ6, 2W12, 2X12, 2Y12


12J45
Rt
9J3
9J4
9J5
28
29
30
1W
19
14
1U
i
1U
30
Rt1
1U30,2E29,2E7,2D7,2D29,
2C29,2C7,2B7,2B29
1U
28
Rt2
1U28,2J29,2J7,2H7,2H29,
2G29,2G7,2F7,2F29
1U
26
Rt3
1U26,2N7,2M7,2M29,2L29,
2L7,2K7,2K29
1U
24
Rt4
1U24,2R7,2R29,2P29,2P7,
2Θ7,2Θ29,2N29
1U
8
Rt5
1U8,2V29,2U29,2U7,2T7,
2T29,2S29,2S7
1U
6
Rt6
1U6,2V7,2W7,2W29,2X29,
2X7,
11J45
St
9J6
9J7
9J8
24
25
26
1W
20
27
14
1T
i
1T
30
St1
1T30,2E28,2D28,2D8,
2C8,2C28,2B28,2B8
1T
28
St2
1T28,2H28,2H8,2G8,
2G28,2F28,2F8,2E8
1T
26
St3
1T26,2M28,2L28,2L8,
2K8,2K28,2J28,2J8
1T
24
St4
1T24,2R28,2P28,2P8,
2Θ8,2Θ28,2N28,2N8,2M8
1T
8
St5
1T8,2V28,2U28,2U8,
2T8,2T28,2S28,2S8,2R8
1T
6
St6
1T6,2V8,2W8,2W28,
2X28,2X8,2Y8,2Y28

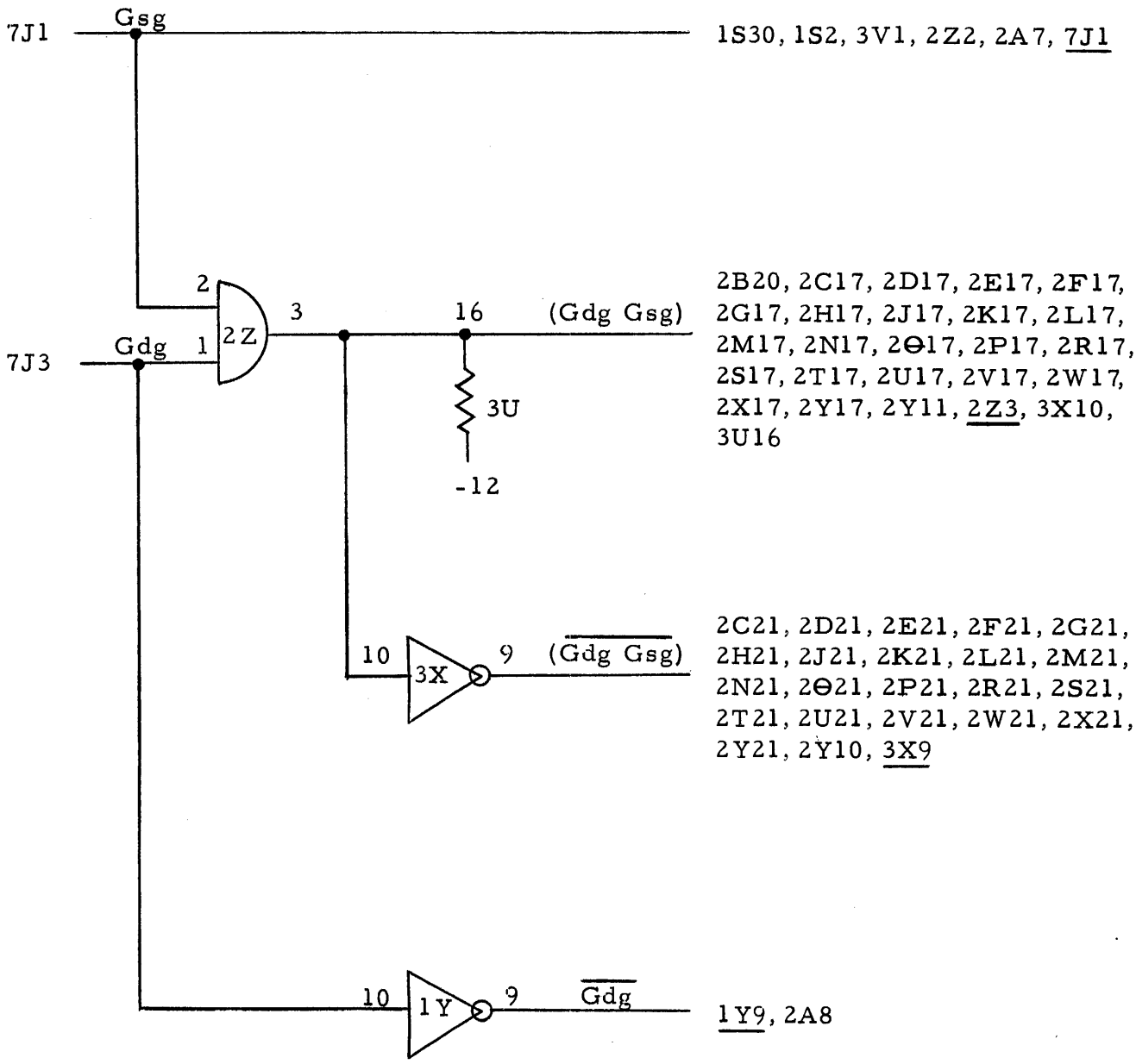

5J3
Ip
5
3X
4
3
3X
2
Ip
3X2, 2A11

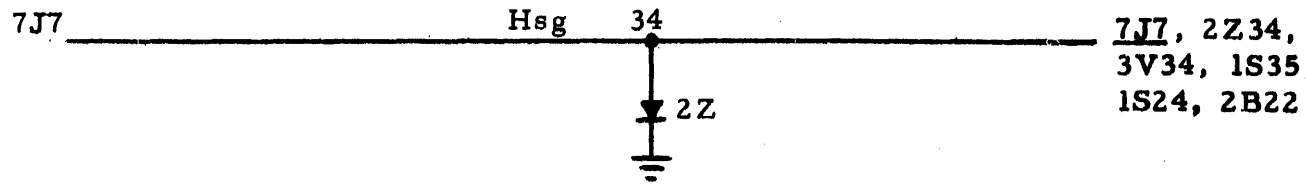

5J1
Cp
2A26, 1T13, 5J1

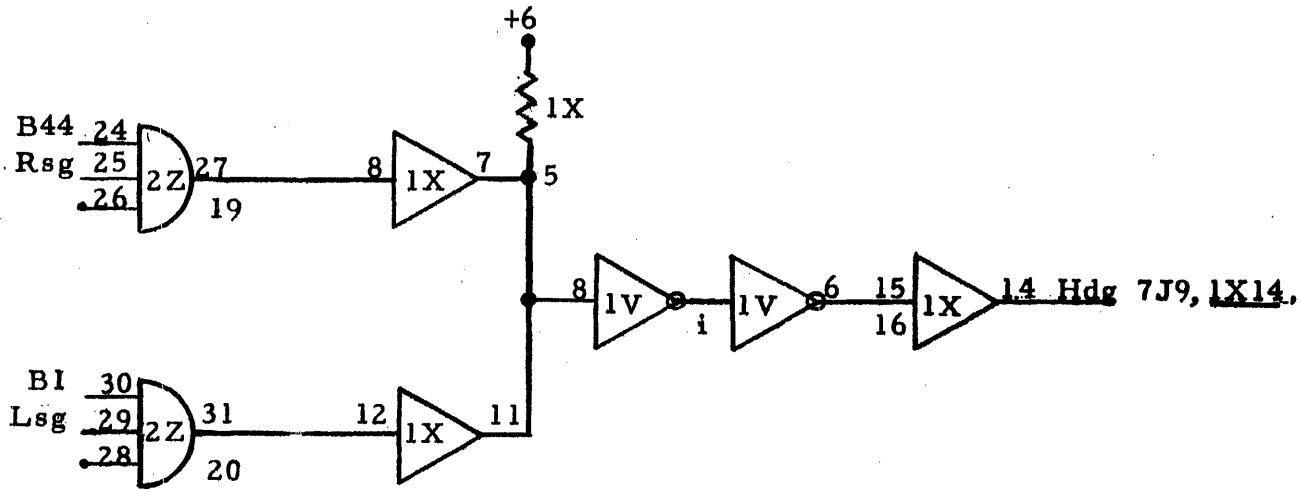

6J5
Sjg
6J5, 1S9, 2A16, 2A19

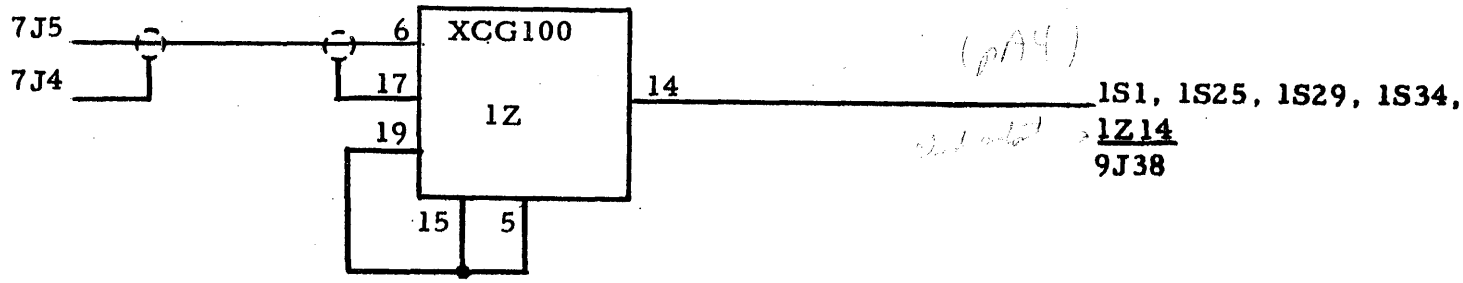

6J3
Ij
2A20, 3X7, 6J3
7
3X
6
Ij
2A17, 3X6

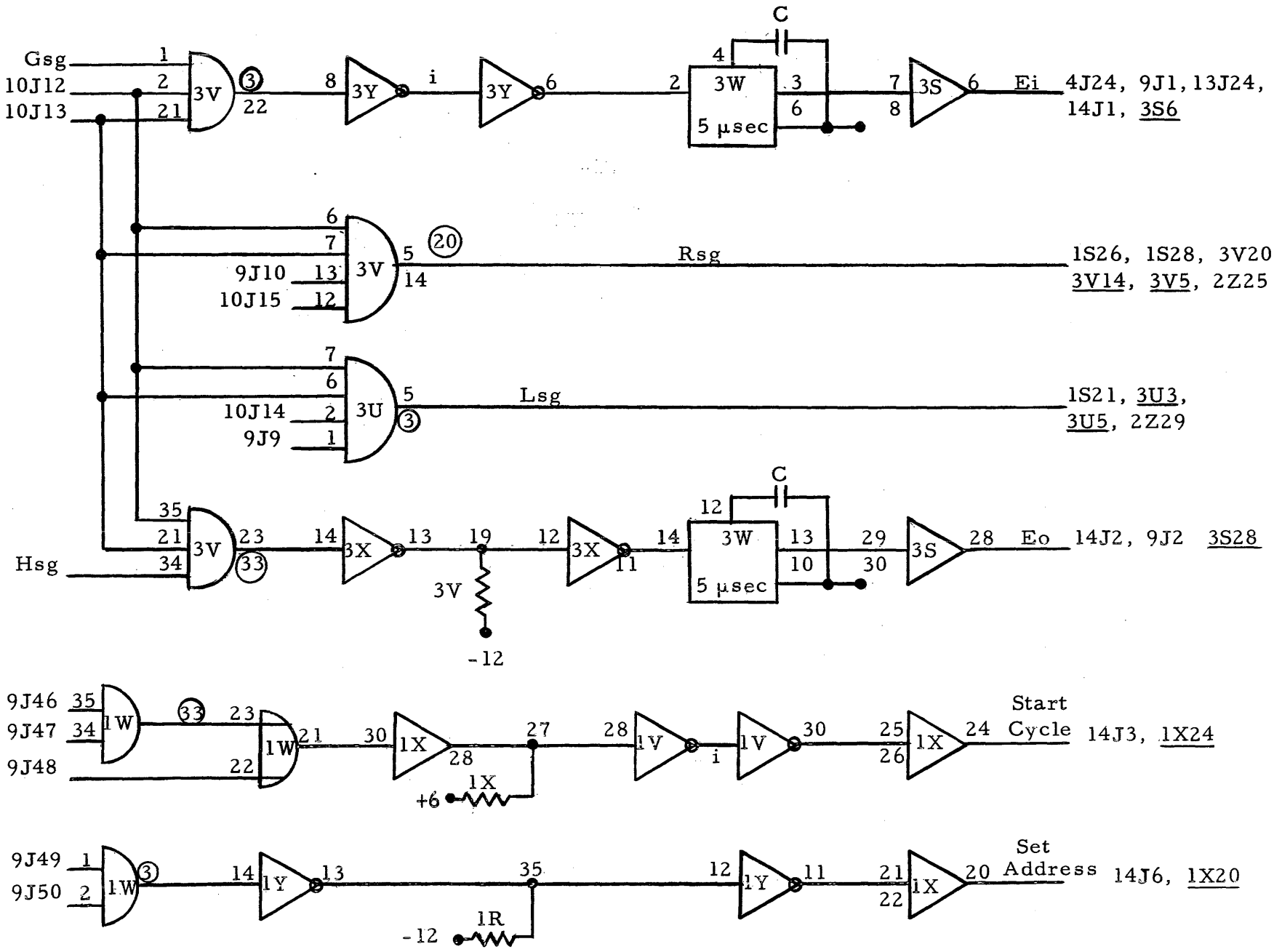

6J1
Cj
6J1, 1S10

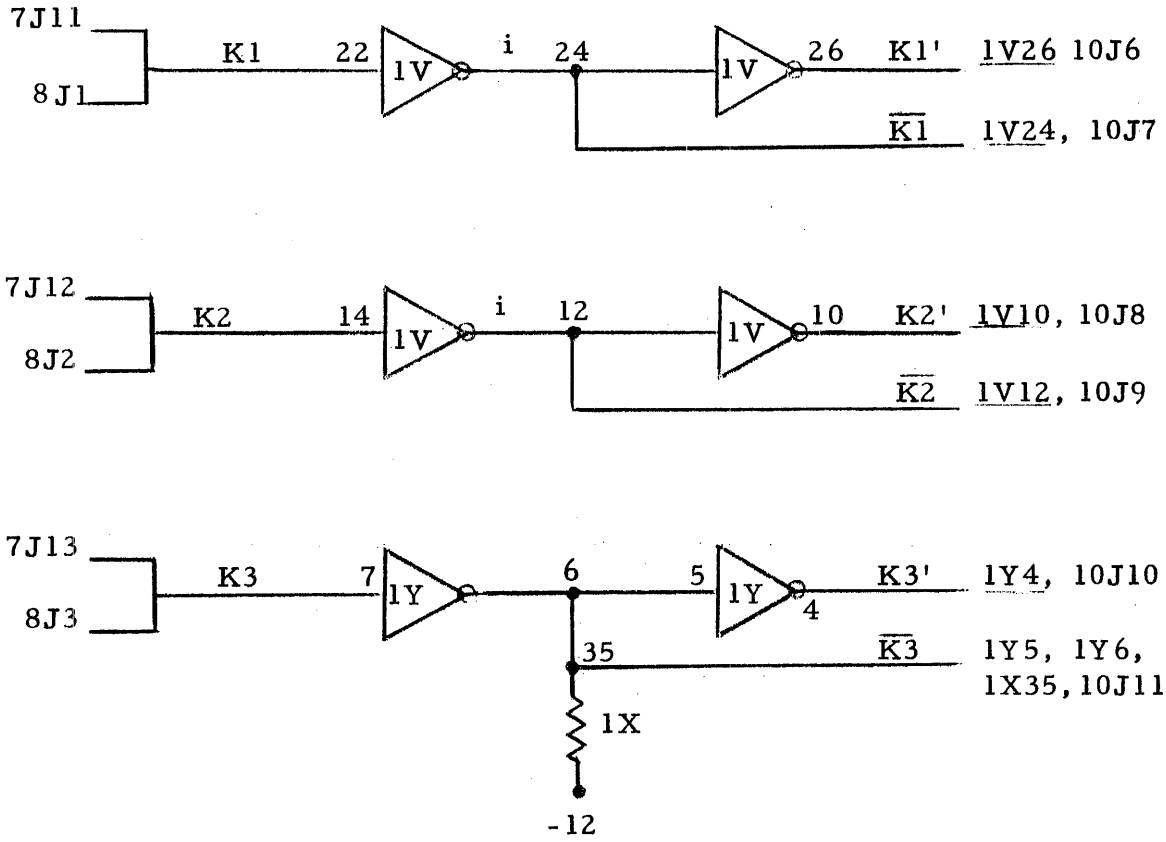

7J1
Gsg
1S30, 1S2, 3V1, 2Z2, 2A7, 7J1
2
7J3
Gdg
1
2Z
3
16
(Gdg Gsg)
2B20, 2C17, 2D17, 2E17, 2F17, 2G17, 2H17, 2J17, 2K17, 2L17, 2M17, 2N17, 2Θ17, 2P17, 2R17, 2S17, 2T17, 2U17, 2V17, 2W17, 2X17, 2Y17, 2Y11, 2Z3, 3X10, 3U16
3U
-12
10
3X
9
(Gdg Gsg)
2C21, 2D21, 2E21, 2F21, 2G21, 2H21, 2J21, 2K21, 2L21, 2M21, 2N21, 2Θ21, 2P21, 2R21, 2S21, 2T21, 2U21, 2V21, 2W21, 2X21, 2Y21, 2Y10, 3X9
10
1Y
9
Gdg
1Y9, 2A8

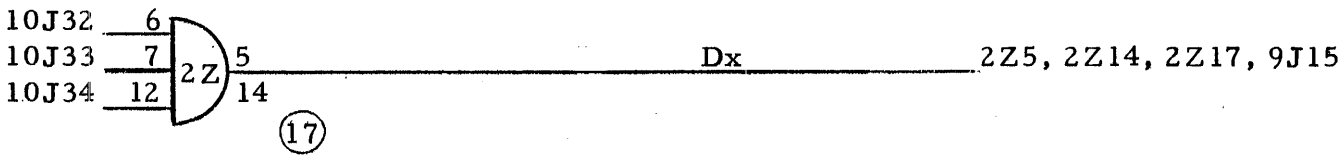

7J7
Hsg
34
2Z
7J7, 2Z34,
3V34, 1S35,
1S24, 2B22

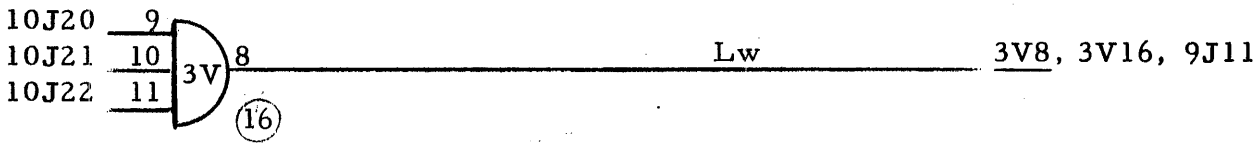

+6
1X
B44
Rsg
24
25
26
2Z
27
19
8
1X
7
5
8
1V
i
1V
6
15
16
1X
14
Hdg
7J9, 1X14,
BI
Lsg
30
29
28
2Z
31
20
12
1X
11

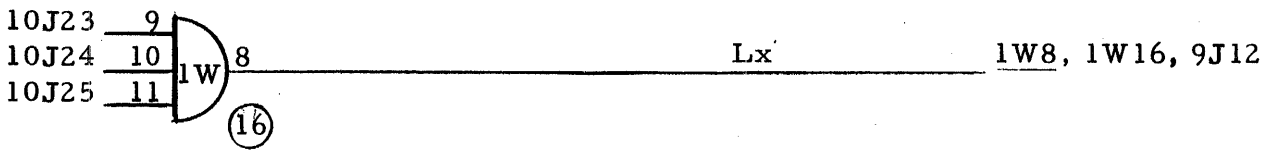

7J5
7J4
6
17
19
XCG100
1Z
14
15
5
1S1, 1S25, 1S29, 1S34,
1Z14
9J38

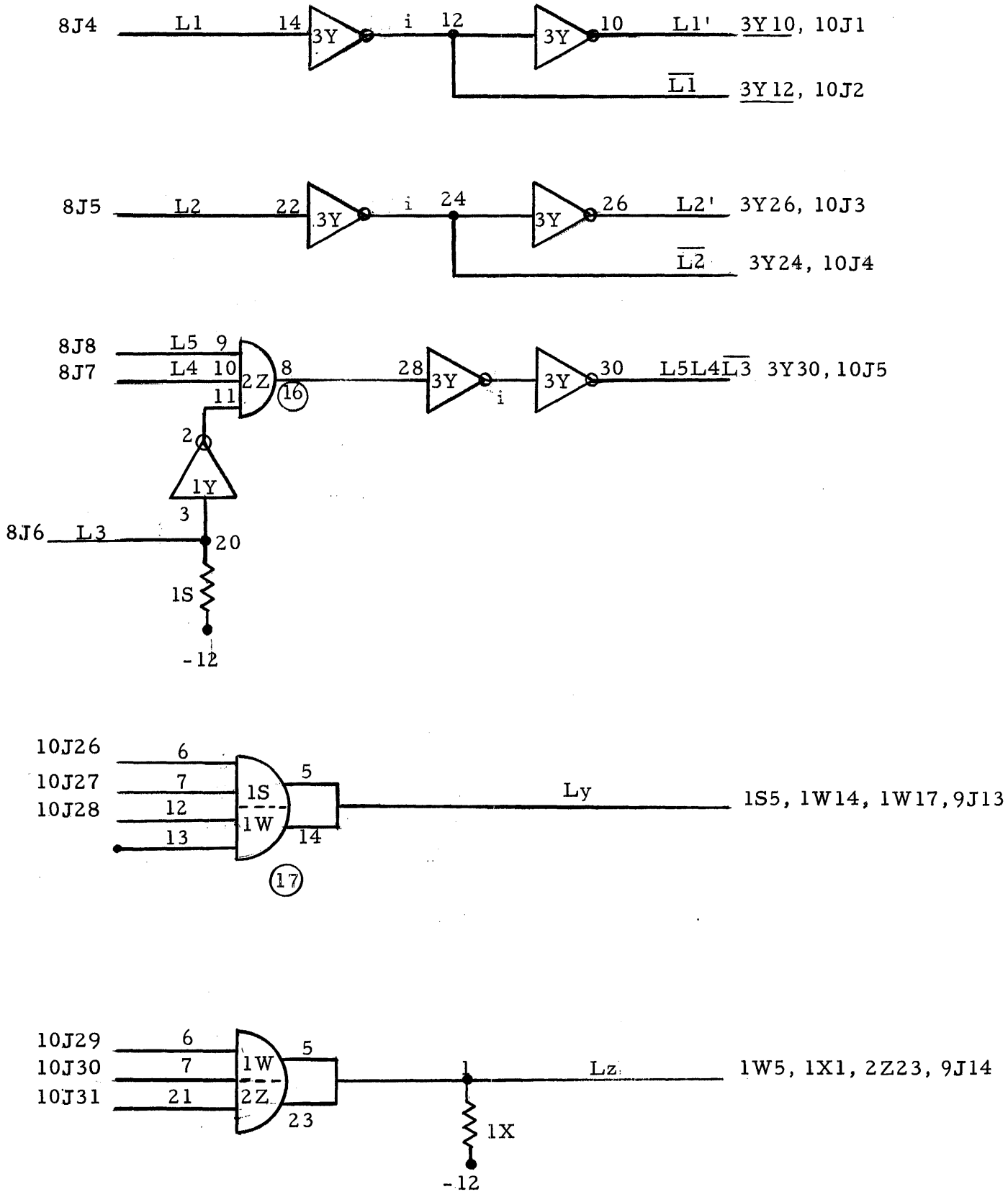

Gsg
10J12
10J13
3V
3Y
3Y
i
C
3W
5 µsec
3S
Ei
4J24, 9J1, 13J24,
14J1, 3S6
9J10
10J15
3V
Rsg
1S26, 1S28, 3V20,
3V14, 3V5, 2Z25
10J14
9J9
3U
Lsg
1S21, 3U3,
3U5, 2Z29
Hsg
3V
3X
3X
3V
-12
C
3W
5 µsec
3S
Eo
14J2, 9J2 3S28
9J46
9J47
9J48
1W
1W
1X
1X
+6
1V
1V
i
1X
Start
Cycle
14J3, 1X24
9J49
9J50
1W
1Y
1Y
-12
1R
1X
Set
Address
14J6, 1X20

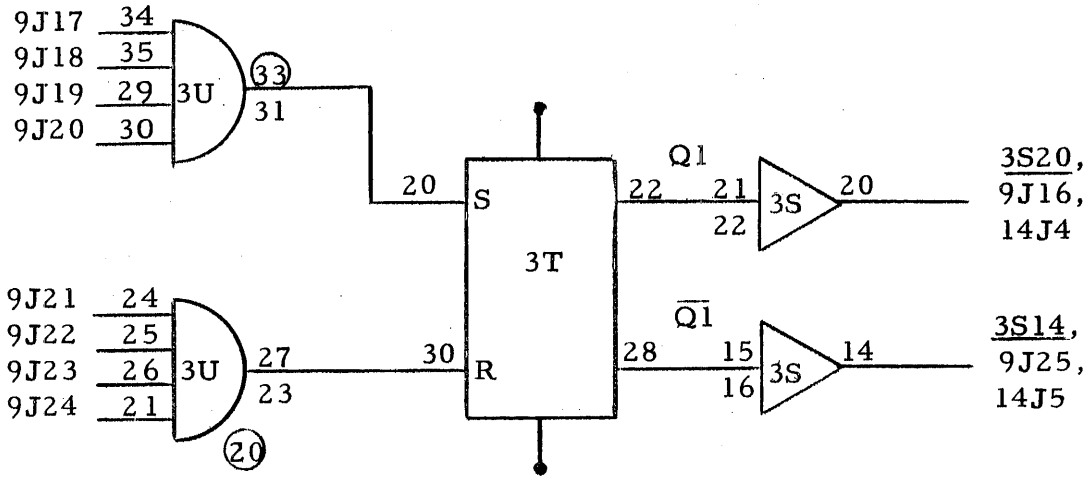

7J11
8J1
K1
22
1V
i
24
1V
26
K1'
1V26 10J6
K1
1V24, 10J7
7J12
8J2
K2
14
1V
i
12
1V
10
K2'
1V10, 10J8
K2
1V12, 10J9
7J13
8J3
K3
7
1Y
6
5
1Y
4
K3'
1Y4, 10J10
35
K3
1Y5, 1Y6,
1X35, 10J11
1X
-12

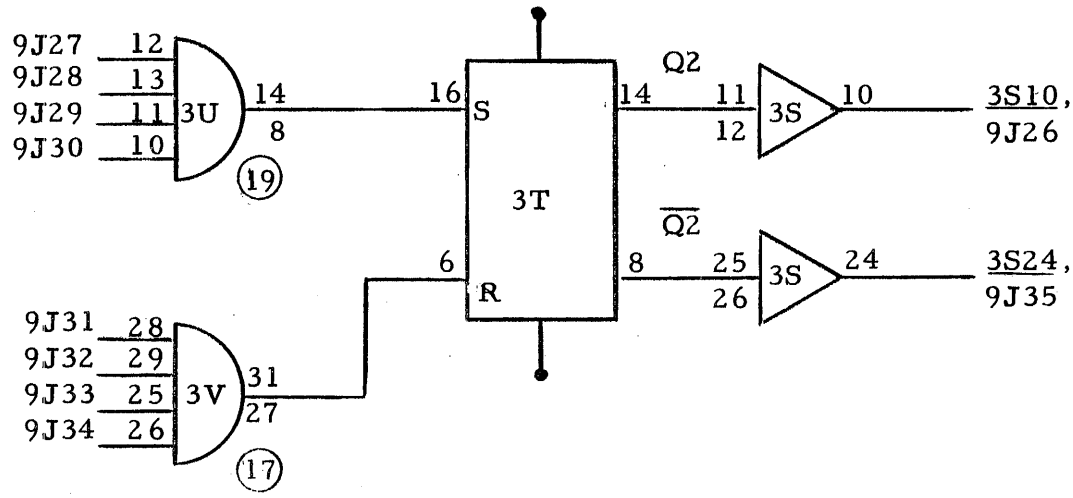

10J32
10J33
10J34
6
7
12
2Z
5
14
Dx
2Z5, 2Z14, 2Z17, 9J15
17

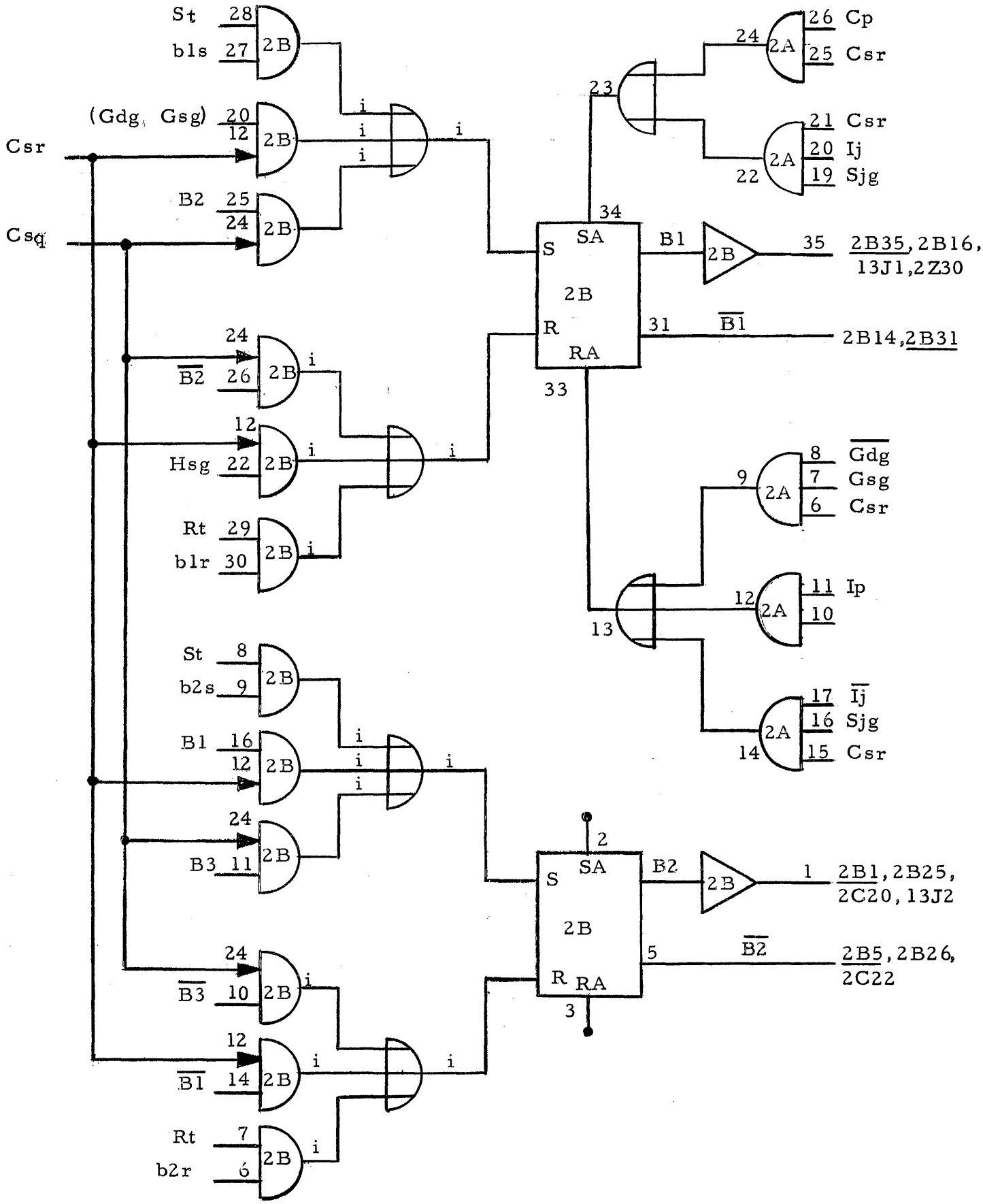

10J20
10J21
10J22
9
10
11
3V
8
Lw
3V8, 3V16, 9J11
16

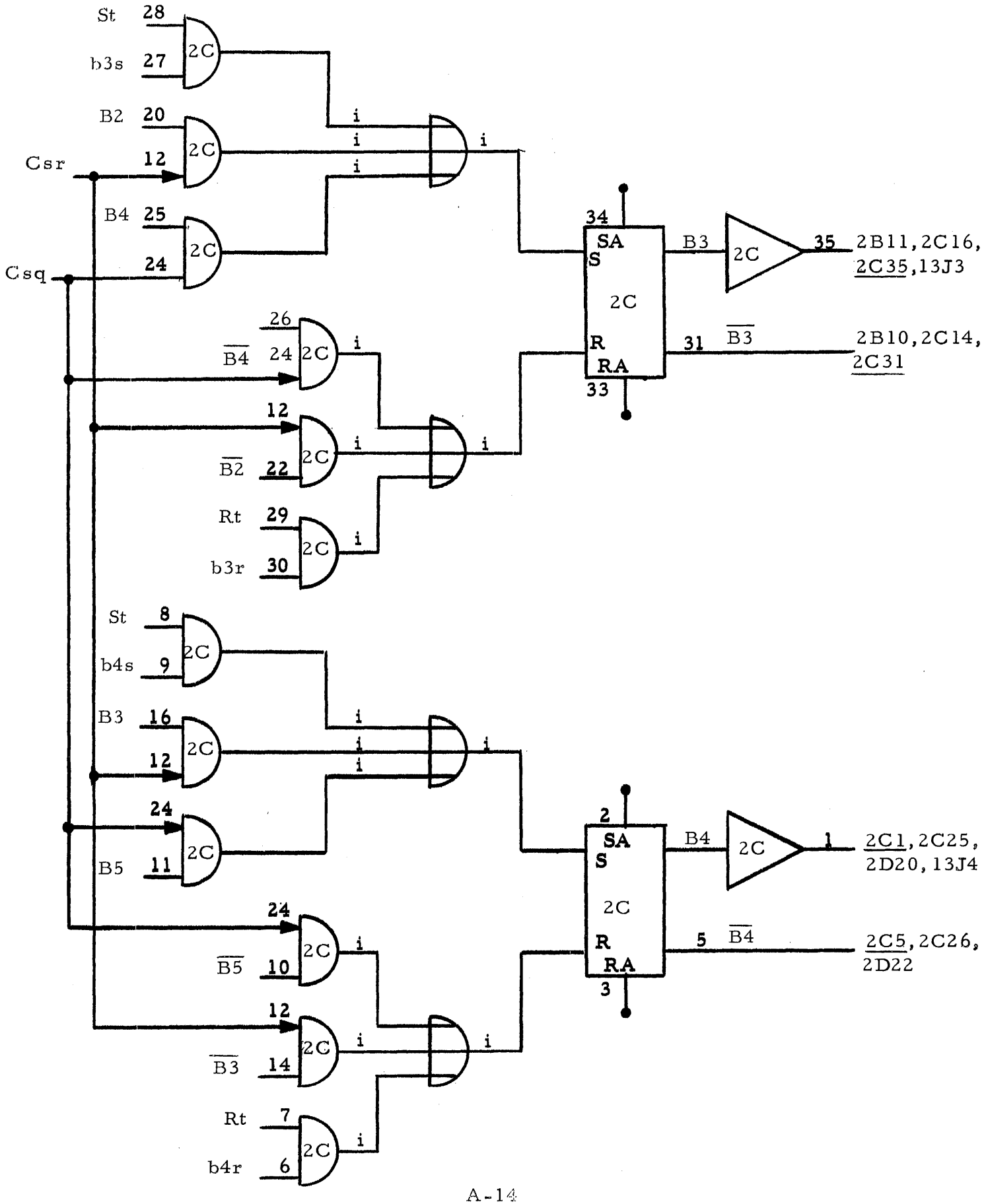

10J23
10J24
10J25
9
10
11
1W
8
Lx
1W8, 1W16, 9J12
16

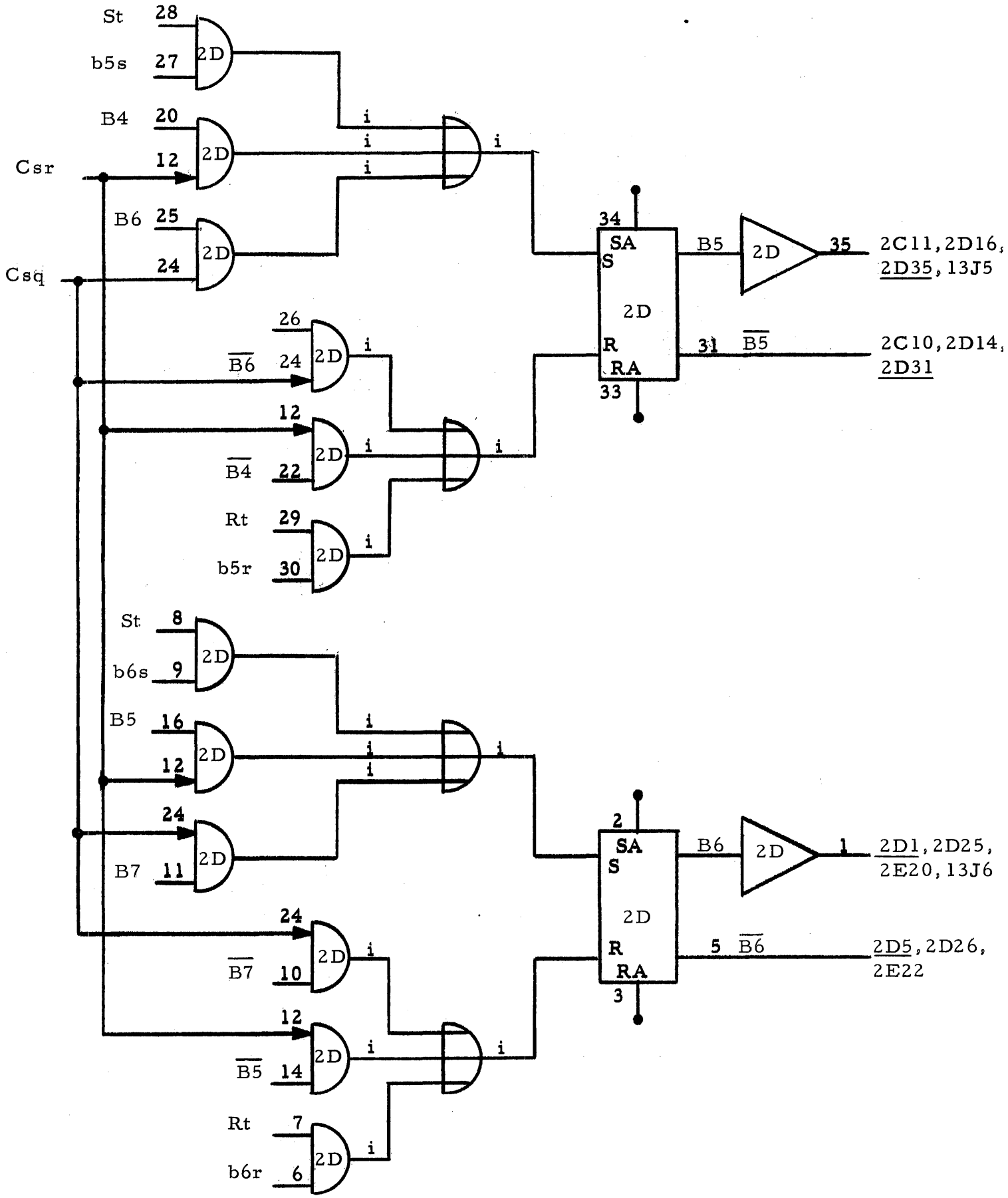

8J4
L1
14
3Y
i
12
3Y
10
L1'
3Y10, 10J1
L1
3Y12, 10J2
8J5
L2
22
3Y
i
24
3Y
26
L2'
3Y26, 10J3
L2
3Y24, 10J4
8J8
8J7
L5 9
L4 10
11
2Z
8
16
28
3Y
i
3Y
30
L5L4L3
3Y30, 10J5
2
1Y
3
8J6
L3
20
1S
-12
10J26
10J27
10J28
6
7
12
13
1S
1W
5
14
17
Ly
1S5, 1W14, 1W17, 9J13
10J29
10J30
10J31
6
7
21
1W
2Z
5
23
1
Lz
1W5, 1X1, 2Z23, 9J14
1X
-12

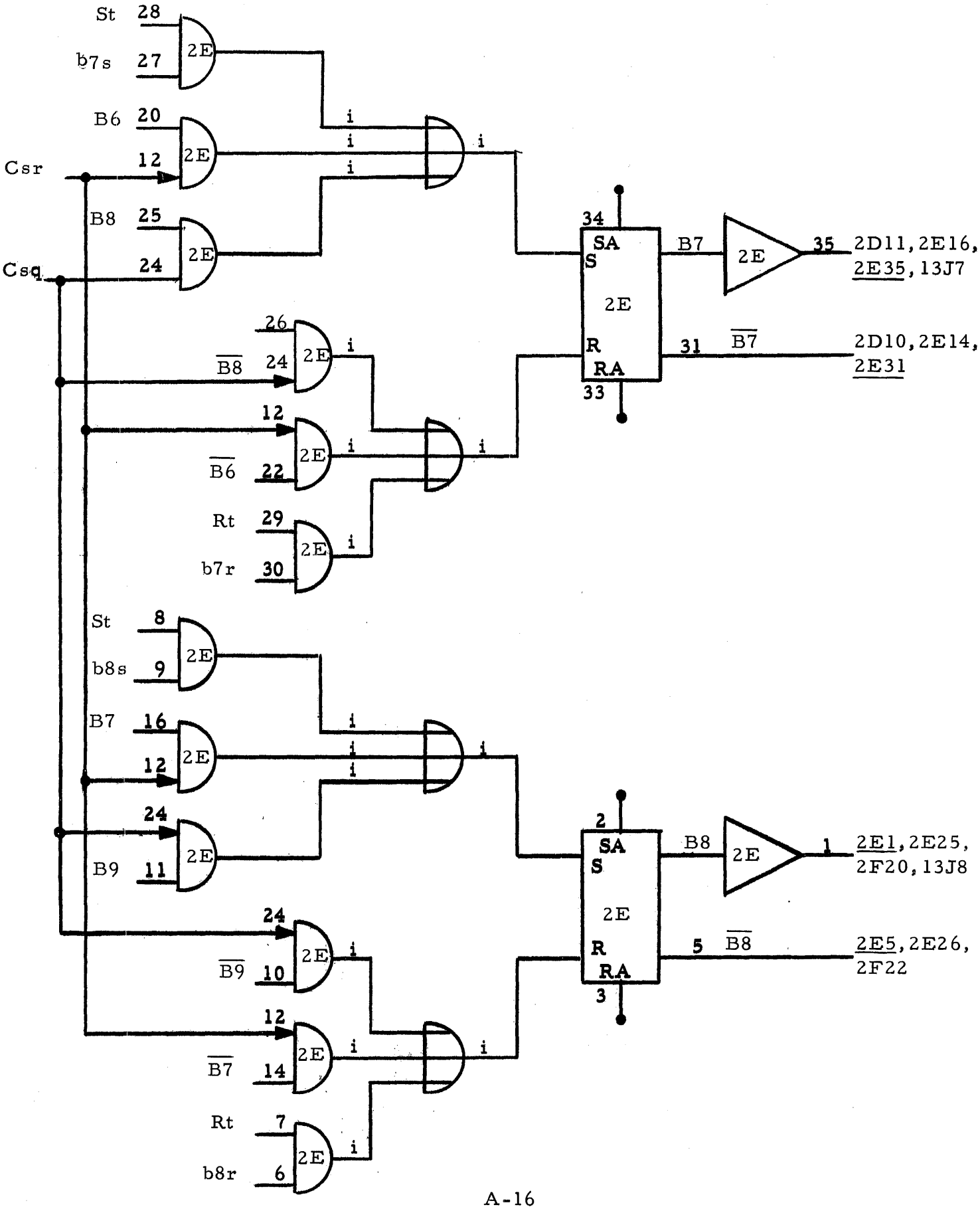

9J17 34
9J18 35
9J19 29
9J20 30
3U
33
31
20
S
3T
Q1
22
21
22
3S
20
3S20,
9J16,
14J4
9J21 24
9J22 25
9J23 26
9J24 21
3U
27
23
20
30
R
$\overline{Q1}$
28
15
16
3S
14
3S14,
9J25,
14J5

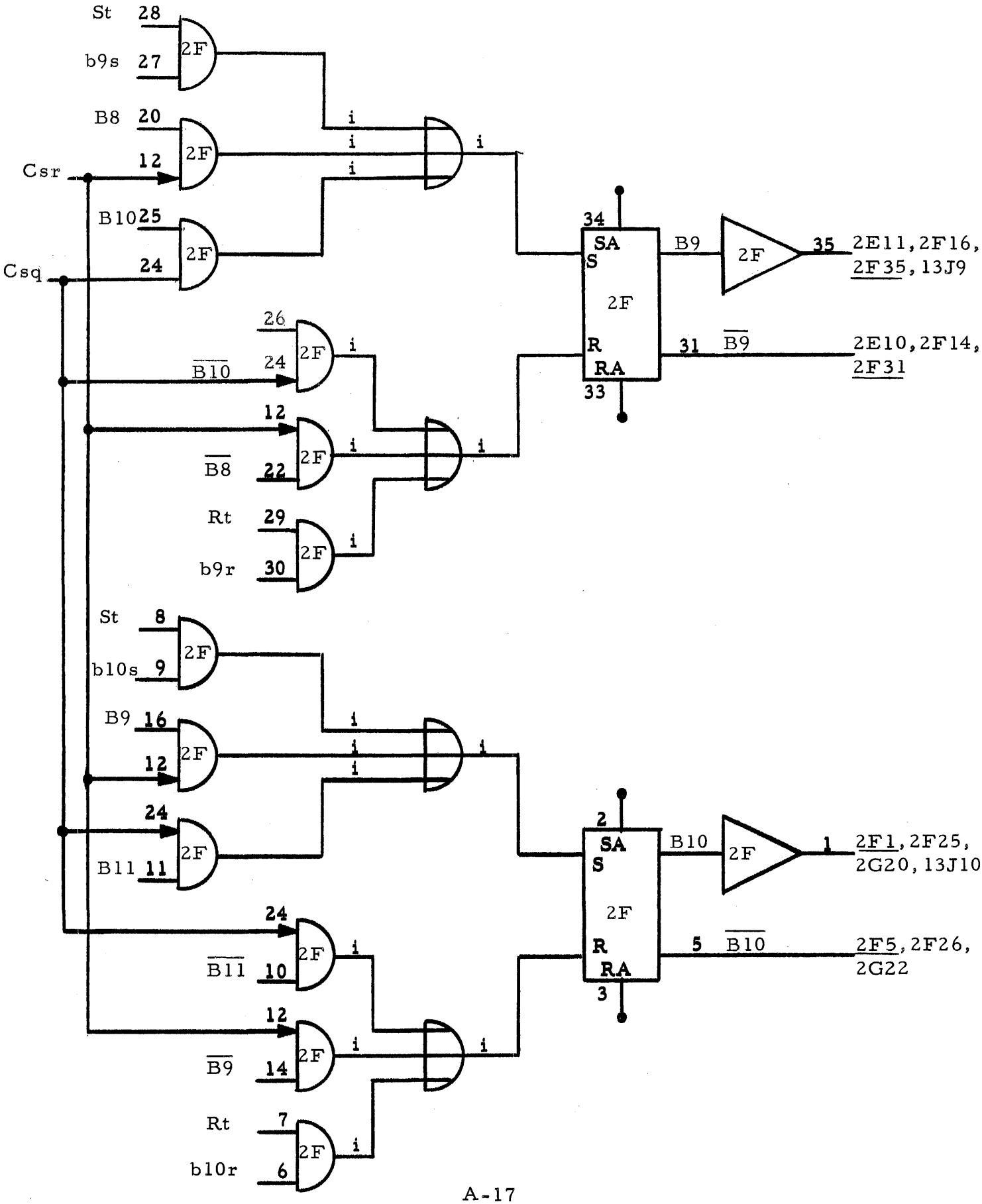

9J27 12
9J28 13
9J29 11
9J30 10
3U
14
8
19
16
S
3T
Q2
14
11
12
3S
10
3S10,
9J26
6
R
$\overline{Q2}$
8
25
26
3S
24
3S24,
9J35
9J31 28
9J32 29
9J33 25
9J34 26
3V
31
27
17

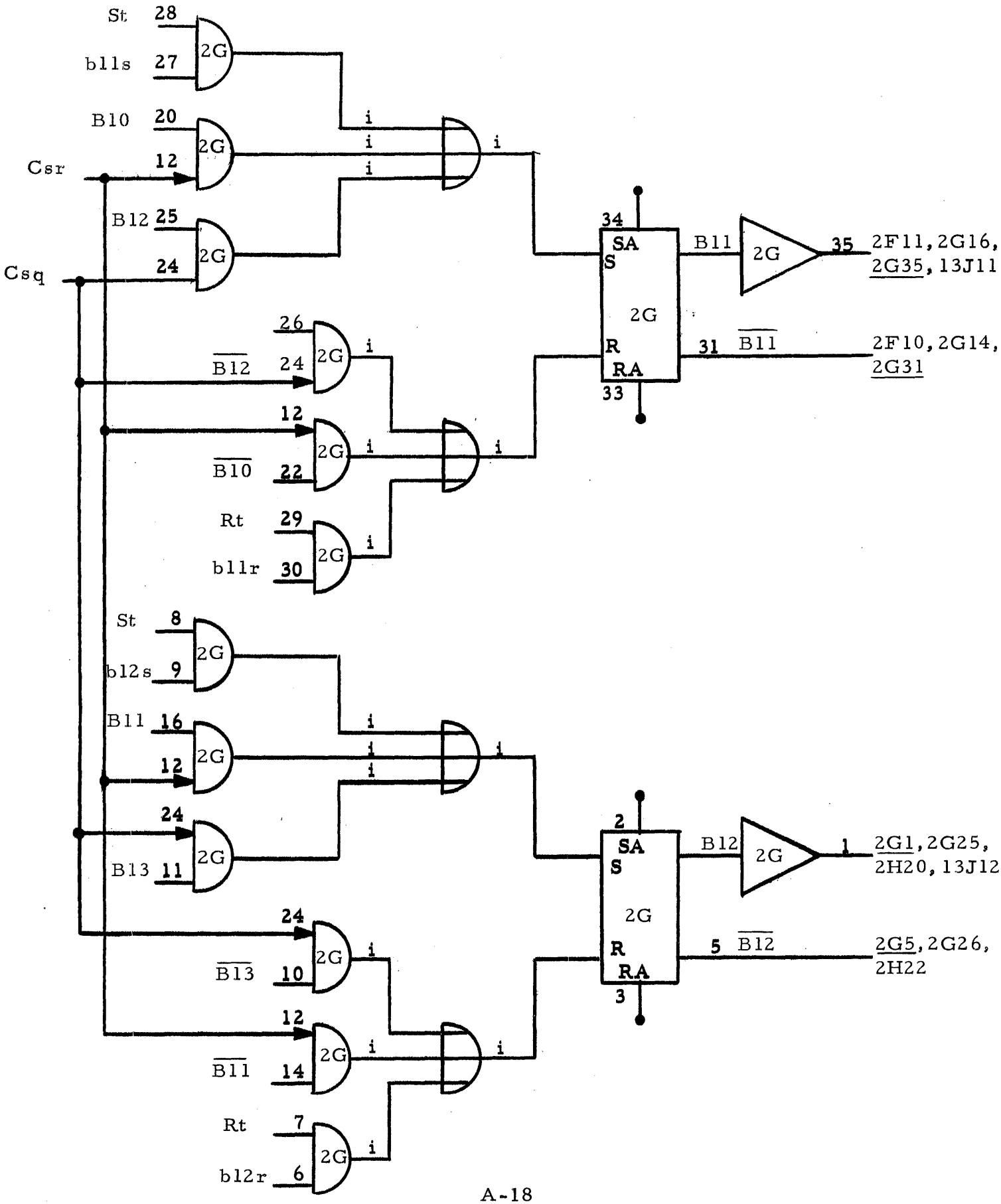

St
bls
(Gdg, Gsg)
Csr
Csq
B2
Hsg
Rt
blr
St
b2s
B1
B3
B1
Rt
b2r
2B
i
SA
S
2B
R
RA
34
33
2
3
B1
B2
2A
Cp
Csr
Ij
Sjg
Gdg
Gsg
Ip
Ij
2B35, 2B16, 13J1, 2Z30
2B14, 2B31
2B1, 2B25, 2C20, 13J2
2B5, 2B26, 2C22

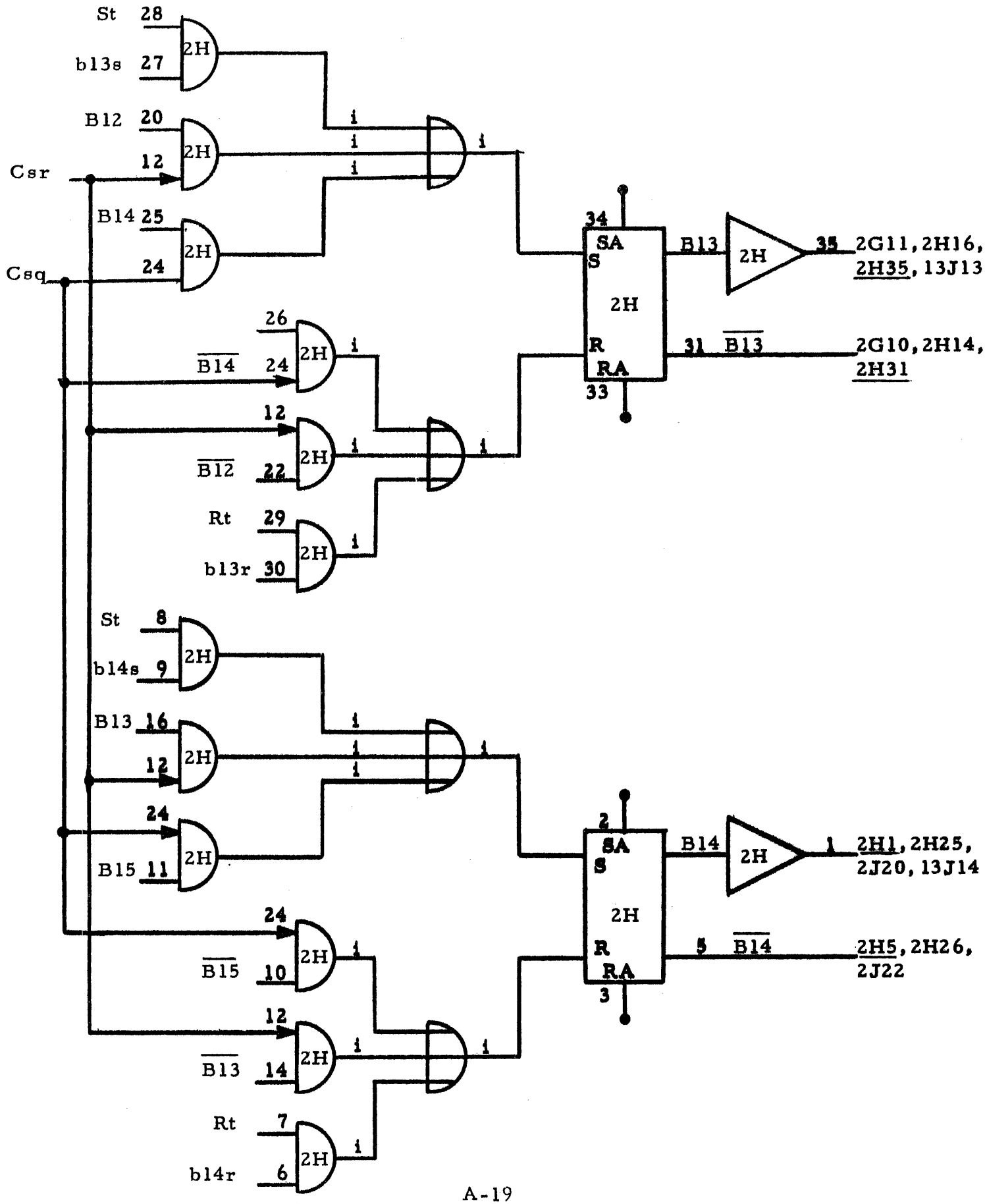

St
28
b3s
27
2C
B2
20
Csr
12
B4
25
Csq
24
i
34
SA
S
2C
R
RA
33
B3
35
2B11,2C16,
2C35,13J3
31
B3
2B10,2C14,
2C31
26
B4
24
12
B2
22
Rt
29
b3r
30
St
8
b4s
9
B3
16
12
24
B5
11
2
2C1,2C25,
2D20,13J4
5
B4
2C5,2C26,
2D22
10
14
7
b4r
6

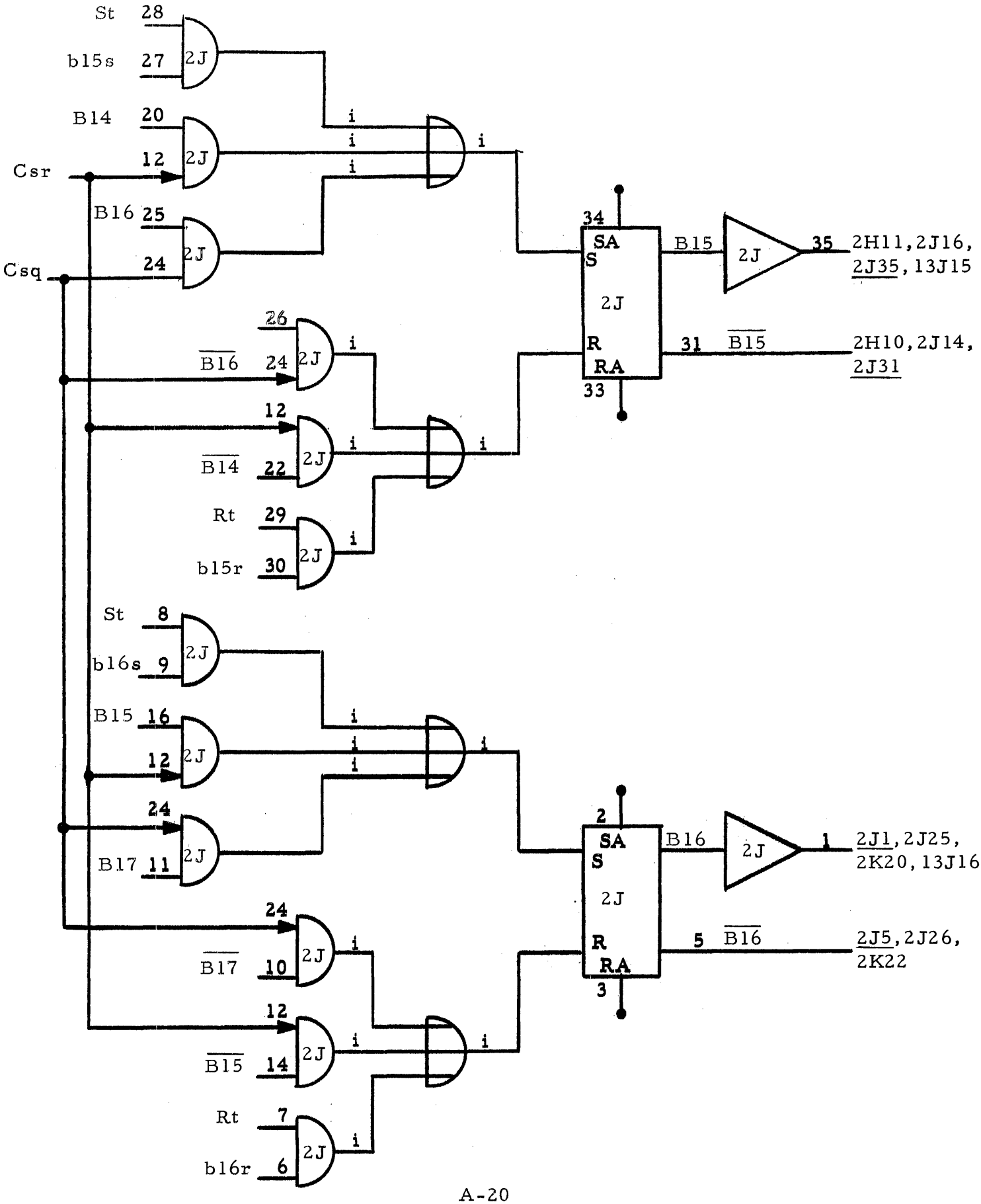

St
28
b5s
27
2D
B4
20
Csr
12
B6
25
Csq
24
i
34
SA
S
2D
R
RA
33
B5
35
31
B5
2C11,2D16,
2D35,13J5
2C10,2D14,
2D31
26
B6
24
12
B4
22
Rt
29
b5r
30
St
8
b6s
9
B5
16
12
24
B7
11
2
1
2D1,2D25,
2E20,13J6
5
B6
2D5,2D26,
2E22
B7
10
B5
14
Rt
7
b6r
6

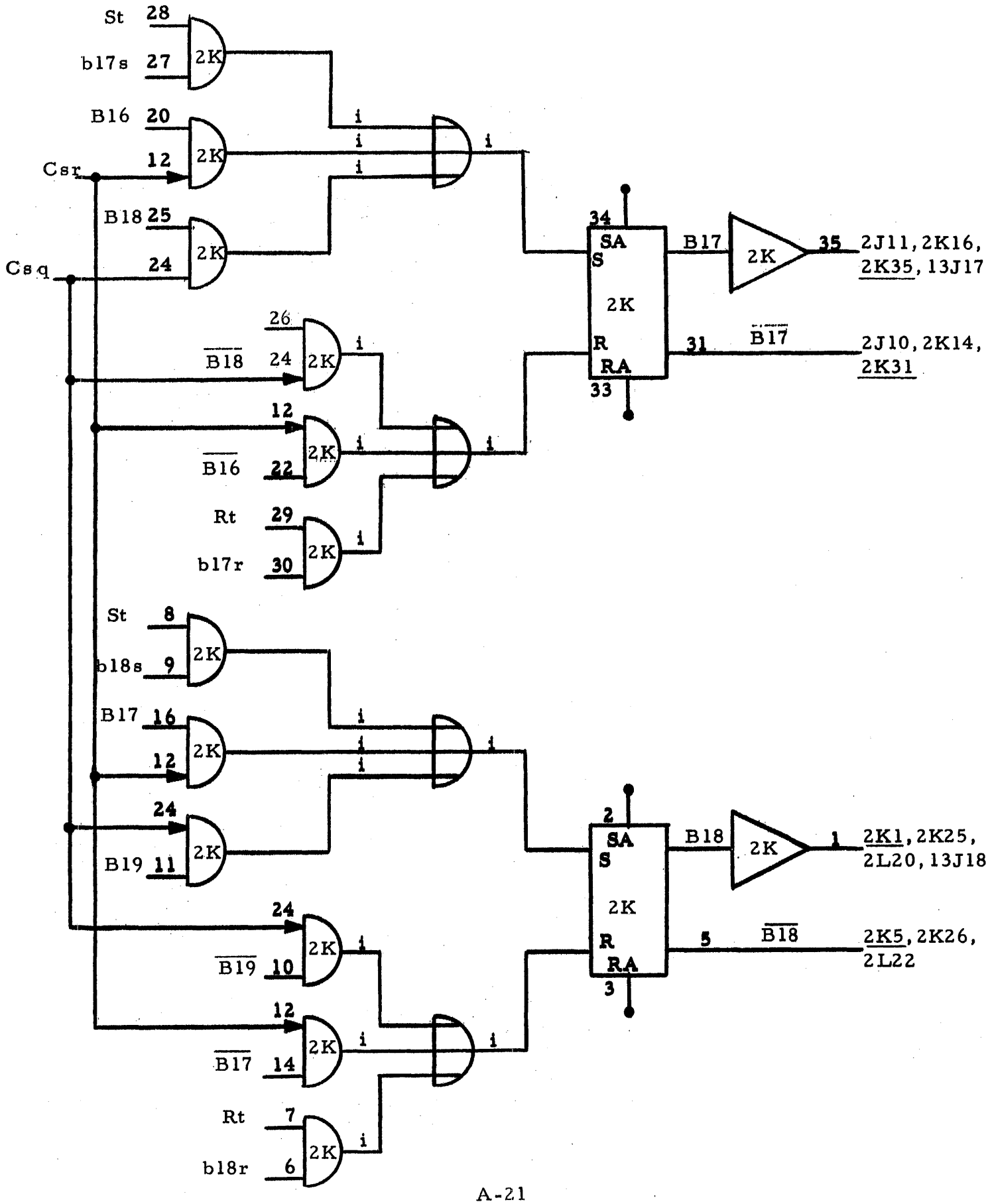

St
28
b7s
27
2E
B6
20
12
Csr
B8
25
24
Csq
i
i
i
i
34
SA
S
2E
R
RA
33
B7
2E
35
2D11,2E16,
2E35,13J7
31
B7
2D10,2E14,
2E31
26
B8
24
12
B6
22
Rt
29
b7r
30
St
8
b8s
9
B7
16
12
24
B9
11
2
B8
1
2E1,2E25,
2F20,13J8
5
B8
2E5,2E26,
2F22
3
24
B9
10
12
B7
14
Rt
7
b8r
6

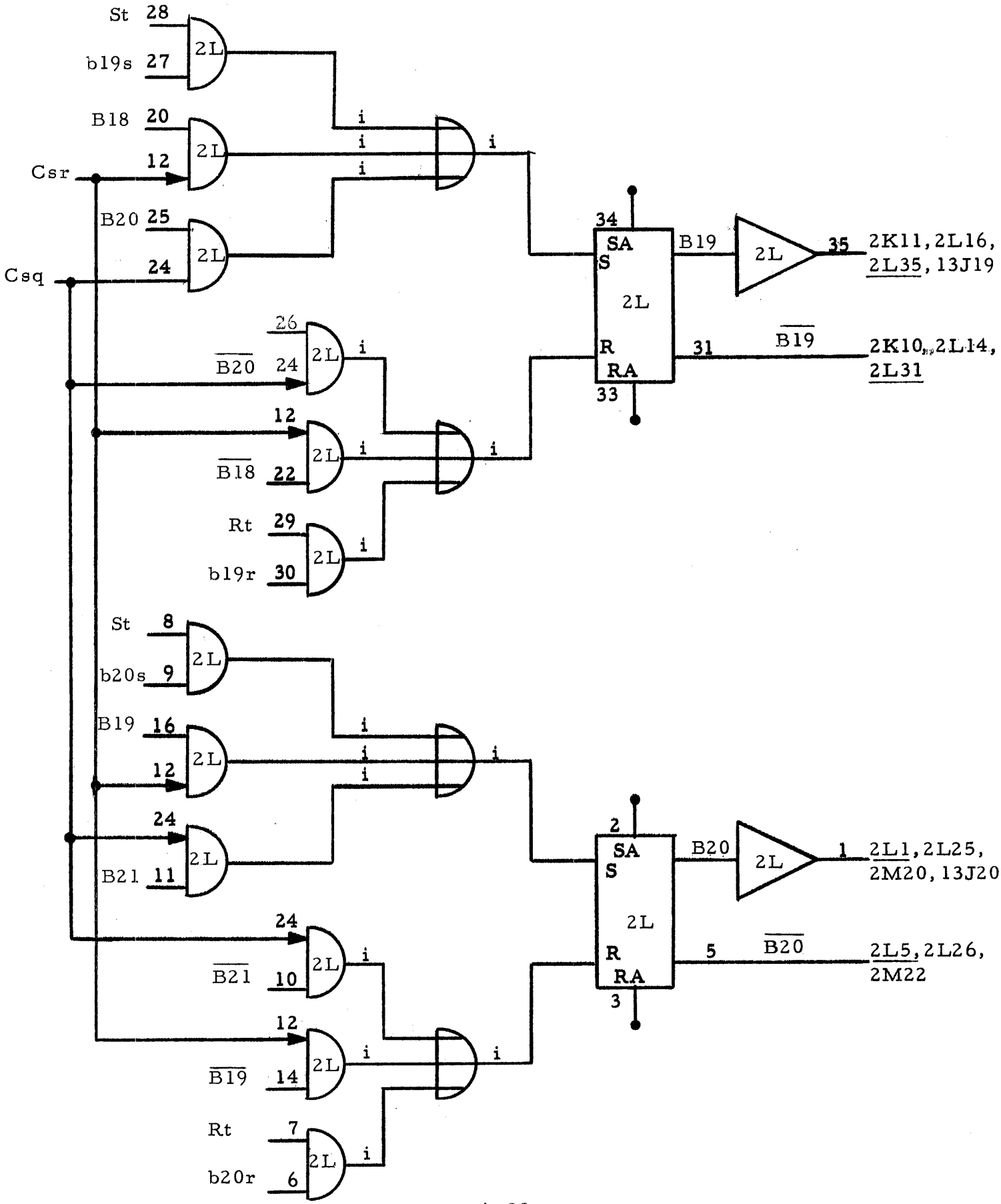

St 28
b9s 27
B8 20
12
Csr
B10 25
24
Csq
2F
i
26
24
B10
12
B8 22
Rt 29
b9r 30
34
SA
S
2F
R
RA
33
B9
35
2E11,2F16,
2F35,13J9
31 B9
2E10,2F14,
2F31
St 8
b10s 9
B9 16
12
24
B11 11
2
5 B10
1
2F1,2F25,
2G20,13J10
2G22
3
B9 14
Rt 7
b10r 6

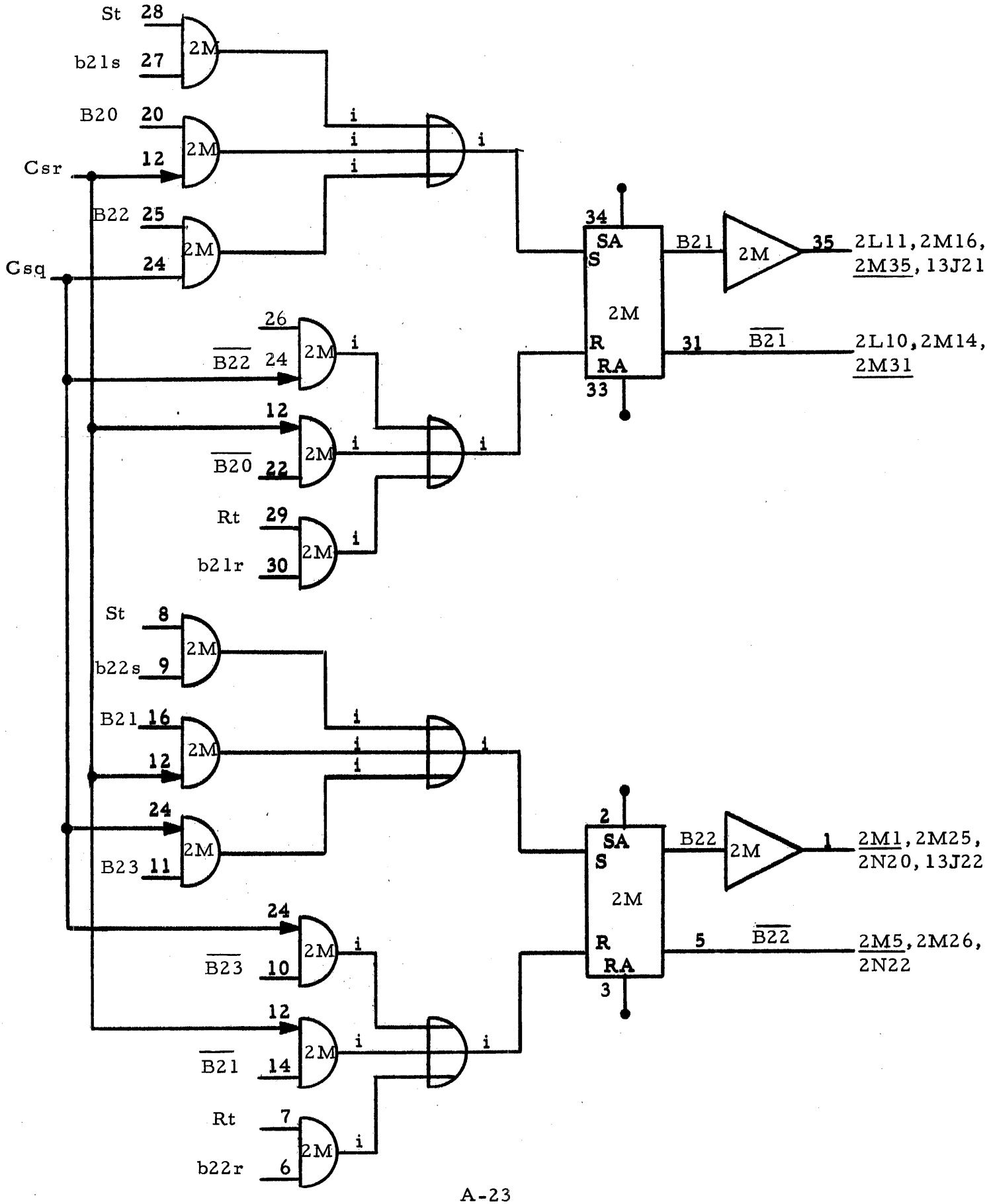

St 28
b11s 27
B10 20
Csr 12
B12 25
Csq 24
2G
i
34
SA
S
2G
R
RA
33
B11
35
2F11, 2G16, 2G35, 13J11
31 B11
2F10, 2G14, 2G31
26
B12 24
12
B10 22
Rt 29
b11r 30
St 8
b12s 9
B11 16
12
24
B13 11
2
B12
1
2G1, 2G25, 2H20, 13J12
5 B12
2G5, 2G26, 2H22
B13 10
B11 14
Rt 7
b12r 6
A-18

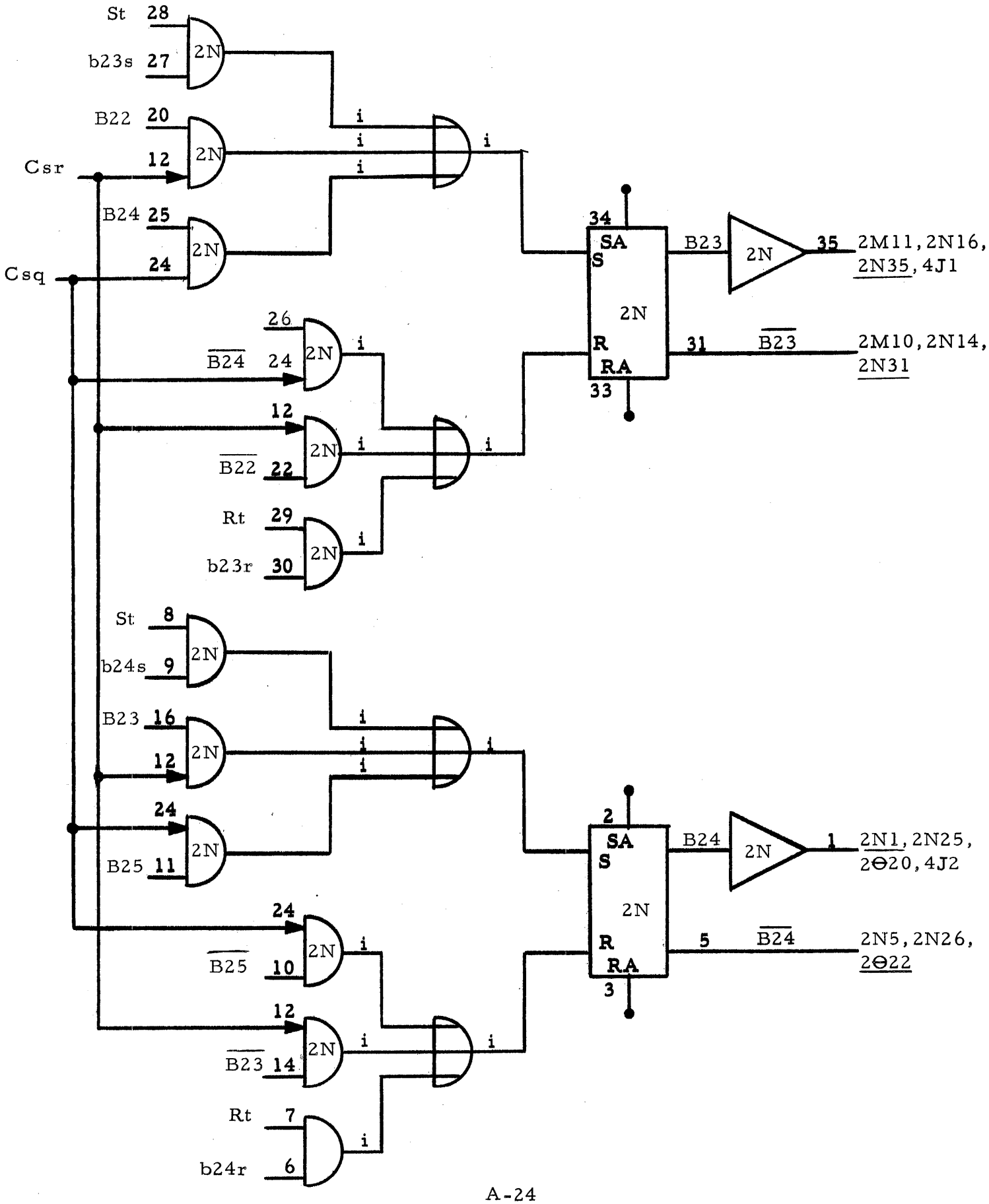

St 28
b13s 27
B12 20
12
Csr
B14 25
24
Csq
2H
i
26
B14 24
12
B12 22
Rt 29
b13r 30
St 8
b14s 9
B13 16
12
24
B15 11
24
B15 10
12
B13 14
Rt 7
b14r 6
34
SA
S
2H
R
RA
33
B13
35
2G11, 2H16, 2H35, 13J13
31 B13
2G10, 2H14, 2H31
2
B14
1
2H1, 2H25, 2J20, 13J14
5 B14
2H5, 2H26, 2J22
3

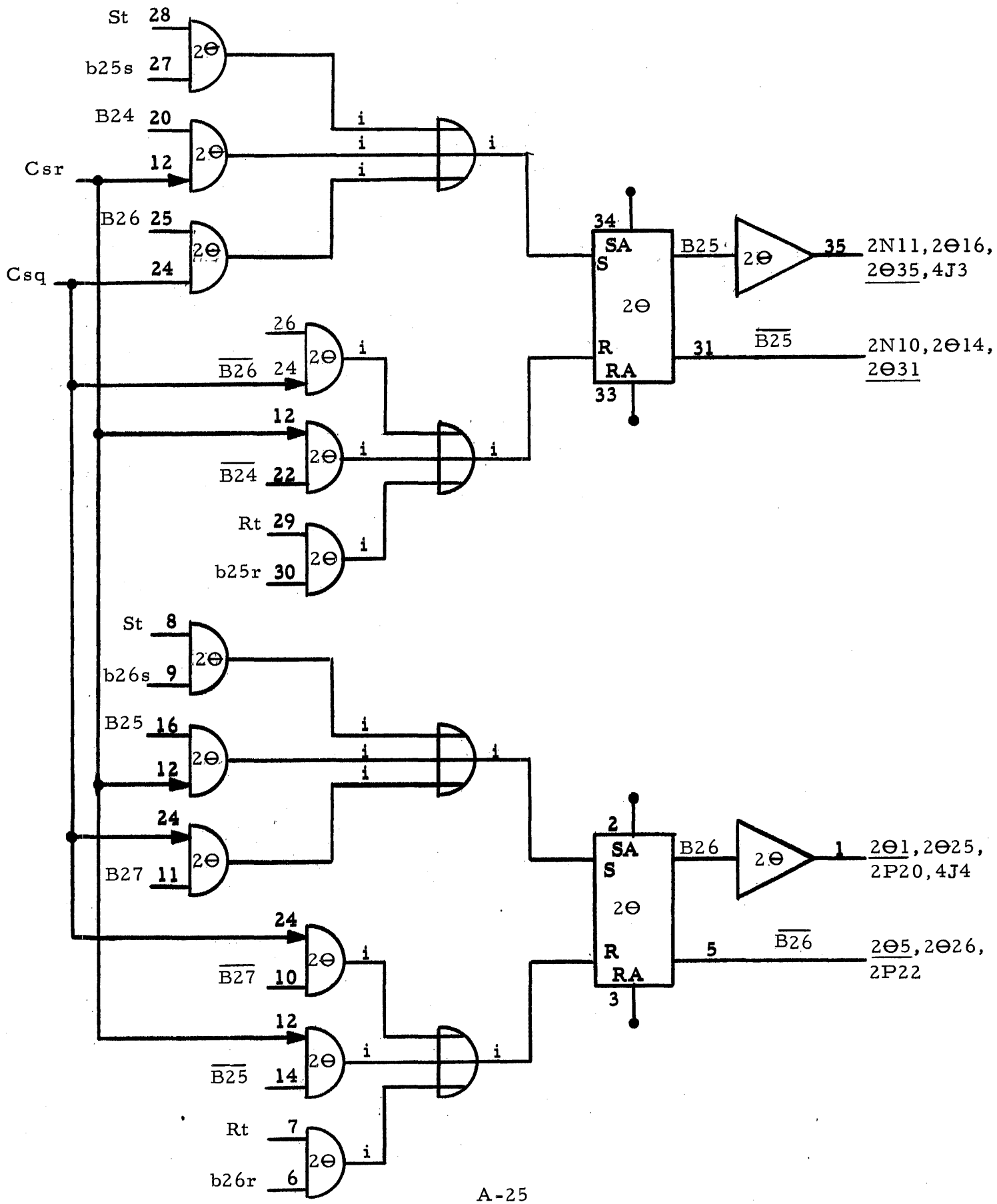

St
28
b15s
27
2J
B14
20
12
2J
Csr
B16
25
24
2J
Csq
i
i
i
i
34
SA
S
2J
R
RA
33
B15
2J
35
2H11,2J16,
2J35,13J15
31
B15
2H10,2J14,
2J31
26
B16
24
2J
12
B14
22
2J
Rt
29
b15r
30
2J
St
8
b16s
9
2J
B15
16
12
2J
24
B17
11
2J
2
SA
S
2J
R
RA
3
B16
2J
1
2J1,2J25,
2K20,13J16
5
B16
2J5,2J26,
2K22
24
B17
10
2J
12
B15
14
2J
Rt
7
b16r
6
2J

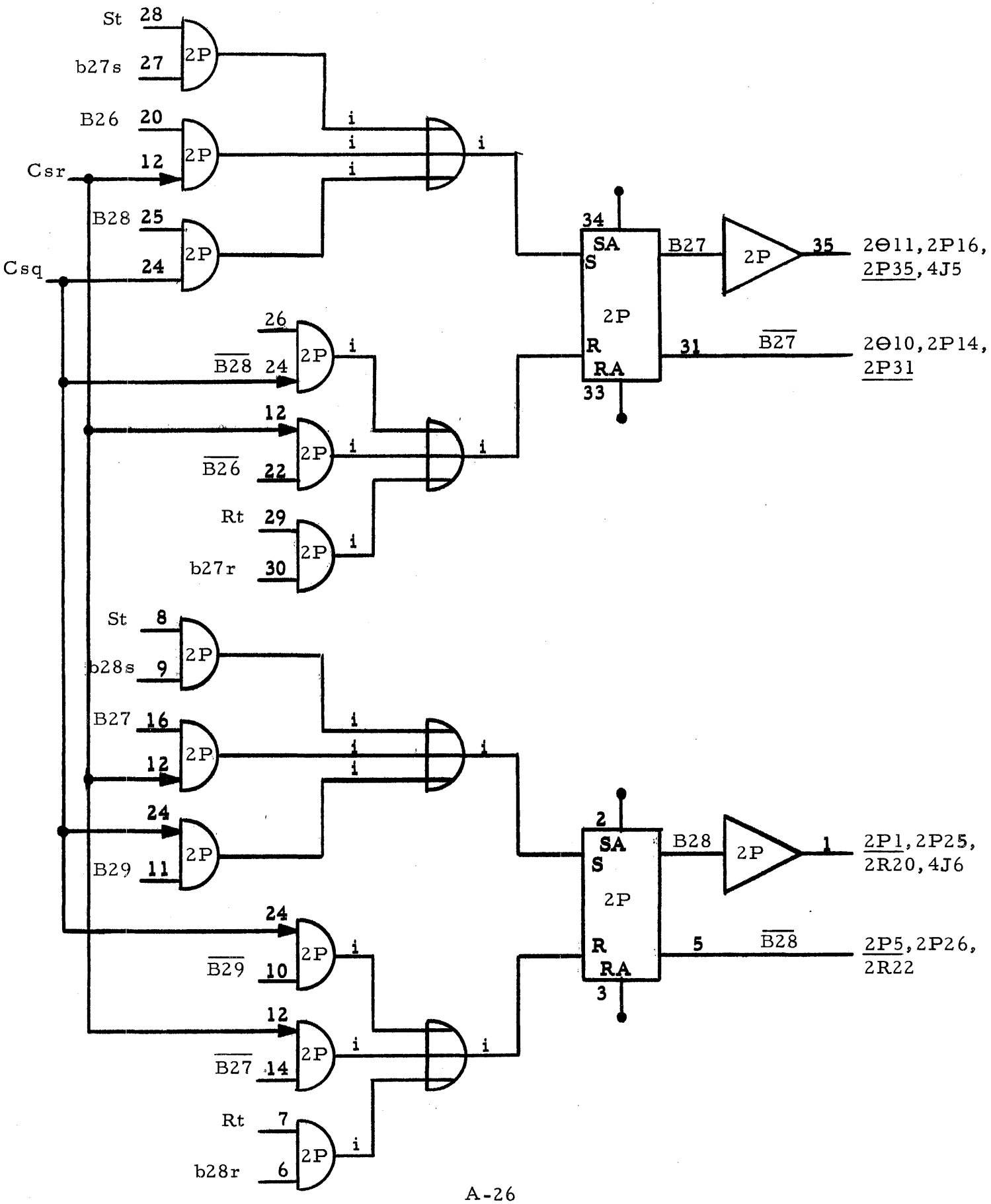

St 28
b17s 27
2K
B16 20
12
Csr
B18 25
24
Csq
i
34
SA
S
2K
R
RA
33
B17
35
2J11, 2K16,
2K35, 13J17
31
B17
2J10, 2K14,
2K31
26
B18 24
12
B16 22
Rt 29
b17r 30
St 8
b18s 9
B17 16
12
24
B19 11
2
1
2K1, 2K25,
2L20, 13J18
5
B18
2K5, 2K26,
2L22
3
24
B19 10
12
B17 14
Rt 7
b18r 6

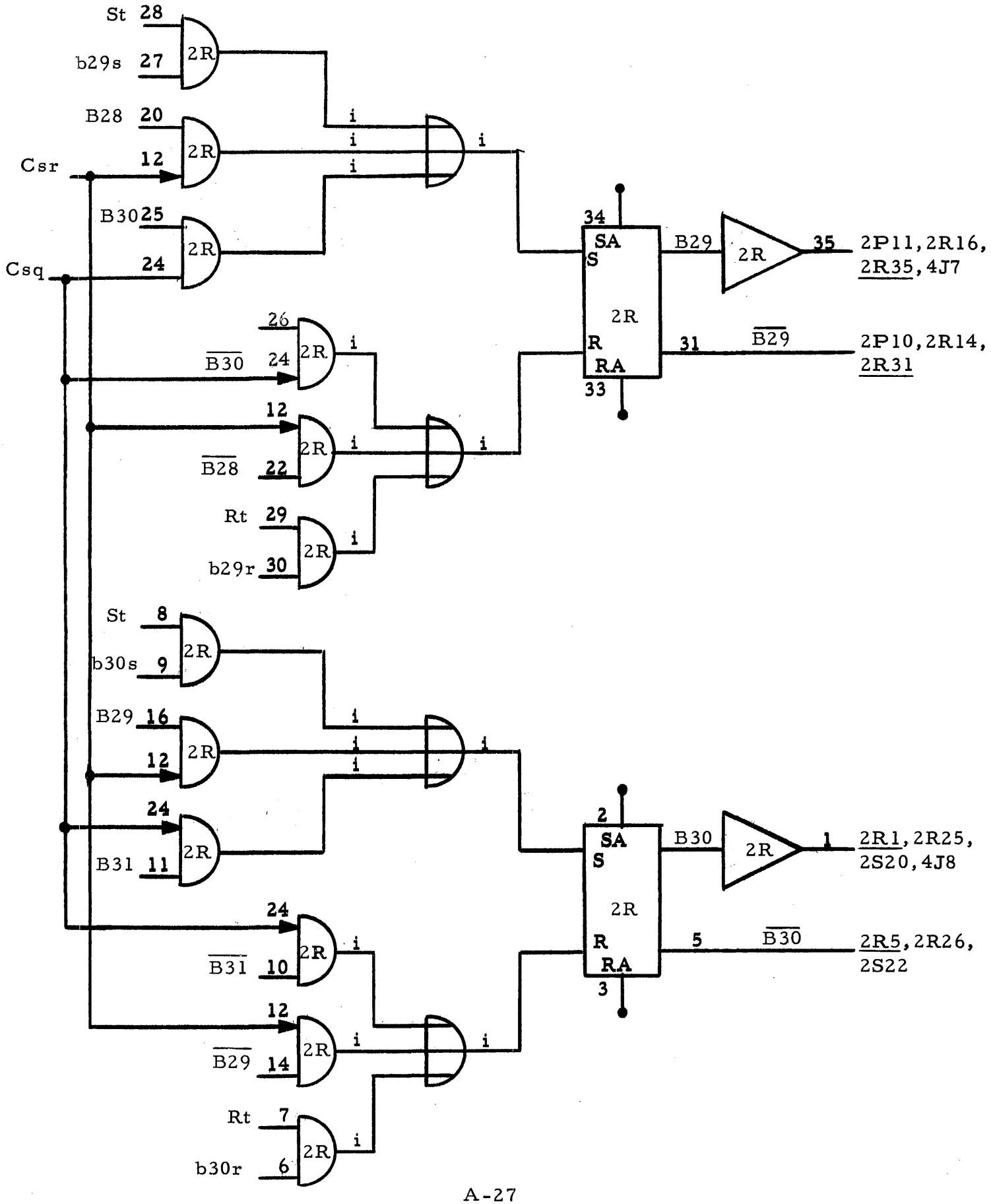

St 28
b19s 27
2L
B18 20
Csr 12
B20 25
Csq 24
i
34
SA
S
2L
R
RA
33
B19
35
2K11, 2L16,
2L35, 13J19
31
B19
2K10, 2L14,
2L31
26
B20 24
12
B18 22
Rt 29
b19r 30
St 8
b20s 9
B19 16
12
24
B21 11
2
B20
1
2L1, 2L25,
2M20, 13J20
5
B20
2L5, 2L26,
2M22
3
B21 10
B19 14
Rt 7
b20r 6

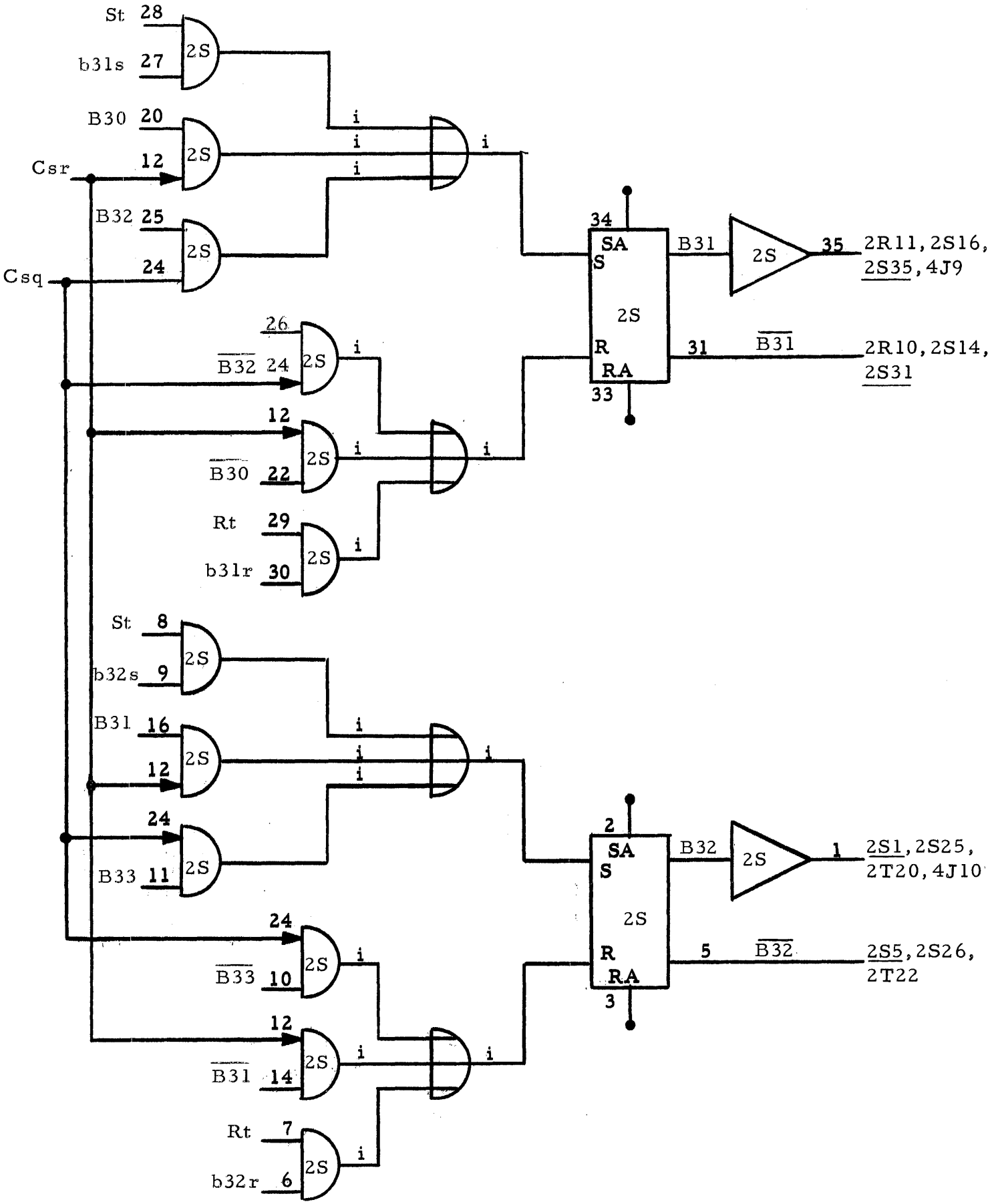

St 28
b21s 27
2M
B20 20
Csr 12
B22 25
Csq 24
i
34
SA
S
2M
R
RA
33
B21
35
2L11, 2M16, 2M35, 13J21
31
B21
2L10, 2M14, 2M31
26
B22 24
12
B20 22
Rt 29
b21r 30
St 8
b22s 9
B21 16
B23 11
2
1
2M1, 2M25, 2N20, 13J22
5
B22
2M5, 2M26, 2N22
B23 10
B21 14
Rt 7
b22r 6

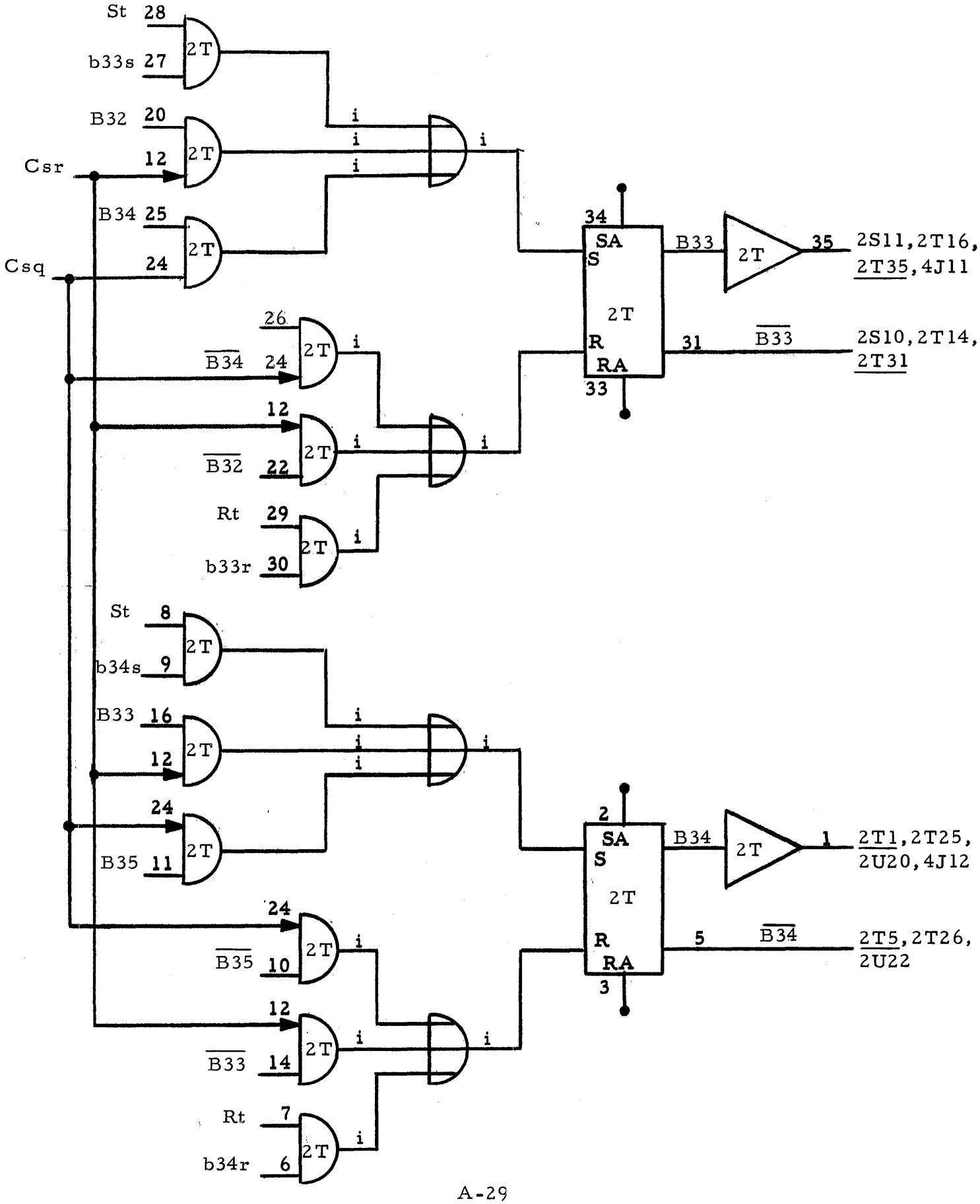

St 28
b23s 27
2N
B22 20
Csr 12
B24 25
Csq 24
i
34
SA
S
2N
R
RA
33
B23
35
2M11, 2N16, 2N35, 4J1
31
B23
2M10, 2N14, 2N31
26
B24 24
12
B22 22
Rt 29
b23r 30
St 8
b24s 9
B23 16
12
24
B25 11
2
1
2N1, 2N25, 2Θ20, 4J2
5
B24
2N5, 2N26, 2Θ22
B25 10
B23 14
Rt 7
b24r 6
3

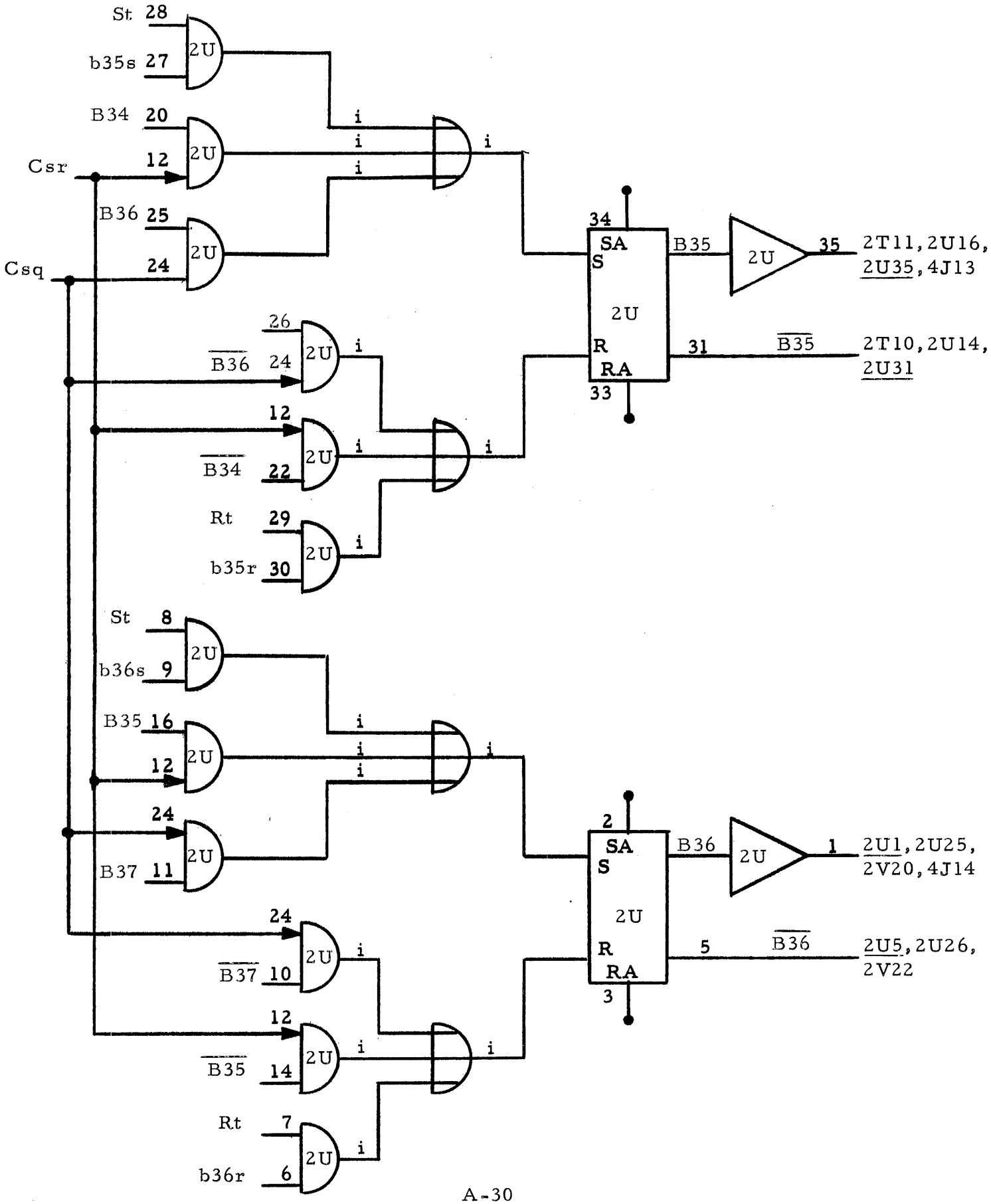

St 28
b25s 27
B24 20
Csr 12
B26 25
Csq 24
26
B26 24
12
B24 22
Rt 29
b25r 30
St 8
b26s 9
B25 16
12
24
B27 11
24
B27 10
12
B25 14
Rt 7
b26r 6
2Θ
i
34
SA
S
2Θ
R
RA
33
B25
35
2N11,2Θ16,
2Θ35,4J3
31
B25
2N10,2Θ14,
2Θ31
2
SA
S
2Θ
R
RA
3
B26
1
2Θ1,2Θ25,
2P20,4J4
5
B26
2Θ5,2Θ26,
2P22

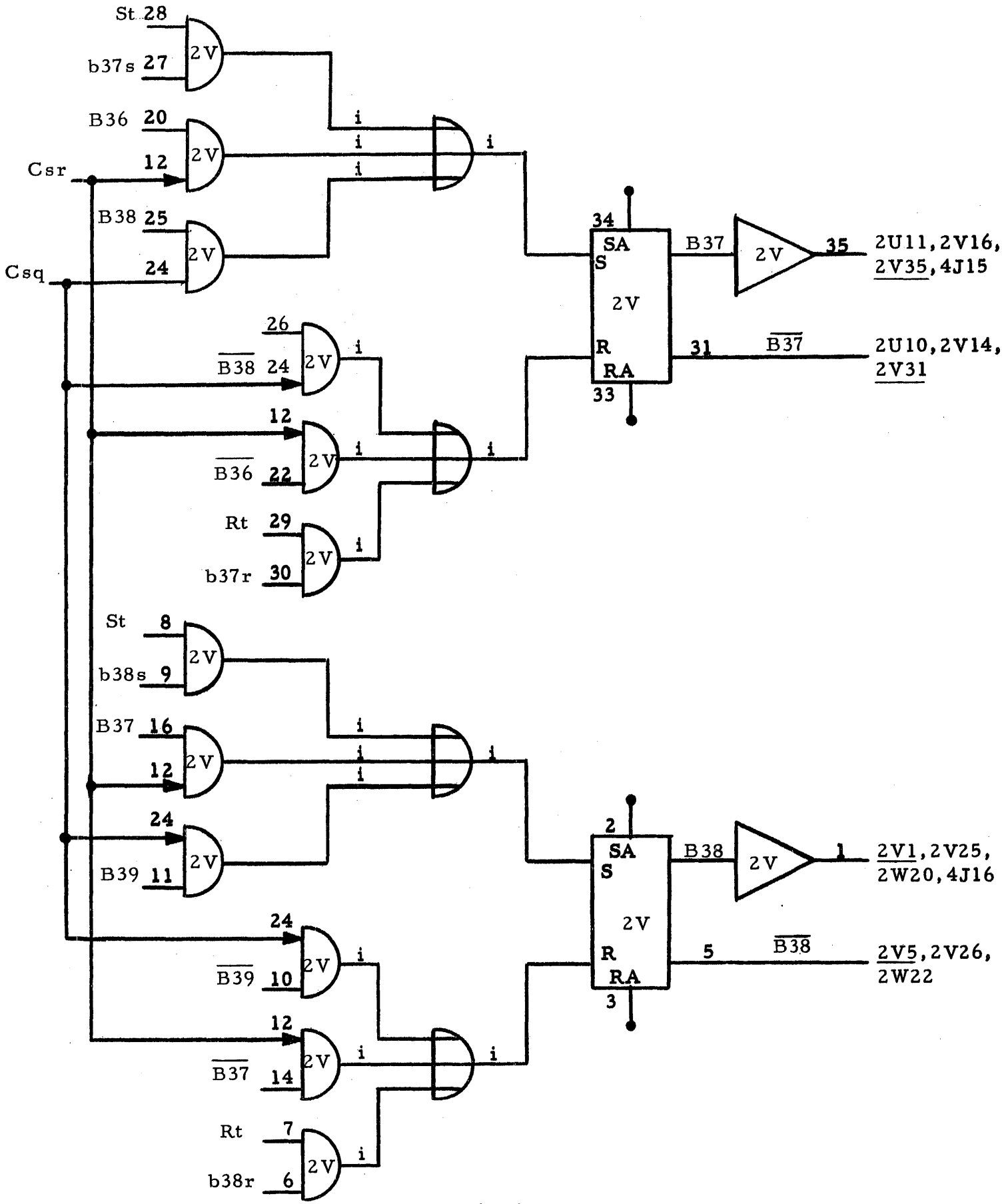

St 28
b27s 27
2P
B26 20
12
Csr
B28 25
Csq 24
i
34
SA
S
2P
R
RA
33
B27
35
2Θ11,2P16,
2P35,4J5
26
B28 24
31
B27
2Θ10,2P14,
2P31
Rt 29
b27r 30
St 8
b28s 9
B27 16
24
B29 11
2
B28
1
2P1,2P25,
2R20,4J6
B29 10
5
B28
2P5,2P26,
2R22
B27 14
3
Rt 7
b28r 6

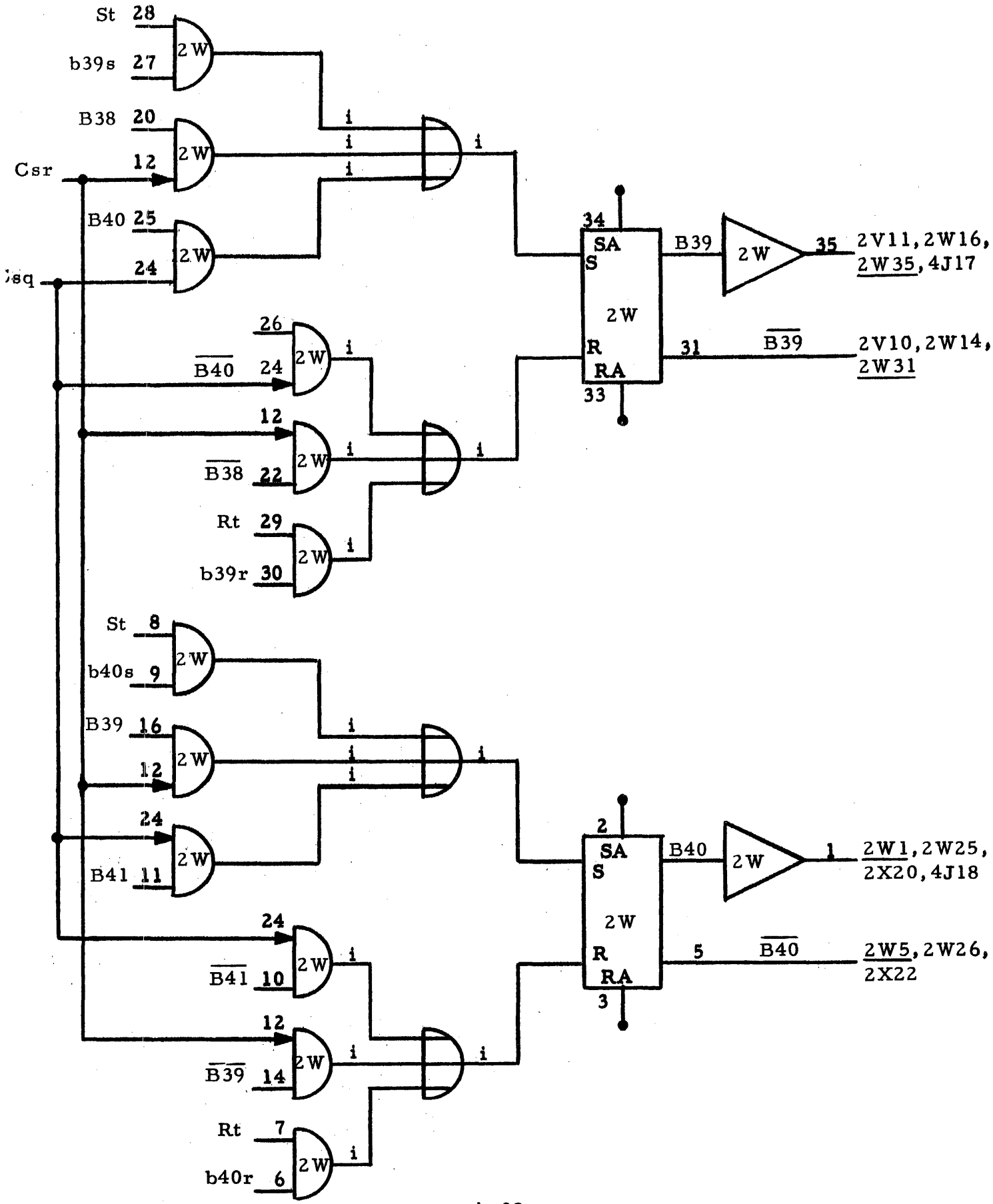

St 28
b29s 27
2R
B28 20
Csr 12
B30 25
Csq 24
i
34
SA
S
2R
R
RA
33
B29
35
2P11,2R16,
2R35,4J7
31
B29
2P10,2R14,
2R31
26
B30 24
12
B28 22
Rt 29
b29r 30
St 8
b30s 9
B29 16
12
24
B31 11
2
B30
1
2R1,2R25,
2S20,4J8
5
B30
2R5,2R26,
2S22
24
B31 10
12
B29 14
Rt 7
b30r 6

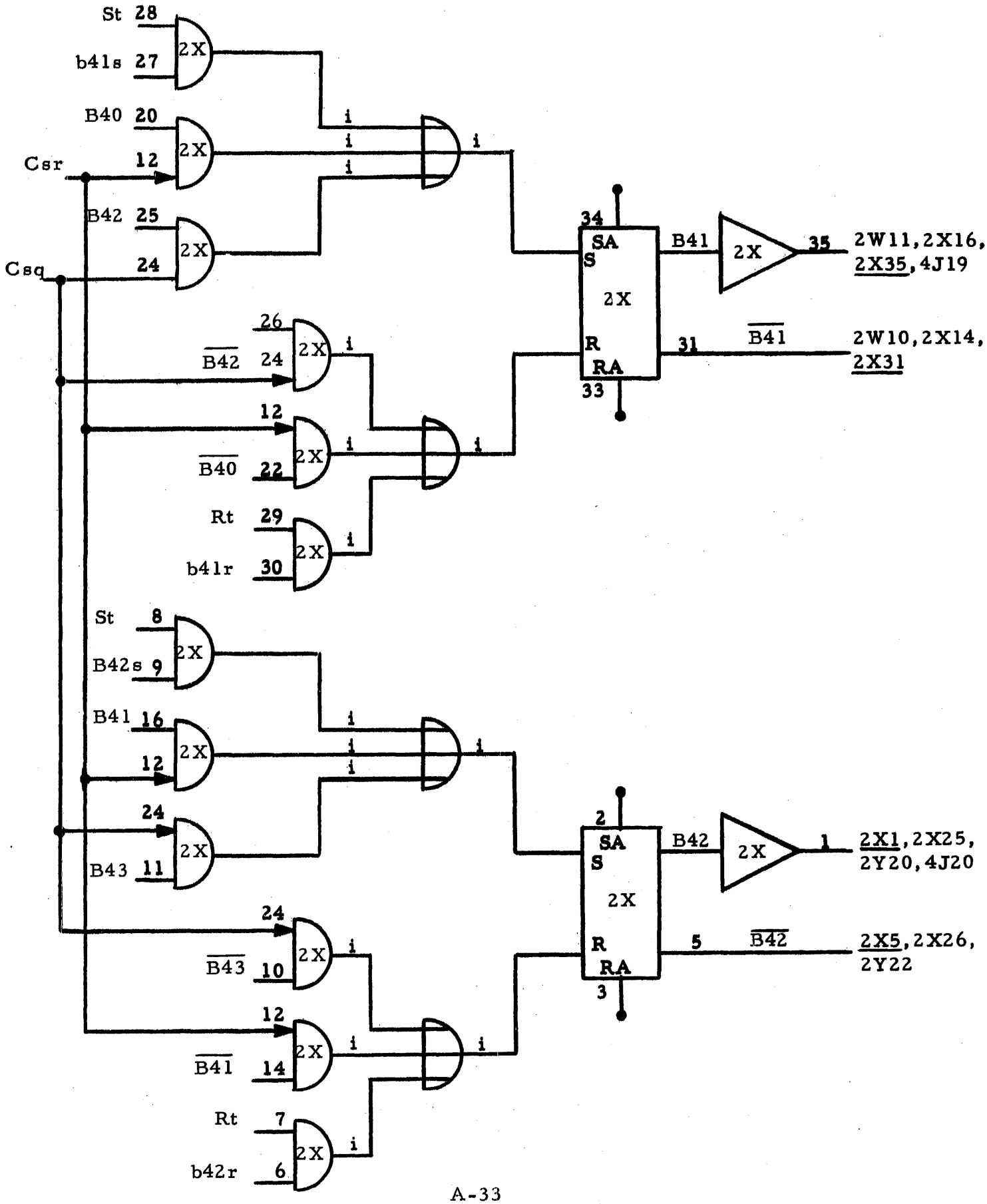

St 28
b31s 27
2S
B30 20
Csr 12
B32 25
Csq 24
i
34
SA
S
2S
R
RA
33
B31
35
2R11, 2S16, 2S35, 4J9
31
B31
2R10, 2S14, 2S31
26
B32 24
12
B30 22
Rt 29
b31r 30
St 8
b32s 9
B31 16
12
24
B33 11
2
B32
1
2S1, 2S25, 2T20, 4J10
5
B32
2S5, 2S26, 2T22
24
B33 10
12
B31 14
Rt 7
b32r 6
3

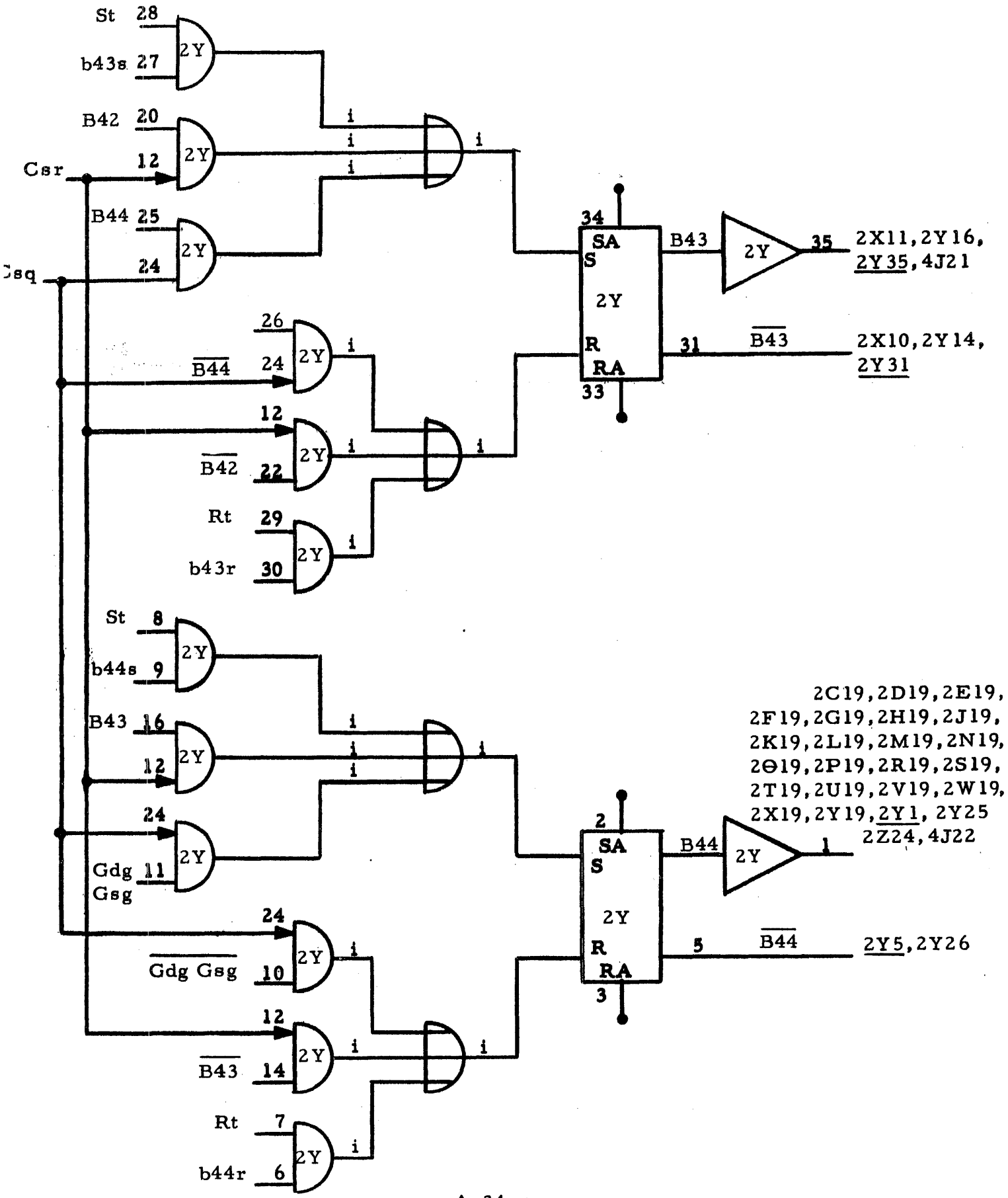

St 28
b33s 27
2T
B32 20
12
Csr
B34 25
24
Csq
i
34
SA
S
2T
R
RA
33
B33
35
2S11,2T16,
2T35,4J11
31
$\overline{B33}$
2S10,2T14,
2T31
26
$\overline{B34}$ 24
$\overline{B32}$ 22
Rt 29
b33r 30
St 8
b34s 9
B33 16
B35 11
2
B34
1
2T1,2T25,
2U20,4J12
5
$\overline{B34}$
2T5,2T26,
2U22
$\overline{B35}$ 10
$\overline{B33}$ 14
Rt 7
b34r 6


St 28
b35s 27
2U
B34 20
Csr
12
B36 25
Csq
24
i
34
SA
S
2U
R
RA
33
B35
35
2T11,2U16,
2U35,4J13
31
B35
2T10,2U14,
2U31
26
B36 24
12
B34 22
Rt 29
b35r 30
St 8
b36s 9
B35 16
B37 11
2
B36
1
2U1,2U25,
2V20,4J14
5
B36
2U5,2U26,
2V22
B37 10
B35 14
Rt 7
b36r 6


St 28
b37s 27
2V
B36 20
12
Csr
B38 25
24
Csq
i
34
SA
S
2V
R
RA
33
B37
35
2U11,2V16,
2V35,4J15
31
B37
2U10,2V14,
2V31
26
B38 24
12
B36 22
Rt 29
b37r 30
St 8
b38s 9
B37 16
12
24
B39 11
2
1
2V1,2V25,
2W20,4J16
5
B38
2V5,2V26,
2W22
3
24
B39 10
12
B37 14
Rt 7
b38r 6


St 28
b39s 27
B38 20
12
Csr
B40 25
24
sq
2W
i
34
SA
S
2W
R
RA
33
B39
35
2V11, 2W16,
2W35, 4J17
31
B39
2V10, 2W14,
2W31
26
B40 24
12
B38 22
Rt 29
b39r 30
St 8
b40s 9
B39 16
12
24
B41 11
2
B40
1
2W1, 2W25,
2X20, 4J18
5
B40
2W5, 2W26,
2X22
3
B41 10
B39 14
Rt 7
b40r 6


St 28
b41s 27
B40 20
Csr 12
B42 25
Csq 24
2X
i
34
SA
S
2X
R
RA
33
B41
35
2W11,2X16,
2X35,4J19
31
B41
2W10,2X14,
2X31
26
B42 24
12
B40 22
Rt 29
b41r 30
St 8
B42s 9
B41 16
12
24
B43 11
2
B42
1
2X1,2X25,
2Y20,4J20
5
B42
2X5,2X26,
2Y22
24
B43 10
12
B41 14
Rt 7
b42r 6
3


St 28
b43s 27
2Y
B42 20
12
Csr
B44 25
24
Csq
i
26
B44
24
12
B42
22
Rt 29
b43r 30
34
SA
S
2Y
R
RA
33
B43
35
2X11,2Y16,
2Y35,4J21
31
B43
2X10,2Y14,
2Y31
St 8
b44s 9
B43 16
12
24
Gdg 11
Gsg
24
Gdg Gsg
10
12
B43 14
Rt 7
b44r 6
2
B44
1
2C19,2D19,2E19,
2F19,2G19,2H19,2J19,
2K19,2L19,2M19,2N19,
2O19,2P19,2R19,2S19,
2T19,2U19,2V19,2W19,
2X19,2Y19,2Y1, 2Y25
2Z24,4J22
5
B44
2Y5,2Y26
3

APPENDIX B

Test Routine and Program Listing

APPENDIX B

HIGH-SPEED BUFFER HSB-N TEST ROUTINE

B-1. PURPOSE

To test the capability of the High-Speed Buffer, HSB-N, to provide communication with the PB 250 Computer.

B-2. STORAGE

Ninety words of line 02 plus five channels of line 00.

B-3. TIMING

36 milliseconds for each successful input-output pass.

B-4. OPERATION

The operating procedure is as follows:

a) Load the Octal Utility Package (see PB 250 Programming Manual, PBC 1004).

b) After loading the HSB-N test routine, transfer control to sector 377, line 02 by typing 37702.

c) After the Flexowriter indicating light comes on, type the buffer length in octal, that is, type $26)_8$ for a 22-bit buffer, or $54)_8$ for a 44-bit buffer.

d) If the BREAK POINT switch is up, the program will shift random numbers into the buffer, read them back and compare with the numbers originally generated.

e) If an error is found, the program will halt with a line number of $12)_8$ displayed in the OPERAND lights of the PB250 Computer panel. To continue testing, clear any parity by depressing both the ENABLE and BREAK POINT switches.

f) When the BREAK POINT switch is down, the program will cycle on the same number until this switch is raised. When the BREAK POINT switch is up, the program will generate new numbers.

g) After an error halt, the operator may inspect the information by dumping (using the Octal Utility Package) sectors 076 and 077 in line 00, which contain the number shifted out and sectors 101 and 102 in line 00 which contain the information received from the buffer.

h) This program will halt whenever an error is found. When troubleshooting, it is necessary to disregard errors and continue repeating the same output to the buffer. For this mode of operation, the command in location 112 line 02 must be changed to 075S3702;.

B-5. METHOD

The program assembles BSO and BSI masks based on the typed-in buffer length. Pseudo-random numbers are generated in the same manner as described in Random Number Write-Read II (PBC catalog number 9001). These numbers are sent out to the buffer using BSO and received immediately using BSI, commands. The numbers are then compared with the numbers originally generated.

If successful, a new random number is generated. The BREAK POINT switch is tested after every pass; if the switch is down, the same number is used until the switch is raised.

Table B-1. (Sheet 1 of 5)

PROGRAM LISTING

Location	Instruction	Symbolic op Code	Remarks
37702$	000 4400;	CLC	Initialize 0 ⟶ A, C
000	001S0702;	LDP	
001	-7777777		
002	-7777777		
003	076 1302;	STD	Full Mask ⟶ BSO, BSI,
044	101 1302	STD	TOF Connector ⟶ 10502
005	006S0502;	LDA	
006	107 7502;	[TOF]	
007	105 1102;	STA	
010	012S4502;	CLA	
011	017S5502;	LAI	
012	010S5102;	RTK	
013	014 5102;	RTK	
014	013 7736;	TES	
015	012 7736;	TES	2 Octal Digit Buffer Size ——F00
016	014S5700;	CIB	
017	+0000007	LAI MASK	
020	024 3502;	TCN	
021	001 0402;	LDC	

Table B-1. (Sheet 2 of 5)

PROGRAM LISTING

Location	Instruction	Symbolic op Code	Remarks
022	026 2110;	ABL	
023	012S4300;	CLB	
024	000 1100;	STA	
025	026S1502;	SUB	Buffer > 22 Bits ?
026	+0000027	+23	
027	047 3502;	TAN	
030	000 0500;	LDA	
031	032S5602;	CAM	Yes. Buffer = 44 Bits
032	+0000054	+44	
033	067 7502;	TOF	
034	113 1502;	SUB	
035	054 2110;	ABL	
036	037S1402;	ADD	
037	044 2110;	ABL	No 22 < Buffer < 44 Form Shift
040	043 1102;	STA	and insert B - 22 Bits into
041	001 0602;	LDB	second BSI and BSO masks
042	000 4500;	CLA	
043	+0000000		
044	077 1102;	STA	

Table B-1. (Sheet 3 of 5)

PROGRAM LISTING

Location	Instruction	Symbolic op Code	Remarks
045	102 1102;	STA	
046	067S3702;	TRU	
047	000 4500;	CLA	
050	077 1102;	STA	Buffer < 23 Bits 0 ⟶ Second Buffer Masks
051	102 1102;	STA	
052	114S3702;	TRU	
053	054S5602;	CAM	
054	+0000026	+22	Buffer = 22 Bits
055	067 7502;	TOF	
056	075 2110;	ABL	
057	060S1402;	ADD	
060	065 2110;	ABL	
061	064 1102;	STA	
062	001 0602;	LDB	No Buffer < 22 Bits Insert B Bits in first word of BSI, BSO Masks
063	000 4500;	CLA	
064	+0000000	ABL	
065	076 1102;	STA	
066	101 1102;	STA	
067	070S0602;	LDB	

Table B-1. (Sheet 4 of 5)

PROGRAM LISTING

Location	Instruction	Symbolic op Code	Remarks
070	077 0600;	LDB	Generate Random Number → F16, F17
071	072S0402;	LDC	
072	+2304555		
073	127 3200;	MUP	
074	076 1300;	STD	
075	100S7200;	BSO	BSO
076	-7777777		
077	-7777777		
100	103S7300;	BSI	BSI
101	-7777777		
102	-7777777		
103	120S3702;	TRU	
104	101 5600;	CAM	First Word Out = First Word In ?
105	107 7502;	TOF	
106	112S3702;	TRU	No. Error
107	124S3702;	TRU	
110	102 5600;	CAM	Second Word Out = Second Word In ?
111	130 7502;	TOF	Yes- Repeat
112	070S0012;	HLT	No. Error

Table B-1. (Sheet 5 of 5)

PROGRAM LISTING

Location	Instruction	Symbolic op Code	Remarks
113	+0000026	+22	
114	111 0502;	LDA	Buffer < 23 Bits Bypass Second Check
115	105 1102;	STA	
116	000 0500;	LDA	
117	053S3702;	TRU	
120	000 4300;	CLB	Extract Bits of Random Number Not Shifted Out
121	076 0400;	LDC	
122	101 4602;	AOC	
123	102S0300;	ROT	
124	000 4300;	CLB	Extract Bits of Random Number Not Shifted Out
125	077 0400;	LDC	
126	102 4602;	AOC	
127	106S0300;	ROT	
130	075 7735;	TES	If Breakpoint Down Hold R. N.
131	071S3702;	TRU	

APPENDIX C

Module Schematics

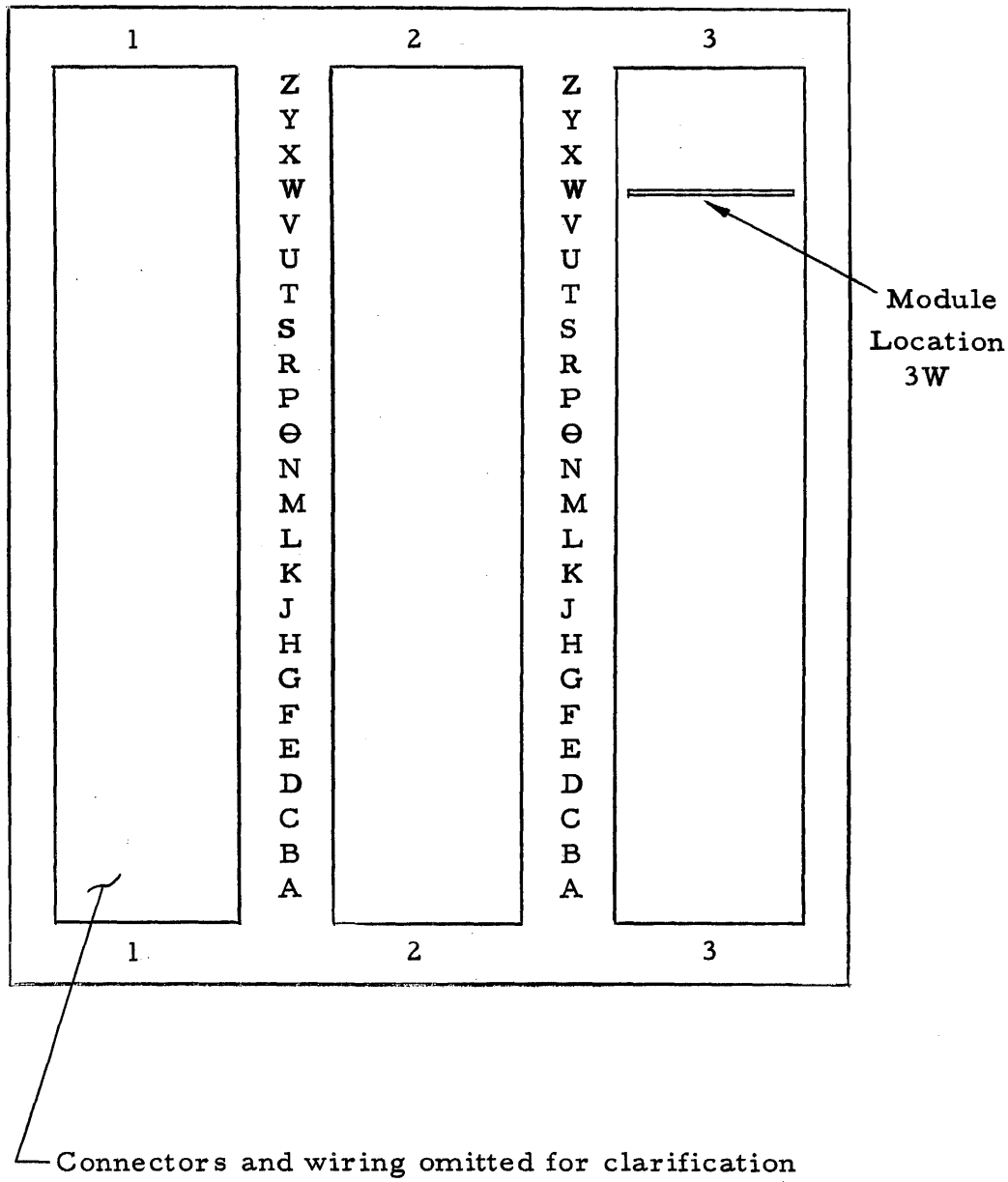


Figure C-1. HSB-N Module Locations (Sheet 1 of 2)

HSB-N MODULE LOCATIONS

Module	Location
CD-100	1Θ 1P 1T 1U
DG-100	2A
DG-102	1S 1W 2Z 3U 3V
EF-101	1R 1X 3S
GD-100	1V 3Y
SR-100	2B through 2Y Note: When installing N/2 number of SR-100's start at position 2B and install in sequence towards 2Y. After installing N/2 number of SR-100's, install one termination module (124-1C5142) in next sequential open position towards 2Y. When N = 44, there is no next sequential open position and no termination module is installed in the unit.
Termination	Refer to Note above
TF-100	3T
TI-4	1Y 3X
TO-3	3W
XCG-100	1Z

Figure C-1. HSB-N Module Locations (Sheet 2 of 2)

FIRST	LAST	DELETED
C1	C8	
CR1		
Q1	Q8	
R1	R29	

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTOR VALUES ARE IN KILOHMS ± 5%, 1/4 W.
2. ALL CAPACITORS ARE IN UUF.
3. ALL TRANSISTORS ARE 2N1500.
(4) CR1 TO BE PER PBCC DWG NO. 358-1A3050.

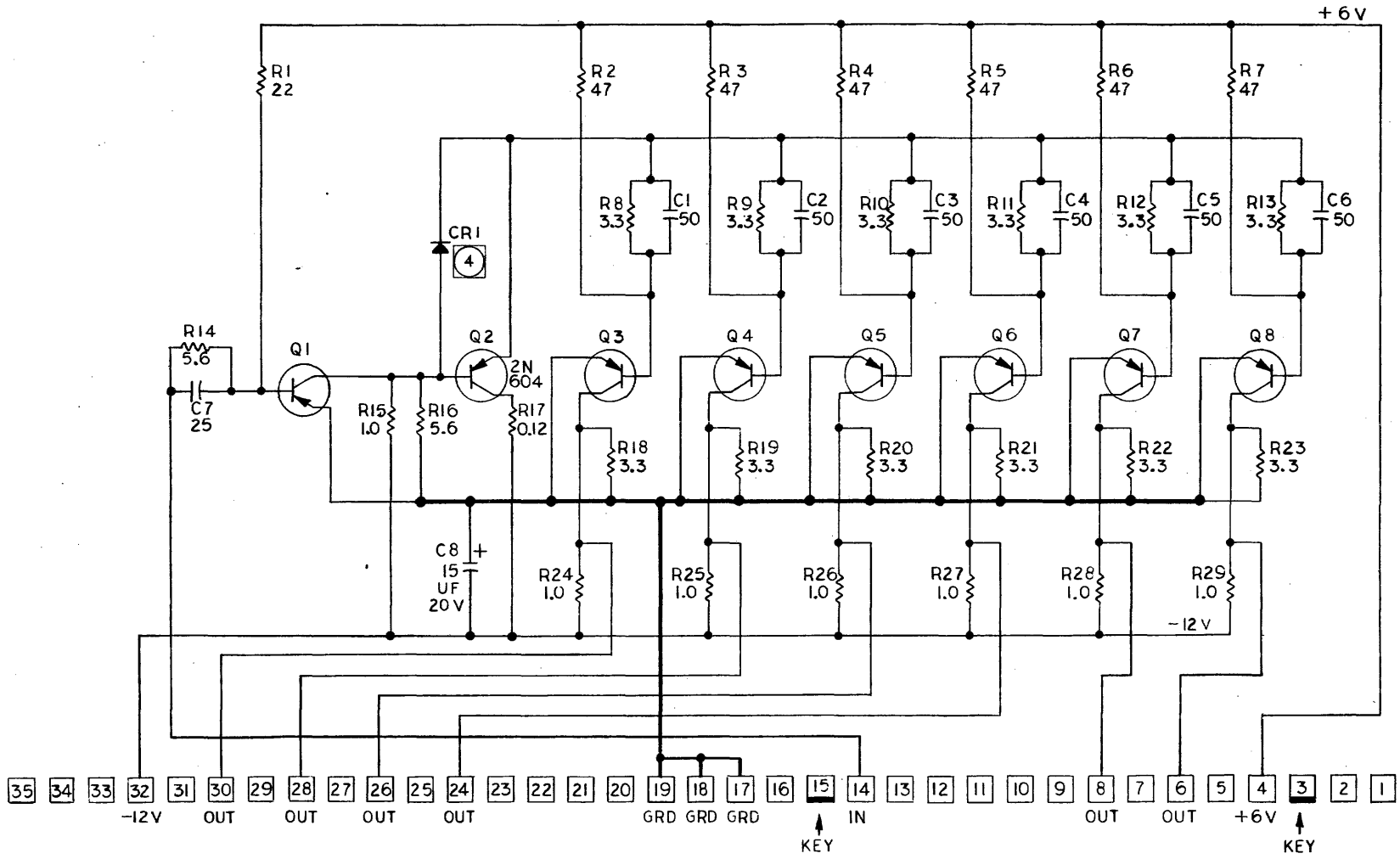


Figure C-2. CD-100 Clock Driver Module Schematic

FIRST	LAST	DELETED
R1	R24	
C1	C8	
CR1	CR35	

NOTES: UNLESS OTHERWISE SPECIFIED
1 ALL RESISTORS ARE IN KILOHMS ±5%, 1/4 W.
2 ALL DIODES TO BE PER P.B.C.C. DWG NO. 358-1A3050.
3 ALL CAPACITORS ARE 500UF.

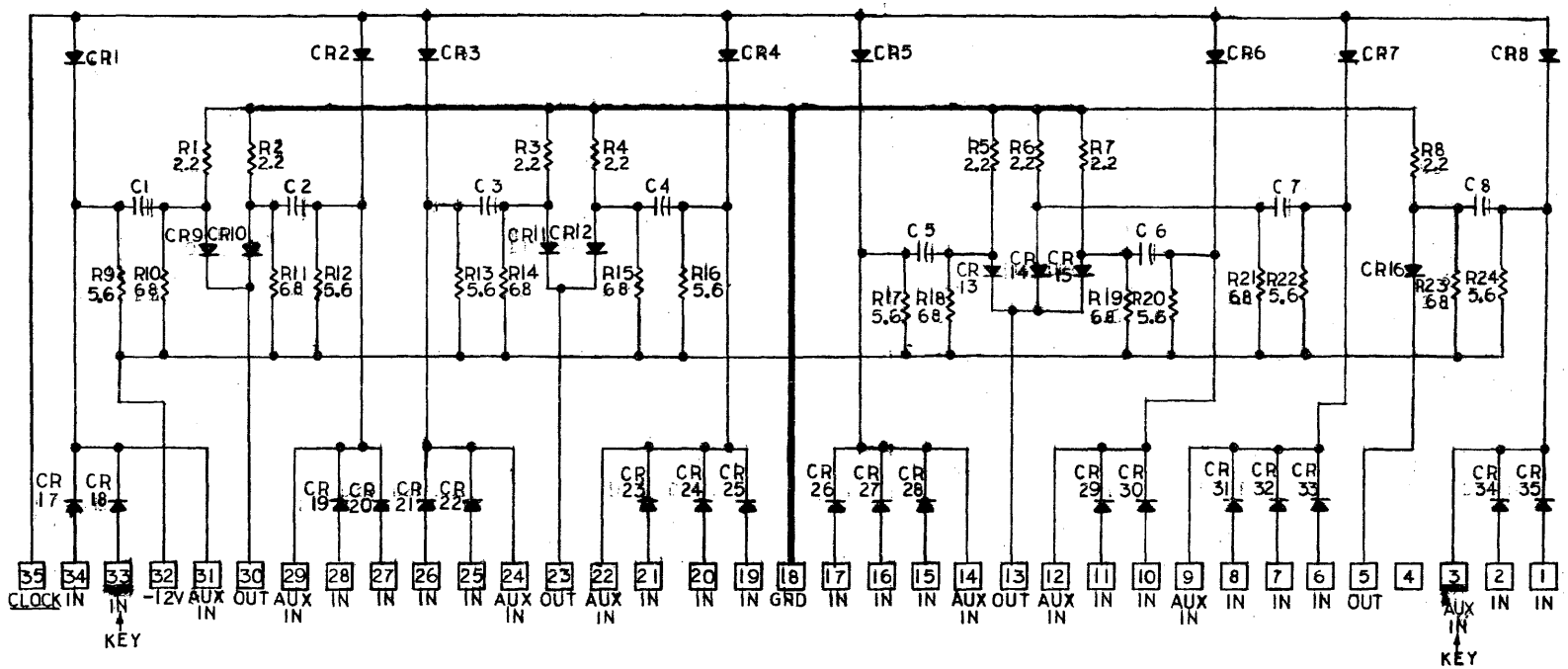


Figure C-3. DG-100 Diode Gate Module Schematic

FIRST	LAST	DELETED
C1	C2	
CR1	CR19	
R1	R6	

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN KILOHMS ± 5%, 1/4W
2. ALL DIODES TO BE PER P.B.C.C. DWG NO. 358-1A3050.

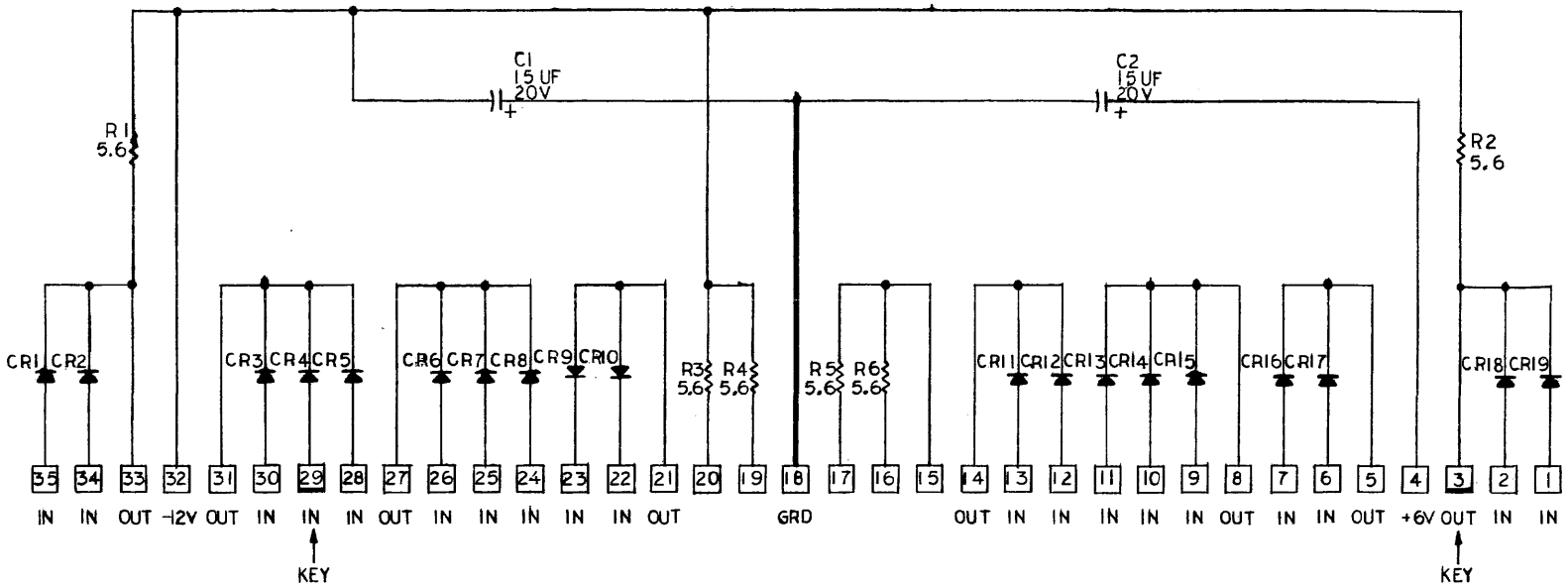


Figure C-4. DG-102 Module Schematic

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL DIODES ARE PER PBCC DWG. NO. 358-1A3050
2. ALL RESISISTOR VALUES ARE IN KILOHMS ±5% 1/4W
3. ALL TRANSISTORS ARE 2N604

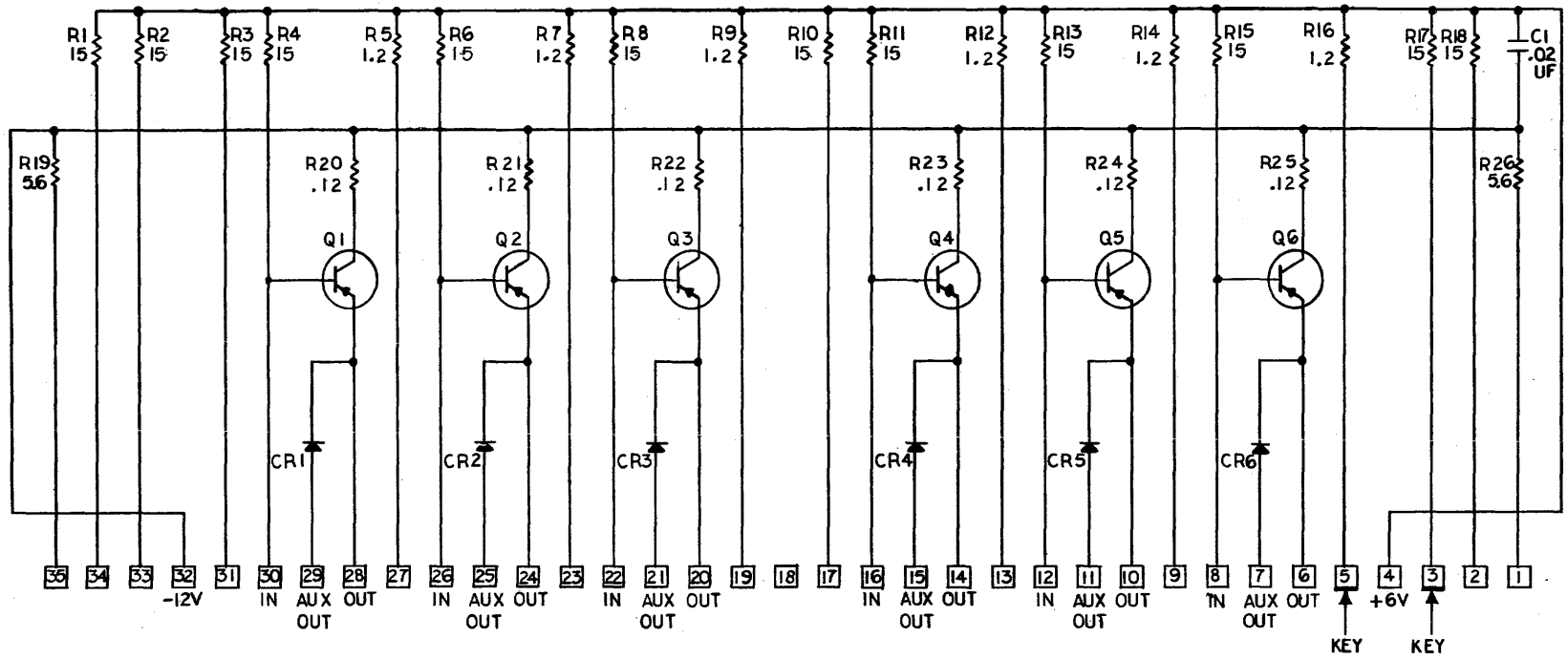


Figure C-5. EF-101 Module Schematic

FIRST	LAST	DELETED
Q1	Q8	
R1	R32	
C1	C9	

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES IN KILOHMS ±5%, 1/4W.
2. ALL CAPACITOR VALUES IN UUF.
3. ALL TRANSISTORS 2N1500.

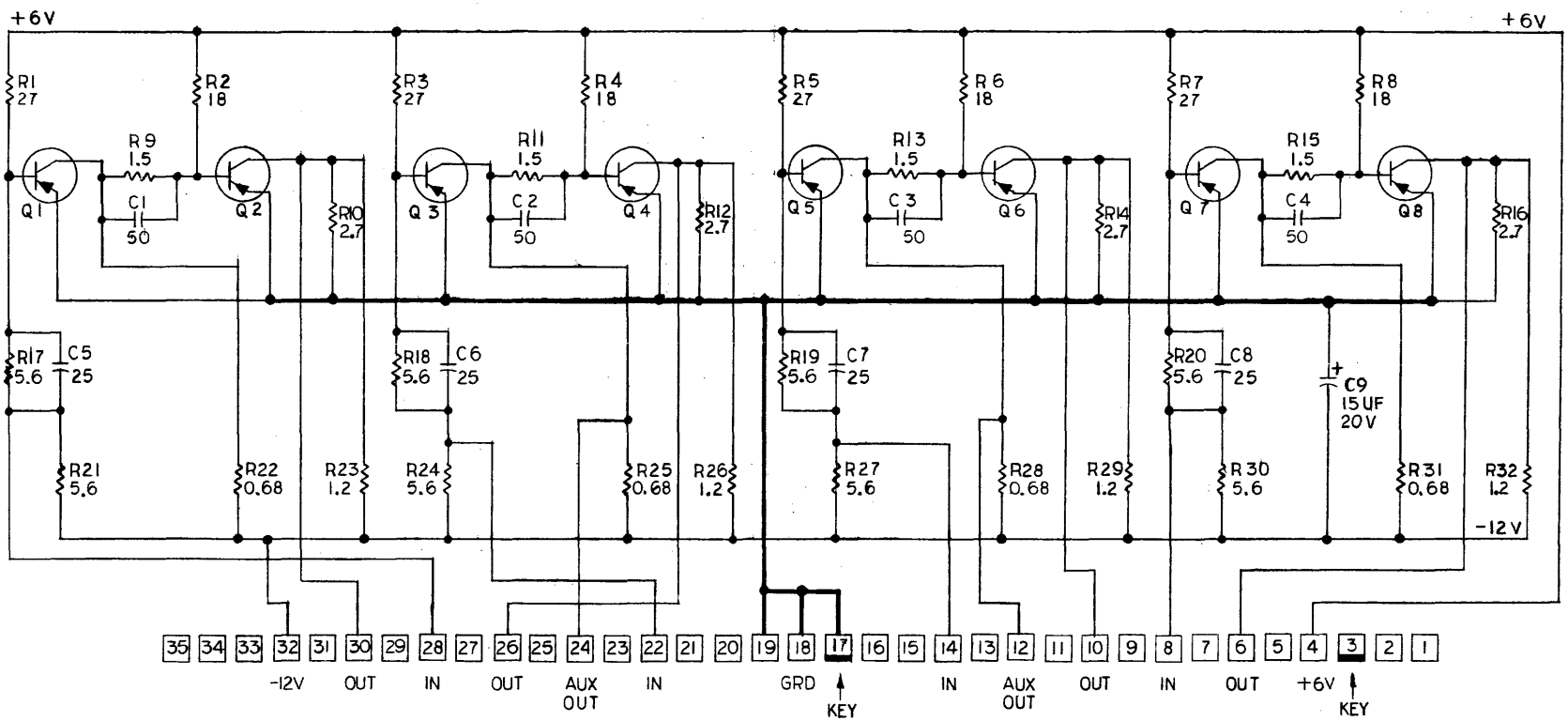


Figure C-6. GD-100 Gate Driver Module Schematic

REFERENCE DESIGNATIONS		
FIRST	LAST	DELETED
C1	C20	C5 & C18
CR1	CR38	
Q1	Q6	
R1	R46	

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTOR VALUES ARE IN KILOHMS ±5%, 1/4W.
2. ALL DIODES; HUGHES HD2935 OR SYLVANIA D1932. (PBCC STANDARD PART NO. 358-1A3050.)
3. ALL TRANSISTORS 2N1500.
4. ALL CAPACITOR VALUES IN UUF.

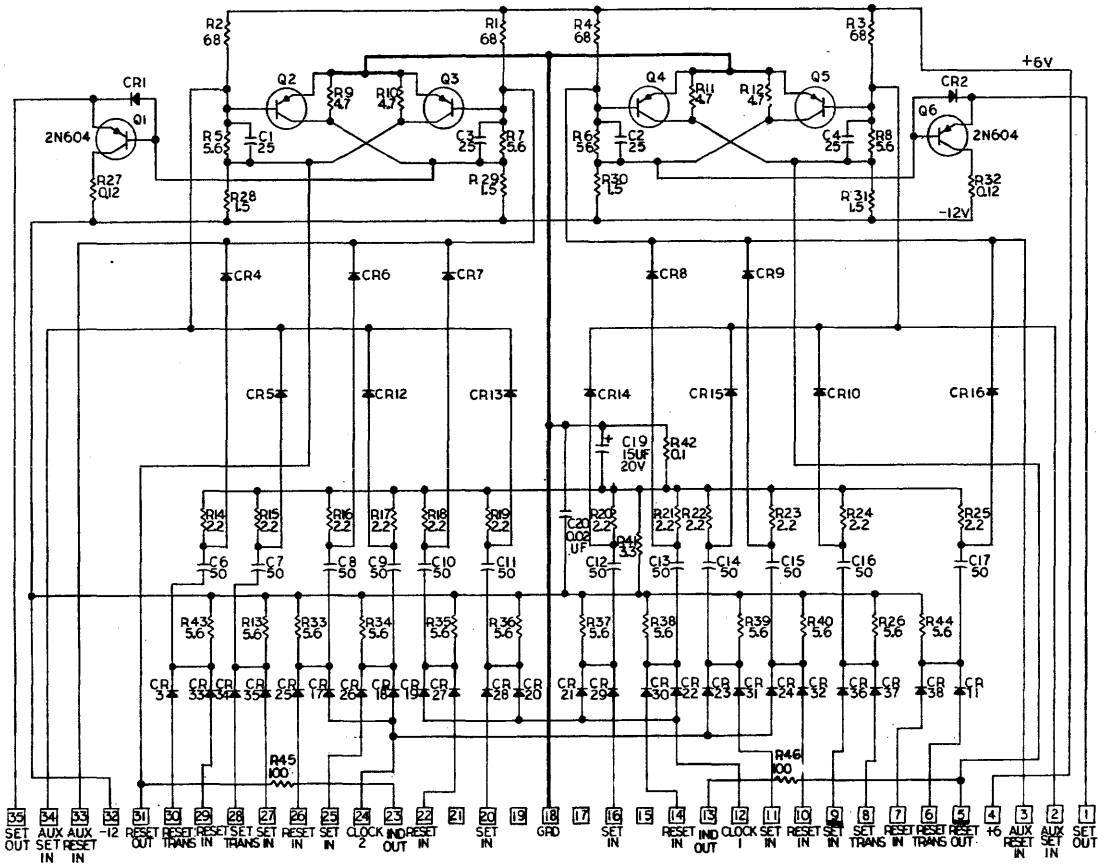


Figure C-7. SR-100 Shift Register Module Schematic

FIRST	LAST	DELETED
Q1	Q 4	
R1	R 32	
C1	C9	
CR1	CR8	

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTOR VALUES ARE IN KILOHMS ±5%, 1/4 W.
2. ALL DIODES TO BE PER PBCC DWG NO.358-1A3050.
3. ALL CAPACITOR VALUES ARE IN UUF.
4. ALL TRANSISTORS ARE 2N1500

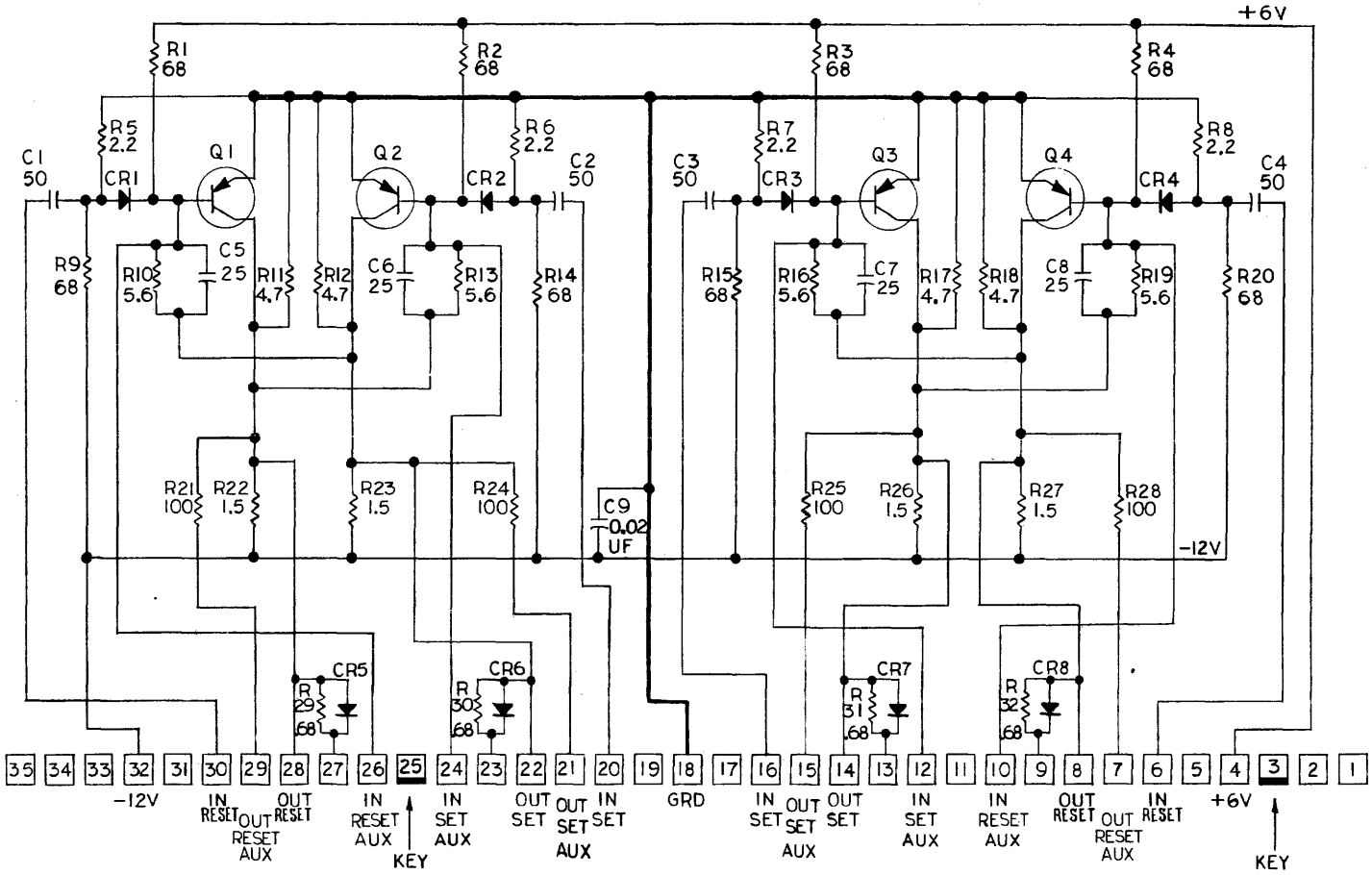


Figure C-8. TF-100 Flip-Flop Module Schematic

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN THOUSAND OHM UNITS ±5% 1/4W.
2. ALL CAPACITORS IN UUF.
3. ALL TRANSISTORS T1474.

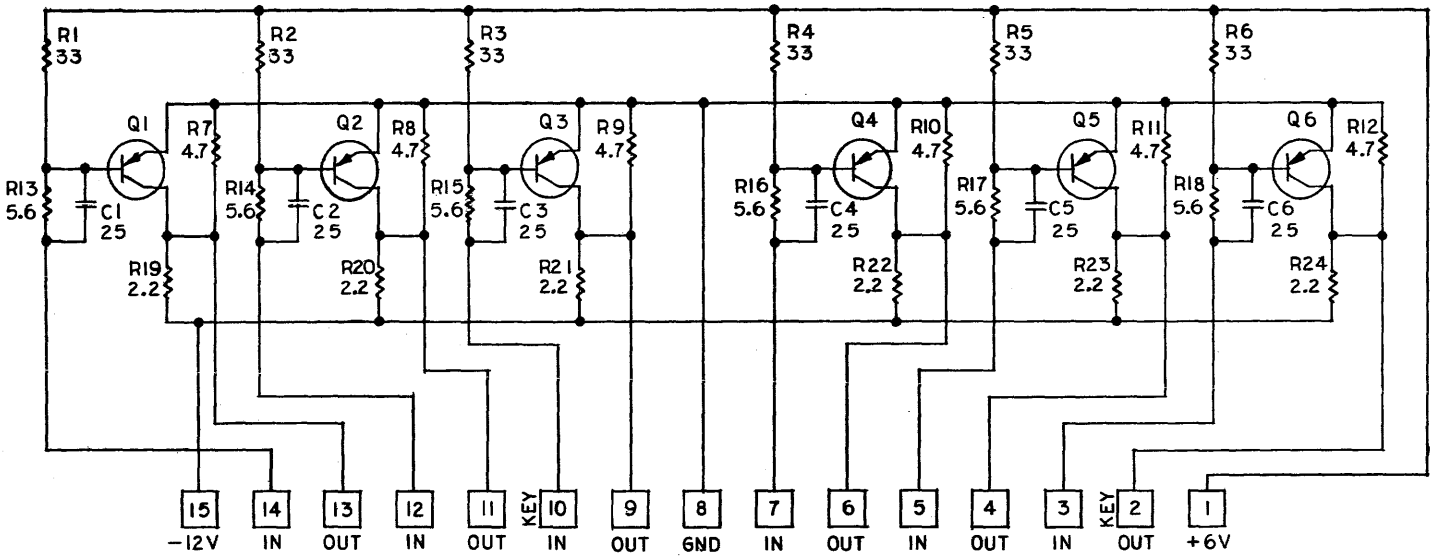
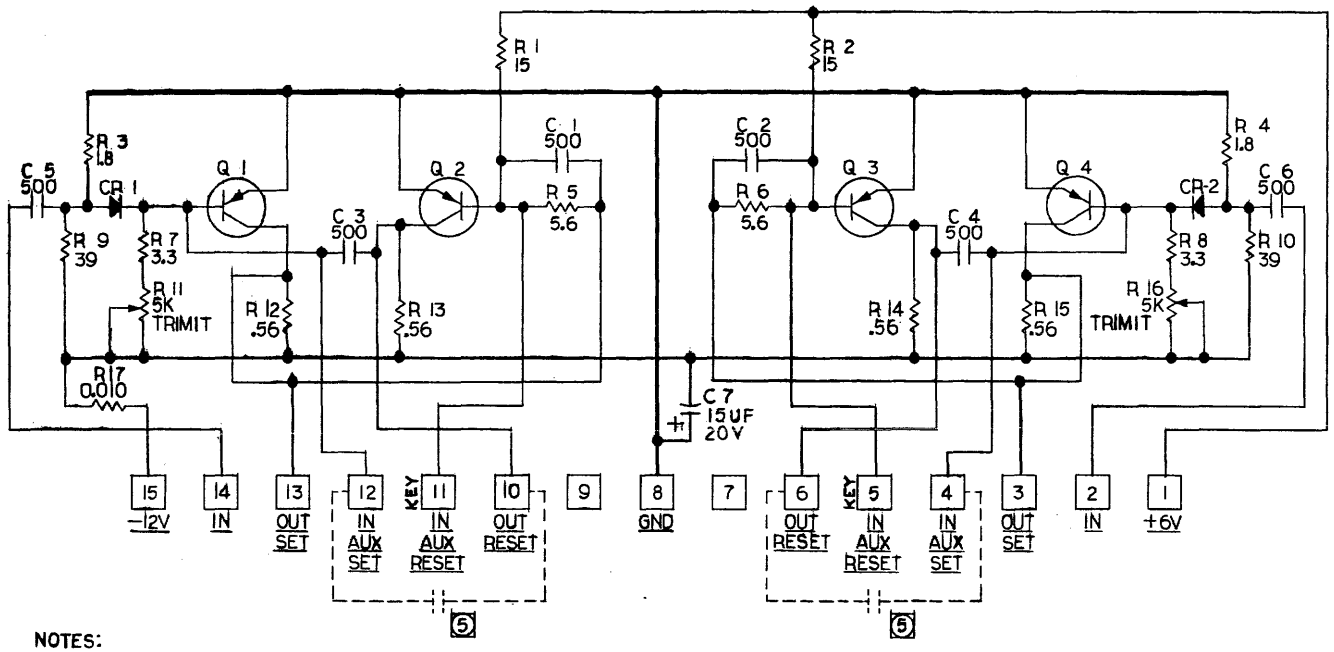


Figure C-9. TI-4 Amplifier-Inverter Module Schematic



NOTES:

1. ALL RESISTOR VALUES ARE IN THOUSAND OHM UNITS ±5% 1/2 W
2. ALL CAPACITORS IN UF UNLESS OTHERWISE NOTED.
3. ALL DIODES HUGHES HD2936 (PBCC STANDARD PART NO. 358-1A3051)
4. ALL TRANSISTORS 2N414.
5. TO VARY PULSE WIDTH (OR DELAY) A CAPACITOR MAY BE ADDED AT PINS 4-6 OR 10-12, AS SHOWN.

Figure C-10. TO-3 One shot Module, Schematic

FIRST	LAST	DELETED
C1	C14	
CR1	CR7	
L2	L4	L1
Q1	Q7	
R1	R24	R6
TP1		
Y1		

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN KILOHMS ± 5%, ¼ WATT.
2. ALL DIODES TO BE PER PBCC DWG NO. 358-1A3050.
3. ALL CAPACITOR VALUES IN UUF.
4. ALL TRANSISTORS ARE 2N604.
5. TWO SWITCHES INCLUDED IN TEST CIRCUIT FUNCTION, NOT LOCATED ON MODULE BOARD.

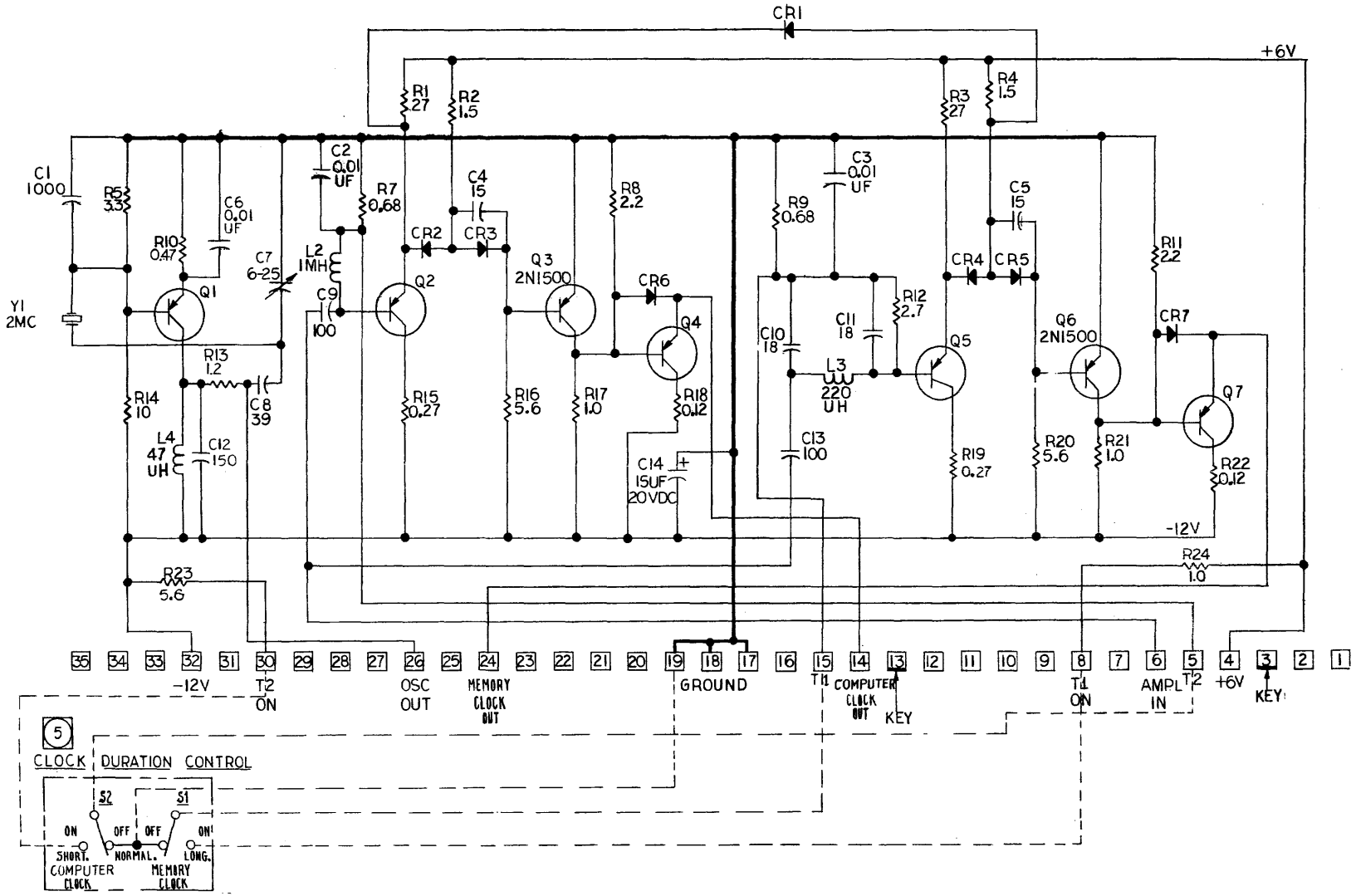


Figure C-11. XCG-100 Clock Generator Module, Schematic