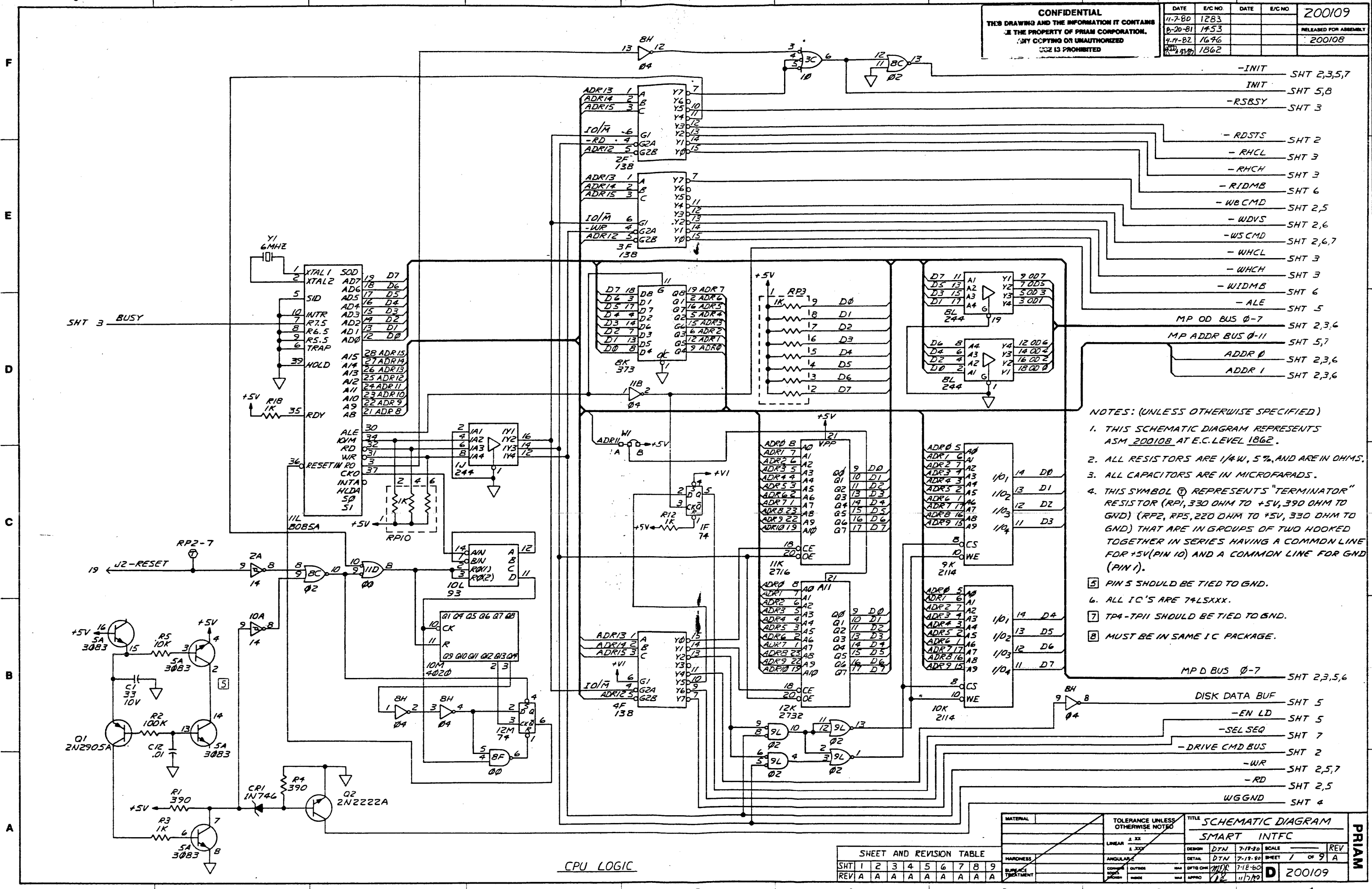


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DATE	E/C NO	DATE	E/C NO	200109
11-7-80	1283			
8-20-81	1453			RELEASED FOR ASSEMBLY
4-14-82	1696			200108
12-1-82	1862			



- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. THIS SCHEMATIC DIAGRAM REPRESENTS ASM 200108 AT E.C. LEVEL 1862.
 2. ALL RESISTORS ARE 1/4W, 5%, AND ARE IN OHMS.
 3. ALL CAPACITORS ARE IN MICROFARADS.
 4. THIS SYMBOL $\text{\textcircled{T}}$ REPRESENTS "TERMINATOR" RESISTOR (RP1, 330 OHM TO +5V, 390 OHM TO GND) (RP2, RPS, 220 OHM TO +5V, 330 OHM TO GND) THAT ARE IN GROUPS OF TWO HOOKED TOGETHER IN SERIES HAVING A COMMON LINE FOR +5V (PIN 10) AND A COMMON LINE FOR GND (PIN 1).
 5. PIN 5 SHOULD BE TIED TO GND.
 6. ALL IC'S ARE 74LSXXX.
 7. TP4-TP11 SHOULD BE TIED TO GND.
 8. MUST BE IN SAME IC PACKAGE.

CPU LOGIC

SHEET AND REVISION TABLE

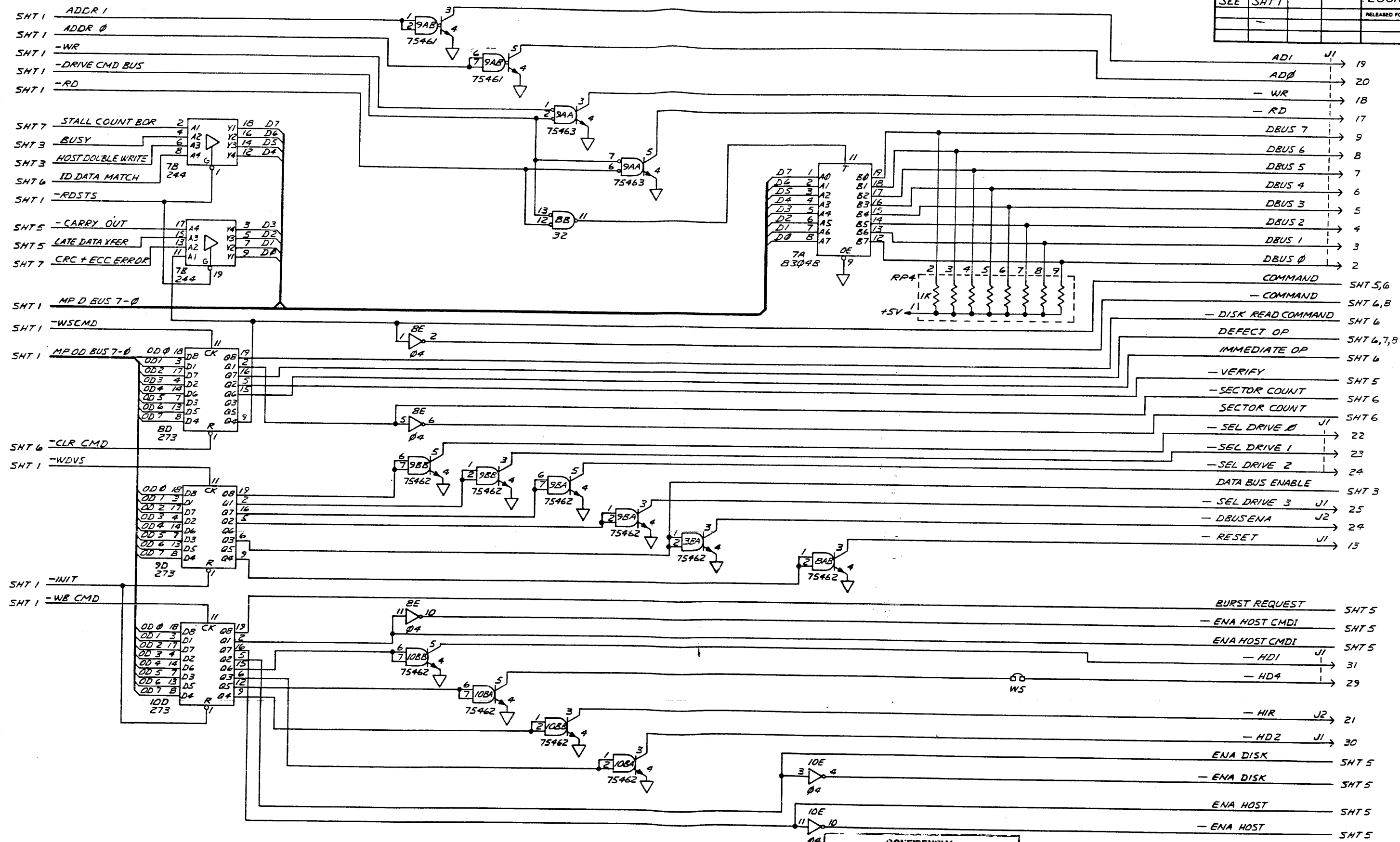
SHT	1	2	3	4	5	6	7	8	9
REV	A	A	A	A	A	A	A	A	A

MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE
	LINEAR ±.3% ANGULAR ±.3%	SCHMATIC DIAGRAM SMART INTFC
HARDNESS	DESIGN DTM 7-18-80	SCALE
SURFACE TREATMENT	DETAIL DTM 7-18-80	SHEET 1 OF 9 A
	DATE CHG 11-8-80	REV
	APPROV 12 11/8/80	D 200109

PRAM

DATE	E/C NO.	DATE	E/C NO.
SEE SHT 1			

200109
RELEASED FOR ASSEMBLY



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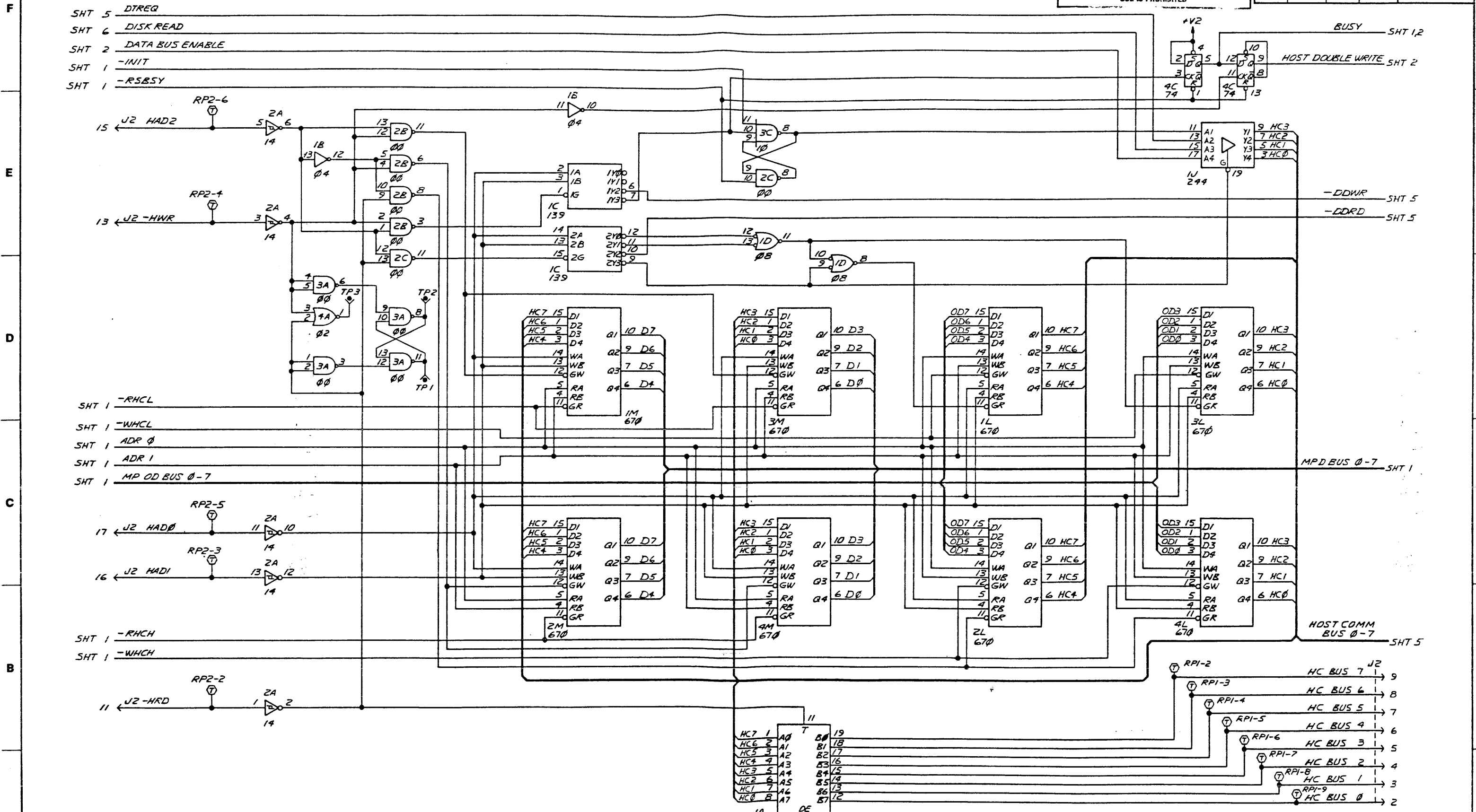
MB MISC REGISTERS

MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE
	LINEAR 2 XX ANGULAR 2 XXX	SCHEMATIC DIAGRAM SMART INTEFC
HARDNESS	CONFORM TO SPEC	DESIGN DTN 7-N-84 DETAIL DTN 7-15-84 DATE 7-18-84 APP'D [Signature]
SURFACE TREATMENT	OUTSIDE	SCALE 1:1 SHEET 2 OF 9 REV A
		200109

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DATE	E/C NO.	DATE	E/C NO.	200109
SEE	SHT 1			RELEASED FOR ASSEMBLY

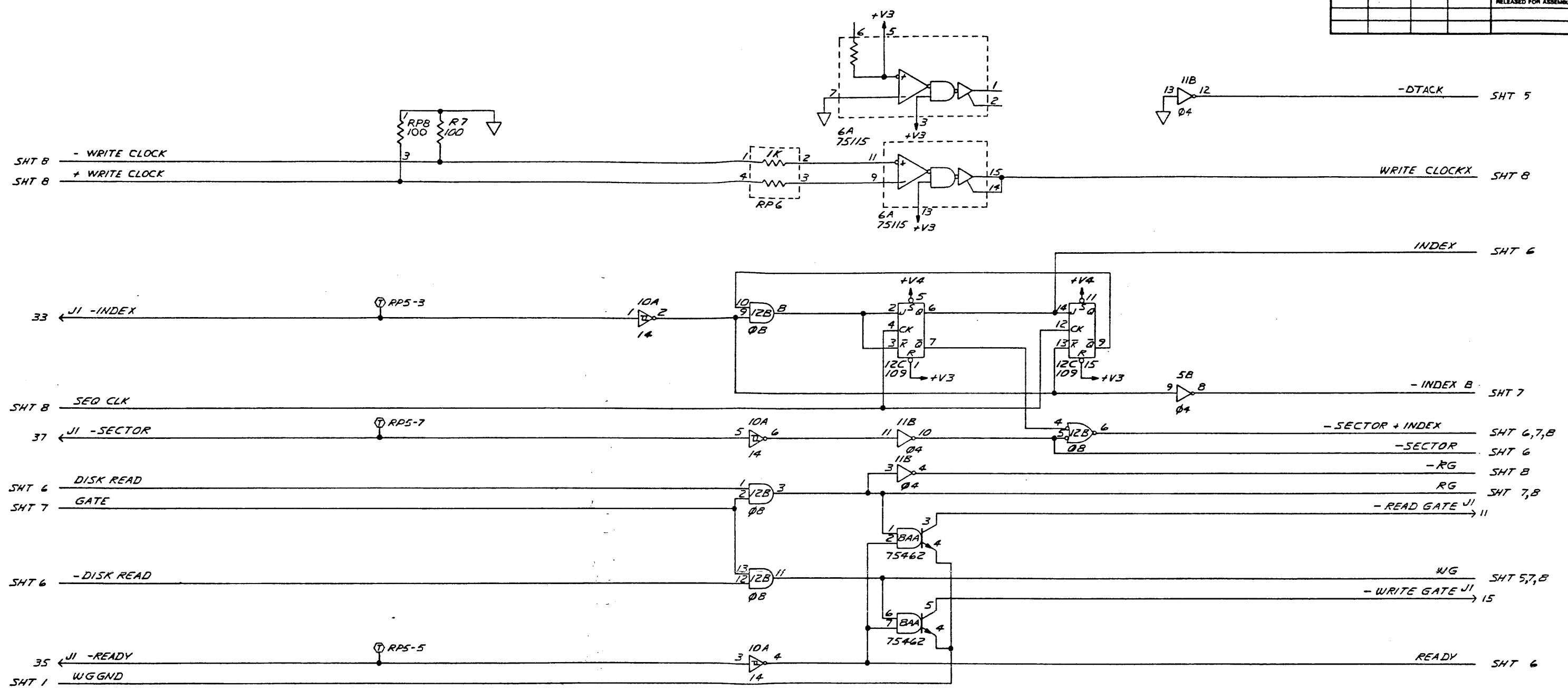


2-PORT FILE

MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE	SCHEMATIC DIAGRAM		PRIAM	
		SMART INTFC				
HARDNESS	LINEAR	DESIGN	DTN	7-18-80	SCALE	REV
SURFACE TREATMENT	ANGULAR	DETAIL	DTN	7-18-80	SHEET	3 OF 9 A
		COMP	DTN	7-18-80		
		CHKD	DTN	11-7-80		
		APPRO	DTN			
						200109

DATE	E/C NO.	DATE	E/C NO.	200109
SEE	SHT 1			RELEASED FOR ASSEMBLY

F
E
D
C
B
A



MISC

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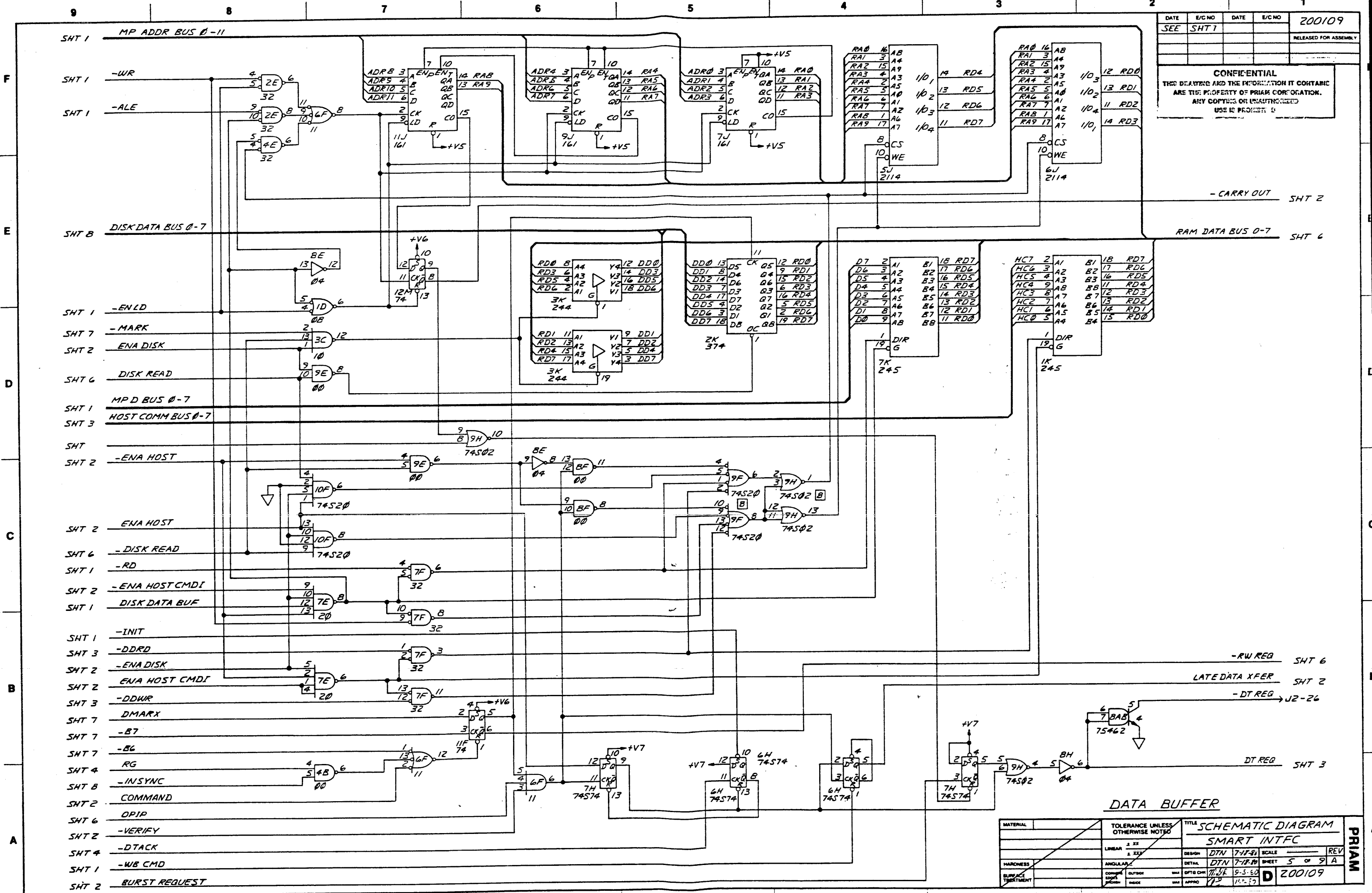
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE	SCHEMATIC DIAGRAM
			SMART INTFC
	LINEAR ± .02	DESIGN	DTN 7/8-80
	ANGULAR ± .02	SCALE	REV
HARDNESS		DETAIL	DTN 7/8-80
SURFACE TREATMENT		DFTS CHG	MDR 11-7-80
		APPRO	11-7-80

PRAM

200109

DATE	E/C NO	DATE	E/C NO	200109
SEE	SHT 1			RELEASED FOR ASSEMBLY

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- CARRY OUT SHT 2

RAM DATA BUS 0-7 SHT 6

- RW REQ SHT 6

LATE DATA XFER SHT 2

- DT REQ → J2-26

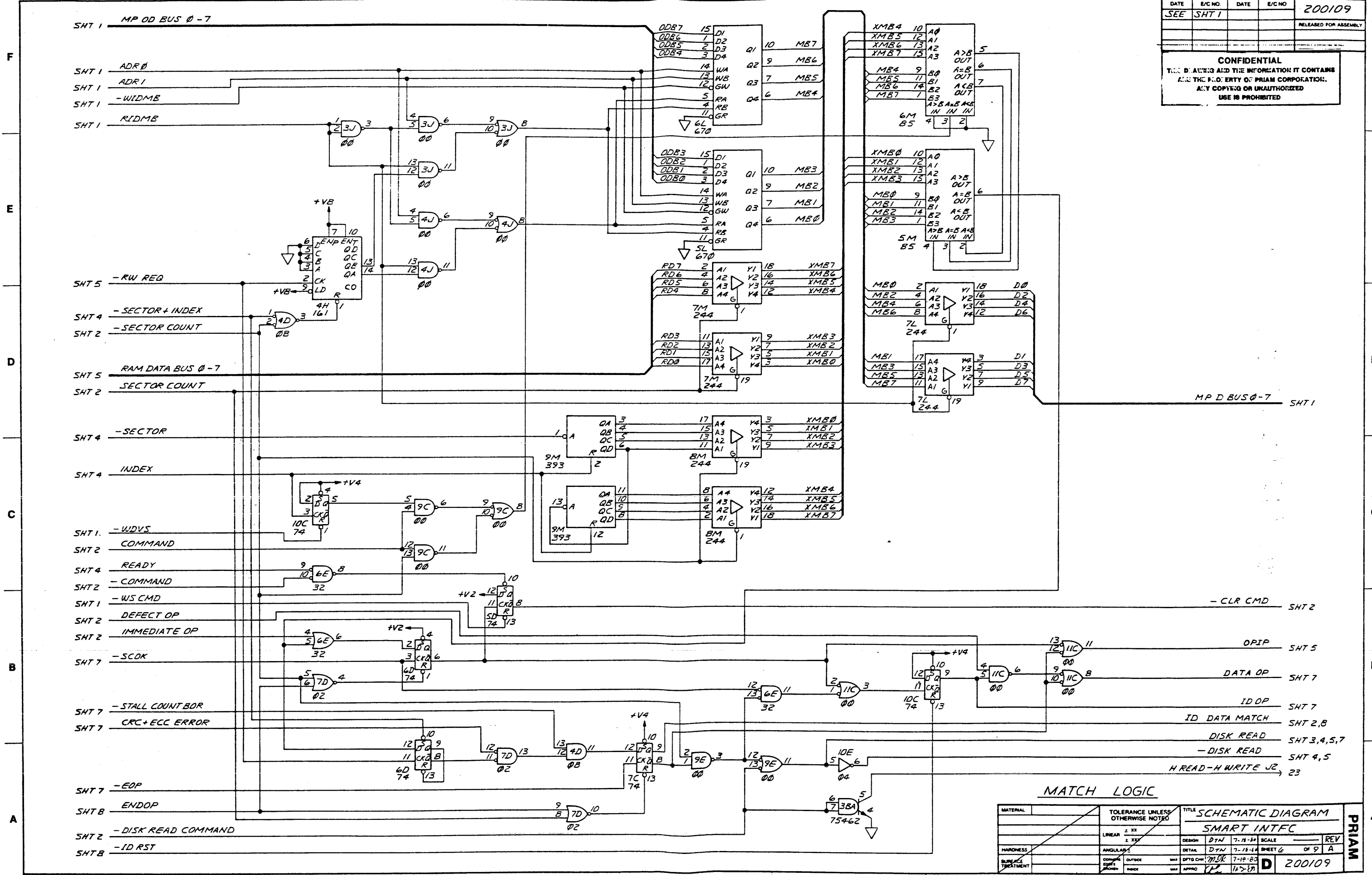
DT REQ SHT 3

DATA BUFFER

MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE SCHEMATIC DIAGRAM		PRIAM
LINEAR	2.00	SMART INTFC		
HARDNESS	ANGULAR	DESIGN	DTN 7-17-80	SCALE
SURFACE TREATMENT	OUTSIDE	DETAIL	DTN 7-17-80	SHEET 5 OF 9 A
		DATE	7/17/80	REV
		APPRO	7/17/80	D 200109

DATE	E/C NO.	DATE	E/C NO.	200109
SEE	SHT 1			RELEASED FOR ASSEMBLY

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MATCH LOGIC

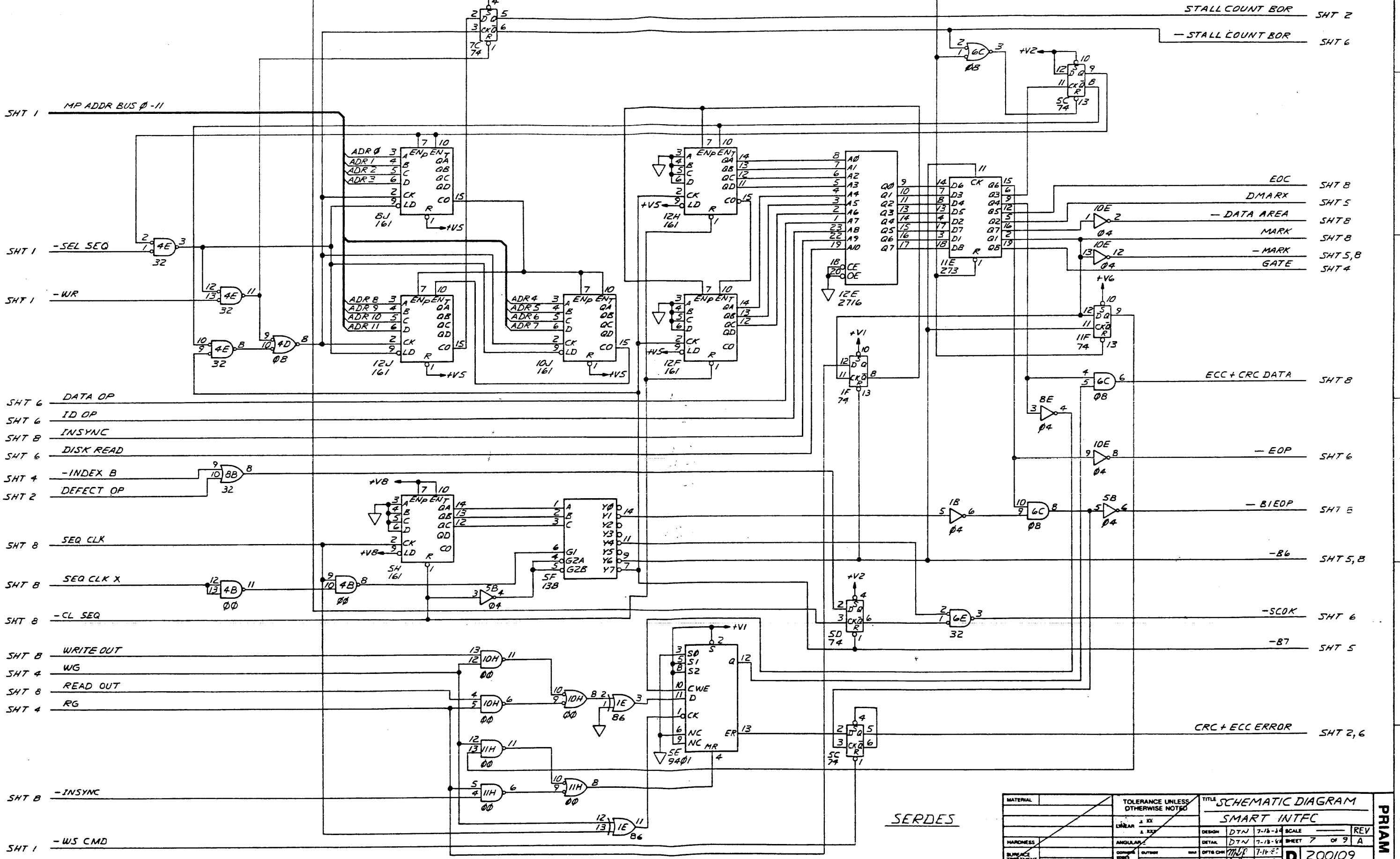
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE	SCHEMATIC DIAGRAM
			SMART INTFC
HARDNESS	ANGULAR	DESIGN	DTN 7-18-83
SURFACE TREATMENT	OUTSIDE	DETAIL	DTN 7-18-83
		SCALE	1:1
		REV	6 OF 9 A
		DATE	7-18-83
		BY	MDK
		CHK	MDK
		APP	MDK
		REV	1/2/83
		REV	200109

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DATE	E/C NO	DATE	E/C NO	200109
SEE	SHT 1			RELEASED FOR ASSEMBLY

SHT 8 - CMDEND
SHT 1 - INIT
SHT 4 - SECTOR + INDEX

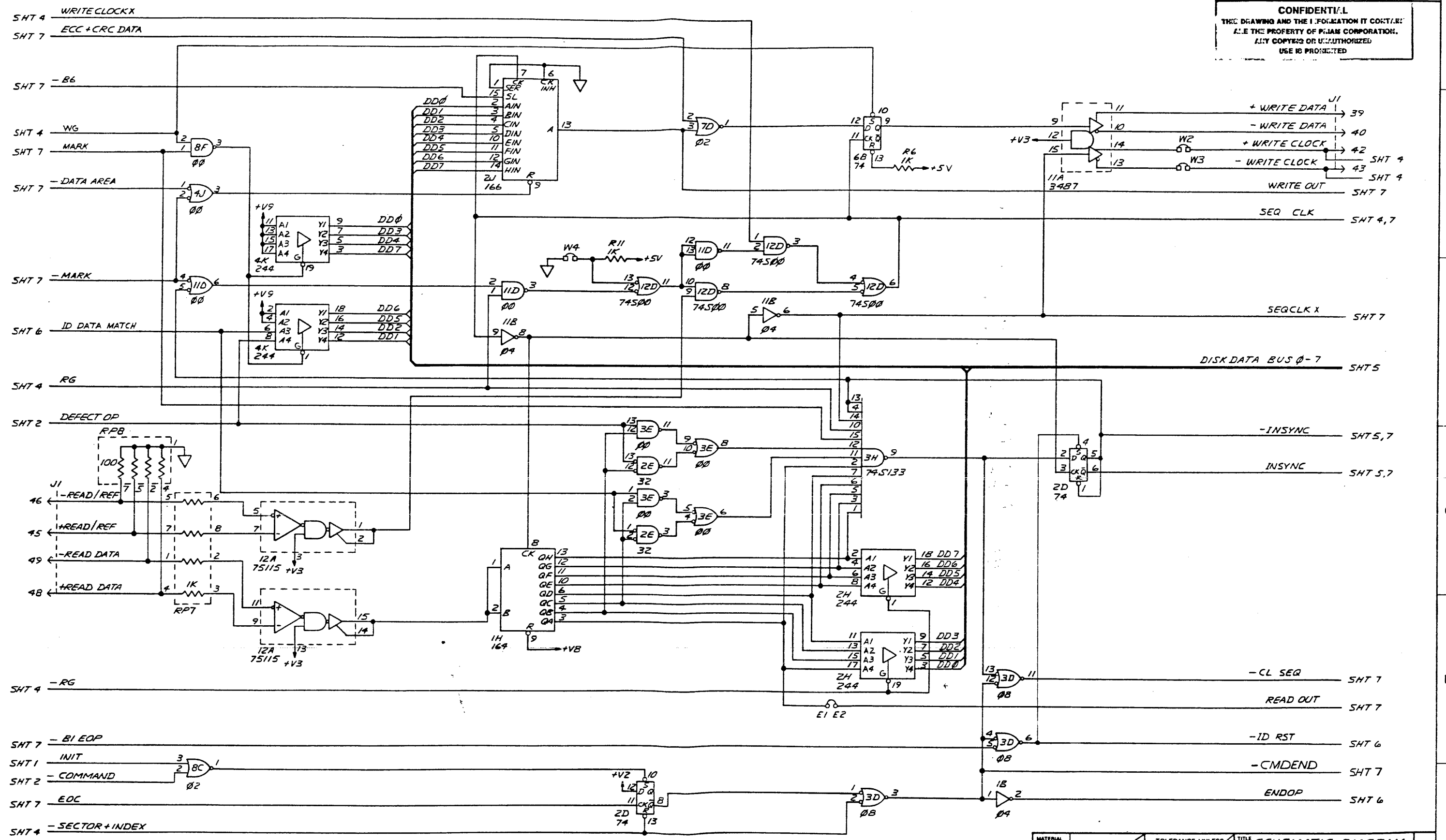


MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE	PRIAM
		SCHEMATIC DIAGRAM	
		SMART INTFC	
		DESIGN DTD 7-15-64	SCALE
		DETAIL DTD 7-15-64	SHEET 7 OF 9
		DATE 7-15-64	REV
		APPROV	D 200109

DATE	E/C NO	DATE	E/C NO	200109
SEE SHT 1				RELEASED FOR ASSEMBLY

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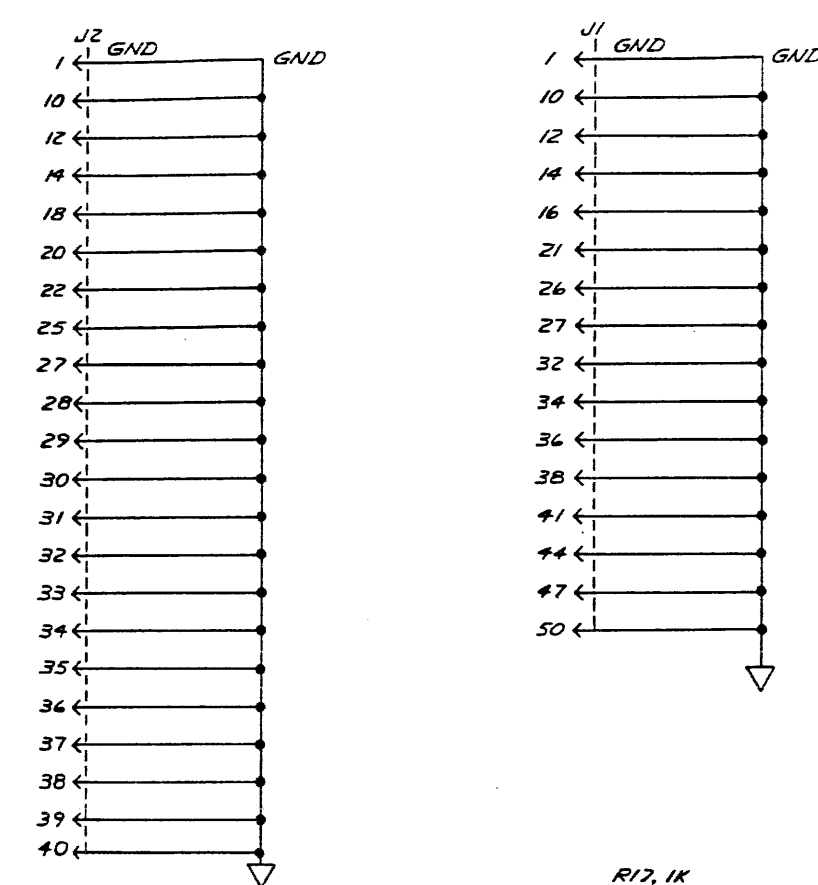
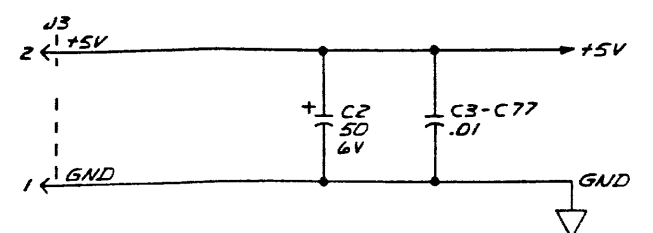
READ/WRITE LOGIC

MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE	SCHMATIC DIAGRAM
			SMART INTFC
HARDNESS	ANGULAR	DESIGN	DTM 7-18-80
SURFACE	COMPL. OUTDR	DETAIL	DTN 7-18-80
		DWG. CHK	MDR 7-18-80
		REV	200109

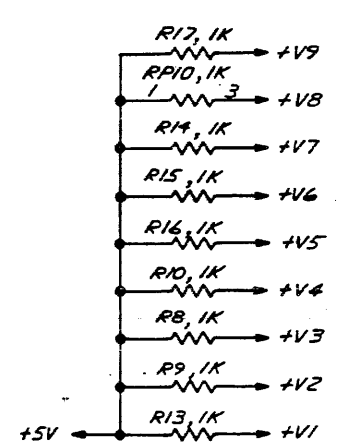
PRAM

DATE	E/C NO	DATE	E/C NO	200109
SEE	SHT 1			RELEASED FOR ASSEMBLY

I.C. TYPE	LOCATION	UNUSED ELEMENTS	+5V	GND
74LS00	2B,2C,9C,11C,11D,3E,9E,8F,10H,11H,3J,4J,3A,4B	9C1,10H1,11H1,4B1,2,2C1,2	14	7
74LS00	12D		14	7
74LS02	8C,7D,9L,4A	8C2,4A2,3,4	14	7
74LS02	9H		14	7
74LS04	1B,11B,8E,10E,8H,5B	8H5,5B1,5,6,1B4	14	7
74LS08	12B,6C,1D,3D,4D	1D1,3D3,4D2	14	7
74LS10	3C		14	7
74LS11	6F		14	7
74LS14	2A,10A	10A5,6	14	7
74LS20	7E		14	7
74LS20	9F,10F		14	7
74LS32	8B,2E,4E,6E,7F	8B1,2	14	7
74LS74	4C,5C,7C,10C,2D,5D,6D,1F,11F,12M,6B	6B1	14	7
74LS74	6H,7H		14	7
74LS85	5M,6M		16	8
74LS93	10L		5	10
74LS109	12C		16	8
74LS133	3H		16	8
74LS138	2F,3F,4F,5F		16	8
74LS139	1C		16	8
74LS161	12F,4H,5H,12H,7J,8J,9J,10J,11J,12J		16	8
74LS164	1H		14	7
74LS166	2J		16	8
74LS244	7B,2H,1J,3K,4K,7L,8L,7M,8M		20	10
74LS245	1K,7K		20	10
74LS273	8D,9D,10D,11E		20	10
74LS373	8K		20	10
74LS374	2K		20	10
74LS393	9M		14	7
74LS670	1L,2L,3L,4L,5L,6L,1M,2M,3M,4M		16	8
75461	9AB		8	4
75462	8AB,3BA,9BA,9BB,10BA,10BB		8	4
75463	9AA		8	4
2114	5J,6J,9K,10K		18	9
2716	12E,11K		24	12
75462	8AA		8	—
3487	11A	11A1	16	8
4020	10M		16	8
8085	11L		40	20
83048	1A,7A		20	10
9401	5E		14	7
75115	6A,12A		16	8
3083	5A		—	—
74LS86	1E	1E2,3	14	7
2732	12K		24	12



REFERENCE DESIGNATION	
LAST USED	NOT USED
R18	—
C77	—
RP10	RP9
W5	—
Y1	—
CR1	—
Q2	—
TP11	—
E2	—



V DESIGNATION	CONNECTED TO
V1	R13,1F4,4F6,1F10,5E2,5E5,5E8,5E9
V2	R9,4C2,4C4,6D4,5D12,5C10,5C12,5D4,2D12
V3	R8,6A5,6A3,6A13,12C1,12C15,12A3,12A13,11A12
V4	R10,12C5,12C11,10C4,10C2,7C10,10C10,10C12,7C4
V5	R16,11J1,9J1,7J10,7J7,7J1,8J1,12H9,12J1,10J1,12F9
V6	R15,12M10,11F4,11F10
V7	R14,7H10,6H12,7H4,7H2
V8	RP10-3,4H7,4H10,4H9,5H7,5H10,5H9,1H9
V9	R17,4K11,4K13,4K15,4K17,4K2,4K4

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MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE	
	LINEAR ±.XX ANGULAR ±.XX	SCHEMATIC DIAGRAM	
HARDNESS	DATE	DESIGN	SCALE
SURFACE TREATMENT	DATE	DTN	7-18-80
	DATE	DETAIL	7-18-80
	DATE	DATE CHG	7-11-80
	DATE	DATE	11-20
	DATE	DATE	200109

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