RAYTHEON

Division Operation Department	MISSILE SYSTEMS Bedford Laboratories Data Processing Systems	Contract No. Distribution aa
To	S. Wallach (S4-61)	File No.
From	S. Nissen (S2-75)	Memo No. 7675-240-74
Subject	RØM Control in PMUE	Date 10 May 1974 28 August 1974-REVISED

Reference: Memo #7675-97-74; RØM Field Specification

The following additional macros have been defined for the PMUE to date. This memo replaces 7675-153-74 dtd 27 March. Assignment of macro numbers is tentative.

21) SIDV – Set INDV

22) SSCK – Inhibit clock skip on bus

23) LDMM – Store kernel address in memory map

24) LPPG – Load PPG with ØRG.

25) PERT – Set page error trap.

26) SEC1 ⎫ These cause the kernel trace trap to be set if TM
27) SEC2 ⎬ Bit 9 is 1. It also causes disable of output buf-
fer load when SECR is 1 or TM Bit 11 is 1. SECR is selected according to RAC4 and RMDO-1. The indicated trap flop is loaded from SECR or as otherwise indicated.

RAC4	RMDO	RMD1	SECR	TRAP
0	0	0	$TM33 \cdot \overline{EXEC}$	13
0	0	1	$TM32 \cdot \overline{EXEC} \cdot \overline{STØREØP}$	14
0	1	0	$(TM8+TM34) \cdot \overline{EXEC}$	12
0	1	1	$TM34 \cdot \overline{EXEC}$	12
1	0	0	$(TM8+TM32+TM33+\overline{TM34}) \cdot \overline{EXEC}+\overline{TM11}$	15
1	0	1	$(TM32 \cdot STOREOP+TM33) \cdot \overline{EXEC}$	13,14*
1	1	0	$(\overline{TM8}+TM34) \cdot \overline{EXEC}+\overline{TM11}$	12
1	1	1	$(\overline{TM8}+TM34) \cdot \overline{EXEC}$	12

* 13 Loaded by $TM33 \cdot \overline{EXEC}$, 14 by $(TM32 \cdot \overline{STOREOP \cdot EXEC})$

8) TSN1   -   Enable a Tristate value onto TB0-15 as described by the table in TSN2.

29) TSN2   -   Enable a tristate value onto TB0-15 according to the following table.

RAC4	RMD0	RMD1	TB0-7	TB8-15
0	0	0	TM0-7	TM8-9,$\overline{10}$,11-15
0	0	1	TMP0-7	
0	1	0	000000,SPR2-3	
0	1	1	000000,SPR2-3	
1	0	0	000000,MMP0-1	MMP2-9
1	0	1	000000,MMP0-1	
1	1	0	RSN0-7	
1	1	1	RSP0-4,RPG0-1,RKRA	

31) ØBRS   -   Load the output buffer unless the output queue is not ready. Transmission type is 01, RMD).

32) ØBF2   -   This macro defines the transmission type for use with the RØB field.

RMD0	RMD1	TRANSMISSION TYPE
0	0	1 1 1
0	1	0 1 0
1	0	0 0 1
1	1	0 1 0, 0 1 1*

*Dependent on data type TM32-34.

33) STPS   -   STP instruction step.

34) SBPG   -   Set BLPG to $\overline{RMD0}$

35) SNXT   -   Cause next actions to occur.

36) SKPG   -   Set NKPG to $\overline{RMD1}$

38) SKBPG   -   Perform both 34 and 36.

37) ØVER   -   Toggle address trap override flop.

39) SLUCK   -   Toggle PMU clock select.

NEW RØM FIELDS

1) Kernel Allow (RKRA) (1 bit)

   This bit, when 1 requires access to the kernel area on this step's memory access deviation causes a trap.

2) PUSH ST2 (RST2) (1 bit)

   This bit, when 1, stores the RØM address of the next consecutive instruction in ST2.

3) Kernel Register Control (RKR0-2) (3 bits)

   The ØRG, PKR and DKR registers are controlled as follows:

RKR0	RKR1	RKR2	FUNCTION
0	0	0	PKR ← TB12,TB13;DKR ← TB14,TB15
0	0	1	PKR ← TB06, TB07
0	1	0	DKR ← TB06, TB07
0	1	1	DKR ← PKR
1	0	0	PKR ← ØPR6,ØPR7
1	0	1	PKR,DKR ← TB06, TB07
1	1	0	IDLE
1	1	1	LOAD ØRG

4) Output Buffer Control (3 bits)

   RØBO, when a 1, causes a load of the output buffer unless it is 1) busy, or 2) a security macro has been specified, with a security violation occurring or TM Bit 3 being 1.

   RØB1-2 selects the output buffer format as follows:

RØB1	RØB2	OUTPUT BUS BITS 0-35
0	0	ØPCD0-7,1111,TM12-23,AU08-15,$\overline{\text{ØPCD7}}$,000
0	1	ØPCD0-7,1111,TM12-23,AU07-14,$\overline{\text{ØPCD7}}$,000
1	0	ØPCD0-7,1111,TM12-31,$\overline{\text{ØPCD7}}$,000
1	1	TM0 0-35

where ØPCD is set to

0, RSP5,0,0, RSP0, RSP1, RSP2, RSP3

and the selected transmission type will be single or double word command according to RSP4 unless either ØBFS or ØBF2 or ØBRS is specified, in which case ØPCD will be determined as shown and transmission type will be controlled by the modifier field as described for ØBFS and ØBF2 and ØBRS.

When RØB0-2 is 010, an acknowledge will be sent on the input bus. An acknowledge will also be sent if RØB0-2 is 011 and there is DATA on the input bus.

5) Page Selector (2 bits)

The page selector is controlled as follows:

RPG0	RPG1	PGS
0	0	DKR
0	1	PPG
1	0	ØRG
1	1	PKR

When RAS0-1 = 11, RPG1 is forced to 0.

6) Sequence Number Select (= $\overline{RSP3}$)

This line, when a 1, causes a sequence number of 11 to be appended to the present output buffer load. When a 0, the sequence number received with the last continue or external instruction interrupt will be sent. When ØBFS macro is selected and SPR0 = 1, sequence number 11 will be sent regardless of the state of this bit.

7) Changes to specification referenced:

    15. <u>Address Select</u>

        ØPR5 is replaced by ØPDB.

    17. <u>Macro Control</u> (8 bits)

        The macro field contains an additional bit which is the MSB of the field, but is named RAC5. Additional macros were defined earlier in this memo.

        16) TTRS -

            The condition field (RSQ) is also expanded by 1 bit which is the MSB and is named RSQ4. Additional conditions are:

            16) SSCF0

            17) RESP0

            18) OPDB1

            19) CNTU1

            20) DIMW1

            21) PREQ1

            22) SPRO1

            23) EOBK1

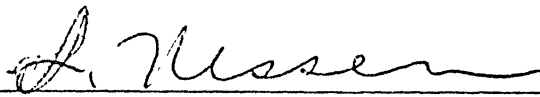   18. <u>Sequence Control (5 bits)</u>

        The special sequence conditions listed in the specification only apply to the ROM when it is in locations 0-255. When in 256-511, they are replaced by 32 others as listed below.

     0) UNCONDITIONAL TRANSFER TO RNA
     1) TRANSFER TO RNA0-8, ØQFLO
     2) TRANSFER TO RNA0-8, RESP0
     3) TRANSFER TO RNA0-8, BLPG1
     4) TRANSFER TO RNA0-8, DATF1
     5) TRANSFER TO RNA0-8, MTYP1
     6) TRANSFER TO RNA0-8, SPRO
     7) TRANSFER TO RNA0-8, DAMF1
     8) RBURST7 (APL NAME)
     9) RBURST3
    10) RBURST2
    11) RUNIV4
    12) RUNIV3

13) RPAGERD2F
14) TRANSFER TO RNA0-6, SPR1-3
15) R475
16) DMFT
17) UNUSED
18) UNUSED
19) TRANSFER TO RNA0-8, NKPGO
20) ROPCDV
21) RINIMV
22) RREGADV
23) TRANSFER TO RNA, NKPGO, SPRO
24) SECURITY LOCAL (e.g. RVIRTRDIOB2)
25) SECURITY REMOTE (e.g. RRDINV2)
26) RMINDV2
27) RVIRTDØP
28) RREGINV
29) RO42
30) RINDEXV
31) NEXT

The full ROM format is now as follows: (70-81 are extensions)

0 2	3 5	6 9	10 11	12 13	14	15 16	17
P REG	IA REG	IB REG	AD BUS	DTBUS	ADSWITCH	AUBUS	SPWRITE

18 19	20 25	26	27 31	32 39	40 43	44	45 47
TMCYCLE	SP ADDRESS	M BUS	TM SELECT	AU	TM ADDRESS	ITC	TM,SP SIGNS

48 52	53 54	55 64	65 68	69	70	71	72
MACRO CONTROL	MACRO MODIFIER	NEXT ADDRESS	SEQUENCE CONTROL	RS	MACRO	SEQUENCE	KERNEL ALLOW

73	74 76	77 79	80 81
RS2	KERNEL REG	OUTPUT BUFFER	PAGE SELECT

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