# 4000 ELECTRONIC DATA PROCESSING SYSTEM

ROYAL McBEE · *data processing division*
PORT CHESTER · NEW YORK

# RPC 4000

Preliminary
Product Information

ROYAL McBEE Corporation, Data Processing Division
EDP Equipment Information Release F.034 Rev.

Rev.5/17/60

# RPC–4000

# PRELIMINARY PRODUCT INFORMATION

# (RELEASE F. 034)

-CONTENTS-

# PREFACE

This release is intended to serve as a preliminary operations-manual for the RPC-4000 digital computer. As such, it presents the salient characteristics of the computer and its basic input-and output equipment. Some previous knowledge of computer techniques and terminology is a necessary pre-requisite for full appreciation of the RPC-4000 information herein presented.

It has been said that a new generation of computers has appeared on the EDP horizon, bringing larger capacity, higher speed, increased reliability, and greater economy than heretofore possible. The RPC-4000 exemplifies this new class of machine, it represents the most recent advances in technicological achievement and the culmination of intensive logical design.

The RPC-4000 is truly a multi-function, multi-purpose management-aid, applicable to solution of the widest range of problems in scientific, engineering, or business activities.

The reliability, capability, flexibility, and variability of this new system will set a new standard for the computer field.

# RPC-4000
# SYSTEM DESCRIPTION

The RPC-4000 is a general purpose "solid-state" electronic computer. Fully transistorized and internally programmed, it features large capacity, small size, high speed, and reliability at low cost, to meet the needs of scientific, engineering, and business data processing.

The RPC-4000 system is comprised of a model 4010 computer and an array of input-output units selected to meet the particular needs of an individual application. Systems control is exercised by the computer in compliance with the internally stored program. A "one-over-one" instruction format provides maximum flexibility and convenience, a wide range of computer-commands simplifies programming, and an exclusive "repeat-execution" feature affords unusual speed benefits.

Data is stored, manipulated, and processed in binary notation with internal conversion from a conventional system of data-coding. The full range of symbols, letters and numbers is handled easily with no reduction in capacity. Arithmetic processes include addition, subtraction, multiplication, and DIVISION in either of <u>two</u> registers.

The principal components of the RPC-4000 are memory, control, arithmetic, and (selected) input-output units. These function together as an integrated system according to the operator-devised "program" and automatic, built-in, logic of the system.

# RPC-SERIES 4000
# ELECTRONIC COMPUTING SYSTEM

| | Model | Description |
|---|---|---|
| COMPUTERS: | 4010 | Computer |
| INPUT/OUTPUT EQUIPMENT: | 4410 | Photo-Electric Reader |
| | 4430 | Punch and Reader |
| | 4431 | Auxiliary Punch and Reader |
| | 4440 | High-Speed Punch |
| | 4480 | Auxiliary Tape Typewriter |
| | 4500 | Input-Output Tape Typewriter System |
| | 4600 | Auxiliary Tape Typewriter System |

# "THE MODEL 4010 COMPUTER"

The computer unit contains the memory, arithmetic, and control elements. It is fully transistorized and requires no special air-conditioning or site-preparation. The low power requirements, long life expectancy, and extreme reliability of this solid-state computer are further enhanced by the automatic parity-checking of input-output code-validity, high operational speeds, and multiple input-output capacity.

## Word-Structure

The basic unit of information is called a "word". It contains 32 BITS (binary-digits) and may represent either a "DATA-WORD" or an "INSTRUCTION-WORD". When used for data, one bit of the word is used for an algebraic "sign", the remaining 31 may represent up to 9 significant "decimal" digits.

When used to represent an instruction the word may contain one complete "basic" instruction composed of a "command" (5 bits), "operand-address" (13 bits), "next-instruction-address" (13 bits) and an "index-tag" (1 bit). These 4 parts of an instruction are explained in subsequent sections of this release.

Each bit in a word may be a "0" or a "1" in conformity with the binary system of positional notation. This system of data representation affords significant advantages to the computer, particularly in data storage efficiency and, consequently, economy of hardware.

Following is an illustration of the basic word-structure:


Fig. II -2

A data-word is arranged:


Fig. II - 3

An instruction word is arranged:

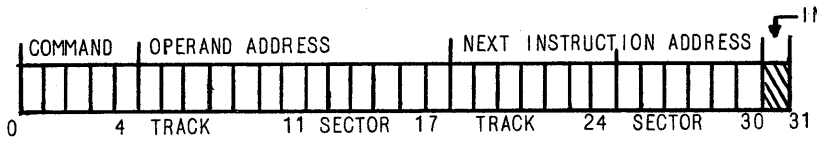



Fig. II - 4

Data transfer is usually accomplished in 1-word units. However, part of a word may be "extracted" and/or operated upon in certain instances at the discretion of the programmer. Additionally, multiple words may be transferred in the repeat mode of operation.

# MEMORY

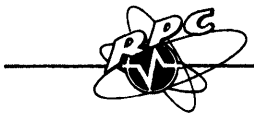
The computer "memory" element is a unique 3600rpm Magnetic Drum with a total storage of 8008 words. The "main memory" section contains 7872 words with an average access time of 8.5 milli-seconds. Additionally, there are 128 words with "dual-access" facility (described later) and 8 words of high-speed memory with an access-time of 1 milli-second average, 2ms MAXIMUM.

## A. MAIN MEMORY

The main-memory surface of the drum contains 123 "tracks". Every track is divided into 64 sectors capable of storing 32 bits (1-word) each. The 123 tracks are "addressed" as 000 through 122 and the sectors as 00 through 63. (See illustration)

Any word location in main memory is selected by specifying the track and sector addresses. Thus, word address 01723 designates the word found in track 17 at sector 23. Address 10961 designates the word in track 109 at sector 61. Hence, 123 tracks of 64 sectors (123 x 64) affords a capacity of 7872 words in main memory, with "addresses" ranging from 00000 to 12263.

Each track has one associated read-write head for data recording and retrieval. The track portion of an address (1st 3 digits) selects the magnetic head ..... its physical location at the drum is of no particular concern to the operation.



B. DUAL ACCESS STORAGE

In addition to the main-memory section, the drum contains 2 tracks with dual access to the data in each track.

1. One dual-access track has 2 read-write heads located 16 sectors apart with each separately addressed. Heads 123 and 125 are on this same track, but head 125 is 16 sectors "behind" 123; that is, a word will pass head 123 first then pass head 125 exactly 16 word-times later. Thus any word on this track may be referred to by either head.

   For example: (word) 12300 = 12516
   (word) 12301 = 12517

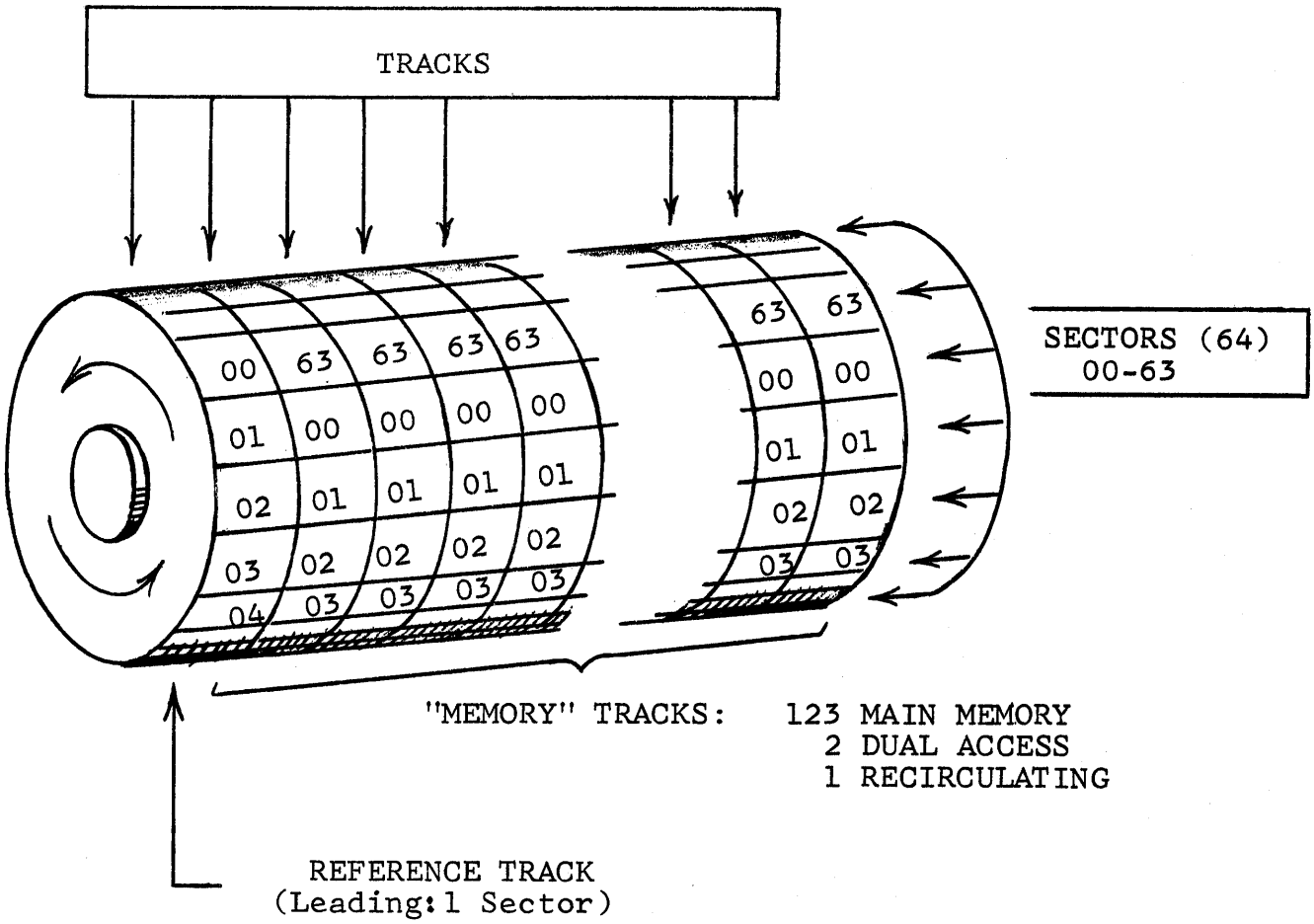
2. Similar characteristics apply to the second "dual-access" track which holds read-write heads 124 and 126. They operate on and share the same track, but with head 126 exactly 24 sectors behind 124.

   Thus (word) 12400 = 12624
   (word) 12401 = 12625

   In each case, the lower numbered head is called the "reference" head because it is in phase with main memory.

   These dual-access tracks have an INITIAL access time of 8.5 milliseconds (average). However, a second access to any word in these tracks may be effected in 4 or 6 milliseconds after the initial-access.






RPC-4010

MAGNETIC DRUM
"STORAGE"

Fig. II - 5

# RECIRCULATING (HIGH SPEED) STORAGE

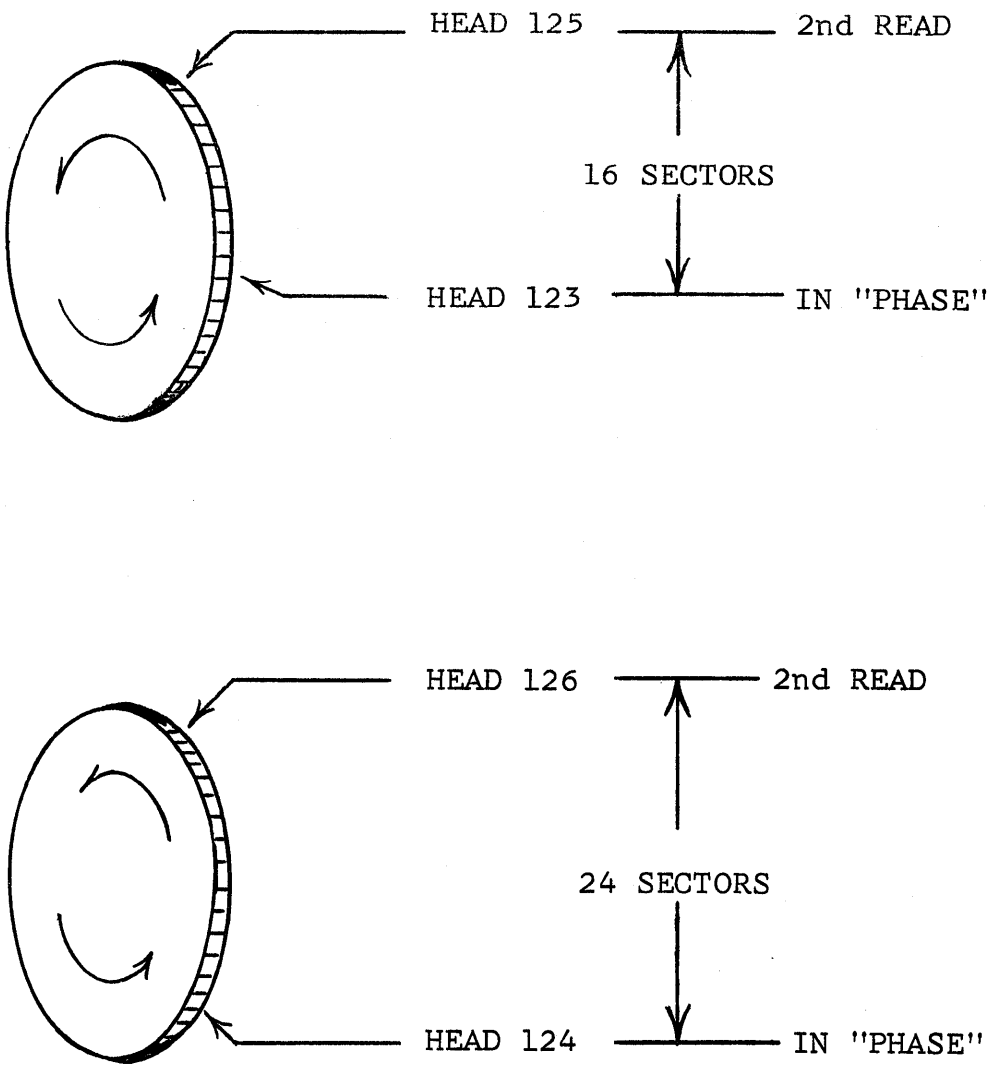
There is one track on the drum devoted to HIGH-SPEED (access) storage of 8 words. This is called a "recirculating line" and has a track address of 127. The sector address is modulo 8, thus sector designations 0, 8, 16, 24, .. 56 all apply to the same word.

This high-speed storage provides 1 millisecond (average) access-time to any of the 8 words in the track. It is used for data which is referred to many times by a program. The extremely rapid access affords significant advantages in program-execution time.

Since 8 sector addresses will select the same word, the programmer may select that which affords minimum access time to the data in this line.

Note: The recirculating line may be considered as 8 "identical blocks" (utilizing a common drum track) of 8 sectors each wherein the same 8 words are recorded in all blocks but with non-conflicting, separate addresses. The read-write head is "in phase" with the main-memory and is used for the data insertion and retrieval. The individual read-head and write-head are employed only for the recirculation process.






RPC-4010

MAGNETIC DRUM
"DUAL-ACCESS TRACKS"

Fig. II - 6

# COMPUTING CONTROL

A. NORMAL

All computer functions are controlled by the 4 registers which comprise the "computing control unit". These are re-circulating lines on the magnetic drum.

All internal calculation is accomplished by directing information to the computing control unit (from memory), processing it, and directing it (after processing) to memory or an output device. Thus, the 4 registers in the Computing Control Unit are the "heart" of the computer. Described below, they are designated as:

U - Upper Accumulator

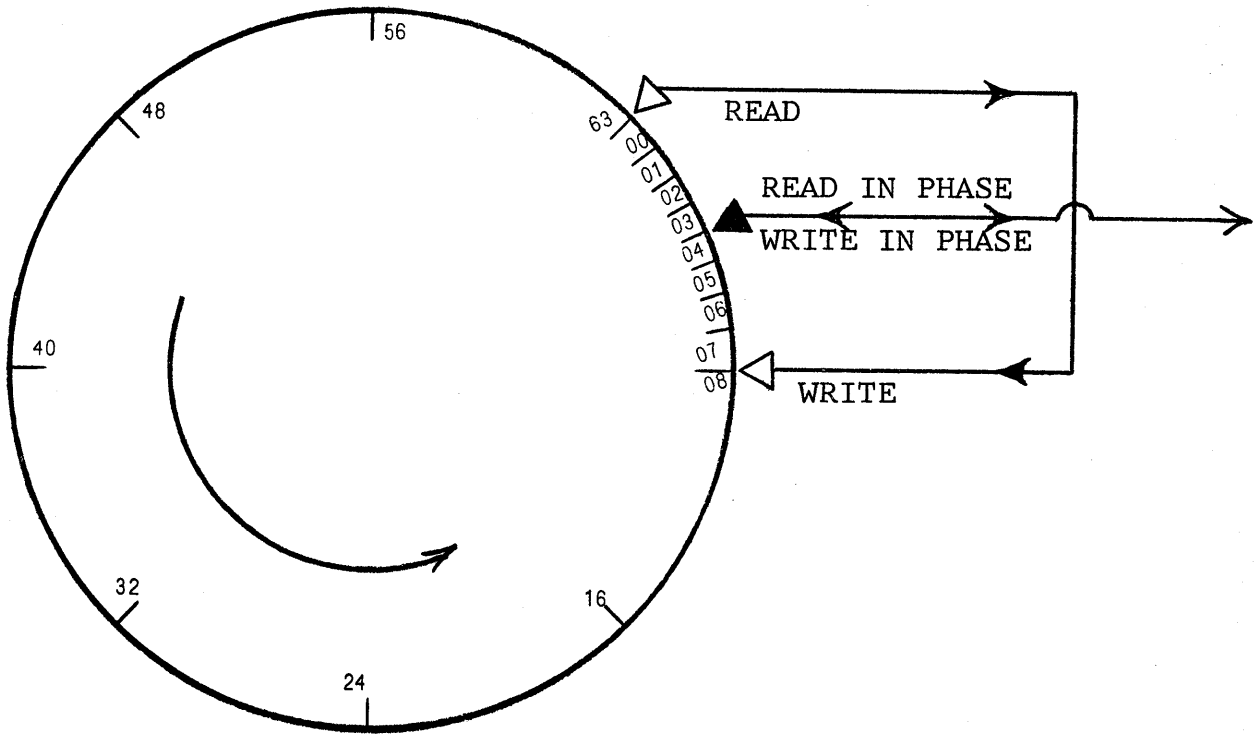
L - Lower Accumulator

C - Command Register

X - Index Register

"U" REGISTER

The Upper Accumulator, U, may contain the result of addition or subtraction, the sign and most significant half of a multiplication product, or the quotient of a division process. It is used in comparisons and certain other functions as described in the Operation-Codes section. Prior to the execution of a command pertaining to this register, it will contain one of the operands, the other operand being specified by the instruction.




RPC-4010

MAGNETIC DRUM
"RECIRCULATING LINE"

Fig. II - 7

"L" REGISTER

The Lower Accumulator, L, may contain the result of an addition or subtraction, least significant half of a product, or the remainder in a division process. It is used in some masking operations and certain other functions as described in the operation-codes section. Prior to execution of a command pertaining to this register it will contain one of the operands, the other being specified by the instruction.

"C" REGISTER

The Command Register, C, contains the instructions being executed. Any instruction to be executed must appear in this register.

An instruction is composed of 4 parts, all of which must be present in the C register. As previously indicated, an instruction word of 32 bits includes:

1. Command, 5 bits (0-4)
2. Operand address, 13 bits (5-17)
3. Next instruction address, 13 bits (18-30)
4. Index tag, 1 bit (31)

"X" REGISTER

The index register X may contain a modifier which is added to any instructions that contain a bit in the Index Tag position of the instruction. Only bits 5-17 (corresponding to the Operand Address) are added to an instruction. The sum of the index register X and the tagged instruction is placed in the command register to be executed by the RPC-4000. The index register X and the instruction (in memory) are not changed by this sequence.



An example:

The RPC-4000 is to execute the instruction at 2040, which is:

| ADU | 01744 | 01941 | 1 |
|---|---|---|---|

. The index register (X) contains

| 0 | 0 | 00203 | 00000 | 0 |
|---|---|---|---|---|

. The generated instruction that would appear in the command register (C) is

| ADU | 01947 | 01941 | 1 |
|---|---|---|---|

and this would be the actual instruction executed. Neither the index register (X) which contains

| 0 | 0 | 00203 | 00000 | 0 |
|---|---|---|---|---|

nor memory location 2040 which contains

| ADU | 01744 | 01941 | 1 |
|---|---|---|---|

are affected.

The index register may be modified by instructions which are explained in the section on Operations Codes. Only bits 5-17 of the index register X are used in the preceding function.

The index register X has two other functions which are explained in the Extension Control section. Neither of these has any effect on the indexing operation, they just share the index register X, to reduce circuitry.



B. EXTENSIONS

The RPC-4010 computational ability may be extended by program modifications, as follows:

1. Extending the lower register (L) to 8 individual accumulators.
2. Repeat-execution of some instructions (up to 127 times) with automatic "address" modification.

These modifications, often used together, provide unusual flexibility as described below:

1. L REGISTER EXTENSION

The command EXC, may be used to turn the lower register to 8 individual accumulators or to one accumulator. If it is set to 8 accumulators, they may be referred to as $L_0$ $L_1$ $L_2$.... $L_7$. The particular lower accumulator will be determined by the sector part of the operand address, (more explicitly, the least 3 bits of the sector part of the operand address). In other words, the sector address (modulo 8) will determine which lower accumulator is affected:

i.e., 1904, 2012, 8952 will all affect lower accumulator $L_4$.

Note: Overflow does not carry from one lower accumulator to another, but any overflo will turn "ON" the branch control toggle, BC. This switch may be "tested" by an instruction (TBC) to determine its state.

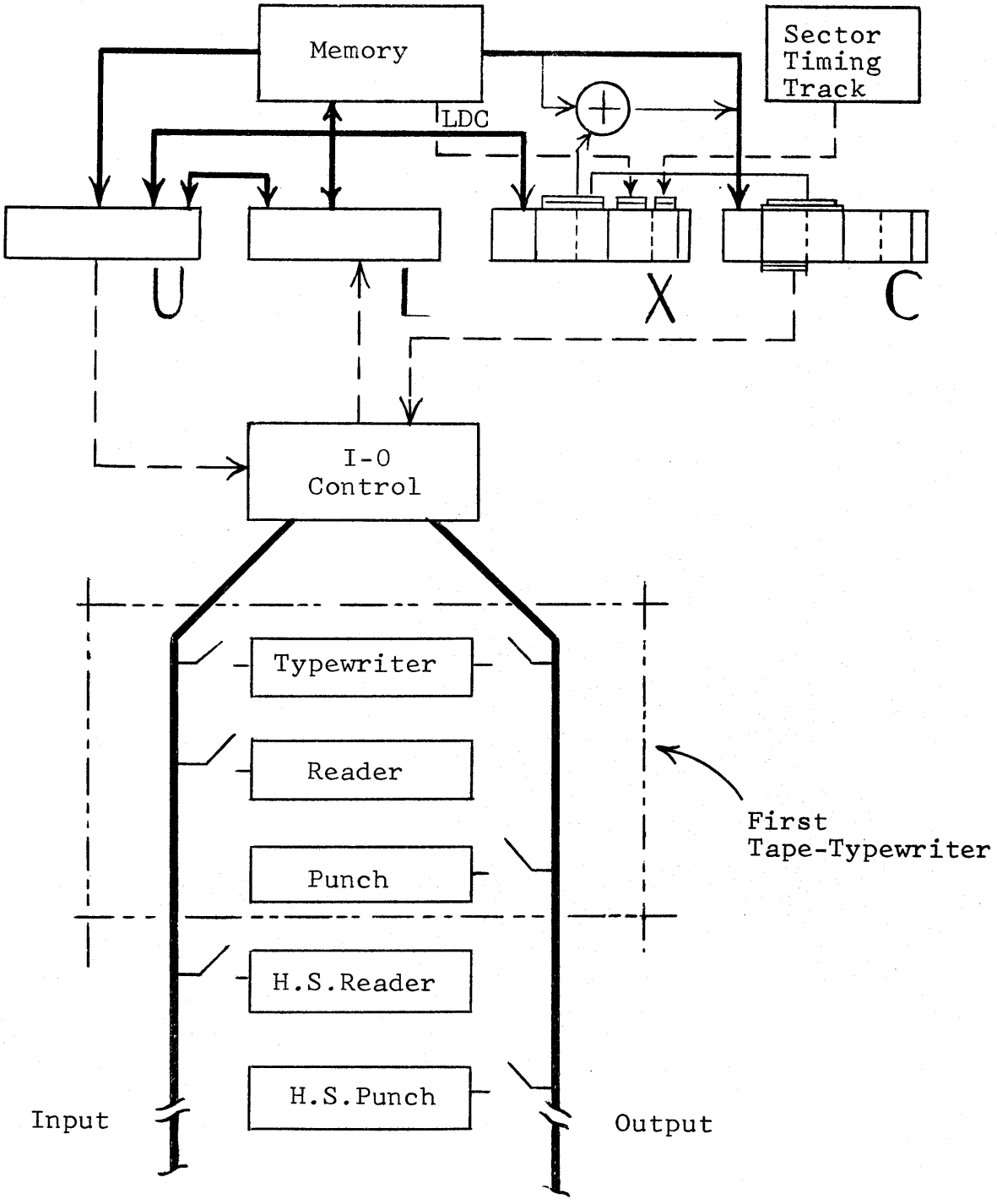
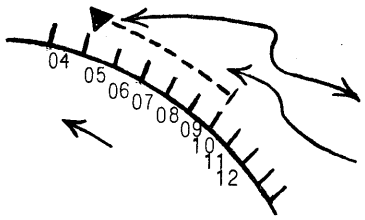

Memory
Sector
Timing
Track
LDC
U
L
X
C
I-O
Control
Typewriter
Reader
Punch
H.S.Reader
H.S.Punch
Input
Output
First
Tape-Typewriter

Fig. II - 10

## 2. REPEAT EXECUTION

It is helpful to visualize the layout of a typical track when thinking of the repeat execution function of the RPC-4000.




Read-write head on track 019

Repeat (EXAMPLE)

Fig. II - 8

In the illustration, the read-write head on track 19 is typical of all memory. Assume it is reading the word at sector 05 which is going through "add" circuits and being added to the upper accumulator. This circuit is normally active only for one word time; in this case, the time the read-write head is over sector 05. The repeat execution function keeps this circuit active for up to 127 more word-times. If the ADU 0 1905 XXXXX 0 were repeated 4 times, the contents of 01905 through 01909 would be added to the upper accumulator U.

A 7-bit portion of the index register X is used to control the number of times the instruction is repeated. The portion used corresponds to the track position of the "next instruction address" in the index register X, bits 18-24.

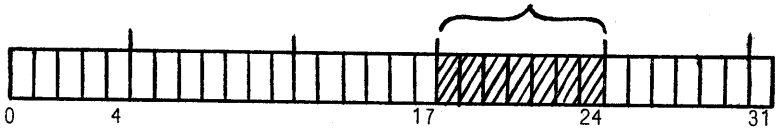



Fig. II - 9

The repeat control portion of the index register X is loaded with the LDC command. The next instruction to be executed will be repeated provided it is not an LDC command also. It will not change tracks when reading or writing from memory. Operation will continue from sector 63 to sector 00 of the same track.

The repeat control and extension of the lower accumulator to 8 words can be used together for 8 word block transfer and 8 word block arithmetic.

The repeat control function may be used with the CME or CMG instructions which compare the upper accumulator U with memory. When the comparison test begins, the sector reference timing track is copied into the lower 6 bits (25-30) of the index register X. This reference track is always one sector ahead of the actual sector under the read-write heads.

When a comparison is true, the branch control toggle, BC, is turned on and the sector reference timing track is inhibited from being copied into the index register. The comparison continues, however, for as many word times as there are left in the repeat control portion of the index register.

The programmer may determine if a comparison was made, by testing the branch control toggle BC; and at what location it was made, by transferring the contents of the index register X to the upper accumulator U (by an EXC command) and examining the sector portion. The track portion must be the same as the compare instruction since the repeat command cannot change the track address.



# COMPUTER INSTRUCTION

Instruction Cycles

Reference to the block-diagram of the system organization will provide an indication of the paths over which information may flow. Heavy lines represent transfer in whole-word units, light lines indicate "operand-address" (bits 5-17) transfers, while broken lines show partial-address transmission.

A typical instruction-cycle proceeds in the following manner:

1. The word contained in the location shown by bits 18-30 ("next-instruction-address") of the Command Register is transferred into the command register, replacing the previous contents of that register.
2. The instruction in the Command Register (as result of 1 above) is executed. Information is transmitted according to the particular operations demanded by the instruction.

This completes an Instruction cycle, where-upon the computer looks for the next-instruction-word and begins the next cycle (Step 1). This sequence is followed by the computer for all instructions EXCEPT when the next-instruction being transferred from memory contains a bit in position 31, the "index-tag". In this case the operand-address is added to the corresponding $(X)_{5-17}$ (operand-address) in the Command register (Step 2). The addition is performed as the word is being transferred into the command register.

# OPERATION CODES

The operations of the RPC-4000 are grouped under arithmetic, logical, and input-output. In general, arithmetic operations operate on a full* word of 31 bits plus sign; logical operations affect only the address portion of the word or deal with manipulation of the index register or repeat function; input-output operations concern the entry and exit of information into the computer.

Numeric and mnemonic codes for each operation are explained in terms of the following symbols:

| | |
|---|---|
| loc | represents the location of the instruction being executed |
| m | represents any memory location (used for operand address) |
| n | represents any memory location (used for next instruction address) |
| U | represents upper accumulator |
| L | represents lower accumulator |
| $L_8$ | represents lower accumulator when it is 8 words |
| $L_i$ | represents one lower accumulator when it is 8 words i=0,1,..7 |
| C | represents command register |
| X | represents index register |
| → | represents replace |
| mj | represents consecutive memory locations in same track |
| ( ) | represents the contents of |
| $m_s$ | represents the sector portion of any memory location |
| $m_t$ | represents the track portion of any memory location |
| $\alpha$ | represents the number of times to repeat an instruction |
| I | represents the integer part only |

.....

*Note: Selected portions of a word may be operated upon; this is accomplished by "masking" techniques.

When the lower accumulator has been extended to 8 words the particular lower accumulator is selected by the operand address in the following manner:

$L_i = (m_s)$ modulo 8

This notation means that the particular lower accumulator is determined by the remainder of: sector portion of (m) divided by 8.

Examples

| | |
|---|---|
| m = 10309 | 09 ÷ 8 remainder = $1 \sim L_1$ |
| m = 02117 | 17 ÷ 8 remainder = $1 \sim L_1$ |
| m = 03151 | 51 ÷ 8 remainder = $3 \sim L_3$ |

02 RAU m n — Reset and Add to Upper

Normal (m) ⟶ (U)

Repeat (mj) ⟶ (U)

03 RAL m n — Reset and Add to Lower

Normal (m) ⟶ (L)

$L_8$ (m) ⟶ ($L_i$) where $L_i$ = ms modulo 8

Repeat (mj) ⟶ (L)

$L_8$, repeat (mj) ⟶ ($L_i$) where $L_i$ = mjs modulo 8

05 MST m n — Masked Store (where 0 bits in U, (mj) unchanged)

Normal (L) ⟶ (m) where 1 bits in U

$L_8$ ($L_i$) ⟶ (m) where 1 bits in U, $L_i$ = ms modulo 8

Repeat (L) ⟶ (mj) where 1 bits in U

$L_8$, repeat ($L_i$) ⟶ (mj) where 1 bits in U, $L_i$ = mjs modulo 8

10 DVU m n — Divide Upper

Normal 1. 0 ⟶ (L)

2. (U) ÷ (m) = quotient and remainder

3. quotient ⟶ (U)

4. remainder ⟶ (L) & ≠ ø

Overflow (U) ≠ (m)

11 DIV m n — Divide

Normal 1. (U) & (L) ÷ (m) = quotient and remainder

2. quotient ⟶ (U)

3. remainder ⟶ (L) & ≠ ø

Overflow (U) ≠ (m)

14 MPY m n — Multiply

Normal 1. $0 \longrightarrow (L)$

2. (U) x (m) = product most significant, least significant

3. product most significant $\longrightarrow$ (U)

4. product least significant $\longrightarrow$ (L)

15 MPT m n — Multiply by Ten

Normal $m_t = 0$ $10 \times (U) \longrightarrow (U)$

$m_t = 64$ $10 \times (L) \longrightarrow (L)$

$L_8$ $m_t = 0$ $10 \times (U) \longrightarrow (U)$

$m_t = 64$ $10 \times (L_i) \longrightarrow (L_i)$ where $L_i$ = modulo 8

repeat $m_t = 0$ $10^{\mathcal{L}+1} \times (U) \longrightarrow (U)$

$m_t = 64$ $10^{\mathcal{L}+1} \times (L) \longrightarrow (L)$

$L_8$, repeat $m_t = 0$ $10^{\mathcal{L}+1} \times (U) \longrightarrow (U)$

$m_t = 64$ $10^{\frac{(\mathcal{L}+1)I}{8}} \times (L_i) \longrightarrow (L_i)$ for i = 0 thru 7

If $\mathcal{L}+1$ modulo 8 $\not\equiv$ 0 (& remainder R)

then $10^1 \times (L_i) \longrightarrow (L_i)$ for i = (ms) modulo 8

thru i = (ms + +2) modulo 8

18 EXT m n — Extract

normal (U) and (M) $\longrightarrow$ (U)

repeat (U) and (mj) $\longrightarrow$ (U)

a bit-by-bit mask, using "logical" product of U and M or mj into U.

19 MML m n — Mask Merge Lower

(L) unaltered where ∅ in (U)

| | | |
|---|---|---|
| Normal | (m) $\longrightarrow$ (L) | where bits in (U) |
| $L_8$ | (m) $\longrightarrow$ $(L_i)$ | where bits in (U) $L_i$ = ms modulo 8 |
| repeat | (mj) $\longrightarrow$ (L) | where bits in (U) |
| $L_8$, repeat | (mj) $\longrightarrow$ $(L_i)$ | where bits in (U) $L_i$ = mjs modulo 8 |

24 STU m n — Store Upper

| | | |
|---|---|---|
| Normal | (U) → (m) | |
| Repeat | (U) → (mj) | |

Note: See page III-8 for Store Lower

26 CLU m n — Clear Upper

| | | |
|---|---|---|
| Normal | (U) → (m)<br>0 → (U) | |
| Repeat | (U) → (mj)* | |

27 CLL m n — Clear Lower

| | | |
|---|---|---|
| Normal | (L) → (m)<br>0 = (L) | |
| $L_8$ | ($L_i$) → (m)<br>0 = (L) | where $L_i$ = ms modulo 8 |
| Repeat | (L) → (mj)*<br>0 = (L) | |
| $L_8$, repeat | ($L_i$) → (mj)*<br>0 = (L) | where $L_i$ = mjs modulo 8 |

28 ADU m n — Add to Upper

| | | |
|---|---|---|
| Normal | (U) + (m) → (U) | |
| Repeat | (U) + (mj) → (U) | |

29 ADL m n — Add to Lower

| | | |
|---|---|---|
| Normal | (L) + (m) → (L) | |
| $L_8$ | ($L_i$) + (m) → ($L_i$) | where $L_i$ = ms modulo 8 |
| Repeat | (L) + (mj) → (L) | |
| $L_8$, repeat | ($L_i$) + (mj) → (L) | where $L_i$ = mjs modulo 8 |

30 SBU m n — Subtract from Upper

| | | |
|---|---|---|
| Normal | (U) - (m) → (U) | |
| Repeat | (U) - (mj) → (U) | |

*After first clear, the accumulator is set to zero for all succeeding clears.

31 SBL — Subtract from Lower

Normal: $(L) - (m) \rightarrow (L)$

$L_8$: $(L_i) - (m) \rightarrow (L_i)$ where $L_i$ = modulo 8

Repeat: $(L) - (mj) \rightarrow (L)$

$L_8$, repeat: $(L_i) - (mj) \rightarrow (L_i)$ where $L_i$ = mjs modulo 8

Logic

00 SNS m n — Sense

1. BC turned off

2. a) $m_t = 0$ — Stop computation

   b) $m_t = 1,2,4,8,16,32$ — BC on if corresponding sense switch is depressed

01 CXE m n — Compare Index Equal

1. BC turned off

2. $m = (X)_{5-17}$ — BC on

04 SAU m n — Store Address Upper

Normal: $(U)_{5-17} \rightarrow (m)_{5-17}$

Repeat: $(U)_{5-17} \rightarrow (mj)_{5-17}$

06 LDC m n — Load Counter

1. $(m)_{18-24} \rightarrow (X)_{18-24}$

2. Next instruction will be repeated $(m)_{18-24}$ times.

07 LDX m n — Load Index m

$m \rightarrow (X)_{5-17}$

LDX m n 1 — Increment Index m

$(X)_{5-17} + m \rightarrow (X)_{5-17}$

09 EXC m n — Exchange

$m_t = 1$ (U) ⟶ (L)

$m_t = 2$ (L) ⟶ (U)

$m_t = 4$ (U) ⟶ (X)

$m_t = 8$ (X) ⟶ (U)

If the lower accumulator is 8 words the $L_i$ selected will be determined as follows: $L_i$ = ms modulo 8

Any or all of the above exchanges may be executed with the same instruction

i.e., $m_t$ = 1 and 2, $m_t$ = 3

(U) ⟶ (L)

(L) ⟶ (U)

Note: m = 2 and 8, m = 10

(L) ⟶ (U)

(X) ⟶ (U)

the upper accumulator will contain the "logical or" of (L) and (X).

$m_t = 16$ set the lower accumulator to 8 words

$m_t = 32$ set the lower accumulator to 1 word

One of these may also be executed with the same instruction as the above exchange

When changing the lower accumulator from 8 to 1 words, the word that is preserved in L is $L_i$ = ms modulo 8

$(L_i) \longrightarrow L$

When changing the lower accumulator from 1 to 8 words, the lower will be preserved in $L_i$ as follows: $L_i$ = ms modulo 8

$(L) \longrightarrow (L_i), (L_i-1), (L_i-2), (L_i-3)$

The contents of the other words in $L_8$ depend upon prior instructions and the degree of optimization employed.

12 SRT, SLT — Shift right, Shift left

(U) and (L) shifted the number of positions specified in the sector address of the operand part of the instruction. The shift will be right if track zero is specified and left if track one is specified.

13 SLC m n — Shift Left and Count

(U) and (L) normalized $\longrightarrow$ (U)

Count $\longrightarrow$ ms of (L)

25 STL m n — Store Lower

| | | | |
|---|---|---|---|
| Normal | (L) | (m) | |
| $L_8$ | $(L_i)$ | (m) | $L_i$ = ms modulo 8 |
| Repeat | (L) | (mj) | |
| $L_8$, repeat | $(L_i)$ | (mj) | $L_i$ = mjs modulo 8 |

20 CME m n — Compare Memory Equal

Normal 1. BC turned off

2. If (U)* masked by (L) = (m) masked by (L) (see note)

a) BC on

b) Sector timing track stops recording in $(X)_{25-30}$

Repeat 1. BC turned off

2. If (U) masked by (L) = (mj) masked by (L)

a) BC on

b) Sector timing track stops recording in $(X)_{25-30}$

21 CMG m n — Compare Memory Greater

Normal 1. BC turned off

2. If (m) maksed by (L) $\geqslant$ (U) masked by (L) (see note)

a) BC on

b) Sector timing track stops recording in $(X)_{25-30}$

Repeat 1. BC turned off

2. If (mj) masked by (L) $\geqslant$ (U) masked by (L)

a) BC on

b) Sector timing track stops recording in $(X)_{25-30}$

22 TMI m n — Transfer on Minus

If (U) $<$ 0

The next instruction will come from location m.

23 TBC m n — Transfer on Branch Control

If BC on

1. Turn BC off
2. The next instruction will come from location m.

*masked by (L) - The comparison is only made where there are 1's in the lower accumulator. If $L_8$ is used, substitute $L_i$ for (L) in above.

Input-Output

08 INP m n — Input

$m_t$ = 0 - 4 bit input

$m_t$ = 64 - 6 bit input

1. Lower Accumulator 1 word

   Information enters the lower accumulator, shifts thru it into the upper accumulator, and is lost when shifted off the most significant end of the upper accumulator, without any loss of any other information:

   a) 16 characters may be entered in 4 bit mode

   b) 10 characters may be entered in 6 bit mode

2. Lower Accumulator 8 words

   Information enters the least significant portion of $L_0$; shifts thru it into $L_1$, $L_2$ ... $L_7$; and is lost when shifted off the most significant end of $L_7$. Without any loss of information.

   a) 64 characters may be entered in 4 bit mode

   b) 42 characters may be entered in 6 bit mode

   This mode may not be employed with the high-speed paper tape reader.

16 PRD m n — Print from Data Address

$m_t$ to output device (see chart for codes)

17 PRU m n — Print from Upper

$m_t$ = 0 $(U)_{0-3}$ to output device

$m_t$ = 64 $(U)_{0-5}$ to output device

RPC-4000

INPUT-OUTPUT SELECTION CODES FOR PRD

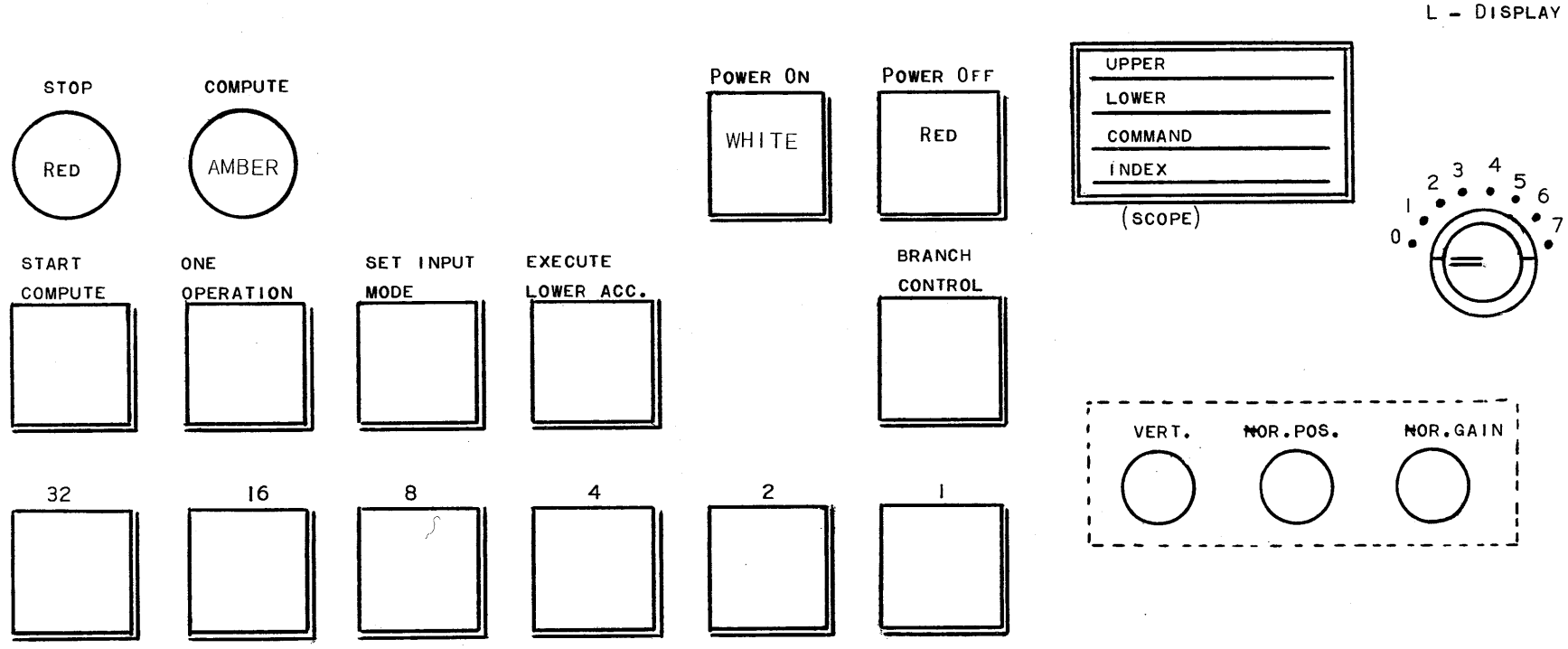
| D Track | Input Selected | Output Selected |
|---|---|---|
| 64 | Reader | |
| 65 | Reader | Punch |
| 66 | Reader | Typewriter |
| 67 | Reader | Punch & Typewriter |
| 68 | Typewriter | |
| 69 | Typewriter | Punch |
| 70 | Typewriter | Typewriter |
| 71 | Typewriter | Punch & Typewriter |
| 72 | Photo-Fwd & Search | |
| 73 | Photo-Rev & Search | |
| 74 | Photo-Fwd | |
| 75 | Photo-Rev | |
| 76-94 | Available for additional units-probably input | |
| 95 | Master Reset-Reset all units | |
| 96 | Available | |
| 97 | | Punch |
| 98 | | Typewriter |
| 99 | | Punch & Typewriter |
| 100 | | |
| 101 | | Punch |
| 102 | | Typewriter |
| 103 | | Punch & Typewriter |
| 104,105 | Search Mode | |
| 106-124 | Available, probably for output units | |
| 125 | Copy Mode On | |
| 126 | Copy Mode Off | |
| 127 | Reset Output Units | |

Notes:

1. Selection of a new input device automatically resets the previous one. Only one input device may be in the system at a time.

2. Output devices may be added in any combination. A reset command is necessary to drop an output device from the system.

3. Because the basic system is standard, multiple selection codes have been included for sections of it.




Control Panel
RPC-4010
(Computer element of RPC 4000)

Fig. IV - 1

# SYSTEM CONTROL

The RPC-4000 is fully automatic and operates under control of an internally stored program. However, the operator is provided means to select any of a wide variety of modes, ascertain internal "states" by means of visual displays, interrupt, intervene, and/or effect an alteration in the system program; this is accomplished through an array of indicators and manually-operated switches conveniently placed in "control-panels".

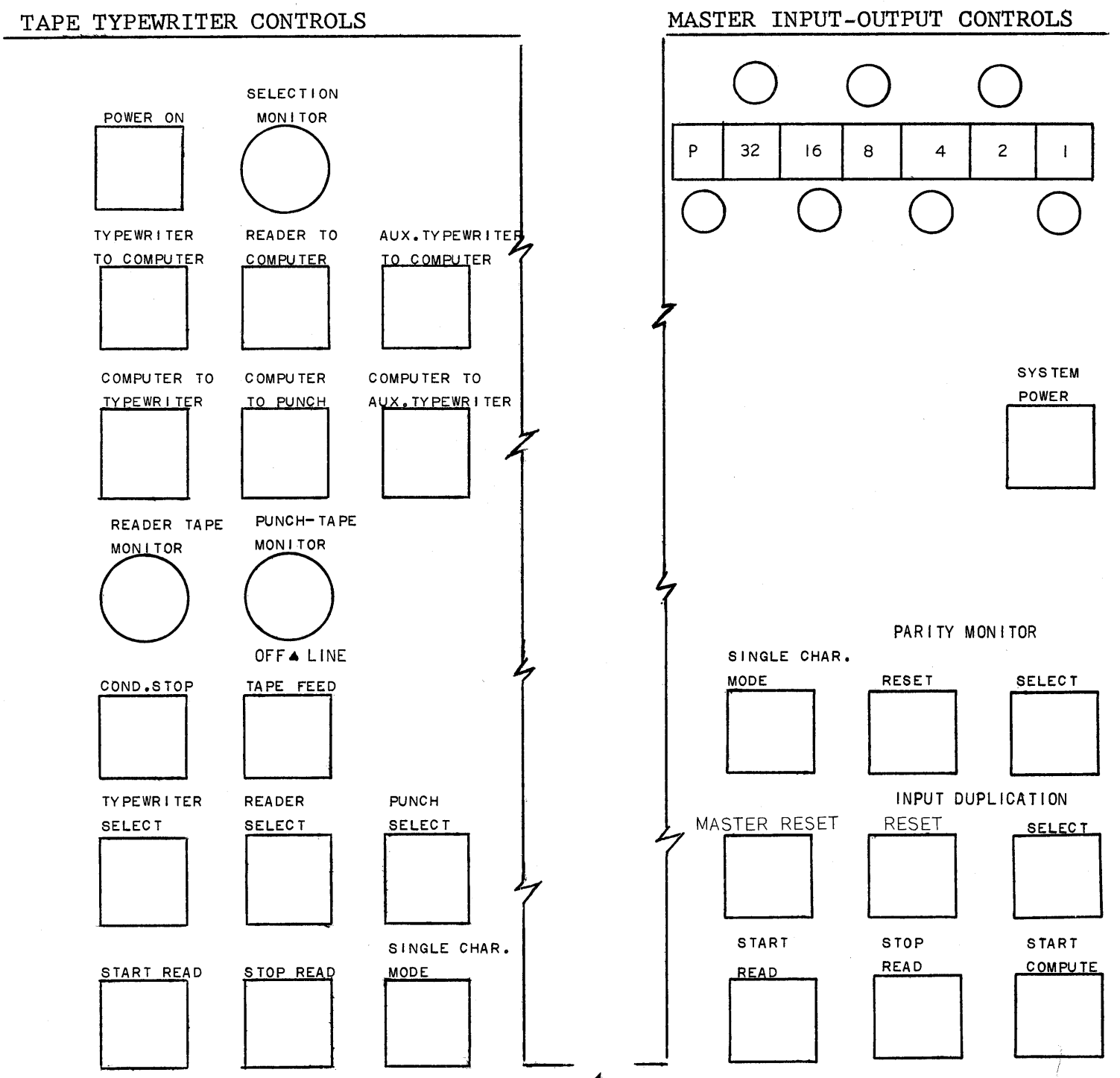
A brief description of the supervisory controls and indicators is presented as an elaboration of the "legends" appearing on the panel escutcheon plates. All components of the panel are clearly and accurately identified by title of function or related action.

## Computer-Control

Operational control of the computer is effected through the control-panel of the 4010 computer. The location, arrangement, and components of this panel provide operator convenience in system-control and supervision.

Indicator and Controls (see diagram):

| Name | Function |
|---|---|
| Power On | This is a momentary switch. It turns "on" the electrical power. |
| Power Off | This momentary switch is used to turn "off" the power. |
| Stop | This light glows to indicate the computer is NOT executing instructions. |
| Computer | This light glows to indicate the computer IS executing instructions. |
| Start | This momentary switch initiates program execution. |




CONTROL PANEL

RPC - 4500

Fig. IV - 2

One Operation

This is a two position selector-switch. When depressed, this will cause the computer to stop after execution of one instruction. When raised it permits the computer to operate at high speed, in the normal instruction-execution mode. The switch is illuminated in the depressed position.

Set-Input Mode

This is a momentary switch. It is used, in conjunction with a depressed "one-operation" switch, to cause the following actions:

1. ZEROIZE $m_t$ of (C)
2. A 4-bit input order given
3. Set L to 1 Word Length

Execute Lower
(2 Positions)

This switch is used in conjunction with the one-operation switch (depressed). It causes the word contained in the Lower Accumulator to be transferred into the Command Register and executed.

Branch Control

This momentary switch may be used to reset (turn OFF) the Branch Control, provided the One Operation switch is in depressed position.

This switch is illuminated when the Branch Control Toggle (BC) is "ON".

Branch Switches
32-16-8-4-2-1

These two-position switches are used in conjunction with the (Programmed) (HALT) instructions. Each switch is lit when depressed.

Oscilloscope

This displays a visual representation of the contents of the registers in the RPC-4010 computer.

L-Display

This rotary (8 position) switch is used to alter the oscilloscope display of the L register. If the lower-accumulator is set to 8-word state, any of the those 8 words may be selected for (scope) display by rotating this switch to the related position.



# MASTER INPUT–OUTPUT CONTROL

The RPC-4000 provides the facility of either: (A) computer-program control of the several input-output devices (RPC-4500, RPC-4410, and RPC-4440), or (B) manual-control of such units.

Program control of the input-output is exercised through a "Master Input-Output Control" unit contained within the basic RPC-4500 Tape Typewriter system. Indicator lights and control switches for this unit are located on the top right-hand side of the Read-Punch cabinet of the RPC-4500 system, adjacent to the tape perforation element, and are as follows (see diagram):

| Name | Function |
|---|---|
| System Power | This two-position switch is used to turn ON or OFF electrical power to all input and output devices connected to the system. Individual power ON-OFF switches of each device are "in-series" with this system power switch so that both must be in the "ON" position to make a unit operable. This switch is illuminated in the depressed (ON) position. |
| Single Character Mode | This is a two-position switch. When depressed it causes the input to halt after each character is read. When in the raised position, it permits normal operation.<br><br>It is illuminated in the depressed position. |
| Parity Monitor RESET | This momentary switch is used to reset a "parity-error-stop" toggle which halts the computer in case a parity-error was detected. Indication of a parity-error is provided by a light (in the reset switch) which glows when the computer stops for this reason. |

| | |
|---|---|
| Parity Monitor SELECT | This two position switch is used to (A) enable parity checking, or (B) inhibit parity-error-detection.<br><br>A. When depressed, parity checking is enabled and the self-contained lamp will be illuminated.<br><br>B. In raised position, parity-checking is inhibited. |
| MASTER RESET | This momentary switch is used to "disconnect" all input-output units from the computer. |
| Input Duplication RESET | This momentary switch is used to turn OFF the "Input Duplication" mode. (See immediately below) |
| Input Duplication SELECT | The momentary switch is used to turn ON the feature of Input-duplication whereby selected output devices "duplicate" (make an exact copy of) the input data as it enters the system.<br><br>Note: This feature of ON-LINE regeneration of input data concurrent with system-entry provides an extremely valuable and unique verification benefit. |
| Start Read | This is a momentary switch by which the selected reader-operation may be initiated. |
| Stop Read | This momentary switch is used to halt operation of the selected reader. |
| Start Compute | This momentary switch is used to initiate program-execution by the computer. |
| Character Indicator Lights | These lights represent the bit-pattern of the character code. They are illuminated to show the NEXT character-code to be read into the system by the reader of the RPC-4500. |

# TAPE TYPEWRITER CONTROLS (RPC-4500/4600)

The Tape Typewriter System, which incorporates a 60cps paper tape reader, a 30cps punch, and one or two typewriters, provides the "basic" input-output to the RPC-4010 computer. It may be used off-line also, as a tape-controlled, tape-producing, manual and/or automatic electric typewriter.

The various controls and indicators of this system are contained in a control-panel on the top left of the reader-punch cabinet (adjacent to the reader element). They are as follows (see diagram).

| Name | Function |
|---|---|
| Power | This 2 position switch is used to turn ON or OFF the electrical power to the RPC-4500. It is illuminated in the depressed (ON) position. |
| Selection Monitor | This light is illuminated to indicate the improper OFF-LINE condition of a "selected" component (of the RPC-4500). Only an ON-LINE device may be selected; the conditional state is monitored by this indicator. |
| Typewriter to Computer | This momentary switch is used to establish the typewriter-to-computer inter-connection. It is illuminated to indicate the typewriter has been "selected" for computer-input. |
| Reader to Computer | This momentary switch is used to establish the reader-to-computer interconnection. It is illuminated to indicate the reader has been selected for computer-input. |
| Auxiliary Typewriter to Computer | Identical to "typewriter to computer" save that it relates to the secondary (auxiliary) typewriter if included in the system. |

| | |
|---|---|
| Computer to Typewriter | This momentary switch is used to establish a computer-to-typewriter interconnection. Illuminated, it indicates the typewriter is "selected" for computer-output. |
| Computer to Punch | This momentary switch establishes computer-to punch interconnection. Illuminated, it indicates the punch is "selected" for computer-output. |
| Reader Tape Monitor | An error-light which indicates:<br><br>Reader out of tape, or<br>Reader tape jammed. |
| Punch Tape Monitor | Same as above, except that it relates to the punch. |
| Conditional Stop | A 2-position switch that conditions the reader to: (A) halt operation upon sensing a "STOP-CODE", or (B) ignore such codes. It is illuminated in the depressed position. |
| Tape Feed | This momentary switch will cause punching of guide (sprocket-feed) holes ONLY in the paper tape for as long as it is held de-pressed. |
| Typewriter Select | A two position switch used to place the type-writer "OFF-LINE" when depressed. |
| Reader Select | A two position switch used to place the reader OFF-LINE when depressed. |
| Punch Select | A two position switch used to place the punch OFF-LINE when depressed. |
| Start Read | A momentray switch used to start operation of the reader when it is in the OFF-LINE state. |
| Stop Read | A momentary switch used to stop reader operation when in the OFF-LINE state. |

Single Character Mode

A two position switch used to:
A - Stop the OFF-LINE areader after one-character is read. Each depression of the start-read switch will cause reading of only 1 character when the Single Character Mode Switch is in depressed position.
B - Permit normal reading in OFF-LINE state.

Note: All units switched to OFF-LINE state are automatically interconnected, for example:

Reader to typewriter if both off-line
Reader to punch if both off-line
Typewriter to punch if both off-line
Reader to typewriter to punch if ALL off-line

| BINARY | CODE PATTERN | ASSIGNED CODE FOR RPC-4000 UC | LC |
|---|---|---|---|
| 0 | 0 0 0 0 0 0 | Tape Feed | |
| 1 | 0 0 0 0 0 1 | CR | |
| 2 | 0 0 0 0 1 0 | Tab | |
| 3 | 0 0 0 0 1 1 | BS | |
| 4 | 0 0 0 1 0 0 | CS | |
| 5 | 0 0 0 1 0 1 | UC | |
| 6 | 0 0 0 1 1 0 | LC | |
| 7 | 0 0 0 1 1 1 | L.F. | |
| 8 | 0 0 1 0 0 0 | Stop Code | |
| 9 | 0 0 1 0 0 1 | | |
| 10 | 0 0 1 0 1 0 | | |
| 11 | 0 0 1 0 1 1 | | |
| 12 | 0 0 1 1 0 0 | | |
| 13 | 0 0 1 1 0 1 | | |
| 14 | 0 0 1 1 1 0 | | |
| 15 | 0 0 1 1 1 1 | | |
| 16 | 0 1 0 0 0 0 | ) | 0 |
| 17 | 0 1 0 0 0 1 | ° | 1 |
| 18 | 0 1 0 0 1 0 | " | 2 |
| 19 | 0 1 0 0 1 1 | # | 3 |
| 20 | 0 1 0 1 0 0 | ≤ | 4 |
| 21 | 0 1 0 1 0 1 | Δ | 5 |
| 22 | 0 1 0 1 1 0 | @ | 6 |
| 23 | 0 1 0 1 1 1 | & | 7 |
| 24 | 0 1 1 0 0 0 | ' | 8 |
| 25 | 0 1 1 0 0 1 | ( | 9 |
| 26 | 0 1 1 0 1 0 | | A |
| 27 | 0 1 1 0 1 1 | | B |
| 28 | 0 1 1 1 0 0 | | C |
| 29 | 0 1 1 1 0 1 | | D |
| 30 | 0 1 1 1 1 0 | | E |
| 31 | 0 1 1 1 1 1 | | F |

| BINARY | CODE PATTERN | ASSIGNED CODE FOR RPC-4000 UC | LC |
|---|---|---|---|
| 32 | 1 0 0 0 0 0 | | G |
| 33 | 1 0 0 0 0 1 | | H |
| 34 | 1 0 0 0 1 0 | | I |
| 35 | 1 0 0 0 1 1 | | J |
| 36 | 1 0 0 1 0 0 | | K |
| 37 | 1 0 0 1 0 1 | | L |
| 38 | 1 0 0 1 1 0 | | M |
| 39 | 1 0 0 1 1 1 | | N |
| 40 | 1 0 1 0 0 0 | | O |
| 41 | 1 0 1 0 0 1 | | P |
| 42 | 1 0 1 0 1 0 | | Q |
| 43 | 1 0 1 0 1 1 | | R |
| 44 | 1 0 1 1 0 0 | | S |
| 45 | 1 0 1 1 0 1 | | T |
| 46 | 1 0 1 1 1 0 | | U |
| 47 | 1 0 1 1 1 1 | | V |
| 48 | 1 1 0 0 0 0 | | W |
| 49 | 1 1 0 0 0 1 | | X |
| 50 | 1 1 0 0 1 0 | | Y |
| 51 | 1 1 0 0 1 1 | | Z |
| 52 | 1 1 0 1 0 0 | $ | . |
| 53 | 1 1 0 1 0 1 | : | = |
| 54 | 1 1 0 1 1 0 | ; | ⊆ |
| 55 | 1 1 0 1 1 1 | % | ⊇ |
| 56 | 1 1 1 0 0 0 | | |
| 57 | 1 1 1 0 0 1 | | |
| 58 | 1 1 1 0 1 0 | ? | + |
| 59 | 1 1 1 0 1 1 | — | - |
| 60 | 1 1 1 1 0 0 | . | . |
| 61 | 1 1 1 1 0 1 | Space | |
| 62 | 1 1 1 1 1 0 | ÷ | / |
| 63 | 1 1 1 1 1 1 | Delete | |

Input-Output

The basic character codes for all input-out devices are as follows:

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0. | Tape feed | 16. | 0 ) | 32. | g G | 48. | w W |
| 1. | CR | 17. | 1 ° | 33. | h H | 49. | x X |
| 2. | tab | 18. | 2 " | 34. | i I | 50. | y Y |
| 3. | BS | 19. | 3 # | 35. | j J | 51. | z Z |
| 4. | CS | 20. | 4 ≤ | 36. | k K | 52. | , $ |
| 5. | UC | 21. | 5 △ | 37. | l L | 53. | = : |
| 6. | LC | 22. | 6 @ | 38. | m M | 54. | ⌐ ; |
| 7. | L.F. | 23. | 7 & | 39. | n N | 55. | ⌋ % |
| 8. | *Stop Code | 24. | 8 ' | 40. | o O | 56. | |
| 9. | | 25. | 9 ( | 41. | p P | 57. | |
| 10. | | 26. | a A | 42. | q Q | 58. | + ? |
| 11. | | 27. | b B | 43. | r R | 59. | - _ |
| 12. | | 28. | c C | 44. | s S | 60. | . . |
| 13. | | 29. | d D | 45. | t T | 61. | space |
| 14. | | 30. | e E | 46. | u U | 62. | / ÷ |
| 15. | | 31. | f F | 47. | v V | 63. | Delete |

The parity level is not considered in this table. It should be in the left-most channel and the other channels are represented in sequence.

Note: Tape codes "00 thru 15" and "63" do not enter the computer in normal mode.



# OPTIMIZING

Optimum programming is the technique by which data and instructions are placed on the drum of the computer so as to minimize non-productive searching time. There is available an Optimizing Assembly Program (ROAR) which enables the coder to write instructions in symbolic form; the computer will convert the symbolic program into machine-instructions and assign "optimum" locations for data and instructions.

## Word-Time Unit

A typical cross section of the drum is illustrated below. Since a word-time is the time it takes one word or sector to pass under the read head, and the drum revolves at 3600 revolutions per minute, one-word-time is 0.26 milliseconds. A word-time is the fundamental unit of time. The track portion of all locations and addresses has no effect on optimizing.

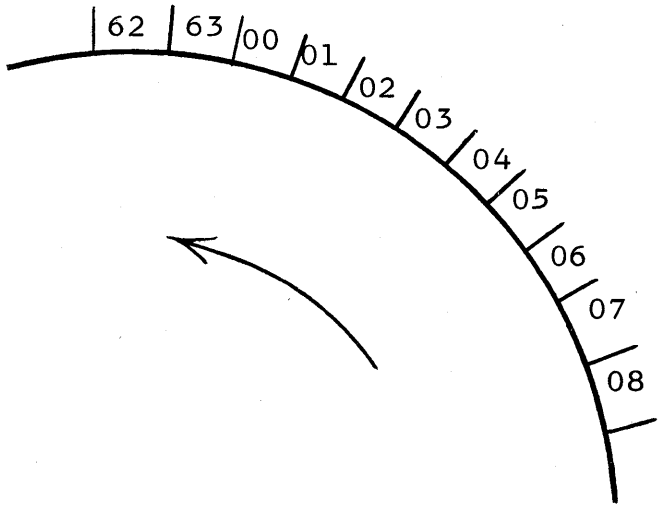



Fig. V - 1

Instruction Phases

A typical instruction operates in the following manner:

A. The word indicated by the "next address" portion (bits 18-30) of the command register is transferred to the command register.

The RPC-4000 creates the two following phases for the sequence.

Phase 1. Search for the next instruction address, bits 18-30 of the command register.

Phase 2. Transfer this word to the command register.

B. The word in the command register is then executed.

The RPC-4000 creates the two following phases for this sequence:

Phase 3. Search for operand address, bits 5-17 of the command register.

Phase 4. Execute the instruction in the command register.

N.B.(The count for the repeat mode of operation and nature of the instruction determines how many word times the computer stays in phase 4).

In a typical instruction, phase 1 and phase 3 may vary between 1 and 64 word times. The minimum time for a typical instruction is 1 word-time for each phase, i.e., 4 word times. An illustration of a completely optimized instruction follows:

| Loc | Operation | Operand Address | Next Instr.Addr. | Index |
|---|---|---|---|---|
| XX00 | RAU | yy02 | zz04 | o |

Fig. V - 2

The following instructions have a 1 word-time for phase 4, and go through phases 1,2,3 in the normal manner. To obtain maximum optimization of these instructions, the Operand Address should be 2 sectors beyond the location of the instruction and the Next Instruction Address should be 2 sectors beyond the Operand Address.

| | | | | |
|---|---|---|---|---|
| RAU | EXT | CLU | SBU | LDC |
| RAL | COL | CLL | SBL | LDX* |
| MST | STU | ADU | CXE* | EXC |
| MPT | STL | ADL | SAU | CME |
| CMG | PRD* | PRU* | HLT* | |

* A search for the sector address is not made in phase 3, however, the computer does spend one word time in phase 3. The PRU and PRD instructions will remain in phase 3 if the selected output device is not ready to receive the output data.*

The timing on the TMI and TBC instructions .....

XXXX (TMI) (TBC) YYYY ZZZZ

..... is explained in the following:

Phase 1 and 2 are exactly the same as with all instructions. If the transfer does not take place (the next instruction is taken from zzzz) phases 3 (1-word time) and 4 (1-word time) are executed in the normal manner. If the transfer does occur (the next instruction is taken from yyyy), there is a normal phase-3 search and the computer is then switched to phase 2 of the next instruction, which fills the command register with (yyyy).

To obtain maximum optimization of these instructions, the Operand Address should be 2 sectors beyond the location of the

* "Unless coded with the most optimum sector address in which event the wait for the ready signal is overridden."



instruction and the Next Instruction Address should be 4 sectors beyond the Operand.

> Note: Phase 4 is not executed if the machine transfers to location yyyy. This is the only case where the repeat mode of operation does not apply to the instruction that immediately follows the LDC instruction.

The following instructions have another phase called phase 4a. In this phase, internal shifting and logical operations are being performed by the computer. In some instructions a specified number of word times will be spent in phase 4a, in other instructions this is variable.

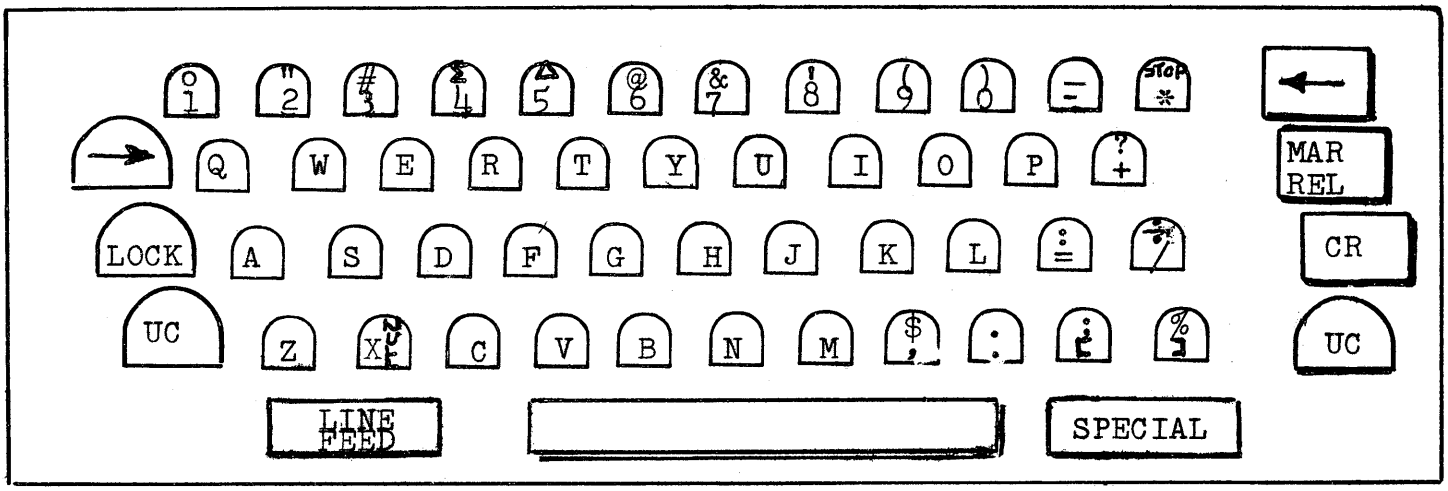
| | | |
|---|---|---|
| SRT, SLT | Phase 1,2,3,4,4a | variable |
| SLC | Phase 1,2,3,4,4a | variable |
| DVU | Phase 1,2,3,(4,) | (64 in 4a) |
| DIV | " " " | " |
| MPY | " " " | " |

To obtain optimization of the shift instructions, the Next Instruction Address should be (7 + number of shifts) sectors beyond the location.

To obtain maximum optimization of the DVU, DIV, and MPY instructions, the Operand Address should be 2 sectors beyond the Location of the instruction and the Next Instruction Address should be (1) sector beyond the Operand Address.

The INP instruction is locked in phase 1 until a start signal is supplied by an input-output device or from the start switch. Optimization of an INP instruction is therefore independent of internal computer operations.

KEYBOARD 180 XE




The Keyboard shown above is that which is used for the typewriter units of the RPC-4000 Computer System.

Note: Typewriter units are designated as "Model 4480" and used in the 4500 and 4600 Tape Typewriter Systems as either "PRIME" or "Auxiliary" character printers.

# INPUT OUTPUT UNITS

As previously mentioned, the basic input-output unit of the RPC-4000 system is a Model 4500 Tape Typewriter system. This system is composed of two units, (1) a Read-Punch combination unit, and (2) an automatic Royal Electric Typewriter.

Additionally, an RPC-4000 may be augmented with optional input and output devices as warranted by the need or preference of any application. Presently available are:

Model 4410 Photo Electric Tape Reader

Model 4431 Auxiliary Read-Punch Unit

Model 4440 High Speed Punch

Model 4480 Auxiliary Tape-Typewriter

Model 4600 Auxiliary Tape-Typewriter System

These units may be added to the RPC-4000 as desired up to a total of 22 input - 23 outputs on line concurrently ... minor modifications extend the total to 60 on-line units. The computer (Model 4010) exercises control, as programmed, over "selection" in input and output devices. Further, the computer may select 4 or 6 bit input as well as choose whether typed copy and/or "duplicate" tapes will be made from input data.

All input data is parity checked for code pattern validation. Output data codes contain proper parity bits in the 7th level for subsequent accuracy control.

# RPC-4500

The Model 4500 Tape Typewriter system is a new and unusual paper-tape and hard-copy producing typewriter amenable to manual and/or paper-tape data insertion. It is composed of a CHAD-tape reader and punch combination unit and a separately packaged electric typewriter. These two units are interconnected to form a multiple-function system capable of a wide variety of operations.

The Read-Punch unit is conveniently placed in its specially designed cabinet which is provided with tape-handling and chad-collection facilities. The typewriter is installed on a special console which provides "work-space" on either side of the keyboard.

The Reader operates at 60, 30, or 10 characters per second. The Punch is capable of 30 or 10 characters per second output, and the typewriter at "operator speed" of 10 per second. The effective speed of any combination is "interlocked" to maintain compatibility.

The complete system includes an operator's chair of matching design. The several components may be arranged in a variety of forms to meet any preference or need.

MODES

The Model 4500 provides the following basic modes of operation:

Reader to Computer
Reader to Punch
Reader to Typewriter
Computer to Punch
Computer to Typewriter
Typewriter to Punch
Typewriter to Computer
Reader to Computer to Punch
Reader to Typewriter to Punch
Reader to Typewriter to Computer to Punch
Computer to Typewriter to Punch
Reader to Computer to Typewriter

In addition, the above modes may be operated in either "normal" or "one-operation" manner.

Controls of this system are explained in the Computer-Control section. Keyboard operation is identical to conventional typing practice. Margin control is achieved easily and conveniently at the keyboard as is tab-stop setting and release.

The keyboard contains "45-keys" in conventional array, plus certain special function or conditional keys. Operator correction of errored entries is simple and easy to effect at the keyboard... punched-tape may be "backspaced" automatically.

RPC-4410

The Model 4410 Photo-Electric-Reader is a high-speed "input" device for the RPC-4000 computer. Capable of reading CHAD punched paper tape at 500 characters per second, this unit is separately packaged in a matching cabinet which provides tape-handling facilities. Tape may be sensed in forward or reverse direction with equal ease. Also, tape may be "searched", for a special code, in either direction while the computer accepts input, emits output, or computes.

The RPC-4000 computer ability to handle 45 on-line input-output devices (60 with minor modifications) plus the Model 4410 speed and bi-directional reading and searching offers an unusual facility for applications wherein paper-tape may be used for un-limited computer "memory" to augment the main-memory of the computer.

# RPC-4431

The Reader-Punch combination unit may be used as a separate optional input-output unit as well as a component of the Model 4500 Tape Typewriter system. This electro-mechanical CHAD tape reader and perforator provides additional computer input of 60 characters per second and output of 30 characters per second.

This individually packaged unit includes tape handling and CHAD collection facilities. Either reeled or strip tapes may be handled with equal ease. Safety interlocks are provided to assure proper operation of either or both elements.

# RPC-4440

The Model 4440 High Speed Punch is capable of perforating paper tape at the rate of 300 characters per second. It is designed for ON-LINE operation with (and under control of) the 4010 computer.

The Model 4440 is an optional output device which may be added to any RPC-4000 system. In extremely high-volume output applications, one or more of these CHAD tape punches will easily achieve the results desired.

# RPC-4600

This is a Tape-Typewriter System similar to the RPC-4500 except that it does not have the Master Input-Output Controls. It is composed of an RPC-4431 and RPC-4480.