Scientific Control Systems

INTRODUCTION

The SCS 650-2 is a low cost, general purpose, digital computer designed for use in a variety of applications. Despite its low cost, the SCS 650-2 offers many features found only in more expensive computers. The SCS 650-2 offers a high-speed, random-access memory with a 2 microsecond cycle time. A powerful and flexible instruction repertoire makes the SCS 650-2 ideal for applications such as process control, on-line data collection and reduction, and scientific computation. The modular design of the system permits the use of a wide variety of peripheral equipment and/or special control devices. Special emphasis has been placed on developing a system which can be adapted in the field to meet the customer's changing requirements. Up to 32 external devices may be connected to each SCS 650-2.

A comprehensive software package is provided with each hardware system. It is designed to take full advantage of the hardware capabilities of the SCS 650-2 while providing the user with a convenient means of communication with the hardware system.

FEATURES

Large Memory Capacity
The basic memory module of the SCS 650-2 contains 4,096 twelve-bit words. The memory capability is expandable to 32,768 words in 4,096 word increments. In keeping with the corporate modular design philosophy, memory expansion may be made in the field.

All Silicon Semiconductors
All circuits utilize reliable, silicon semiconductors mounted on printed circuit plug-in cards. The system is highly maintainable at any modular level.

Fully Parallel Operation
All arithmetic and logical operations, together with high speed data transfers between memory and the various registers, are completed in parallel.

Hardware Index Register
In addition to providing address modification for memory reference instructions, the index register is a valuable aid in logical operation. A special set of instructions provide logical and arithmetic operations which use the index register and the accumulator as operands.

Priority Interrupt Channels
The interrupt channel, included as standard equipment, may be activated by internal computer conditions needing service. These include such functions as accumulator overflow, I/0 error, etc.

A priority facility is incorporated to permit external devices to command the computer to transfer to a specific subroutine. Using this facility priority channels can be added which are fully nested. That is, a higher priority channel may interrupt lower priority interrupt routines and the lower priority routine will be resumed after completion of the higher priority function.

Memory Protect Feature
Hardware memory protection is provided for lower numbered memory positions. The protect feature allows the reading of instructions or data from the protected area but inhibits any writing into the protected area of memory. Attempting to write into the protected area causes a program interrupt, allowing the programmer to take corrective action as required. The memory protect feature may be enabled or disabled under program control or from a switch on the control console.

Direct Memory Access Feature
The direct memory access feature permits high speed data transfer between memory and external devices. This access channel operates on a cycle stealing basis. As a result, the external device is not required to wait until the present instruction is complete before control of the memory is transferred to the external device. Complete isolation between memory banks allows the computer to continue undisturbed if the external device requests a memory bank other than the one being used by the processor. Also, memory overlap can occur when two or more external devices request different memory modules simultaneously. Therefore, each of eight different devices can transfer data simultaneously at a rate of 500,000 twelve-bit words per second for a total rate of 4,000,000 words/second.

Micro-Programmable Instructions
All instructions which do not reference memory may be micro-programmed. This group of instructions allows the computer to execute up to four non-memory instructions in a single computer cycle. It also provides the programmer with a variety of bit-manipulation, shift, skip, test, and I/0 instructions.

Flexible Subroutine Linkages
A single instruction executes a transfer to a subroutine in any core bank and provides the mechanism for a single instruction return to the calling program.

Four Addressing Modes
The addressing techniques employed in the SCS 650-2 computer permit four modes of addressing — indirect, direct, relative or indexed.

Functional Control Console

The control console is designed as a functional man-machine interface. The addressable registers are continuously displayed on the control console. These register displays are arranged for quick operator recognition of their contents. Special switches are provided for a fast, convenient means of entering information into memory or examining the contents of memory.

The computer may be operated either in run or single-step modes.

Literal Instructions

Several literal instructions are incorporated which use the last six bits of the instruction as the operand. This feature allows high speed, one character arithmetic or logical operations.

BASIC INSTRUCTION FORMAT

The basic instruction format is as follows:

0	1	2	3	4	5	6	7	8	9	10	11

Instruction Address

Mode Bit

Indirect Address Bit

Basic Operation Code
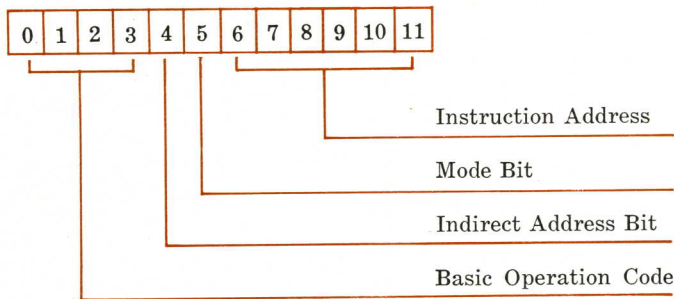
In addition to the mode specification bit in the basic instruction, an index state may be initiated through the status register. When the index state is in effect, the index register is used in lieu of the P counter for address modification.

ADDRESSING MODES

Primary Address

Each of the four possible addressing modes is based on the concept of a "primary address." The primary address of an instruction is defined to be any address which can be formed using the instruction address and the available address modification registers.

Direct Mode . . . Mode Bit = 0   Index State = 0
Primary address is determined by the instruction address. In the direct mode, the primary address always refers to the first 64 locations of memory bank zero.

Index Mode . . . Mode Bit = 1   Index State = 1
Primary address is the sum of the instruction address and the contents of the index register. It will always be in the same memory bank as the instruction.

Relative Mode . . . Mode Bit = 1 Index State = 0
Primary address is the sum of the instruction address and the address from which the instruction was taken. It will always be in the same memory bank as the instruction.

Indirect Mode

The indirect address bit is always applied after the contents of the primary address has been obtained. If the indirect address bit is zero, the contents of the primary address is used as the operand of the instruction. If the indirect address bit is a one, the contents of the primary address is interpreted not as an operand but as the 12 low-order bits of an operand address. The 3 high-order bits of the operand address are specified by the indirect bank register.
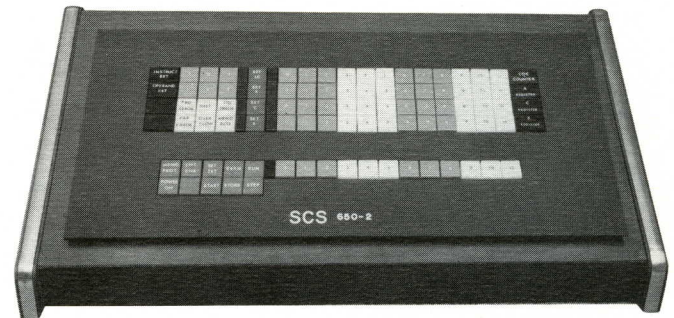
SCS 650-2

INSTRUCTIONS

The instruction repertoire of the SCS 650-2 is described below. The conventions used in instruction description are as follows:

(1) A register name enclosed in parentheses denotes the contents of the register.

(2) Subscription is used to denote bit positions within a register.

(3) The right arrow symbol, "→", is read "is transferred into."

(4) The letter "M" denotes the effective address, i.e., M denotes the memory address used in the execution of the instruction.

Arithmetic Instructions

Instruction	Mnemonic	Cycles	Op Codes
Add to Accumulator	ADD	2	1001
$(A) + (M) \rightarrow A$			
$(M) \rightarrow M$			
Subtract from Accumulator	SUB	2	1101
$(A) - (M) \rightarrow A$			
$(M) \rightarrow M$			
Exclusive OR with Accumulator	XOR	2	1011
$(A) \oplus (M) \rightarrow M$			
$(M) \rightarrow M$			

2

| AND with Accumulator | AND | 2 | 1111 |

$(A) \cdot (M) \to A$
$(M) \to M$

| Memory Increment and Skip on Zero | MIN | 2 | 1000 |

$(M) + 1 \to M$
$(A) \to A$
If $(M) = 0$, $(P) + 2 \to P$
If $(M) \neq 0$, $(P) + 1 \to P$

Load and Store Instructions

Instruction	Mnemonic	Cycles	Op Codes
Load Accumulator	LDA	2	1100

$(M) \to A$
$(M) \to M$

| Store Accumulator | STA | 2 | 0111 |

$(A) \to M$
$(A) \to A$

| Load Index | LDX | 2 | 0010 |

$(M) \to X$
$(M) \to M$

| Store Index | STX | 2 | 0011 |

$(X) \to M$
$0 \to X$

Jump Instructions

Instruction	Mnemonic	Cycles	Op Codes
Jump Forward	JMF	2	0100

$M \to P$
$(A) \to A$

Note: If Bit 4 = 0, $M = (P) + (INS)_{6-11}$

| Jump Backward | JMB | 2 | 0101 |

$MA \to P$
$(A) \to A$

Note: If Bit 4 = 0, $M = (P) - (INS)_{6-11}$

| Jump and Store Location | JSL | 2 | 1010 |

$Status \to (M)$
$(P) + 1 \to M + 1$
$M + 2 \to P$
$(A) \to A$

| Return Jump | JRT | 2 | 1110 |

$(M) \to Status$
$(M + 1) \to P$
$(A) \to A$

Literal Instruction Format

0	1	2	3	4	5	6	7	8	9	10	11

Operand

Literal Instruction

Operation Code = 0110
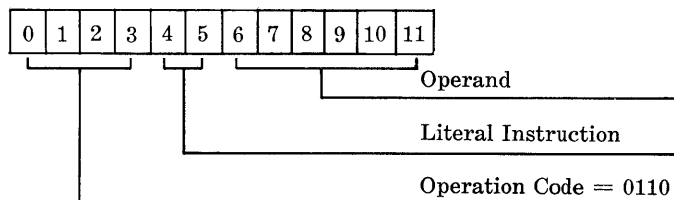
R_4	R_5	Instruction	Mnemonic
0	0	AND Literal	ANL
0	1	EXCLUSIVE OR Literal	XOL
1	0	LOAD A Literal	LAL
1	1	ADD Literal	ADL

Instruction	Mnemonic	Cycles	R_4	R_5
AND Literal	ANL	1	0	0

$(INS)_{6-11} \cdot (A) \to A$

| Exclusive OR, Literal | XOL | 1 | 0 | 1 |

$(INS)_{6-11} \oplus (A) \to A$

| Load A, Literal | LAL | 1 | 1 | 0 |

$(INS)_{6-11} \to A$

| Add, Literal | ADL | 1 | 1 | 1 |

$(INS)_{6-11} + (A) \to A$

Operate Instruction Format (Microinstructions)

0	1	2	3	4	5	6	7	8	9	10	11

Bit 11 = 1 Specifies this as a microinstruction

Bit 10 = 1 Clear selected register

Bit 9 — Register selection bit
0 = A Register
1 = X Register

Bits 6-8 — Specifies a function to be performed on the selected register

Bits 4 & 5 — Specifies a test to be performed on the results of the above function

Basic Operation Code
0000 = Operate
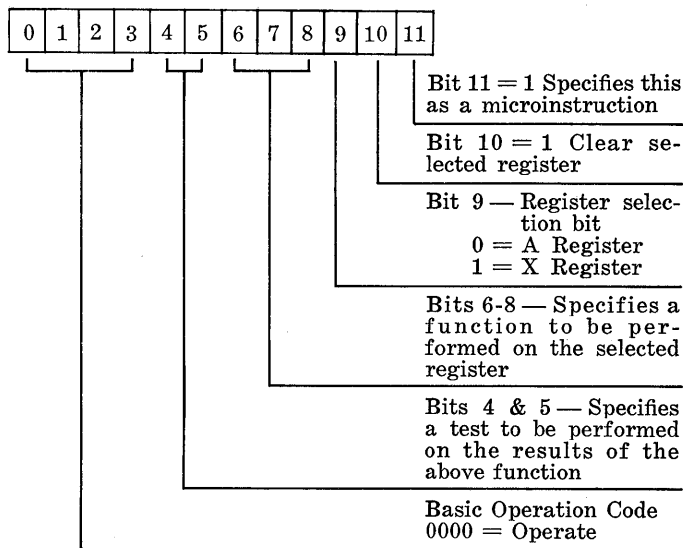
First Microinstruction

Select the register defined by Bit 9

0 = A Register

1 = X Register

Second Microinstruction

Clear selected register if specified by Bit 10.
If bit 10 = 0, do not clear selected register.

Third Microinstruction

Perform one of eight functions as specified by Bits 6-8.

000	Test Selected Register only.
001	Increment Selected Register (Sel Reg) + 1 → Sel Reg
010	Logical AND Selected Register with Unselected Register (Sel Reg) · (Unsel Reg) → Sel Reg

011	Exclusive OR Selected Register with Unselected Register (Sel Reg) $\oplus$ (Unsel Reg) $\rightarrow$ Sel Reg
100	One's complement of Selected Register $(\overline{\text{Sel Reg}}) \rightarrow$ Sel Reg
101	Two's complement of Selected Register $(\overline{\text{Sel Reg}}) + 1 \rightarrow$ Sel Reg
110	Complement Selected Register and Exclusive OR with Unselected Register $(\overline{\text{Sel Reg}}) \oplus$ (Unsel Reg) $\rightarrow$ Sel Reg
111	Subtract Selected Register from Unselected Register (Unsel Reg) – (Sel Reg) $\rightarrow$ Sel Reg

Fourth Microinstruction
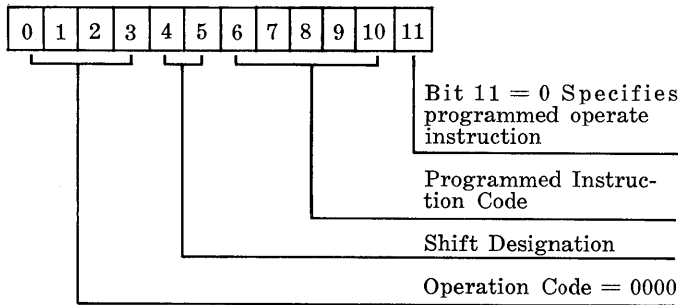
Test the results of the above functions and skip as follows:

R_4	R_5	
0	0	No Skip
0	1	Skip if positive
1	0	Skip if negative
1	1	Skip if Zero

Commonly Used Microinstructions — One Cycle

Instruction Code	Description
0003	Clear A Register
0007	Clear X Register
0101	Test A Register and skip if positive
0201	Test A Register and skip if negative
0301	Test A Register and skip if zero
0105	Test X Register and skip if positive
0205	Test X Register and skip if negative
0305	Test X Register and skip if zero
0011	Increment A and no skip
0111	Increment A and skip if positive
0211	Increment A and skip if negative
0311	Increment A and skip if zero
0015	Increment X and no skip
0115	Increment X and skip if positive
0215	Increment X and skip if negative
0315	Increment X and skip if zero
0021	AND A with X, results into A Register, No Skip
0121	AND A with X, results into A Register — Skip if positive
0221	AND A with X, results into A Register — Skip if negative
0321	AND A with X, results into A Register — Skip if zero
0025	AND A with X, results into X Register — No skip
0125	AND A with X, results into X Register — Skip if positive
0225	AND A with X, results into X Register — Skip if negative
0325	AND A with X, results into X Register — Skip if zero
0031	Exclusive OR A with X, Results into A Register — no skip
0131	Exclusive OR A with X, Results into A Register — Skip if positive
0231	Exclusive OR A with X, Results into A Register — Skip if negative
0331	Exclusive OR A with X, Results into A Register — Skip if zero
0035	Exclusive OR A with X, Results into X Register — No Skip
0135	Exclusive OR A with X, Results into X Register — Skip if positive
0235	Exclusive OR A with X, Results into X Register — Skip if negative
0335	Exclusive OR A with X, Results into X Register — Skip if zero
0041	One's complement of A — No skip
0141	One's complement of A — Skip if positive
0241	One's complement of A — Skip if negative
0341	One's complement of A — Skip if zero
0045	One's complement of X — No skip
0145	One's complement of X — Skip if positive
0245	One's complement of X — Skip if negative
0345	One's complement of X — Skip if zero
0051	Two's complement of A — No skip
0151	Two's complement of A — Skip if positive
0251	Two's complement of A — Skip if negative
0351	Two's complement of A — Skip if zero
0055	Two's complement of X — No skip
0155	Two's complement of X — Skip if positive
0255	Two's complement of X — Skip if negative
0355	Two's complement of X — Skip if zero
0061	Complement A and Exclusive OR with X, Place result in A register — No Skip ·
0161	Complement A and Exclusive OR with X, Place result in A register — Skip if positive
0261	Complement A and Exclusive OR with X, Place result in A register — Skip if negative
0361	Complement A and Exclusive OR with X, Place result in A register — Skip if zero
0065	Complement X and Exclusive OR with A, Place result in X register — No skip
0165	Complement X and Exclusive OR with A, Place result in X register — Skip if positive
0265	Complement X and Exclusive OR with A, Place result in X register — Skip if negative
0365	Complement X and Exclusive OR with A, Place result in X register — Skip if zero
0071	Subtract A from X, Place result in A register — No skip
0171	Subtract A from X, Place result in A register — Skip if positive
0271	Subtract A from X, Place result in A register — Skip if negative
0371	Subtract A from X, Place result in A register — Skip if zero
0075	Subtract X from A, Place result in X Register — No skip
0175	Subtract X from A, Place result in X Register — Skip if positive
0275	Subtract X from A, Place result in X Register — Skip if negative
0375	Subtract X from A, Place result in X Register — Skip if zero

4

Operate Instruction Format (Programmed)

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| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
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Bit 11 = 0 Specifies programmed operate instruction

Programmed Instruction Code

Shift Designation

Operation Code = 0000

Instruction	Mnemonic	Programmed Instruction Code	Cycles
Halt	HLT	00	1
No Operation	NOP	01	1
Rotate Right	RTR	04	1
Rotate Left	RTL	05	1
Shift Right	SHR	06	1
Shift Left	SHL	07	1

In shift instructions, bits R_4 and R_5 are interpreted as follows:

R_4		R_5	
0	Shift one place	0	Arithmetic Shift
1	Shift two places	1	Logic Shift

Instruction	Mnemonic	Programmed Instruction Code	Cycles
Exchange Halves of A	XHA	10	1
$(A)_{0-5} \to A_{6-11}$			
$(A)_{6-11} \to A_{0-5}$			
Exchange A & X	XAX	20	1
$(A) \to X$			
$(X) \to A$			
Copy A to X	CAX	20	1
$(A) \to X$		$R_4 = 1$	
$(A) \to A$			
Copy X to A	CXA	20	1
$(X) \to A$		$R_5 = 1$	
$(X) \to X$			
Load A from Switches	LAS	24	1
$(SW) \to A$			
Add with Carry	ADC	26	1
$(A) + (CO) \to A$			
Carry $\to$ CO			

Instruction	Mnemonic	Programmed Instruction Code	Cycles
Load A from Status	LST	30	1
(Status) $\to$ A			
(Status) $\to$ Status			
Load Status from A	LSA	34	1
(A) $\to$ Status			
(A) $\to$ A			

Input-Output Instruction Format

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| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
```

Device Selection

I/0 Command

Operation Code = 0001
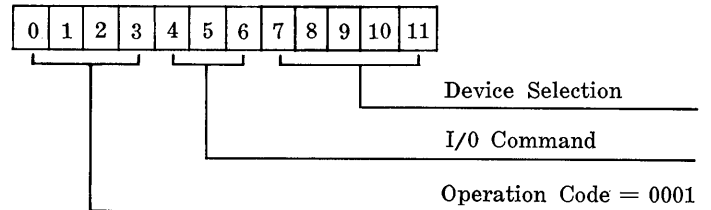
I/0	Commands	Mnemonic	Cycles
000	Transmit to A & Skip	TTA	1
	(Selected device) $\to$ A } If device		
	(P) + 2 $\to$ P } is ready		
001	Transmit from A & Skip	TFA	1
	(A) $\to$ Selected device } If device		
	(P) + 2 $\to$ P } is ready		
010	Input Device Status	DST	1
	(Device status) $\to$ A } If device		
	(P) + 2 $\to$ P } is ready		
011	Skip on device flag	SDF	1
	FLAG = 1		
	(P) + 2 $\to$ P		
	FLAG = 0		
	(P) + 1 $\to$ P		
100	Execute Command in A	EXU	1
	External device executes command in A		
101	Terminate	TMR	1
	Inactivate device		
110	Select without leader	SWL	1
	Activate device no leader		
111	Select with leader	SOL	1
	Activate device with leader		

5

INTERNAL MACHINE ORGANIZATION

Figure 1 shows a block diagram of the internal operation of the SCS 650-2 computer. In this illustration, all arrows indicate data paths and all transfers over these data paths are parallel transfers.

As can be seen from this illustration, the computer contains seven twelve-bit registers, three three-bit registers, three one-bit registers, a parallel adder, and miscellaneous gates and control registers. The operation of these registers is as follows:

C Register — The C Register accepts data from the memory and is used as a holding register into the parallel adder. In the halt mode, this register contains the instruction which will be executed next. Execution of the instruction contained in the C Register causes the transfer of the instruction into the R Register which is used to hold the instruction throughout its execution time.

R Register — The R Register holds instructions for decoding into various instruction signals.

Z Register — The Z Register is the second holding register into the parallel adder. The parallel adder uses as its input the output of both the C Register and the Z Register.

X Register — The X Register is a twelve-bit register which can be used for indexing and addressing modification. Microinstructions use the X and the A registers for internal manipulation.

The X Register also serves as the extended accumulator for multiply and divide operations.

A Register — The A Register is the computer's main accumulator. All arithmetic and logical operations performed within the computer use this register to hold the results of the operation.
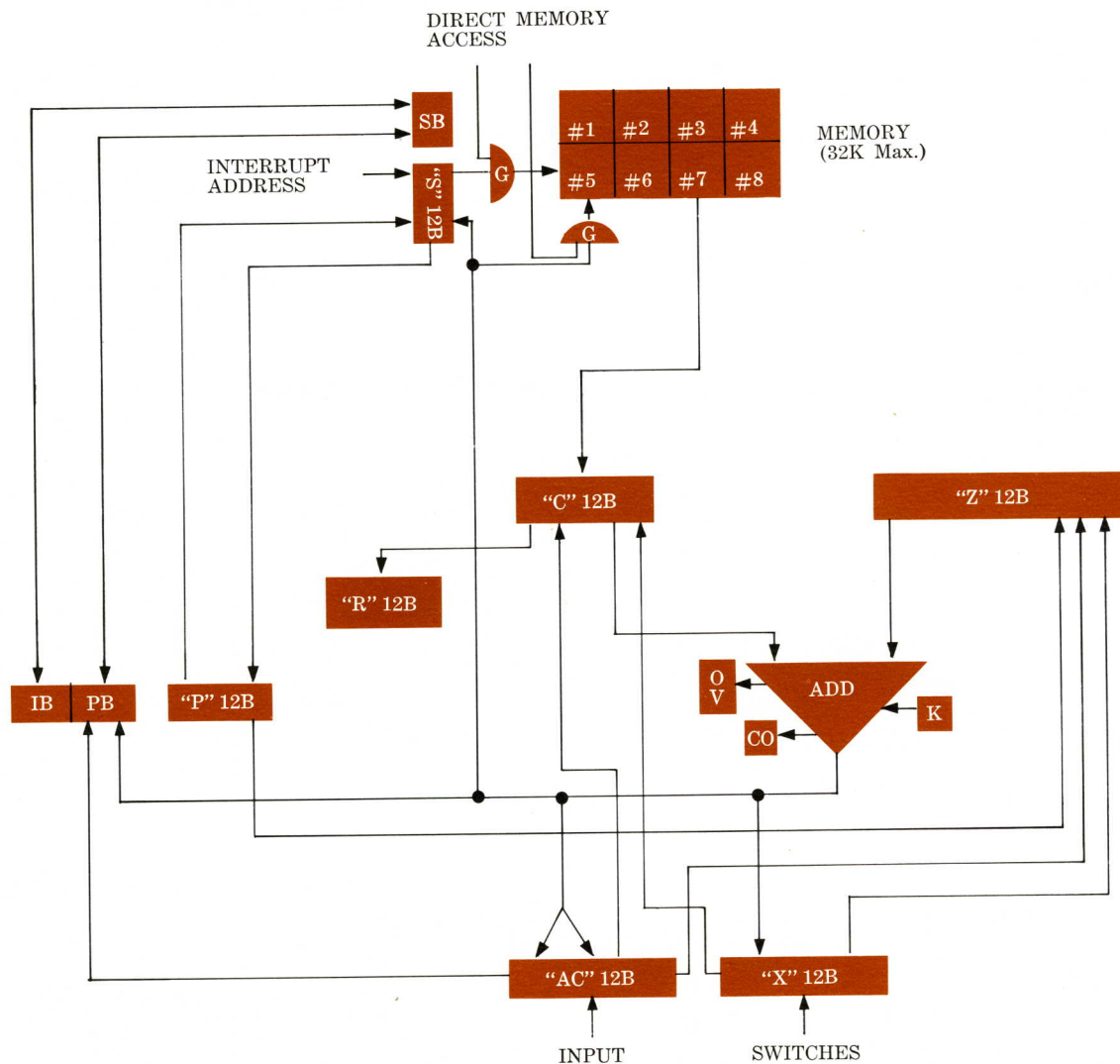
DATA PATHS

Figure 1

P Register — The P Register is a twelve-bit register which is used as the location counter for the computer. When in the relative mode, the six-bit instruction address is added to the contents of the P counter to determine the effective address of the instruction to be executed.

S Register — The S Register is the memory address register consisting of twelve bits.

PB Register — The PB Register is the instruction extension register used to determine the memory bank from which instructions and all relative operands will be taken.

IB Register — The IB Register is the indirect extension register used to specify a particular memory bank for indirectly addressed operands.

SB Register — The SB Register is a three-bit register which is decoded and used to specify which memory banks will be used for a particular memory operation.

Adder — The twelve-bit parallel adder is capable of arithmetic operations (add and subtract) as well as logical operations such as AND, OR, and EXCLUSIVE OR.

K Register — The K Register is a one-bit register used to initiate a carry into the adder. This register is used for two's complement operation and for incrementing registers.

CO Register — The CO Register is a one-bit register which is set when the output of the adder has a carry-out.

Overflow Register — The Overflow Register is a one-bit register which is set to "one" when the adder has an overflow.

Status Register — The Status Register is a twelve-bit composite register consisting of:

(1) The PB register (3 bits)
(2) The IB register (3 bits)
(3) The CO register (1 bit)
(4) The Overflow register (1 bit)
(5) The Memory Protect register (1 bit)
(6) The Index State (1 bit)
(7) The Parity Select register (1 bit)
(8) The I/O Error register (1 bit)

G Gates — The G Gates serve as a buffer between the central processing unit and memory. When memory is being directly addressed by external devices, the G Gates disconnect memory from the CPU allowing transfer between memory and the external device to take priority. During the time that the external device is using memory, the CPU enters an idle state for one cycle.

Memory — Memory for the computer is broken into eight 4,096 word banks. Memory isolation is provided between the CPU and each bank of memory allowing overlap between memory operations of the CPU and other external devices. If an external device requests a memory bank other than the one being requested by the CPU, both requests are honored simultaneously.

Switch Register — A switch register consisting of twelve switches is located on the front panel of the computer. Data can be transferred from the twelve switches into the accumulator under program control. Also, data from these switches may be transferred to any of the active registers during a halt mode operation. In the halt mode, the store switch may be used to store the data contained in the switch register in the memory location specified by the P counter.

INPUT/OUTPUT FACILITY

Communications with the SCS 650-2 computer can be accomplished by any of three basic means:

Programmed Data Transfer

This facility allows the computer to control the input/output sequence by initiating proper I/O instructions and testing to see if the external device is in a ready state. If the external device is ready, then the computer will initiate a data transfer and skip the next instruction. Programmed data transfer can be initiated by the programmer or by the external device using a program interrupt. Upon receipt of an interrupt from the external device, the computer will trap to the particular subroutine which is programmed to service the interrupting device.

Direct Memory Access

Individual data words or blocks of data can be entered into or taken from the computer memory directly through the direct memory access system. When operating in this mode, the computer will enter an idling state until the external device has completed the data transfer. If the external device is using a memory bank other than the one being requested by the computer, the computer may proceed without intervention. In this case, memory overlap occurs and the external device and the central processing unit are using different banks of memory simultaneously. After initiating a request for memory, the external device does not have to wait until the end of a current instruction to initiate a transfer. The maximum length of waiting time for such a transfer is one computer cycle or two microseconds.

Skip Testing

The computer contains a facility to allow the CPU under program control to request the status of external equipment and, based on the contents of that status, either skip or execute the following instruction. This feature allows the computer to make decisions during the program based on the condition of many external devices.

OPTIONAL EQUIPMENT

Extended Arithmetic Elements

This option allows the computer to perform a hardware multiply and divide using the X Register as an extended accumulator. This option also allows for added instructional capabilities for normalizing and scaling of data.

Memory Extension Control

The basic computer can be expanded to include eight banks of memory by using the memory extension control. The control provides all the logic elements necessary for the addition of seven memory banks.

Memory Modules

The basic memory module is a high speed, random access memory with a 2 microsecond cycle time consisting of 4,096 twelve bit words.

Analog Multiplexer

This option allows for the sequential sampling of 32 analog channels of 0 to 5 volts DC. The multiplexer contains a buffer amplifier and all the interface necessary for operation with the A-D Converter. The number of channels can vary in groups of two up to the maximum of 32. The computer can address the multiplexer on a random access basis or program the multiplexer for sampling the analog channels sequentially.

Analog to Digital Converter

The Analog to Digital Converter digitizes the output of the analog multiplexer to an eleven bit plus sign digital data word. Digitizing rates up to 50 KC can be provided. A sample and hold amplifier is included with the analog to digital converter.

High Speed Tape Reader

The high speed paper tape reader is an eight channel photo-electric unit which operates at a rate of 300 characters per second.

Paper Tape Punch

The paper tape punch punches an eight channel paper tape at the rate of 50 characters per second.

Card Reader

A punched card reader is available which reads at the rate of 200 cards per minute or at 400 cards per minute.

Card Punch

The card punch operates at a punching rate of 100 cards per minute.

Incremental Plotter

A CalComp Model 565 incremental plotter and control unit is available for the high speed plotting of points, continuous curves and points connected by lines.

Line Printer

This machine prints a selection of 64 characters at the rate of 300 lines per minute and with a 132 character per column format. The vertical format is selected by a punched paper tape within the printer.

Magnetic Tape Controller

The magnetic tape controller can control up to four magnetic tape decks simultaneously. Each magnetic tape can be controlled to read or write in densities of 200, 556, and 800 bpi and at speeds of from 75 ips to 120 ips.

Magnetic Tape Transports

The magnetic tape transports will write or read IBM compatible magnetic tape at transfer rates of 15 KC to 96 KC.

Interrupt Clock

A clock is available which generates an interrupt within the computer after a preset period of time has elapsed.

Teletype Input/Output Device

The Model 33 ASR Teletype set can be supplied with each computer. The ASR contains both paper tape reader and paper tape punch in addition to the normal typewriter keyboard.

Remote Teletype Unit

This option allows the Teletype I/O writer to be remotely located up to 1,000 yards from the central processing unit.

Selectric Typewriter

An IBM Selectric Typewriter with a maximum speed of 15.5 characters per second is available. The typewriter is equipped with a pin-feed platen allowing the use of continuous form paper.

MECHANICAL SPECIFICATIONS

Desk Model

The SCS 650-2 computer is housed in a standard size walnut desk with typewriter arm. The electronics is mounted inside the desk. Total weight of the desk model is 250 pounds.

Standard Cabinet Model

The cabinet model is rack mounted in a standard RETMA 19 inch relay rack, 6 feet in height. The teletype unit is contained on its own stand with the cabinet model. Total weight of the cabinet is 150 pounds. Weight of the Teletype with stand is 40 pounds.

Power Requirements

115 volts, 60 cycle, single phase, at 10 amps. 220 volts can be accommodated on special order.

Digital Signal Levels

0 Volts — False, + 8 Volts — True.

SOFTWARE

The SCS 650-2 includes a symbolic assembler, FORTRAN compiler, utility and math subroutines, and diagnostic routines. Other software is available from a library of programs. Custom programming is available through qualified personnel who are capable of obtaining maximum use and flexibility from the SCS 650-2.

AREAS OF APPLICATION

I. Business and Manufacturing in General

1. Office
Cost analysis
Forecasting
Inventory control
Mailing list operations
Management strategy analysis
Performance evaluation
Price analysis
Purchase order writing
Sales forecasting
Wage and salary analysis
Work-in-process records

2. Plant and Production
Assembly line balancing
Lathe operations: automatic control
Procurement
Production scheduling
Quality control records
Route accounting (bakeries, bottling plants, dairies, etc.

3. Libraries
Information retrieval
Records and control

4. Magazine Publishing
Classified advertisement preparation
Mailing list maintenance
Subscription fulfillment

5. Oil Industry
Depletion accounting
Map construction
Oil purchase accounting
Operating records: logging
Remote control of oil production
Seismic data reduction
Well logs: corrections

6. Textile Industry
Fabric quality control
Material availability evaluation
Production planning
Sales analysis
Style reporting

7. Transportation
Air traffic control
Aircraft maintenance scheduling
Collision warning systems
Navigating systems
Preventive maintenance scheduling
Travel reservations

II. Science and Engineering

1. Aeronautics and Space Engineering
Curve fitting
Flight control for missiles and space vehicles
Flight simulation
Flight test data reduction
Heat transfer analysis
Vibration analysis
Wind tunnel data reduction

2. Chemical Engineering and Chemistry
Gas line calculation
Process control
Spectrum analysis

3. Civil Engineering
Abutment design
Beam design
Cut and fill calculations
Earthwork computations
Freeway assignment
Highway profiles
Monthly equipment summary
Stress analysis
Triangulation

4. Electrical Engineering
Component design
Computer logic circuits; design by numerical control
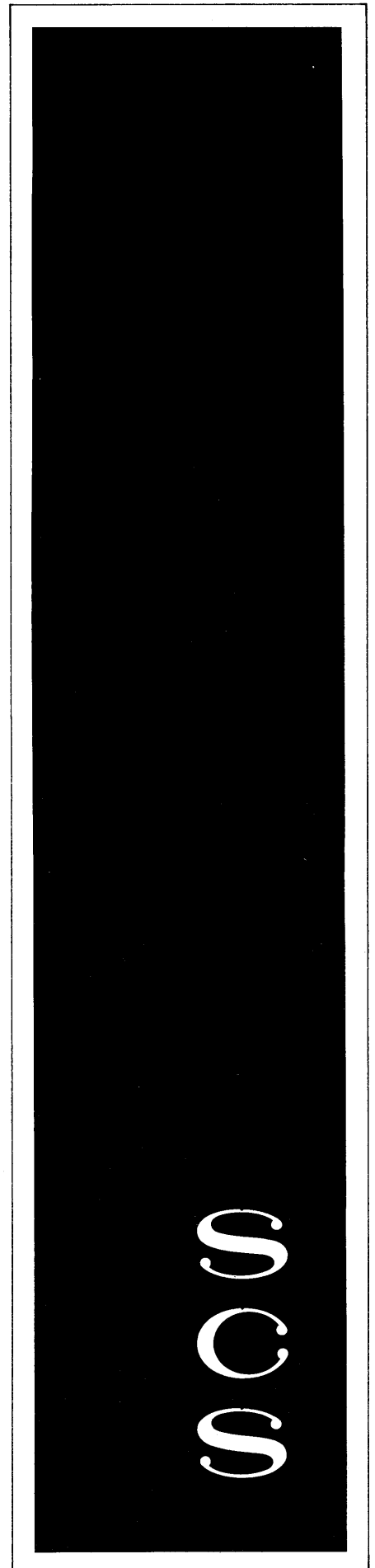Feedback system, single loop, finding the root locus

5. Mechanical Engineering
Air conditioning calculations
Heat flow
Machine vibration analysis

6. Medicine and Physiology
Telemetering and analysis of Medical data
Probability in medical diagnosis

7. Military Engineering
Ballistic trajectories
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