901594A

TECHNICAL MANUAL

SIGMA 3 CORE MEMORY

Specifications, equipment descriptions, and procedures contained herein are subject to change without notice.

April 1973

This publication supersedes 901594A
dated August 1972

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Sigma 3 Computer Reference Manual	901592
Sigma 3 Central Processor, Model 8101 , Technical Manual	901593
Sigma 3 External Input/Output Processor, Model 8171, Assembly No. 148557, Technical Manual	901595
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SECTION I

INTRODUCTION

1-1. SCOPE OF MANUAL

This manual contains technical information pertinent to the Sigma 3 Core Memory which is one of the main units included as part of the Sigma 3 Computer system. This manual describes the Sigma 3 Core Memory both physically and functionally as applied in the Sigma 3 Computer system.

This manual also includes information necessary to install and maintain the memory unit in the field of operation.

1-2. CONTENT OF MANUAL

The contents of this manual are sectionalized as follows: Section I contains an introduction to the equipment covered by the manual and to the method and type of coverage.

Section II contains a general description of the basic memory system operation. The overall mode of operation is divided into several functional groups of logic and each group is analyzed in the order of data transfer to, within, and from the memory system.

Section III provides detailed descriptions of the logic elements which comprise each functional group outlined in Section II.

Section IV provides unit installation and checkout procedures.

Section V contains preventive and corrective maintenance procedures for the equipment in the field of operation.

Section VI provides an illustrated parts breakdown and parts list of those field replaceable items and also provides a list of option items for basic memory system expansion.

1-3. RELATED PUBLICATIONS

A list of related publications, page , preceding Section I, is provided as additional reference material essential to the maintenance personnel to insure a complete awareness of proper installation, operation and maintenance of the memory system relative to the Sigma 3 Computer system.

1-4. PREREQUISITES TO MANUAL USE

In the construction of this manual, it is assumed the user is familiar with the functions of transistorized digital circuitry and can interpret MIL-STD-806B logic symbology. It is also assumed the user can interpret logic functions expressed in logic equation form and is familiar with machine language programming.

It is essential the user is capable of using standard test equipment in diagnosing and repairing hardware malfunction associated with digital equipment and has experience in the operation and troubleshooting of magnetic core memories.

1-5. SIGMA 3 CORE MEMORY

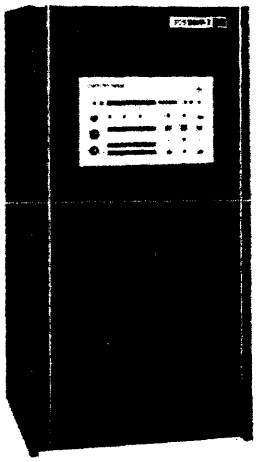
1-6. PHYSICAL DESCRIPTION

The Sigma 3 Core Memory consists of a basic building block of memory with provisions for optional expansion. This basic memory system is physically located in the No. 1 frame position of the Sigma 3 Computer system (Models 8101/8102) cabinet, as shown in figure 1-1.

The basic memory frame assembly consists of a nine-high frame and chassis which contain the logic for a single port access to a starter 8K expandable memory. The frame assembly also provides for the insertion of additional modules for optional memory expansion to a maximum 32K capacity.

The basic memory system occupies five chassis locations; C, D, E, H, and J. Chassis A and B are reserved for system logic other than the memory system, and chassis F and G are reserved for basic memory system expansion. Power supply PT16B, mounted on frame No. 2 provides regulated dc operating voltages of +4.0, -8.0 and +8.0 for logic circuits, and PT17B, mounted on frame No. 1, provides +25 volts (adjustable and non-adjustable) to drive the memory cores. High velocity fans at the top and bottom of the frame provide cooling for the drive circuitry and to keep the core diode modules at a temperature approaching the ambient air. The fans operate from 120V, 60 Hz power.

The basic memory system is physically and functionally divided into two sections; the basic memory unit (BMU) which provides an 8K stack of core and core drive logic, and memory port multiple (MPM) which provides a multiple port memory control with a single port interface.



SIGMA 3
COMPUTER

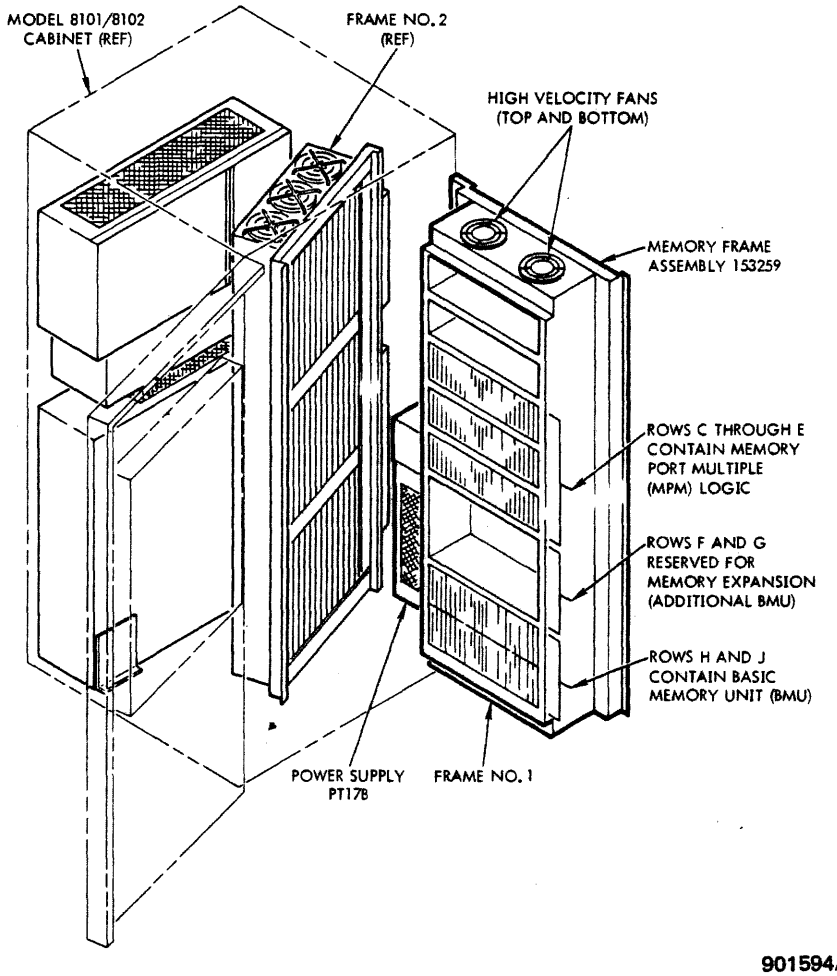


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Figure 1-1. Sigma 3 Core Memory Location in 8101/8102 Model Cabinet

1-7. Basic Memory Unit (BMU)

Chassis H and J provide for a fully expanded BMU or 16K of core and core drive logic. The basic memory system, however, contains a BMU consisting of four core diode modules (8K), twelve modules of core drive and sense logic and two ribbon cable connector cards for signal connection to the MPM. Refer to figure 1-2.

Extractor levers on all modules provide easy extraction of the module from the associated connector. Each module assembly terminates in printed circuit connector contacts which mate with spring type contacts in the associated connector mounted on an etched backwiring board (motherboard) at the rear of the chassis.

1-8. Core Diode Module (CDM). Each core diode module (figure 1-3) consists of hinged printed boards (2) with magnetic core arrays and associated decoding diodes; the printed circuit boards are insulated from each other by nylon spacers. The CDM is completely symmetrical both physically and electrically which provides for proper operation when inserted in either possible direction.

1-9. Core Drive and Sense Logic. The modules which contain the core drive and sense logic (refer to figure 1-2) are single 2-Hi printed circuit boards with board mounted detail electronic parts. These modules are not reversable (for insertion) as the CDMS, however, the modules conform to the general description in paragraph 1-7.

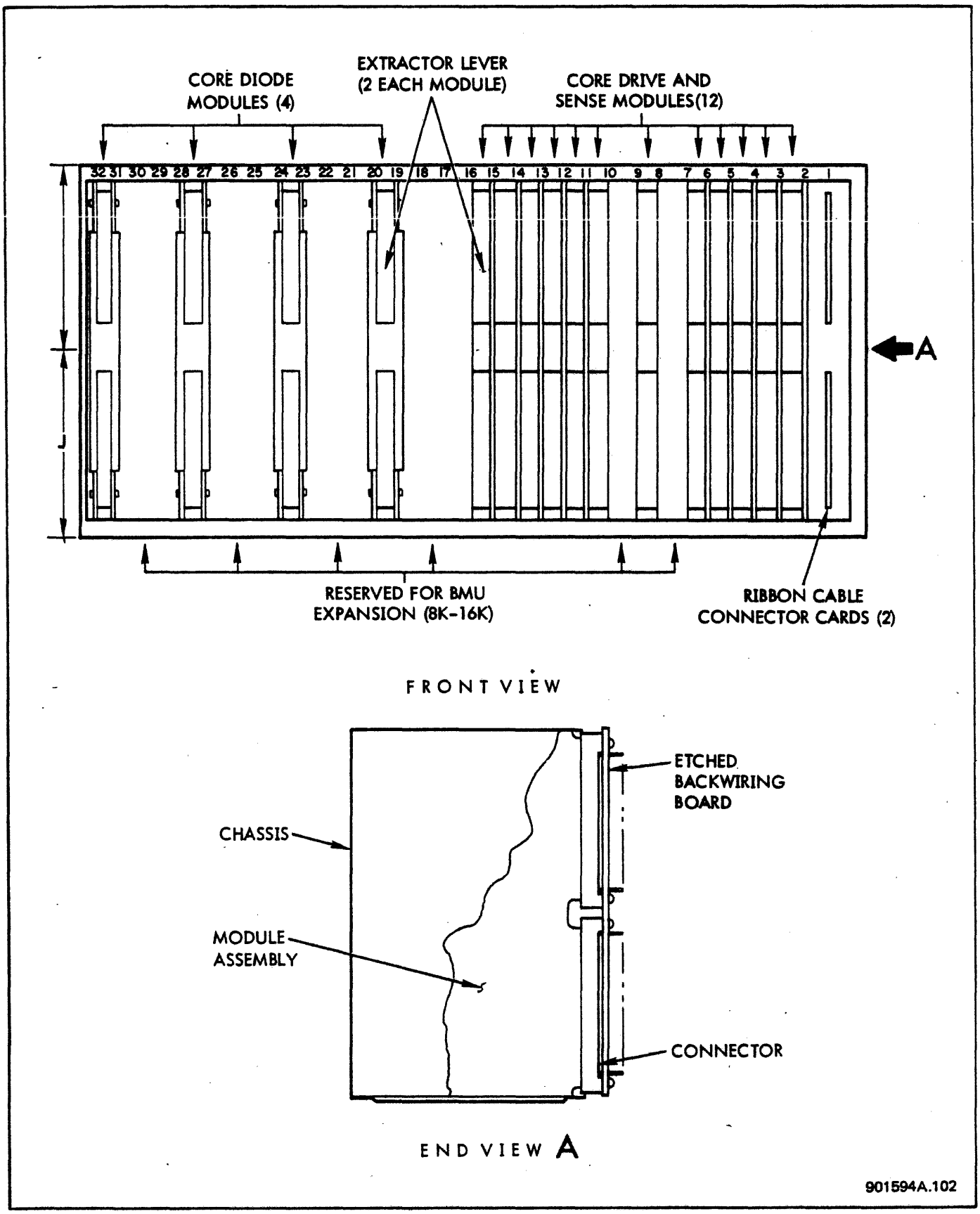


Figure 1-2. BMU Configuration for Basic Memory System

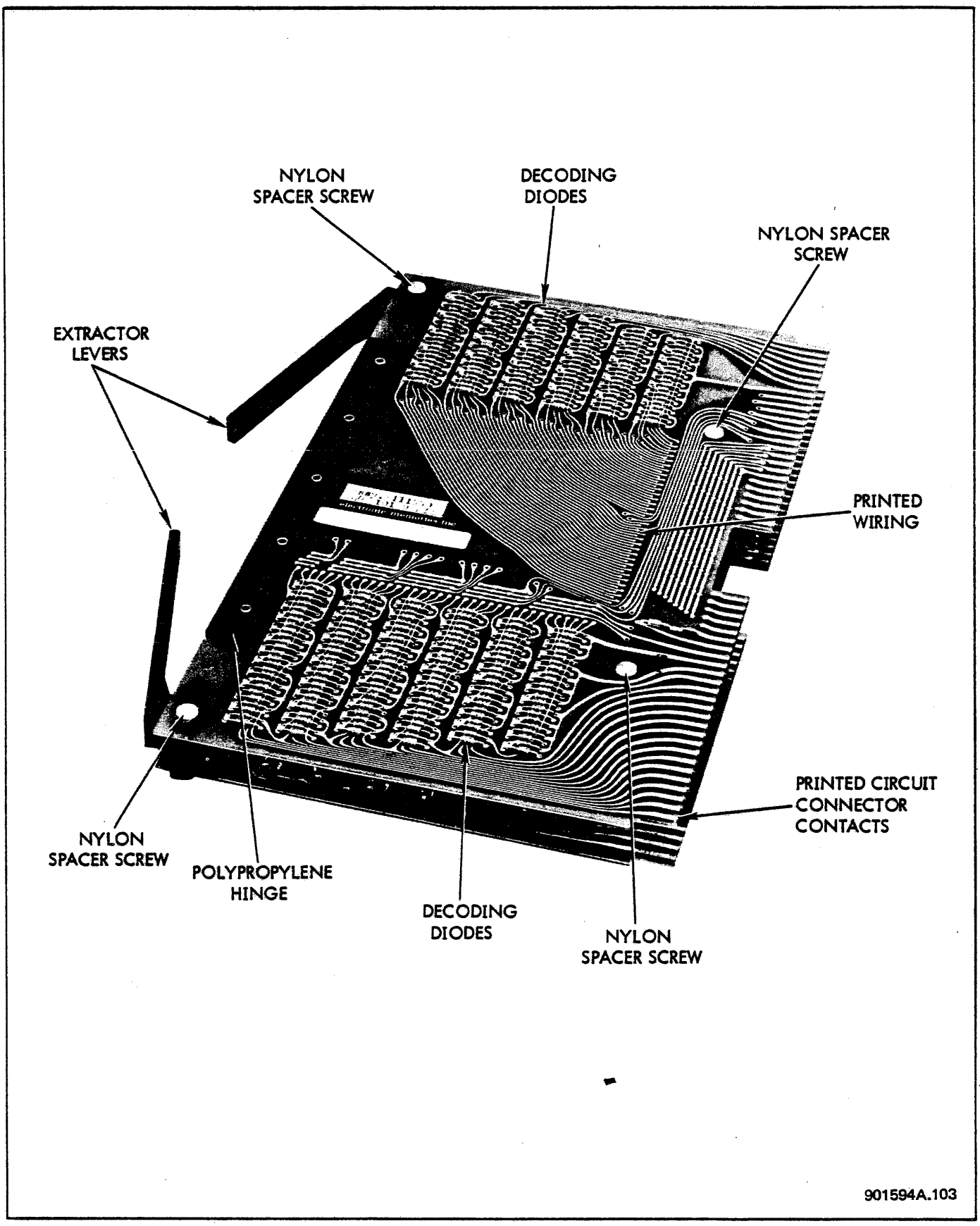


Figure 1-3. Core Diode Module (CDM)

1-10. Memory Port Multiple (MPM)

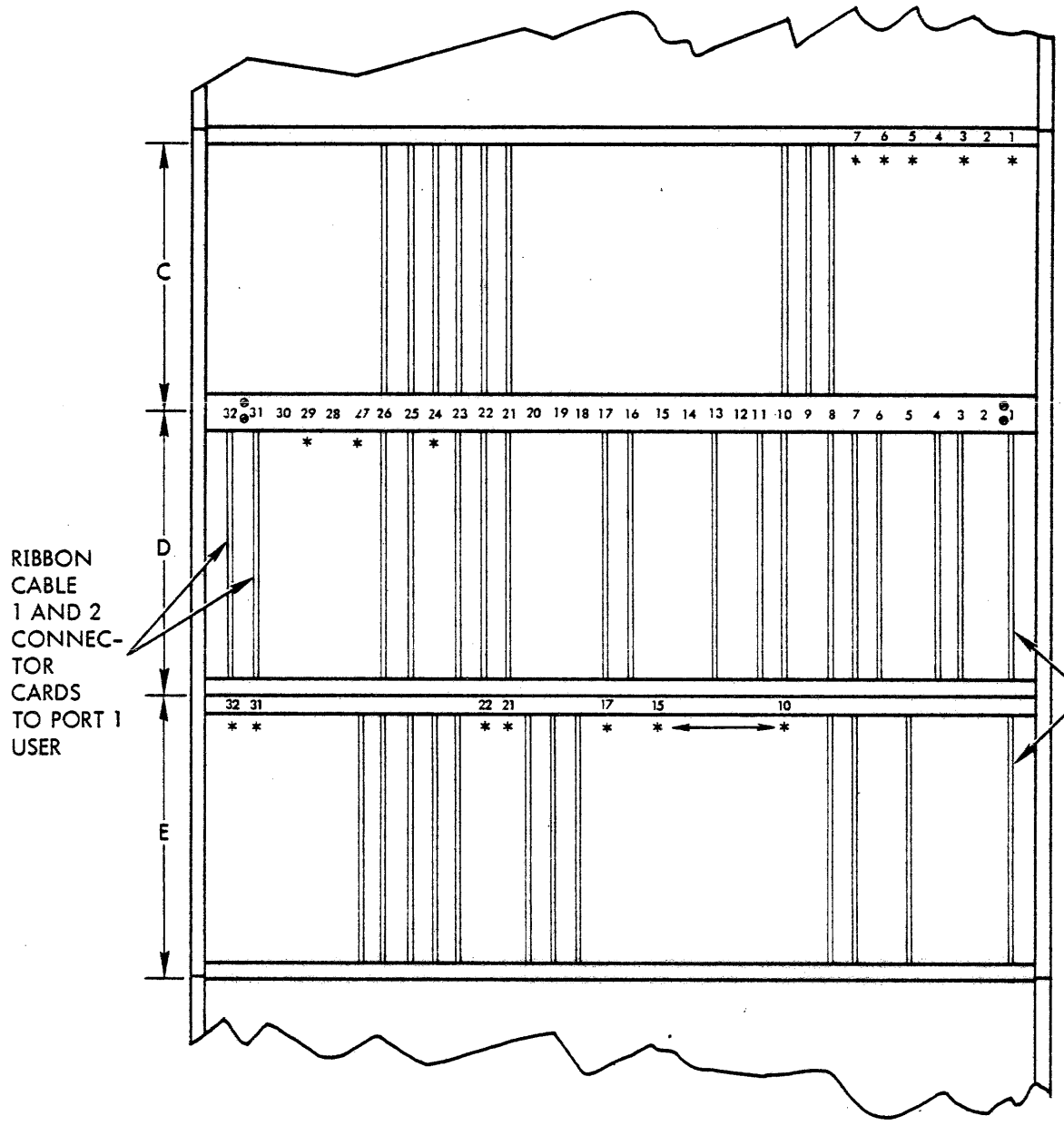
Chassis C, D, and E provide for a fully expanded MPM (four-port access to two expanded BMUS) However, the MPM portion of the basic memory system provides the logic for multiple port control and one port to access one expanded BMU (16K), this configuration is shown in figure 1-4.

The MPM section of the basic memory system consists of 35, one-chassis high modules and the necessary ribbon cable connector cards for connections between one port and the BMU and one port and the user. Each module is a printed circuit board with board mounted detail electronic parts. The modules terminate in printed circuit connector contacts and mate with spring-type contacts in the appropriate connector mounted on an etched backwiring board (motherboard) at the rear of the chassis. Provisions for electrical connections are identical to the basic memory unit, figure 1-2, view A, with the exceptions allowed for single-chassis high modules.

1-11. CAPABILITIES

The basic memory frame assembly provides the basic building block of the Sigma 3 Core Memory system. Figure 1-5 is a simplified block diagram showing the relation of this building block to a Sigma 3 Computer system when all optional memory expansion capabilities are utilized.

The basic memory frame assembly provides an 8K stack of core (8196 words) and one memory access port to a central processor (CPU) with an integral I/O processor (IIOP). With the addition of optional module kits, the basic memory can be expanded to provide for an access to a storage capacity of 32,768 words.



NOTE:

* THESE LOCATIONS ARE UNASSIGNED - ALL OTHER EMPTY LOCATIONS ARE FOR MPM EXPANSION

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Figure 1-4. MPM Configuration for Basic Memory System

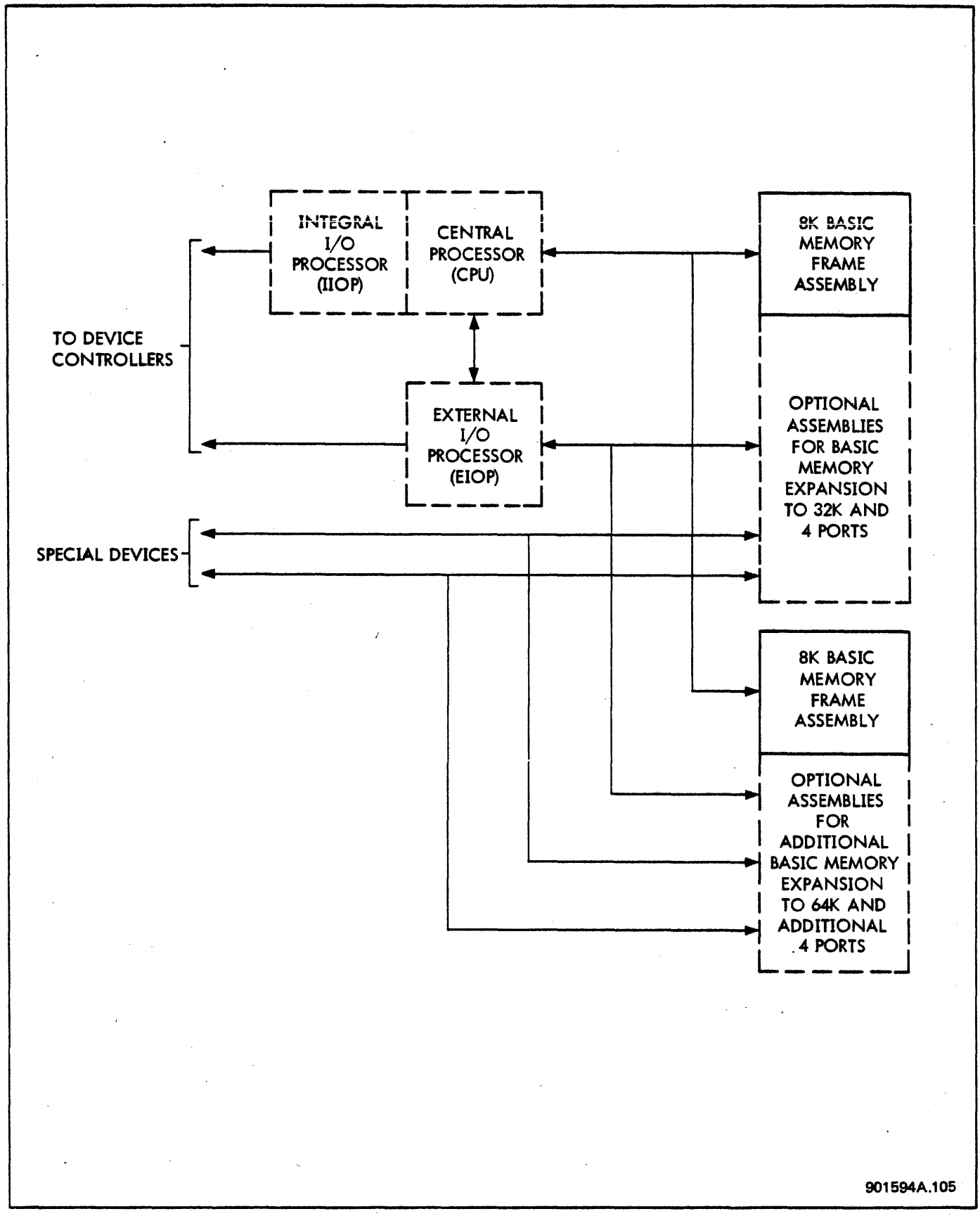


Figure 1-5. Relation of the 8K Basic Memory System to Sigma 3 Computer System of 64K

Further port expansion provides for direct communication with special devices selected to use the Sigma 3 Core Memory, and direct communication with an external I/O processor (EIOP) which greatly increases the speed of computation.

For a complete Sigma 3 Computer configuration, two fully expanded basic frame assemblies are used to provide a 64K memory. The second frame of memory, however, requires the No. 1 frame portion in an additional cabinet.

The expansion capabilities of the Sigma 3 Core Memory provide for a very flexible memory unit. A single port user can have access to a core memory ranging from 8K to 64K, several ports can share 64K of memory, or there is the availability of any variation of application in between.

1-12. Basic Memory System Expansion

The basic memory system is a fully operational system for controlling the transfer of data in and out of one 8K stack of storage area to one memory port user.

Physically, the Sigma 3 Core Memory system provides for expanding the basic system to a variety of larger memory configurations by the availability of optional module kits. Refer to figure 1-6. The basic memory unit (BMU) is expanded to 16K capacity by the installation of the optional 8K to 16K memory expansion kit. A second 16K bank is added to the memory system by the installation of the optional bank B drive (MPM expansion), an optional BMU and an 8K-16K memory expansion kit. A one to four-way memory access is obtained by the installation of the appropriate optional memory port assembly kits. With this type of expansion capability, two memory

banks of 16K operate independently, and different memory cycles take place simultaneously in the two banks under control of different ports.

1-13. MEMORY ADDRESS AND DATA WORD FORMAT

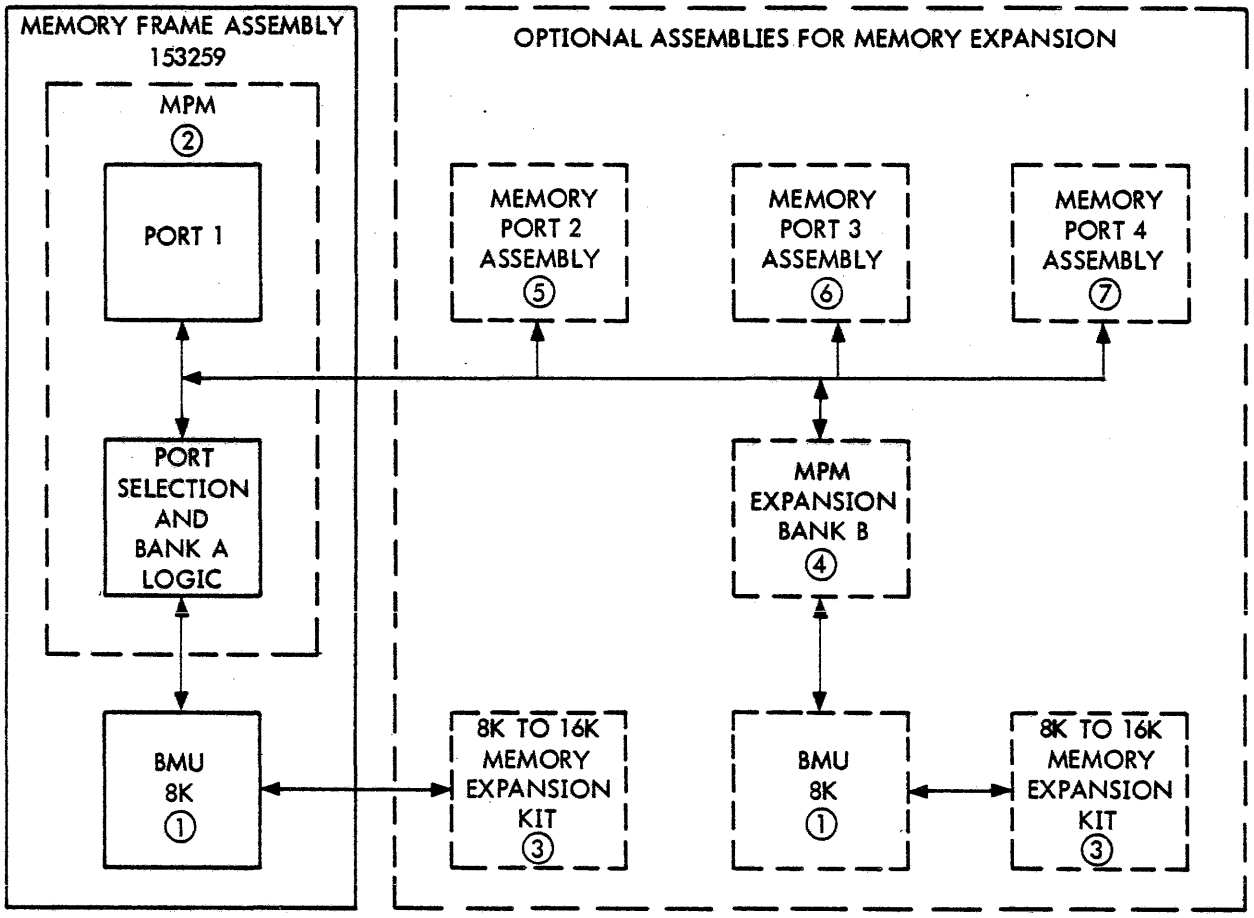
The Sigma 3 Core Memory uses an address word of 16 bits which allows for the addressing of 64K of memory. However, two fully expanded basic memory systems (32K) are required to utilize the entire address field.

The Sigma 3 Core Memory provides storage for a data word consisting of 16 bits of data and a parity bit.

1-14. MEMORY SYSTEM POWER REQUIREMENTS

The memory system utilizes voltage tabs on voltage bus-bar assemblies mounted on the memory frame assembly. Power is available from one side on the back panel. The voltages are referenced to the power supply ground. The power requirements are as follows:

VOLTAGE	MAXIMUM CURRENT	VOLTAGE TOLERANCE
+22 VDC (Nom)	8.5 amps	± 1%
+24 VDC	1.8	± 1%
+8 VDC	8.0	± 1%
-8 VDC	2.0	± 1%
+4 VDC	19.0	± 1%



LEGEND: ① 148418 - 8K BASIC MEMORY ASSEMBLY (BMU)
148423 - MEMORY CHASSIS ASSEMBLY
154492 - MODULE KIT ASSEMBLY (4 CORE DIODE MODULES, 12 CORE DRIVE AND SENSE MODULES) AND ASSOCIATED HARDWARE

② 149395 - MEMORY PORT MULTIPLE (MPM)
116231 - 32-MODULE CHASSIS (3)
149400 - WIRED BOARD
154643 - MODULE KIT ASSEMBLY (35 MPM MODULES, 4 RIBBON CABLES) AND ASSOCIATED HARDWARE

③ 149668 - 8K TO 16K MEMORY EXPANSION KIT
(4 CORE DIODE MODULES AND 2 CORE DRIVE MODULES

④ 149401 - BANK B DRIVE
(KIT OF 17 MPM MODULES AND 2 RIBBON CABLES)

⑤ 158910 - MEMORY PORT 2 ASSEMBLY
(KIT OF 3 MPM MODULES, 2 RIBBON CABLES)

⑥ 149403 - MEMORY PORT 3 ASSEMBLY
(KIT OF 7 MPM MODULES, 2 RIBBON CABLES)

⑦ 149404 - MEMORY PORT 4 ASSEMBLY
(KIT OF 3 MPM MODULES, 2 RIBBON CABLES)

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Figure 1-6. 8K Basic Memory Frame Assembly and Expansion Capabilities

1-15. Power Supplies

Power to the memory system is supplied by the PT-16B and PT-17B power supplies. The PT-16B, located on frame No. 2 which houses the CPU, supplies the +8V, -8V and +4V for logic circuit operation. These voltages are cabled from the PT-16B power supply to the bus-bar assembly on the memory frame assembly, frame No. 1.

Power supply PT-17B is located on frame No. 1 and supplies a non-adjustable +24V and an adjustable core drive voltage (nom. +22V) to the bus-bar assembly on the frame. The PT-17B is capable of supplying power to two fully expanded BMUS.

SECTION II

FUNCTIONAL DESCRIPTION

2-1. INTRODUCTION

The function of the Sigma 3 Core Memory in the Sigma 3 Computer system is dual-purpose; (1) to provide a core storage facility for data, and (2) to provide the means to control the interchange of data between core memory and a memory port user.

This section describes the logical methods used to perform the required data access and storing function of the basic memory system and follows the functional flow of figure 2-1. To facilitate an understanding of basic memory system operation, the following functional description is divided logically into two sections; the basic memory unit (BMU) section and the memory port multiple (MPM) section.

2-2. MEMORY PORT MULTIPLE (MPM) SECTION

The logic assigned to the memory port multiple section of the basic memory system provides the interface to one port, the capability to select multiple port input/output, and to control the data transfer to and from memory bank A (an expanded BMU of 16K.)

The memory address lines (16) from a port user will address two 32K frames of memory (64K). Since the functional description of data flow from one port to one bank of memory is typical for a complete memory system, figure 2-1 shows the interface between one port, port No. 1 and one bank, bank A.

The logic utilized in this section is grouped as follows: Port select, address decode and reset early logic which provides for (1) selecting a particular port for interface with memory (on a port priority basis), (2) for

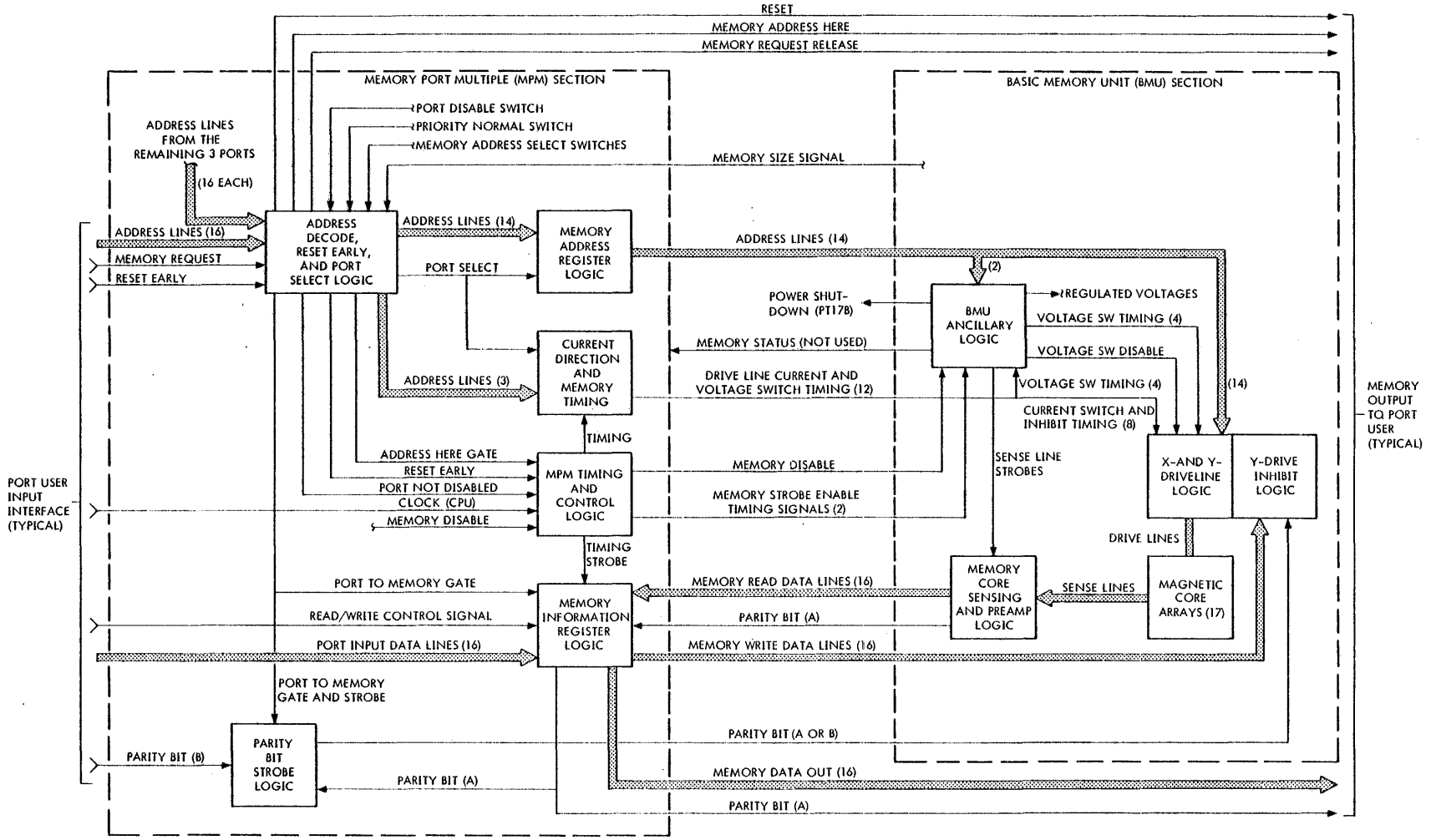

Figure 2-1. Basic Memory System, Functional Flow Block Diagram

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decoding the address for memory bank selection; and (3) for establishing a memory reset condition; the memory address register logic which supplies temporary storage for the selected memory address during the memory cycle; the memory information register logic which supplies temporary storage for data during the memory cycle; the MPM timing and control logic which provides the memory timing cycle and the port to/from memory data transfer signals; and the current direction and memory timing logic which supplies the timing signals to control the direction and application of core driveline current.

2-3. ADDRESS DECODE-RESET EARLY-PORT SELECT LOGIC

A port user requiring the use of the core memory will transmit a memory request signal. At the receipt of this signal the 16 memory address bits, which are also presented by the port user, are examined to determine if the address is within either bank (BMU) connected to the MPM. The basic MPM contains memory address select switches for ports 1 and 2 which define the starting address in terms of 8K increments for two banks of memory and the BMU supplies a memory-size signal (8K or not 8K) which indicates the size of each bank, 8K or 16K. The MPM also contains port disable switches to break with a particular port user.

If the port is disabled, the memory request from the port user is not recognized and also the user reset-early signal cannot reset the memory timing cycle. If the port has not been disabled and the memory address is available, the following events take place: A memory-address-here signal is developed and the memory timing cycle circuitry is enabled in the MPM timing and control logic; a port-to-memory gate is developed to connect the selected port to the selected memory bank and the memory-address-here signal is transmitted to the port user. A port-select transfer signal is also developed for transferring the address bits to logic within the MPM, and after the memory timing

cycle has started a memory-request-release is transmitted to the port user permitting the user to drop the memory request and change the address bits.

The port select logic determines the highest priority port that has an address-here condition, and with the port-select transfer signal, transfers those address bits (14) to the memory address register associated with the bank which is addressed. At the same time, three of the address bits are also selected for decoding by the current direction and memory timing logic.

The MPM has two modes of priority determination between ports; the mode is selected by the setting of the priority-normal toggle switch. When the priority-normal switch is set to normal, port select logic selects port 4, port 3, port 2 and port 1, in this order. If two or more memory requests are received at the same time, the port with the higher priority is processed first, then each one in descending order is processed before any new requests are considered. This prevents high data rate devices from locking out other devices.

When the priority-normal switch is set to a position other than normal, a straight priority scheme prevails where the higher priority port may use every memory access to the exclusion of the other ports.

2-4. MPM TIMING AND CONTROL LOGIC

After the address-here condition has been satisfied and the MPM timing and control logic has been enabled, the following events can take place: If the memory is not busy with a previous request and a port has not

commanded an early reset (return to initial condition) of the timing cycle, the memory timing cycle (read/write sequence) is started at the receipt of the first clock B pulse from the CPU. This clock pulse is used only to synchronize the beginning of each memory cycle; after the cycle has started the memory timing and control is asynchronous.

The MPM timing and control logic provides a timing delay line with the necessary control circuitry. A full timing cycle consists of two consecutive transmissions through the delay line. Pickoff signals at specific time-from-start points on the delay line establish the time for certain events to take place during the read sequence (first transmission) and the write sequence (second transmission). The pickoff signals determine the on/off time and direction of the driveline current in the BMU as well as time to generate strobe signals for the sense line circuits.

2-5 MEMORY ADDRESS REGISTER LOGIC

At the time port priority has been established, 14 of the 16 original address bits from the port user are transferred (by the port-select transfer signal) to the memory address register associated with the addressed memory bank (refer to paragraph 2-3). These address bits enable the X and Y driveline circuitry associated with specific core locations in memory. The addressed bits are latched in the register until the register is reset near the end of the write half cycle of the memory cycle.

2-6 CURRENT DIRECTION AND MEMORY TIMING LOGIC

Reading out of or writing in to memory involves the requirement to establish coincident X and Y current at the cores selected for information; part of the address, therefore, determines the direction of each current in relation to the other (both positive or both negative).

When a port has been selected three bits of the memory address are converted, by the current direction and memory timing logic, to X and Y current direction codes. These codes are transferred by the port-select signal to an X and Y driveline timing circuit within the same logic group. During specific phases of the timing cycle, these codes are used to develop the twelve X and Y driveline timing signals which turn on the positive and negative current and voltage driveline switches in the BMU.

2-7 MEMORY INFORMATION REGISTER LOGIC

The memory information register logic group contains a memory information register for temporarily storing 17 bits of data read out of memory or presented by the port user, and additional circuitry for restoring data back into memory or writing new data into memory.

A mode control signal (read or not read) from the user determines the source of data written into core during the write portion of the memory cycle.

At the beginning of the memory cycle, if the logic state of the user's mode control signal is at the level to select the read mode of operation, 17 bits of data are strobed from memory to the memory information register and transferred from the register to the port user. During the write half cycle portion of the memory cycle this data is gated back into memory (data restore operation) through the inhibit circuitry in the BMU.

At the beginning of the memory timing cycle, if the logic state of the user's mode control signal is at the level to select the write mode of operation, the transfer from memory is inhibited during the read half cycle portion; and the 17 bits presented by the user for writing in to memory is transferred, during the write half cycle, through the inhibit circuitry.

The memory information is cleared (reset) near the end of the write half cycle of the memory cycle by the change in the logic levels of the mode-control signal and/or the port-to-memory gate.

2-8. PARITY BIT STROBE LOGIC

The parity bit is generated by the user, and since 16 bits of data must be assembled before this bit is generated, it lags the data presented and is processed separately. The MPM section provides the circuitry to transfer the parity bit from memory (parity bit A) to the port user, and strobe the parity bit from the user (parity bit B) into memory.

2-9. BASIC MEMORY UNIT (BMU) SECTION

The basic memory unit section receives 14 bits of a decoded address on parallel address lines. These address bits locate the core storage area for writing in or reading out information in memory. Two separate groups of data lines are provided for the input and output of 16 data bits (plus parity.) There are no registers in the BMU and therefore the MPM section of the basic memory system performs the storage function of the address and data bits during the memory cycle. The memory cycle (read and write sequence) is controlled by timing pulses generated in logic circuits also provided by the MPM section.

At the beginning of the memory cycle, if the read mode is selected, data is strobed from the cores on the memory read data lines to the selected

port memory information register for output; conversly, if the write mode is selected, data from the cores are blocked during the read portion and, at the beginning of the write portion of the cycle, port input data is transferred to memory on the write data lines.

The BMU employs a 3-wire (X,Y, and sense) memory system or what is known as the 2-1/2 D organization. The system does not have an inhibit wire; the Y wire is common to both core driving and inhibiting.

The logic utilized in this section is grouped as follows: The X and Y driveline logic which drives the magnetic memory cores, the memory sense and preamp logic which provides signal amplification and discrimination when reading out a core, and additional logic necessary to support the drive and sense circuitry.

2-10. X AND Y DRIVELINE LOGIC

Each magnetic core represents a bit position in memory and is located by a unique set of X and Y drivelines and each line is driven by bipolar current and voltage switches. Each line carries one-half the current required to change the logic state of the core. Predrive switch circuits, selected by address terms and gated by X and Y driveline timing signals (12) from the MPM section, drive the bipolar current and voltage switches.

Each bit plane has an inhibit circuit which controls current flow through a selected Y driveline, this inhibit action prevents (writes a zero) or allows the writing of a logic one in an addressed core.

The BMU contains protect features which prevent damage to the X and Y driveline circuitry when abnormal airflow, voltage or timing conditions exist. Refer to BMU ancillary logic, paragraph 2-12.

2-11. MEMORY CORE SENSING AND PREAMP LOGIC

The logic state of each bit position (core) in a word is sensed by a sense wire threaded through the core together with the X and Y drivelines.

During a read cycle, the address select circuits in the X and Y driveline logic feed current through the appropriate X and Y drivelines. If the currents are additive in either the positive or negative direction the core switches from one polarity (representing a logic one or zero) to the other. This switching of the logic state causes a pulse on the associated sense line. At the arrival of the senseline strobe signals generated in the BMU ancillary logic, paragraph 2-17, the pulse is amplified by the selected preamp circuits, and discriminated and converted by sense amplifier circuits to a convential logic level. These logic levels (data) are fed onto the memory read data lines for memory information retister output to the selected port user and back to the core.

2-12. BMU ANCILLARY LOGIC

The BMU ancillary logic provides protect features which prevent damage to driveline switches when power drops below operating limits or timing conditions exist; data-save is also provided. The ancillary logic also augments the drive, predrive and sensing circuitry.

This logic group is mechanized by airflow and voltage monitor circuits, timing pulse protection circuits, a predrive disable circuit, voltage generation and regulation circuits and preamp select and strobe driver circuits.

2-13. Airflow and Voltage Monitor Circuits

The airflow monitor circuit senses airflow rate (fan-vane position) of either of two cooling fans installed in the bottom section of the memory frame; and provides a signal to disable the PT-17B power supply (power shutdown signal.)

During power-up or power-down cycle, the memory disable signal from the power monitor circuit is used to override the airflow monitor circuit output. This action prevents false tripping of the PT-17B circuit breaker during a temporary low-fan-power condition.

The voltage monitor circuit senses the value of +8V, +4V, +24V, and -8V supply voltages and causes a predrive disable circuit to be activated when any of these voltages fall below predefined limits. In addition to activating the predrive disable circuit, this monitor allows a memory status signal to go true (memory not operating.) The memory status signal is true when the output of both the voltage monitor and airflow monitor circuits is true. (Note: Although the memory status signal is made available to the MPM section through the logic contained in the BMU, it is not used in the Sigma 3 configuration.)

2-14. Timing Pulse Protection Circuits

Each pair (pos & neg-X or pos & neg-Y) voltage switch timing pulses are guarded against overlap by the provision of delay latch circuits in the ancillary logic. These circuits control minimum spacing between positive and negative timing pulses to prevent damage to the corresponding voltage switches when switching from a read to a write operation. The latches also prevent damage due to complete loss of timing pulses. An interlock signal grounds the timing pulses in case the ancillary logic module is removed while the power is still applied.

2-15. Predrive Disable Circuit

The predrive disable circuit prevents memory accessing by grounding the predrive circuits in the X and Y driveline logic during the following conditions: Power turn-on/turn-off cycles, airflow failure and voltage failure. During power trun-on/turn-off cycles, the memory disable signal activates the predrive disable circuit. The output from the airflow and voltage monitor circuits (paragraph 2-13) activate the predrive disable circuit during airflow failure and voltage failure.

The predrive disable circuit causes data to be saved and damage to the voltage switches is prevented when power drops.

2-16. Voltage Generation and Regulation Circuits

The voltage generator and regulator circuits in the ancillary logic provide for the following: (1) Discrimination level voltage (threshold) for the sense amplifiers in the memory core sensing and preamp logic, (2) Start level voltage for the sense amplifier strobe driver, (3) Bias voltage for the current source circuit in the preamplifier circuit, and (4) Bias voltage for the X and Y voltage switches developed from the driveline voltage.

2-17. Preamp Select and Strobe Driver Circuits

Two timing pulses from the MPM section (memory strobe enable) are used to activate the preamp select circuit and the strobe driver circuit in the ancillary logic. Two address bits and one of the timing pubses turnon the preamp select circuit which generates one of the sense line strobe signals used in the memory core sensing and preamp logic. The other timing pulse is used to gate the strobe driver circuit which generates the remaining sense line strobe signal. Refer to paragraph 2-11 for application of these sense line strobe signals.

SECTION III

DETAIL PRINCIPLES OF OPERATION

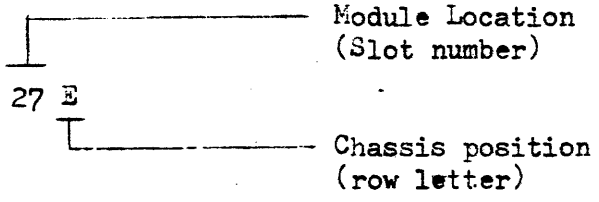
3-1. INTRODUCTION

This section contains detail descriptions of the logic and the mechanization of the logic used in the Sigma 3 Core Memory system in the performance of the required data access and storing functions of the Sigma 3 Computer System.

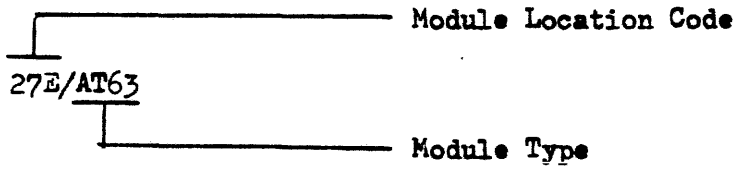
This section follows the outline of Section II, however, the logic groups are further divided in order to key the detail principles of operation to the Engineering Support Manual (ESM) 902401, Sigma 3 Core Memory (hereafter referred to as ESM 902401). The text content is based, generally, on figure 3-4, Detail Principles of Operation, Block Diagram.

Individual logic diagrams are used throughout the text to support the detailed descriptions of the mechanization of the logic equations contained in Section I of the ESM 902401.

A module location is designated by a code representing the module position number (slot) in the chassis and the chassis position (row) in the frame. The module slots are numbered (01 - 32) as viewed from the module-insertion side of the chassis. The chassis positions (9) are lettered A through J (excluding I) beginning at the top of the frame. An example of module location is as follows:



In most cases another code is added to the module location code to designate the type of module, as follows;



The information contained in this section pertinent to the Sigma 3 Core Memory power is general technical coverage. For detail theory of operation and maintenance refer to the applicable Data Package for the PT-14B, PT-15B, PT-16B and PT-17B power supplies; 901655, 901656, 901657 and 901658, respectively.

3-2 SIGMA 3 POWER DISTRIBUTION

Figure 3-1, a block diagram of the Sigma 3 Power Distribution, in included in this section in order to show the position of the Sigma 3 Core Memory in the overall power supply structure.

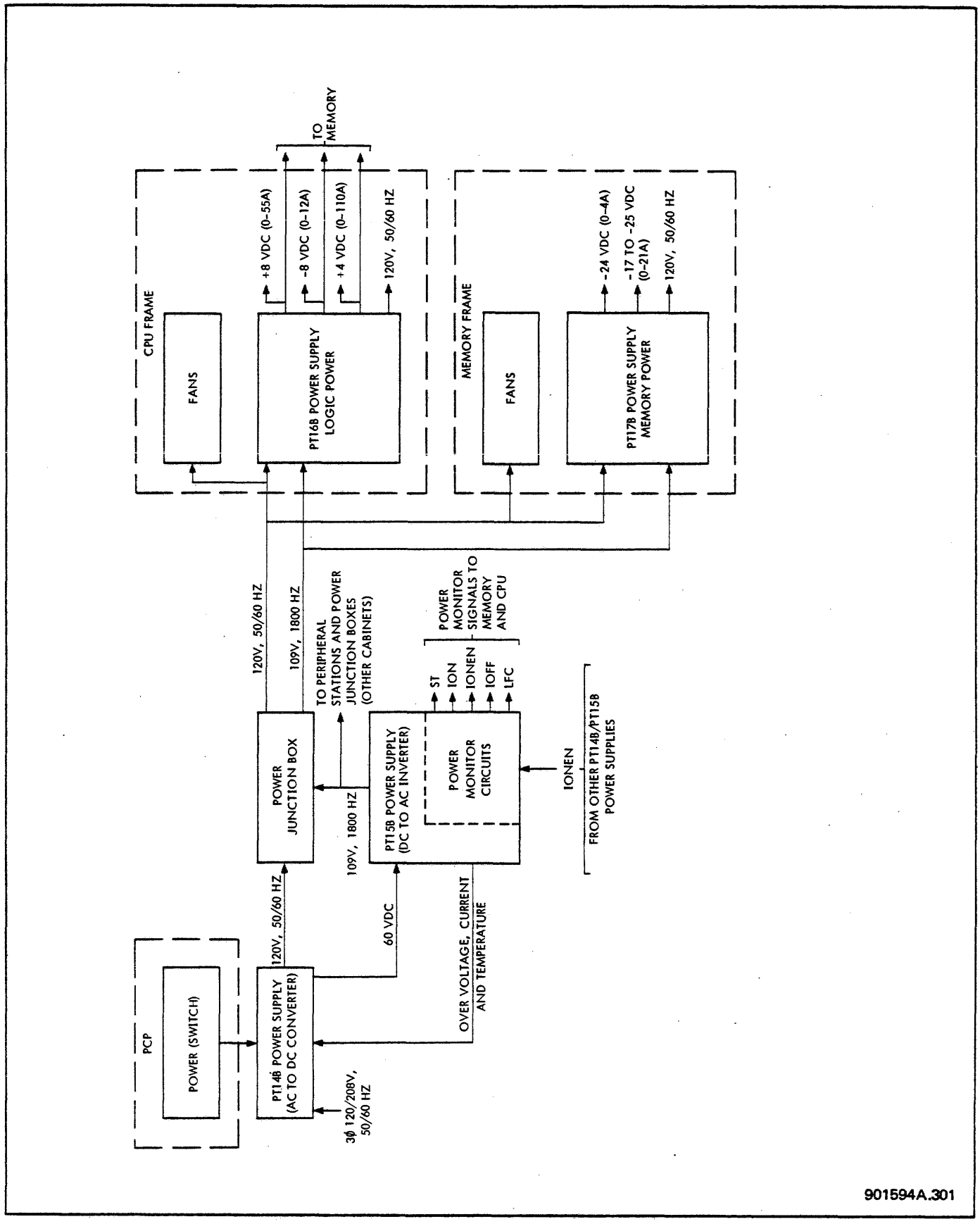


Figure 3-1. Sigma 3 Power Distribution

When the POWER switch on the Sigma 3 Computer system processor control panel (PCP) is pressed, 3 phase, 120/208V, 60 mHz, facility power is applied to the first internal power supply, PT-14B. The PT-14B supply converts the facility power to 60 VDC to power the PT-15B power supply. Also, a 120V, 50/60 mHz output from the PT-15B is cabled to a power junction box for distribution within the system.

The PT-15B power supply converts the 60VDC to an ac voltage of 109V, 1800 mHz which is connected to the power junction box for distribution to the PT-16B and PT-17B power supplies. This voltage (109V, 1800 mHz) is also available to peripheral stations and the power junction box in other cabinets of the computer system.

The PT-15B also contains circuitry which monitors overvoltage, overload and fan failure. When anyone of these conditions prevail, the main circuit breaker in the PT-14B is opened, disconnecting the facility power. If the power fail safe option is included in the Sigma 3 System, PT-15B will contain power monitor circuits. Refer to paragraph 3-3 for detail description.

The 120V, 50/60 mHz junction box output is used to operate the fans on the CPU and memory frames and is available as auxiliary power for other general applications.

The PT-16B power supply converts the 109V, 1800 mHz power from the PT-15B to regulated dc power for logic circuit operation. The dc output is +8 V, -8 V, +4 V and is made available to all logic circuits in frame No. 2 through bus-bar assemblies mounted on the frame.

Two pig tails terminating in connectors P1 and P2 from the PT-17B power supply (refer to figure 3-2) are connected to 109V, 1800 mHz and 120V, 50/60 mHz, respectively, from the system junction box. PT-17B converts the 109V, 1800 mHz to two regulated dc voltages. One voltage is VC, a non-adjustable +24 volts used for the predrive circuits in core memory. The other, an adjustable nominal +22 volts is used to drive the X and Y drivelines in core memory. These voltages are distributed to both BMUS via the core voltage bus-bar. The 120V, 50/60 mHz is routed out through connectors P5 and P4 to the upper and lower frame-ventilating fans.

The memory logic circuit operating voltages are cabled (7) from the voltage bus-bar on frame No. 2 from the PT-16B power supply. These logic operating voltages are distributed to all chassis in the memory frame (No. 1) via the logic voltage bus-bar.

3-3 MEMORY PROTECT FEATURES

During power turnon/turnoff or failure the power monitor system (optional) generates signals which provide for the selection of two interrupt levels (CPU option), a system reset-early sequence (MPM), as well as a signal to the predrive disable circuit in the BMU to protect the voltage switches in core memory.

The predrive disable circuit is also enabled when a voltage monitor circuit in the BMU detects the dc power supplies have dropped below the following limits:

+8V supply	$\leq$ +6V
+4V supply	$\leq$ +3V
-8V supply	$\leq$ -4V
+24 supply	$\leq$ +20V

The voltage monitor circuit operates independent of the power monitor system output.

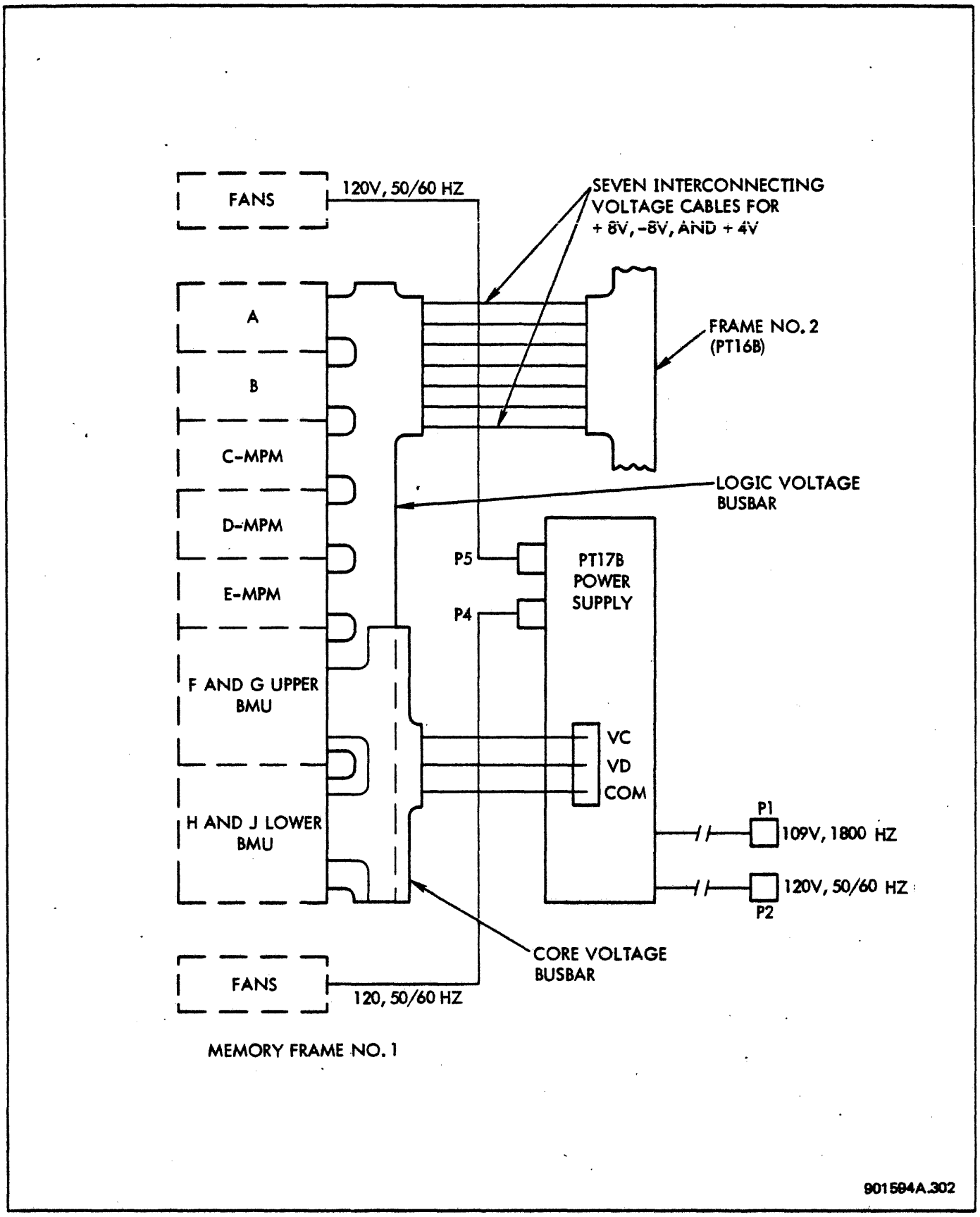


Figure 3-2. Power Distribution to Sigma 3 Core Memory

3-4. POWER MONITOR SYSTEM

Refer to figure 3-3. The 60 VDC input to the PT-15B power supply is monitored, which in effect, is monitoring the facility input power to the PT-14B power supply. When power is turned off or there is a power failure, IONEN (power-on enable interrupt) and IOFF (power-off interrupt) are true. IOFF is true for 5 milliseconds during which time the CPU performs a software interrupt subroutine to store all volatile registers to prevent critical program loss. At the end of 5 milliseconds, an ST (start/stop) signal goes true and stays true until the output of the dc supplies have decayed to a minimum of 15% of the initial values.

The ST signal is one of two possible input signals to the reset-early circuit (paragraph 3-10) in the AT63 module in memory (MPM) where it inititates the reset-early sequence. During the reset-early sequence, memory port input is inhibited and latches are dropped on MPM timing logic. The ST signal is also applied to a special line receiver circuit in the WTT10 module (BMU). This circuit prevents damage to the predrive voltage switches (when power is unstable) by grounding the drive voltage (VC) at predrive resistors, YVPR and XVPR. Refer to ESM 902401, drawing No. 153726, sheet 4, for further details.

When power starts up (or turned on) ST goes true and after 3 microseconds STM enables the predrive disable circuit. ST stays true until the dc power supplies are stabilized (1 to 3 seconds). When ST goes false, ION (power-on interrupt) is true and the CPU performs a subroutine to restore all critical conditions existing prior to the power-off state.

The LFC (PWRFREQ) line frequency clock is the output of a schmitt trigger circuit in the AT67 module and can be used as an input to counters 4, 3, and 2 in the CPU internal priority interrupt system.

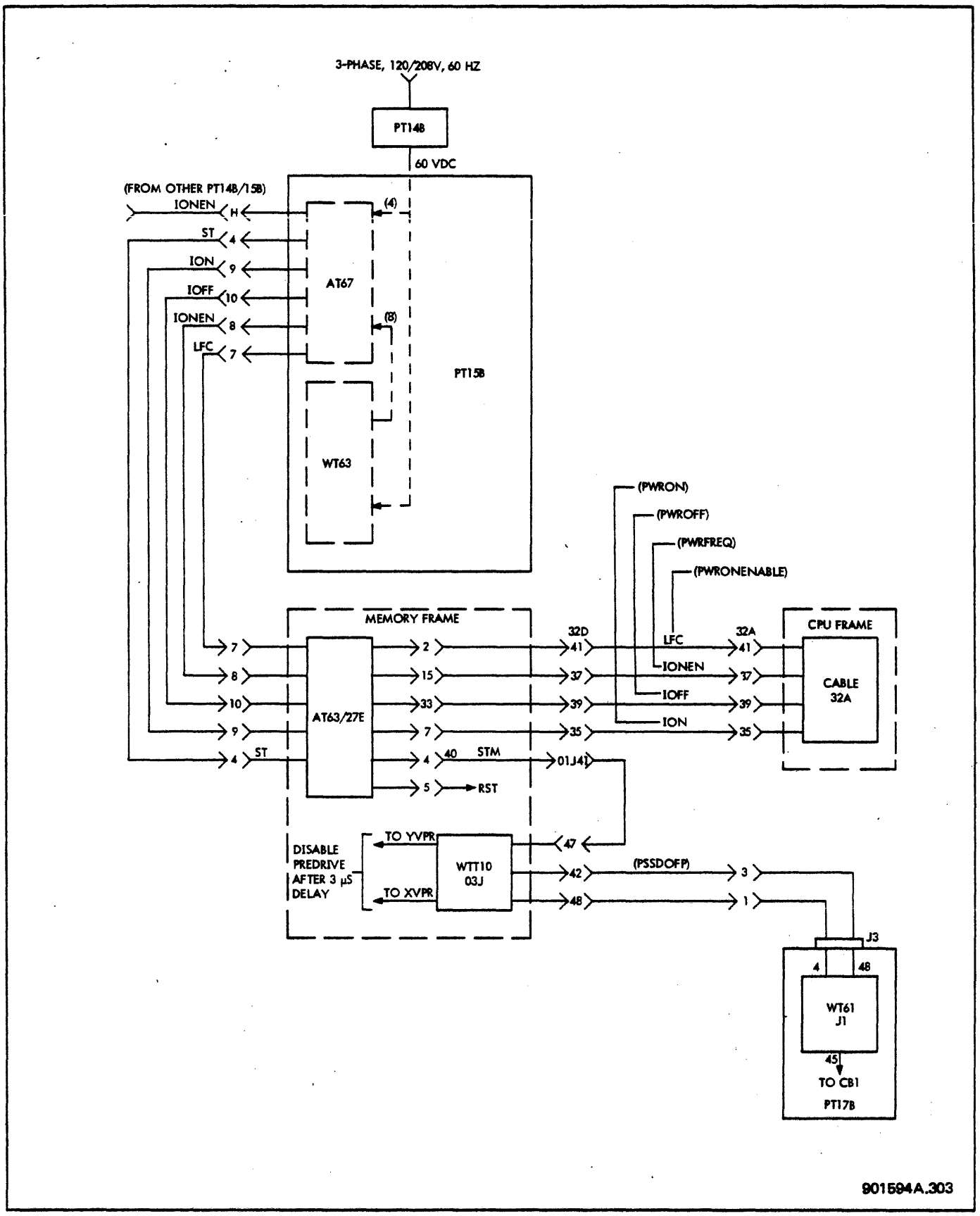


Figure 3-3. Sigma 3 Power Monitor System (Power Fail-Safe) and PT17B Shutdown

3-5. PT-17B SHUTDOWN

The BMU provides an airflow monitor circuit which monitors the temperature of the lower memory frame fan area. The output of two thermistor circuits installed on the WTT10 module is input to the monitor circuit. When the monitor senses airflow failure (rise in temperature) PSSDOFP (which is normally false) goes true and turns on a circuit in the VC and VD overvoltage monitoring circuit on the WT61 module in the PT-17B power supply. (Refer to the associated ESM, Section II, drawing No. 153726, sheet 4.) A subsequent pulse generated by the overvoltage circuit triggers the SCR in the PT-17B power supply which in turn triggers the circuit breaker (CB1).

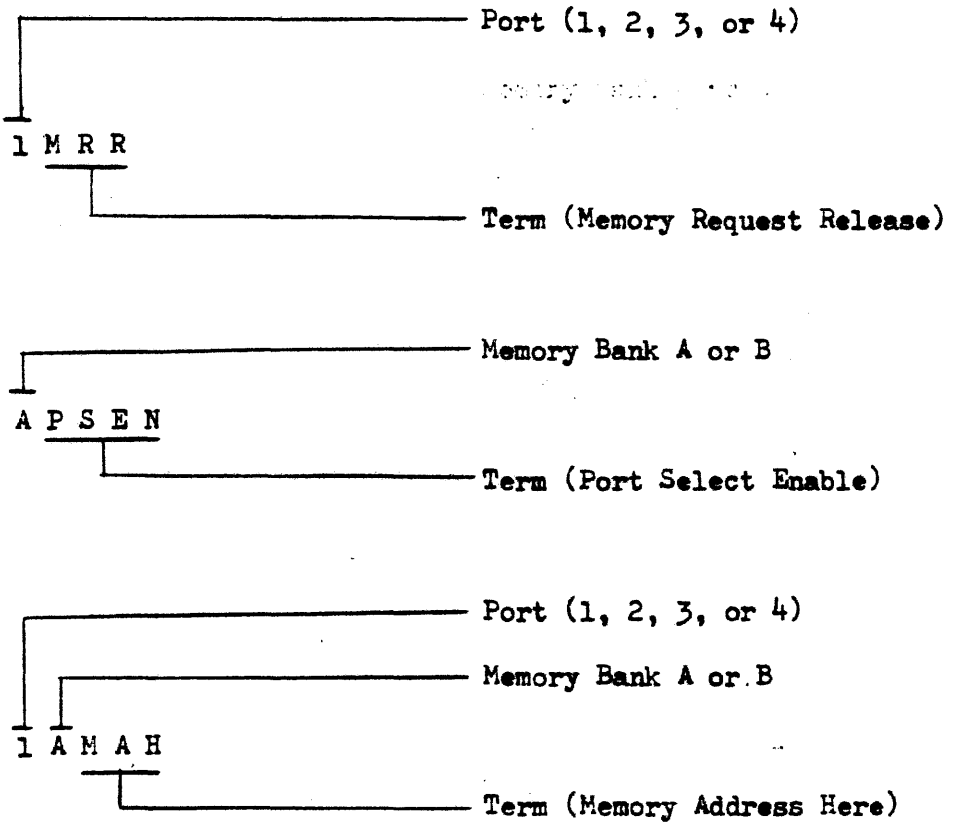
The ST signal from the power monitor system (paragraph 3-3) is also used to keep PSSDOFP low during power turnon/turnoff sequence and therefore not trigger the PT-17B circuit breaker if the airflow fails at this time.

3-6. SIGMA 3 CORE MEMORY LOGIC

Sigma 3 Core Memory logic is documented in Section III of this manual and in ESM 902401. The circuit diagrams in this section are keyed to the line numbers in the Logic Equations, Pin List and Pin Index in Section I of the associated ESM. The text contained in this section is referenced to information contained in Section II of the ESM 902401 for Logic Glossary and further details pertinent to circuit descriptions.

Figure 3-4, Detail Principles of Operation, Block Diagram , is an overall representation of the logic involved in the Sigma 3 Core Memory. Primary internal and interface terms associated with the system are shown. Terms at the port interface are enclosed within two diagonal lines / /. The first character, if a number in the complete term, represents a port (1, 2, 3, or 4); or if a letter, the letter represents a memory bank (A orB). The second character , if A or B and preceded by a port number, is the

memory bank A or B. Three typical complete logic terms are:



The letter N preceding a complete term designates the negation of the term.

3-7. SIGNAL DISTRIBUTION

Refer to MPM Cable Table ESM 902401, Section II, drawing 155369, MPM Module Location Chart 153272, and BMU Module Location Chart 153726.

The major portion of signal distribution, externally between a user and a memory port and internally between the MPM and BMU sections, is achieved through ribbon cable assemblies. Two ribbon cable assemblies (ZT45), terminating in etched-circuit boards at right angles to the cables, distribute signals between the MPM and BMU sections (two for each, bank A and bank B). The ribbon cables extending from 01D to 01H and 01F to 01J distribute the signals listed in the Interface Table in 153726.

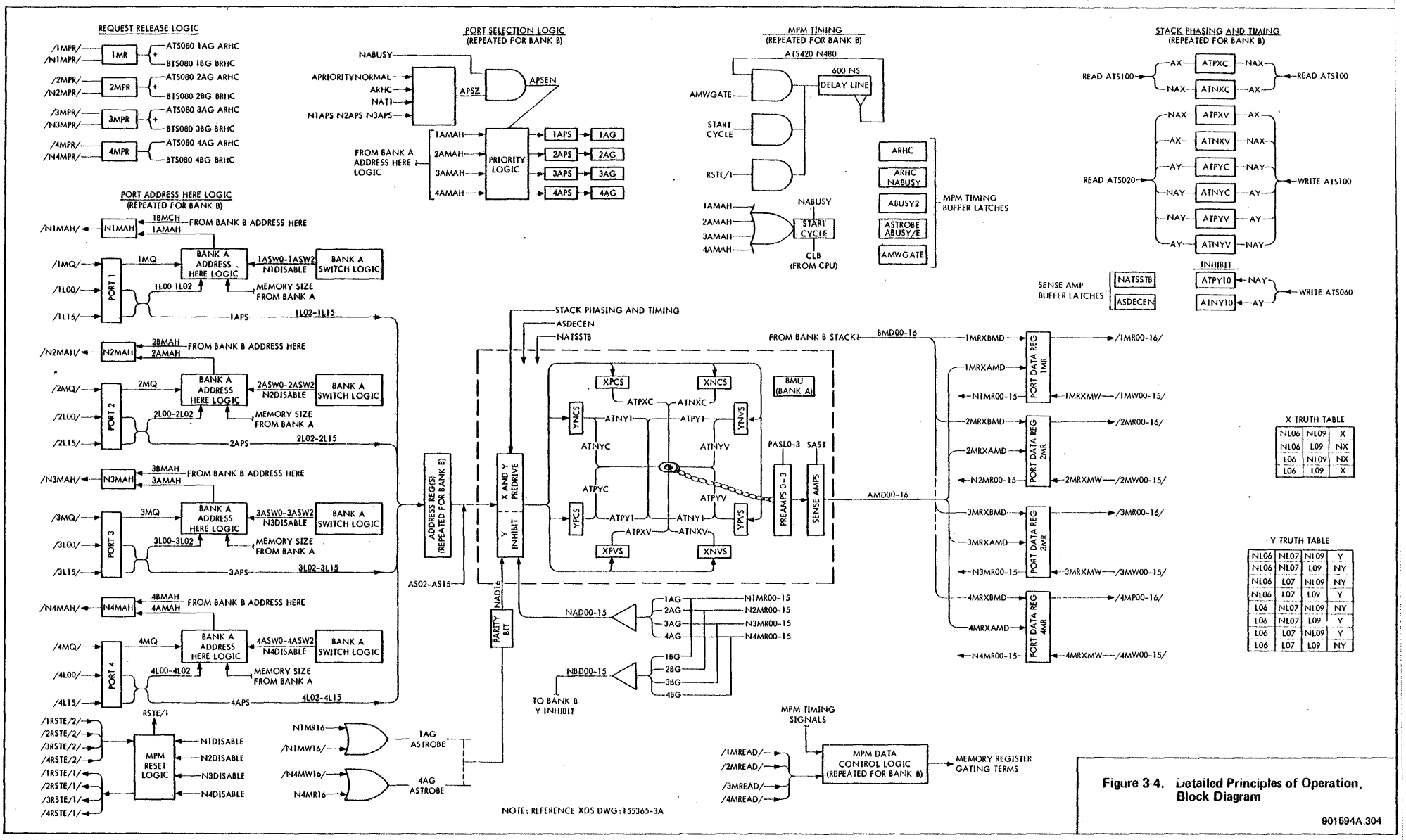


Figure 3-4. Detailed Principles of Operation, Block Diagram

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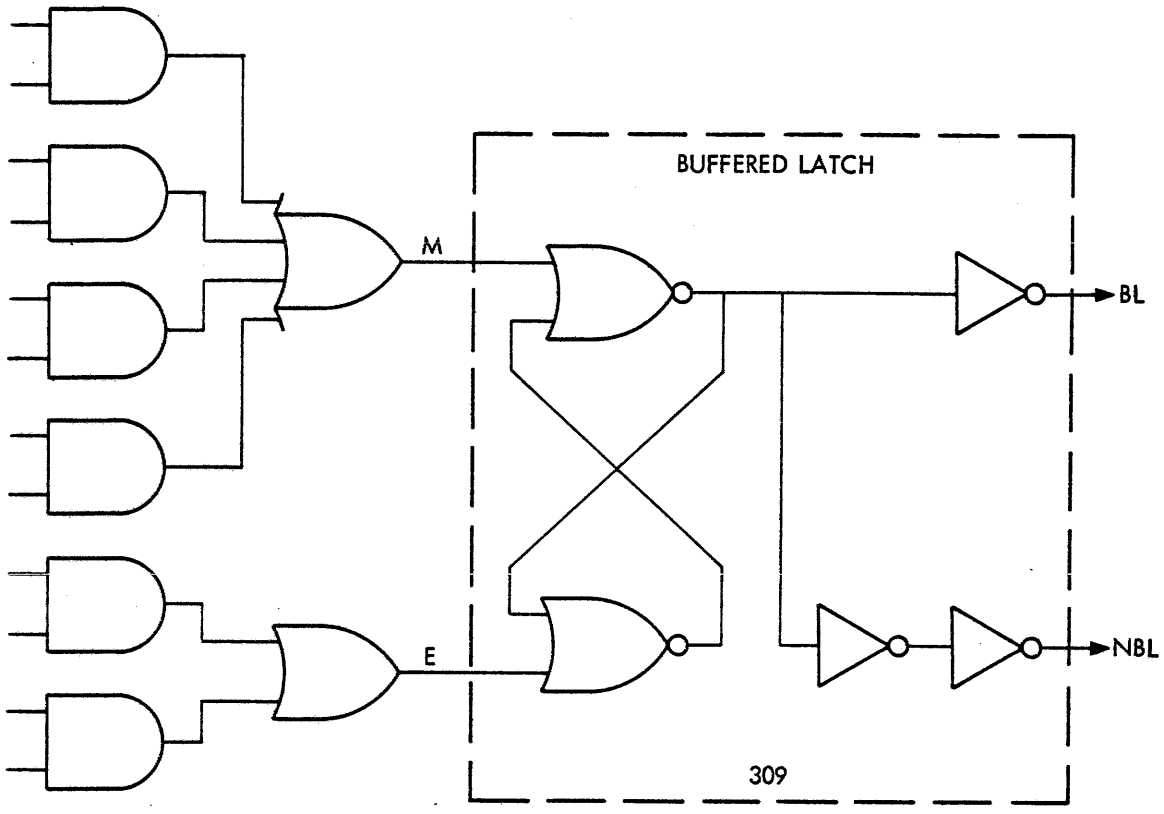
The major portion of the MPM logic is mechanized using the 309 buffered latch. Figure 3-5 includes a logic diagram showing the AND/OR input to a typical buffered latch and a general description of circuit operation. All registers, the major portion of the MPM timing and control logic and stack phasing (current direction) logic are mechanized using the 309 buffered latch.



CIRCUIT OPERATION: WHEN THE ERASE TERM (E) IS HIGH, BL FOLLOWS THE MARK (M) INPUT TERM AND NBL IS THE INVERSION OF BL. IF THE MARK (M) TERM IS LOW WHILE THE ERASE (E) TERM IS HIGH, OUTPUT BL IS LOW AND NBL IS HIGH. THEREAFTER, IF E GOES LOW WHILE M IS LOW, BL AND NBL REMAIN LOW AND HIGH, RESPECTIVELY. SUBSEQUENTLY, IF M GOES HIGH, OUTPUT BL GOES HIGH AND NBL IS LOW AND THIS OUTPUT REMAINS REGARDLESS OF CHANGES IN M, UNTIL E GOES HIGH AGAIN

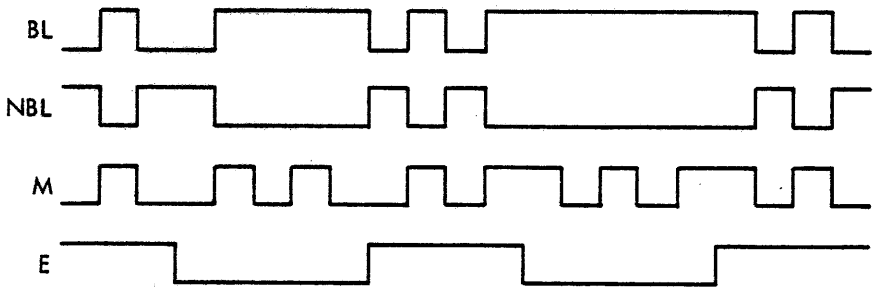


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Figure 3-5. Buffered Latch, 309

3-9 ADDRESS DECODE (PORT ADDRESS-HERE) LOGIC

Port address-here logic is implemented separately for each port and bank connected to an MPM so that any port can connect to any bank, independently. The logic descriptions for one port and one bank are identical for all ports and both banks, therefore, the following description covers port 1 connected to bank A.

The input to port address-here logic is as follows: (1) memory request /1MQ/ and the most significant address lines /1L00 - 1L02/ from the port user, (2) starting address information for each port from switch logic (1ASW0 - 1ASW2), (3) not-port disable (N1DISABLE) information from switch logic and (4) memory bank size information, 8K or not 8K (16K) from the BMU section.

Refer to figure 3-6. An ST14 module in position 08C provides the toggle switches for switch logic input to the address decode logic for bank A. Three switches, each, are provided for ports 1 and 2 for setting the starting address for each port for bank A of memory. Two switches are provided to disable port 1 or 2, if required. Table 3-1 provides a reference for switch designations and locations for a complete system of 4 ports and 2 banks.

Table 3-1. Port Address-Here Switch Designations and Locations

MPM 1 or 2	Port	Switch No. For Starting Address SW0	SW1	SW2	Switch No. For Port Disable	Module ST14 Location	Switch No. For Priority-Normal
Bank A	1	5	4	3	15	08C	2 on 08C
	2	9	8	6	1	08C	
	3	5	4	3	2	02C	
	4	9	8	6	15	02C	
Bank B	1	5	4	3	-	04C	14 on 08C
	2	9	8	6	-	04C	
	3	2	1	11	-	04C	
	4	15	14	12	-	04C	

Table 3-2. Port Address-Here Decoding

Memory Address Decimal	Memory Address Hexidecimal	Starting Address SW0	SW1	SW2	Bank Size Term A8K/B8K	L-Lines 0	1	2
0-8191	0000-1FFF	0	0	0	High	0	0	0
0-16383	0000-3FFF	0	0	0	Low	0	0	0
						or		
						0	0	1
8192-16383	2000-3FFF	0	0	1	Low	0	0	1
16384-24575	4000-5FFF	0	1	0	High	0	1	0
16384-32767	4000-7FFF	0	1	0	Low	0	1	0
						or		
						0	1	1
24576-32767	6000-7FFF	0	1	1	Low	0	1	1
32768-40959	8000-9FFF	1	0	0	High	1	0	0
32768-49151	8000-BFFF	1	0	0	Low	1	0	0
						or		
						1	0	1
40960-49151	A000-BFFF	1	0	1	Low	1	0	1
49152-57343	C000-DFFF	1	1	0	High	1	1	0
49152-65535	C000-FFFF	1	1	0	Low	1	1	0
						or		
						1	1	1
57344-65535	E000-FFFF	1	1	1	Low	1	1	1

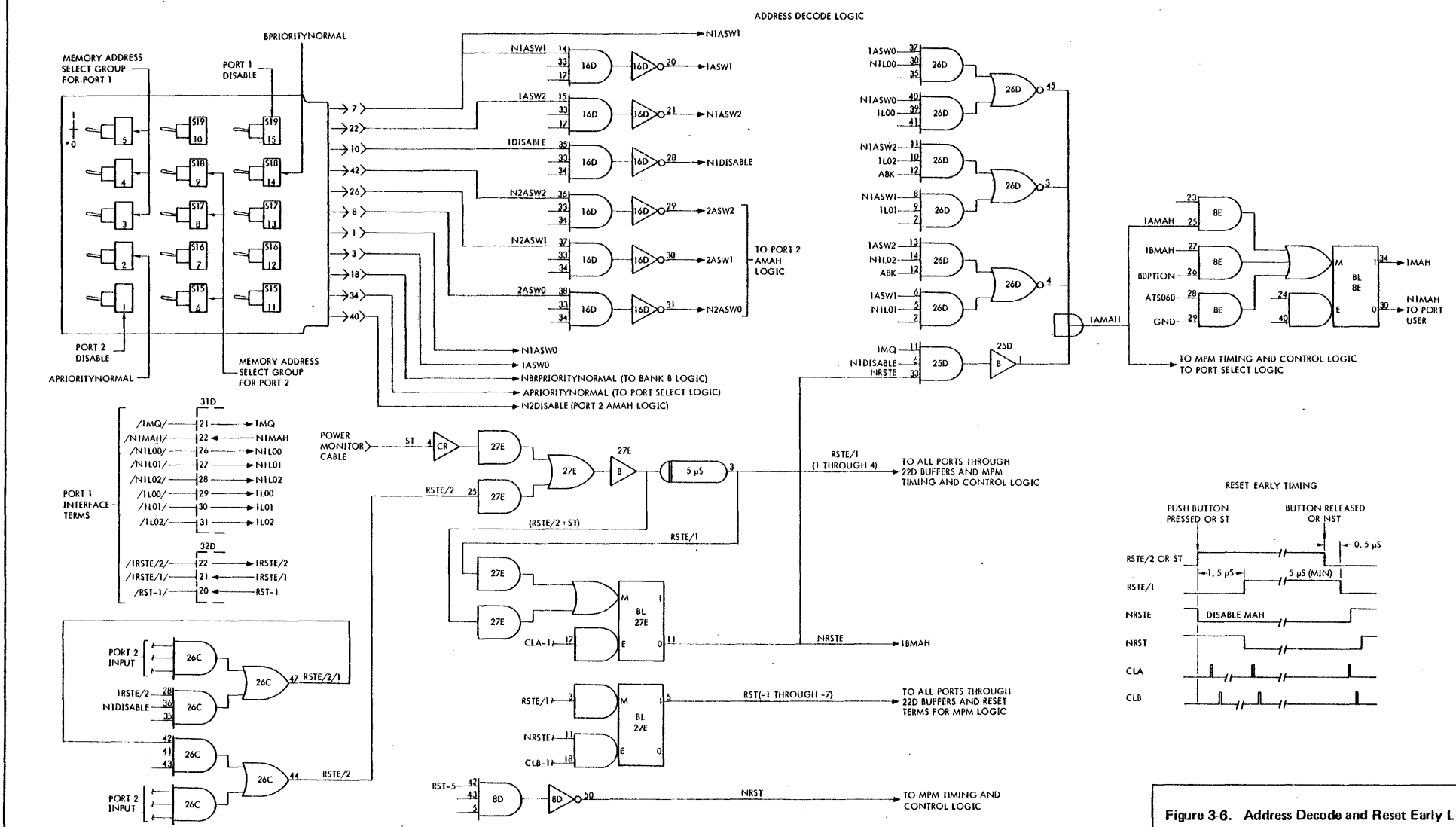

Figure 3-6. Address Decode and Reset Early Logic

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All input to the address decode portion of the port address-here logic must establish a false condition to have selected a legal address in bank A. Refer to table 3-2 showing the address-here decoding method. Table 3-2 is used in conjunction with figure 3-6, in the area showing module 26D/IT24.

The following is an example of conditions used to detemmine a legal address. Assume the following input to the address decoding logic: N1ASW0, N1ASW1 and N1ASW2 indicating a starting address of zero. The A8K term from the BMU is low (bank A contains a full 16K). The L-lines are N1LO0, N1LO1 and 1LO2. Under these conditions not one of the input AND conditions is satisfied, therefore the address is legal. However, if the A8K term is high indicating bank A has only 8K, the AND condition N1ASW2.1LO2.A8K is satisfied, therefore the address is illegal and 1AMAH is inhibited.

When the address decode has determined a legal address, the 1AMAH term can go high if there's a memory request, the port is not disabled and a reset-early has not been generated. The 1AMAH term is used as input to the memory-start cycle logic in memory timing and control logic and as input to the priority logic in the port selection logic.

The 1AMAH or 1BMAH term is selected as the 1MAH output to the port user through a buffered latch on 08E. The inversion of 1MAH is also sent to the port user.

3-10. RESET-EARLY LOGIC

Reset-early logic inhibits memory access and initializes all logic in the MPM section. The reset-early logic also provides signals to the port user to reset internal logic.

There are several donditions which could occur in the Sigma 3 Computer System operation which would cause reset-early (RSTE/1/ - /4) to go high. RSTE/2/1 - /4 is generated and reset-early is initiated when the RESET button on the PCP panel of the CPU is pressed or the automatic reset feature on the PCP panel is utilized, or a system reset is generated by users on ports 2, 3, or 4. Also if the power monitor system option has been included in the system the ST term from the monitor system will initiate an RSTE/1.

In any of the previously described conditions, the arrival of an RSTE/2 or an ST at the reset-early logic will initiate the following sequence of events (refer to reset-early timing diagram on figure 3-6:) RSTE/2 or ST is high at the input to reset-early logic and also to a 5 microsecond delay line in module 27E/AT63. After a 1.5 microsecond delay RSTE/1 goes high and remains high for a minimum of 5 microseconds or as long as RSTE/2 or ST remain high. RSTE/1/1 - /4 are used by the associated port user to control internal logic.

During the time RSTE/1 is high, NRSTE is low thereby inhibiting MAH for all ports. Also, during the time RSTE/1 is high, RST is high and lifts all latches on all MPM timing terms. RST-1 through 4 are used by the associated port user to reset internal logic. RST-5 holds NRST low; NRST is used to disable certain key timing signals (refer to equations at lines 0151300 and 0151800 in Section I of the ESM). With NRST low ARHC is not

generated, APS/E is high (refer to figure 3-9) and the latches are reset on all port select and memory address register logic as well as current phasing logic; also memory strobe signals are inhibited. RST-6 resets the latches on all port-to-memory gates (AG).

While RSTE/1 is high, at each clock B (approximately every 325 nanoseconds) the memory timing delay line is restarted (refer to figure 3-7). This recycling of the memory delay line is to insure all timing latches are initialized (the mark input low) when the erase term (RST) goes low again.

Within 500 nanoseconds after RSTE/2 or ST goes low, RSTE/1 is low. At the next clock A, NRSTE goes high, and at the following clock B, NRST goes high; when NRSTE is high the memory may be accessed again.

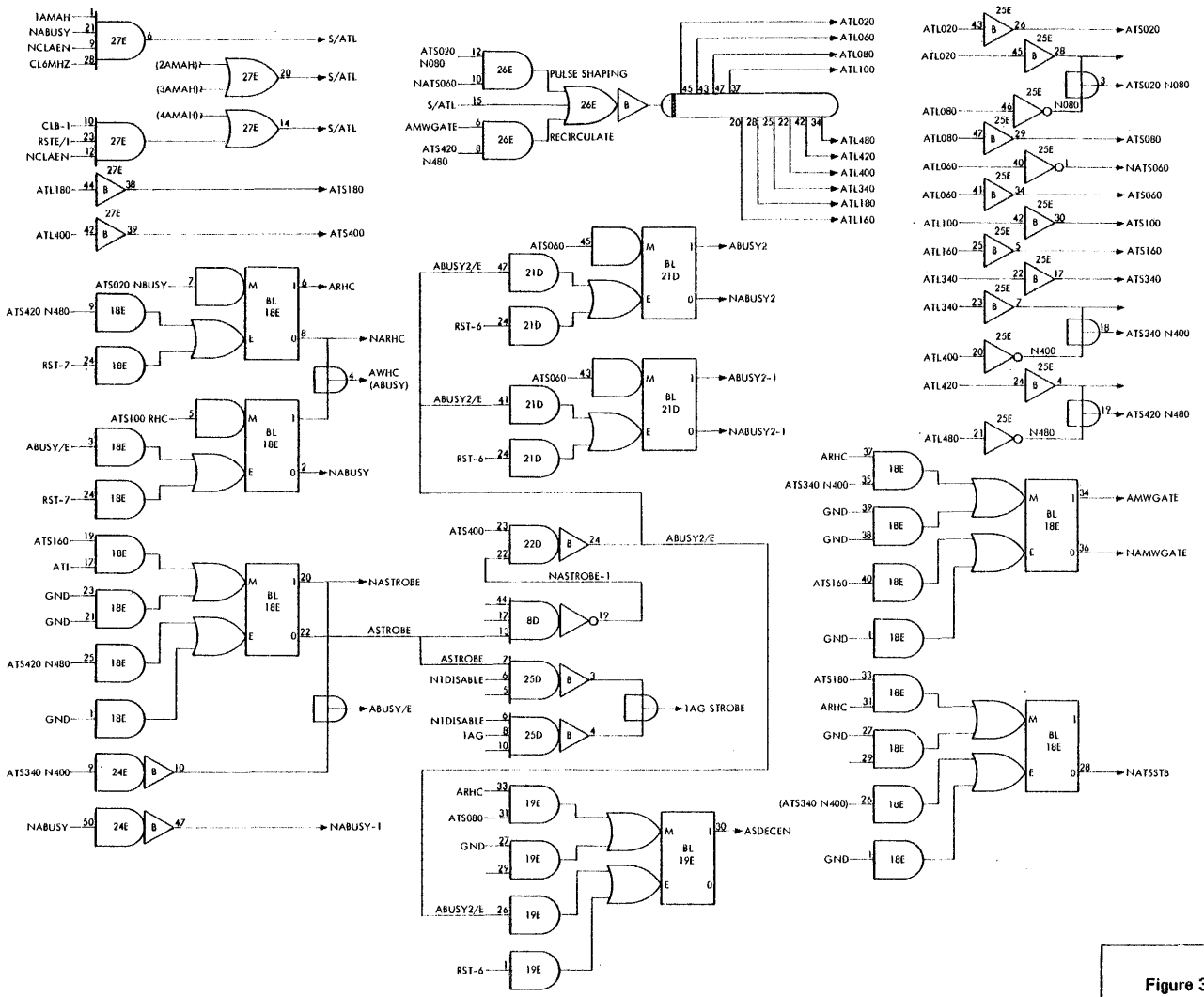

Figure 3-7. MPM Timing and Control Logic

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3-11. MPM TIMING AND CONTROL LOGIC

The MPM timing and control logic provides the overall synchronization for a memory cycle. The circuitry consists of a 600 nanosecond delay line, the delay line sensors and 309 buffered latches for control signal generation. The Sigma 3 MPM provides separate timing and control logic for each bank connected to an MPM.

The memory cycle is divided into two halves; the first half is the read half cycle, the last half, the write half cycle. The two half cycles are provided by recirculating the delay line at the end of the read half cycle. Each memory cycle always consists of a full read half cycle followed by a full write half cycle. There is no provision for a partial cycle.

The delay line is tapped at specific intervals (between ATL020 - ATL480) and these taps are sensed by delay-line sensors, the output of which (ATS020 - ATS420.N480) is applied to buffered latches. The buffered latches provide the MPM control terms.

Refer to figure 3-7 and 3-8. The memory timing sequence is as follows: The previous cycle ended with NABUSY latched high. If a legal address (AMAH) has been established in the port address-here logic, start-A-time line (S/ATL) will go high at the arrival of a clock B pulse and the delay line is started. The clock B pulse is derived from not-clock-A enable (NCLAEN) and the 6 MHz pulse,both from the CPU, and is used only to synchronize the beginning of each memory cycle. After the cycle has started, the memory timing and control is asynchronous.

Output ATS020.N080 from delay line sensors are returned to the input of the delay line to develop a theoretical delay line pulse width of 60 nanoseconds.

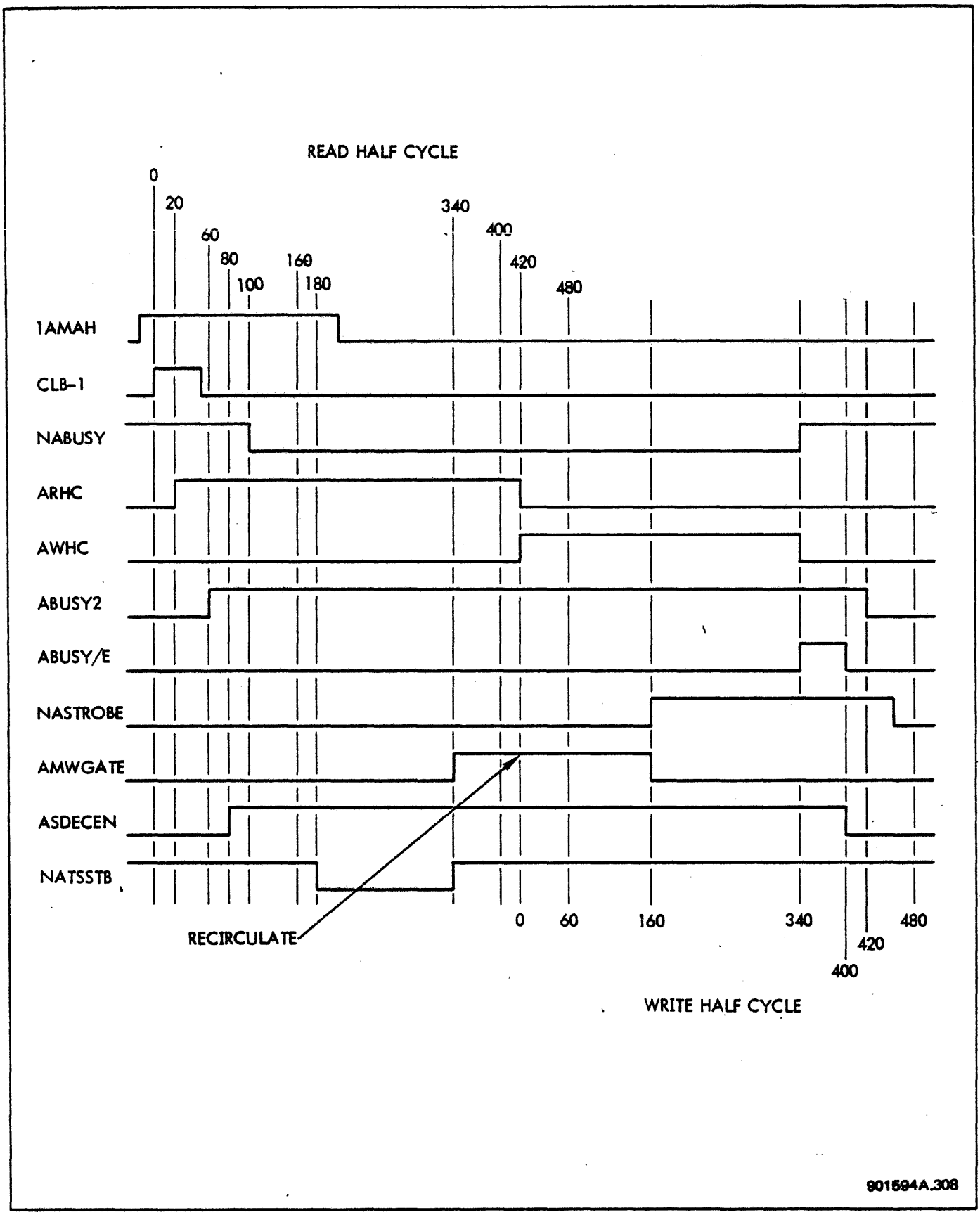

Figure 3-8. Control Signals Timing Diagram

In actual pratice, however, logic and other circuit delays will cause the delay line pulse width to range between 90 and 120 nanoseconds. The MPM timing diagram in Section II, drawing No. 155365, sheet 7, of the ESM is derived by taking this tolerance into consideration.

The read half cycle (ARHC) is actually started at ATS020; ARHC goes high when NRST.NABUSY.ATL020 (0151300) are all high and is latched high until ATS420 of the read cycle. ABUSY2 goes high at ATS060 of the read cycle and the inversion of this term (NABUSY2) is used to control the buffered latches in the port select and memory address register logic (figure 3-9). The term NABUSY2 enables the port-to-memory gate (AG) to enable the selected port to control the associated memory information register (MR), as well as latch the current direction (stack phasing) logic (figure 3-12).

At ATS080 of the read cycle sense-decode enable (ASDECEN) is high to enable the preamp select circuit in the BMU. At ATS100, NABUSY goes low causing the port-select enable (APSEN) term to go low inhibiting further port selection during the memory cycle (refer to port select logic paragraph 3-11.) At ATS180 in the read cycle, not-time-for sense strobe (NATSSTB) goes low to the strobe driver circuits in the BMU and, at a point between ATS180 and ATS340 data is strobed from the sense lines onto the AMD lines in the selected port memory information register (MR). With ASTROBE high at ATS420, 1AG.STROBE is high and data is gated to the selected port user if the read mode of operation was selected.

At (ATS420.NA80), NARHC goes high and pulls the write half cycle term (AWHC) high. The AWHC term is latched high with ABUSY/E held low by NASTROBE. Also at ATS420, with memory write gate (AMWGATE) previously latched high, the delay line is recirculated (starting at T zero); this is the start of

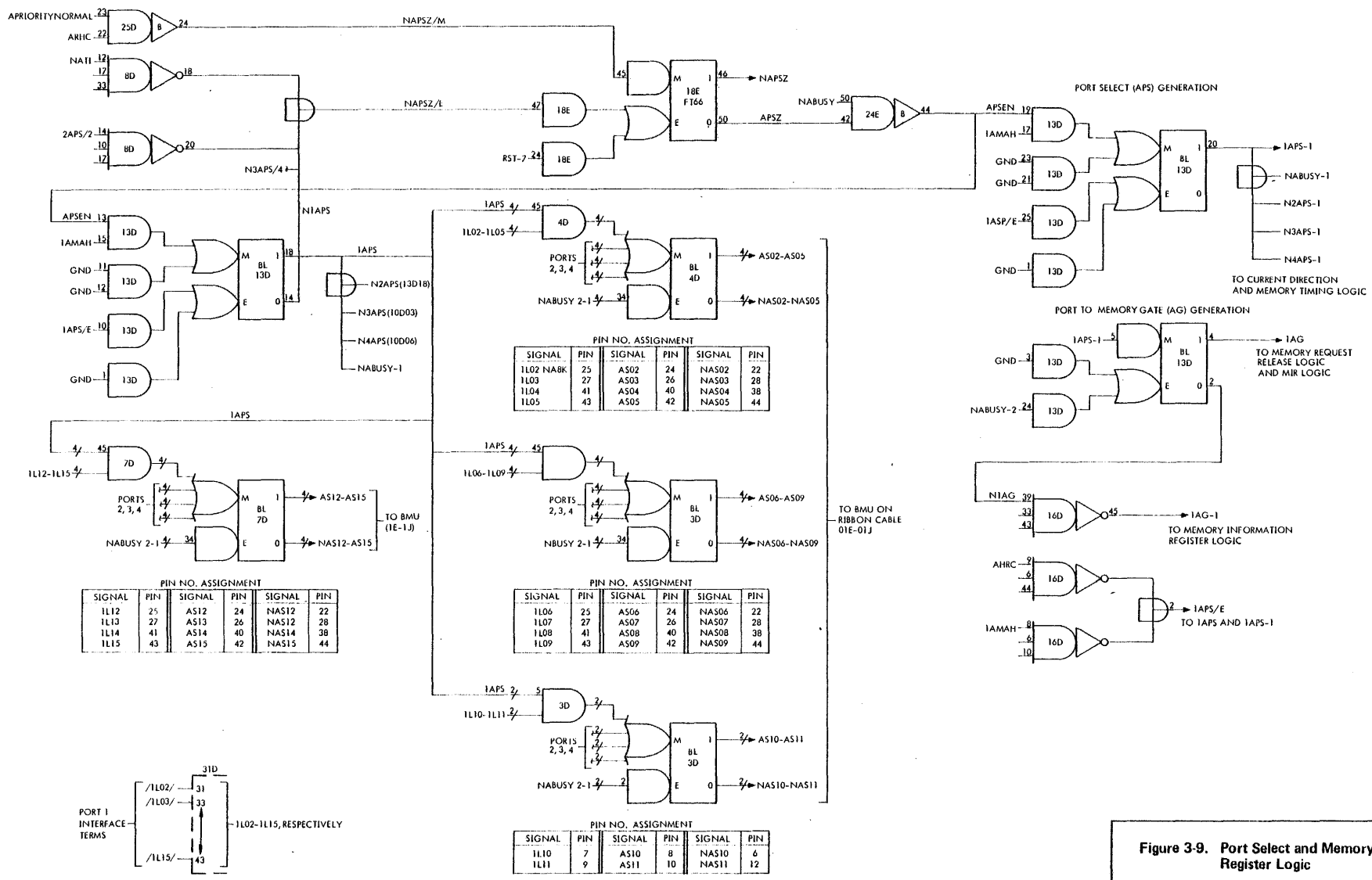

Figure 3-9. Port Select and Memory Address Register Logic

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the write half cycle. At this time, if the write mode of operation was selected, data from the port user (MW) is transferred to the MR.

At ATS160 in the write half cycle, NASTROBE goes high enabling ABUSY/E to go high at ATS340.NS400. When ABUSY/E goes high the latch is dropped on AWHC and NABUSY. With NABUSY high, a new memory cycle can be initiated.

A start-A-time delay line (S/ATL) can be generated when 1AMAH is inhibited during a reset-early (RSTE/1) sequence as described in paragraph 3-10.

3-12 PORT SELECTION AND MEMORY ADDRESS REGISTER LOGIC

It is possible that all four ports will present memory requests (MQ) simultaneously to the same bank and memory address-here conditions can be established for all ports. Since only one port may access memory at a time, the port selection logic is repeated for each bank connected to an MPM. The output of the port selection logic (APS and AG) are gating signals with the primary purpose to enable memory address and data transfers between the selected port and the correct bank.

Port priority is established in one of two modes depending on the position of the APRIORITY-NORMAL switch located on card 08C (refer to figure 3-6.)

3-13. APRIORITY-NORMAL True

In the true position (down) the APRIORITY-NORMAL toggle switch selects the port priority mode which effectively selects all ports, with an AMAH pending at one time, and connects each in a priority sequence until the lowest priority port has been serviced. In the event of two simultaneous requests, the lower priority will wait only a maximum of one full memory cycle

(in addition to the remaining portion of the current cycle, if any) after raising the memory request line.

Refer to figure 3-9, 3-10 and 3-11. At the end of a memory timing cycle, NAPSZ/E is low due to NATI (not-A-time inhibit) going high. NAPSZ is low since one of the conditions satisfying the mark input (ARHC) is low causing APSZ to be high. NABUSY was latched high near the end of the previous memory cycle and this condition allows the APSEN term (port-select-enable for bank A) to go high. Assume two address-here conditions are simultaneously met; 3AMAH and 4AMAH. Raising 4APS (0087300) depends on only APSEN, 4AMAH and NABUSY-1 to be high, therefore port 4 is serviced first and the L-lines (/4L02 - /4L15/) from port 4 are latched in the memory address register for bank A. At the same time the port-to-bank A memory gate (4AG) is latched high by NABUSY2 (low) and 3APS is held low by the inverted 4APS term (N4APS).

A memory cycle started with 4AMAH high and, at ATS020, ARHC goes high making the mark input to NAPSZ high, causing APSZ to drop low. When APSZ is low port-select enable (APSEN) is low and the start of another port priority sequence is inhibited during this memory cycle. At ATS100 the latch is dropped on NABUSY bringing term 4APS low; port 4 can change address lines in anticipation of the next request.

With 4AG and ARHC high, memory request release (4MRR) is high to the port user at ATS080 (figure 3-11). After the arrival of /4MRR/, the port user will drop the memory request (4 MQ) before the end of the read cycle (NRHC) at ATS420; dropping 4MQ will cause 4AMAH to drop. At ATS420 APS/E goes high to lift the latches on all port APS terms. However, only N4APS goes high since N1APS and N2APS are already high and N3APS/4 is latched low by 3APS/E; 3APS/E is held low by the 3AMAH term remaining high.

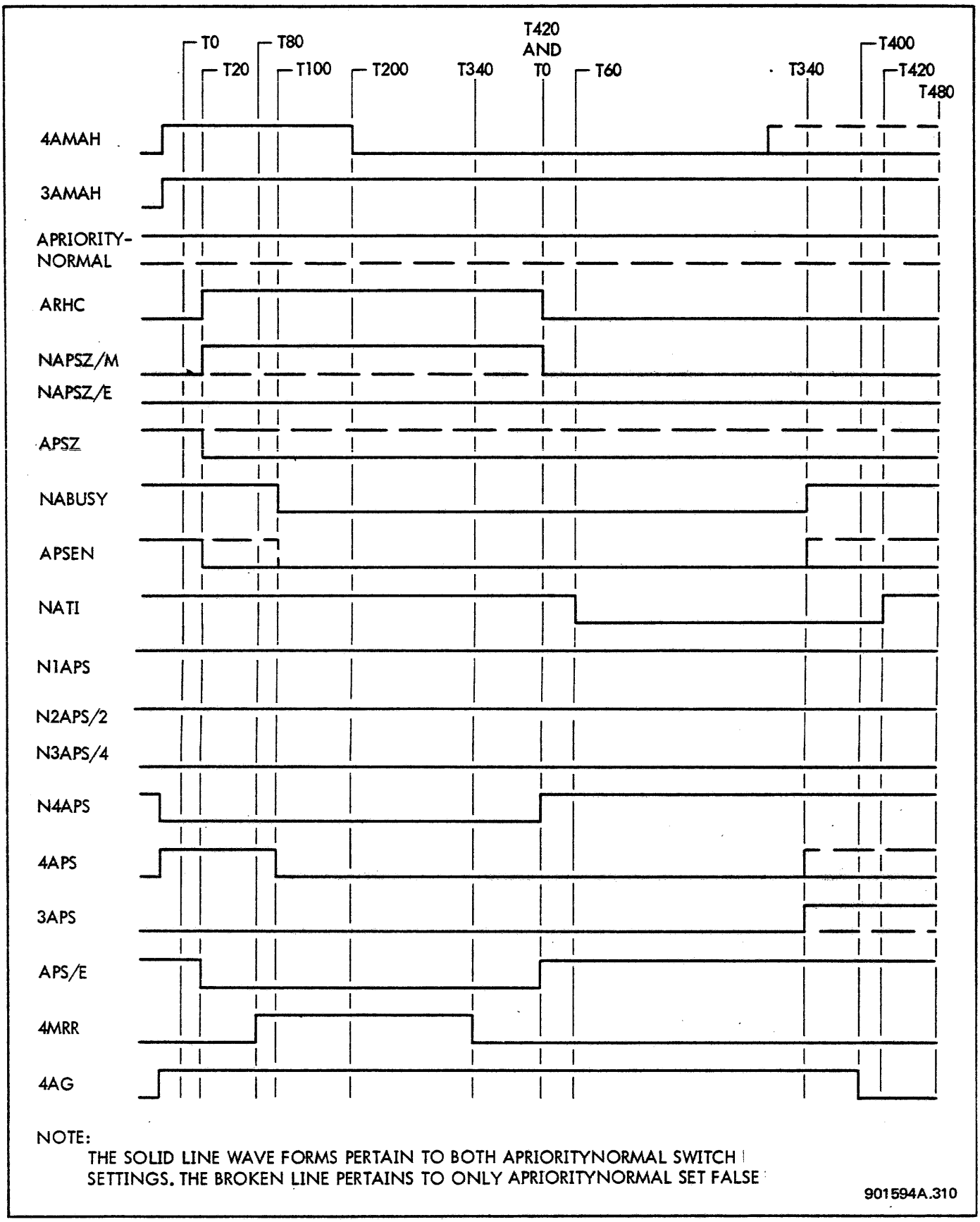


Figure 3-10. Port Selection Timing Diagram

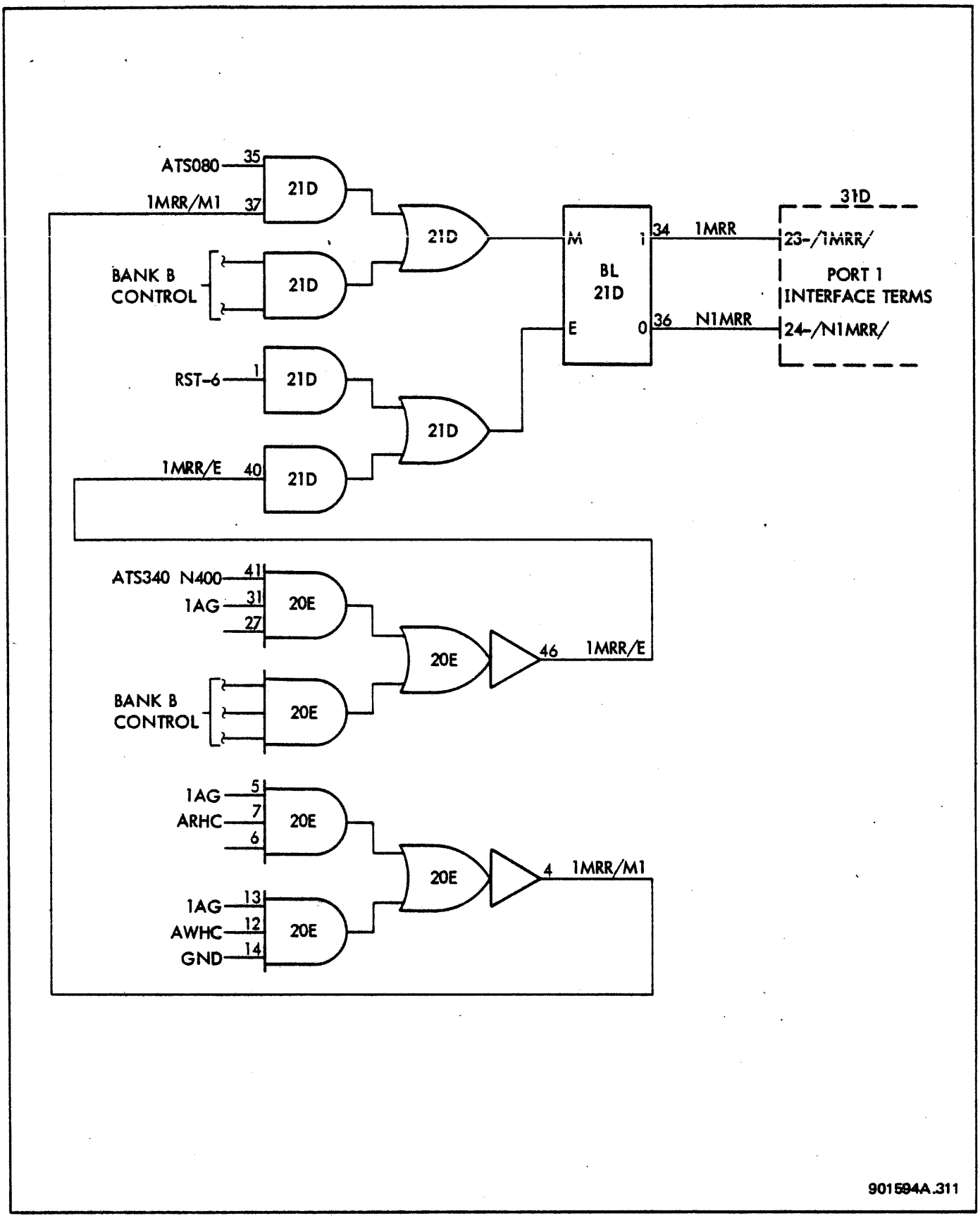


Figure 3-11. Memory Request Release Logic

When ARHC goes low at the end of the read cycle, the mark input to NAPSZ goes low. The NAPSZ reset term NAPSZ/E does not change state when NATI goes low at ATS060 of the write cycle due to N3APS/4; this condition keeps APSZ low which will keep APSEN disabled. With APSEN low, if port 4 tries another request during the current cycle, it will not be serviced. When NABUSY goes high at ATS340 in the write cycle, 3APS will go high and the address lines (AS02 - AS15) will reflect port 3 L-lines when NABUSY2 goes high at ATS400. Also, when NABUSY2 goes high the latch is lifted on 4AG, removing port 4 from memory and 3AG goes high connecting port 3 to memory.

The next memory cycle starts with the remaining 3AMAH still high; APSZ and APSEN are still low and with the port-select enable term low, port 4 is inhibited from service. After /3MRR/ is sent to port 3 at ATS080 of the read cycle, port 3 will cause 3AMAH to drop low before ARHC goes low at ATS420. With both 3AMAH and ARHC low, 3APS/E will go high, lifting the latch on N3APS/4. When NATI goes low at ATS060 in the write cycle, all conditions to satisfy NAPSZ/E will be met and APSZ will go high. With APSZ high when NABUSY goes high at ATS340, APSEN will go high allowing the initation of another port priority sequence.

3-~~13~~ 14. APRIORITY-NORMAL False

In the false position (up) APRIORITY-NORMAL toggle switch selects the priority mode which will service port requests in a straight priority sequence. Port 4 has the highest priority and port 1 the lowest. Multiple requests by a higher priority port will be permitted access to core. Using the same example set up in paragraph 3-12 for APRIORITY-NORMAL true, the detailed sequence of the port selection is as follows: Port 4 will be connected in

an identical manner as outlined in the second paragraph under paragraph 3-12. However, the condition met at ATS020 (ARHC) true) has no significance since APRIORITY-NORMAL is false. With NAPSZ/M and NAPSZ/E low, APSZ is latched high and stays high throughout the entire memory cycle. With APSZ high, a port request from a higher priority port is not inhibited during the current memory cycle.

The remaining steps in this priority sequence are the same as those outlined in APRIORITY-NORMAL true with the exception that at ATS340 of the write cycle, NABUSY goes high bringing APSEN high to enable a new port selection. If port 4 is able to request access to bank A again (4AMAH) prior to or simultaneously with NABUSY high at ATS340, port 4 will once again assume control of memory as described in the preceding paragraphs and 3APS term will be held low with N4APS. Port 3 will have to wait one (or more) memory cycle (s) to gain access to core.

3-15. Memory Address Register Logic

The basic MPM (assembly 149395) provides the memory address register (S) for memory bank A. When bank B (optional) is added and identical memory address register is provided for bank B. The S-register is a 14-bit register which temporarily stores the memory address during the memory cycle.

Refer to figure 3-9. The memory address register for bank A is contained on FT68/FT83 modules in positions 03, 04 and 07 in chassis D. The FT68/FT83 modules contain 309 buffered latches; these latches form the S-register.

When a port (or ports) raise a memory request, the L-lines (L02 - L15) from the port are present at the input gates of the memory address register. When the port selection logic determines which port will access memory, the

associated APS term gates the L-lines to the BMU on the ribbon cable assembly from O1E in the MPM to O1J in the BMU.

With NABUSY2-1 high during T0 to T60, the BL output (AS02 - AS15) to the BMU follows the mark input (high or low) and the NBL (NAS02 - NAS15) is the inversion of the BL output. At ATS060 of the read cycle NABUSY2-1 goes low and the address terms are latched and will remain stable until NABUSY2-1 goes high at ATS400 of the write cycle. At this time, if changes have been made in the L-lines and the associated port APS term is high, the output will reflect these changes in the memory address to the BMU.

3-16 STACK PHASING (CURRENT DIRECTION) AND TIMING LOGIC

The stack phasing and timing logic developes signals which determine the direction of current through the X and Y-drivelines in order to produce coincident current at the addressed core. When current direction is determined, timing signals are developed at the beginning of the read and write half cycles. These timing signals are applied to the X and Y-driveline circuitry in the BMU to turnon positive and/or negative current and voltage switches. The same Y-driveline current direction signals are also applied to circuits in the stack phasing and timing logic during the write half cycle, to establish the time to inhibit the writing of a logic one (write a zero instead). These signals are transferred to the positive and negative Y-current inhibit circuits in the BMU.

Current direction is determined by the decoding of the logic levels of 3 L-bits from the port user, bits 6, 7, and 9. The X and Y truth tables on figure 3-4 list the possible combinations of these bits and the resulting selection of AX and AY.

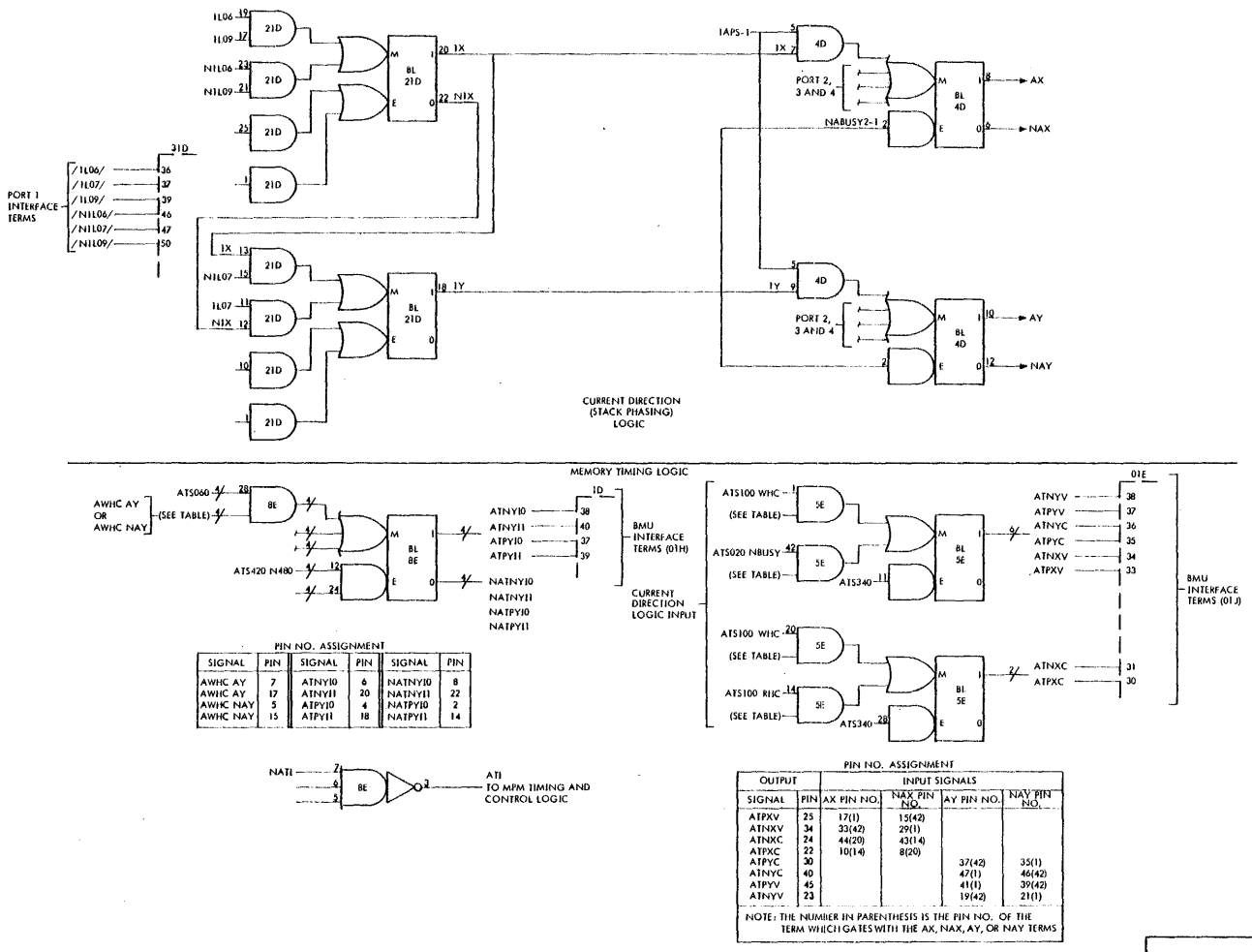
Refer to figure 3-12. On the read half cycle, time-for-positive Y-current and time-for-negative Y-voltage (ATPYC and ATNYV), time-for negative Y-current and time-for-positive Y-voltage (ATNYC and ATPYV), and time-for-negative or positive X-voltage (ATNXV or ATPXV)are enabled by ATS020.NBUSY. Only time-for-negative or positive X-current (ATNXC or ATPXC) are established at ATS100 of the read cycle. This is to prevent excessive noise in the stack drivelines which might result if both X and Y-drivelines were pulsed at the same time. Excessive noise could result in erroneous signals on the sense lines. On the

write half cycle, however, (when sense lines are not used) all the above signals are developed at ATS100.

An example to determine the resultant timing signals for L-lines 6, 7, and 9 from port 1, is as follows: Without the use of the truth tables, assume a bit configuration of 1L06.N1L07.1L09 (101). Terms 1L06 and 1L09 satisfy the mark input to 1X. Term 1X is high and 1APS-1 from port selection logic gates the resultant AX to the timing signal circuits. The output 1X is fed back to the 1Y buffered latch and ANDS with N1L07 to satisfy the mark input to 1Y. Term 1Y is high and 1APS-1 from port selection logic gates the resultant AY to the timing signal circuits.

Refering to the table for X and Y timing signal pin numbers, the second column (AX pin number) shows that during the read cycle with ATS020.NBUSY on pin 42 AND with AX on pin 33 the resultant output is ATNXV on pin 34. Also with ATS100.RHC on pin 14 AND with AX on pin 10 the result is ATPXC on pin 22. The forth column (AY pin No.) shows that during the same read cycle with ATS020.NBUSY on pin 42 and AY on pin 37 the result is ATPYC on pin 30; and with AY on pin 19 the result is ATNYV on pin 23. With ATS340 low at this time, all read timing signals are latched until ATS340 goes high near the end of the read cycle. Obviously, timing signals are ganerated in pairs; if the result is ATPYC (positive Y-current) there must be ATNYV (negative Y-voltage) to enable the circuits which control the correct pair of switches for a selected Y-driveline. At ATS340 of the read cycle the latches are dropped on the read timing signals.

When the memory cycle recirculates to the write half cycle the polarity of the current and voltage timing signals are reversed. Refer again to the table of



PIN NO. ASSIGNMENT

SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN
AWHC AY	7	ATNY10	6	NATNY10	8
AWHC AY	17	ATNY11	20	NATNY11	22
AWHC NAY	5	ATPY10	4	NATPY10	2
AWHC NAY	15	ATPY11	18	NATPY11	14

PIN NO. ASSIGNMENT

OUTPUT		INPUT SIGNALS			
SIGNAL	PIN	AX PIN NO.	NAX PIN NO.	AY PIN NO.	NAY PIN NO.
ATPXV	25	17(1)	15(42)		
ATNXV	34	33(42)	29(1)		
ATNXC	24	44(20)	43(14)		
ATPXC	22	10(14)	8(20)		
ATPYC	30			37(42)	35(1)
ATNYC	40			47(1)	46(42)
ATPYV	45			41(1)	39(42)
ATNYV	23			19(42)	21(1)

NOTE: THE NUMBER IN PARENTHESIS IS THE PIN NO. OF THE TERM WHICH GATES WITH THE AX, NAX, AY, OR NAY TERMS

Figure 3-12. Current Direction (Stack Phasing) and Memory Timing Logic

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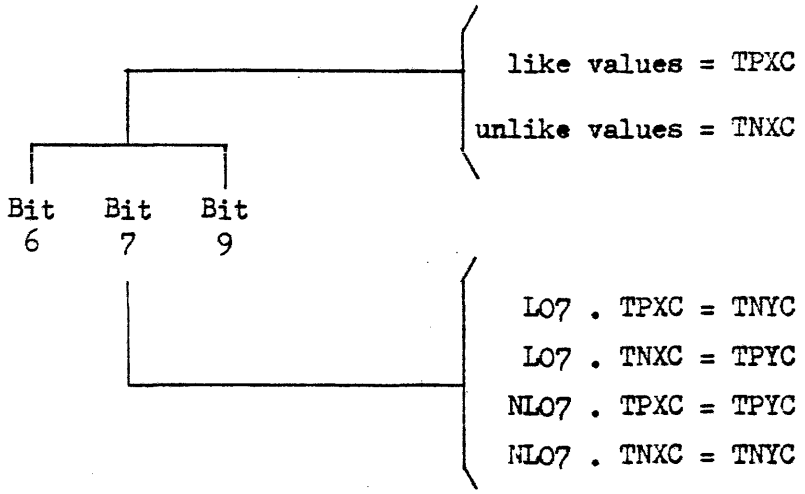
timing signal pin numbers. During the write cycle with ATS100.WHC on pin 1 and AX on pin 17 the result is ATPXV on pin 25. With ATS100.WHC on pin 20 and AX on pin 44 the result is ATNXC on pin 24. Also with ATS100.WHC on pin 1 and AY on pin 47 the result is ATNYC on pin 40; and withAY on pin 41 the result is ATPYV on pin 45. At ATS340 of the write cycle the latches are dropped on the write timing signals.

Another method to determine the timing signals is to scan the 3 L-bits as follows:



Bit 7 determines the Y-current direction in relation to the X-current direction. If LO7 is high the Y-current is the opposite polarity of the X-current. If LO7 is low (NLO7) the Y-current is in the same direction as the X-current.

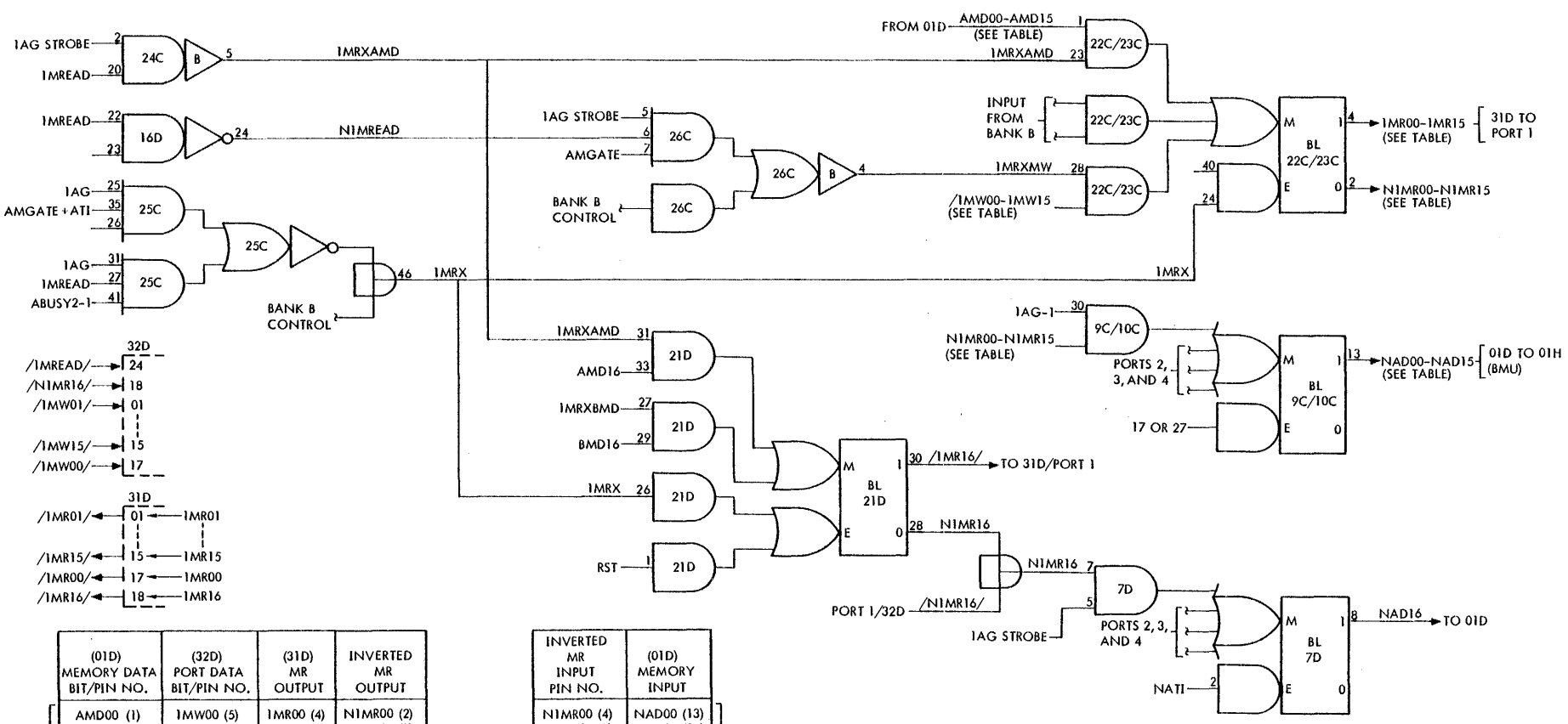
The time-for-negative or positive inhibit (ATNYI or ATPYI) is determined at ATS060 of the write cycle. These timing terms are written with the last character as a 1 or 0. The term ATNYI0 is used with bit planes zero through 7 and ATNYI1 is used with bit planes 8 through 16. Refer to the table of inhibit timing signal pin numbers and with ATS060 on pin 28 and AWHC.AY on pin 7 the result is ATNYI0 on pin 6 and ATNYI1 on pin 17. According to this result, time-for negative Y-inhibit (ATNYI) is high during the write cycle. Since negative Y-current (ATNYC) was selected for the write cycle it is essential that the Y-current is inhibited if the data to be written in core is a zero.

3-17. MEMORY INFORMATION REGISTER LOGIC

The basic MPM (assembly 149395) provides the memory information register logic for port 1. When ports 2, 3, or 4 (optional) are added, identical logic is provided for each port. Refer to figure 3-13. The memory information register (MR) is a 16-bit register which temporarily stores data going to and from a port during a memory cycle. Additional logic is provided to develop the required signals for the transfer of data to and from the MR.

At a point between ATS180 and ATS340 of the read cycle, data is strobed from core onto the AMD00-AMD15 lines via the 01H to 01D ribbon cable assembly. At the beginning of the memory cycle, if the mode control signal, memory-read (1MREAD) is high from the port user, the transfer-memory-data to the MR (1MRXAMD) is developed at ATS420 and is used to gate the memory data lines to the port user on the ribbon cable assembly 31D to port 1. The BL output (1MR00-1MR16) follows the mark input (AMD00-AMD16) and the NBL output (N1MR00-N1MR16) is the inversion of the mark input. These output levels are latched since the MRX term is low at ATS060 of the read cycle through ATS420 of the write half cycle. The MR output cannot follow a change (if any) in the mark input when MRX is low.

At the same time the memory data lines are transferred to the port user on 31D, the inversion of data (NAD00-NAD16) is gated by 1AG-1 from the port selection logic back (restored) to memory via ribbon cable assembly 01D to 01H. The NAD00-NAD16 buffered latches are wired to perform only as buffers, not as latches for temporary storage. The inversion of data, plus the proper timing pulse (TN/PYI), control the Y-current inhibit switches which control the writing into memory. Also at ATS420 the term MRX goes high lifting the latches on the MR; this action clears the register for the next input.



SLOT	(01D) MEMORY DATA BIT/PIN NO.	(32D) PORT DATA BIT/PIN NO.	(31D) MR OUTPUT	INVERTED MR OUTPUT
22C	AMD00 (1)	1MW00 (5)	1MR00 (4)	N1MR00 (2)
	AMD01 (10)	1MW01 (7)	1MR01 (6)	N1MR02 (8)
	AMD02 (11)	1MW02 (15)	1MR02 (18)	N1MR03 (14)
	AMD03 (21)	1MW03 (17)	1MR03 (20)	N1MR04 (22)
	AMD04 (25)	1MW04 (29)	1MR04 (34)	N1MR05 (30)
	AMD05 (35)	1MW05 (31)	1MR05 (36)	N1MR06 (38)
	AMD06 (37)	1MW06 (41)	1MR06 (44)	N1MR07 (42)
	AMD07 (50)	1MW07 (43)	1MR07 (46)	N1MR08 (47)
23C	AMD08 (1)	1MW08 (5)	1MR08 (4)	N1MR08 (2)
	AMD09 (10)	1MW09 (7)	1MR09 (6)	N1MR09 (8)
	AMD10 (11)	1MW10 (15)	1MR10 (18)	N1MR10 (14)
	AMD11 (21)	1MW11 (17)	1MR11 (20)	N1MR11 (22)
	AMD12 (25)	1MW12 (29)	1MR12 (34)	N1MR12 (30)
	AMD13 (35)	1MW13 (31)	1MR13 (36)	N1MR13 (38)
	AMD14 (37)	1MW14 (41)	1MR14 (44)	N1MR14 (42)
	AMD15 (50)	1MW15 (43)	1MR15 (46)	N1MR15 (47)

INVERTED MR INPUT PIN NO.	(01D) MEMORY INPUT	
N1MR00 (4)	NAD00 (13)	9C
N1MR01 (7)	NAD01 (14)	
N1MR02 (6)	NAD02 (15)	
N1MR03 (19)	NAD03 (18)	
N1MR04 (26)	NAD04 (33)	
N1MR05 (42)	NAD05 (35)	
N1MR06 (41)	NAD06 (34)	
N1MR07 (45)	NAD07 (37)	
N1MR08 (4)	NAD08 (13)	10C
N1MR09 (7)	NAD09 (14)	
N1MR10 (6)	NAD10 (15)	
N1MR11 (19)	NAD11 (18)	
N1MR12 (26)	NAD12 (33)	
N1MR13 (42)	NAD13 (35)	
N1MR14 (41)	NAD14 (34)	
N1MR15 (45)	NAD15 (37)	

Figure 3-13. Memory Information Register and Parity Bit Strobe Logic

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At the beginning of the memory cycle, if the mode control (1MREAD) from the port user is low, the signal is inverted (N1MREAD) to indicate the write mode and transfer-memory-write-data to the MR (1MRXMW) is developed at ATS420 of the read cycle; this term is used to gate the memory-write lines (1MW00-1MW15) from the port user on 32D. (Gating data from memory was inhibited during the read half cycle because 1MREAD was low.)

The NBL output (N1MR00-N1MR15) is the inversion of the mark input (1MW00-1MW15) and these data are applied to the AND gate input to the NAD00-NAD15 buffers to memory. Data is written into memory in the same manner described in the third paragraph under 3-16 covering the restore-function of the logic.

3-18. PARITY BIT STROBE LOGIC

The parity bit is generated by the port user and stored in the 17th bit position of a memory word on a separate data line. When a word is read from memory the parity bit is transfered out to the port user on a separate data line. Since the data must be assembled to generate or check a parity the parity bit lags the data. Therefore, a separate latch and gating circuit is provided to transfer this bit.

Refer to figure 3-13. During the read half cycle, the parity bit from memory (AMD16) is gated by the same transfer signal (1MRXAMD) to the port user on ribbon cable 31D to port 1. The BL and NBL output is latched by MRX in the same manner as the associated word from memory, paragraph 3-16. To restore the parity bit in memory the NBL output (N1MR16) is gated back into memory by 1AG.STROBE at ATS420 of the read cycle.

The parity bit from the user is written into memory in the same manner as the restored parity bit.

3-19. BASIC MEMORY UNIT (BMU) - ASSEMBLY NO. 148418

Basic Memory Unit Assembly 148418 provides the chassis (2-high) and hardware required to support the core and logic for a full bank of 16K. However, only the core and logic for 0-8K is included. When memory expansion kit assembly 149668 (optional) is utilized the BMU provides the storage for a maximum of 16K. A Basic Memory Unit Assembly 148418 for bank A is always located in 2-high chassis H/J. A BMU for bank B (optional) is located in 2-high chassis F/G. Both banks are identical in operation and hardware except for the airflow sensor and power supply control, which is located only in bank A. Therefore, only the BMU in bank A is described in the following paragraphs. A fully expanded BMU contains eight core diode modules for data storage and 14 modules containing X and Y-driveline and inhibit logic, core sense line logic and a module of miscellaneous logic. Refer to the module location chart in Section II, sheet 1 of BMU logic diagrams in ESM 902401.

3-20. CORE DIODE MODULES FTT13 AND FTT14

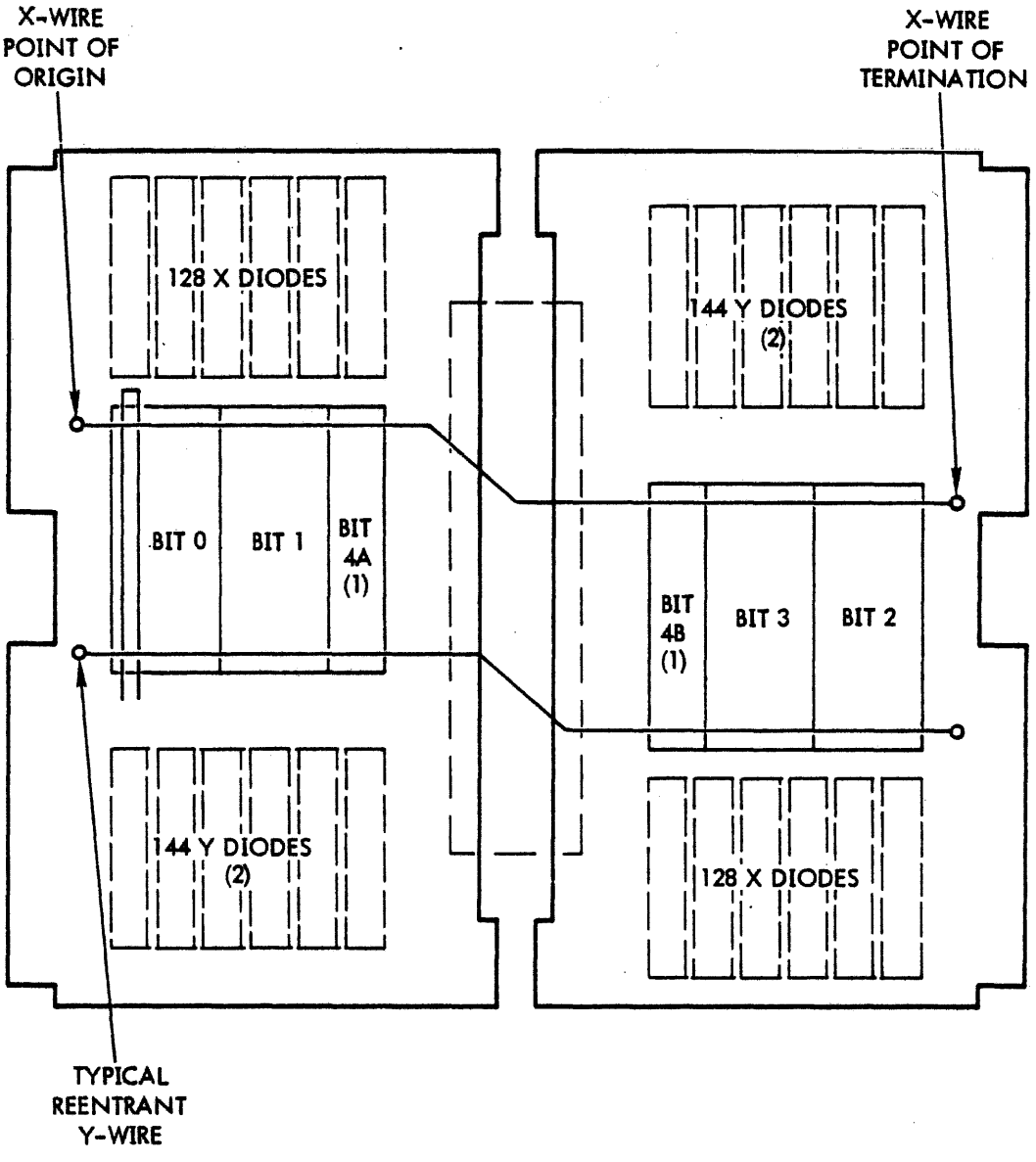
Two each of FTT13 and FTT14 core diode modules (4) provide 0-8K storage for a 16-bit word plus parity. The modules are located in slots 32/31, 28/27, 24/23, and 20/19. The core diode portion of the optional memory expansion kit for 8-16K is an additional set of FTT13 and FTT14 core diode modules occupying slots 30/29, 26/25, 22/21, and 18/17. Two FTT13 core diode modules (4 bit planes each) supply the storage area for the first eight bits of the 17-bit word and are designated 1/2-byte 0 and 1 or byte 0. Two FTT14 core diode modules (4½ bit planes each) supply the storage area for the remaining eight bits plus parity of the 17-bit word and are designated 1/2-byte 2 and 3 or byte 1 and parity. The Sigma 3 word organization is as follows:

Bits	0-3	4-7	8-11	12-15	P
½ Byte	0	1	2	3	
Byte	0		1		
Parity					X

Figure 3-14 provides the core diode module layout for both the four and four and one-half bit configurations. The Sigma 3 Core Memory emplays a 2½D organization or a 3-wire (X, Y, and sense) memory system. The Y-wire is common to both

core driving and inhibiting. As shown in figure 3-14, the X-wire begins at one side of the 4½-bit array and terminates at the other side. However, the Y-wire loops and reenters the Y-plane before the Y-line is terminated. The sense lines are not shown to avoid the confusion of additional lines. The sense lines are described in paragraph 3-30.

Drive current through both the X and Y lines is applied through a pair of bi-directional diodes that gate current direction. There are a total of 128 X-lines per 4 or 4½-bit array requiring 256 diodes and there are 288 (or 256) diodes feeding 144 (or 128) Y-line loops, 32 loops per bit plane (64 Y-lines) and 16 loops per 1/2-bit plane. Each bit plane, therefore is an X-Y matrix of 128 x 64 cores or 8192. and the ½-bit is equal to 4,096 cores.



NOTES:

1. NOT PRESENT ON 8K x 4 BIT CDM
2. 128 Y DIODES ON 8K x 4 BIT CDM
3. 8K x 4 BITS PLUS 4K x 1 BIT = 8K x 4 1/2 BITS

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Figure 3-14. 8K x 4 1/2 Bits - Core Diode Module Layout

The core diode modules are driven by external X and Y driveline and Y-inhibit logic and sensed by memory core sensing and preamp logic contained on 2-high, single modules located in the remaining positions shown on the BMU module location chart in the associated ESM.

3-21. MAGNETIC CORE

Since the magnetic core is the basic element in the forming of a core memory the following is a description of the properties of the magnetic core and how these properties function to provide the required capability of computer memory. Knowledge of the theory of magnetism and the hysteresis effect produced in magnetic materials are prerequisite to understanding the following information.

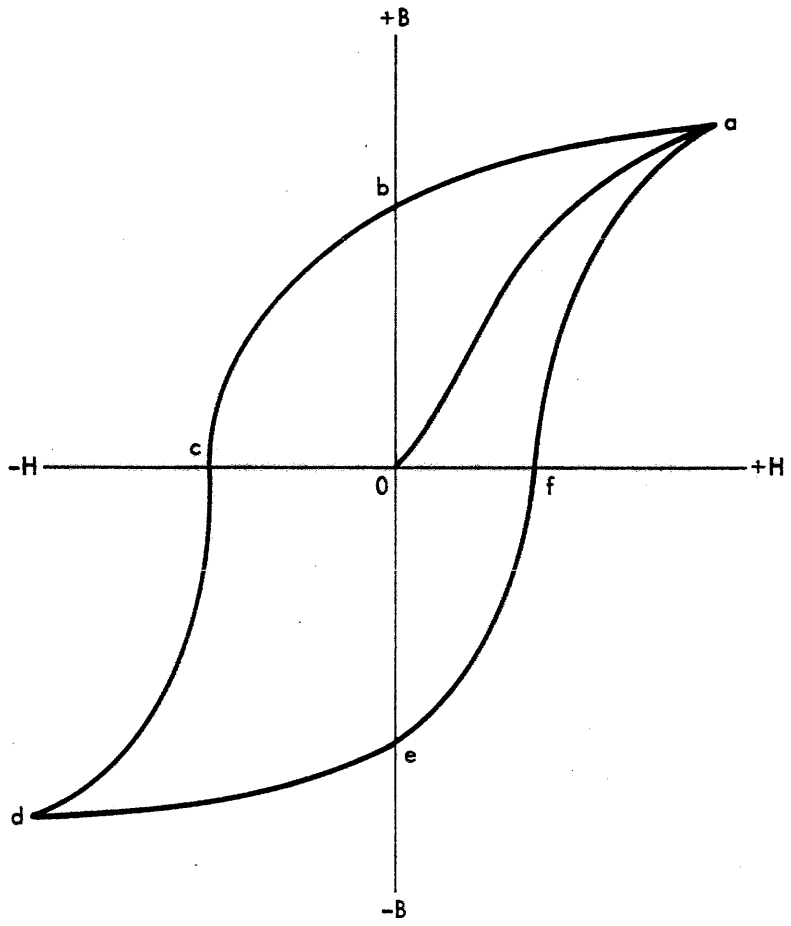
Figure 3-16, Hysteresis Loop (typical ferromagnetic material) is a graphic explanation of the effect of a magnetizing force on an iron core within the field of the magnetizing force. Curves a-b and d-e illustrate that the flux density of the iron core does not become zero each time the magnetizing force is removed. A coercive force (one in the reverse direction of the original force) is necessary to reduce it to zero. This lagging of the magnetic flux behind the magnetizing force which produces it, is hysteresis, or the internal resistance to change.

It is known that the energy loss due to hysteresis is proportional to the area of the hysteresis loop. For this reason the material for cores in the con-

struction of electromagnets and transformers has a hysteresis loop with a very small area. The distance c-f must be relatively small, preferably a loop which is nearly a straight line. In contrast, the hysteresis effect is exploited in the design of the magnetic core used in a computer memory.

The magnetic core of the basic memory unit is contructed of a special ferrite powdered material which broadens the c-f distance considerably. This material retains most of the magnetism once departed, as shown by the almost square hysteresis loop developed in firuge 3-16. The remanent flux density is almost equal to the maximum flux density at saturation. As a result, variations in the field intensity less than a critical switching value have pratically no effect on the flux density, while a change in H, greater than the critical value, abruptly reverses the magnetization of the core material.

Because of the square-loop effect, magnetic cores in the basic memory unit are always in one of two stable states, either near positive saturation or near negative saturation, indicating one of two binary states similiar to the flip-flop circuit. Unlike the flip-flop, there is no way to determine



-H TO +H = EXTERNAL MAGNETIZING FIELD

-B TO +B = INDUCED FLUX DENSITY FIELD

0 - a = INCREASE IN FLUX DENSITY VERSUS INCREASE IN MAGNETIZING FORCE ON UNMAGNETIZED MATERIAL (THIS CURVE IS NEVER REPEATED)

a = MAGNETIC SATURATION POINT

a - b = DECREASE OF FLUX DENSITY AFTER REMOVAL OF MAGNETIZING FORCE

b - 0 = REMANENT FLUX DENSITY

0 - c = COERCIVE FORCE (REVERSED MAGNETIZING FORCE) CAUSING FLUX DENSITY TO RETURN TO ZERO

c - d = MAGNETIZATION IN OPPOSITE DIRECTION DUE TO INCREASE IN MAGNETIZING FORCE

d - e = a - b

e - 0 = b - 0

0 - f = 0 - c

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Figure 3-15. Hysteresis Loop (Typical Ferromagnetic Material)

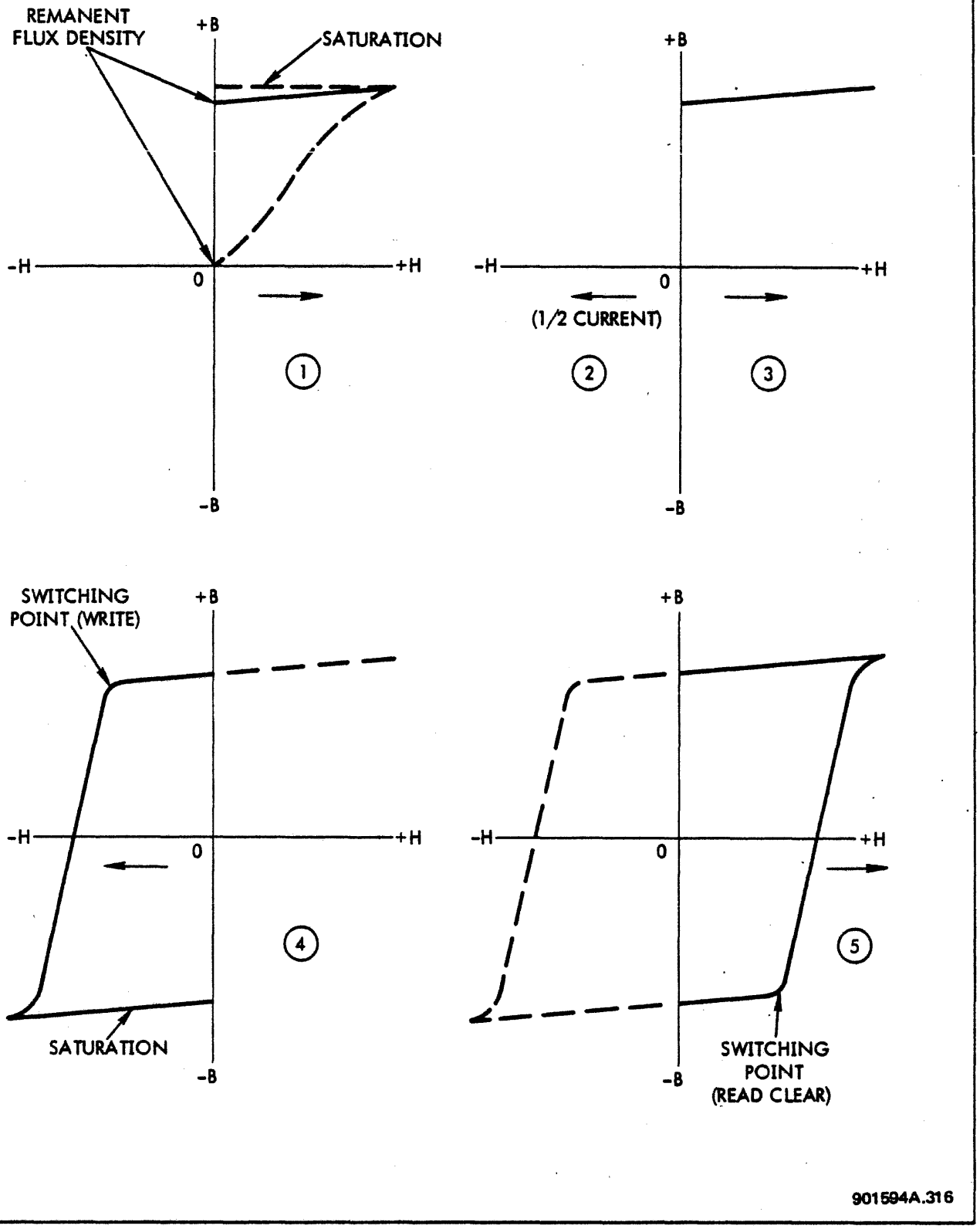


Figure 3-16. Square Hysteresis Loop - Memory Magnetic Core

the logic state of the core and therefore a sense wire is inserted through the core to provide this information. In order to understand the use of the magnetic core as a memory or storage cell, the following is a read/write sequence of events concerned with a single core. The sequence provides a step-by-step generation of the square hysteresis loop, figure 3-16.

Assume the magnetic memory core read/write sequence begins with an unpolarized core. The magnetic core has been located (addressed) by the X and Y drivelines and at the beginning of the read cycle, the X and Y drivelines apply a magnetizing force (additive 1/2 currents) on the core in the direction shown in state 1. The force is removed and the core remains magnetized to near saturation for the first time.

During the restore/write cycle the magnetizing force is reversed, stage 2, but the Y-driveline is inhibited in order to write in a zero. The magnetizing force therefore is less than the critical switching value and has no effect on the flux density; a zero is stored in the core. With the magnetic core polarized as shown in stage 3, the read cycle starts again with the same X and Y driveline coincidence and a magnetizing force is applied in the same direction as in the first read cycle. The core is already near saturation and the force has little or no effect on the flux density, There is no reversal of polarity and therefore no pulse on the sense line. The absense of a pulse is interpreted as a zero and this state is stored in the memory information register (MR).

A write cycle is started and the magnetizing force (X and Y-driveline coincidence)is reversed, stage 4; the Y-driveline is not inhibited therefore the change in H is greater than the critical value and this change abruptly

reverses the magnetization of the core. The core changes state from zero to one. This change is not stored in any external register as the sense line is inhibited during the write operation.

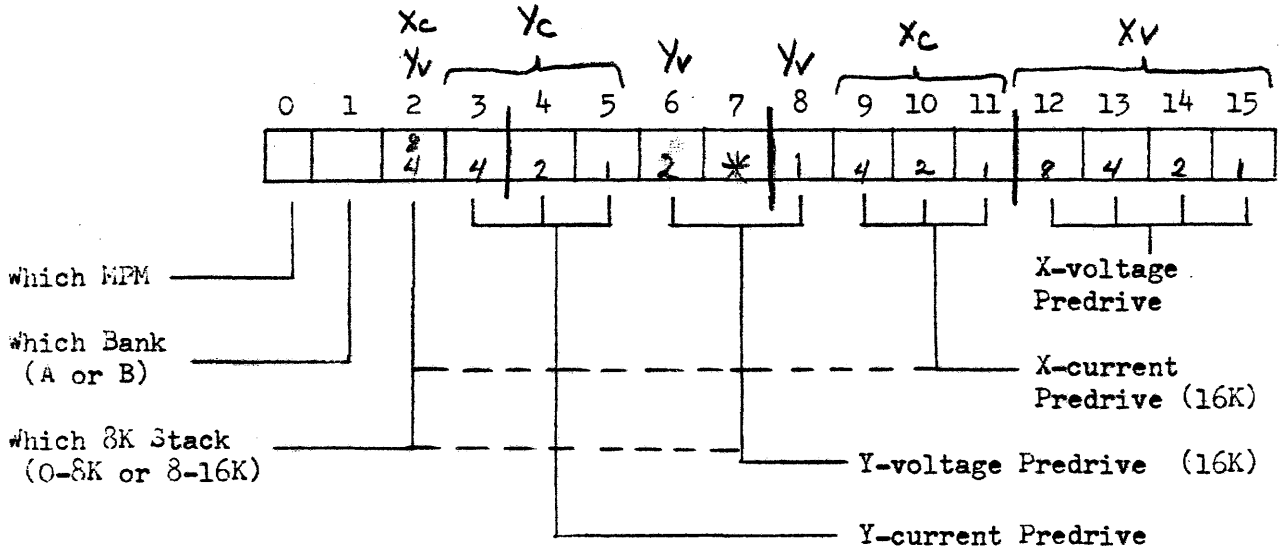
During the following memory cycle (read half-cycle portion) the magnetizing force (the same X and Y currents) is reversed, stage 5. This force is greater than the critical switching value and the core is switched to the opposite state, or the core is cleared to a zero. This clearing pulse is sensed by the sense line and is interpreted as a one; this affects a change in the state of the data bit stored in the MR register. The previously stored zero (in the MR register) is replaced by a one and the core has returned to a zero state. This last operation indicated that the read half-cycle is destructive, therefore the read-cycle is always followed by the write-cycle in order to restore the core to the previous state or to write in new information.

3-22 X AND Y-DRIVELINE AND Y-INHIBIT LOGIC

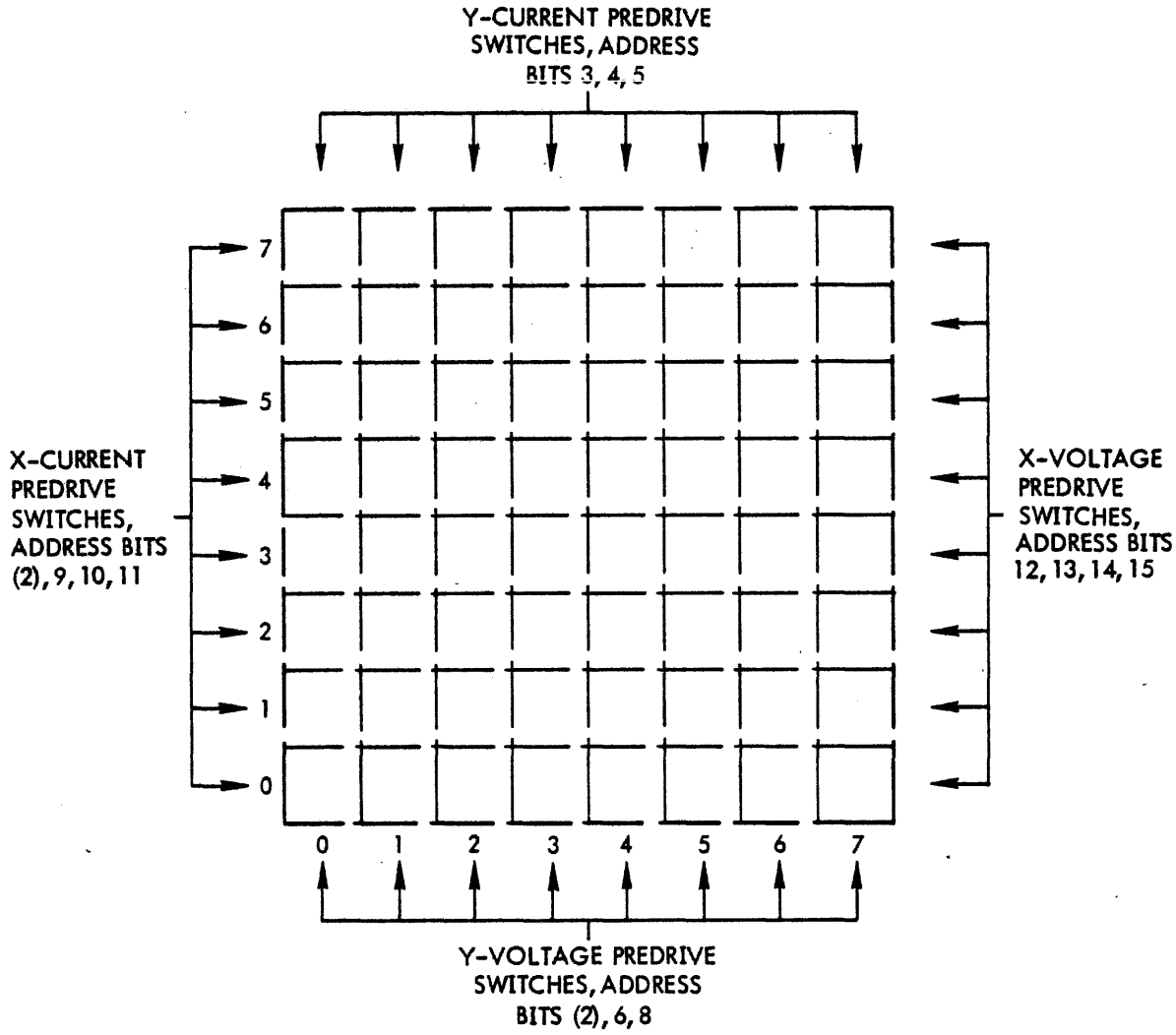
As previously described in paragraph 3-20, each magnetic core in memory is located (addressed) by a set of X and Y-drivelines. The drivelines supply the magnetizing force to switch the state of the core in reading out data or writing in data. Refer to figure 3-4. The X and Y-driveline and Y-inhibit logic consists of current and voltage predrive circuits and bipolar-current and voltage switches (YCPS, YCNS, XCPS, XCNS, YVPS, YVNS, XVPS and XVNS) controlled by the associated predrive circuits. The predrive and inhibit circuits are gated by appropriate timing pulses ATPYC, ATNYC, ATPYV, ATNYV, ATNXC, ATPXC, ATNXV, ATPXV, ATPYI and ATNYI from the MPM stack and phasing and timing logic (paragraph 3-15). The X and Y-driveline and Y-inhibit logic is contained on 2-high modules in slots 7 through 16 of chassis H/J. The X and Y drivelines require a source of drive current (positive)

at one end and a sink for this current at the other. The source and sink are both provided by the current and voltage switches depending on the configuration of address bits L06, L07 and L09 (refer to paragraph 3-16).

At the beginning of a memory cycle, after the port selection logic in the MPM section determines which port will access memory, the associated address bits (AS02-AS15) are gated to the X and Y predrive circuits in the BMU. The following is the 16-bit address word format showing the bit assignments for X and Y-predrive circuit selection.



Refer to figure 3-17 in conjunction with the address word format shown above. Each bit plane is divided into 64-16 x 8 core groups. The X-Y elements (cores) of the 64 matrices are assigned to coded areas 0 through 7 in both dimensions. Address bits 3, 4, 5, 6 and 8 select the Y-voltage and current predrive



NOTE:
Y-MATRIX ORDER FOR BIT PLANES 0, 1, 4, 5, 8, 9, 12, 13 AS SHOWN.
THE Y-MATRIX ORDER IS OPPOSITE FOR BITS 2, 3, 6, 7, 10, 11, 14, 15

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Figure 3-17. Typical Bit Plane Division for Core Location

circuits which control the Y-dimension of core matrices in 8k of memory. Address bits 9 through 15 select the X-current and voltage predrive circuits which control the X-dimension for 8K of memory. Address bit 2 determines which group of predrive circuits are to be selected, those controlling 0-8K or 8-16K. Address bit 7 is used in the MPM logic to determine Y-current direction (paragraph 3-16) and also (in conjunction with bit 2) to determine preamplifier selection in the sensing and preamp logic, paragraph 3-35.

In the X-dimension, the binary value of bits 9, 10, and 11 plus a timing pulse, select an X-band (0 through 7) and the direction of X-current. The binary value of bits 12 through 15 plus a timing pulse select one of 16 X-lines in the selected X-band. In the Y-dimension, the binary value of bits 3, 4, and 5 plus a timing pulse select a Y-column (0 through 7) and the direction of the Y-current. The binary value of bits 6 and 8 plus a timing pulse select one of four Y-line loops in the selected Y-column. Address bit 2 determines in which 8K the four Y-line loops are located, 0-8K or 8-16K.

3-23 X-Driveline Circuits - Modules RTT11 and RTT12

The X-current predrive circuits and current switches for 0-8K of bank A are provided for by two RTT11 modules in slots 12 and 14 of 2-high chassis H/J. Two additional RTT11 modules (optional) are added in slots 8 and 10 to provide the current predrive and current switches for an additional 8K (8-16K) for bank A. The X-voltage predrive circuits and voltage switches for 0-16K of bank A are provided for by two RTT12 modules in slots 15 and 16.

Theoretically, the core diode module (½ byte, 0, 1, 2, or 3) is folded longitudinally along the X-dimension into upper and lower sections. Memory address register bit 2 determines which 8K is selected (0-8K or 8-16K) and address bit 9 determines which section (upper or lower) of the X-bands is selected.

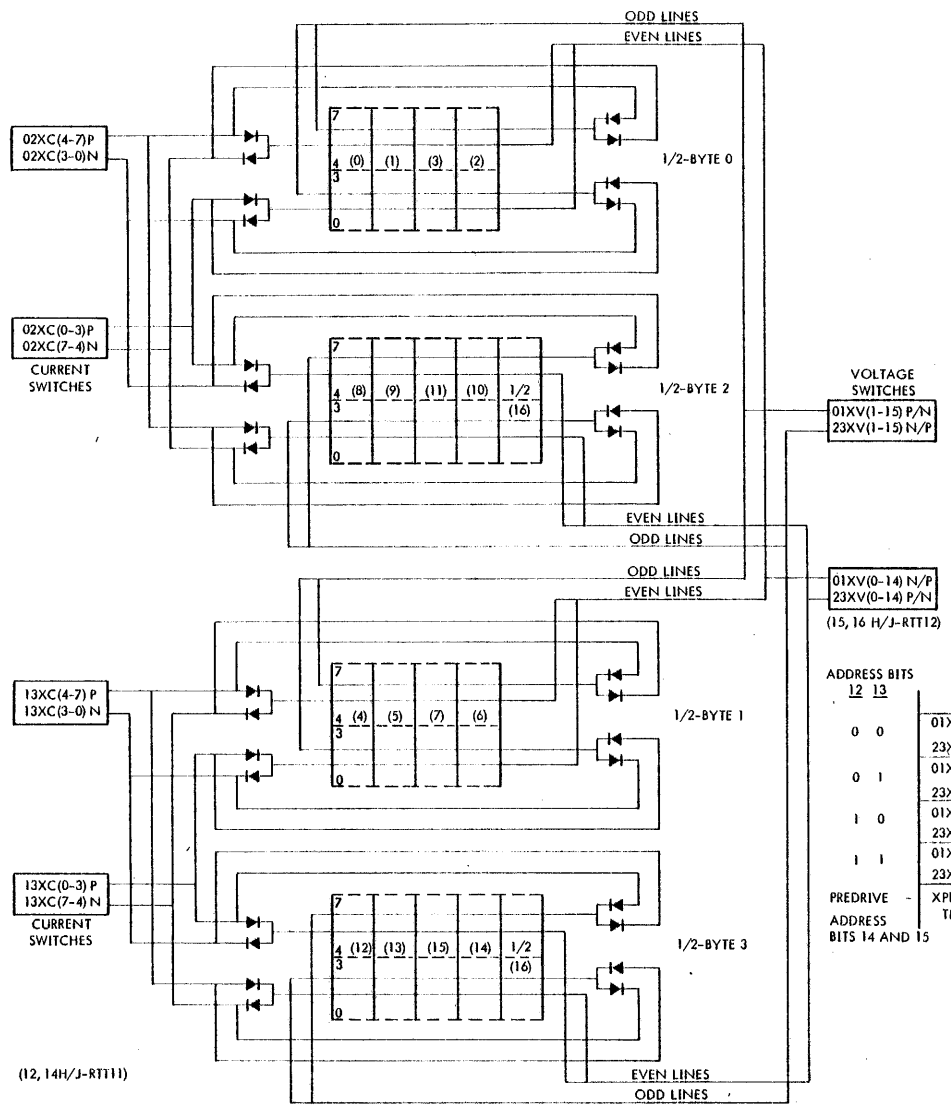
Refer to figure 3-18 and ESM 902401, Section II, sheet 8 of BMU logic diagrams. Address bits 2, 9, 10 and 11 select the four predrive circuits whick control a 4 x 4 matrix of X-current switches arranged in 16 groups of four current switches each. Each RTT11 module provides four groups of eight pairs (eight positive and eight negative switches). Each group of switches control a specific pair of complement X-bands (0/7, 1/6, ... 8/15, 9/14, etc.). Note: X-bands in 8-16K are numbered 8-15 and are located in equivalent positions to 0 through 7 in 0-8K.

Address bits 2 and 9 plus a current direction timing pulse (TPXC or TNXC) select the top of a predrive line (XPNCKO through XPNCK3) and address bits 10 and 11 plus the same timing pulse select the bottom of the same predrive line. Each predrive circuit provides control for four groups of switches (i.e., XPNCKO controls groups 0, 4, 8, and 12 or complement X-bands 0/7, 4/3, 8/15, 12/11). Only one group is selected at any given time.

If predrive XPNCKO is selected for the read half cycle, the complement predrive (XPNCK3) is selected for the write half cycle by a change to the other current direction timing pulse (TPXC/TNXC). The X-current predrive address bits and the timing pulses, therefore, select a pair of predrive circuits, for a complete read/write memory cycle. (i.e., XPNCKO and XPNCK3, XPNCK1 and XPNCK2, XPNCK3 and XPNCKO or XPNCK2 and XPNCK1.)

Each group of switches selected by a predrive circuit contains two pairs of unipolar switches. Each pair provides the source or sink for complement X-bands in alternate 1/2-bytes (0 and 2, and 1 and 3). Positive (P) designations represent a source and negative (N) designations represent a sink.

3-24. X-Band Selection. An example X-band selection is as follows: Assume a binary coded decimal address of NAS02, NAS09, AS10, and NAS11 (00 at the top of the predrive line and 10 at the bottom or 0010 = 2) and the TPXC current direction timing pulse. Predrive circuit XPNCK2 is selected and the switch



X-CURRENT SWITCHES 4 X 4 MATRIX

ADDRESS BITS 2 9					
TPXC, 0 0 OR TNXC, 0 1	02XC0P 0 02XC7N 13XC0P 13XC7N	02XC1P 1 02XC6N 13XC1P 13XC6N	02XC2P 2 02XC5N 13XC2P 13XC5N	02XC3P 3 02XC4N 13XC3P 13XC4N	RTT11-14H/J 0K-8K
TPXC, 0 1 OR TNXC, 0 0	02XC4P 4 02XC3N 13XC4P 13XC3N	02XC5P 5 02XC2N 13XC5P 13XC2N	02XC6P 6 02XC1N 13XC6P 13XC1N	02XC7P 7 02XC0N 13XC7P 13XC0N	RTT11-12H/J
TPXC, 1 0 OR TNXC, 1 1	02XC8P 8 02XC15N 13XC8P 13XC15N	02XC9P 9 02XC14N 13XC9P 13XC14N	02XC10P 10 02XC13N 13XC10P 13XC13N	02XC11P 11 02XC12N 13XC11P 13XC12N	RTT11-10H/J 8K-10K
TPXC, 1 1 OR TNXC, 1 0	02XC12P 12 02XC11N 13XC12P 13XC11N	02XC13P 13 02XC10N 13XC13P 13XC10N	02XC14P 14 02XC9N 13XC14P 13XC9N	02XC15P 15 02XC8N 13XC15P 13XC8N	RTT11-08H/J
PREDRIVE –	XPNCK0	XPNCK1	XPNCK2	XPNCK3	
TPXC, OR TNXC,	00 11	01 10	10 01	11 00	BITS 10 AND 11

X-VOLTAGE SWITCHES 4 X 4 MATRIX

ADDRESS BITS 12 13	EVEN LINES 0, 4, 8, 12		ODD LINES 1, 5, 9, 13		EVEN LINES 2, 6, 10, 14		ODD LINES 3, 7, 11, 15		
0 0	01XV00P 23XV00N	01XV00N 0 23XV00P	01XV01P 23XV01N	01XV01N 1 23XV01P	01XV02P 23XV02N	01XV02N 2 23XV02P	01XV03P 23XV03N	01XV03N 3 23XV03P	RTT12-15H/J
0 1	01XV04P 23XV04N	01XV04N 4 23XV04P	01XV05P 23XV05N	01XV05N 5 23XV05P	01XV06P 23XV06N	01XV06N 6 23XV06P	01XV07P 23XV07N	01XV07N 7 23XV07P	
1 0	01XV08P 23XV08N	01XV08N 8 23XV08P	01XV09P 23XV09N	01XV09N 9 23XV09P	01XV10P 23XV10N	01XV10N 10 23XV10P	01XV11P 23XV11N	01XV11N 11 23XV11P	RTT12-16H/J
1 1	01XV12P 23XV12N	01XV12N 12 23XV12P	01XV13P 23XV13N	01XV13N 13 23XV13P	01XV14P 23XV14N	01XV14N 14 23XV14P	01XV15P 23XV15N	01XV15N 15 23XV15P	
PREDRIVE – ADDRESS BITS 14 AND 15	XPNVK0 TPXV 00	XNPVK0 TNXV	XPNVK1 TPXV 01	XNPVK1 TNXV	XPNVK2 TPXV 10	XNPVK2 TNXV	XPNVK3 TPXV 11	XNPVK3 TNXV	

Figure 3-18. X-Drive Line Logic

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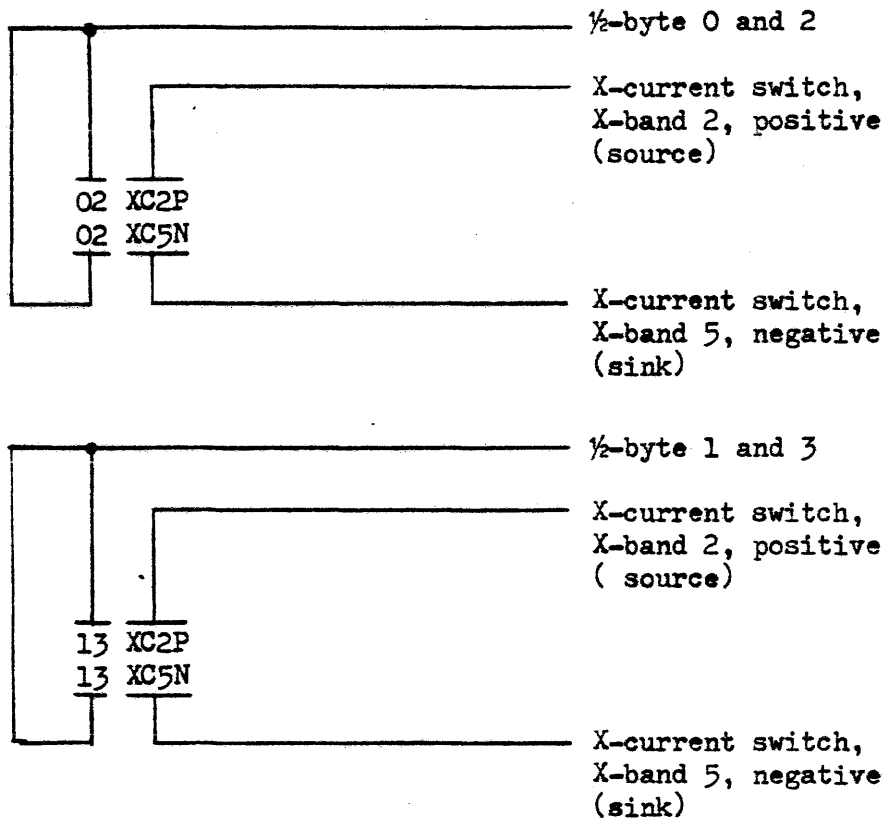
pairs in group two are pulsed by the predrive circuit. The output of group two is coded as follows:



The 02XC2P portion of group two provides the source for X-band 2 in 1/2-byte 0 and X-band 5 in 1/2-byte 2. The 02XC5N portion of group two provides the sink for X-band 2 in 1/2-byte 2 and X-band 5 in 1/2-byte 0. The unipolar switch pair 13XC2P/13XC5N provides the same potentials for 1/2-byte 1 and 3.

3-25. X-Line Selection. Address bits 12 through 15 and a timing pulse (TPXV or TNXV) select one of eight predrive circuits which control a 4X4 matrix of X-voltage switches arranged in 16 groups of two bipolar switches each. Each group controls a specific X-line (lines 0 through 15) in each X-band. There are a total of eight pairs of switches per RTT10 module.

Address bits 12 and 13 plus a voltage timing pulse select the top of one of eight predrive lines (XPNVK0 through XPNVK3 and XNPVK0 through XNPV3) and address bits 14 and 15 plus the same timing pulse select the bottom of the predrive line. Each predrive circuit controls the polarity of the output of four groups of two bipolar voltage switches (i.e., XNPVK2 controls the polarity output of groups 2, 6, 10 and 14 or the control of lines 2, 6, 10, and 14 of each X-band.)

If predrive XNPVK2 is selected for the read half cycle, the complement predrive (XPNVK2)is selected for the write half cycle by a change in the timing pulse (i.e., TNXV to TPXV). The X-voltage predrive address bits and the timing pulses, therefore, select both the source and sink circuits for a pair of predrive lines for a complete read/write memory cycle (i.e., XPNVK0 and XNPVK0, XPNVK1 and XNPVK1, etc.). One predrive circuit selects one polarity output each (opposite polarities) from a pair of bipolar switches. If one switch output provides the sink for X-lines in byte 0 (½-byte 0 and 1) the other provides the source for the same X-lines in byte 1 (½-byte 2 and 3). Therefore, when the complement predrive circuit is selected by a change in the timing pulse, the opposite output from the same bipolar switches provide the opposite polarities to the same X-lines in byte 0 and byte 1. Positive (P) designations represent a source and negative (N) represent a sink.

An example of X-line selection is as follows: Assume a binary coded decimal address of NAS12, AS13, AS14, and NAS15 (01 at the top of the predrive line and 10 at the bottom, or 0110 = 6) and a timing pulse of TNXV. Note: /Current direction timing pulse TPXC was selected previously (paragraph 3-24) for X-current, therefore, TNXV is selected for X-voltage predrive. Address 0110 and TNXV select predrive XNPVK2 and alternate polarity output is pulsed from the bipolar switch pair 01XV06/23XV06. Bipolar switch 01YV06 is negative with respect to Vm and provides

the sink for line 6 in complement X-bands in byte 0 (½-byte 0 and 1) and bipolar switch 23XV06 is positive with respect to Vm and provides the source for line 6 in complement X-bands for byte 1 (½-byte 2 and 3).

Considering both examples, X-band selection (02XC2P/02XC5N and 13XC2P/13XC5N, paragraph 3-24) and the X-line selection, the only X-line in which drive current is completed is in line 6, X-band 2 of both bytes 0 and 1. The drive current in line 6 of complementary X-band 5 is not completed due to the same polarity present at each end of the line (i.e.; 02XC5N to 01XV6N and 13XC2P to 23XV6P.) However, the drive current in line 6 of X-band 5 can be completed when X-current predrive XPNCK2 is addressed by bits 2, 9, 10 and 11 in the configuration of 0101 = 5 in conjunction with timing pulse TNXC and voltage predrive XPNVK2 selected by a change in the timing pulse from TNXV to TPXV.

3-26. Y-Driveline Circuits - Modules RTT10 and RTT11

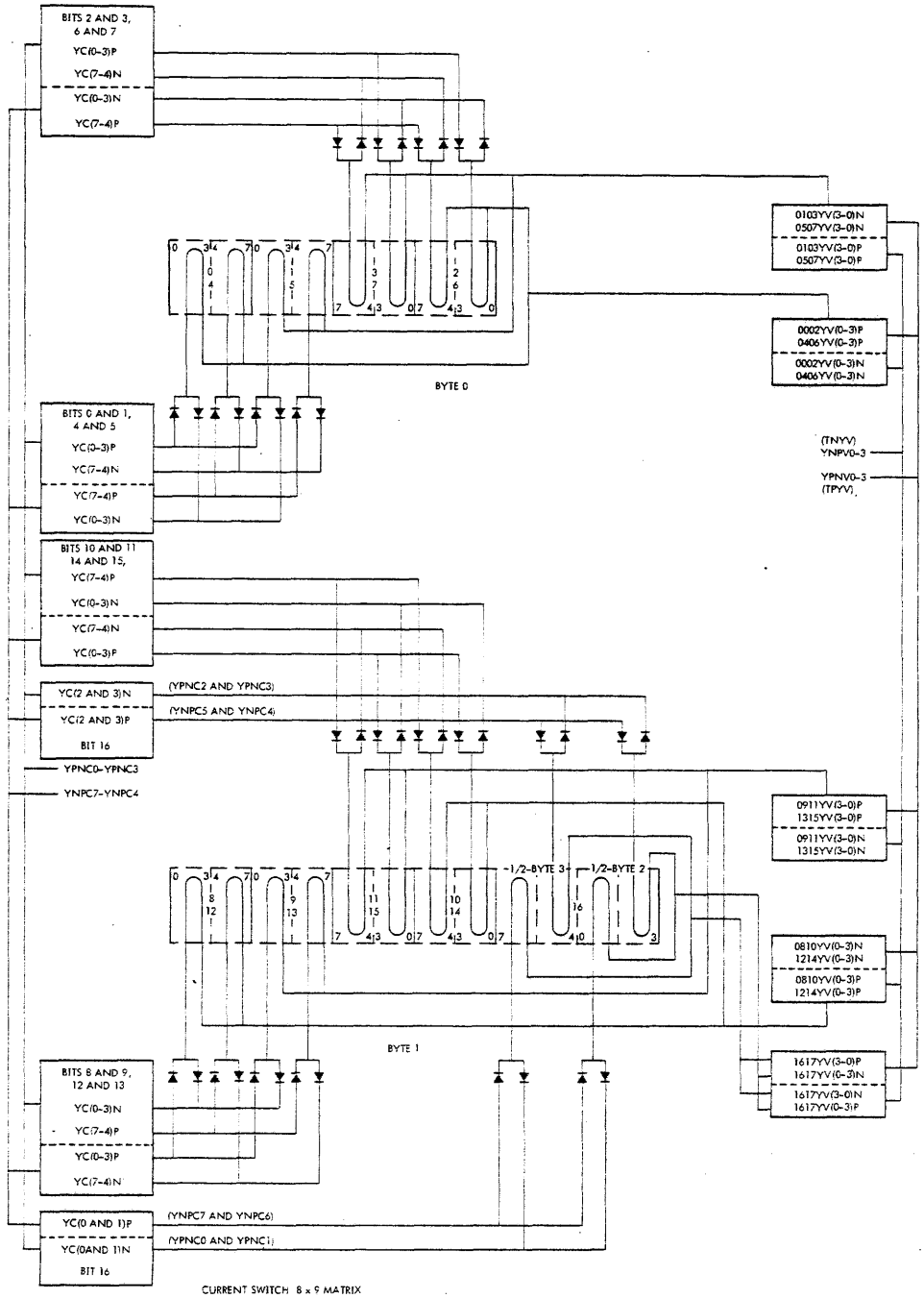
The Y-current predrive circuits and current switches for 16K (bank A) are provided for by four RTT10 modules located in slots 7, 9, 11, and 13 of 2-high chassis H/J. The Y-voltage predrive and voltage switches for 0-8K are provided for by two RTT11 modules in slots 12 and 14. Two additional RTT11 modules (optional) are added in slots 8 and 10 to provide for voltage predrive and voltage switches for an additional 8K (8-16K) for bank A. Slots 7 through 14 of chassis H/J, therefore, contain the Y-driveline logic for bank A.

Theoretically, the bit-plane is folded vertically into two halves, four Y-columns each. Y-columns 0-3 in one half and Y-columns 4-7 in the remaining half. The logic level of address bit 3 determins which half of the bit-plane is selected; NAS03 = Y-columns 0-3 and AS03 = Y-columns 4-7. Y-columns are selected from both halves in complementary pairs, 0 and 7, 1 and 6, etc., and one bit-plane is a mirror image of the adjacent bit-plane from bit zero through bit 15.

Refer to figure 3-19 and ESM 902401, Section II, sheets 6 and 7 of BMU logic diagrams. Address bits 3, 4, and 5 select an 8X9 matrix of Y-current switches which control all 16K. One of eight predrive circuits is addressed by bits 3, 4, and 5 in the configuration of a binary coded decimal value of 0 through 7 plus TPYC, or the inversion (complement) value, plus TNYC (i.e.; 000=0 and TPYC or 111=7 and TNYC selects predrive YPNC0.)

Each predrive circuit selects a string of nine bipolar pairs of current switches (18 unipolar switches, nine positive and nine negative). There are four pairs (8) for byte 0, for pairs (8) for byte 1 and one pair for bit 16. There is a pair assigned for each two adjacent bit-planes zero through 15 and one pair for bit-plane 16. During the read half cycle, if one string is selected by a predrive circuit and TPYC, the complement predrive is selected during the write half cycle by a change in the Y-current direction timing pulse to TNYC. The Y-current predrive address bits and the timing pulses, therefore, select a pair of predrive circuits for a complete read/write memory cycle (i.e., YPNC0/YNPC7, YPNC1/YNPC6, YPNC2/YNPC5, or YPNC3/YNPC4). Positive (P) designations represent a source and negative (N) represent a sink.

Four bipolar pairs of switches in a selected string provide the source for a Y-column and the sink for the complementary Y-column (i.e.; YC0P/YC7N, YC1P/YC6N, etc.) in adjacent bit-planes in byte 0 (bits 0-7). The next four pairs in the string provide the source and sink for complementary Y-columns in adjacent bit-planes in byte 1 (bits 8-15), however, the current is in the opposite direction to that chosen for the same Y-columns in byte 0 (i.e.; YC7P/YC0N, YC6P/YC1N, etc.) Only one of the pair assigned to bit 16 is used in each string; if the positive switch is used in one string, the negative switch is used in the complement string (i.e.; YC0N/YC0P for predrives YPNC0/YNPC7, respectively.



CURRENT SWITCH 8 x 9 MATRIX

BYTE 0 (4 PAIRS)	-	YC0P YC7N	YC7P YC0N	YC1P YC6N	YC6P YC1N	YC2P YC5N	YC5P YC2N	YC3P YC4N	YC4P YC3N
BYTE 1 (4 PAIRS)	-	YC7P YC0N	YC0P YC7N	YC6P YC1N	YC1P YC6N	YC5P YC2N	YC2P YC5N	YC4P YC3N	YC3P YC4N
BIT 16 (1 PAIR)	-	YC0N	YC0P	YC1N	YC1P	YC2N	YC2P	YC3N	YC3P
TPYC (AND 3, 4, 5) TNYC (AND 3, 4, 5)	- -	YPNC0 (000) (111)	YNPC7 (111) (000)	YPNC1 (001) (110)	YNPC6 (110) (001)	YPNC2 (010) (101)	YNPC5 (101) (010)	YPNC3 (011) (100)	YNPC4 (100) (011)

VOLTAGE SWITCH 8 x 10 MATRIX

		YV0		YV1		YV2		YV3		YV4		YV5		YV6		YV7	
		YPNV0	YNPV0	YPNV1	YNPV1	YPNV2	YNPV2	YPNV3	YNPV3	YPNV4	YNPV4	YPNV5	YNPV5	YPNV6	YNPV6	YPNV7	YNPV7
BYTE 0	EVEN BITS (2) -	YV0P	YV0N	YV1P	YV1N	YV2P	YV1N	YV3P	YV3N	YV4P	YV4N	YV5P	YV5N	YV6P	YV6N	YV7P	YV7N
	ODD BITS (2) -	YV3N	YV3P	YV2N	YV2P	YV1N	YV2P	YV0N	YV0P	YV7N	YV7P	YV6N	YV6P	YV5N	YV5P	YV4N	YV4P
BYTE 1	EVEN BITS AND 16 (3) -	YV0N	YV0P	YV1N	YV1P	YV2N	YV1P	YV3N	YV3P	YV4N	YV4P	YV5N	YV5P	YV6N	YV6P	YV7N	YV7P
	ODD BITS AND 16 (3) -	YV3P	YV3N	YV2P	YV2N	YV1P	YV2N	YV0P	YV0N	YV7P	YV7N	YV6P	YV6N	YV5P	YV5N	YV4P	YV4N
2, 6, 8 (AND TPYV OR TNYV)		(000) LOOP 0 AND 3		(001) LOOP 1 AND 2		(010) LOOP 2 AND 1		(011) LOOP 3 AND 0		(100) LOOP 0 AND 3		(101) LOOP 1 AND 2		(110) LOOP 2 AND 1		(111) LOOP 3 AND 0	
		0-8K								8-16K							

Figure 3-19. Y-Drive Line Switch Logic

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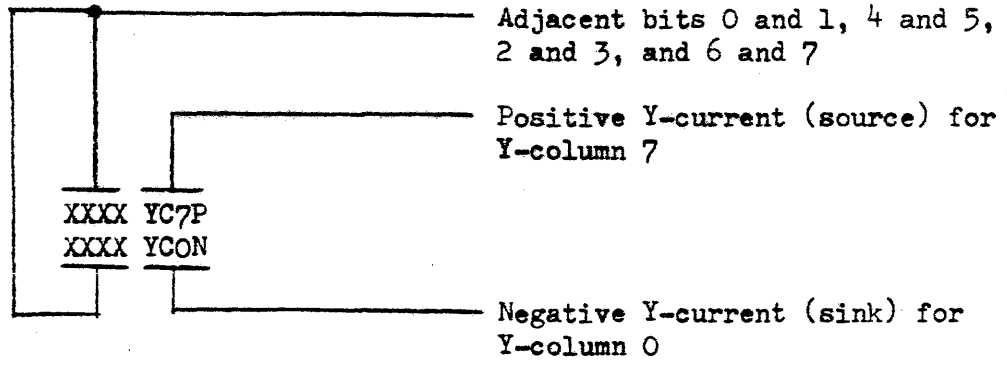
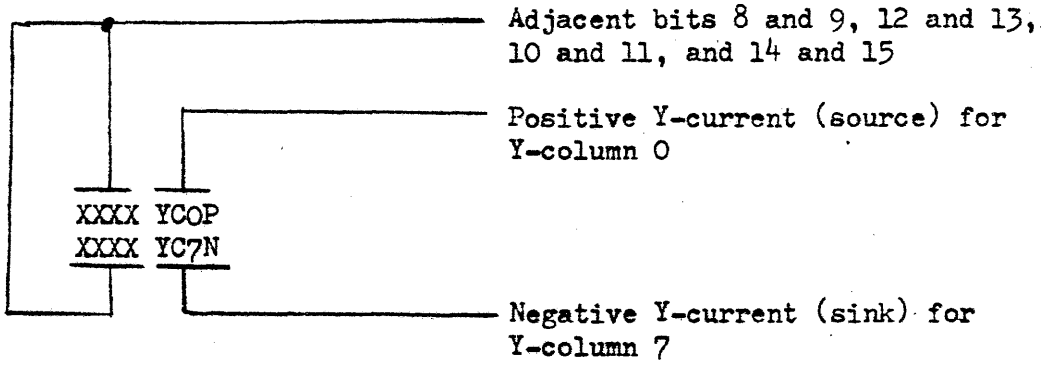
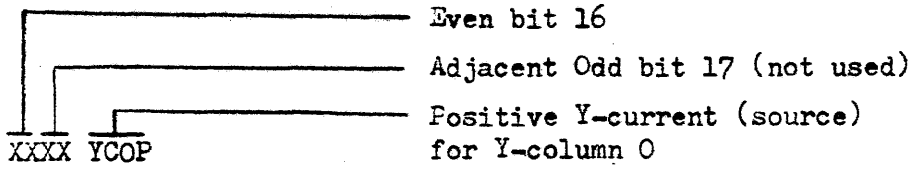
3-27. Y-Column Selection. An example of Y-column selection is as follows: Assume a binary coded decimal address configuration of AS03, AS04, and AS05 (111 = 7) and Y-current direction pulse TPYC. With these conditions, predrive YNPC7 is selected and the switch pairs in the second string (figure 3-19) are pulsed by the predrive circuit. The output from the first four bipolar pairs of current switches are coded as follows:



The next four pairs:



The last pair:



The 0001-0607YC7P portion of the first four pairs provide the source for Y-column 7 in byte 0 and the 0001-0607YC0N portion provides the sink for the complement column, 0. The 0809-1415YC7N portion of the second four pairs provide the sink for Y-column 7 and the source for Y-column 0 in byte 1. The positive portion of 16YC0 provides the source for Y-column 0 on bit-plane 16.

3-28. Y-Line Loop Selection. Address bits 2, 6, and 8 and a timing pulse, TPYV or TNYV, select an 8X10 Y-voltage switch matrix controlling 16K. The binary value of address bits 2, 6, and 8 (000=0 through 111=7) select one of eight strings (YV0 through YV7) of 10 bipolar voltage switches. Each side of the string consists of one-half the polarity output from 10 switches, arranged in alternate polarity output sequence. Each side of the string is selected by a separate predrive circuit and there are 16 predrive circuits which are selected by one of eight address configurations and one of two timing pulses. For example: Predrives YPNV0 through TPNV7 are selected by 000-0 through 111=7 and TPYV, and YNPV0 through YNPV7 are selected by the same address configurations, and TNYV.

Each Y-column of a bit plane is made up of four Y-line loops (0 through 3) providing eight Y-lines per Y-column. One end of each loop terminates at the same Y-current switch and the other at one of four voltage switches (refer to figure 3-20.) Each string of bipolar voltage switches (YV0 through YV7) control a Y-line loop in Y-columns in one bit plane and the complement Y-line loop in Y-columns in the adjacent bit-plane; one Y-line loop in all even bits and the complement Y-line loop in all odd bits throughout the 16-bit data word. Two loops are selected in bit-plane 16 (17th bit) but the current in only one is completed. Switch strings designated as YV0 through YV3 control Y-line loops 0 through 3 and those designated as YV4 through YV7 control equivalent loops in 8-16K.

During the read half cycle, if one of the YNPV0 through YNPV7 predrive circuits is selected, the associated string of bipolar voltage switches are pulsed by the predrive. The first four switches of the string provide the sink for one

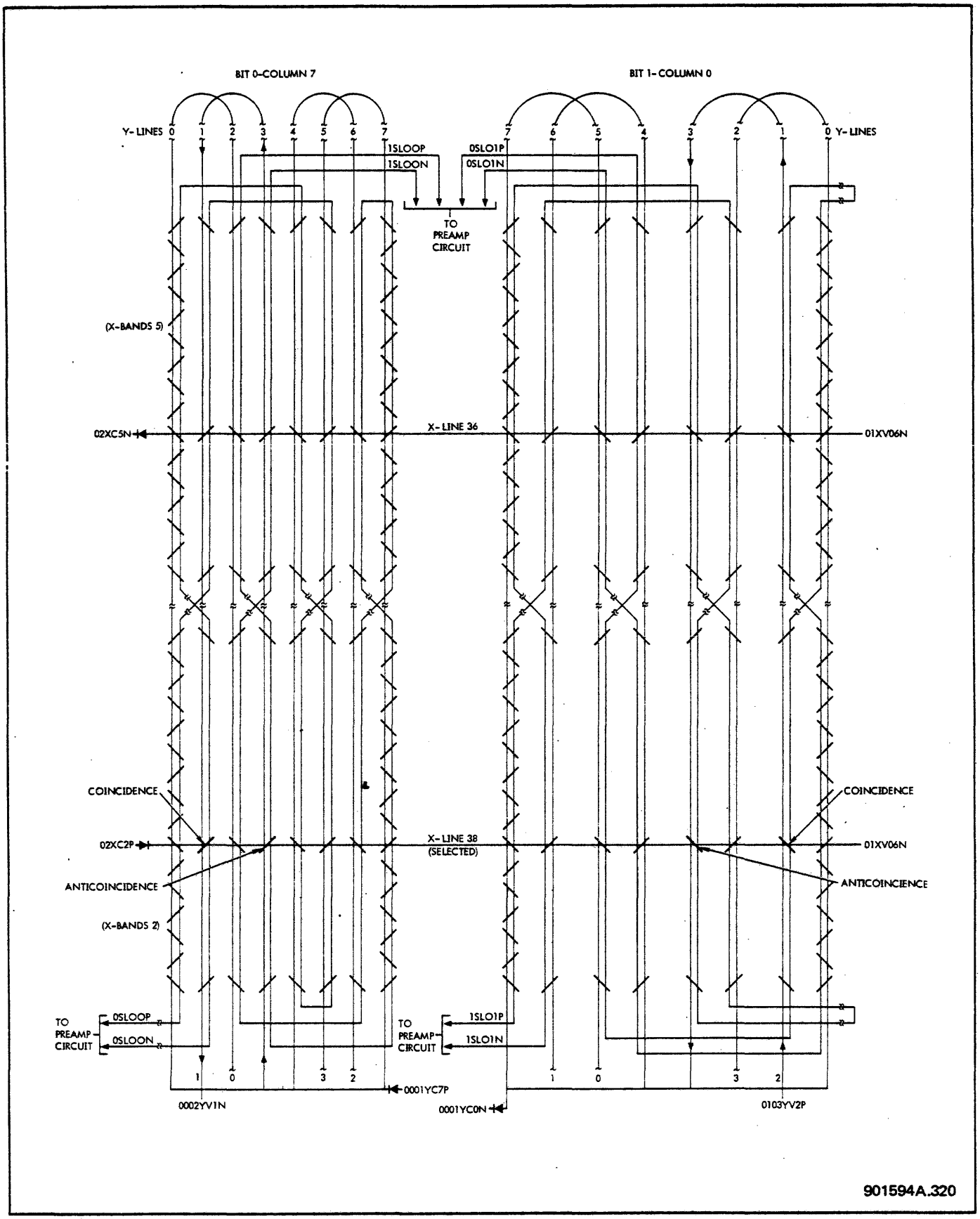
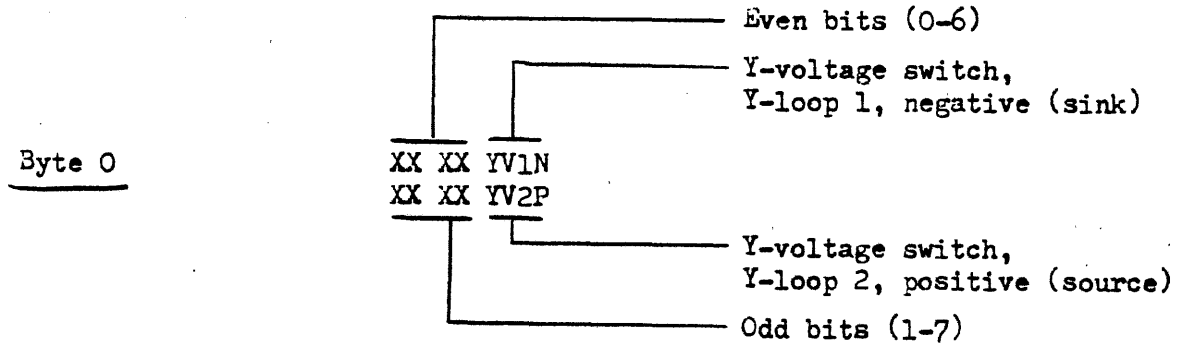


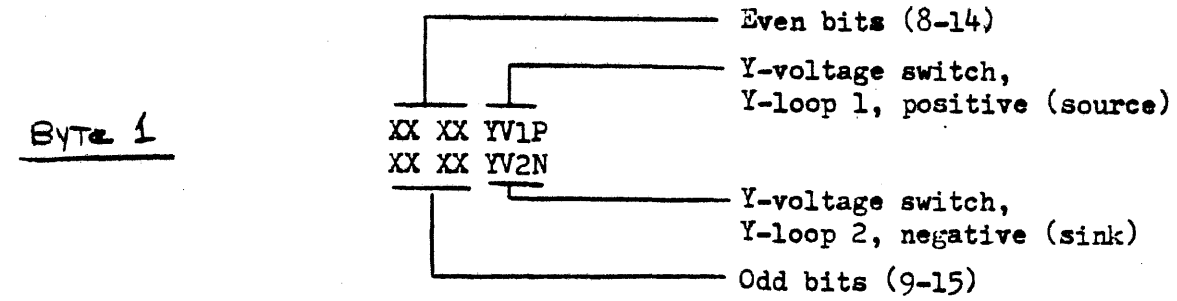
Figure 3-20. Coincident and Anticoincident Selection and Sense Line Pattern

of four Y-line loops in the even bit-planes and the source for the complement Y-line loops in the odd bit-planes in byte 0. The next four provide the reverse polarities for the same loops in byte 1. The remaining two provide the sink and source for complement Y-loops of bit 16. During the write half cycle the complement predrive is selected by a change in the timing pulse from TNYV to TPYV and the complement predrive selects the opposite output from the string of switches and the X-line loops are driven in the opposite direction.

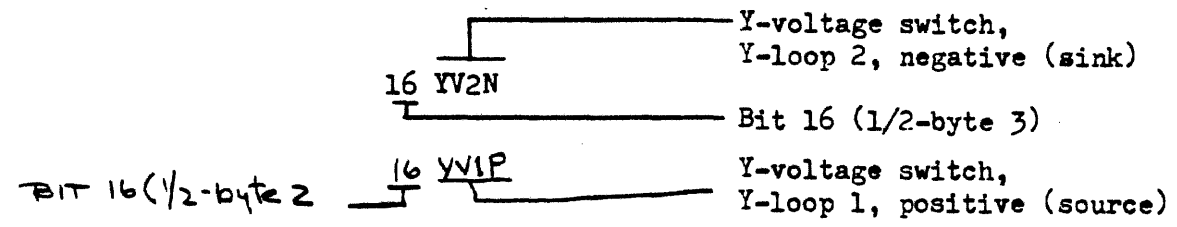
An example of Y-line loop selection is as follows: Assume a binary coded decimal address of NAS02, NAS06 and AS08 (001=1). The YV1 string is selected and if TNYV is generated (TPYC was generated for the Y-current in the example in paragraph 3-27) the N to P side of the switch string is selected by predrive circuit YNPV1. The associated string is pulsed by the predrive and the output from the first four switches of the string are coded as follows:



The next four are coded as follows:



The last two are coded as follows:

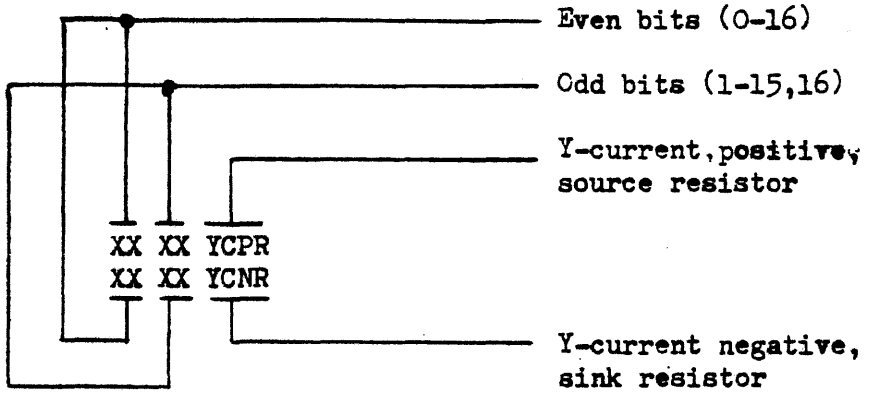


With reference to the Y-column selection procedure in paragraph 3-27, the following Y-loop selection takes place: The sink for Y-line loop 1 in byte 0 and source for Y-line loop 1 in byte 1 is provided for Y-column 7 for all even bits. The source for complement Y-line loop 2 in byte 0 and the sink for Y-line loop 2 in byte 1 is provided for complement Y-column 0 for all odd bits. Since only the source for Y-column 0 was provided for bit 16 in the Y-column example, only the sink for loop 2 will complete the current in this loop; the source for loop 1 cannot be completed with the same polarity present at both ends of the loop.

3-29. Y-Driveline Inhibit Circuits - Modules RTT11 and RTT12

Refer to ESM 902401, Section II, Sheet 6 of BMU Logic Diagrams. The Y-driveline inhibit circuits drop the operating level of the source output and raise the operating level of the sink output of the Y-current bipolar switches controlling the Y-drivelines. This action inhibits the function of the selected Y-current bipolar switches. Inhibit circuits for bit planes 0 through 15 are provided by RTT10 modules in slots 7, 9, 11, and 13 of 2-high chassis H/J. The inhibit circuit for bit plane 16 is provided by RTT12 module in slot 15.

During the write half-cycle when the data to be stored in core is a zero, the Y-driveline circuits must be inhibited in order not to write in a one. Therefore, the negation of data terms (NDOO through ND16) plus the appropriate timing pulse for inhibiting are used to satisfy the conditions to energize an inhibit circuit. There is a pair of source/sink inhibit circuits for each two adjoining bit planes. These circuits are coded as follows:



The timing pulse used by the inhibit circuit represents the same polarity (TPYCI or TNYCI) as the Y-current timing pulse (TPYC or TNYC) used during the write cycle.

3-30. X and Y-Driveline Coincidence

A magnetic core switches state when the X and Y-drivelines at the core are in coincidence. Coincidence at a core occurs when the direction of current flow in both drivelines is in the same direction as the current approaches the same face of the core. Coincidence at a core (if a one has been previously stored) results in a pulse on a senseline threaded through the cores parallel to the Y-line. Figure 3-20 illustrates the configuration of bit-planes 0 and 1 as a result of the address used in the examples described in paragraphs 3-24 through 3-28.

The X-line, line 38, is X-line 6 in X-band 2 and is driven by 02XC2P X-current switch (paragraph 3-24) and the sink for the current on this line is provided by X-voltage switch 01XV06N (paragraph 3-25). The X-line 86 is line 6 in X-band 5. The drive current on this line, however, was not completed by the example address.

On bit-plane 0, column 7, Y-line loop 1 is selected by Y-voltage switch 0002YV1N (paragraph 3-28). This switch provides a sink for the current flow on line 3 provided by Y-current switch 0001YC7P (paragraph 3-27). The current flow (conventional) is up line 3 and down line 1 to the sink switch. In bit-plane 1, column 0, Y-line loop 2 is driven by Y-voltage switch 0103YV2P (paragraph 3-28). This switch provides the source for the current flow on line 3 which is completed through line 1 by Y-current switch 0001YC0N (paragraph 3-27).

Coincidence occurred on line 1 on both bit-planes in complementary columns; bit-plane zero, therefore, is a mirror image of bit one. The same pattern prevails in the remaining bit-planes of ½-byte zero; bit-plane 2 mirrors bit-plane 3 and each half of the 1/2-byte is a mirror of the other half.

As indicated in figure 3-20, the selected Y-line also meets the X-line at a core in anti-coincidence. (Refer to Y-column 7 in bit-plane zero.) Coincidence cannot occur at this core due to the direction of the Y-current on the way up line 3. However, if address bit 7 was high in the example address, the Y-current would be reversed and coincidence would occur at this core; bit 7 is considered the anti-coincidence address bit (refer to paragraph 3-16). Address bit 7 (in conjunction with bit 2) also determines which senseline loop of the bit-plane is to be monitored for data information.

3-31. CORE SENSING AND PREAMP LOGIC - MODULE HTT10

The switching of a core in memory causes a pulse on a sense line threaded through the core. This pulse is strobed (discriminated and converted) to a logic level of a one or zero by the core sensing and preamp logic. Three each of HTT10, 2-high modules located in slots 4, 5, and 6 of chassis F/G or H/J provide the logic for strobing the core sense lines.

Figure 3-20, bit-plane one, Y-column zero, shows the sense line as a wire threaded through the cores parallel to a Y-line, skipping three Y-lines, and entering the fourth. This pattern of threading is continued throughout the entire bit-plane and is then looped back in a manner to allow the sense line to parallel two adjacent Y-lines, skip two Y-lines and continue this pattern of threading until the senseline is returned to parallel the Y-line adjacent to the point of origin. Another sense line loop parallels the remaining Y-lines in the same manner.

Each sense line monitors one-half the cores (4096) on each bit-plane. Each sense line loop terminates at the input to a preamp circuit; there are, therefore, four preamp circuits to each sense-amp circuit. Each HTT10 module contains six sense-amp circuits representing the data output of one core each of six bit-planes.

Figure 3-21 illustrates a sense line channel for bit-plane zero; also refer to ESM 902401, Section II, BMU logic diagram, sheet 5. One of four preamp select circuits (PASL0 through PASL3) contained in the BMU ancillary logic (module WTT10, paragraph 3-32) selects the preamp circuit receiving input from a sense line loop in a group of 18 sense-amp circuits in one 8K stack. Memory data output MD00 through MD15 requires 16 sense-amp circuits and parity bit MD16 requires two sense-amp circuits (refer to paragraph 3-31.)

The output V_e from a generator/regulator circuit (module WTT10, paragraph 3-36) provides the bias voltage for the preamp circuit (-6.5V referenced to the -8.0V supply). The input to a preamp circuit is strobed, during the read half cycle, by a strobe driver circuit in the BMU ancillary logic (WTT10 module, paragraph 3-35). The strobe driver provides the input timing pulse for the strobe/reference circuit in the sense-amp circuit. The discrimination level at which the sense-amp circuit yields a one output with a differential input signal is determined by the strobe/reference circuit. A V_t voltage (0.35V from V_t regulator, paragraph 3-38) is varied to determine the value at which a one is discriminated.

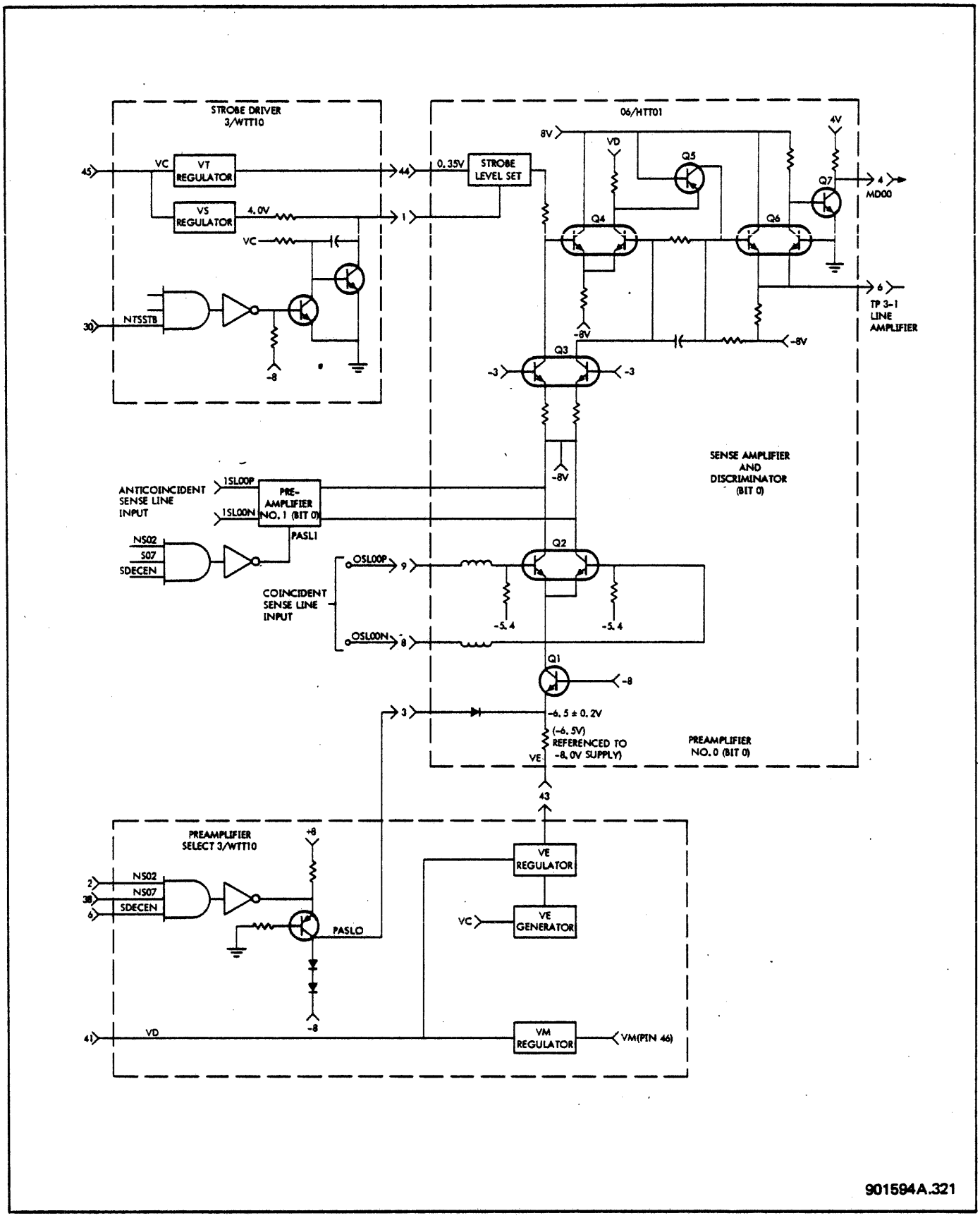


Figure 3-21. Typical Sense Line Channel for 0K - 8K – Bit 0 Shown

3-32. Parity Bit-Plane Sense Line Pattern and Channel

The parity bit-plane is divided between two 1/2-bytes, 2 and 3. Each one-half of the bit-plane is again divided into two parts, A and B as illustrated on the core diode module layout, figure 3-14. The sense line pattern and channel for parity bit-plane 16 is illustrated by figure 3-22.

A sense line enters the bit-plane and is threaded in the same manner as described in paragraph 3-30, however, unlike the other bit-planes, the sense line leaves the core diode module before it loops back to its origin. The sense line in bit-part A of one 1/2-byte is threaded into part A of the other 1/2-byte before the line makes a return loop. The same pattern prevails for bit-part B of each 1/2-byte. Bit-plane 16, therefore, requires four sense line loops instead of two, each sense-line monitoring 2024 cores. The four sense line loops require four preamp circuits per 8K, and as in the other bit-planes, there is a set of four preamp select circuits per sense-amp circuit. The output of the two sense-amp circuits are ORed prior to the logic output to provide the MD16 output.

3-33. BMU ANCILLARY LOGIC - MODULE WTT10

Module WTT10 is located in slot 3 of chassis F/G and/or H/J. This module provides miscellaneous support logic and regulated dc voltages for the core sensing and preamp logic (paragraph 3-30) as well as a threshold voltage for voltage switch (driveline) operation. The WTT10 module also provides memory protect circuits to inhibit the X and Y predrive circuits and shutdown the PT17B power supply if module cooling is interrupted or dc operating voltage levels drop below a safe level.

3-34. Sense Amplifier Support Logic

The sense-amp support logic contained in the WTT10 module consists of four pre-

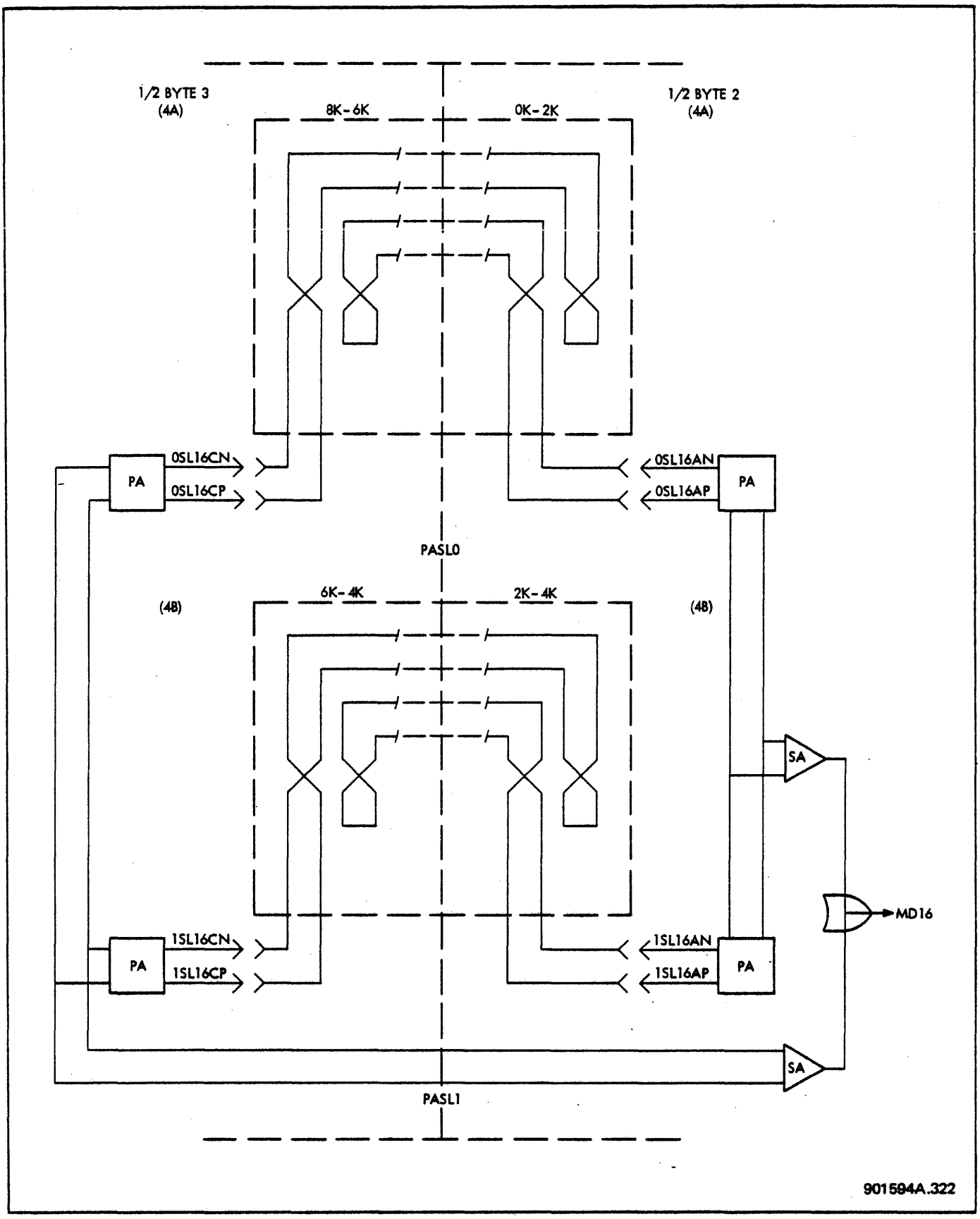


Figure 3-22. Sense Line Pattern and Channel for Bit Plane 16 (Parity) 0K - 8K

amp select circuits (PASLO - PASL3), one strobe driver (SAST), a V_t generator/regulator, a V_s regulator and a V_t regulator.

3-35. Preamp Select Circuit. Four preamp select circuits provide an address decode group which selects the appropriate preamp circuit monitoring the sense line associated with the addressed cores. Two address bits (2 and 7) and timing pulse sense-decode-enable (SDECEN) gate a preamp select circuit which turns on the appropriate preamp circuit. Preamp select terms PASLO and PASL1 turn on the preamp circuits for two sense line loops in 0-8K and terms PASL2 and PASL3 turn on the preamp circuits for two sense line loops in 8-16K. Refer to figure 3-21 for an illustration of PASLO/PASL1 input to the preamp circuit controlling bit-plane zero.

3-36. Strobe Driver Circuit. One strobe driver circuit controls the timing for all sense amplifier circuits. The term not-time-for-sense strobe (NTSSTB) from the MPM timing and control logic is held high, inhibiting sense-amp-strobe (SAST) for most of the memory cycle. At ATS180 of the read half-cycle NTSSTB goes low for approximately 160 nanoseconds. When NTSSTB drops low the strobe driver circuit is turned on and a negative going pulse (SAST) is developed. The up level of the pulse is determined by V_s (4.0V) and the lower level by V_t (0.35V). Refer to figure 3-21 and paragraph 3-30 describing the application of the strobe driver.

3-37. V_e Generator/Regulator. A V_e generator/regulator contained in the sense amplifier support logic provides a bias voltage for the preamp circuits. This bias voltage (-6.5V referenced to the -8.0V supply) tracks with temperature and has a nominal value of -14.5V at 25°C. As VD (driveline voltage) varies with temperature, V_e varies as follows:

V_D = +18.0V : V_e = 7.55 to 7.25V

V_D = +21.0V : V_e = 6.55 to 6.25V

V_D = +24.0V : V_e = 5.55 to 5.25V

Refer to figure 3-21 for an illustration of V_e application.

3-38 V_s Regulator. The V_s regulator contained in the sense amplifier support logic defines the strobe driver up-level output. V_s is nominally set at 4.0V and is adjustable; refer to Section IV for procedures.
Refer to Figure 3-21 and paragraph 3-35 for V_s application.

3-39. V_t Regulator. The V_t regulator contained in the sense amplifier support logic defines the strobe driver down-level; this voltage is adjustable, refer to Section IV for procedures. Refer to figure 3-21 and paragraph 3-30 for V_t application.

3-40. V_M Regulator

The WTT10 module contains a V_M regulator which provides the voltage for biasing the driveline voltage switches at the switch output to the core diode modules. This regulated output provides the source or sink for driveline recovery. Nominally, V_M is equal to one-half the drive voltage (V_D/2) and tracks with V_D.

3-41 Memory Protect Circuits

The BMU ancillary logic contains protect features which prevent damage to the BMU circuits when abnormal airflow, voltage or timing conditions exist. Data save is also provided when an STM (start/stop) signal is provided from the

power monitor system (paragraph 3-4) All protect circuits are located on the WTT10 module in location 03H/J or F/G. The protect circuits are the predrive disable, airflow monitor, voltage monitor and timing pulse protection. Refer to ESM 902401, Section II, BMU logic diagram, sheet 4.

3-42. Predrive Disable Circuit. The predrive disable circuit prevents memory accessing by logically grounding the predrive resistors for the driveline voltage switches. In addition to preventing data accessing, damage to the voltage switches is prevented since the drive power is eliminated. A three microsecond delay occurs before the predrive disable circuit responds to any of the following input:

a. During system power turn-on/turn-off sequence via STM signal from the power monitor system (STM occurs during ST; refer to paragraph 3-4).

b. During airflow failure, via PSSDOFP signal to the PT17B (refer to paragraph 3-5.)

c. During voltage failure via voltage monitor circuit output (refer to paragraph 3-3.)

3-43. Airflow Monitor Circuit. The airflow monitor circuit senses airflow rate and disables the PT17B power supply via a PSSDOFP signal in case of airflow failure. PSSDOFP is normally false and goes true when the monitor senses airflow failure. During turn-on/turn-off times, STM is used to override the output of the airflow monitor circuit. An STM inverter circuit clamps PSSDOFP low (false). This action prevents false tripping of the PT17B circuit breaker during times when the dc voltages drop low enough to cause an airflow failure condition.

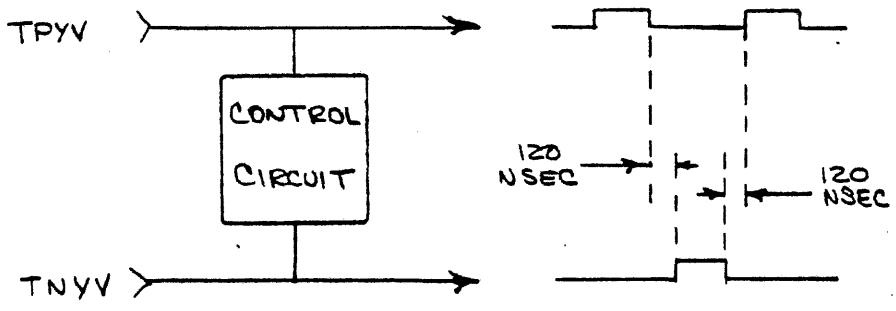
3-44. Voltage Monitor Circuit. The voltage monitor circuit senses the value of +8V, +4V, +24V and -8V supply voltages and causes the predrive disable circuit (paragraph 3-41) to activate when any of these voltages fall below limits defined by:

+8V supply	+6V
+4V supply	+3V
-8V supply	-4V
+24 supply	+20V

A failure causes a true signal to be presented to the predrive disable circuit and causes MSTAT to go true.

3-45. MSTAT. MSTAT goes true when airflow or voltage monitor circuit output is true. MSTAT can be unstable during the period of discrimination of either airflow or voltage monitor failures. After failure has been discriminated, MSTAT will be stable.

3-46. Timing Pulse Protection Circuit. Each pair of voltage switch timing pulses (TPYV/TNYV and TPXV/TNXV) are guarded against overlap by a delay latch. The action of the delay latch (for one pair of timing pulses) is illustrated as follows:



The latch ensures a space between a pair of timing pulses by establishing a delay of approximately 120 nanoseconds between the trailing edge of the preceding pulse and the leading edge of the following pulse.

SECTION IV

INSTALLATION AND VERIFICATION

4-1. INTRODUCTION

This section contains information on the installation and verification of Sigma 3 Core Memory Frame Assembly 153259 and optional assemblies and/or kits for memory expansion.

4-2. REFERENCES

Tables 4-1 and 4-2 are lists of documents, test equipment, special tools and materials required to perform the procedures described in this section. Also refer to Section VI, Illustrated Parts Breakdown and Parts Lists.

Table 4-1. Maintenance and Support Documentation

Number	Title	Use
704022 (900676)	Sigma 3 Memory Diagnostic (Medic 2/3)	Used during verification and troubleshooting Sigma 3 Core Memory, Bank B Option and Memory Port expansion installations.
705672 (901615)	Sigma 3 Multi-Port Memory Ramdom Exercisor	Used during verification and troubleshooting Sigma 3 Core Memory and Memory Port expansion installations.
902401	Engineering Support Manual Sigma 3 Core Memory	Used during verification and troubleshooting Sigma 3 Core Memory and all memory expansion options.

Table 4-2. Test Equipment, Special Tools and Materials Required

Model	Name	Use
180A	Oscilloscope Hewlet Packard	General signal verification
260	VOM, Simpson (or equivalent)	General resistance and voltage measurements
211	Precision Voltmeter Digitek	Verification of operating voltages
7230 (7140-5)	Production Tool VACO	V_s and V_t voltage adjustment in the BMU
153253	Thermometer, XDS	Verify V_d adjustment range

4-3. SIGMA 3 CORE MEMORY INSTALLATION

4-4. MEMORY FRAME ASSEMBLY 153259

Memory Frame Assembly 153259 is part of the Sigma 3 System Configuration 153253 and is shipped to the site installed in place in the system cabinet. Therefore, any installation procedures pertinent to the memory frame assembly is included in the installation instruction/control sheet for the particular system installation.

CAUTION

System power (logic, VC and VD) must be off during all removal and/or replacement procedures. Do not remove any module for at least five seconds after power is shut down due to required power supply bleed down time.

4-5. BANK B OPTION

The bank B option consists of Bank B Drive Assembly 149401 (a kit of 17 single modules of logic and 2 ribbon cables) and 8K Basic Memory Unit (BMU) Assembly 148418. Assembly 148418 contains chassis Assembly 148423 and Module Kit

Assembly 154492 containing four 2-high core diode modules, 12 X and Y-driveline and senseline modules and a module of miscellaneous supporting logic. The modules of the BMU are already installed in the chassis when received at the site.

4-6. Basic Memory Unit (BMU) 148418

To install the BMU proceed as follows:

a. Remove Basic Memory Unit Assembly 148418 from packing case and store case and packing for possible reshipment of assembly.

b. Check material received against packing list and visually inspect the unit for obvious damage; inspect backwiring board for bent pins, broken wires, etc.

c. On Memory Frame Assembly 153259, remove two ribbon cables (137481-182) extending from slots 01D to 01H and 01E to 01J,

d. Remove PT17B power supply in accordance with paragraph 5-12.

e. On the BMU, remove washers and nuts from power input studs on backwiring board and insert BMU in memory frame in rows F/G and guide power input studs through associated lugs on power bus bars.

f. Secure BMU in place using attachment hardware.

g. Replace PT17B power supply in accordance with paragraph 5-13.

h. Secure BMU power input studs to bus bars using attachment hardware removed in step e; tighten nuts sufficiently to provide proper electrical contact between BMU and power bus bars.

4-7. Bank B Drive Assembly 149401

To install Bank B Drive Assembly 149401 proceed as follows:

a. Check material received against packing list.

NOTE

while performing the following step, visually inspect modules and cables for obvious damage; broken components, etc., clean contacts, if necessary (para 5-11)

b. Install modules in assigned slots in chassis C, D, and E in accordance with slot identification provided on the internal shipping case or/module location chart in ESM 902401. Set appropriate starting address switches on ST14 module to proper configuration (refer to table 3-1 and 3-2).

c. Replace two ribbon cables removed in step 4-6c, by threading the cables through empty No. 1 slot in chassis F/G.

d. Install two new ribbon cables (137481-122 and -201) between slots 02D and 01G and slots 02E and 01F.

e. Store shipping container and packing for possible reshipment of assembly.

4-8. 8K to 16K MEMORY EXPANSION KIT 149668

Memory Expansion Kit 149668 is an assembly of two FTT13 and two FTT14 core diode modules and two RTT11 modules of driveline circuitry. Install the kit as follows:

CAUTION

Do not disassemble core diode modules. This action will void all warranties by XDS and/or the vendor. Exercise extreme care when cleaning module contacts. Do not allow cleaning material to project internally beyond contact surface.

a. Check material received against packing list.

b. Install modules in assigned slots in chassis H/J or F/G in accordance with slot identification provided on the internal shipping case or BMU module location chart in ESM 902401. Visually inspect modules for clean contacts; clean, if necessary (paragraph 5-11).

c. Store shipping container and packing for possible reshipment of assembly.

4-9 MEMORY PORT 2, 3, or 4 ASSEMBLIES

Memory Port 2 Assembly 158910 and Memory Port 4 Assembly 149404 are kits of three modules each; two FT80 (FT64) and one FT66. Memory Port 3 Assembly 149403 is a kit of seven modules, two FT80 (FT64), and one each FT66, ST14, IT13, IT24 and XT10. Install any memory port assembly kit as follows:

a. Check material received against packing list.

b. Install modules in assigned slots in chassis in accordance with slot identification provided on the internal shipping container or MPM module location chart in ESM 902401. Visually inspect modules for clean contacts; clean, if necessary (paragraph 5-11).

c. Store shipping container and packing for possible reshipment of assembly.

d. Set appropriate starting address switches on ST14 module to proper configuration (refer to table 3-1 and 3-2) and properly set the port disable switches.

4-10 SIGMA 3 CORE MEMORY INSTALLATION VERIFICATION

Verification of Sigma 3 Core Memory installation is accomplished by running diagnostic programs as well as performing certain manual checkout procedures. The diagnostic programs listed in table 4-1 are delivered in the form required by a particular site installation. Therefore, it is assumed the equipment required to run the programs is available. Special tools and test equipment required for manual checkout are listed in table 4-2. The following paragraphs describe the verification procedures for the memory frame assembly and all available options for memory expansion.

4-11. MEMORY FRAME ASSEMBLY 153259

Memory Frame Assembly 153259 is delivered to the site as part of the Sigma 3 System configuration. Therefore, verification procedures for the memory frame assembly is limited to the running of the diagnostic programs associated with Sigma 3 Core Memory in relation to the complete system. Refer to table 4-1 for the list of diagnostics and programs used at the system level. If these diagnostics cannot be run without error refer to table 5-3 for troubleshooting procedures.

4-12. BANK B OPTION

To verify the proper installation of the bank B option (assemblies 149401 and 148418) perform the following procedures:

a. With system power off, check continuity between voltage busses and ground (backwiring panel etch). Use low ohm scale on VOM to measure a typical resistance of 0.1 to 0.5 ohms. Zero indicates open contact between power stud and power bus lug; tighten associated hardware.

b. Set circuit breaker OFF on PT17B power supply and turn system power on.

NOTE

In the following step, if all ones do not appear refer to module swapping information on MPM module location chart in ESM 902401 to determine problem module. If problem cannot be determined by module swapping, isolate problem using oscilloscope and appropriate logic equations, Section I of ESM 902401. Also refer to table 5-3 for troubleshooting procedures.

c. With PT-17B power supply off, manually perform a read-from-memory. Enter any address configuration contained in bank B; except to fetch all ones.

d. Manually perform a read-from-memory cycle and increment using switch on PCP (processor control panel). Enter any address configuration contained in bank B and allow a continuous memory fetch from that address; expect all ones.

e. While performing the read-from-memory cycle, use oscilloscope and check the B timing and address lines to insure a changing state on both types of lines.

f. Use Oscilloscope at BTPXV and BTNXV input to the BMU (01G33 and 01G34) to insure no overlap of timing pulses; repeat procedure for BTPYV and BTNYV at 01G37 and 01G38.

g. Discontinue read-from-memory cycle and turn on PT17B power supply.

h. Using digital voltmeter, check PT16B output to be within the following tolerances and adjust as necessary:

+8 VDC = +8.08 to +7.92

+4 VDC = +4.04 to +3.96

-8 VDC = -7.92 to -8.08

i. Using digital voltmeter, check the following internal voltages:

VC = +24.24 to +23.76 (pin 03F45)

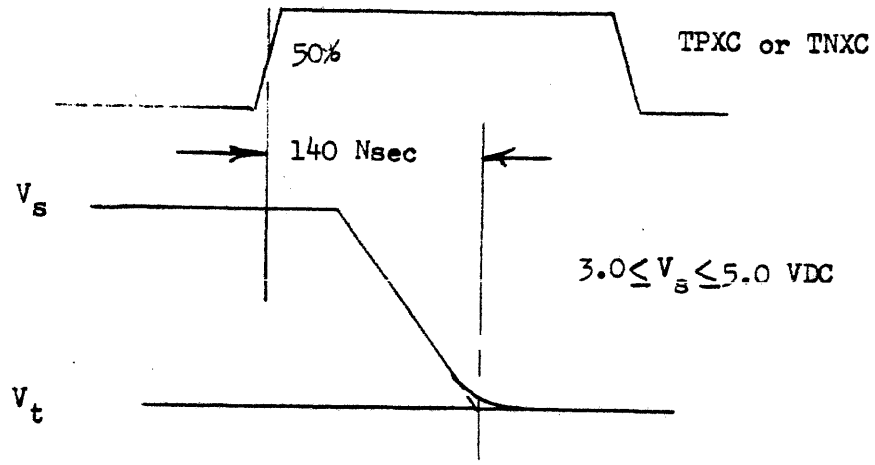
V_e = -14.4 (pin 03F18-voltage not adjustable)

V_t = +0.35 at 03F14 (use special tool 7104.5 through top hole in module WTT10 and adjust pot.

j. Manually perform a read-from-memory cycle (without incrementing. Ente any address configuration contained in Bank B and allow a continuous memory fetch from that address. V_s at 03F11 is set at +4.0 nominal; adjust V_s as follows:

1. Use oscilloscope and probe sense strobe (SAST) at 03F22 in reference to TPXC at 01G30 or TNXC at 01G31 (whichever is available at strobe time).

2. With special production tool 7104-5 (P230) adjust V_s pot (through lower hole in WTT10 module) to position the sense strobe as follows:



NOTE

In the following step, if the diagnostic fails to run over address range of interest, refer to table 5-3 for information to determine the problem.

k. Load Sigma 3 MEDIC (2/3) diagnostic 704022; set address switches to encompass the maximum area to be tested; perform test in accordance with 900676 MEDIC (2/3) program manual.

CAUTION

Do not remove any module for at least five seconds after power is shut down due to required bleed off time. Installation of modules in wrong module position may lead to module damage.

l. Perform optimum VD adjustment (paragraph 4-13).

m. Load and perform Sigma 3 MPM Random Exercisor 705672, if EIOP is installed.

n. Load and perform all appropriate diagnostics for other port users.

4-13. Optimum VD Adjustment (Schmooing)

Perform the optimum VD adjustment as follows:

a. Load MEDIC diagnostic.

b. Enter address, limits of memory area to be tested.

c. Set parity switch to HALT position.

d. Delete test 15 from program

e. With MEDIC running, perform the following:

1. With digital voltmeter at 03H41, adjust VD (very slowly) towards hig limit using VD adjust Heli-pot on PT17B, and if necessary, adjust (with production tool P230) the VCR null pot inside the PT17B (Module WT60).

2. Record value of VD (VD max) when MEDIC fails

3. Adjust VD towards low limit using VD adjust Heli-pot on PT17B and record value of VD (VD min) when MEDIC fails

4. Determine the VD limits obtained meet the requirements of figure 4-1. Note the ambient air temperature (TA) must be obtained before proper determination can be made. (Refer to table 4-2 for thermometer used.) TA must be measured adjacent to the air filter directly under the lower fan.

5. Set Heli-pot on PT17B to 5.0 and adjust VCR pot for the value determined by

$$VD = \frac{VD\ max + VD\ min}{2}$$

f. If optimum adjustment cannot be obtained, refer to paragraph 5-10.

g. Discontinue running MEDIC; remove digital voltmeter.

4-14. 8K to 16K MEMORY EXPANSION KIT 149668 INSTALLATION VERIFICATION

To verify the proper installation of the 8K to 16K memory expansion kit, perform the following procedures:

a. Turnon system power.

b. Perform procedural steps 4-12h through 4-12L.

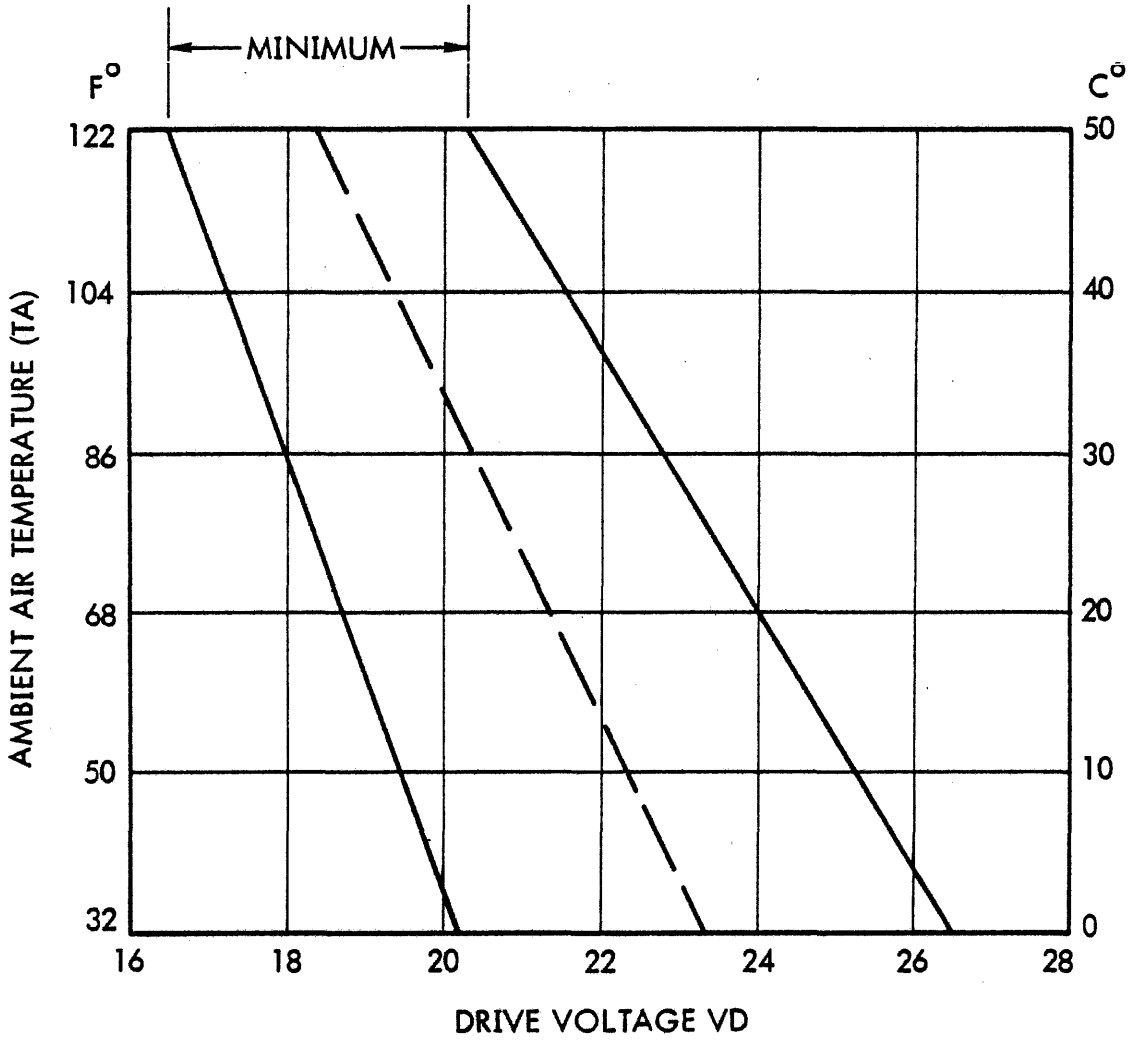


Figure 4-1. Acceptable Limits for VD as a Function of Ambient Air Temperature

SECTION V

FIELD MAINTENANCE PROCEDURES

5-1. INTRODUCTION

This section contains information on preventive and corrective maintenance necessary to support the Sigma 3 Core Memory in the field. The major portion of preventive maintenance is performed by periodically running appropriate diagnostic programs for system checkout, verifying operating voltages, and testing the airflow monitor circuit. Corrective maintenance includes troubleshooting and the replacement of faulty components.

5-2. REFERENCES

Table 5-1 is a list of maintenance support documents and special tools used to perform field maintenance on the Sigma 3 Core Memory. Refer to tables 4-1 and 4-2 for additional information and special tools required to perform procedures in this section. Also refer to Section VI, Illustrated Parts Breakdown and Parts Lists.

Table 5-1. Maintenance Support Documents, Special Tools and Materials

Number	Title	Use
705529 (901604)	Sigma 3 Memory Diagnostic-Fault Locator	To isolate malfunctions in BMU
901655	PT14B Power Supply Data Package	Troubleshoot power supply
901656	PT15B Power Supply Data Package	Troubleshoot power supply
901657	PT16B Power Supply Data Package	Troubleshoot power supply
901658	PT17B Power Supply Data Padkage	Troubleshoot power supply
155253	Thermometer, XDS	Optimum VD adjustment
#14	Sigma Tool Kit	Field repair procedures
Isopropyl	Alcohol (ASC or equivalent)	Cleaning module contacts
½ Inch	Brush (fine brass or nylon)	Cleaning module contacts

5-3. PREVENTIVE MAINTENANCE

Preventive maintenance performed on Sigma 3 Core Memory consists of procedures listed in table 5-2.

Table 5-2. Preventive Maintenance Procedures

Period	Description	Results
Daily	Visually inspect internal and external appearance of equipment	External appearance: 1. Surfaces shall be clean and free of dust. 2. Doors and panels shall close completely in reasonable alignment 3. Top of cabinet shall be free of all materials to allow freedom of air exhaust and intake. Internal appearance: 1. No clip leads or push-on-jumpers in use (unresolved and unoffical changes) 2. Cables shall be neatly dressed by sufficient ties and/or routing 3. No wire cuttings, dust, or other trash within equipment cabinet 4. All chassis and frames shall be sufficiently and properly bolted down.
Frequency determined by site conditions	Clean Air Filter	In accordance with para 5-5

Table 5-2. Preventive Maintenance Procedures, Contd.

Period	Description	Results
Every 2 weeks	Run Sigma 3 MEDIC Diagnostic (do not margin system)	All tests run without error
Quarterly	Run Sigma 3 MEDIC Diagnostic (include system margin test para 5-8)	All tests run without error
Quarterly	Perform voltage verification procedure (para 5-6)	In accordance with para 5-6
Quarterly	Perform temperature sense shutdown test (para 5-7)	In accordance with para 5-7

5-4. CLEANING

Cleaning procedures concerned with the Sigma 3 Core Memory is limited to the cleaning of the air filter located at the bottom of the memory frame assembly. Module contacts are cleaned, if necessary, when received in the field and during corrective maintenance (refer to paragraph 5-11).

5-5 Air Filter

Remove filter from lower fan assembly and shake filter over waste receptacle;

5-6 . VOLTAGE VERIFICATION

Verify operating voltages by performing the following procedures:

a. Using digital voltmeter, check PT16B output to be within the following tolerances and adjust as necessary:

+8 VDC = +8.08 to +7.92

+4 VDC = +4.04 to +3.96

-8 VDC = -7.92 to -8.08

b. Using digital voltmeter, check the following internal voltages:

VC = +24.24 to +23,76 (pin 03H45)

V_t = 0.35 (pin 03H14)

V_s = 2.0 to 5.0V (pin 03H11)

V_e = Approx. -6.4V (measured at 03H18 with respect to -8)

VD = at 03H41, nominal as determined by optimum VD adjust.

VM = at 03H46, 1/2 VD ± 1.0V

c. If correct voltages cannot be obtained, refer to paragraph 5-10.

5-7 . TEMPERATURE SENSE SHUTDOWN TEST

The airflow monitor circuit in the BMU monitors temperature of the lower memory frame blower area. Test the operation of this circuit as follows:

a. With system power on, set COMPUTE switch to IDLE

b. Disconnect power to lower memory frame blowers

c. Observe PT17B circuit breaker is tripped within 1/2 minute after blowers are disabled

d. If correct results are not obtained, refer to paragraph 5-10.

5-8. MEMORY SYSTEM MARGIN TEST

All dc output voltages from the PT16B power supply are externally adjustable to within ± 10% of the nominal output level. The adjustments are made using the three-position margin switch on the PT16B power supply. The system margin test is performed using this switch. Perform the memory system margin test as follows:

a. Load MEDIC diagnostic

b. Enter address configuration of memory area

c. Successfully run MEDIC for five minutes; rotate margin switch on PT16B power supply to HI; after five minutes rotate margin switch to LOW and allow five minutes in this position

d. Rotate margin switch back to NOM; run MEDIC for five minutes in this position

e. If MEDIC fails during steps c and d, refer to paragraph 5-10

f. Discontinue running MEDIC.

5-9 CORRECTIVE MAINTENANCE

Corrective maintenance consists of troubleshooting and repair. Troubleshooting procedures are performed as the result of running the diagnostics listed in Section IV and V, performing manual test procedures, and intermittent memory problems; these procedures are listed in table 5-3. Repair is the replacement of faulty items and the cleaning of module contacts as a result of troubleshooting. The level of field repair is outlined in table 5-3 in the probable cause/remedy column.

5-10 TROUBLESHOOTING AND REPAIR PROCEDURES

CAUTION

System power must be off during all removal and/or replacement procedures. Do not remove any module for at least five seconds after power is shut down due to the required bleed off time. Installation of modules in the

CAUTION

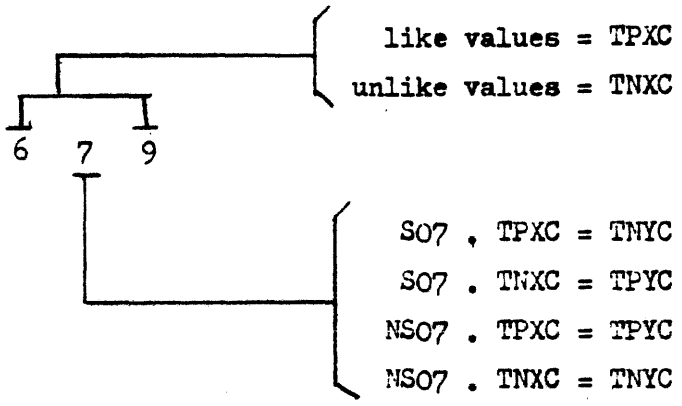
Do not disassemble core diode modules. This action will void all warranties by XDS and/or vendor.

NOTES

1. If the remedy suggested in table 5-3 fails to repair the fault, continue troubleshooting by using oscilloscope and logic equations in ESM 902401, and logic diagrams and detail descriptions of circuit operation in Section III. Also clean module contacts, if necessary, in accordance with paragraph 5-11.

2. Refer to paragraph 5-14 for typical waveform information.

3. A method to determine timing signals is to scan three address bits as follows:



Bit 7 determines the Y-current direction in relation to X-current direction. If S07 is high the Y-current is the opposite polarity of the X-current. If S07 is low (NS07) the Y-current is in the same direction as the X-current.

Table 5-3. Troubleshooting and Repair Procedures

Item	Test Procedure	Problem	Probable Cause/Remedy
1	-	Memory completely inoperative	a. External dc voltage supplies; troubleshoot PT15B, PT16B and PT17B power supplies in accordance with data packages 901656, 901657 and 901658, respectively b. Run Memory Diagnostic-Fault Locator; refer to item 13 for troubleshooting procedures c. X-voltage predrive circuits XPNVKO-3 and XNPVKO-3, RTT12 modules in slots 15 and 16; F/G or H/J; replace modules d. X-current predrive circuits XPNCKO-3, RTT11 modules in slots 8, 10, 12 and 14, F/G or M/J; replace modules e. Y-current predrive circuits YPNCO-3 and YNPC4-7, RTT10 modules in slots 7, 9, 11 and 13; F/G or H/J; replace modules f. Y-voltage predrive circuits YPNVO-3 and YNPVO-3, RTT11 modules in slots 8, 10, 12, and 14; F/G or H/J; replace modules g. Check XVPR and YVPR. If both are low the predrive is disabled. Check STM to determine if low; replace WTT10 module h. Check SAST at 03H22/03F22; check NTSSTB; check MSTAT (refer to BMU Logic Diagram, Page 1, ESM 902401, Section II); replace WTT10; replace FT66 in 16E or 18E

Table 5-3. Troubleshooting and Repair Procedures Contd.

Item	Test Procedure	Problem	Probable Cause/Remedy
			a. Check SDECEN at 03J06; replace WTT10; replace FT66 in 4J9.
2	-	INTERMITTENT PROBLEMS All memory failing	a. Refer to item 1, remedy a. b. Airflow monitor circuit; perform steps 5-7a through 5-7c; replace WTT10 module in 5J c. Timing pulses (refer to BMU Logic Diagram Page 1 ESM 902401, Section II); replace FT65 in 5E or 6E and/or FT64 in 8E or 9E
3	-	Part of memory failing	a. Address lines (refer to BMU Logic Diagram Page 1 ESM 902401, Section II); replace FT68 slots 3D, 4D, and 7D and/or 3E, 4E, and 5D b. X and Y predrive circuits; refer to item 1, remedies c through f.
4	-	Full byte (1/2-byte 0 and 1 or 2 and 3)	a. X-voltage switches; refer to figure 3-18 for appropriate switches; replace RTT12 in slots 15 and 16F/G or H/J

Table 5-3. Troubleshooting and Repair Procedures Contd.

Item	Test Procedure	Problem	Probable Cause/Remedy
			b. Inhibit timing; refer to BMU Logic Diagram, Page 1, ESM 902401, Section II); replace FT64 in 8E or 9E
5	-	Alternate 1/2-bytes (0 and 2 or 1 and 3)	X-current switches; refer to figure 3-18 for appropriate switches; replace RTT11 in slots 8, 10, 12 and 14F/G or H/J
6	-	Two adjacent bits	Y-current switches; refer to figure 3-19 for appropriate switches; replace RTT10 in slots 7, 9, 11, and 13F/G or H/J
7	-	Two alternate bits	Y-voltage switches; refer to figure 3-19 for appropriate switches; replace RTT11 in slots 12 and 14F/G or H/J
8	-	One bit, all memory	a. Sense amplifiers; refer to BMU logic diagram, page 5, Section II, ESM 902401; replace HTT10 modules in slots 4, 5, and 6 6F/G or H/J b. Data lines; refer to BMU logic diagram, page 1, ESM 902401, Section II; replace FT63 modules in slots 9C, 10C, 11C or 12C

Table 5-3. Troubleshooting and Repair Procedures Contd.

Item	Test Procedure	Problem	Probable Cause/Remedy
9	-	One bit, part of memory	a. Pre-amp select circuit; refer to BMU logic diagram, page 4, ESM 902401, Section II; replace WTT10 in slot 3F/G, or H/J b. Pre-amp circuits; refer to BMU logic diagram, page 5, ESM 902401, Section II; replace HTT10 in slots 4, 5, and 6F/G or H/J
10	-	1/2-byte or one bit, at one address	Core diode module; replace appropriate module in slots 17 through 32F/G or H/J
11	MEDIC 2/3 704022D (900676D)	Failed any test 0-15	Refer to applicable remedies for intermittent memory problems, items 2 through 10.
12	MPM Exercisor Test 705672A (901615A)	Failed any test 1-3 (after I/O operation has been verified)	a. Refer to logic diagrams in Section III b. Refer to applicable remedies for intermittent memory problems, items 2 through 10.

Table 5-3. Troubleshooting and Repairs Procedures Contd.

Item	Test Procedure	Problem	Probable Cause/Remedy
13	Fault Locator 705529B (901604B)	Failed any test	a. Troubleshoot in accordance with directions in program listing b. Refer to applicable remedies for intermittent memory problems, items 2 through 10
14	Voltage verification (para 5-6)	a. DC output of PT16B not within tolerance b. VC and VD not within tolerance c. V_t or V_s not within tolerance	a. Troubleshoot PT16B in accordance with data package 901657 b. Troubleshoot PT17B in accordance with data package 901658 c. WTT10 module in slot 3J or 3G; adjust V_t and Vs according to paragraph 4-12j; if necessary, replace module
15	Temperature Sense Shutdown Test (para 5-7)	Circuit breaker on PT17B did not trip within 1/2 minute	a. Troubleshoot PT17B in accordance with Power Supply, Model PT17B, Assy. No. 148806, Power Supply data package 901658 b. WTT10 module in slot 3J; replace module
16	Memory System Margin Test (para 5-6	a. MEDIC failed during HI b. MEDIC failed during LOW	a. Voltage sensitive module; isolate module; replace module in MPM or BMU b. Voltage sensitive module; isolate module; replace module in MPM or BMU

Table 5-3. Troubleshooting and Repair Procedures Cont.

Item	Test Procedure	Problem	Probable Cause/Remedy
17	Optimum VD Adjustment (para 4-3a)	Optimum VD adjust cannot be made	a. Refer to applicable remedies for intermittent memory problems, items 2 through 10 b. Troubleshoot PT178 in accordance with data package 901658

5-11 CLEANING MODULE CONTACTS

> Exercise extreme care when cleaning Core Diode Modules (CDM). Do not allow cleaning material to project internally beyond contact surface.

a. Brush module contacts with alcohol (table 5-1) until clean. Remove residue with additional alcohol.

5-12 PT17B POWER SUPPLY 148806 REMOVAL

Remove PT17B power supply as follows:

a. Disconnect power supply output lines (3) from bus bar

b. Disconnect blower cable connectors (2)

c. Disconnect memory-sense cable connector

d. Disconnect power input cables (2) from system power distribution box

e. Remove cable ties on power supply which dress signal cables to side of memory frame

f. At bottom of power supply, remove air filter and loosen power supply mounting screws, utilizing screwdriver clearance slots provided at bottom of power supply

g. At top of power supply, remove power supply mounting hardware and lift power supply from frame

5-13 PT17B POWER SUPPLY 148806 REPLACEMENT

Replace PT17B power supply as follows:

a. If required, remove PT17B power supply from shipping container; store container and packing for possible reshipment of unit.

b. If necessary, remove air filter from bottom of power supply

c. On memory frame assembly, install power supply by sliding slotted bracket of power supply over loosened mounting screws; do not tighten screws

d. At top of power supply, install mounting hardware and engage top mounting screws sufficiently to hold power supply; do not tighten screws

e. Connect power supply output lines (3) to bus bar; tighten for proper electrical contact.

f. Connect blower cable connectors (2) and memory-sense cable connector to power supply; connect power input cables (2) from power supply to system power distribution box

g. Tighten power supply mounting screws at top and bottom; replace air filter at bottom of power supply.

h. Install cable ties on signal cables; dress cables to the left side of the memory frame providing sufficient clearance for module removal and replacement; secure cable ties to power supply case.

5-14. WAVEFORMS

This paragraph contains analysis of illustrated waveform patterns which will be encountered during troubleshooting procedures. Reactive components in the memory circuits, or a poor grounding technique of a scope probe, will tend to produce distortion in waveform pattern. Therefore, the following information is included to aid in the discrimination of acceptable waveforms. Refer to figure 5-1.

a. Waveform Group No. 1. The read-half cycle timing pulse (RHC) is used to sync the patterns in the waveform group No. 1. The areas of importance are 1 through 4 and are described as follows:

1. Linear amplifier output; negative excursion indicates the reading out of a one.

2. Distortion created by X and Y-driveline switches turning off (positive distortion), on (negative) and off again.

3. This positive excursion indicates a one is being written into the addressed core.

4. A memory cycle (both read and write half-cycles).

Note

SDECEN occurs near the beginning of each memory cycle.

b. Waveform Group No. 2. The RHC timing pulse is also used to sync the patterns shown in waveform group No. 2. The areas of importance are 1 through 3 and are described as follows:

1. Linear amplifier output; negative excursion indicates the reading out of a zero. (Note: This excursion is smaller in amplitude than the excursion for one in the previous waveform pattern.)

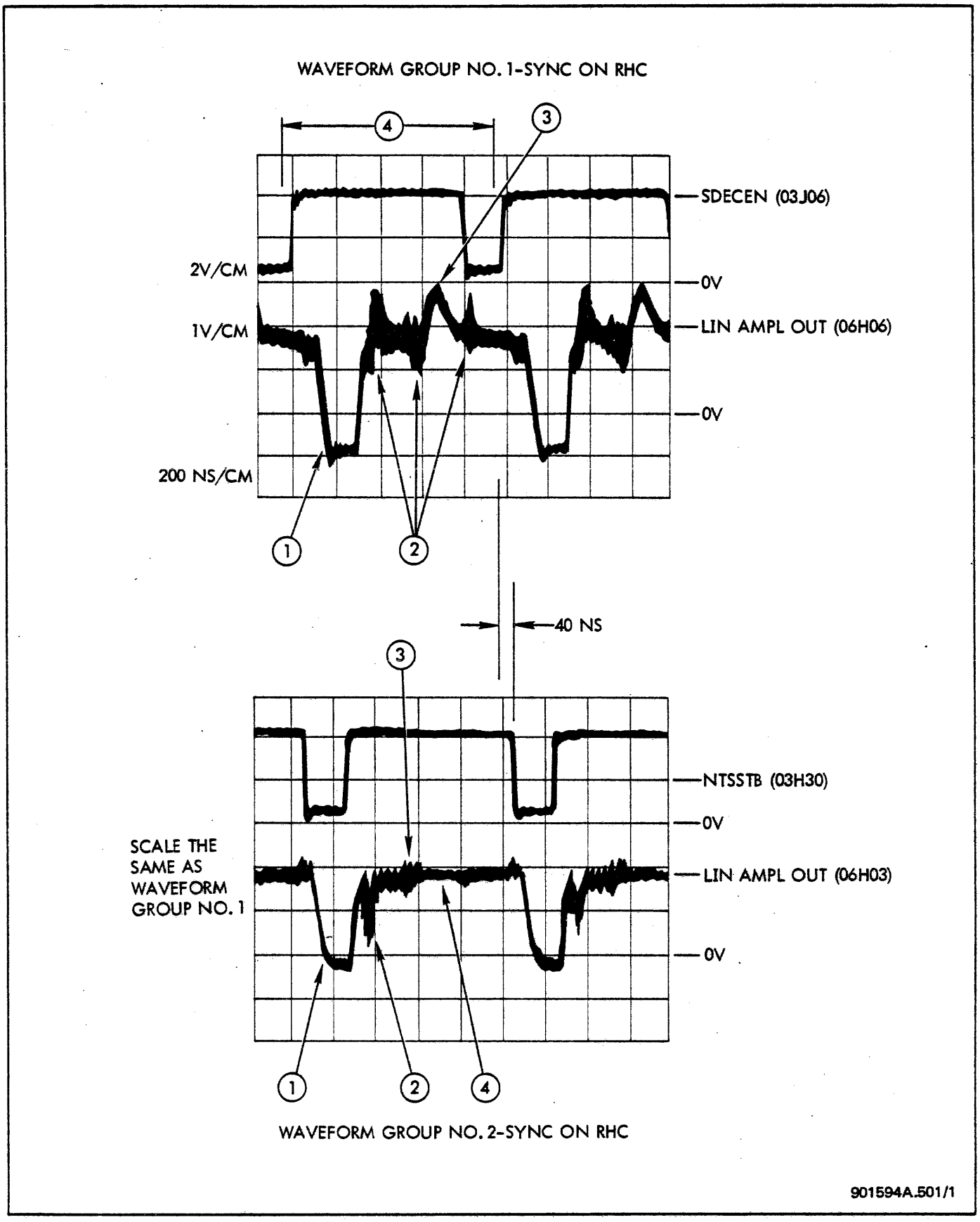


Figure 5-1. BMU Waveforms (Sheet 1 of 10)

2. Negative distortion created by X and Y-driveline switches turning off.(Note: This distortion is of opposite polarity to the distortion of the switches turning off in Group No. 1. If the negative amplitude does not extend beyond the negative level of the Strobe 1, it is normal. If for some reason the negative distortion extends beyond Strobe 1, the sense amplifier would output a short pulse which might be strobed into the memory information register (M-register) as a one.)

3. Distortion caused by X and Y-driveline switches being set up for the write portion of the memory cycle. Note: NTSSTB drops low (initiating SAST for strobing) approximately 40 nanoseconds after SDECEN goes high.

4. A zero is being written into this core. Compare to 3 of group 1.

c. Waveform Group No. 3. The timing pulse TPXC is used to sync the patterns shown in waveform group No. 3, many addresses are being cycled. The areas of importance are 1 through 6 and are described as follows:

1 and 2. Linear amplifier output for ones and zeros; 1 = a one and 2 = a zero.

3 and 4. Indicates the writing in of a zero, 3 and a one 4.

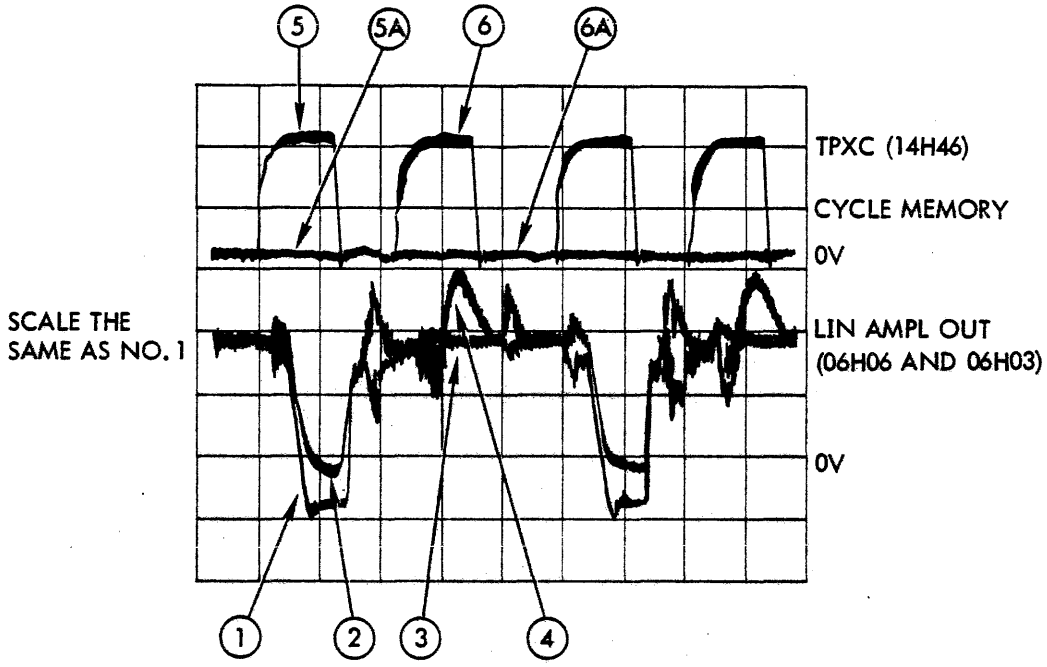
5. Timing pulse TPXC during read, at one address.

5a. Timing pulse NTPXC during read at a different address.

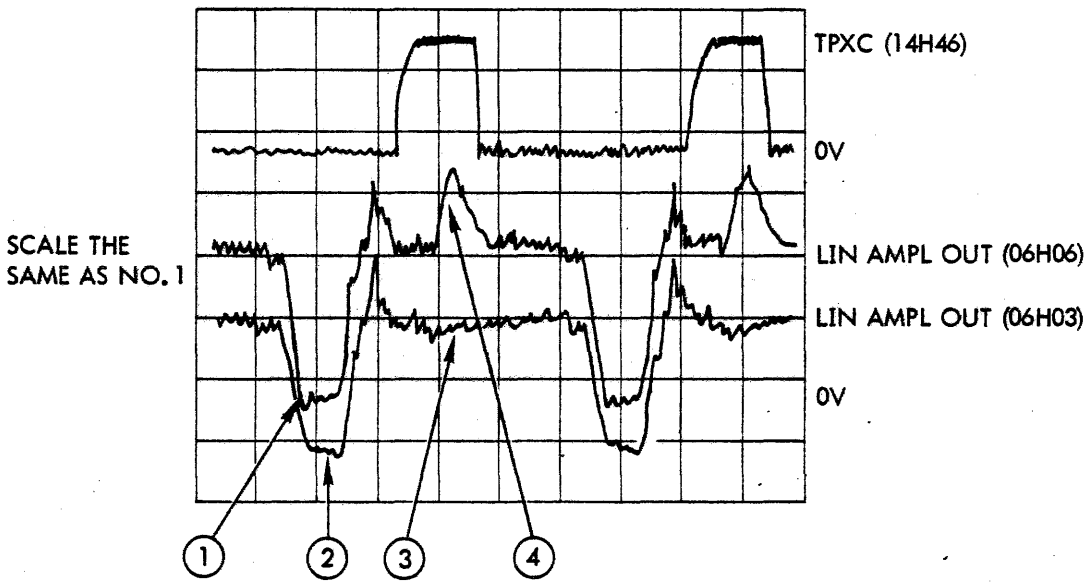
6. Timing pulse TPXC during write, at the same address as 5.

6a. Timing pulse NTPXC during write at a different address. Note: The delay between TPXC and the X and Y switch turnon (distortion prior to strobe 1 or 2) is due to the predrive and driveline switch delays. The delay from TPXC turnoff to switch turnoff is also due to the same condition in the switches.

d. Waveform Group No. 4. Timing pulse TPXC is also used to sync the waveform patterns in group No. 4. The patterns represent one address being cycled. TPXC appears during the write portion and the linear amplifiers output have different ground reference levels for wave separation. Areas 1 through 4 are described in waveform 3 analysis.



WAVEFORM GROUP NO. 3 - SYNC ON TPXC



WAVEFORM GROUP NO. 4-SYNC ON TPXC

901594A.501/2

Figure 5-1. BMU Waveforms (Sheet 2 of 10)

e. Waveform Group No. 5

Timing pulse TPYI/TNYI is used to sync the waveform pattern of group No. 5. The areas of interest are 1 through4. and are described as follows:

1. Width of drive voltage pulse measured at 0001YPR positive inhibit switch circuit output during a write-zero; VD is the quiescent voltage level.

2. Width of drive voltage pulse measured at 0001YPR positive inhibit switch circuit output during a write-one; VD is the quiescent voltage level.

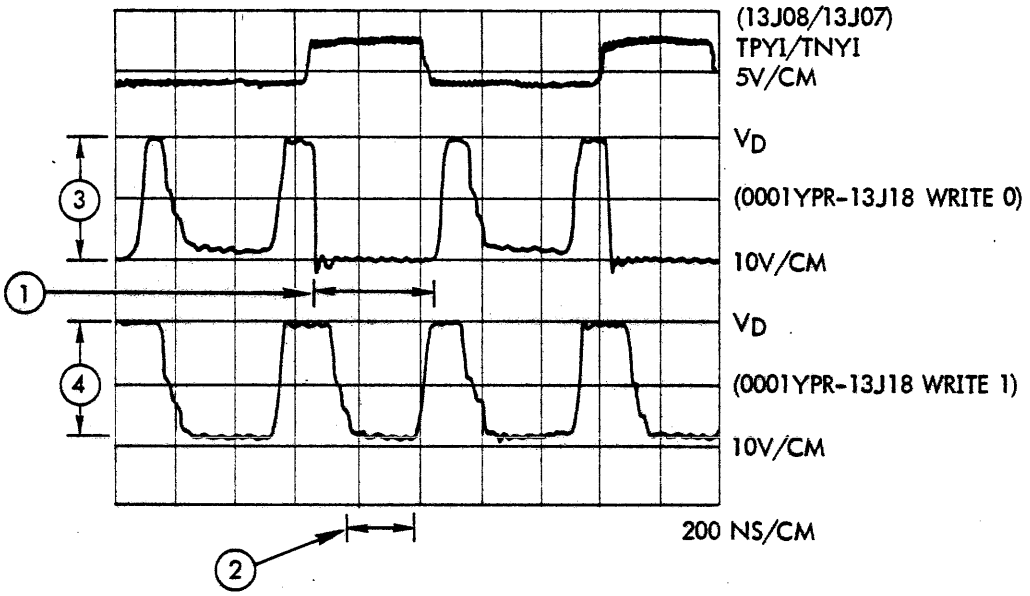
3. Amplitude of drive voltage during write-zero.

4. Amplitude of drive voltage during write-one.

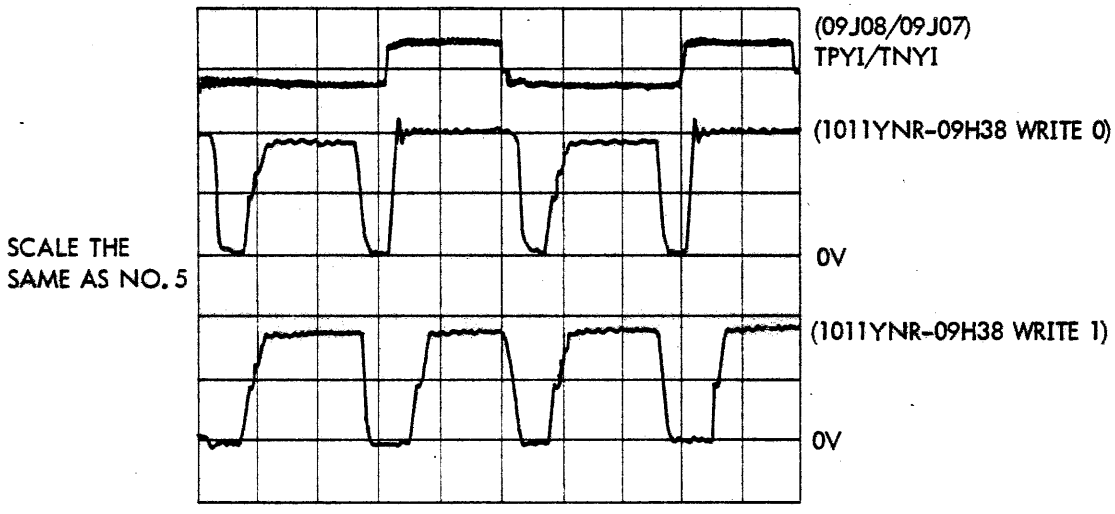
Note: The difference in pulse width between 1 and 2 is due to the inhibit switch turning on in the writing of a zero. Also timing pulse TPYI/TYNI is a wider pulse than TPYV or TPYC used during the writing of a one. The difference in amplitude between 3 and 4 is due to the different paths to ground for both currents. In 3 the inhibit switch, switches directly to groung and in 4 the drive current from the Y-current switch is completed to ground through the Y-current switch, driveline diode, core, and finally the Y-voltage switch which sinks the current.

f. Waveform Group No. 6. Timing pulse TPYI/TNYI is also used to sync the waveform patterns of group No. 6. These waveforms are identical to group No. 5 with the exception that the patterns are of the output of a negative inhibit switch and the 1011YNR quiescent voltage is zero.

g. Waveform Group No. 7. This waveform diagram is the waveform diagram of No. 6 with the drive voltage pulses for a zero and one superimposed to convey the differences in pulse width and amplitude. Bits 10 and 11 are different, one is a zero and the other a one.



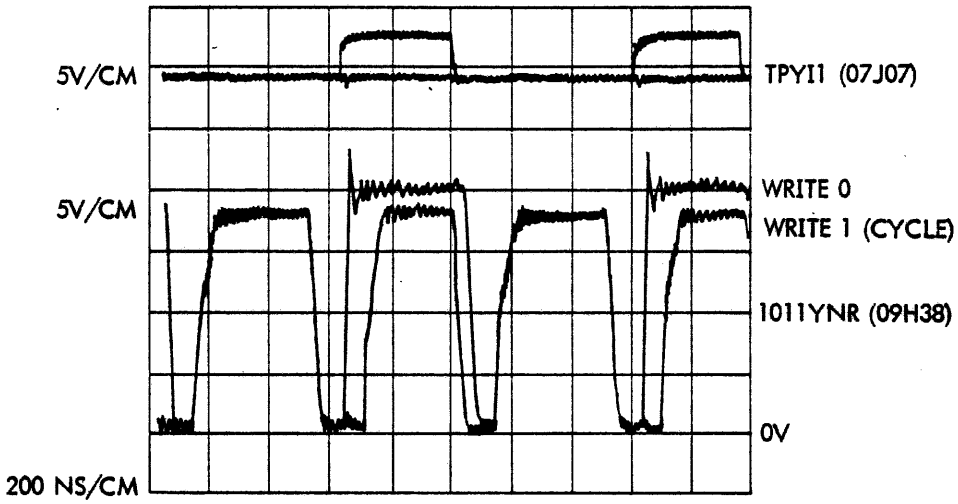
WAVEFORM GROUP NO. 5



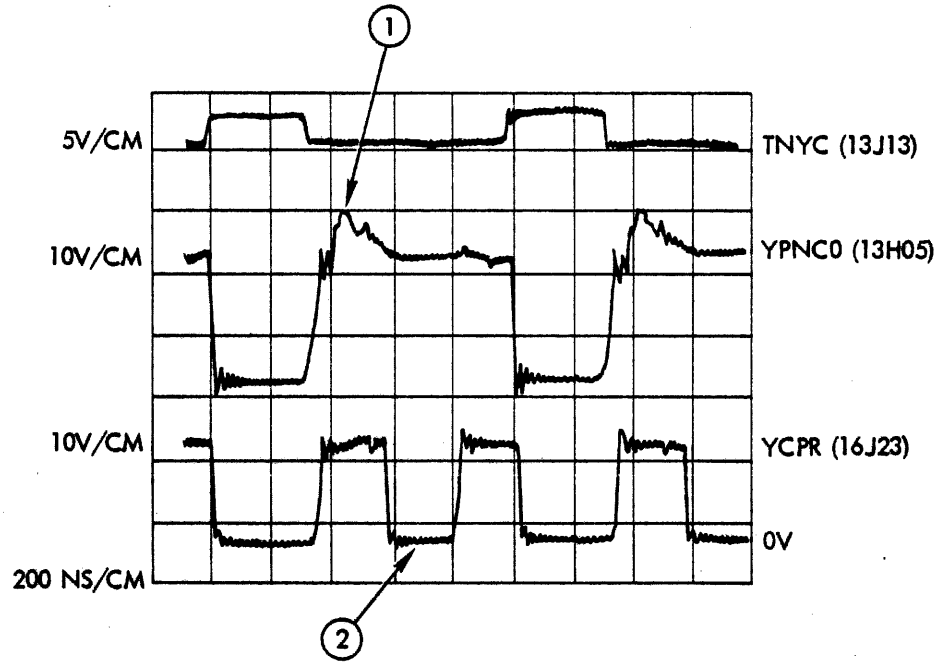
WAVEFORM GROUP NO. 6

901594A.501/3

Figure 5-1. BMU Waveforms (Sheet 3 of 10)



WAVEFORM GROUP NO. 7



WAVEFORM GROUP NO. 8

901594A.501/4

Figure 5-1. BMU Waveforms (Sheet 4 of 10)

h. Waveform Group No. 8. Timing pulse TYNC is used to sync the waveform patterns of group No. 8. Area 1 and 2 are described as follows:

1. This positive excursion is normal and is due to YC predrive line discharging.

2. YCPR drops to zero again during the write half-cycle with timing pulse TPYC (not shown) and a complement Y-current predrive address.

i. Waveform Group No. 9. Timing pulse TPYC or TNYC is used to sync waveform group No. 9. The areas of interest are 1 through 4 and are described as follows:

1. Time of interest (TYC during write zeros - inhibit switch is on)

2. Disregard excursions during this period as no useful work is being performed by this YC switch.

3. YC7N is normally recovered to approximately Vm; the negative spike which follows is due to the positive voltage switch turning on.

4. This spike due to voltage switch turning off.

Note: Trace three (YCOP) is for a positive YC switch and is approximately an inverse of trace two which is for a negative YC switch. Trace two and three show line fluctuations as a result one switch turning on. No useful work was accomplished since the time was for a write-zero.

j. Waveform Group No. 10. This waveform group is for the same set of circumstances as group 9 except a one is being written. The areas of interest are 1 and 2 and are described as follows:

1. At TYC time the YC7N switch turned on slightly ahead of the negative voltage switch and caused the first spike; the second spike is caused by YCOP switch turning off slightly before the voltage switch.

2. This long recovery curve is normal for any YC switch and occurs during the time when useful work is not being performed by this YC switch.

Note: If a Y-line has no noise or spikes, etc., it may be shorted to ground orVD.

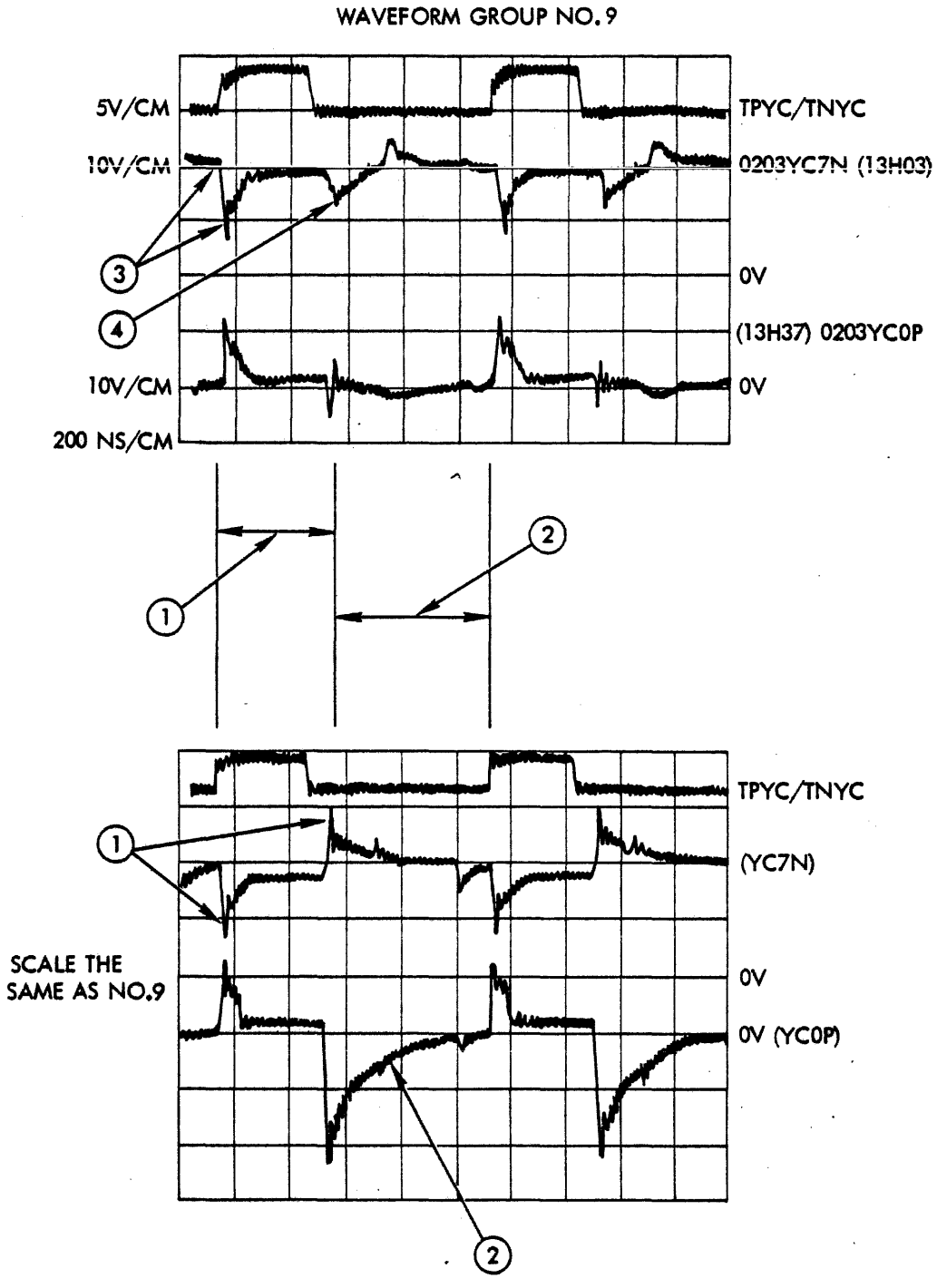


Figure 5-1. BMU Waveforms (Sheet 5 of 10)

k. Waveform Group No. 11. Timing pulse TPYV (during write) is used to sync the waveform pattern in Group No. 11. These areas of importance are 1 through 3 and are described as follows:

1. YVPR responds to both half portions (read and write) of the memory cycle. These areas show VC during read (1st negative excursion - longer duration) and write (2nd negative excursion - shorter duration). The difference in duration is due to the YV predrive being turned on longer during the read cycle.

2. This negative excursion is predrive switch turnon.

3. This positive spike is caused by the inductive discharge (kickback) of the predrive line; this is normal and will vary in amplitude on different lines.

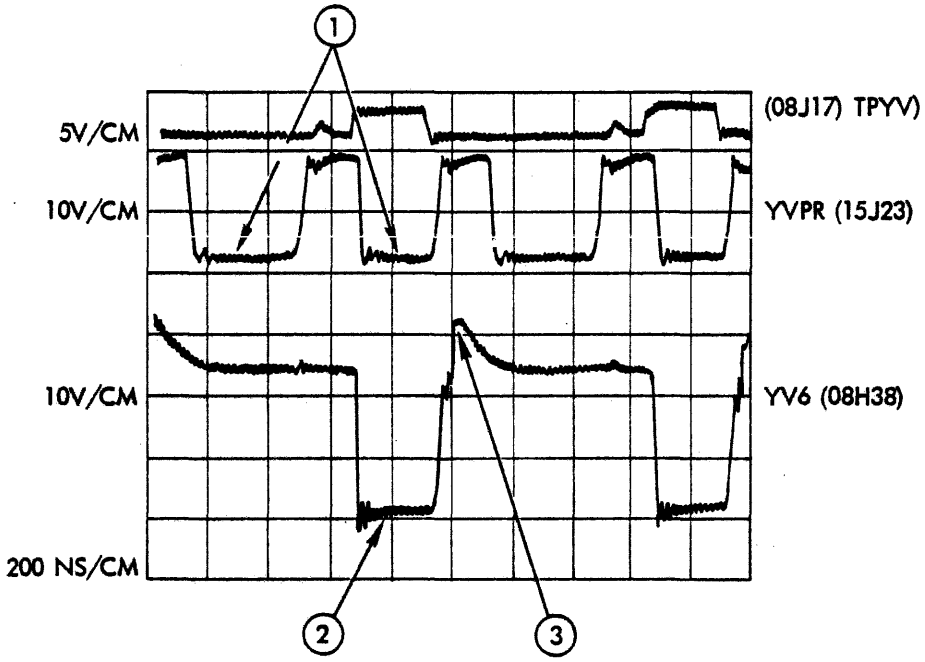
l. Waveform Group No. 12. This waveform shows a Y-voltage switch output in relation to timing pulses TPYV and TNYV. The areas of importance are 1 through 5 and are described as follows:

1. Note the longer timing pulse (TNYV) during the read portion of the cycle; this allows for longer ontime for voltage switch during read.

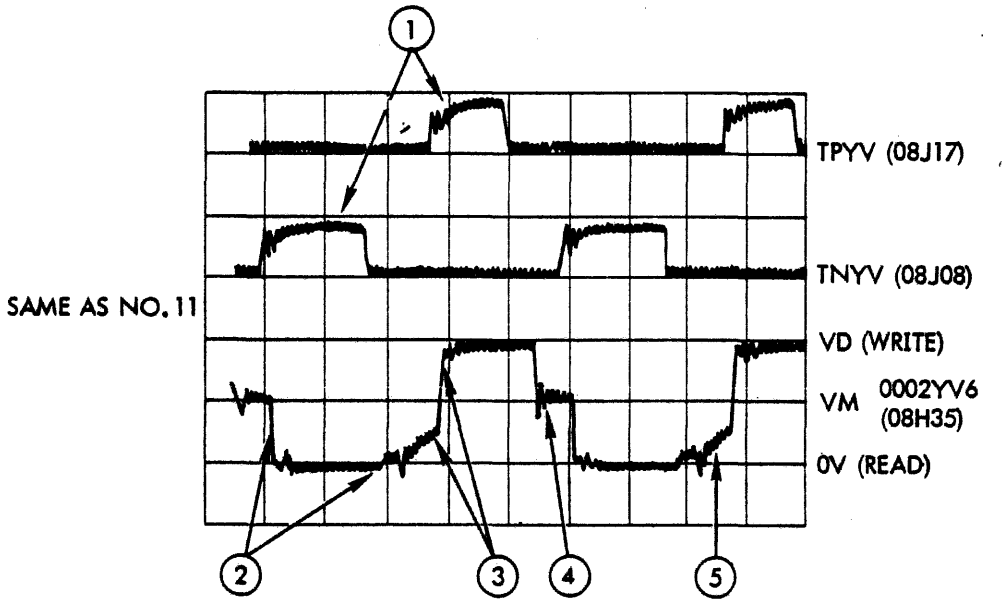
2. This slight delay in voltage switch turnon and turnoff is normal, however, the delay at turnoff must not be excessive (extend into the write portion of the memory cycle.)

3. Normal recovery to the direction of Vm. The voltage does not quite reach Vm, however, before the switch goes positive (during write) and forces it to VD.

4. Rapid recovery to Vm after write may or may not occur (see 3 of group 13). Note: Either recovery pattern (4 or 5) can occur after read or write and both are acceptable. The important facts in waveform group No. 12 are that the voltage switch switched from Vm to ground, recovered to Vm and switched from Vm to VD as directed by the timing pulses, and made proper recoveries between cycle and half cycles.



WAVEFORM GROUP NO. 11



WAVEFORM GROUP NO. 12

901594A.501/6

Figure 5-1. BMU Waveforms (Sheet 6 of 10)

m. Waveform Group No. 13. Timing pulse TPYV or TNYV is used to sync these waveform patterns. The areas of interest are 1 through 3 and are described as follows:

1. YVPR properly switches from VC to ground at turnon time. (This pattern is made while memory is being cycled.)

2. All predrive lines but one are turning off together; one is slower in turning off, this predrive switch should be replaced (refer to waveform group No. 14 for further analysis).

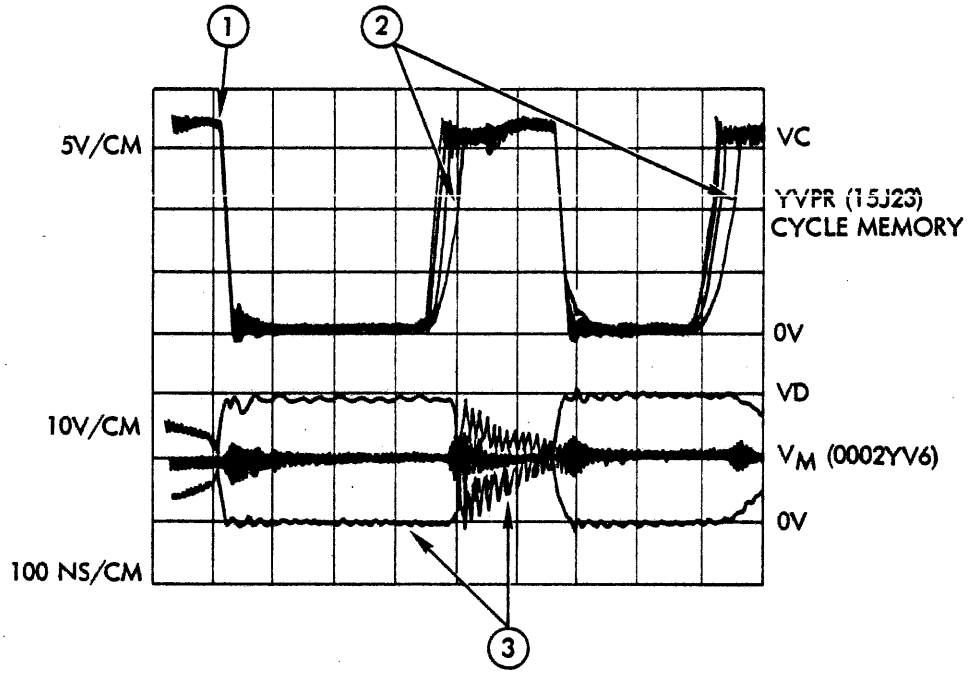
3. Proper output and recovery pattern (during read and write) from 0002YV6 voltage switch (output from a good voltage switch, i.e., not a voltage switch driven by the bad predrive line).

n. Waveform Group No. 14. The same set of conditions prevail for these patterns as for No. 13. The areas of interest are 1 and 2 and are described as follows:

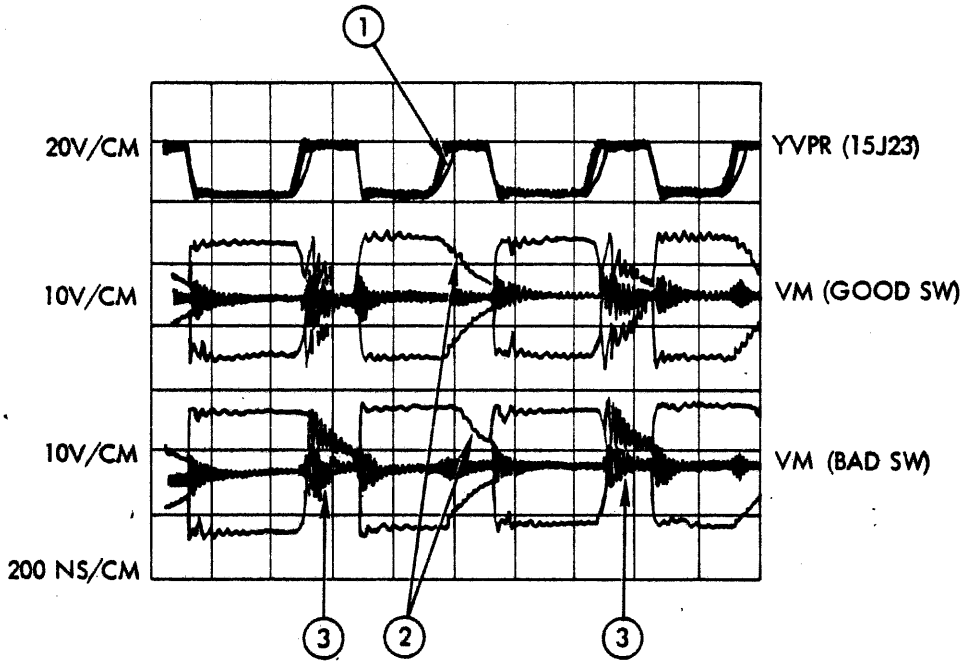
1. This is the defective Y voltage predrive line described in waveform pattern No. 13.

2. Note the extended ontime of the voltage switch. This is due to the predrive being on for a longer duration.

3. Note the recovery area of the waveform from the defective voltage switch. The positive side always recovers much later than that shown in the above waveform (good switch) and the recovery on the negative side is damped. This group illustrates a condition which may result in an intermittent memory failure due to decreased recovery time.



WAVEFORM GROUP NO. 13



WAVEFORM GROUP NO. 14

901594A.501/7

Figure 5-1. BMU Waveforms (Sheet 7 of 10)

o. Waveform Group No. 15. Timing pulse TPXC is used to sync waveform Group No. 15. The areas of importance are 1 through 3 and are described as follows:

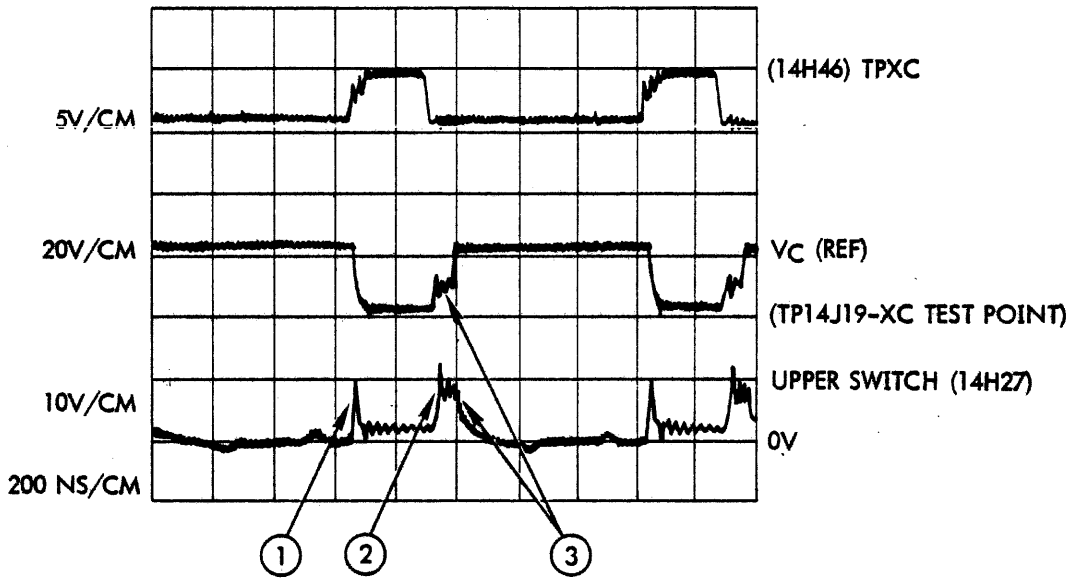
1. This positive spike at turnon time on trace three is due to the inductance in the predrive line and is normal. Trace three is the output at 14H27 of the positive predrive switch at the upper end of the 4X4 X-current switch matrix.

2. This positive spike at turnoff time is caused by the switch at the lower end of the switch matrix turning off first; this is also normal.

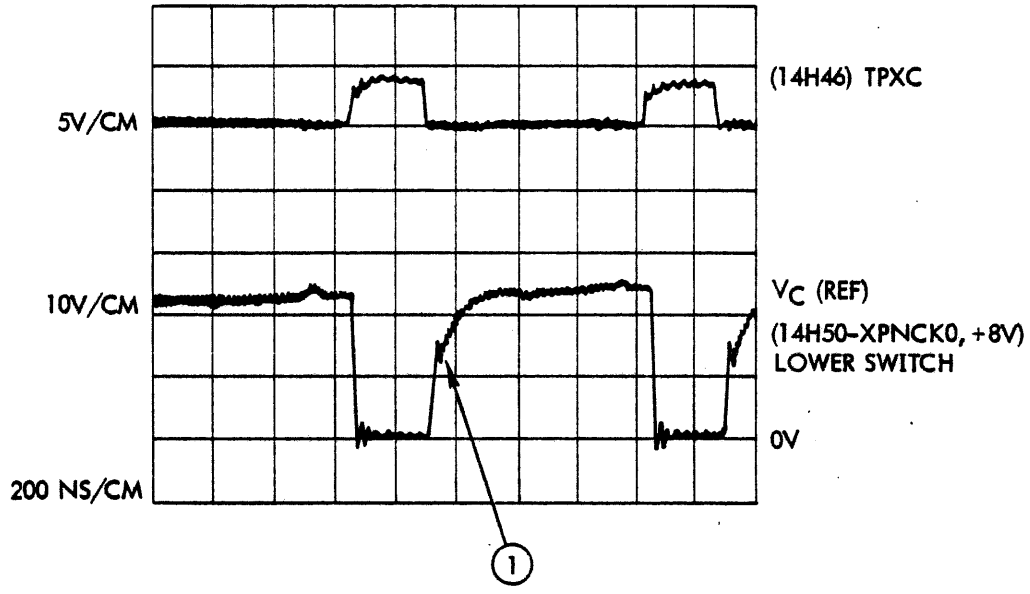
3. This indicates a momentary recovery to the value of the predrive switch emitter bias (+8V) when the lower switch turns off. The return to ground occurs when the upper switch turns off.

Note: Trace two is the result of current through the predrive resistor and indicates the predrive switches turned on.

p. Waveform Group No. 16. The same timing pulse used in group No. 15 is used to sync group No. 16. Trace two is the output at 14H50(XPNCKO) of the switch at the lower end of the switch matrix described in the analysis of waveform group No. 15. Trace two shows the switch turned on and off properly during the timing pulse. The recovery after turnoff is quick due to the fact that the upper switch is still on as described in step 2 of waveform analysis No. 15. However, after the predrive emitter bias diode turns off at +8V (step 3 of No. 15) the recovery is slower (1); this is normal.



WAVEFORM GROUP NO. 15



WAVEFORM GROUP NO. 16

901594A.501/8

Figure 5-1. BMU Waveforms (Sheet 8 of 10)

q. Waveform Group No. 17. Timing pulse TPXC is used to sync the waveform group No. 17. Refer to groups 15 and 16. Trace three of No. 15 is the output of an addressed upper predrive switch. Trace two of No. 17 is the output of an unaddressed upper switch; this trace is / from a point which is not selected to carry current for the addressed lower switch, which is trace three of no. 17. The noise and spikes of trace two are caused by electrical coupling between a selected predrive line and the unselected predrive line. These are normal distortions which are not of interest since very little current flows. therefore, XC switches on this unaddressed XC predrive line will not turn on.

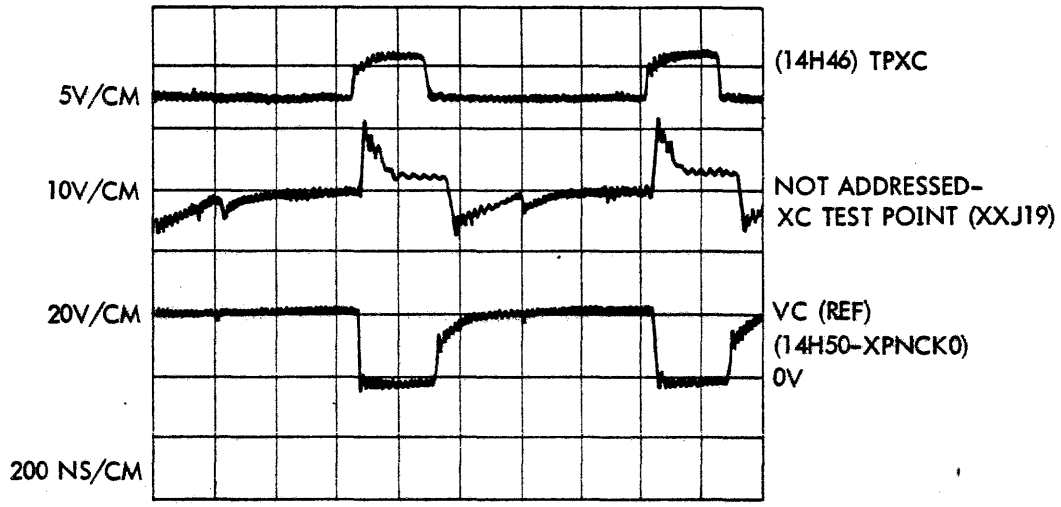
r. Waveform Group No. 18. Timing pulse TPXV is used to sync waveform No. 18. The memory is being cycled and the group of waveforms illustrate almost ideal results of switching. Trace two is the XV predrive resistor waveform. Trace three is the output of a voltage switch during a memory cycle. Note area No. 1; the group of lines at turnoff time for XVPR illustrate several switches on the same line of the 4X4 voltage switch matrix, are turning off and have similar turnoff characteristics (i.e., none are too slow).

s. Waveform Group No. 19. Timing pulse TPXV is used to sync waveform group No. 19. The waveforms in this group are similar to those in group No. 18 except that the memory is being cycled on only one address. This group is included to illustrate another acceptable configuration of the conditions shown in group No. 18. The areas of interest are 1 through 3 and are described as follows:

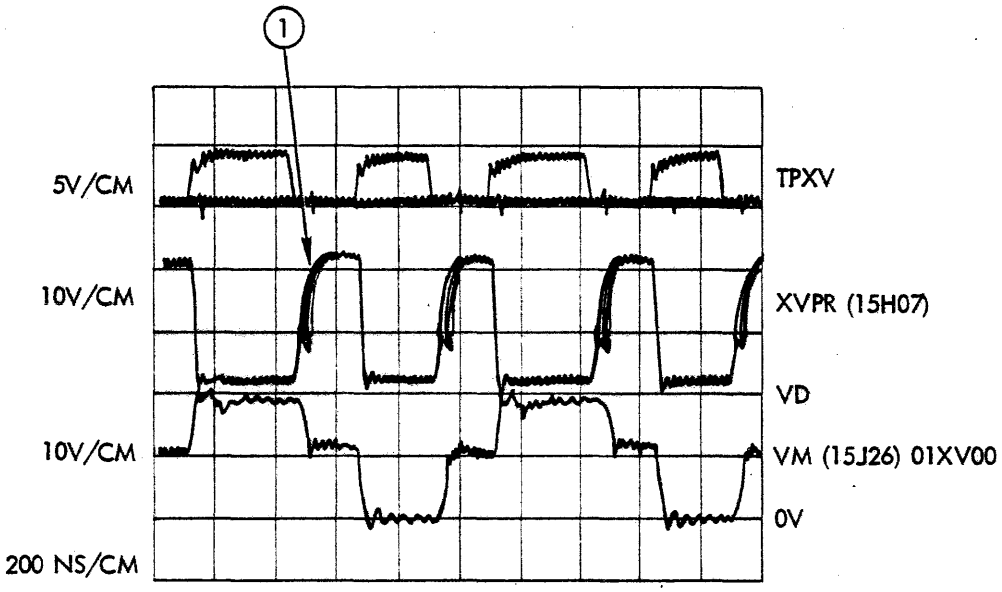
1. The first excursion is negative during read (as opposed to the line positive in group No. 18); the switch turned on and/dropped immediately to ground and recovered to a value slightly above ground when the X-current switch turned on.

2. At switch turnoff, an inductive overshoot occurs and the line recovers to near Vm.

3. The write portion is uneventful until recovery time at turnoff; the voltage switch line recovers very slowly and is eventually driven past Vm to ground when the switch goes negative again during read of the next cycle. Note: Although the overall action of the voltage switch shown in this group differ from the one in group No. 18, the action is considered normal.



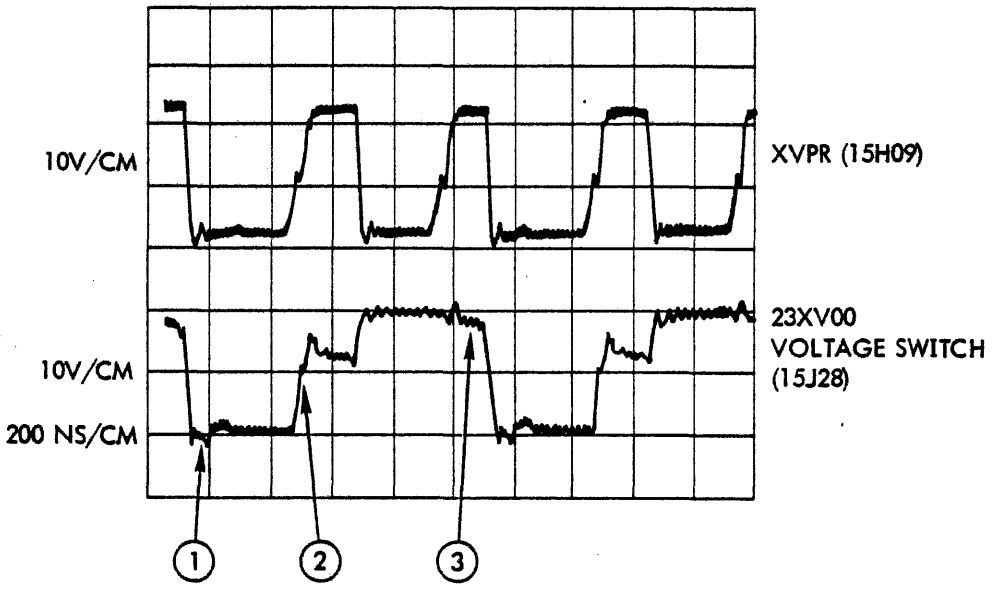
WAVEFORM GROUP NO. 17



WAVEFORM GROUP NO. 18

901594A.501/9

Figure 5-1. BMU Waveforms (Sheet 9 of 10)



WAVEFORM GROUP NO. 19

901594A.501/10

Figure 5-1. BMU Waveforms (Sheet 10 of 10)

SECTION VI
ILLUSTRATED PARTS BREAKDOWN

6-1 GROUP ASSEMBLY PARTS LIST

The Group Assembly Parts List is a breakdown of all systems, assemblies, and subassemblies which can be disassembled, reassembled, or replaced and which are contained in the end article. The Group Assembly Parts List consists of columnar listings of parts related to illustrations. Parts are listed in order of disassembly sequence, except in cases where sequence of disassembly cannot be maintained. Attaching parts are listed below the related assembly or subassemblies. Items which are purchased in bulk form (for example, wire and insulating materials) are not listed.

Each parts list table is arranged in seven columns as follows:

a. The figure number of the part listed and the index number corresponding to the illustration reference

b. The XDS manufacturer's part number for the part

c. The vendor's part number for the part (if available)

d. A brief description of the part

e. The manufacturer's code for the part

f. The quantity of the part used per assembly

g. Usable on code column indicating that when a letter is used in the code column, the use of the coded part is restricted to the model identified by the code letter.

(Where no letter symbol appears in this column, the part is used on all models of this configuration.)

How to use the Illustrated Parts Breakdown.

To obtain information about a part, the following steps should be taken:

a. Refer to the applicable assembly breakdown.

b. Compare the part with the illustration until part is located.

c. Note the index number.

d. Locate the index number in the corresponding Group Assembly Parts List.

e. Find the part number and name of part opposite the index number listed.

6-2 NUMERICAL INDEX

This index is a listing of the items contained in the Group Assembly Parts List. The numerical order of the index (table 6-8) is determined by the XDS part number.

ILLUSTRATED PARTS BREAKDOWN CONTENTS

Note: Model Numbers with dash numbers called out in the Usable on Code Column are for internal reference only and should not be confused with Basic Model Numbers.

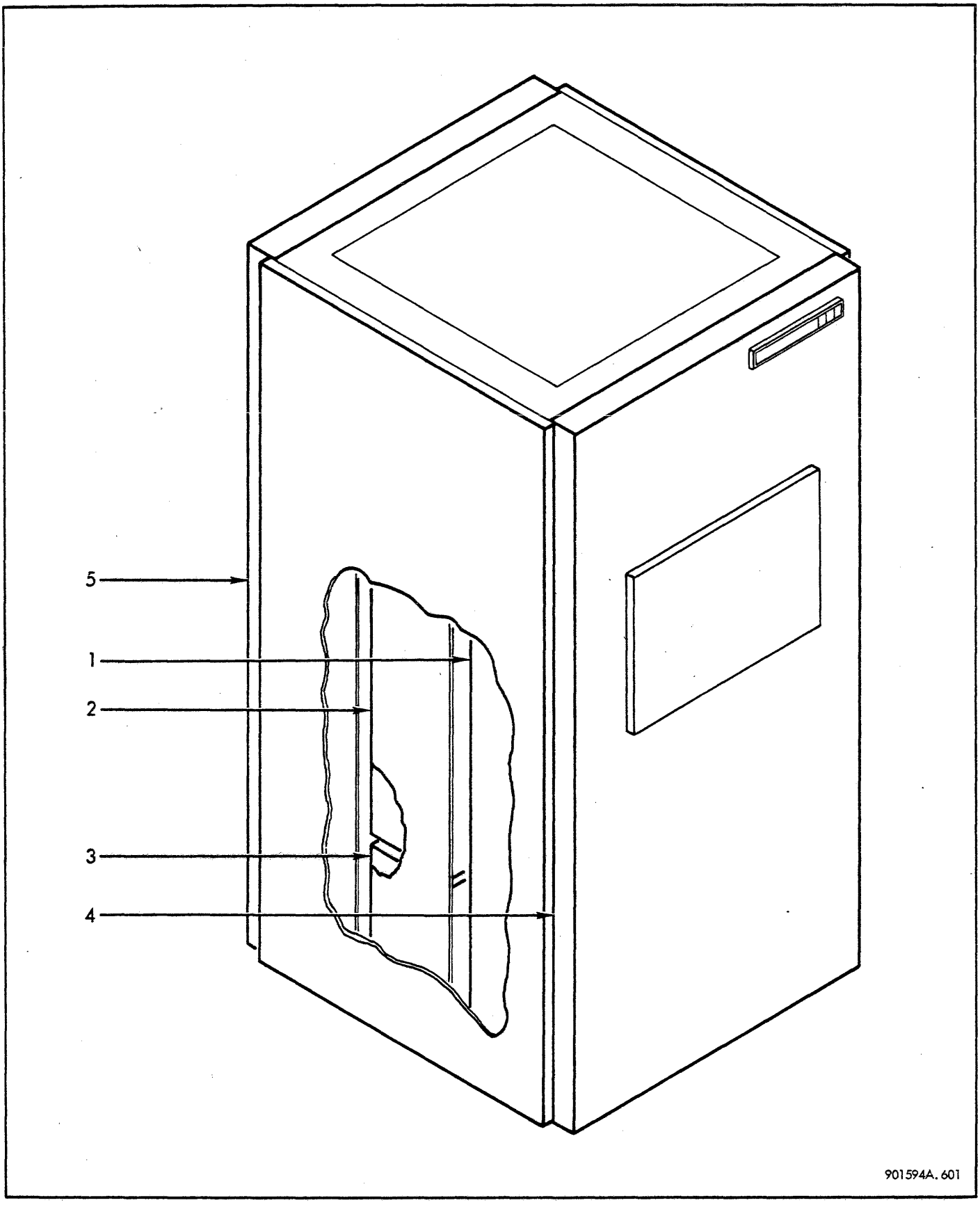


Figure 6-1. Sigma 3 Core Memory (Model 8151)

Table 6-1. Sigma 3 Core Memory (Model 8151)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-1-			Sigma 3 Core Memory (Model 8151)	XDS		8151
-1	153259D		Sigma 3 Memory-Frame Assy	XDS	1	
-	139204G		Hardware Kit Assy, Front Frame	XDS	1	
-2	148586		CPU Frame Assy	XDS	REF	
-3	148557		EIOP Assy	XDS	REF	
-4	148721		PCP Door Assy	XDS	REF	
-5	131416		Basic Cabinet Assy	XDS	REF	

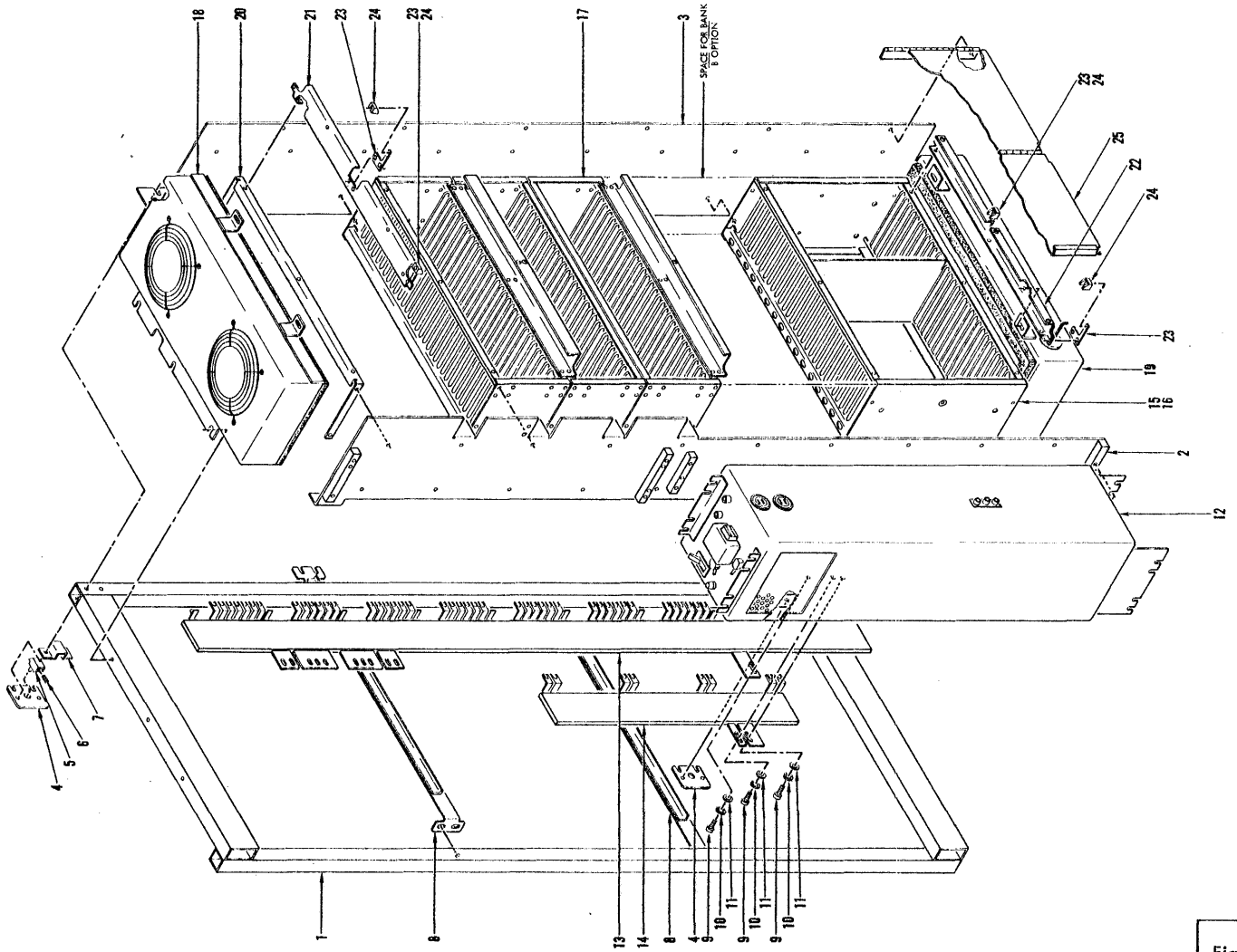


Figure 6-2. Sigma 3 Memory Frame Assembly

901594A. 602

Table 6-2. Sigma 3 Memory Frame Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-2-	153259D		Sigma 3 Memory-Frame Assy	XDS	REF	8151
6-2-	153372C		. Basic-Frame Assy		1	
-1	152009		. . Frame, Swing		1	
-2	152010		. . Bracket, Chassis Mtg		1	
-3	152011		. . Angle, Chassis Mtg		1	
			(Attaching Parts)			
-			. . Screw, Flat Hd 10-32		8	
			- - - * - - -			
-4	152240		. . Plate, Frame Latch		2	
			(Attaching Parts)			
-			. . Screw, Pan Hd 8-32		4	
			- - - * - - -			
-5	147595		. . Latch		2	
-6	108051		. . Spring, Pre-Load		2	
-7	147596		. . Bracket, Latch Mtg		2	
			(Attaching Parts)			
-			. . Screw, Pan Hd 8-32		4	
			- - - * - - -			
-8	153767		. Bracket, Pin Protect		2	
			(Attaching Parts)			
-	100012-408		. Screw, Pan Hd Rec Phil		8	
-	100024-400		. Washer, Lock Int Tooth		8	
-	100008-400		. Washer, Flat		8	
			- - - * - - -			
-9	100012-510		. Screw, Pan Hd Rec Phil		3	
-10	100024-500		. Washer, Lock Int Tooth		3	
-11	100018-500		. Washer, Flat		3	

(Continued)

Table 6-2. Sigma 3 Memory Frame Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-2-						
-12	148806		. Power Supply Assy, Memory (PT17B)		1	
			(Attaching Parts)			
-	100012-509		. Screw, Pan Hd Rec Phil		4	
-	100018-500		. Washer, Flat		4	
-	100024-500		. Washer, Lock Int Tooth		4	
			- - - * - - -			
-13	158047-001		. Busbar, Memory/Logic (Laminar)		1	
-14	158055-001		. Busbar, Memory-4 High (Laminar)		1	
			(Attaching Parts)			
-	100008-300		. Nut, Hex Mach		29	
-	100024-300		. Washer, Lock Int Tooth		29	
-	100018-300		. Washer, Flat		29	
			- - - * - - -			
-15	148418G		. 8K Basic Memory Assy (See Fig 6-3)		1	
			(Attaching Parts)			
-	100012-405		. Screw, Pan Hd Rec Phil		8	
-	100008-400		. Washer, Flat		8	
-	100024-300		. Washer, Lock Int Tooth		8	
			- - - * - - -			
-16	148418G		. 8K Basic Memory Assy (Rows F and G are Reserved for 8K Basic Assy Required for Memory B Bank Option)		REF	
-17	149395E		. Memory Port Multiple (MPM) (See Fig 6-5)		1	
			(Attaching Parts)			
-	100013-405		. Screw, Pan Hd Rec Phil		16	
-	100008-400		. Washer, Flat		16	
-	100024-300		. Washer, Lock Int Tooth		16	
			- - - * - - -			

(Continued)

Table 6-2. Sigma 3 Memory Frame Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-2-						
-18	153704		. Top Fan Assy, High Velocity		1	
-19	153705		. Bottom Fan Assy, High Velocity		1	
			(Attaching Parts)			
-	100012-406		. Screw, Pan Hd Rec Phil		6	
-	100008-400		. Washer, Flat		6	
-	100024-400		. Washer, Lock Int Tooth		6	
-	100012-205		. Screw, Pan Hd Rec Phil		4	
-	100018-200		. Washer, Flat		4	
-	100024-200		. Washer, Lock Int Tooth		4	
-	100008-200		. Nut, Hex Mach		4	
			- - - * - - -			
-20	130639		. Bracket, Door Latch Mtg Support		1	
			(Attaching Parts)			
-	100012-408		. Screw, Pan Hd Rec Phil		4	
-	100024-400		. Washer, Lock Int Tooth		4	
-	100008-400		. Nut, Hex Mach		4	
			- - - * - - -			
-21	152012		. Bracket, Door Latch Mtg		1	
-22	158990		. Bracket, Door Latch Mtg		1	
			(Attaching Parts)			
-	100012-205		. Screw, Pan Hd Rec Phil		6	
-	100018-200		. Washer, Flat		6	
-	100024-200		. Washer, Lock Int Tooth		6	
			- - - * - - -			

(Continued)

Table 6-2. Sigma 3 Memory Frame Assembly (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-2-						
-23	134171		. Spring, Door Latch		4	
			(Attaching Parts)			
-	100012-203		. Screw, Pan Hd Rec Phil		8	
-	100018-300		. Washer, Flat		8	
-	100024-300		. Washer, Lock Int Tooth		8	
			- - - * - - -			
-24	129554		. Trigger, Door Latch		4	
			(Attaching Parts)			
-	100012-103		. Screw, Pan Hd Rec Phil		4	
			- - - * - - -			
-25	134169		. Door, Chassis		1	
			(Attaching Parts)			
-	100012-205		. Screw, Pan Hd Rec Phil		5	
-	100018-200		. Washer, Flat		5	
-	100024-200		. Washer, Lock Int Tooth		5	
			- - - * - - -			
-	110871		. Connector, Male, 14 Contacts		1	
-	137481-182		. ZT45 Interframe Ribbon Cable Assy (1 from MPM, 01E to BMU,01,J) (1 from MPM, 01D to BMU,01H)		2	
-	135633-601		. Marginal Volt Indicator Cable Assy (From PT17B, MPM #1)		1	
-	153732-132		. ZT23 Interconnecting Cable Assy (From PT15B to MPM #1, 27E to MPM #2, 27E)		1	
-	152035-152		. Co-ax Cable-Clock, Assy (From CPU, 13C and 32D to MPM #1, 27E)		1	

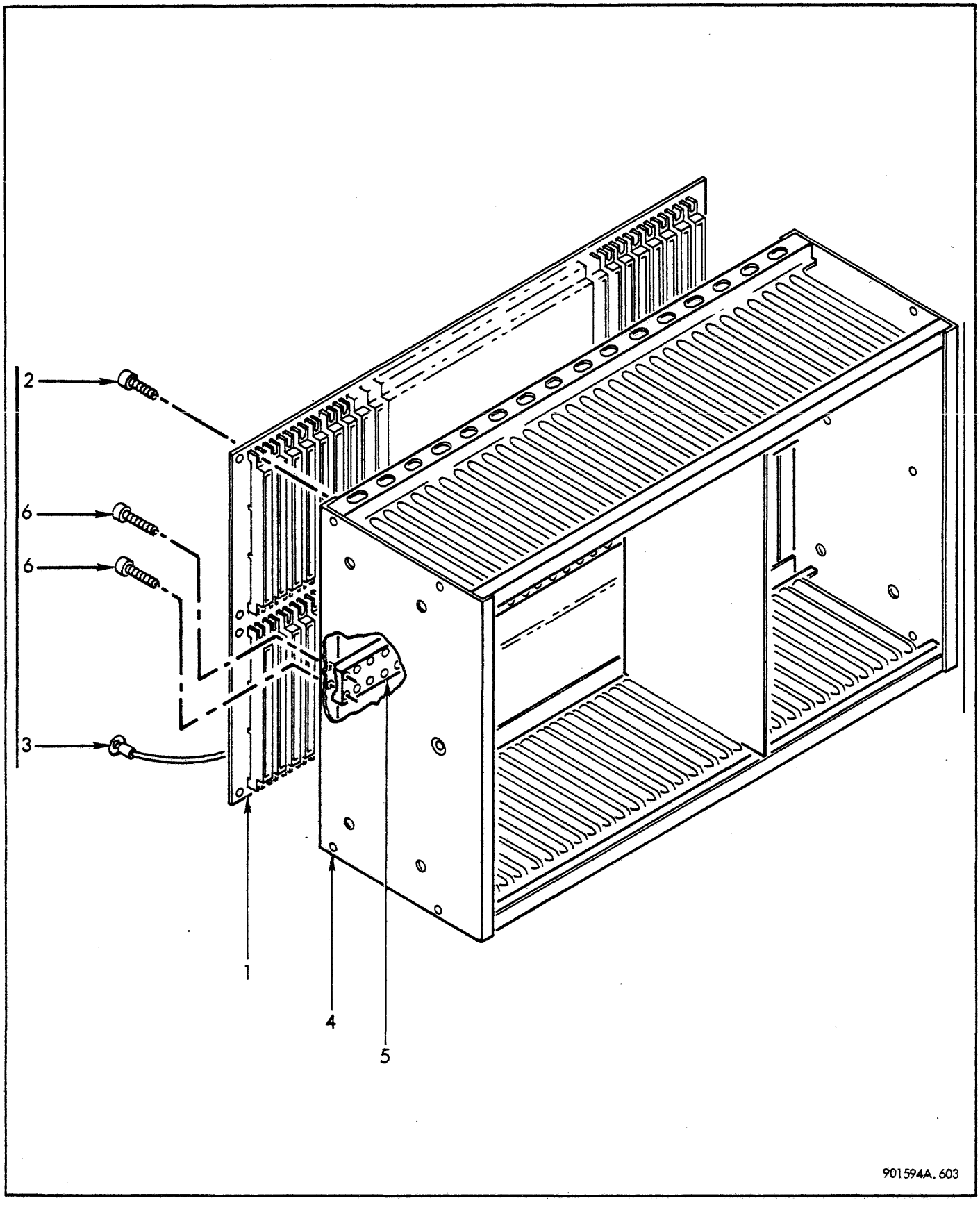


Figure 6-3. 8K Basic Memory Assembly

Table 6-3. 8K Basic Memory Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-3-	148418G		8K Basic Memory Assy		REF	8151 Ref 8151-1/2
6-3-	148423D		. . Memory Chassis Assy		1	
-1	148425		. . . Backwiring Board Assy, Memory		1	
			(Attaching Parts)			
-2	148832-512		. . . Screw, Thread Forming		36	
			- - - * - - -			
-3	131891-007		. . . Cable-Busbar Pick-Up Assy		1	
-	152235C		. . . Memory Chassis Assy		1	
-4	149485		. . . . Chassis, Memory Module		1	
-5	154630		. . . . Support, Bar		1	
			(Attaching Parts)			
-6	148832-506		. . . . Screw, Thread Forming		4	
			- - - * - - -			
-	154492B		. . Module Kit Assy (See Fig 6-4 for Module Locations)		1	

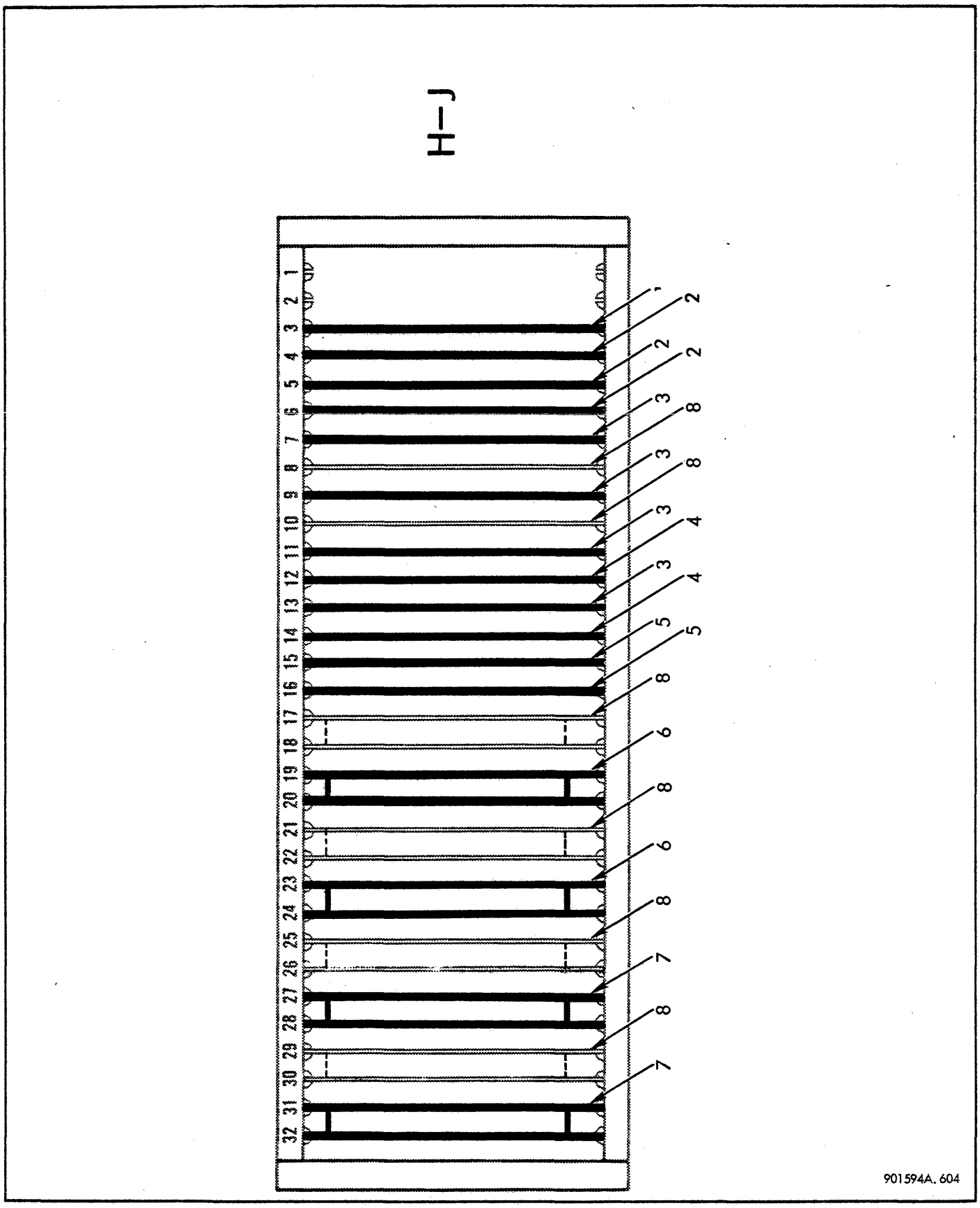


Figure 6-4. Module Locations, 8K Basic Memory Assembly

Table 6-4. Module Locations, 8K Basic Memory Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-4-			Module Locations, 8K Basic Memory Assy			
6-4-	154492B		. . Module Kit Assy	XDS	REF	8151 Ref 8151-1/2
-1	149647		. . . Module Assy, WTT10 Memory Voltage Regulator (Loc 3H-3J)		1	
-2	149348		. . . Module Assy, HTT10 Memory Sense Amp (Loc 4H-4J, 5H-5J, 6H-6J)		3	
-3	148850		. . . Module Assy, RTT10 Y Current Drive (Loc 7H-7J, 9H-9J, 11H-11J, 13H-13J)		4	
-4	149040		. . . Module Assy, RTT11 X Current Y Voltage Drive (Loc 12H-12J, 14H-14J)		2	
-5	149164		. . . Module Assy, RTT12 X Voltage Drive (Loc 15H-15J, 16H-16J)		2	
-6	147860		. . . Core Diode Module Assy (FTT14) (1 in Loc 19H-19J-20H-20J) (1 in Loc 23H-23J-24H-24J)		2	
-7	147869		. . . Core Diode Module Assy (FTT13) (1 in Loc 27H-27J-28H-28J) (1 in Loc 31H-31J-32H-32J)		2	
-	149668C*		. . 8K to 16K Memory Expansion Kit Assy (Model 8152)		1-2	8152 Ref 8151-1/2
-8	149040		. . . Module Assy, RTT11 X Current Y Voltage Drive (Loc 8H-8J-10H-10J)		2	
-8	147860		. . . Core Diode Module Assy (FTT14) (1 in Loc 17H-17J-18H-18J) (1 in Loc 21H-21J-22H-22J)		2	
-8	147869		. . . Core Diode Module Assy (FTT13) (1 in Loc 25H-25J-26H-26J) (1 in Loc 29H-29J-30H-30J)		2	
			*Memory Expansion Kit for addition to 8151-1 and 8151-2. Expansion of Basic 8K Module to 16K.			

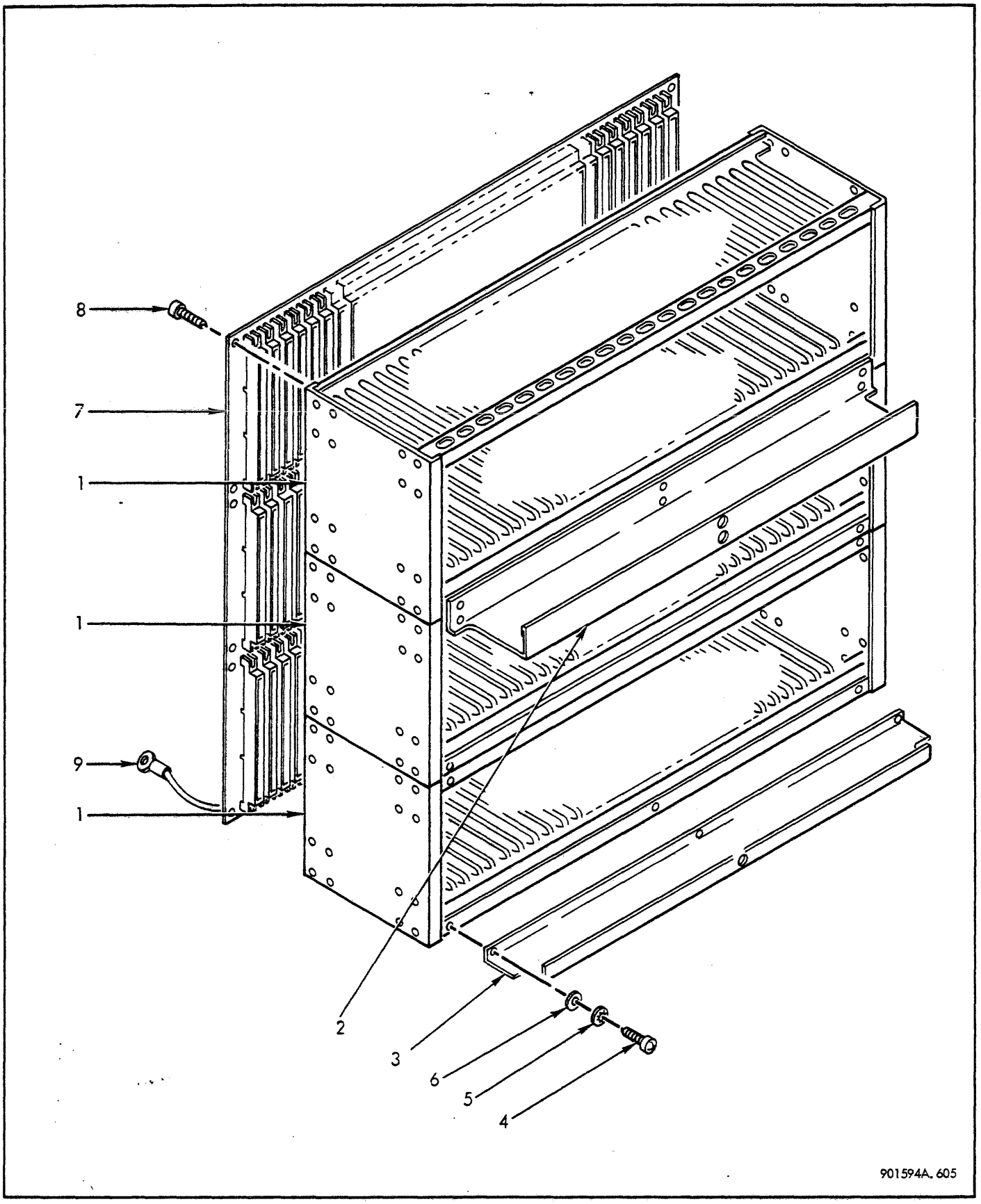


Figure 6-5. Memory Port Multiple Assembly (MPM)

Table 6-5. Memory Port Multiple Assembly (MPM)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-5-	149395E		Memory Port Multiple (MPM)		REF	8151 Ref 8151-1/2
-1	116231		. . Chassis, 32 Module		3	
-	154643B		. . Modules Assy (MPM) (See Fig 6-6 for Module Locations)		1	
-2	152013		. . Channel, Cable Routing		1	
-3	158225-001		. . Channel, Cable Routing		1	
			(Attaching Parts)			
-4	100012-204		. . Screw, Pan Hd Rec Phil		9	
-5	100024-204		. . Washer, Lock Int Tooth		9	
-6	100018-200		. . Washer, Flat		9	
			- - - * - - -			
-7	149400		. . Wired Board Assy (MPM)		1	
			(Attaching Parts)			
-8	148832-512		. . Screw, Thread Forming		54	
			- - - * - - -			
-9	131891-001		. . Cable-Busbar Pick-Up Assy		1	

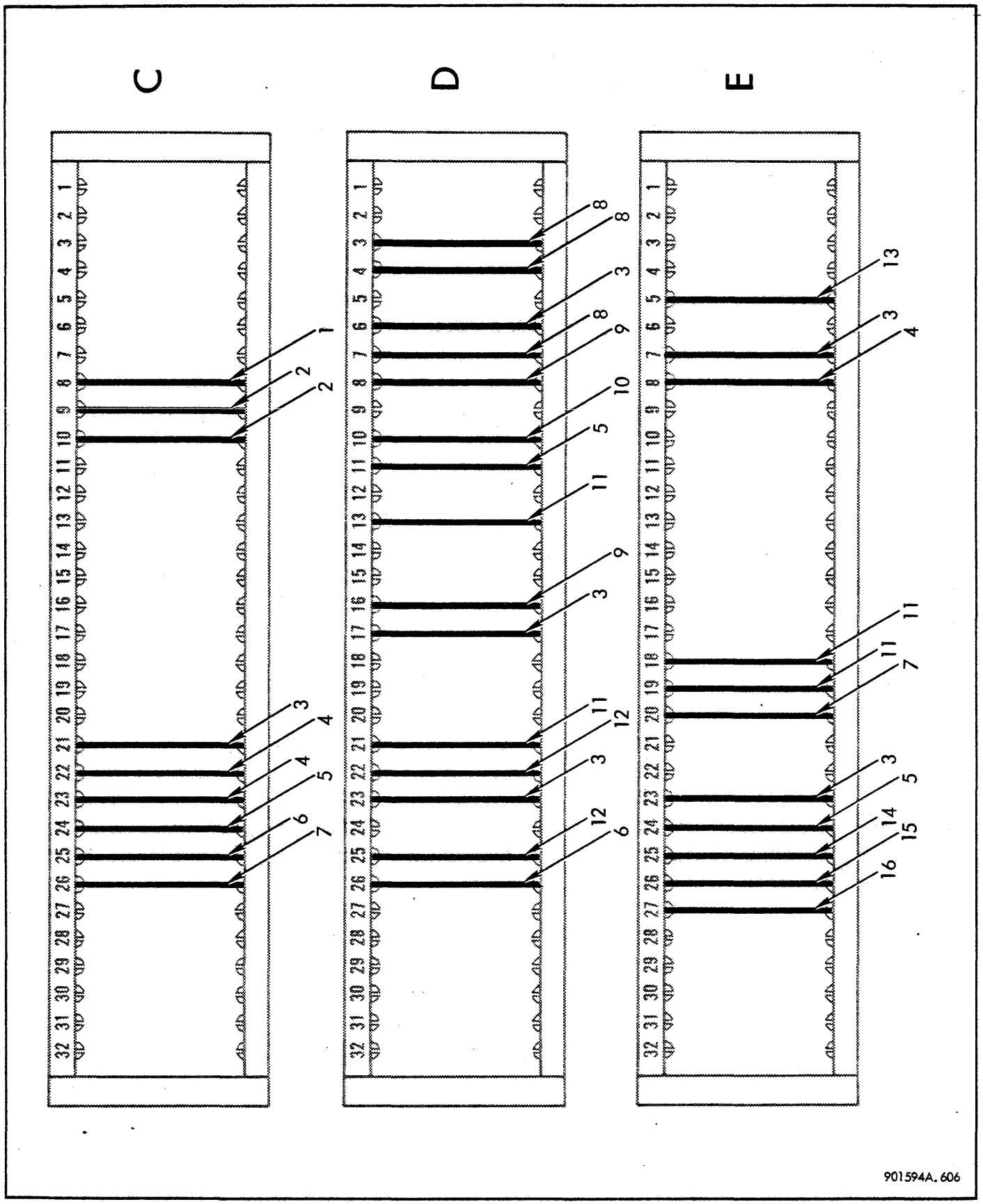


Figure 6-6. Module Locations, MPM Assembly

Table 6-6. Module Locations, MPM Assembly

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-6-			Module Locations, MPM Assy			8151 Ref 8151-1/2
6-6-	154643B		. . Modules Assy, MPM	XDS	REF	
-1	123008		. . . Module Assy, ST14 Toggle Switch Mod		1	
-2	156459*		. . . Module Assy, FT79 Buff Latch		2	
-3	116257		. . . Module Assy, XT10 Term Module		6	
-4	156468**		. . . Module Assy, FT80 Buff Latch		4	
-5	125262		. . . Module Assy, BT16 Gated Buffer		3	
-6	128188		. . . Module Assy, IT24 NAND/NOR Gate		2	
-7	116056		. . . Module Assy, BT10 Buff AND/OR Gate		2	
-8	156495***		. . . Module Assy, FT83 Buff Latch		3	
-9	117000		. . . Module Assy, IT13 Inverter Matrix		2	
-10	156486[t]		. . . Module Assy, FT82 Buff Latch		1	
-11	148711		. . . Module Assy, FT66 Buff Latch		4	
-12	116407		. . . Module Assy, BT13 Buff Matrix		2	
-13	156477[tt]		. . . Module Assy, FT81 Buff Latch		1	
-14	127391		. . . Module Assy, HT15 Delay Line Sensor		1	
-15	126963		. . . Module Assy, DT11 Delay Line		1	
-16	149793		. . . Module Assy, AT63 Delay Line Driver		1	

*This Module may be either an FT79 or an FT63.

**This Module may be either an FT80 or an FT64. 1 FT80 or FT64 goes in the CPU

***This Module may be either an FT83 or an FT68

[t]This Module may be either an FT82 or an FT67

[tt]This Module may be either an FT81 or an FT65

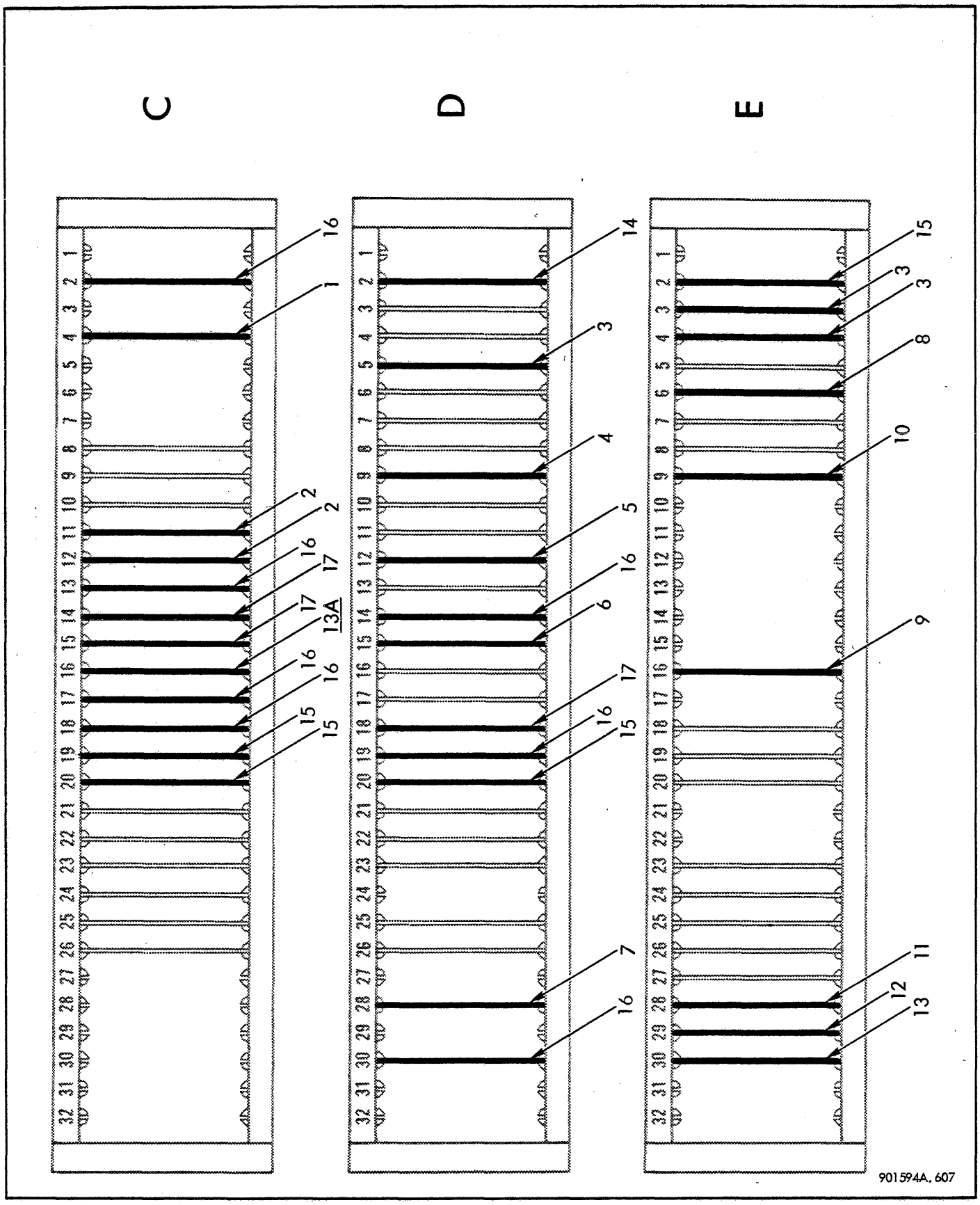


Figure 6-7. Module Locations, Bank-B Drive and Port Assemblies

Table 6-7. Module Locations, Bank B Drive and Port Assemblies

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-7-	149401C		Bank-B Drive Assy (Option) (Used for expanding 8151 above 16K)	XDS	1	8151 Ref 8151-2
-1	123008		. . Module Assy, ST14 Toggle Switch Module		1	
-2	156459*		. . Module Assy, FT79 Buff Latch		2	
-3	156495**		. . Module Assy, FT83 Buff Latch		3	
-4	156486***		. . Module Assy, FT82 Buff Latch		1	
-5	116407		. . Module Assy, BT13 Buff Matrix		1	
-6	117000		. . Module Assy, IT13 Inverter Matrix		1	
-7	128188		. . Module Assy, IT24 NAND/NOR Gate		1	
-8	156477†		. . Module Assy, FT81 Buff Latch		1	
-9	148711		. . Module Assy, FT66 Buff Latch		1	
-10	156468††		. . Module Assy, FT80 Buff Latch		1	
-11	149793		. . Module Assy, AT63 Delay Line Driver		1	
-12	126963		. . Module Assy, DT11 Delay Line		1	
-13	127391		. . Module Assy, HT15 Delay Line Sensor		1	
-13A	116257		. . Module Assy, XT10 Term Module		1	
-14	137481-122		. . ZT45 Interframe Ribbon Cable Assy (Loc 2D)		1	
-15	137481-201		. . ZT45 Interframe Ribbon Cable Assy (Loc 2E)		1	
			*This Module may be either an FT79 or an FT63.			
			**This Module may be either an FT83 or an FT68.			
			***This Module may be either an FT82 or an FT67.			
			†This Module may be either an FT81 or an FT65.			
			††This Module may be either an FT80 or an FT64.			

(Continued)

Table 6-7. Module Locations, Bank B Drive and Port Assemblies (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-7-						
			Optional:			
			Port Expansion Module Kit for 1 Memory: (8101/8102 is pre-requisite)			Ref 8155-11
-	158910C		. Memory Port 2 Assy (1-2)		1	8155
-15	156468[tt]		. . Module Assy, FT80 Buff Latch (Loc 19C 20C)		2	
-15	148711		. . Module Assy, FT66 Buff Latch (Loc 20D)		1	
			Port Expansion Module Kit for 2 Memory: (8151-1 is pre-requisite)			Ref 8155-12
-	158910C		. Memory Port 2 Assy (1-2)		2	
			Port Expansion Module Kit for 1 Memory: (8155-11 is pre-requisite)			Ref 8155-21
-	149403D		. Memory Port 3 Assy (2-3)		1	8155
-16	123008		. . Module Assy, ST14 Toggle Switch Module (Loc 2C)		1	
-16	116257		. . Module Assy, XT10 Term Module (Loc 13C)		1	
-16	156468[tt]		. . Module Assy, FT80 Buff Latch (Loc 17C 18C)		2	
-16	117000		. . Module Assy, IT13 Inverter Matrix (Loc 14D)		1	
-16	148712		. . Module Assy, FT66 Buff Latch (Loc 19D)		1	
-16	128188		. . Module Assy, IT24 NAND/NOR Gate (Loc 30D)		1	
			Port Expansion Module Kit for 2 Memory: (8155-12 is pre-requisite)			Ref 8155-22
-	149423D		. Memory Port 3 Assy (2-3)		2	
			[tt]This Module may be either an FT80 or an FT64.			

(Continued)

Table 6-7. Module Locations, Bank B Drive and Port Assemblies (Cont.)

Fig. & Index No.	XDS Part Number	Vendor Part Number	Description 1 2 3 4 5 6 7	Mfg. Code	Units Per Assy	Usable on Code
6-7-			Optional:			
			Port Expansion Module Kit for 1 Memory: (8155-11 and 8155-21 are pre-requisite)			Ref 8155-31
-	149404C		. Memory Port 4 Assy (3-4)		1	8155
-17	156468[tt]		. . Module Assy, FT80 Buff Latch (Loc 14C 15C)		2	
-17	148711		. . Module Assy, FT66 Buff Latch (Loc 18D)		1	
			Port Expansion Module Kit for 2 Memory: (8155-12 and 8155-22 are pre-requisite)			Ref 8155-32
-	149404C		. Memory Port 4 Assy (3-4)		2	

Table 6-8. Numerical Index

Fig. & Index No.	XDS Part Number	Description
6-8-		Numerical Index
2-	100008-200	Nut, Hex Mach
2-	100008-300	Nut, Hex Mach
2-	100008-400	Washer, Flat
2-	100012-103	Screw, Pan Hd Rec Phil
2-	100012-203	Screw, Pan Hd Rec Phil
2-	100012-205	Screw, Pan Hd Rec Phil
4-	100012-204	Screw, Pan Hd Rec Phil
2-	100012-405	Screw, Pan Hd Rec Phil
2-	100012-406	Screw, Pan Hd Rec Phil
2-	100012-408	Screw, Pan Hd Rec Phil
2-	100012-509	Screw, Pan Hd Rec Phil
2-9	100012-510	Screw, Pan Hd Rec Phil
2-	100018-200	Washer, Flat
5-6	100018-200	Washer, Flat
2-	100018-300	Washer, Flat
2-11	100018-500	Washer, Flat
2-	100024-200	Washer, Lock Int Tooth
5-5	100024-204	Washer, Lock Int Tooth
2-	100024-300	Washer, Flat
2-	100024-400	Washer, Lock Int Tooth
2-10	100024-500	Washer, Lock Int Tooth
2-6	108051	Spring, Pre-Load
2-	110871	Connector, Male 14 Contacts
6-7	116056	Module Assy, BT10 Buff AND/OR Gate
5-1	116231	Chassis, 32 Module
6-3	116257	Module Assy, XT10 Term Module
7-13A	116257	Module Assy, XT10 Term Module
7-16	116257	Module Assy, XT10 Term Module
6-12	116407	Module Assy, BT13 Buff Matrix
7-5	116407	Module Assy, BT13 Buff Matrix
6-9	117000	Module Assy, IT13 Inverter Matrix
7-6	117000	Module Assy, IT13 Inverter Matrix
7-16	117000	Module Assy, IT13 Inverter Matrix
6-1	123008	Module Assy, ST14 Toggle Switch Module
7-1	123008	Module Assy, ST14 Toggle Switch Module
7-16	123008	Module Assy, ST14 Toggle Switch Module
6-5	125262	Module Assy, BT16 Gated Buffer
6-15	126963	Module Assy, DT11 Delay Line
7-12	126963	Module Assy, DT11 Delay Line
6-14	127391	Module Assy, HT15 Delay Line Sensor
7-13	127391	Module Assy, HT15 Delay Line Sensor
6-6	128188	Module Assy, IT24 NAND/NOR Gate
7-7	128188	Module Assy, IT24 NAND/NOR Gate

(Continued)

Table 6-8. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
6-8-		
7-16	128188	Module Assy, IT24 NAND/NOR Gate
2-24	129554	Trigger, Door Latch
2-20	130639	Bracket, Door Latch Mtg Support
1-5	131416	Basic Cabinet Assy
5-9	131891-001	Cable-Busbar Pick-Up Assy
3-3	131891-007	Cable-Busbar Pick-Up Assy
2-25	134169	Door, Chassis
2-23	134171	Spring, Door Latch
2-	135633-601	Marginal Volt Indicator Cable Assy
7-14	137481-122	ZT45 Interframe Ribbon Cable Assy
2-	137481-182	ZT45 Interframe Ribbon Cable Assy
7-15	137481-201	ZT45 Interframe Ribbon Cable Assy
1-	139204G	Hardware Kit Assy, Front Frame
2-5	147595	Latch
2-7	147596	Bracket, Latch Mtg
4-6	147860	Core Diode Module Assy (FTT14)
4-8	147860	Core Diode Module Assy (FTT14)
4-7	147869	Core Diode Module Assy (FTT13)
4-8	147869	Core Diode Module Assy (FTT13)
2-15	148418G	8K Basic Memory Assy
3-	148418G	8K Basic Memory Assy
2-16	148418G	8K Basic Memory Assy (Used with Bank B only)
3-	148423D	Memory Chassis Assy
3-1	148425	Backwiring Board Assy Memory
1-3	148557	EIOP Assy
1-2	148586	CPU Frame Assy
6-11	148711	Module Assy, FT66 Buff Latch
7-9	148711	Module Assy, FT66 Buff Latch
7-15	148711	Module Assy, FT66 Buff Latch
7-17	148711	Module Assy, FT66 Buff Latch
7-16	148712	Module Assy, FT66 Buff Latch
1-4	148721	PCP Door Assy
2-12	148806	Power Supply Assy Memory (PT17B)
3-6	148832-506	Screw, Thread Forming
3-2	148832-512	Screw, Thread Forming
5-8	148832-512	Screw, Thread Forming
4-3	148850	Module Assy, RTT10 Y Current Drive
4-4	149040	Module Assy, RTT11 X Current Y Voltage Drive
4-8	149040	Module Assy, RTT11 X Current Y Voltage Drive
4-5	149164	Module Assy, RTT12 X Voltage Drive
4-2	149348	Module Assy, HTT10 Memory Sense Amp

(Continued)

Table 6-8. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
6-8-		
2-13	158047-001	Busbar, Memory/Logic (Laminar)
2-14	158055-001	Busbar, Memory-4 High (Laminar)
5-3	158225-001	Channel, Cable Routing
7-	158910C	Memory Port 2 Assy
2-22	158990	Bracket, Door Latch Mtg

Fig. & Index No.	XDS Part Number	Description

Table 6-8. Numerical Index (Cont.)

Fig. & Index No.	XDS Part Number	Description
6-8-		
2-17	149395E	Memory Port Multiple (MPM)
5-	149395E	Memory Port Multiple (MPM)
5-7	149400	Wired Board Assy (MPM)
7-	149401C	Bank B Drive Assy
7-	149403D	Memory Port 3 Assy
7-	149404C	Memory Port 4 Assy
3-4	149485	Chassis, Memory Module
4-1	149647	Module Assy, WTT10 Memory Voltage
4-	149668C	8K to 16K Memory Expansion Kit Assy
7-11	149793	Module Assy, AT63 Delay Line Driver
7-16	149793	Module Assy, AT63 Delay Line Driver
2-1	152009	Frame, Swing
2-2	152010	Bracket, Chassis Mtg
2-3	152011	Angle, Chassis Mtg
2-21	152012	Bracket, Door Latch Mtg
5-2	152013	Channel, Cable Routing
2-	152035-132	Co-Ax Cable-Clock Assy
3-	152235C	Memory Chassis Assy
2-4	152240	Plate, Frame Latch
1-1	153259D	Sigma 3 Memory-Frame Assy
2-	153259D	Sigma 3 Memory-Frame Assy
2-	153372C	Basic-Frame Assy
2-18	153704	Top Fan Assy, High Velocity
2-19	153705	Bottom Fan Assy, High Velocity
2-	153732-132	ZT23 Interconnecting Cable Assy
2-8	153767	Bracket, Pin Protect
3-	154492B	Module Kit Assy
4-	154492B	Module Kit Assy
3-5	154630	Support, Bar
5-	154643B	Modules Assy (MPM)
6-2	156459	Module Assy, FT79 Buff Latch
6-4	156459	Module Assy, FT79 Buff Latch
7-10	156468	Module Assy, FT80 Buff Latch
7-15	156468	Module Assy, FT80 Buff Latch
7-16	156468	Module Assy, FT80 Buff Latch
7-17	156468	Module Assy, FT80 Buff Latch
6-10	156486	Module Assy, FT82 Buff Latch
7-4	156486	Module Assy, FT82 Buff Latch
6-8	156495	Module Assy, FT83 Buff Latch
7-3	156495	Module Assy, FT83 Buff Latch
6-13	156477	Module Assy, FT81 Buff Latch
7-8	156477	Module Assy, FT81 Buff Latch

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