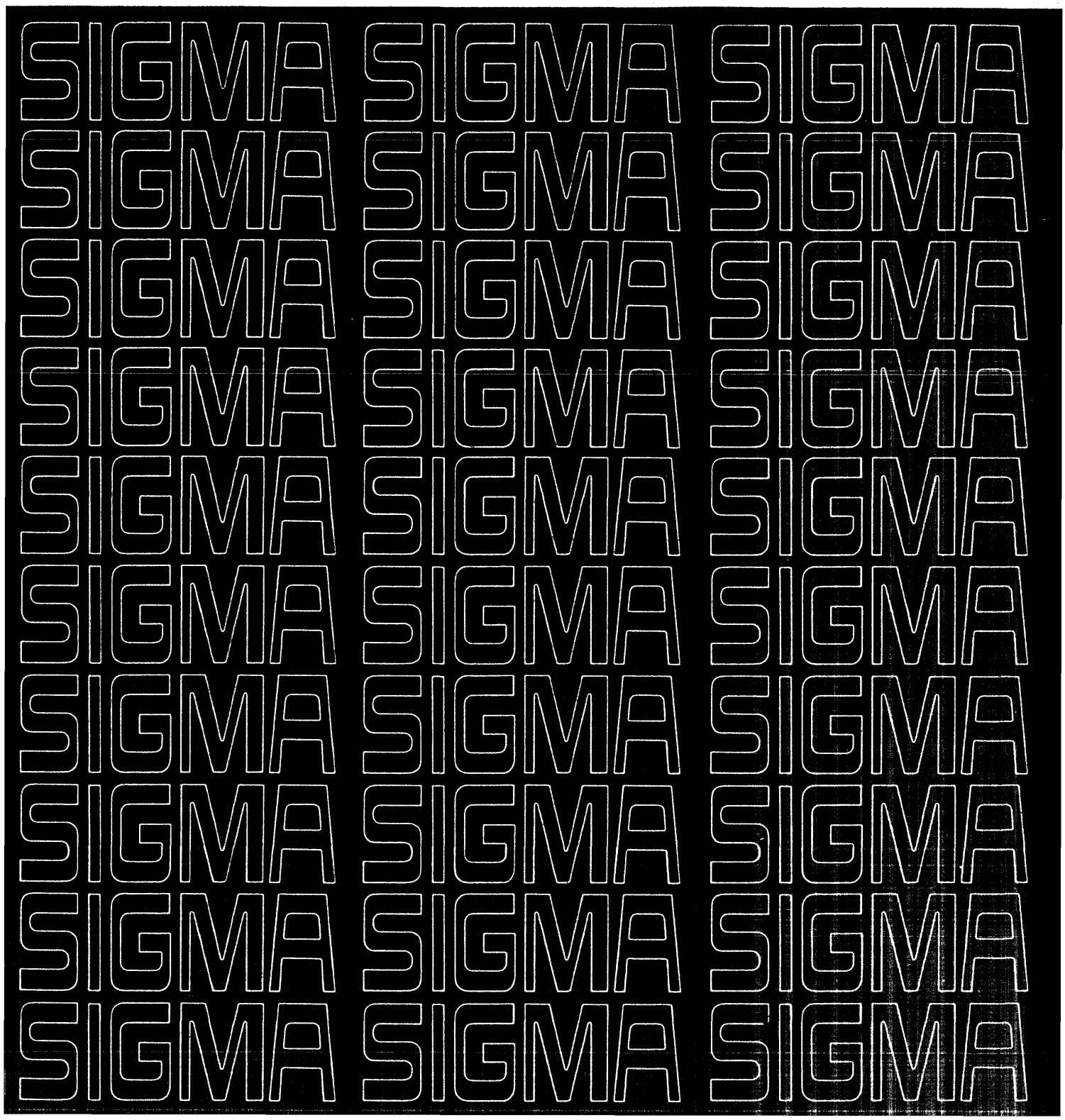
SDS SIGMA 5 COMPUTER

Reference Manual

SCIENTIFIC DATA SYSTEMS



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RELATED PUBLICATIONS

Title	Publication No.
Sigma 5/7 Symbol/Meta-Symbol/Reference Manual	90 09 52A
Sigma Glossary of Computer Terminology	90 09 57A

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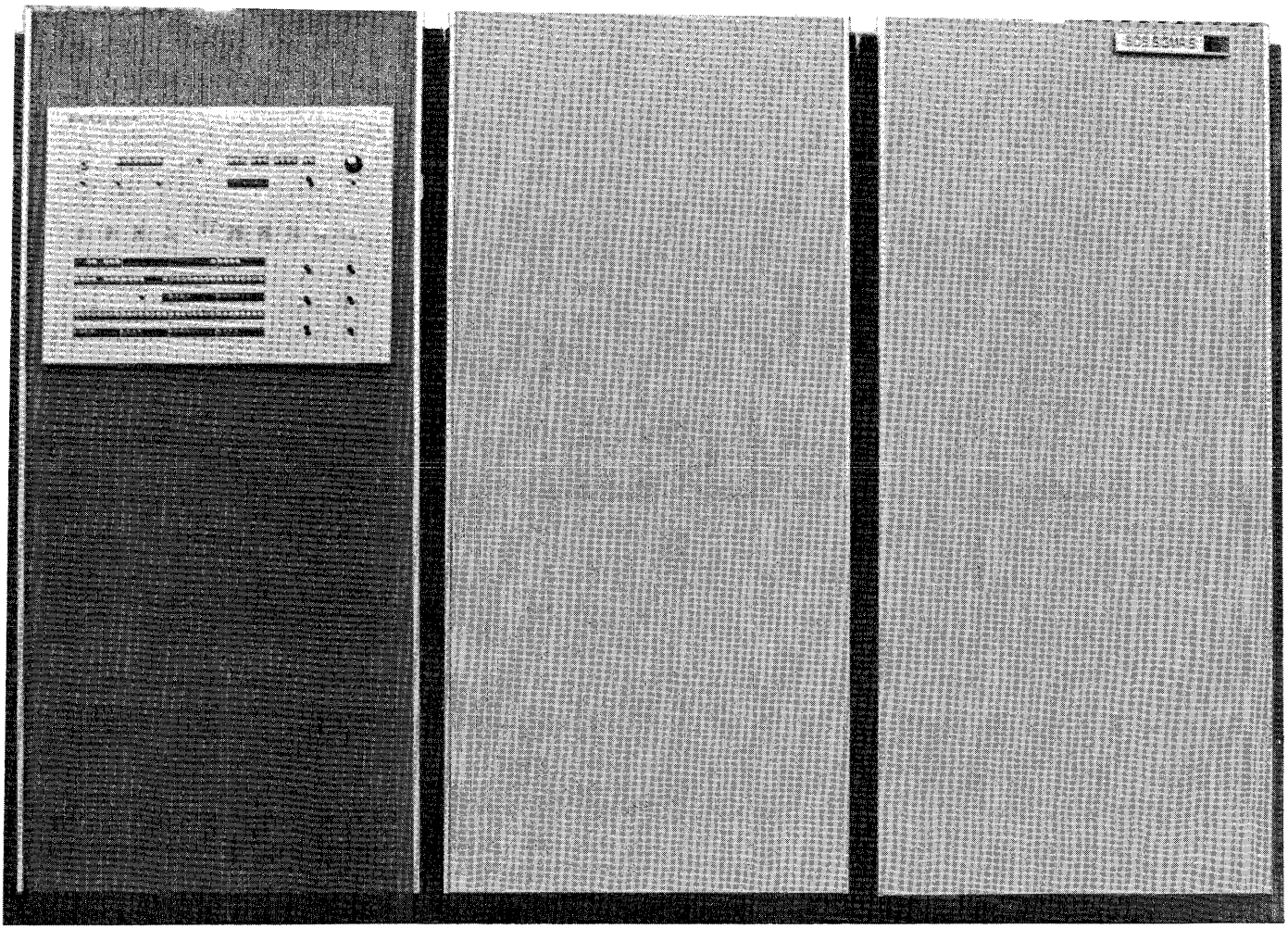


SDS SIGMA 5 Computer

1. SIGMA 5 SYSTEM

A typical SIGMA 5 system (see Figure 1) consists of the following major elements:

- A memory consisting of up to eight magnetic core storage modules
- A central processing unit (CPU) that addresses core memory, fetches and stores information, performs arithmetic and logical operations, sequences and controls instruction execution, and controls the exchange of information between core memory and other elements of the system.
- An input/output system controlled by one or more input/output processors (IOPs), each providing data transfer between core memory and peripheral input/output devices, and operating simultaneously with the CPU.

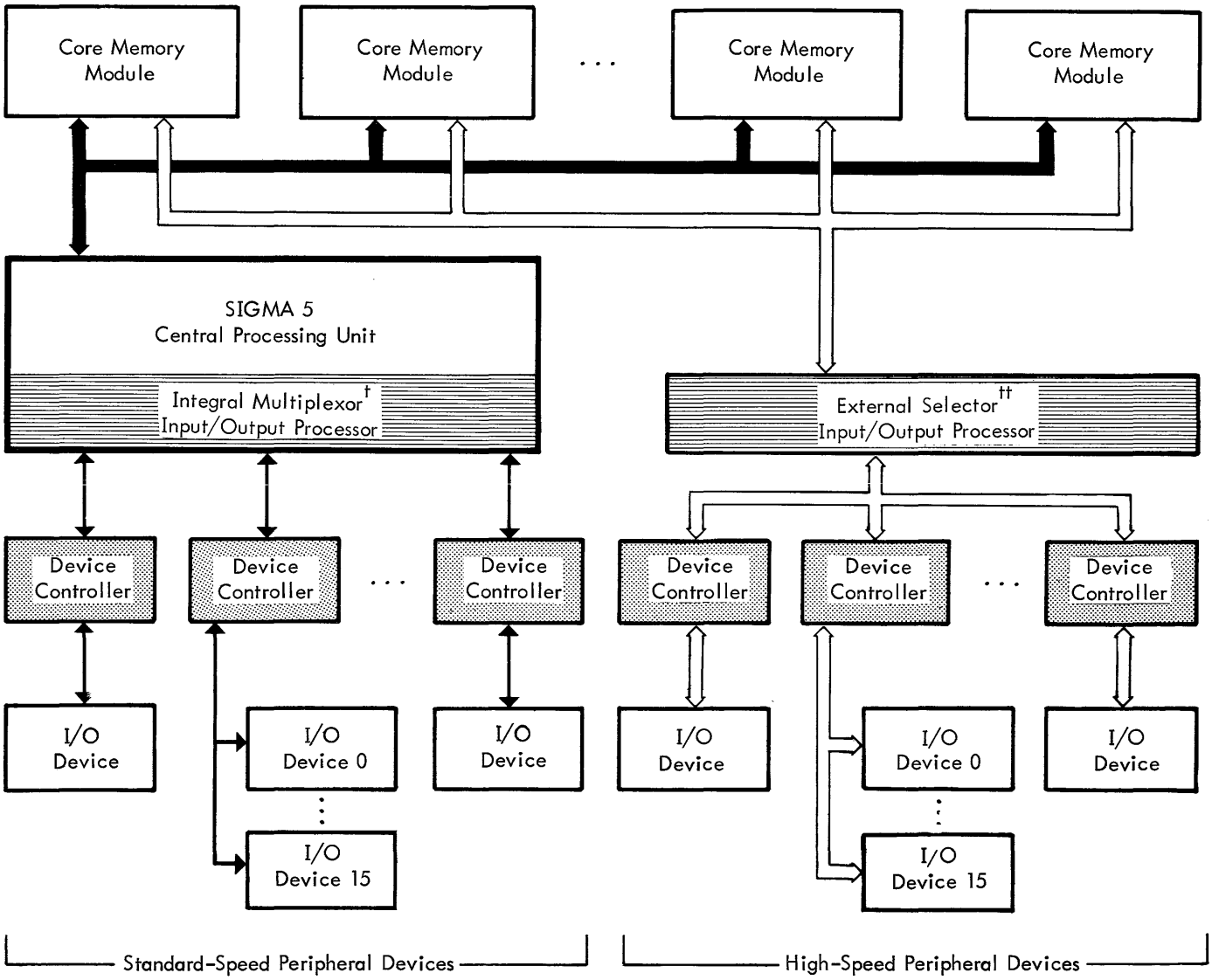


Figure 1. A typical SIGMA 5 System

†The integral multiplexor IOP allows up to 32 devices (one per device controller) to operate simultaneously. This IOP preempts central processor memory accesses and computation time. Other multiplexor (or selector) IOPs may be added to the SIGMA 5 system, with each additional IOP having an independent memory path. IOPs with independent paths allow for input/output simultaneous with computation.

††The selector IOP allows one device at a time to operate at a high-speed transfer rate of up to one 32-bit word per memory cycle. A selector IOP may service up to 32 high-speed devices.

GENERAL CHARACTERISTICS

A SIGMA 5 system has many advanced features and operating charactersitics that enable it to function efficiently in real-time, general-purpose, and multiusage computing environments:

- Word-oriented memory (32-bit word plus parity bit) for maximum efficiency; memory is addressable and alterable by byte (8-bit), halfword (2-byte), word (4-byte), and doubleword (8-byte) quantities.
- Full parity checking for both CPU/memory and input/output operations
- Memory expandable from 4096 to 131,072 words (16,384 to 524,288 bytes) in blocks of 4096, 8192, 12,288 or 16,384 words, for complete flexibility of capacity
- Direct addressing of the entire core memory, within the primary instruction word and without the need for base registers, indirect addressing, or indexing
- Indirect addressing, with or without post-indexing, for additional programming flexibility
- Displacement index registers, automatically self-adjusting for all data sizes
- Immediate addressing of operands, for greater storage efficiency and increased speed
- 16 general-purpose registers, expandable (in blocks of 16) to 256 to reduce transfer of data into and out of registers in a multiusage environment
- Selective memory write protection (optional)
- Watchdog timer, assuring nonstop operation
- Real-time priority interrupt system with automatic identification and priority assignment, extremely fast response time, and up to 240 levels that can be individually armed and/or enabled by program control
- Interruptibility of long instructions, guaranteeing fastest possible response to interrupts by the system
- Automatic traps for error conditions and for simulation of optional instructions not physically implemented, all under flexible program control
- Power fail-safe for automatic, safe shutdown in the event of a power failure
- Multiple interval timers, with a choice of resolutions for independent time bases
- Privileged instruction logic (master/slave modes), for concurrent, multiusage operation
- Complete, powerful instruction set including:
  - Byte, halfword, word, and doubleword operations
  - Use of all memory-referencing instructions for register-to-register operations, with or without indirect addressing and post-indexing, and within the normal instruction format
  - Multiple-register operations
  - Fixed-point arithmetic operations in halfword, word and doubleword modes
  - Optional floating-point hardware operations, in short and long formats, with significance, zero, and normalization control and checking, all under full program control
  - Full complement of logical operations (AND, OR, exclusive OR)
  - Comparison operations, including compare between limits (with limits in memory or in registers)
  - Calls, an extension of the SDS programmed operators concept, permitting up to 64 dynamically variable, user-defined instructions, and permitting a program to gain access to monitor functions without monitor intervention
  - Push-down stack operations (hardware implemented) of single or multiple words, with automatic limit checking, for dynamic space allocation, subroutine communication, and recursive routine capability
  - An analyze instruction, for facilitating effective address computation
  - An interpret instruction, for increased compilation effectiveness and speed
  - Shift operations (left and right) of words or doublewords, including logical, circular, arithmetic, and floating-point modes
- Efficiently operating input/output system with the following features:
  - Direct input/output of a full word, without the use of a channel
  - Up to five external input/output processors
  - Multiplexor input/output processors, for simultaneous operation of up to 32 standard-speed devices per I/O processor. One multiplexor I/O processor is integral with the CPU, sharing memory access and processing time; optional I/O processors operate semi-independently and simultaneously with computation
  - Selector input/output channels (8 or 32 bits wide), for data rates approaching 3.3 million bytes per second
  - Up to 32 device controllers connected to each external I/O processor
  - Both data and command chaining, for scatter-read and gather-write operations
  - Up to 32,000 output control signals and input test signals
- Comprehensive array of modular software:
  - Expands in capability and speed as system grows, with no reprogramming required
  - Operating systems: Basic Control Monitor and Batch Processing Monitor

- Compiler: FORTRAN IV in standard and high-efficiency versions
- Assemblers: Symbol and advanced Meta-Symbol
- Conversational language: FORTRAN IV calculator mode
- Library: Mathematical, utility, and input/output programs
- Business software: Generalized Sort/Merge, 1401 Simulator, and SDS COBOL-65

- The same comprehensive, field-proven peripheral devices that are available for SIGMA 7 computer systems are also available for SIGMA 5 computer systems. The available peripheral devices include the following:

  - Rapid-access data (RAD) files: Capacities to 5.37 million bytes per unit; transfer rates to 3 million bytes per second; average access times as low as 17 milliseconds. Fixed read/write head for each track eliminates time delays associated with movable-head units.
  - Magnetic tape units: Four models; 7-track and 9-track systems, IBM-compatible; high-speed units operate at 150 inches per second with transfer rates of up to 120,000 bytes per second; low-cost units operate at 37.5 inches per second with transfer rates of 20,800 characters per second
  - Displays: Keyboard/display, buffered, with 8.5 x 11-inch page area containing up to 2048 characters displayed in any of 32 lines of 86 characters each. The display operates in character or message modes. Graphic display has standard character generator, vector generator, and closeups, as well as light pen, refresh buffer, and alphanumeric/function kayboard options. Both types feature display rates of up to 100,000 characters per second.
  - Card equipment: Reading speeds of up to 1500 cards per minute; punching speeds of up to 300 cards per minute; intermixed binary and EBCDIC card codes; simplified punch programming does not require "corner-turning" logic
  - Line printers: Fully buffered, with speeds of up to 1,000 lines per minute; 132 print positions with 56 different characters.
  - Keyboard/printers: 10 characters per second; also available with integral paper tape reader (20 characters per second) and punch (10 characters per second)
  - Paper tape equipment: Readers with speeds of up to 300 characters per second; punches with speeds of up to 120 characters per second.
  - Graph plotters: Digital incremental; providing drift-free plotting in two axes in up to 300 steps per second at speeds from 30 mm to 3.5 inches per second.
  - Data communications equipment: A complete line of character- and message-oriented equipment to connect remote and local user terminals to common-carrier lines

REAL-TIME FEATURES

Real-time applications are characterized by a need for hardware that provides quick response to an external environment, speed great enough to keep up with the real-time process itself, and sufficient input/output flexibility to handle a wide variety of data types at varying speeds. The SIGMA 5 system includes provisions for the following real-time computing features:

Multilevel, True Priority Interrupt System. The real-time-oriented SIGMA 5 system provides for quick response to interrupts by means of up to 224 external interrupt levels. The source of each interrupt is automatically identified and responded to according to its priority (this function need not be programmed). For further flexibility, each level can be individually disarmed (to discontinue accepting inputs to it) and disabled (to defer responding to it). Use of the disarm/disable feature makes programmed dynamic reassignment of priorities quick and easy, even while a real-time process is in progress. In establishing a configuration for the system, each group of 16 interrupt levels can have its priority assigned in different ways in order to meet the specific needs of the problem; the way in which interrupt levels are programmed is not affected by the priority assignment.

Programs that deal with interrupts from specially designed equipment sometimes must be checked out before that equipment is actually available. To permit simulating this special equipment, any SIGMA 5 interrupt level can be triggered by the CPU itself through execution of a single instruction. This capability is also useful in establishing a hierarchy of responses. For example, in responding to a high-priority interrupt, after the urgent processing is completed, it may be desirable to assign a lower priority to the remaining portion in order to respond to other critical stimuli. The interrupt routine can accomplish this merely by triggering a lower-priority level, which processes the remaining data only after other interrupts have been handled.

Nonstop Operation. When connected to special devices (on a ready/resume basis), the computer can sometimes become excessively delayed if the special device does not respond quickly. A built-in watchdog timer assures that the SIGMA 5 computer cannot be delayed for an excessive length of time.

Real-Time Clocks. Many real-time functions must be timed to occur at specific instants. Other timing information is also needed – elapsed time since a given event, for example, or the current time-of-day. SIGMA 5 can contain two or four real-time clocks with varying degrees of resolution (1/60 second or 1/8 millisecond, for example) to meet these needs. These clocks also allow easy handling of separate time bases and relative time priorities.

Rapid Context Switching. When responding to a new set of interrupt-initiated circumstances, a computer system must

preserve the current operating environment, for continuance later, while setting up the new environment. This changing of environments must be done quickly, with a minimum of "overhead" costs in time. In SIGMA 5, each one of up to 16 blocks of general-purpose arithmetic registers can, if desired, be assigned to a specific environment. All relevant information about the current environment (instruction address, current general register block, memory-protection key, etc.) is kept in a 64-bit program status doubleword (PSD). A single instruction stores the current PSD anywhere in memory and loads a new one from memory to establish a new environment, which includes information identifying a new block of general-purpose registers. A SIGMA 5 system can thus preserve and change its operating environment completely through the execution of a single instruction.

Simultaneous Device Operation. The integral multiplexor input/output processor permits up to 32 channels with standard-speed devices to operate concurrently; the addition of external multiplexor I/O processors increases this throughput.

High-Speed Channel Operation. The use of the selector I/O processor permits very high-speed data transfer – up to one 32-bit word per memory cycle. To meet special needs, data size can be 8 or 32 bits wide.

Memory Protection. Both foreground (real-time) and background programs can be run concurrently in a SIGMA 5 system because a foreground program is protected against destruction by an unchecked background program. The optional memory write-protection feature guarantees that protected areas of memory can be written into only under certain conditions.

Variable Precision Arithmetic. Many of the data encountered in real-time systems are 16 bits (or less) in precision. To permit this length of data to be processed efficiently, SIGMA 5 provides halfword arithmetic operations in addition to full word operations. Doubleword arithmetic operations (for extended precision) are also included.

Direct Data Input/Output. For handling asynchronous I/O, a 32-bit word can be transferred directly to or from a general-purpose register, so that an I/O channel need not be occupied with relatively infrequent transmissions.

Interleave/Overlap. To increase processing speeds, memory modules overlap cycles automatically wherever possible. Core memory addresses can be interleaved modulo-2 (odd-even), or modulo-4 to increase the probability of overlapping.

GENERAL-PURPOSE FEATURES

General-purpose computing applications are characterized primarily by an emphasis on computation, internal data handling, and large amounts of input/output at standard speeds. The SIGMA 5 system includes the following general-purpose computer features:

Floating-Point Hardware (optional). Floating-point instructions are available in both short (32-bit) and long (64-bit) formats. Under program control, the user can select optional zero checking, normalization, and significance checking (which causes the computer to trap when a post operation shift of more than two hexadecimal places occurs in the fraction of a floating-point number). The significance checking feature permits the use of the short floating-point format for high processing speed and storage economy and the use of the long format when loss of significance is detected.

Indirect Addressing. This feature provides for simple table linkages and permits the user to keep data sections of his program separate from procedure sections for ease of maintenance.

Displacement Indexing. The technique of indexing by means of a "floating" displacement permits the user to access the desired unit of data without the need to consider its size. The index registers automatically align themselves appropriately; thus, the same index register can be used on arrays with different data sizes. For example, in a matrix multiplication of any array of fullword, single-precision, fixed-point numbers, the results can be stored in a second array as double-precision numbers, using the same index quantity for both arrays. If an index register contains the value of k, then the user always accesses the kth element, whether it is a byte, halfword, word, or doubleword. Incrementing by various quantities according to data size is not required; instead, incrementing is always by units in a continuous array table no matter which size of data element is used.

Powerful Instruction Set. The availability of a large number of major instructions results in programs that are short, rapidly assembled, and quickly executed.

Call Instructions. Four instructions permit handling up to 64 user-defined subroutines (as if they were built-in machine instructions) and gaining access to specified monitor services without requiring monitor intervention.

Interpret Instruction. This instruction simplifies and speeds compiling operations, thus reducing the space and time requirements for compilers.

Four-Bit Condition Code. This feature simplifies the checking of results by automatically providing information on almost every instruction execution (including indicators for overflow, underflow, zero, minus, and plus, as appropriate) without requiring an extra instruction execution.

MULTIUSAGE FEATURES

"Multiusage operation", as implemented in the SIGMA 5 system, consists of two or more major kinds of computing applications running concurrently – general purpose computing with real-time process control, for example. Because SIGMA 5 has been designed on a real-time base, it is qualified for efficient operation in a multiusage

environment. Many of its hardware features that prove valuable for certain application areas are equally useful for others, although in different ways. This characteristic of SIGMA 5 makes it particularly effective in multiusage applications. The major SIGMA 5 multiusage computer features are:

Priority Interrupt. In a multiusage environment, many elements operate asynchronously. Thus, having a true priority interrupt system, as SIGMA 5 does, is expecially important. With it the computer system can respond quickly (and in proper order) to the many demands being made upon it, without the high overhead costs of complicated programming, lengthy execution time, and extensive storage allocations.

Quick Response. The many features that combine to produce a quick-response system – multiple register blocks, quick context saving, push-pull operations – benefit all users because more of the machine's power at any instant is available for useful work.

Multiple Register Blocks. The optional availability of up to 16 blocks of general-purpose registers further improves response time by reducing the need to store and load register blocks. As needed, each user can be assigned a distinct block; the program status doubleword automatically points to the currently applicable register block.

Rapid Context Saving. When changing from one user to another, the operating environment can be switched quickly and easily. Stack-manipulating instructions permit from one to 16 general-purpose registers to be stored in a push-down stack by a single instruction – with automatic updating of stack status information – and to be retrieved (again, by a single instruction) when needed. The current program status doubleword, which contains the entire description of the current user's environment and mode of operation, can be stored anywhere in memory and a new program status doubleword loaded, all with a single instruction.

User Protection. The master/slave mode of operation restricts each user to his own set of instructions while reserving to the monitor those instructions that could, if used incorrectly, destroy another user's program. The optional memory write protection feature not only protects each user from every other user, but also guarantees the integrity of programs essential to critical real-time applications.

Input/Output. Because of its wide range of capacities and speeds (with and without channels), the SIGMA 5 I/O system simultaneously satisfies the needs of many different application areas economically, both in terms of equipment and of programming. SIGMA 5 can control up to eight input/output processors (of two types in various combinations. Each multiplexor I/O processor can have to 32 standard-speed I/O channels operating simultaneously; selector I/O processors can have any one of up to 32 high-speed I/O devices operating on each processor. The external I/O processors operate semi-independently of the central processor, leaving it free to provide faster response to overall system needs.

Nonstop Operation. A watchdog timer assures that the system continues to operate even if certain special I/O capabilities are used with special devices that can cause delays or halts if they fail.

Instruction Set. The large, powerful SIGMA 5 instruction set provides the computational and data handling capabilities required for widely differing application areas, so that each user's program length (thus running time) is decreased and the speed of obtaining results is increased.

Flexible Storage Capacity. SIGMA 5 memory is available in 32 sizes (from 4096 to 131,072 words) to provide the precise capacity needed, while assuring potential for expansion.

COMPATIBILITY WITH SIGMA 7 SYSTEMS

SIGMA 5 computer hardware and software systems have been designed for program compatibility with SIGMA 7 systems. In this context, "compatibility" means the following:

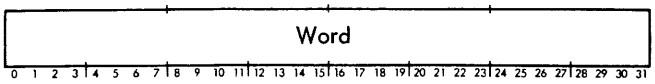
1. Any program written for a SIGMA 5 computer can be assembled (or compiled) by SIGMA 7 software and then executed by either a SIGMA 5 or a SIGMA 7 computer.
2. Any program written for a SIGMA 5 computer and assembled (or compiled) by SIGMA 5 software can be executed by a SIGMA 7 computer.
3. Any program written for a SIGMA 7 computer can be assembled (or compiled) by SIGMA 5 software, even if the program cannot be executed by the SIGMA 5 computer.
4. Any SIGMA 7 program that can be executed under control of the SIGMA 7 Basic Control Monitor or the SIGMA 7 Batch Processing Monitor can be executed under control of the corresponding SIGMA 5 monitor. A simulation package is provided as part of the standard SIGMA 5 monitor systems for those SIGMA 7 instructions that are not implemented in the SIGMA 5 computer. The instruction simulation package occupies a portion of core memory while the SIGMA 7 program is being executed; thus, the maximum size for programs that require simulated instructions is less than the maximum size for programs that use only SIGMA 5 instructions, within a specific memory system.
5. The only SIGMA 7 programs that cannot be executed under the control of a SIGMA 5 monitor system are those programs that either use the SIGMA 7 memory map option or require the Universal Time-Sharing Monitor system to use the memory map option. Such programs include conversational, time-sharing programs.

2. SIGMA 5 SYSTEM ORGANIZATION

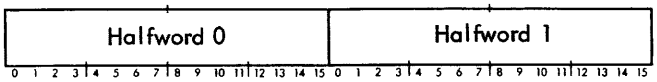
The primary elements in a basic SIGMA 5 system – a central processor, core memory, and input/output processor – are all designed around a central bus structure. Each primary element of the system operates asynchronously and semi-independently, automatically overlapping the operation of the other elements (when circumstances permit) for greater speed. The basic configuration can be expanded merely by increasing the number of core memory modules (up to eight), increasing the number of buses (up to six), or by increasing the number of input/output processors (up to six).

INFORMATION FORMAT

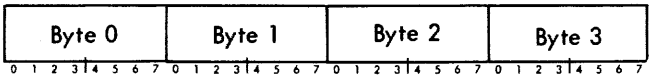
The basic element of SIGMA 5 information is a 32-bit word, in which the bit positions are numbered from 0 through 31, as follows:



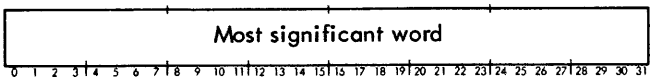
A SIGMA 5 word can be divided into two 16-bit parts (called halfwords) in which the bit positions are numbered from 0 through 15, as follows:

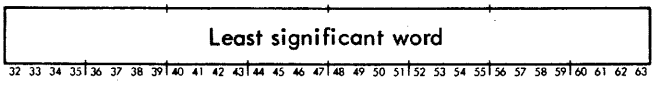


A SIGMA 5 word can also be divided into four 8-bit parts (called bytes) in which the bit positions are numbered from 0 through 7, as follows:



Two SIGMA 5 words can be combined to form a 64-bit element (called a doubleword) in which the bit positions are numbered from 0 through 63, as follows:





Four bits of information can be expressed by means of a single hexadecimal digit. Hexadecimal digits (and their binary and decimal equivalents) are expressed in the following notation:

Hexadecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
B	1011	11
C	1100	12
D	1101	13
E	1110	14
F	1111	15

Thus, a byte can be expressed as a 2-digit hexadecimal number, a halfword as a 4-digit hexadecimal number, a word as an 8-digit hexadecimal number, and a doubleword as a 16-digit hexadecimal number. In this reference manual, a hexadecimal number is displayed as a string of hexadecimal digits surrounded by single quotes and preceded by the letter "X". For example, the binary number 01011010 is expressed hexadecimally as X'5A'.

CORE MEMORY

SIGMA 5 core memory systems use a 32-bit word (four 8-bit bytes, plus a parity bit) as the basic unit of information. All core memory is directly addressable both by the CPU (except for memory locations 0 through 15) and by the IOP. The SIGMA 5 addressing capability accommodates a maximum core memory size of 131,072 words (524,288 bytes). Core memory is modular and is available in up to 8 blocks of 4096 words (16,384 bytes), 8192 words (32,768 bytes), 12,288 words (49,152 bytes), or 16,384 words (65,536 bytes), in almost any combination.

DEDICATED CORE MEMORY LOCATIONS

Core memory locations 0 through 319 are reserved by standard SDS software for special purpose as shown in Table 1.

INFORMATION BOUNDARIES

SIGMA 5 instructions assume that bytes, halfwords, and doublewords are located in core storage according to the following boundary conventions:

1. A byte is located in bit positions 0 through 7, 8 through 15, 16 through 23, or 24 through 31 of a word.
2. A halfword is located in positions 0 through 15 or 16 through 31 of a word.
3. A doubleword is located so that bits 0 through 31 of the doubleword are contained within an even-numbered word, and bits 32 through 63 of the same doubleword are contained within the next consecutive (odd-numbered) word.

The various information boundaries are illustrated in Figure 2.

Table 1. Dedicated SIGMA 5 Core Memory Locations

Location		Function
Decimal	Hexadecimal	
0 : 15	0 : F	Addresses of general registers
16 : 31	10 : 1F	Reserved for future use
32 33	20 21	CPU/IOP communication
34 : 41	22 : 29	Program stored by LOAD switch on the processor panel
42 : 63	2A : 3F	First record read from peripheral device during a load operation
64 : 79	40 : 4F	Traps
80 : 87	50 : 57	Override interrupts
88 : 91	58 : 5B	Counter interrupts
92 : 95	5C : 5F	Input/output interrupts
96 : 319	60 : 13F	External interrupts

COMPUTER MODES

The SIGMA 5 computer operates in either the master mode or the slave mode. The mode of operation is determined by the state of the master/slave mode control bit in the arithmetic and control unit.

MASTER MODE

The master mode is the basic operating mode of the computer. In this mode, all legal SIGMA 5 operations are permissible. It is assumed that there is a resident executive program (operating in the master mode) that controls and supports the operation of other programs (which may be in the master mode or in the slave mode).

SLAVE MODE

The slave mode is the problem-solving mode of the computer. In this mode, certain "privileged" operations are prohibited. Privileged operations are those relating to input/output and to changes in the basic control state of the computer. All privileged operations are performed (in the master mode only) by a group of privileged instructions. Any attempt by a program to execute a privileged instruction while the computer is in the slave mode results in a return of control to the resident executive program. The master/slave mode control bit can be changed only when the computer is in the master mode; thus, a slave program cannot directly change the computer mode from slave to master. However, the slave program can gain direct access to certain executive program operations by means of CALL instructions without requiring executive program intervention. The operations available through CALL instructions are established by the resident executive program.

CPU FAST MEMORY

Several special (fast) memories may be used in a SIGMA 5 CPU. These memories consist of high-speed integrated circuits that are capable of delivering information to (or receiving information from) the arithmetic and control unit simultaneously with the operation of core memory modules. These integrated-circuit memories are not accessible to any other unit in a SIGMA 5 system.

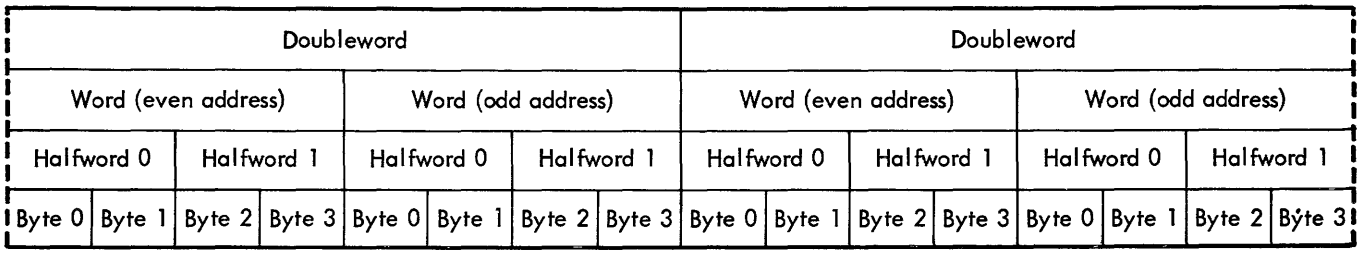


Figure 2. Information Boundaries

CENTRAL PROCESSING UNIT

This section describes the organization and operation of the SIGMA 5 central-processing unit in terms of information processing and program control, instruction and data formats, indirect addressing and indexing, memory write-protection, overflow and trap conditions, and interrupt control. Basically, the SIGMA 5 CPU consists of a fast memory and an arithmetic and control unit (see Figure 3).

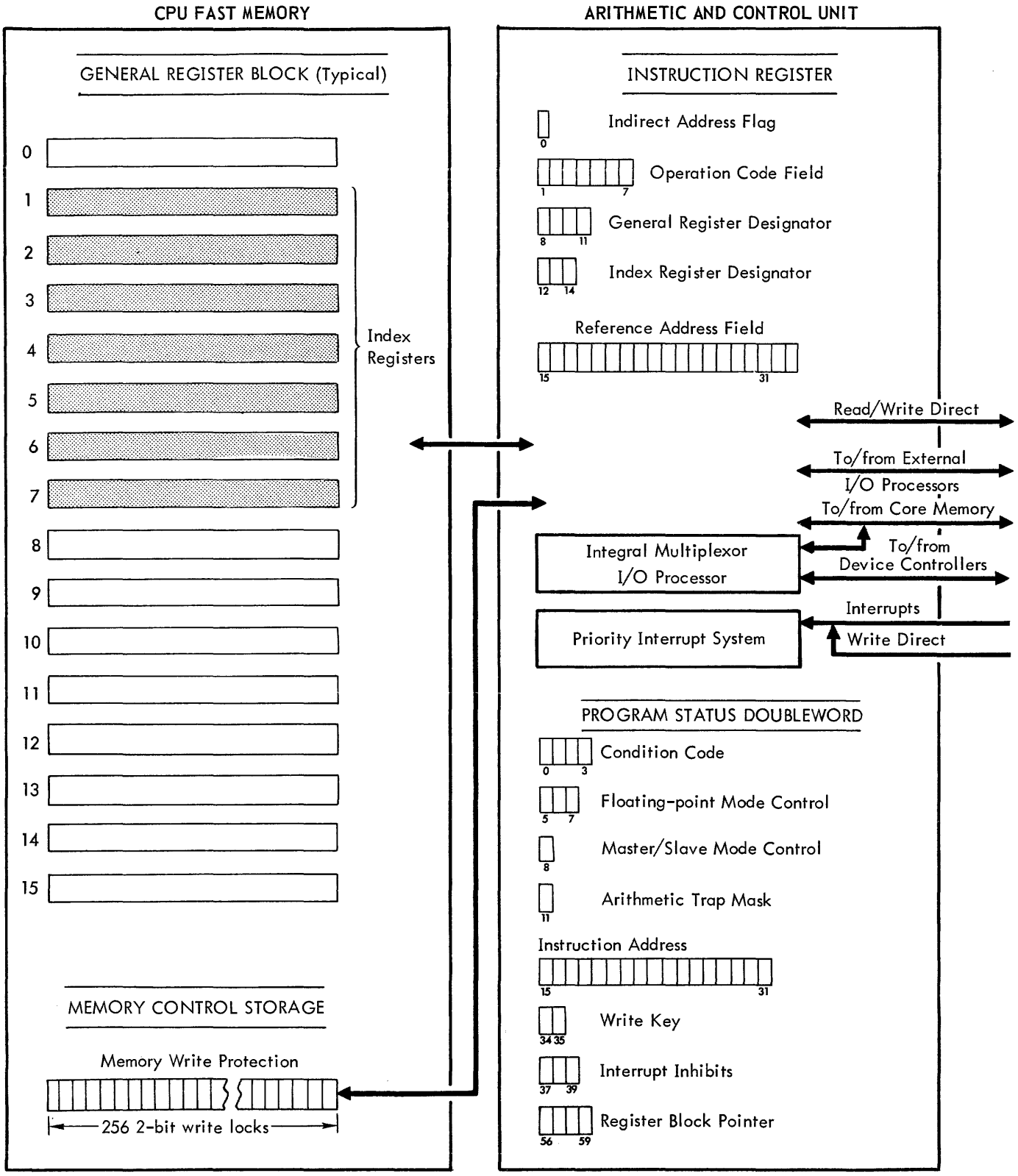


Figure 3. SIGMA 5 Central Processing Unit

GENERAL REGISTERS AND REGISTER BLOCK POINTER

An integrated-circuit memory, consisting of sixteen 32-bit words, is contained within the basic SIGMA 5 CPU for general-purpose register usage; these 16 words of fast memory are referred to as a register block. A SIGMA 5 system may contain up to 16 such register blocks, and a 4-bit control field (called the register block pointer) in the arithmetic and control unit selects the block currently available to a program. The 16 general registers selected by the register block pointer are referred to as the current register block. The register block pointer can be changed only when the computer is in the master mode, thus, a slave program cannot change the register block pointer.

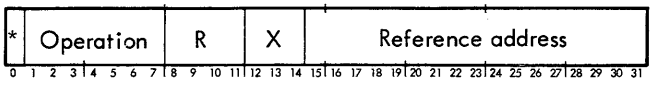
Each of the general registers in a register block is identified by a 4-bit code in the range 0000 through 1111 (0 through 15 in decimal, or X'0' through X'F' in hexadecimal notation). Any of the general registers can be used as fixed-point accumulators, floating-point accumulators, temporary storage, or to contain control information such as data addresses, counts, pointers, etc. Any (or all) of general registers 1 through 7 can be used as index registers.

MEMORY CONTROL STORAGE

An optional, high-speed integrated-circuit memory is available for storage of a set of memory write-protection codes, or locks, which can be changed only when the computer is in the master mode. The memory write-protection option includes the necessary integrated-circuit memory for the memory write locks. These locks operate in conjunction with a 2-bit field, called the write key, in the arithmetic and control unit. The locks and the key determine whether or not the program (slave or master) may alter the contents of specific regions of core memory. The write key can be changed only when the computer is in the master mode; thus the current write key cannot be changed by a slave program. (The functions of the locks and key are described in the section "Memory Write Protection".)

INSTRUCTION FORMATS

The normal SIGMA 5 memory addressing instruction has the following format:



* — This bit position indicates whether or not indirect addressing is to be performed. Indirect addressing is performed (one level only) if this bit position contains a 1, and is not performed if this bit position contains a 0.

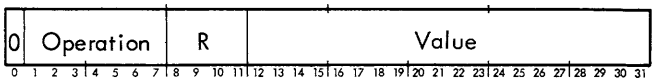
Operation — This 7-bit field contains the code that designates the operation to be performed.

R — This 4-bit field designates any of the 16 registers of the current register block as an operand source, result destination, or both.

X — This 3-bit field designates any one of registers 1-7 of the current register block as an index register. X = 0 designates no indexing; hence register 0 cannot be used as an index register.

Reference address — This 17-bit field contains the initial address of the instruction operand. The reference address field allows any word, doubleword, left halfword, or leftmost byte within a word in memory to be directly addressed. Halfword and byte operations require additional address bits for halfwords and bytes that do not begin on a word boundary. Thus, to address the second halfword of a word, the X field of the instruction must designate a register that contains a 1 in its low-order bit position. To address bytes 1, 2, or 3 of a word, the X field of the instruction must designate a register that contains 01, 10, or 11, respectively, in its two low-order bit positions. See "Indexing and Index Registers" for a more complete description of the SIGMA 5 indexing process.

Some SIGMA 5 instructions are of the immediate-addressing type. The format of these instructions provides for an operand within the instruction word itself, as shown below. The functions of the Operation and R fields are identical to those of the normal instruction format.



0 — This bit position is coded with a 0 because indirect addressing is not meaningful for this type of instruction. If indirect addressing is attempted, the computer treats the instruction as a nonexistent instruction.

Value — This field contains an operand that is 20 bits in length, with negative numbers represented in two's-complement form.

There are several methods by which an instruction word may specify the source of an operand or the destination of a result. These methods are explained below.

Immediate Operand

The operation code of an immediate-addressing instruction specifies that an operand is to be found in the value field (bit positions 12-31) of the instruction word itself and not in a general register or core memory location. The value field of this type of instruction cannot be modified by indexing. The following SIGMA 5 instructions are of the immediate-addressing type:

Instruction Name	Mnemonic	Page
Load Immediate	LI	26
Load Conditions and Floating Control Immediate	LCFI	30
Add Immediate	AI	34
Multiply Immediate	MI	36
Compare Immediate	CI	39

MEMORY REFERENCE ADDRESSES

Core Memory locations 0 through 15 are not accessible to the programmer because memory addresses 0 through 15 are reserved as register designators for register-to-register operations. Thus, an instruction can treat any register of the current register block as if it were a location in core memory. Furthermore, the register block can be used to hold an instruction (or a series of up to 16 instructions) for execution just as if the instruction (or instructions) were in core memory. The only restriction upon the use of the register block for instruction storage is:

> If an instruction accessed from a general register uses the R field of the instruction word to designate the next higher-numbered register and execution of the instruction would alter the contents of the register so designated, the contents of that register should not be used as the next instruction in sequence; otherwise, the operation of the instruction in the affected register is unpredictable.

In the maximum core memory configuration (131,072 words), memory addresses "wrap around" with address 0 (general register 0) being the next consecutive memory address after X'1FFFF'(131,071). Core memory location 16 follows general register 15 as the next location in ascending sequence. All SIGMA 5 instructions not of the immediate-address type are reference addressing instructions, which specify that the reference address field (bit positions 15-31) of the instruction is to be used as the initial address of the location where an operand is to be obtained (or the location where a result is to be stored), or as an initial instruction value.

Direct Reference Address. If neither indirect addressing nor indexing is called for by the instruction, the reference address field of the instruction is a direct reference address.

Indirect Reference Address. If indirect addressing is called for by the instruction (a 1 in bit position 0 of the instruction word), the reference address field is used to access a word location that contains the direct reference address in bit positions 15-31. The direct reference address then replaces the indirect reference address. Indirect addressing is limited to one level; only the reference address field of the indirect word is significant.

Indexed Reference Address. If indexing is called for by the instruction (a nonzero value in bit positions 12-14 of the instruction), the direct reference address is modified by addition of the displacement value in the general register (index) called for by the instruction (after scaling the displacement according to the instruction type). This final reference address value (after indirect addressing, indexing, or both) is defined as the effective address of the instruction. If indirect addressing and indexing are both called for in an instruction, the index displacement is not used to modify the indirect reference address, but is used to modify the direct reference address obtained from the location pointed to by the indirect reference address. This method of indexing after indirect addressing is called post-indexing.

Register Address. If any instruction produces an address that is a memory reference (i.e., a direct, indirect, or indexed reference address) in the range 0 through 15, the CPU does not attempt to read from or write into core memory. Instead, the 4 low-order bits of the reference address are used as a general register address, and the general register (of the current register block) corresponding to this address is used as the operand location or result destination. Thus, the instruction can use any register in the current register block as the source of an operand, the location of a direct address, or the destination of a result.

Effective Address

An effective address is defined as the final address produced for an instruction. The effective address is usually used as the address of an operand location or result destination. However, some instructions do not use the effective address as a location reference; instead, the effective address is used to control the operation of the instruction (as in a shift instruction), to designate the address of an input/output device (as in input/output instruction), or to designate a specific element of the system (as in a READ DIRECT or WRITE DIRECT instruction).

Effective Location

An effective location is defined to be the location in core memory or in the current register block that is to receive the result of a memory-referencing instruction, and is referred to by means of an effective address (whether the effective address refers to core memory or to a general register).

Effective Operand

An effective operand is defined to be the contents of a location in core memory or in the current register block that is to be used as an operand by a memory-referencing instruction, and is referred to by means of an effective address.

ADDRESS MODIFICATION

Indirect Addressing

The 7-bit operation code field of the SIGMA 5 instruction word format provides for up to 128 instruction operation codes, nearly all of which can use indirect addressing (the exceptions, already mentioned, are the immediate-addressing instructions). The indirect addressing operation is limited to one level, as called for by the indirect address bit (bit position 0) of the instruction word. Indirect addressing does not proceed to further levels, regardless of the contents of the word location pointed to by the reference address field of the instruction. Indirect addressing occurs before indexing; that is, the 17-bit reference address field of the instruction is used to obtain a word, and the 17 low-order bits of the word thus obtained effectively replace the initial reference field; then, indexing is carried out according to the operation code of the instruction.

Indexing and Index Registers

The X field of the normal instruction format permits any one of registers 1 through 7 in the current register block to be designated as an index register. The contents of this register are then treated as a 32-bit displacement value.

The indexing technique employed in SIGMA is unique. SIGMA instructions provide for operations on bytes, halfwords, words, and doublewords. These units of information are typically organized in lists that are processed sequentially. The SIGMA indexing technique is based on the concept that the index register contains an integer value (k) that permits the accessing of the kth item of a list (where k = 0 refers to the first item, k = 1 refers to the second item, etc.), independent of the kind of data that is in the list. Thus, a byte-addressing instruction that is indexed accesses the kth byte of a list; a halfword-addressing instruction that refers to the same index register obtains the kth halfword of a list; a word-addressing instruction that refers to the same index register obtains the kth word of a list; and a doubleword-addressing instruction that is indexed with the same register obtains the kth doubleword of a list.

Figure 4 shows how the indexing operation takes place. As the instruction is brought from memory, it is loaded into a 34-bit instruction register that initially contains 0's in the 2 low-order bit positions (32 and 33). The displacement value from the index register is then aligned with the instruction register (as an integer) relative to the addressing type of the instruction. That is, if it is a byte-addressing instruction, the displacement is lined up so that its low-order bit is aligned with the least significant bit of the 34-bit instruction register. The displacement is shifted one bit to the left of this position for a halfword-addressing instruction, two bits to the left for a word-addressing instruction, and three bits to the left for a doubleword-addressing instruction. An addition process then takes place to develop a 19-bit address, which is referred to as the effective address of the instruction. High-order bits of the 32-bit displacement field are ignored in the development of this effective address (i.e., the 15 high-order bits are ignored for word operations, the 25 high-order bits are ignored for shift operations, and the 16 high-order bits are ignored for doubleword operations). However, the displacement value can cause the effective address to be less than the initial reference address within the instruction if the displacement value contains a sufficient number of high-order 1's (i.e., the displacement is a negative integer in two's complement form).

The effective address of an instruction is always a 19-bit byte address value; however, this value is automatically adjusted to the SIGMA 5 information boundary conventions. Thus, for halfword-addressing instructions, the low-order bit of the effective halfword address is 0, for word-addressing instructions, the 2 low-order bits of the effective word address are 0's; and for doubleword-addressing instructions, the 3 low-order bits of the effective doubleword address are 0's.

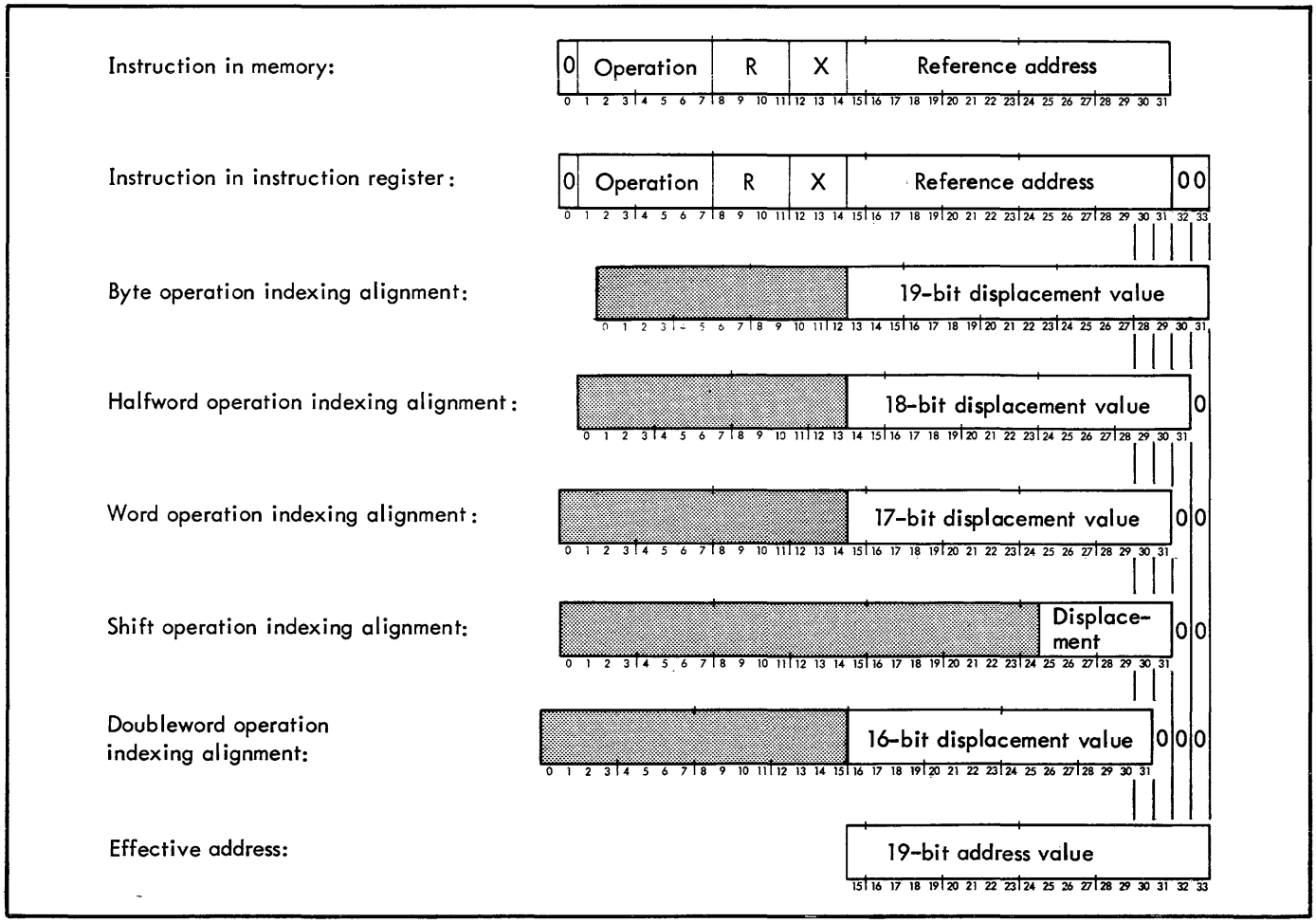


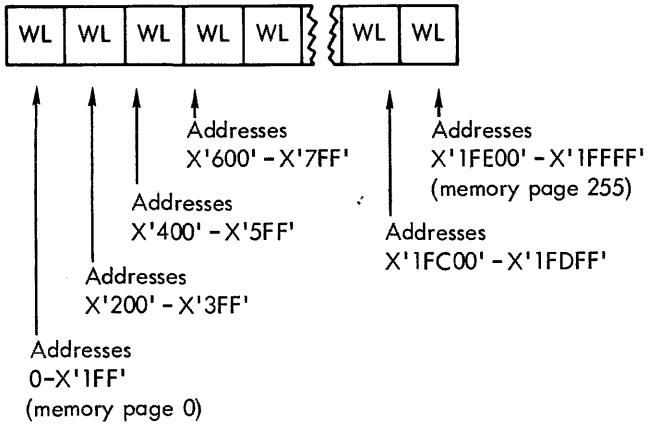
Figure 4. Index Displacement Alignment

If no indexing is used with a byte-addressing instruction, the effective byte is the first byte (bit positions 0-7) of a word location, if no indexing is used with a halfword-addressing instruction, the effective halfword is the first halfword (bit positions 0-15) of a word location. A doubleword operation always involves a word at an even-numbered word address and the word at the next sequential (odd-numbered) word address. If an odd-numbered word location is specified in a doubleword-addressing instruction, the low-order bit of the effective address field (bit position 31) is automatically forced to 0. Thus, an odd-numbered word address (referring to the middle of a doubleword) designates the same doubleword as an even-numbered word address, when used in a doubleword-addressing instruction.

MEMORY WRITE PROTECTION

With a SIGMA 5 computer, an optional method is available for controlling the use of core memory by a program: the lock and key technique implemented in the memory write-protection feature.

This feature provides a 2-bit write-protect lock (WL) for each 512-word page of core memory addresses. Thus, there are 256 of these locks, each one assigned to a 512-word page of addresses as follows:



The write-protect locks can be changed only by the execution of the privileged instruction MOVE TO MEMORY CONTROL (see "Control Instructions", Chapter 3).

The write-key (a 2-bit field in the arithmetic and control unit) works in conjunction with the lock storage to determine whether or not the program (whether slave or master) can write into a specific block of memory. The keys and locks control access for writing, according to the following rules:

A lock value of 00 means that the corresponding memory block is "unlocked"; write access to that block is permitted independent of the key value.

A key value of 00 is a "skeleton" key that will open any lock; thus, write access to any memory block is permitted independent of its lock value.

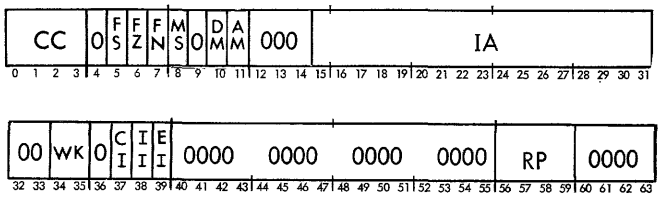
A lock value other than 00 for a memory block permits write access to that block only if the key value is identical to the lock value.

Thus, a program can write into a given memory block if the lock value is 00, if the key value is 00, or if the key value matches the lock value.

If an instruction attempts to write into a write-protected memory page, the computer aborts the instruction, and traps to location X'40', which is the "nonallowed operation" trap (see "Trap System").

PROGRAM STATUS DOUBLEWORD

The critical control conditions of the SIGMA 5 CPU can be defined within 64 bits of information. These 64 bits are collectively referred to as the current program status doubleword (PSD). The current PSD can be considered as a 64-bit internal CPU register, although it actually exists as a collection of separate registers and flip-flops. When stored in memory, the PSD is always in the following format:



Designation	Function
CC	Condition code. This generalized 4-bit code indicates the nature of the results of an instruction. The significance of the condition code bits depends on the particular instruction just executed. After an instruction is executed, the instructions BRANCH ON CONDITIONS SET (BCS) and BRANCH ON CONDITIONS RESET (BCR) can be used, singly or in combination, to test for a particular condition code setting (these instructions are described in "Execute/Branch Instructions", Chapter 3). In some operations only a portion of the condition code is involved; thus, the term CC1 refers to the first bit of the condition code, CC2 to the second bit, CC3 to the third bit, and CC4 to the fourth bit. Any program (slave or master mode) can change the current value of the condition code by executing either the instruction LOAD CONDITIONS AND FLOATING CONTROL IMMEDIATE (LCFI) or the instruction LOAD CONDITIONS AND FLOATING CONTROL (LCF); any program can store the current condition code by executing STORE CONDITIONS AND FLOATING CONTROL (STCF). These instructions are described in "Load/Store Instructions", Chapter 3.
FS	Floating significance mode control
FZ	Floating zero mode control
FN	Floating normalize mode control The three floating-point mode bits (FS, FZ, and FN) control the operation of the computer with respect to floating-point significance checking, the generation of zero results, and the normalization

Designation	Function
	of the results of floating-point additions and subtractions, respectively. (The floating-point mode controls are described in "Floating-point Instructions", Chapter 3). Any program (slave or master) can change the state of the current floating-point mode controls by executing either the instruction LCFI or the instruction LCF; any program can store the current state of the current floating-point mode controls by executing the instruction STCF.
MS	Master/slave mode control. The computer is in the master mode when this bit is a 0; it is in the slave mode when this bit is a 1. The master/slave mode control cannot directly be changed by a slave program, however, a master mode program can change the control by executing either the instruction LOAD PROGRAM STATUS DOUBLEWORD (LPSD) or the instruction EXCHANGE PROGRAM STATUS DOUBLEWORD (XPSD). These two privileged instructions are described in "Control Instructions", Chapter 3.
DM	Decimal mask. This bit position is used only to preserve the status of the decimal arithmetic fault trap mask when a SIGMA 7 program is being executed. The decimal mask bit does not affect the operation of the SIGMA 5 computer in any other way.
AM	Arithmetic mask. The fixed-point arithmetic overflow trap is in effect when this bit is a 1; the trap is not in effect when this bit is a 0. The instructions that can cause fixed-point overflow are described in the section "Trap System". The arithmetic trap mask cannot be changed by a slave program; a master mode program can change the mask by executing either the instruction LPSD or the instruction XPSD.
IA	Instruction address. This 17-bit field contains the address of the next instruction to be executed.
WK	Write key. This field contains the 2-bit key used in conjunction with the optional memory protection feature. A slave program cannot change the current write key; a master mode program can change the write key by executing either the instruction LPSD or the instruction XPSD.
CI	Counter interrupt group inhibit
II	Input/output interrupt group inhibit
EI	External interrupt group inhibit
	The three interrupt inhibit bits (CI, II, and EI) determine whether an interrupt can occur. The functions of the interrupt inhibits are described in the section "Interrupt System". A slave program cannot change the state of the interrupt inhibits; a master mode program can change the interrupt inhibits by executing LPSD, XPSD, or the instruction WRITE DIRECT (WD). The WD instruction is described in "Control Instructions", Chapter 3.
RP	Register pointer. This 4-bit field selects one of the 16 possible blocks of general-purpose registers as the current register block. A slave program cannot change the register pointer; a master mode program can change the register pointer by executing LPSD, XPSD, or the instruction LOAD REGISTER POINTER (LRP). The LRP instruction is described in the section "Control Instructions".

INTERRUPT SYSTEM

The SIGMA 5 priority interrupt system is an improved version of the system used successfully in SDS 900/9300 series computers. Up to 237 interrupt levels are normally available, each with a unique location (see Table 2) assigned in core memory, each with a unique priority, and each capable of being selectively armed and/or enabled by the CPU. Also, any interrupt level can be "triggered" by the CPU (supplied with a signal at the same physical point where the signal from the external source would enter the interrupt level). The triggering of an interrupt permits the testing of special systems programs before the special systems equipment is actually attached to the computer, and also permits an interrupt-servicing routine to defer a portion of the processing associated with an interrupt level by processing the urgent portion of an interrupt-servicing routine, triggering a lower-priority level (for a routine that handles the less-urgent part), then clearing the high-priority interrupt level so that other interrupts may occur before the deferred interrupt response is processed.

SIGMA 5 interrupts are arranged in groups that are connected in a predetermined priority chain by groups of levels. The priority of each level within a group is fixed: the first has the highest priority and the last level the lowest. The user has the option of ordering a machine with a priority chain starting with the override group and connecting all remaining groups in any sequence. This allows the user to establish external interrupts above, between, or below the counter and input/output groups of internal interrupts. Figure 5 illustrates this with a configuration that a typical user might establish; where (after the override group) the counter group of internal interrupts is given the second highest priority, followed by the first group of external interrupts, then the input/output group of internal interrupts, and finally all succeeding groups of external interrupts.

INTERNAL INTERRUPTS

Internal interrupts include the standard interrupts normally supplied with a SIGMA 5 system, as well as the optional power fail-safe and the additional counter interrupts.

Override Group (Locations X'50' to X'56'

The seven interrupt levels of this group always have the highest priority in a Sigma 5 system.

The power on and power off interrupt levels are included in the optional power fail-safe feature.

Table 2. SIGMA 5 Interrupt Locations

Location Dec.	Location Hex.	WRITE DIRECT Register bit†	Function	Availability	PSD Inhibit	WRITE DIRECT Group code††
80	50	none	Power on	optional (as a set)	none	none
81	51	none	Power off			
82	52	16	Counter 1 count pulse	optional (as a set)		X'0'
83	53	17	Counter 2 count pulse			
84	54	18	Counter 3 count pulse	standard		
85	55	19	Counter 4 count pulse			
86	56	20	Memory parity			
87	57		Unassigned			
88	58	22	Counter 1 equals zero	optional (as a set)	CI	
89	59	23	Counter 2 equals zero			
90	5A	24	Counter 3 equals zero	standard		
91	5B	25	Counter 4 equals zero			
92	5C	26	Input/output	standard	II	
93	5D	27	Control panel			
94	5E		Unassigned			
95	5F					
96	60	16	External Group 2	optional	EI	X'2'
⋮	⋮	⋮				
111	6F	31				
112	70	16	External Group 3			X'3'
⋮	⋮	⋮				
127	7F	31				
⋮	⋮	⋮	⋮			⋮
288	120	16	External Group 14			X'E'
⋮	⋮	⋮				
303	12F	31				
304	130	16	External Group 15			X'F'
⋮	⋮	⋮				
319	13F	31				

†When the privileged instruction WRITE DIRECT is used in the interrupt control mode to operate on interrupt levels, the interrupt levels are selected by specific bit positions in register R. The numbers in this column indicate the bit positions in register R that correspond to the various interrupt levels.

††The numbers in this column indicate the group codes (for use with WRITE DIRECT) of the various interrupt levels.

The override group can also contain 2 or 4 count-pulse interrupt levels that are triggered by pulses from clock sources. Counters 1, 2, and 3 can be individually set to any of five manually switchable frequencies—the commercial line frequency, 50 Hz, 2kHz, 8kHz, and a user-supplied external signal — that may be different for each counter. Counter 4 has a constant frequency of 500 Hz. All counter frequencies are synchronous, except for the line frequency and the signal supplied by the user. Each of the count-pulse interrupt locations must contain one of the modify and test instructions, MTB, MTH, or MTW. The results of any other instruction are unpredictable when the instruction is executed as the result of a count-pulse interrupt level advancing to the active state. When the modification of the effective byte, halfword, or word causes a zero result, the appropriate counter-equals-zero interrupt level is triggered (see "Counter-Equals-Zero Group").

The override group also includes a memory parity interrupt level that is triggered whenever a memory parity error is reported to the CPU.

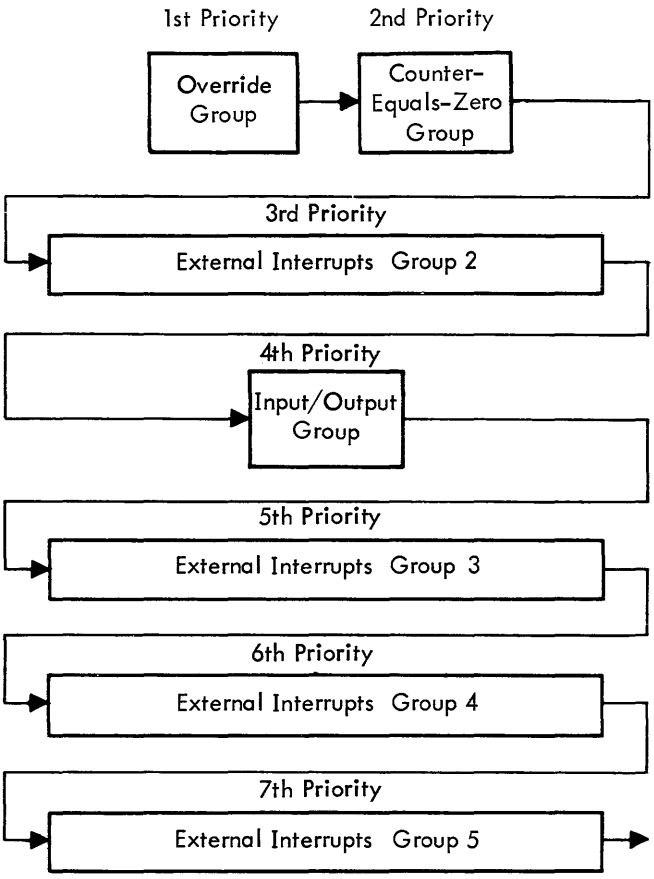


Figure 5. Typical Interrupt Priority Chain

Counter-Equals-Zero Group (Locations X'58' to X'5B')

Each interrupt level in the counter group (called a counter-equals-zero interrupt) is associated with a count-pulse interrupt level in the override group. When the execution of a modify and test instruction in the count-pulse interrupt location causes a zero result in the effective byte, halfword, or word location, the corresponding counter-equals-zero interrupt is triggered.

All of the counter-equals-zero interrupt levels can be inhibited or permitted as a group. If bit position 37 (CI) of the current program status doubleword contains a 0, the counter-equals-zero interrupt levels are allowed to interrupt the program being executed. However, if the CI bit is a 1, the counter-equals-zero interrupt levels are not allowed to interrupt the program; also, the interrupt levels are effectively removed from the priority chain, allowing a lower-priority interrupt level to interrupt the program even if a counter-equals-zero interrupt level is currently in the waiting state.

Input/Output Group (Locations X'5C' and X'5D')

This interrupt group includes two standard interrupts: the I/O interrupt and the control panel interrupt. The I/O interrupt level accepts interrupt signals from the standard I/O system. The I/O interrupt location normally contains an EXCHANGE PROGRAM STATUS DOUBLEWORD (XPSD) instruction that transfers program control to a routine for servicing all I/O interrupts. The I/O routine then contains an ACKNOWLEDGE I/O INTERRUPT (AIO) instruction that identifies the source and reason for the interrupt.

The control panel interrupt level is connected to the INTERRUPT switch on the processor control panel. The control panel interrupt level can thus be triggered by the computer operator, allowing him to initiate a specific routine.

The interrupts in the input/output group can be inhibited or permitted by means of bit position 38 (II) of the program status doubleword. If II is a 0, the interrupts in the I/O group are allowed to interrupt the program being executed. However, if the II bit is a 1, the interrupts are inhibited from interrupting the program, and are effectively removed from the interrupt priority chain.

EXTERNAL INTERRUPTS

A SIGMA 5 system can contain up to 14 groups of optional interrupt levels, with 16 levels in each group. As shown in Figure 5, the groups can be connected in any priority sequence.

All external interrupts can be inhibited or permitted by means of bit position 39 (EI) of the program status doubleword. If EI is a 0, external interrupts are allowed to interrupt the program; however, if EI is a 1, all external interrupts are inhibited and effectively removed from the priority chain.

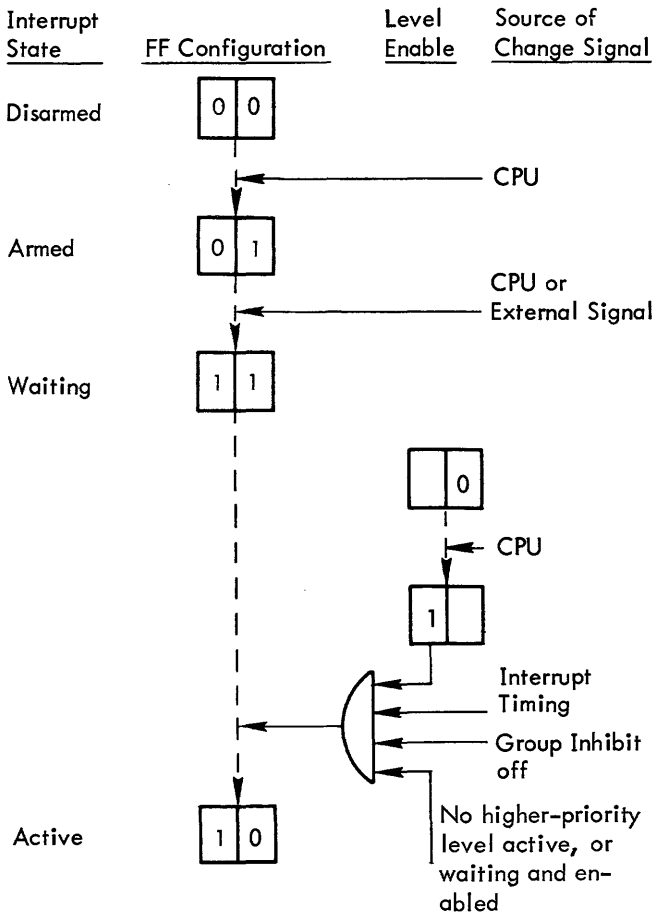


Figure 6. Interrupt Level Operation

STATES OF AN INTERRUPT LEVEL

A SIGMA 5 interrupt level is mechanized by means of three flip-flops. Two of the flip-flops are used to define any of four mutually exclusive states: disarmed, armed, waiting, and active. The third flip-flop is used as a level-enable. The various states and conditions causing them to change state (see Figure 6) are described in the following paragraphs.

Disarmed

When an interrupt level is in the disarmed state, no signal to that interrupt level is admitted; that is, no record is retained of the existence of the signal, nor is any program interrupt caused by it at any time.

Armed

When an interrupt level is in the armed state, it is to accept and remember an interrupt signal. The receipt of such a signal advances the interrupt level to the waiting state.

Waiting

When an interrupt level in the armed state receives an interrupt signal, it advances to the waiting state, and remains in the waiting state until it is allowed to advance to the active state. If the level-enable flip-flop is off, the interrupt level can undergo all state changes except that of moving from the waiting to the active state. Furthermore, if this flip-flop is off, the interrupt level is completely removed from the chain that determines the priority of access to the CPU. Thus, an interrupt level in the waiting state with its level-enable in the off condition does not prevent an enabled, waiting interrupt of lower priority from moving to the active state.

When an interrupt level is in the waiting state, the following conditions must all exist simultaneously before the level advances to the active state.

1. The level must be enabled (i.e., its level-enable flip-flop must be set to 1).
2. The CPU must be at an interruptible point in the execution of a program.
3. The group inhibit (CI, II, or EI, if applicable) must be off (i.e., the appropriate inhibit in the PSD must be a 0.
4. No higher-priority interrupt level is in the active state, or is in the waiting state and totally enabled (i.e., enabled and not inhibited).

Active

When an interrupt level meets all of the conditions necessary to permit it to move from the waiting state to the active state, it is permitted to do so by being acknowledged by the computer, which then executes the contents of the assigned interrupt location as the next instruction. The instruction address portion of the program status doubleword remains unchanged until the instruction in the interrupt location is executed. The instruction in the interrupt location must be one of the following: EXCHANGE PROGRAM STATUS DOUBLEWORD (XPSD), MODIFY AND TEST BYTE (MTB), MODIFY AND TEST HALFWORD (MTH), or MODIFY AND TEST WORD (MTW). If the execution of any other instruction in an interrupt location is attempted as the result of an interrupt level advancing to the active state, the results of the instruction are unpredictable.

The use of the privileged instruction EXCHANGE PROGRAM STATUS DOUBLEWORD (XPSD) in an interrupt location permits an interrupt-servicing routine to save the entire current machine environment and establish a new environment. If working registers are needed by the routine and additional register blocks are available, the contents of the current register block can be saved automatically with no time loss. This is accomplished by changing the value of the register pointer, which results in the assignment of a new block of 16 registers to the routine.

An interrupt level remains in the active state until it is cleared (removed from the active state) by the execution of the instruction LOAD PROGRAM STATUS DOUBLEWORD (LPSD) or the instruction WRITE DIRECT (WD). (See "Control Instructions" for the detailed descriptions of LPSD and WD.) An interrupt-servicing routine can itself be interrupted (whenever a higher-priority interrupt level meets all of the conditions for becoming active) and then continued (after the higher-priority interrupt is cleared). However, an interrupt-servicing routine cannot be interrupted by a lower-priority interrupt as long as it remains in the active state. Normally, the interrupt-servicing routine clears its interrupt and transfers program control back to the point of interrupt by means of an LPSD instruction with the same effective address as the XPSD instruction in the interrupt location.

CONTROL OF THE INTERRUPT SYSTEM

The SIGMA 5 system has two points of interrupt control. One point of control is achieved by means of the interrupt inhibits in the program status doubleword. The interrupt inhibits can be changed by executing XPSD, LPSD, or a WD instruction.

The second point of interrupt control is at the individual interrupt level. The WD instruction can be used to individually arm, disarm, enable, disable, or trigger any interrupt level (except for the power fail-safe interrupts, which are always armed, always enabled, never inhibited, and have the highest priority). The detailed operation of the WD instruction is described in the section "Control Instructions".

TIME OF INTERRUPT OCCURRENCE

The SIGMA 5 CPU permits an interrupt to occur during the following time intervals (related to the execution cycle of an instruction) providing the control panel COMPUTE switch is in the RUN position and no "halt" condition exists:

1. Between instructions: An interrupt is permitted between the completion of any instruction and the initiation of the next instruction.

2. Between instruction iterations: An interrupt is also permitted to occur during the execution of the instruction Move to Memory Control (MMC). The control and intermediate results of this instruction reside in registers and memory; thus, the instruction can be interrupted between the completion of one iteration (operand execution cycle) and the point in time (during the next iteration) when a memory location or register is modified. If an interrupt occurs during this time, the current iteration is aborted and the instruction address portion of the program status doubleword remains pointing to the interrupted instruction. After the interrupt-processing routine is completed, the instruction continues from the point at which it was interrupted and does not begin anew.

SINGLE-INSTRUCTION INTERRUPTS

A single-instruction interrupt is a situation where an interrupt level is activated, the current program is interrupted, the single instruction in the interrupt location is executed, the interrupt level is automatically cleared and armed, and the interrupted program continues without being disturbed or delayed (except for the time required for the single instruction).

If any of the following instructions is executed in any interrupt location, then that interrupt automatically becomes a single-instruction interrupt.

Instruction Name	Mnemonic	Page
Modify and Test Byte	MTB	38
Modify and Test Halfword	MTH	38
Modify and Test Word	MTW	38

The modify and test instruction modifies the effective byte, halfword, or word (as described in the section "Fixed-point Arithmetic Instructions") but the current condition code remains unchanged (even if overflow occurs). The execution of a modify and test instruction in an interrupt location is independent of the write-protection locks; thus, a memory protection violation trap cannot occur (a nonexistent memory address trap can occur). Also, the fixed-point overflow trap cannot occur as the result of overflow caused by executing MTH or MTW in an interrupt location.

The execution of a modify and test instruction in a count-pulse interrupt location automatically clears and arms the corresponding interrupt level, allowing the interrupted program to continue. When a modify and test instruction is executed in a count-pulse interrupt location, all the above conditions apply, in addition to the following: if the resultant value in the effective location is zero, the corresponding counter-equals-zero interrupt level is triggered.

TRAP SYSTEM

When a condition that is to result in an interrupt is sensed, a signal is sent to an interrupt level. If that level is "armed" it advances to the waiting state. When all of the conditions for its acknowledgment have been achieved, the interrupt level eventually advances to the active state, where it finally causes the computer to take an instruction from a specific location in memory. The computer may execute many instructions between the time that the interrupt requesting condition is sensed and the time that the actual interrupt acknowledgment occurs. However, detecting any of the conditions listed in Table 3 results in a trap (the immediate execution of the instruction in a unique location in memory).

When a trap condition occurs, the CPU sets the trap state. Depending on the type of trap, the instruction currently being executed by the CPU may or may not be carried to completion. In any event, the instruction is terminated with a trap sequence. In this sequence, the instruction address (IA) portion of the program status doubleword (PSD), which has already been incremented by 1, is decremented by 1 and then the instruction in the location associated with the trap is executed. An interrupt acknowledgment cannot occur until the execution of the instruction in the trap location is completed. The instruction in the trap location must be an XPSD instruction; if the execution of any other instruction in a trap location is attempted as the result of a trap activation, the results of the instruction are unpredictable. No memory protection violation or privileged instruction violation can occur as a result of executing an XPSD instruction in a trap location. The detailed operation of XPSD is described in "Control Instructions", Chapter 3.

NONALLOWED OPERATIONS

The occurrence of one of the nonallowed operations always causes the computer to abort the instruction being executed (at the time that the nonallowed operation is detected) and to immediately execute the instruction in trap location X'40'.

Nonexistent Instruction

Any instruction that is neither standard nor optional on SIGMA 5 is defined as nonexistent (this includes immediate-addressing instructions that are indirectly addressed). If execution of a nonexistent instruction is attempted, the computer traps to location X'40 at the time the instruction is decoded. The operation of the XPSD instruction in trap location X'40' (with respect to the condition code and instruction address portions of the PSD) is as follows:

1. Store the current PSD. The condition code stored is that which existed at the end of the instruction executed immediately prior to the nonexistent instruction. The instruction address stored is the address of the nonexistent instruction.

Table 3. Summary of SIGMA 5 Trap System

Location Dec.	Location Hex.	Trap Condition	PSD Mask Bit	Time of Occurrence	Special Action During XPSD
64	40	Nonallowed operation	none		
		1. Nonexistent instruction		Instruction decode	Set CC1 after new CC is loaded from memory. If bit 9 of XPSD is 1, add 8 to the new instruction address value loaded from memory.
		2. Nonexistent memory address		Prior to memory access	Set CC2 after new CC is loaded from memory. If bit 9 of XPSD is 1, add 4 to the new instruction address value loaded from memory.
		3. Privileged instruction in slave mode		Instruction decode	Set CC3 after new CC is loaded from memory. If bit 9 of XPSD is 1, add 2 to the new instruction address value loaded from memory.
		4. Memory protection violation		Prior to memory access	Set CC4 after new CC is loaded from memory. If bit 9 of XPSD is 1, add 1 to the new instruction address value loaded from memory.
65	41	Unimplemented instruction	none	Instruction decode	none
66	42	Push-down stack limit reached	TW,TS[†]	At time of stack limit detection	none
67	43	Fixed-point arithmetic overflow	AM	For all instruction except DW and DH, trap occurs after completion of instruction. For DW and DH, instruction is aborted with memory, registers, CC1, CC3, CC4 unchanged.	none
68	44	Floating-point fault			
		1. Characteristic overflow	none	At time of fault detection; the condition code is set to indicate the reason for the trap	none
		2. Divide by zero	none		
		3. Significance check	FS,FZ, FN		
70	46	Watchdog timer runout	none	At time of runout	none
72	48	CALL 1	none	Instruction decode	The R field of the CALL instruction is ORed into new CC settings loaded from memory. If bit 9 of XPSD is 1, the R field of the CALL instruction is added to the new instruction address value loaded from memory.
73	49	CALL 2	none	Instruction decode	
74	4A	CALL 3	none	Instruction decode	
75	4B	CALL 4	none	Instruction decode	

[†]The push-down stack limit trap is masked within the stack pointer doubleword for each push-down stack (see page 49).

2. Load the new PSD. The current PSD is replaced by the contents of the doubleword location following the doubleword location in which the current PSD was stored.
3. Modify the new PSD:
    a. Set CC1 to 1 (CC2, CC3, and CC4 remain set at the values loaded from memory).
    b. If bit position 9 of XPSD contains a 1, the instruction address loaded from memory is incremented by 8. If bit position 9 of XPSD contains a 0, the instruction address remains at the value loaded from memory.

Nonexistent Memory Address

Any attempt to access a nonexistent memory address causes a trap to location X'40' at the time of the request for memory service. The operation of XPSD in trap location X'40' is as follows:

1. Store the current PSD. The condition code stored is that which existed immediately prior to the instruction that attempted to access a nonexistent memory address. The instruction address stored is the address of the instruction that attempted to access a nonexistent memory address. If an instruction execution is followed by an access to a nonexistent memory address for the next instruction in sequence, the stored instruction address is the nonexistent memory address.
2. Load the new PSD.
3. Modify the new PSD:
    a. Set CC2 to 1 (CC1, CC3, and CC4 remain set at the values loaded from memory).
    b. If bit position 9 of XPSD contains a 1, the instruction address loaded from memory in incremented by 4. If bit position 9 of XPSD contains a 0, the instruction address remains at the value loaded from memory.

Privileged Instruction in Slave Mode

An attempt to execute a privileged instruction while the CPU is in the slave mode causes a trap to location X'40' at the time of instruction decoding. The operation of XPSD in trap location X'40' is as follows:

1. Store the current PSD. The condition code stored is that which existed immediately prior to the privileged instruction. The instruction address stored is the address of the privileged instruction.
2. Load the new PSD.
3. Modify the new PSD:
    a. Set CC3 to 1 (CC1, CC2, and CC4 remain set at the values loaded from memory).
    b. If bit position 9 of XPSD contains a 1, the instruction address loaded from memory is incremented by 2. If bit position 9 of XPSD contains a 0, the instruction address remains at the value loaded from memory.

The operation codes 0C, 0D, 2C, 2D and their indirectly addressed forms, 8C, 8D, AC, AD, are both nonexistent and privileged. If one of these operation codes is used while the CPU is in the slave state, both CC1 and CC3 will be set to 1's after the new PSD has been loaded, and if bit position 9 of XPSD contains a 1, the instruction address loaded from memory is incremented by 10.

Memory Write-Protection Violation

A memory protection violation occurs when any instruction attempts to alter write-protected memory and the current write key is nonzero and does not match the write lock for the memory page. When a memory protection violation occurs, the CPU aborts execution of the current instruction (without changing protected memory) and traps to location X'40'. The operation of the XPSD in trap location X'40' is as follows:

1. Store the current PSD. The condition code stored is that which existed immediately prior to the instruction attempting to alter protected memory. The instruction address stored is the address of the instruction that attempted to alter protected memory.
2. Load the new PSD.
3. Modify the new PSD:
    a. Set CC4 to 1 (CC1, CC2, and CC3 remain at the values loaded from memory).
    b. If bit position 9 of XPSD contains a 1, the instruction address loaded from memory is incremented by 1. If bit position 9 of XPSD contains a 0, the instruction address remains at the value loaded from memory.

An attempt to access a memory location that is both write-protected and nonexistent causes both CC2 and CC4 to be set to 1's after the new PSD has been loaded, and if bit position 9 of XPSD contains a 1, the instruction address loaded from memory is incremented by 5.

UNIMPLEMENTED INSTRUCTIONS

There is on optional SIGMA 5 instruction group, the floating-point option, which includes the following instructions:

Instruction Name	Mnemonic	Page
Floating Add Short	FAS	47
Floating Add Long	FAL	47
Floating Subtract Short	FSS	47
Floating Subtract Long	FSL	48
Floating Multiply Short	FMS	48
Floating Multiply Long	FML	48
Floating Divide Short	FDS	48
Floating Divide Long	FDL	48

If an attempt is made to execute an instruction in this group when the floating-point option is not implemented, the computer traps to location X'41'.

The operation of the XPSD in trap location X'41' is as follows:

1. Store the current PSD. The condition code stored is that which existed immediately prior to the unimplemented instruction. The instruction address stored is the address of the unimplemented instruction.

2. Load the new PSD. The condition code and the instruction address portions of the PSD remain at the values loaded from memory.

Note: The Move to Memory Control (MMC) instruction is always considered implemented even if the memory-protection option is not implemented.

PUSH-DOWN STACK LIMIT REACHED

Push-down stack overflow or underflow can occur during execution of any of the following instructions:

Instruction Name	Mnemonic	Page
Push Word	PSW	50
Pull Word	PLW	50
Push Multiple	PSM	51
Pull Multiple	PLM	51
Modify Stack Pointer	MSP	52

During the execution of any stack-manipulating instruction (see "Push-down Instructions") the stack is either pushed (words added to stack) or pulled (words removed from stack). In either case, the space count and word count fields of the stack pointer doubleword are tested prior to moving any words. If execution of the instruction would cause the space count to become less than 0 or greater than $2^{15}-1$, the instruction is aborted with memory and registers unchanged; then, if bit 32 (TS) of the stack pointer doubleword is 0, the CPU traps to location X'42'. If execution of the instruction would cause the word count to become less than 0 or greater than $2^{15}-1$, the instruction is aborted with memory and registers unchanged; then, if bit 48 (TW) of the stack pointer doubleword is a 0, the CPU traps to location X'42'. The execution of XPSD in trap location X'42' is as follows:

1. Store the current PSD. The condition code stored is that which existed immediately prior to the aborted push-down instruction. The instruction address stored is the address of the aborted push-down instruction.

2. Load the new PSD. The condition code and instruction address portions of the PSD remain at the values loaded from memory.

FIXED-POINT OVERFLOW

Fixed-point overflow can occur for any of the following instructions:

Instruction Name	Mnemonic	Page
Load Complement Word	LCW	28
Load Absolute Word	LAW	28
Load Complement Doubleword	LCD	28
Load Absolute Doubleword	LAD	28
Add Immediate	AI	34
Add Halfword	AH	34
Add Word	AW	34
Add Doubleword	AD	35
Subtract Halfword	SH	35
Subtract Word	SW	35
Subtract Doubleword	SD	35
Divide Halfword	DH	37
Divide Word	DW	37
Add Word to Memory	AWM	37
Modify and Test Halfword	MTH	38
Modify and Test Word	MTW	38

Except for the instructions DIVIDE HALFWORD (DH) and DIVIDE WORD (DW), the instruction execution is allowed to proceed to completion, CC2 is set to 1 and CC3 and CC4 represent the actual result (0, -, or +) after overflow. If the fixed-point arithmetic trap mask (bit 11 of PSD) is a 1, the CPU traps to location X'43' instead of executing the next instruction in sequence.

For DW and DH, the instruction execution is aborted without changing any register and CC2 is set to 1; but CC1, CC3, and CC4 remain unchanged from their values at the end of the instruction immediately prior to the DW or DH. If the fixed-point arithmetic trap mask (AM) is a 1, the CPU traps to location X'43' instead of executing the next instruction in sequence.

The execution of XPSD in trap location X'43' is as follows:

1. Store the current PSD. If the instruction causing the trap was an instruction other than DW or DH, the stored condition code is interpreted[†] as follows:

1[††]	2	3	4	Significance
-	1	0	0	result after overflow is zero
-	1	0	1	result after overflow is negative
-	1	1	0	result after overflow is positive
0	-	-	-	no carry from bit position 0
1	-	-	-	carry from bit position 0

[†] A hyphen (-) indicates that the condition code bit is not affected by the condition given under the "significance" heading.

[††] CC1 remains unchanged for the instructions LCW, LAW, LCD, and LAD.

If the instruction causing the trap was DW or DH, the stored condition code is interpreted as follows:

1	2	3	4	Significance
-	1	-	-	overflow

The stored instruction address is the address of the instruction that caused fixed-point overflow.

2. Load the new PSD. The condition code and instruction address portions of the PSD remain at the value loaded from memory.

FLOATING-POINT ARITHMETIC FAULT CONDITION

Floating-point fault detection is performed after the operation called for by the instruction code is performed, but before any results are actually loaded into the general registers; thus, the floating-point operation that causes an arithmetic fault is not carried to completion (in the sense that the original contents of the general registers remain unchanged). Instead, the computer traps to location X'44' with the current condition code indicating the reason for the trap. A characteristic overflow or an attempt to divide by zero always results in a trap condition; a significance check or a characteristic underflow result in a trap condition only if the floating-point mode controls (FS, FZ, and FN) in the program status doubleword are set to the appropriate state.

If a floating-point instruction causes a trap, the execution of XPSD in trap location X'44' is as follows:

1. Store the current PSD. If division is attempted with a zero divisor or if characteristic overflow occurs, the stored condition code is interpreted as follows:

1	2	3	4	Significance
0	1	0	0	divide by zero
0	1	0	1	characteristic overflow, negative result
0	1	1	0	characteristic overflow, positive result

If none of the above conditions occurs, but characteristic underflow occurs with the floating zero (FZ) mode bit set to 1, the stored condition code is interpreted as follows:

1	2	3	4	Significance
1	1	0	1	characteristic underflow, negative result
1	1	1	0	characteristic underflow, positive result

If none of the above conditions occurs, but an addition or subtraction results in either a zero result (with FS = 1 and FN = 0), or a postnormalization shift of more than two hexadecimal places (with FS = 1 and FN = 0), the stored condition code is interpreted as follows:

1	2	3	4	Significance
1	0	0	0	zero result of addition or subtraction
1	0	0	1	more than 2 postnormalizing shifts, negative result
1	0	1	0	more than 2 postnormalizing shifts, positive result

The stored instruction address is the address of the instruction that caused the floating-point fault.

2. Load the new PSD. The condition code and instruction address portions of the PSD remain at the values loaded from memory.

WATCHDOG TIMER RUNOUT

The instruction watchdog timer insures that the CPU must periodically reach interruptible points of operation in the execution of instructions. An interruptible point is a time during the execution of a program when an interrupt request (if present) would be acknowledged. Interruptible points occur at the end of every instruction and during the execution of some instructions. The watchdog timer measures elapsed time from the last interruptible point. If the maximum allowable time has been reached before the next time that an interrupt could be recognized, the current instruction is aborted and the watchdog timer runout trap is activated. Except for a nonexistent address used with READ DIRECT (RD) or WRITE DIRECT (WD), programs trapped by the watchdog timer cannot (in general) be continued. Execution of XPSD in trap location X'46' is as follows:

1. Store the current PSD. The stored condition code is, in general, meaningless. The instruction address stored is the address of the aborted instruction.
2. Load the new PSD. The instruction address portion of the PSD remains at the value loaded from memory; however, the resulting condition code value is generally, meaningless. If the watchdog timer runout trap was activated while an operation was being performed by the integral IOP, the condition code is set to all 1's. In this case the integral IOP is inhibited from further operation until the inhibit is reset by a specific configuration of the WD instruction or by pressing either the CPU RESET/CLEAR switch or the SYSTEM RESET/CLEAR switch on the processor control panel.

CALL INSTRUCTIONS

The four CALL instructions (CAL1, CAL2, CAL3, and CAL4) cause the computer to trap to location X'48' (for CAL1) X'49' (for CAL2), X'4A' (for CAL3), or X'4B' (for CAL4). Execution of XPSD in the trap location is as follows:

1. Store the current PSD. The stored condition code is that which existed immediately prior to the CALL instruction. The stored instruction address is the address of the CALL instruction.
2. Load the new PSD.

3. Modify the new PSD.

   a. The R field of the CALL instruction is logically ORed with the condition code value loaded from memory, and the result is loaded into the condition code.

   b. If bit 9 of XPSD contains a 1, the R field of the CALL instruction is added to the instruction address loaded from memory.

      If bit 9 of XPSD contains a 0, the instruction address remains at the value loaded from memory.

3. INSTRUCTION REPERTOIRE

This section describes all SIGMA 5 instructions, grouped into the following functional classes:

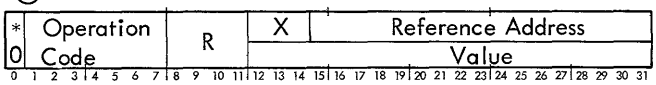
SIGMA 5 instructions are described in the following format:

MNEMONIC ① INSTRUCTION NAME ②

(Addressing type ③, Optional ④,

Privileged ⑤, Interrupt Action ⑥)

⑦



Description ⑧

Affected ⑨ Trap ⑩

Symbolic notation ⑪

Condition Code Settings ⑫

Trap Action ⑬

Example ⑭

1. MNEMONIC is the code used by the SIGMA 5 assemblers to produce the instruction's basic operation code.

2. INSTRUCTION NAME is the instruction's descriptive title.

3. The instruction's addressing type is one of the following:

   a. Byte addressing: the reference address field of the instruction can be used to address a byte in core memory or in the current block of general registers.

   b. Halfword addressing: the reference address field of the instruction can be used to address a halfword in core memory or in the current block of general registers.

   c. Word addressing: the reference address field of the instruction can be used to address any word in core memory or in the current block of general registers.

   d. Doubleword addressing: the reference address field of the instruction can be used to address any doubleword in core memory or in the current block of general registers. The addressed doubleword is automatically located within doubleword storage boundaries.

   e. Immediate addressing: the instruction word contains an operand value used as part of the instruction execution. If indirect addressing is attempted with this type of instruction (i.e., bit 0 of the instruction word is a 1), the instruction is treated as a nonexistent instruction, in which case the computer unconditionally aborts execution of the instruction (at the time of operation code decoding) and traps to location X'40', the "nonallowed operation" trap. Indexing does not apply to this type of instruction.

4. If the instruction is not in the standard SIGMA 5 instruction set, it is labeled "optional". If execution of an optional instruction is attempted on a computer in which the instruction is not implemented, the computer unconditionally aborts execution of the instruction (at the time of operation code decoding) and traps to location X'41', which is the "unimplemented instruction trap".

5. If the instruction is not executable while the computer is in the slave mode, it is labeled "privileged". If execution of a privileged instruction is attempted while the computer is in the slave mode, the computer unconditionally aborts execution of the instruction (at the time of operation code decoding) and traps to location X'40'.

6. If the instruction can be successfully resumed after its execution sequence has been interrupted by an interrupt acknowledgement, the instruction is labeled "continue after interrupt". Otherwise, the instruction is either completed or the instruction is aborted and then restarted after the interrupt is cleared. In the case of the "continue after interrupt" instruction, certain general registers contain intermediate results or control information that allows the instruction to continue properly.

7. Instruction format:

   a. Indirect addressing — If bit position 0 of the instruction format contains an asterisk (*), the instruction can utilize indirect addressing; however, if bit position 0 of the instruction format contains a 0, the instruction is of the immediate addressing type, which is treated as a nonexistent instruction if indirect addressing is attempted (resulting in a trap to location X'40').

   b. Operation code — The operation code field (bit positions 1-7) of the instruction is shown in hexadecimal notation.

   c. R field — If the register address field (bit positions 8-11) of the instruction format contains the letter

"R", the instruction can specify any register in the current block of general registers as an operand source, result destination, or both; otherwise, the function of this field is determined by the instruction.

d. X field – If the index register address field (bit positions 12-14) of the instruction format contains the character "X", the instruction can specify indexing with any one of registers 1 through 7 in the current block of general registers; otherwise, the function of this field is determined by the instruction.

e. Reference address field – Normally, the reference address field (bit positions 15-31) of the instruction format is used as the initial address value for an instruction operand. For some instructions the effective address of the instruction is not used to access an operand; instead, the effective address itself is used as an operand. In these cases, the function of the effective address is represented in the lower half of the reference address field in the instruction format diagram.

f. Value field – In immediate addressing instructions, bit positions 12-31 of the instruction format contain the word "value". This field is treated as a 20-bit integer, with negative integers represented in two's complement form.

g. Ignored fields – In the instruction format diagrams, any area that is shaded represents a field or bit position that is ignored by the computer (i.e., the content of the shaded field or bit has no effect on instruction execution) but should be coded with 0's so as to preclude conflict with possible modifications.

8. The description of the instruction defines the operations performed by the computer in response to the instruction configuration depicted by the instruction format diagram. Any instruction configuration that causes an unpredictable result is so specified in the description.

9. All programmable registers and storage areas that can be affected by the instruction are listed (symbolically) after the word "Affected". The instruction address portion of the program status doubleword is considered to be affected only if a branch condition can occur as a result of the instruction execution, since the instruction address is updated (incremented by 1) as part of every instruction execution.

10. All trap conditions that may be invoked by the execution of the instruction are listed after the word "Trap". SIGMA 5 trap locations are summarized in the section "Trap System".

11. The symbolic notation presents the instruction operation as a series of generalized symbolic statements. The symbolic terms used in the notation are defined in Table 4.

12. Condition code settings are given for each instruction that affects the condition code. A 0 or a 1 under any of columns 1, 2, 3, or 4 indicates that the instruction causes a 0 or 1 to be placed in CC1, CC2, CC3, or CC4, respectively, for the reasons given. If a hyphen (-) appears in column 1, 2, 3, or 4, that portion of the condition code is not affected by the reason given for the condition code bit(s) containing a 0 or 1. For example, the following condition code settings are given for a comparison instruction:

1	2	3	4	Result of comparison
-	-	0	0	equal
-	-	0	1	register operand is arithmetically less than effective operand
-	-	1	0	register operand is arithmetically greater than effective operand
-	0	-	-	logical product (AND) of the two operands is zero
-	1	-	-	logical product of the two operands is nonzero

CC1 is unchanged by the instruction. CC2 indicates whether or not the two operands have 1's in corresponding bit positions, regardless of their arithmetic relationship. CC3 and CC4 are set according to the arithmetic relationship of the two operands, regardless of whether or not the two operands have 1's in corresponding bit positions. For example, if the register operand is arithmetically less than the effective operand and the two operands both have 1's in at least one corresponding bit position, the condition code setting for the comparison instruction is:

1	2	3	4
-	1	0	1

The above statements about the condition code are valid only if no trap occurs before the successful completion of the instruction execution cycle. If a trap does occur during the instruction execution, the condition code is normally reset to the value it contained before the instruction was started, and then the appropriate trap location is activated.

13. Actions taken by the computer for those trap conditions that may be invoked by the execution of the instruction are described. The description includes the criteria for the trap condition, any controlling trap mask or inhibit bits, and the action taken by the computer. In order to avoid unnecessary repetition, the two trap conditions that apply to all instructions (i.e., nonallowed operations and watchdog timer runout) are not described for each instruction.

14. Some instruction descriptions provide examples to illustrate the results of the instruction. These examples are intended only to show how the instructions operate, and not to demonstrate their full capability. Within the examples, hexadecimal notation is used to represent the contents of general registers and storage locations (condition code settings are shown in binary notation). The character "x" is used to indicate irrelevant or ignored information.

Table 4. Glossary of Symbolic Terms

Term	Meaning
( )	Contents of
AM	Fixed-point arithmetic trap mask – bit 11 of the program status doubleword. If this bit is a 1, the computer traps to location X'43' after executing an instruction that causes fixed-point arithmetic overflow; if this bit is a 0, the computer does not trap to location X'43'.
I	Instruction register – the internal CPU register used to hold instructions obtained from memory while they are being decoded.
R	General register address value – the 4-bit contents of bit positions 8-11 (the R field) of an instruction word, also expressed symbolically as $(I)_{8-11}$.
Ru1	Odd register address value – register Ru1 is the general register pointed to by the value obtained by logically ORing 0001 into the address value for register R. Thus, if the R field of an instruction contains an even value, Ru1 = R + 1 and if the R field contains an odd value, Ru1 = R.
X	Index register address value – the 3-bit contents of bit positions 12-14 (the X field) of an instruction word. If X = 0 for an instruction, no indexing is performed. If X ≠ 0 for an instruction, indexing is performed (after indirect addressing, if indirect addressing is called for) with general register X in the current register block.
EA	Effective address – the final address value obtained as a result of indirect addressing and/or indexing.
EBL	Effective byte location – the byte location pointed to by the effective address of a byte-addressing instruction.
EB	Effective byte – the 8-bit contents of the effective byte location, or (EBL).
EHL	Effective halfword location – the halfword location pointed to by the effective address of the halfword addressing instruction.
EH	Effective halfword – the 16-bit contents of the effective halfword location, or (EHL).
EWL	Effective word location – the word location pointed to by the effective address of a word-addressing instruction.
EW	Effective word – the 32-bit contents of the effective word location, or (EWL).
EDL	Effective doubleword location – the doubleword location pointed to by the effective address of a doubleword-addressing instruction.
ED	Effective doubleword – the 64-bit contents of the effective doubleword location, or (EDL).
CC	Condition code – a 4-bit value (whose bit positions are labeled CC1, CC2, CC3, and CC4) that is established as part of the execution of most SIGMA 5 instructions.
FN	Floating normalize mode control – bit 7 of the program status doubleword. If this bit is a 0, the results of floating-point additions and subtractions are to be normalized; if this bit is a 1, the results are not normalized.
FS	Floating significance mode control – bit 5 of the program status doubleword. If this bit is a 1, the computer traps to location X'44' when more than two hexadecimal places of postnormalization shifting are required for a floating-point addition or subtraction; if this bit is a 0, no significance checking is performed.
FZ	Floating zero mode control – bit 6 of the program status doubleword. If this bit is a 1, the computer traps to location X'44' when either characteristic underflow or a zero result occurs for a floating-point multiplication or division; if this bit is a 0, characteristics underflow and zero results are treated as normal conditions.
IA	Instruction address – the 17 bit value that defines the address of an instruction immediately before the instruction is executed.
X'n'	Hexadecimal qualifier – a hexadecimal value (n) is a string of hexadecimal digits enclosed by quote marks and preceded by the qualifier "X".
∩	AND (logical product, where 0 ∩ 0 = 0, 0 ∩ 1 = 0, 1 ∩ 0 = 0, and 1 ∩ 1 = 1.
∪	OR (logical inclusive OR, where 0 ∪ 0 = 0, 0 ∪ 1 = 1, 1 ∪ 0 = 1, and 1 ∪ 1 = 1).
⊕	EOR (logical exclusive OR, where 0 ⊕ 0 = 0, 0 ⊕ 1 = 1, 1 ⊕ 0 = 1, and 1 ⊕ 1 = 0).
SE	Sign extension – some SIGMA 5 instructions operate on two operands of different lengths; the two operands are made equal in length by extending the sign of the shorter operand by the required number of bit positions. For positive operands, the result of sign extension is high-order 0's prefixed to the operand; for negative operands, high-order 1's are prefixed to the operand. This sign extension process is performed after the operand is accessed from memory and before the operation called for by the instruction code is performed.

LOAD/STORE INSTRUCTIONS

The following load/store instructions are implemented in SIGMA 5 computers:

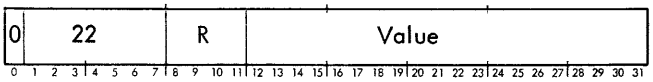
SIGMA 5 load and store instructions operate with information fields of byte, halfword, word, and doubleword lengths. Load instructions load the information indicated into one of the general registers in the current register block. Load instructions do not affect core memory storage; however, nearly all load instructions provide a condition code setting that indicates the following information about the contents of the affected general register(s) after the instruction is successfully completed.

Condition code settings:

1	2	3	4	Result
-	-	0	0	zero—the result in the affected register(s) is all 0's.
-	-	0	1	negative—register R contains a 1 in bit position 0.
-	-	1	0	positive—register R contains a 0 in bit position 0, and at least one 1 appears in the remainder of the affected register(s) (or appeared during execution of the current instruction.)
-	0	-	-	no fixed-point overflow—the result in the affected register(s) is arithmetically correct.
-	1	-	-	fixed-point overflow—the result in the affected register(s) is arithmetically incorrect.

Store instructions affect only that portion of memory storage that corresponds to the length of the information field specified by the operation code of the instruction; thus, register bytes are stored in memory byte locations, register halfwords in memory halfword locations, register words in memory word locations, and register doublewords in memory doubleword locations. Store instructions do not affect the contents of the general register specified by the R field of the instruction, unless the same register is also specified by the effective address of the instruction.

LI LOAD IMMEDIATE
(Immediate addressing)



LOAD IMMEDIATE extends the sign of the value field (bit position 12) of the instruction word 12 bit positions to the left and then loads the 32-bit result into register R.

Affected: (R), CC3, CC4

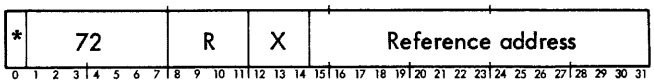
$(I)_{12\text{-}31SE} \longrightarrow R$

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive

If LI is indirectly addressed, it is treated as a nonexistent instruction, in which case the computer unconditionally aborts execution of the instruction (at the time of operation code decoding) and traps to location X'40' with the contents of register R and the condition code unchanged.

LB LOAD BYTE
(Byte addressing)



LOAD BYTE loads the effective byte into positions 24-31 of register R and clears bit positions 0-23 of the register to all 0's.

Affected: (R), CC3, CC4

$EB \longrightarrow R_{24\text{-}31}$; $0 \longrightarrow R_{0\text{-}23}$

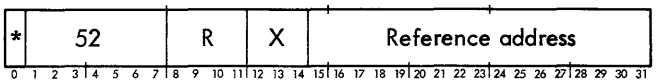
Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	1	0	nonzero

Example:

		Before execution	After execution
EB	=	X'B4'	X'B4'
(R)	=	xxxxxxxx	X'000000B4'
CC	=	xxxx	xx10

LH LOAD HALFWORD
(Halfword addressing)



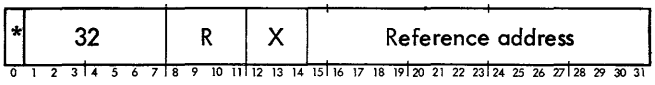
LOAD HALFWORD extends the sign of the effective halfword 16 bit positions to the left and then loads the 32-bit result into register R.

Affected: (R), CC3, CC4
$EH_{SE} \longrightarrow R$

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive

LW LOAD WORD
(Word addressing)



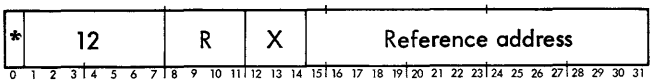
LOAD WORD loads the effective word into register R.

Affected: (R), CC3, CC4
$EW \longrightarrow R$

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive

LD LOAD DOUBLEWORD
(Doubleword addressing)



LOAD DOUBLEWORD loads the 32 low-order bits of the effective doubleword into register Rul and then loads the 32 high-order bits of the effective doubleword into register R.

If R is an odd value, the result in register R is the 32 high-order bits of the effective doubleword. The condition code settings are based on the effective doubleword, rather than the final result in register R (see example 3, below).

Affected: (R), (Rul), CC3, CC4
$ED_{32-63} \longrightarrow Rul$; $ED_{0-31} \longrightarrow R$

Condition code settings:

1	2	3	4	Effective doubleword
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive

Example 1, even R field value:

		Before execution	After execution
ED	=	X'0123456789ABCDEF'	X'0123456789ABCDEF'
(R)	=	xxxxxxxx	X'01234567'
(Rul)	=	xxxxxxxx	X'89ABCDEF'
CC	=	xxxx	xx10

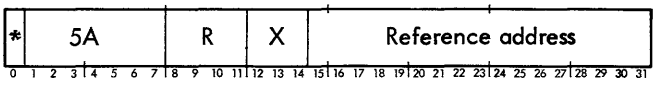
Example 2, odd R field value:

ED	=	X'0123456789ABCDEF'	X'0123456789ABCDEF'
(R)	=	xxxxxxxx	X'01234567'
CC	=	xxxx	xx10

Example 3, odd R field value:

ED	=	X'0000000012345678'	X'0000000012345678'
(R)	=	xxxxxxxx	X'00000000'
CC	=	xxxx	xx10

LCH LOAD COMPLEMENT HALFWORD
(Halfword addressing)



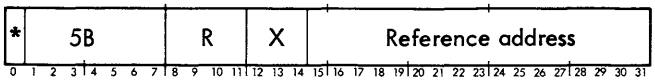
LOAD COMPLEMENT HALFWORD extends the sign of the effective halfword 16 bit positions to the left and then loads the 32-bit two's complement of the result into register R. (Overflow cannot occur.)

Affected: (R), CC3, CC4
$-[EH_{SE}] \longrightarrow R$

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive

LAH LOAD ABSOLUTE HALFWORD
(Halfword addressing)



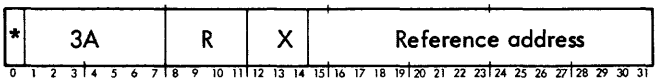
If the effective halfword is positive, LOAD ABSOLUTE HALFWORD extends the sign of the effective halfword 16 bit positions to the left and then loads the 32-bit result in register R. If the effective halfword is negative, LAH extends the sign of the effective halfword 16 bit positions to the left and then loads the 32-bit two's complement of the result into register R. (Overflow cannot occur.)

Affected: (R), CC3, CC4
$|EH_{SE}| \longrightarrow R$

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	1	0	nonzero

LCW LOAD COMPLEMENT WORD
(Word addressing)



LOAD COMPLEMENT WORD loads the 32-bit two's complement of the effective word into register R. Fixed-point overflow occurs if the effective word is -2^{31} (X'80000000'), in which case the result in register R is -2^{31} and CC2 is set to 1; otherwise, CC2 is reset to 0.

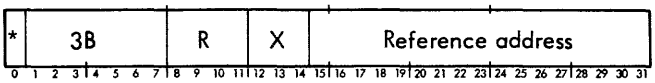
Affected: (R), CC2, CC3, CC4 Trap: Fixed-point overflow
-EW ⟶ R

Condition code settings:

1	2	3	4	Result in R
-	0	0	0	zero
-	-	0	1	negative
-	0	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	0	1	fixed-point overflow

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after execution of LOAD COMPLEMENT WORD; otherwise, the computer executes the next instruction in sequence.

LAW LOAD ABSOLUTE WORD
(Word addressing)



If the effective word is positive, LOAD ABSOLUTE WORD loads the effective word into register R. If the effective word is negative, LAW loads the 32-bit two's complement of the effective word into register R. Fixed-point overflow occurs if the effective word is -2^{31}(X'80000000'), in which case the result in register R is -2^{31} and CC2 is set to 1; otherwise, CC2 is reset to 0.

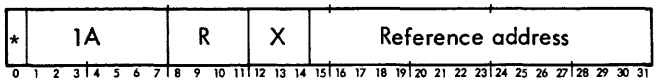
Affected: (R), CC2, CC3, CC4 Trap: Fixed-point overflow
|EW| ⟶ R

Condition code settings:

1	2	3	4	Result in R
-	0	0	0	zero
-	-	1	0	nonzero
-	0	-	-	no fixed-point overflow
-	1	1	0	fixed-point overflow

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after execution of LOAD ABSOLUTE WORD; otherwise, the computer executes the next instruction in sequence.

LCD LOAD COMPLEMENT DOUBLEWORD
(Doubleword addressing)



LOAD COMPLEMENT DOUBLEWORD forms the 64-bit two's complement of the effective doubleword, loads the 32 low-order bits of the result into register Ru1, and then loads the 32 high-order bits of the result into register R.

If R is an odd value, the result in register R is the 32 high-order bits of the two's complemented doubleword. The condition code settings are based on the two's complement of the effective doubleword, rather than the final result in register R.

Fixed-point overflow occurs if the effective doubleword is -2^{63}(X'8000000000000000'), in which case the result in registers R and Ru1 is -2^{63} and CC2 is set to 1; otherwise, CC2 is reset to 0.

Affected: (R), (Ru1), CC2, CC3, CC4 Trap: Fixed-point overflow

$[-ED]_{32-63} \longrightarrow$ Ru1; $[-ED]_{0-31} \longrightarrow$ R

Condition code settings:

1	2	3	4	Two's complement of effective doubleword
-	0	0	0	zero
-	-	0	1	negative
-	0	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	0	1	fixed-point overflow

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after execution of LOAD COMPLEMENT DOUBLEWORD; otherwise the computer executes the next instruction in sequence.

Example 1, even R field value:

		Before execution	After execution
ED	=	X'0123456789ABCDEF'	X'0123456789ABCDEF'
(R)	=	xxxxxxxx	X'FEDCBA98'
(Ru1)	=	xxxxxxxx	X'76543211'
CC	=	xxxx	x001

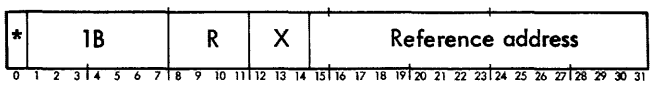
Example 2, even R field value:

ED	=	X'FEDCBA9876543210'	X'FEDCBA9876543210'
(R)	=	xxxxxxxx	X'01234567'
(Ru1)	=	xxxxxxxx	X'89ABCDF0'
CC	=	xxxx	x010

Example 3, odd R field value:

ED	=	X'0123456789ABCDEF'	X'0123456789ABCDEF'
(R)	=	xxxxxxxx	X'FEDCBA98'
CC	=	xxxx	x001

LAD LOAD ABSOLUTE DOUBLEWORD
(Doubleword addressing)



If the effective doubleword is positive, LOAD ABSOLUTE DOUBLEWORD loads the 32 low-order bits of the effective

doubleword into register Ru1, and then loads the 32 high-order bits of the effective doubleword into register R. If R is an odd value, the result in register R is the 32 high-order bits of the effective doubleword. The condition code settings are based on the effective doubleword, rather than the final result in register R.

If the effective doubleword is negative, LAD forms the 64-bit two's complement of the effective doubleword, loads the 32 low-order bits of the two's complemented doubleword into register Ru1, and then loads the 32 high-order bits of the two's complemented doubleword into register R. If R is an odd value, the result in register R is the 32 high-order bits of the two's complemented doubleword. The condition code settings are based on the two's complement of the effective doubleword, rather than the final result in register R.

Fixed-point overflow occurs if the effective doubleword is -2^{63} (X'8000000000000000'), in which case the result in registers R and Ru1 is -2^{63} and CC2 is set to 1; otherwise, CC2 is reset to 0.

Affected: (R), (Ru1), CC2 ⟶ Trap: Fixed-point overflow
CC3, CC4
$|ED|_{32-63}$ ⟶ Ru1; $|ED|_{0-31}$ ⟶ R

Condition code settings:

1	2	3	4	Absolute value of effective doubleword
-	0	0	0	zero
-	-	1	0	nonzero
-	0	-	-	no fixed-point overflow
-	1	1	0	fixed-point overflow

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after execution of LOAD ABSOLUTE DOUBLEWORD; otherwise, the computer executes the next instruction in sequence.

Example 1, even R field value:

		Before execution	After execution
ED	=	X'0123456789ABCDEF'	X'0123456789ABCDEF'
(R)	=	xxxxxxxx	X'01234567'
(Ru1)	=	xxxxxxxx	X'89ABCDEF'
CC	=	xxxx	x010

Example 2, even R field value:

ED	=	X'FEDCBA9876543210'	X'FEDCBA9876543210'
(R)	=	xxxxxxxx	X'01234567'
(Ru1)	=	xxxxxxxx	X'89ABCDF0'
CC	=	xxxx	x010

Example 3, odd R field value:

ED	=	X'0123456789ABCDEF'	X'0123456789ABCDEF'
(R)	=	xxxxxxxx	X'01234567'
CC	=	xxxx	x010

LS LOAD SELECTIVE
(Word addressing)

Register Ru1 contains a 32-bit mask. If R is an even value, LOAD SELECTIVE loads the effective word into register R in those bit positions selected by a 1 in corresponding bit positions of register Ru1. The contents of register R are not affected in those bit positions selected by a 0 in corresponding bit positions of register Ru1.

If R is an odd value, LS logically ANDs the contents of register R with the effective word and loads the result into register R. If corresponding bit positions of register R and the effective word both contain 1's, a 1 remains in register R in the corresponding bit position of register R.

Affected: (R), CC3, CC4

If R is even, $[EWn(Ru1)] \cup [(R) \cap \overline{(Ru1)}]$ ⟶ R
If R is odd, EWn(R) ⟶ R

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	bit 0 of register R is a 1
-	-	1	0	bit 0 of register R is a 0 and bit positions 1-31 of register R contain at least one 1

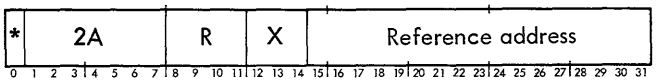
Example 1, even R field value:

		Before Execution	After execution
EW	=	X'01234567'	X'01234567'
(Ru1)	=	X'FF00FF00'	X'FF00FF00'
(R)	=	xxxxxxxx	X'01xx45xx'
CC	=	xxxx	xx10

Example 2, odd R field value:

EW	=	X'89ABCDEF'	X'89ABCDEF'
(R)	=	X'F0F0F9F0'	X'80A0C0E0'
CC	=	xxxx	xx01

LM LOAD MULTIPLE
(Word addressing)



LOAD MULTIPLE loads a sequential set of words into a sequential set of registers. The set of words to be loaded begins with the word pointed to by the effective address of LM, and the set of registers begin with register R. The set of registers is treated modulo 16 (i.e., the next register loaded after register 15 is register 0 in the current register block).

The number of words to be loaded into the general registers is determined by the value of the condition code immediately before the execution of LM. (The desired value of the condition code can be set with LCF or LCFI.) An initial value of 0000 for the condition code causes 16 consecutive words to be loaded into the register block.

Affected: (R) to (R+CC-1)
(EWL) ⟶ R;...(EWL+CC-1) ⟶ R+CC-1

If the instruction starts loading words from an existent region of memory and then crosses into a nonexistent memory region, the nonexistent memory address trap occurs. In this case, the trap is activated with

the condition code unchanged from the value it contained before the execution of LM. The effective address of the instruction permits the trap routine to compute how many registers have been loaded. Since it is permissible to use indirect addressing or indexing through a general register or even to execute an instruction located in a general register, a trapped LM instruction may have already overwritten the index, direct address, or the LM instruction itself, thus destroying any possibility of continuing the program successfully. If such programming must be done, it is advisable that the register containing the direct address, index displacement, or instruction be the last register loaded by the LM instruction.

LCFI LOAD CONDITIONS AND FLOATING CONTROL IMMEDIATE
(Immediate addressing)

If bit position 10 of the instruction word contains a 1, LOAD CONDITIONS AND FLOATING CONTROL IMMEDIATE loads the contents of bit position 24 through 27 of the instruction word into the condition code; however, if bit 10 is 0, the condition code is not affected.

If bit position 11 of the instruction word contains a 1, LCFI loads the contents of bit positions 29 through 31 of the instruction word into the floating significance (FS), floating zero (FZ), and floating normalize (FN) mode control bits, respectively (in the program status doubleword); however, if bit 11 is 0, the FS, FZ and FN control bits are not affected. The functions of the floating-point control bits are described in the section "Floating-Point Instructions".

Affected: CC, FS, FZ, FN
If $(I)_{10} = 1$, $(I)_{24-27} \longrightarrow$ CC
If $(I)_{10} = 0$, CC not affected
If $(I)_{11} = 1$, $(I)_{29-31} \longrightarrow$ FS, FZ, FN
If $(I)_{11} = 0$, FS, FZ, and FN are not affected

Condition code settings, if $(I)_{10} = 1$:

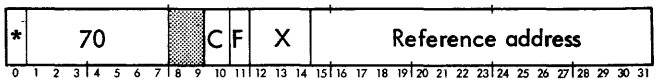
1	2	3	4
$(I)_{24}$	$(I)_{25}$	$(I)_{26}$	$(I)_{27}$

If LCFI is indirectly addressed, it is treated as a nonexistent instruction, in which case the computer unconditionally aborts execution of instruction (at the time of operation code decoding) and traps to location X'40' with the condition code unchanged.

Example:

		Before execution	After execution
(I)	=	X'023000A1'	xxxxxxxx
CC	=	xxxx	1010
FS	=	x	0
FZ	=	x	0
FN	=	x	1

LCF LOAD CONDITIONS AND FLOATING CONTROL
(Byte addressing)



If bit position 10 of the instruction word contains a 1, LOAD CONDITIONS AND FLOATING CONTROL loads bits 0 through 3 of the effective byte into the condition code; however, if bit 10 is 0, the condition code is not affected.

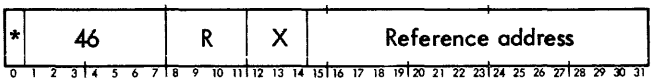
If bit position 11 of the instruction word contains a 1, LCF loads bits 5 through 7 of the effective byte into the floating significance (FS), floating zero (FZ), and floating normalize (FN) mode control bits, respectively; however, if bit 11 is 0, the FS, FZ, and FN control bits are not affected. The functions of the floating-point mode control bits are described in the section "Floating-Point Instructions".

Affected: CC, FS, FZ, FN
If $(I)_{10} = 1$, $EB_{0-3} \longrightarrow$ CC
If $(I)_{10} = 0$, CC not affected
If $(I)_{11} = 1$, $EB_{5-7} \longrightarrow$ FS, FZ, FN
If $(I)_{11} = 0$, FS, FZ, FN not affected

Condition code settings, if $(I)_{10} = 1$:

1	2	3	4
$(EB)_0$	$(EB)_1$	$(EB)_2$	$(EB)_3$

XW EXCHANGE WORD
(Word addressing)



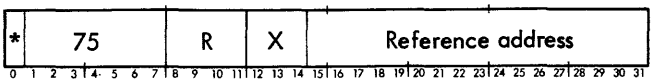
EXCHANGE WORD exchanges the contents of register R with the contents of the effective word location.

Affected: (R), (EWL), CC3, CC4
(R) $\longleftrightarrow$ (EWL)

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive

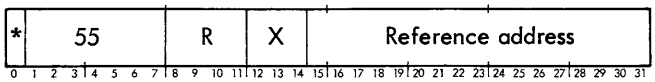
STB STORE BYTE
(Byte addressing)



STORE BYTE stores the contents of bit positions 24-31 of register R into the effective byte location.

Affected: (EBL)
$(R)_{24-31} \longrightarrow$ EBL

STH STORE HALFWORD
(Halfword addressing)



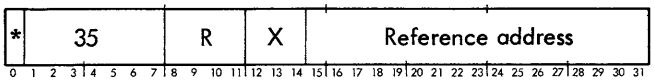
STORE HALFWORD stores the contents of bit positions 16-31 of register R into the effective halfword location. If the information in register R exceeds halfword data limits, CC2 is set to 1; otherwise, CC2 is reset to 0.

Affected: (EHL), CC2
$(R)_{16-31} \longrightarrow$ EHL

Condition code settings:

1	2	3	4	Information in R
-	0	-	-	$(R)_{0-16}$ = all 0's or all 1's
-	1	-	-	$(R)_{0-16} \neq$ all 0's or all 1's

STW STORE WORD
(Word addressing)



STORE WORD stores the contents of register R into the effective word location.

Affected: (EWL)
(R) $\longrightarrow$ EWL

STD STORE DOUBLEWORD
(Doubleword addressing)

STORE DOUBLEWORD stores the contents of register R into the 32 high-order bit positions of the effective doubleword location and then stores the contents of register Ru1 into the 32 low-order bit positions of the effective doubleword location.

Affected: (EDL)
(R) $\longrightarrow EDL_{0-31}$; (Ru1) $\longrightarrow EDL_{32-63}$

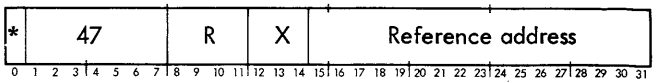
Example 1, even R field value:

	Before execution	After execution
(R) =	X'01234567'	X'01234567'
(Ru1) =	X'89ABCDEF'	X'89ABCDEF'
(EDL) =	xxxxxxxxxxxxxxxx	X'0123456789ABCDEF'

Example 2, odd R field value:

(R) =	X'89ABCDEF'	X'89ABCDEF'
(EDL) =	xxxxxxxxxxxxxxxx	X'89ABCDEF89ABCDEF'

STS STORE SELECTIVE
(Word addressing)



Register Ru1 contains a 32-bit mask. If R is an even value, STORE SELECTIVE stores the contents of register R into the effective word location in those bit positions selected by a 1 in corresponding bit positions of register Ru1; the effective word remains unchanged in those bit positions selected by a 0 in corresponding bit positions of register Ru1.

If R is an odd value, STS logically inclusive ORs the contents of register R with the effective word and stores the result into the effective word location. The contents of register R are not affected.

Affected: (EWL)
If R is even, $[(R) \cap (Ru1)] \cup [EW \cap (\overline{Ru1})] \longrightarrow$ EWL
If R is odd, $(R) \cup EW \longrightarrow$ EWL

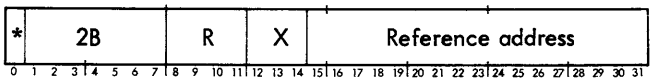
Example 1, even R field value:

	Before execution	After execution
(R) =	X'12345678'	X'12345678'
(Ru1) =	X'F0F0F0F0'	X'F0F0F0F0'
EW =	xxxxxxxx	X'1x3x5x7x'

Example 2, odd R field value:

(R) =	X'00FF00FF'	X'00FF00FF'
EW =	X'12345678'	X'12FF56FF'

STM STORE MULTIPLE
(Word addressing)



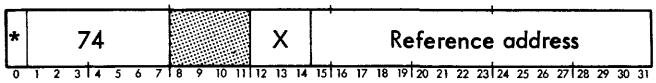
STORE MULTIPLE stores the contents of a sequential set of registers into a sequential set of word locations. The set of locations begins with the location pointed to by the effective word address of STM, and the set of registers begins with register R. The set of registers is treated modulo 16 (i.e., the next sequential register after register 15 is register 0). The number of registers to be stored is determined by the value of the condition code immediately before execution of STM. (The condition code can be set to the desired value before execution of STM with LCF or LCFI.) An initial value of 0000 for the condition code causes 16 general registers to be stored.

Affected: (EWL) to (EWL + CC-1)
(R) $\longrightarrow$ EWL, . . . , (R + CC-1) $\longrightarrow$ EWL + CC-1

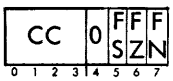
If the instruction starts storing words into an accessible region of memory and then crosses into an inaccessible memory region, either the memory protection trap or the nonexistent memory address trap can occur. In either case, the trap is activated with the condition code unchanged from the value it contained before the execution of STM. The effective address of the instruction permits the trap routine to compute how many words of

memory have been changed. Since it is permissible to use indirect addressing through one of the affected locations, or even to execute an instruction located in one of the affected locations, a trapped STM instruction may have already overwritten the direct address, or the STM instruction itself, thus destroying any possibility of continuing the program successfully. If such programming must be done, it is advisable that the direct address, or the STM instruction, occupy the last location in which the contents of a register are to be stored by the STM instruction.

STCF STORE CONDITIONS AND FLOATING CONTROL
(Byte Addressing)



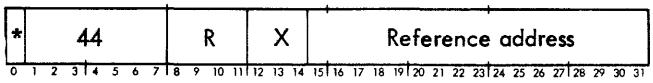
STORE CONDITIONS AND FLOATING CONTROL stores the current condition code and the current values of the floating significance (FS), floating zero (FZ), and floating normalize (FN) mode control bits of the program status doubleword into the effective byte location as follows:



Affected: (EBL)
$(PSD)_{0-7} \longrightarrow EBL$

ANALYZE/INTERPRET INSTRUCTIONS

ANLZ ANALYZE
(Word addressing)



The ANALYZE instruction treats the effective word as a SIGMA 5 instruction and calculates the effective address that would be generated by the instruction if the instruction were to be executed. ANALYZE produces an answer to the question, "What effective address would be used by the instruction located at N if it were executed now?" The ANALYZE instruction determines the addressing type of the "analyzed" instruction, calculates its effective address (if the instruction is not an immediate-addressing instruction), and loads the effective address into register R as a displacement value (the condition code settings for the ANALYZE instruction indicate the addressing type of the analyzed instruction)

The nonexistent instruction, the privileged instruction violation, and the unimplemented instruction trap conditions can never occur during execution of the ANLZ instruction. However, the nonexistent memory address trap condition can occur as a result of any memory access initiated by the ANLZ instruction. If this trap condition occurs, the instruction address stored by an XPSD in trap location X'40' is the address of the ANLZ instruction.

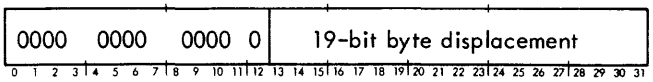
The detailed operation of ANALYZE is as follows:

1. The contents of the location pointed to by the effective address of the ANLZ instruction are obtained. This effective word is the instruction to be analyzed. The nonallowed operation trap (nonexistent memory address) can occur as a result of this memory access.

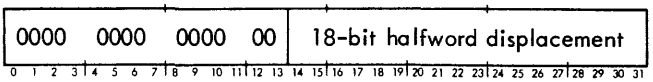
2a. If the operation code portion of the effective word specifies an immediate-addressing instruction type, the condition code is set to indicate the addressing type, and instruction execution proceeds to the next instruction in sequence after ANLZ. The original contents of register R are not changed when the analyzed instruction is of the immediate addressing type.

2b. If the operation code portion of the effective word specifies a nonimmediate addressing type, the condition code is set to indicate the addressing type of the analyzed instruction and the effective address of the analyzed instruction is computed (using all of the normal address computation rules). If bit 0 of the effective word is a 1, the contents of the memory location specified by bits 15-31 of the effective word are obtained and then used as a direct address. The nonallowed operation trap (nonexistent memory address) can occur as a result of this memory access. Indexing is always performed (with an index register in the current register block) if bits 12-14 of the analyzed instruction are nonzero. The effective address of the analyzed instruction is aligned as an integer displacement value and loaded into register R, according to the instruction addressing type, as follows:

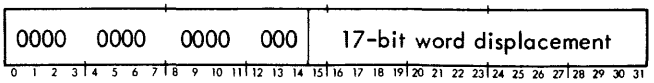
Byte Addressing:



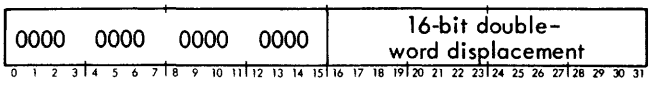
Halfword Addressing:



Word Addressing:



Doubleword Addressing:



Operation codes and mnemonics for the SIGMA 5 instruction set are shown in Table 5. Circled numbers in the table indicate the condition code value (decimal) available to the next instruction after ANALYZE when a direct-addressing operation code in the corresponding addressing type is analyzed. The R field of the instruction in the effective word location is ignored.

Affected: (R), CC

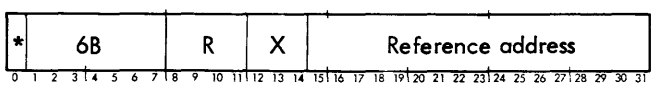
Condition code Settings:

1	2	3	4	Instruction addressing type
0	0	-	0	byte
0	0	-	1	immediate, byte
0	1	-	0	halfword
1	0	-	0	word
1	0	-	1	immediate, word
1	1	-	0	doubleword
-	-	0	-	direct addressing ($EW_0 = 0$)
-	-	1	-	indirect addressing ($EW_0 = 1$)

Table 5. ANALYZE Table for SIGMA 5 Operation Codes

X'n'	X'00' + n	X'20' + n	X'40' + n	X'60' + n
00	—	AI	—	—
01	—	CI	—	— (1)
02	LCFI (9)	LI	—	—
03	—	MI	—	—
04	CAL1	SF	ANLZ	BDR
05	CAL2	S	CS	BIR
06	CAL3	—	XW	AWM
07	CAL4	—	STS	EXU
08	PLW	—	EOR	BCR
09	PSW	— (8)	OR	BCS
0A	PLM	LM	LS	BAL
0B	PSM	STM	AND	INT
0C	—	—	SIO	RD
0D	— (12)	—	TIO	WD
0E	LPSD	WAIT	TDV	AIO
0F	XPSD	LRP	HIO	MMC
10	AD	AW	AH	LCF
11	CD	CW	CH	CB
12	LD	LW	LH	LB
13	MSP	MTW	MTH	MTB
14	—	—	—	STCF
15	STD	STW	STH	STB (0)
16	—	DW	DH (4)	—
17	—	MW	MH	—
18	SD	SW	SH	—
19	CLM	CLR	—	—
1A	LCD	LCW	LCH	—
1B	LAD	LAW	LAH	—
1C	FSL	FSS	—	—
1D	FAL	FAS	—	—
1E	FDL	FDS	—	—
1F	FML	FMS	—	—

INT INTERPRET
(Word addressing)



INTERPRET loads bits 0-3 of the effective word into the condition code, loads bits 4-15 of the effective word into bit positions 20-31 of register R (and loads 0's into the remainder of register R), and then loads bits 16-31 of the effective word into bit positions 16-31 of register Rul (and loads 0's into bit positions 0-15 of register Rul). If R is an odd value, INT loads bits 0-3 of the effective word into the condition code, loads bits 16-31 of the effective word into bit positions 16-31 of register R, and loads 0's into bit positions 0-15 of register R (bits 4-15 of the effective word are ignored in this case).

Affected: (R), (Rul), CC

$EW_{0-3} \longrightarrow CC$

$EW_{4-15} \longrightarrow R_{20-31}$; $0 \longrightarrow R_{0-19}$

$EW_{16-31} \longrightarrow Rul_{16-31}$; $0 \longrightarrow Rul_{0-15}$

Condition code settings:

1	2	3	4
EW_0	EW_1	EW_2	EW_3

Example, even R field value:

	Before execution	After execution
EW =	X'12345678'	X'12345678'
(R) =	xxxxxxxx	X'00000234'
(Rul) =	xxxxxxxx	X'00005678'
CC =	xxxx	0001

FIXED-POINT ARITHMETIC INSTRUCTIONS

The following fixed-point arithmetic instructions are included as a standard feature of the SIGMA 5 computer:

Instruction Name	Mnemonic	Page
Add Immediate	AI	34
Add Halfword	AH	34
Add Word	AW	34
Add Doubleword	AD	35
Subtract Halfword	SH	35
Subtract Word	SW	35
Subtract Doubleword	SD	35
Multiply Immediate	MI	36
Multiply Halfword	MH	36
Multiply Word	MW	37
Divide Halfword	DH	37
Divide Word	DW	37
Add Word to Memory	AWM	37
Modify and Test Byte	MTB	38
Modify and Test Halfword	MTH	38
Modify and Test Word	MTW	38

The fixed-point arithmetic instruction set performs binary addition, subtraction, multiplication, and division with integer operands that may be data, addresses, index values, or counts. One operand may be either in the instruction word itself or may be in one or two of the current general registers; the second operand may be either in core memory or in one or two of the current general registers. For most of these instructions, both operands may be in the same general register, thus permitting the doubling, squaring, or

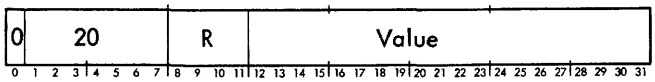
clearing the contents of a register by using a reference address value equal to the R field value.

All fixed-point arithmetic instructions provide a condition code setting that indicates the following information about the result of the operation called for by the instruction:

Condition code settings:

1	2	3	4	Result
-	-	0	0	zero – The result in the specified general register(s) is all zeros.
-	-	0	1	negative – The instruction has produced a fixed-point negative result.
-	-	1	0	positive – The instruction has produced a fixed-point positive result.
-	0	-	-	fixed-point overflow has not occurred during execution of an add, subtract, or divide instruction, and the result is correct.
-	1	-	-	fixed-point overflow has occurred during execution of an add, subtract, or divide instruction. For addition and subtraction, the incorrect result is loaded into the designated register(s). For a divide instruction, the designated register(s), and CC1, CC3, and CC4 are not affected.
0	-	-	-	no carry – For an add or subtract instruction, there was no carry of a 1-bit out of the high-order (sign) bit position of the result.
1	-	-	-	carry – For an add or subtract instruction, there was a 1-bit carry out of the sign bit position of the result.

AI ADD IMMEDIATE
(Immediate addressing)



The value field (bit positions 12-31) of the instruction word is treated as a 20-bit, two's complement integer. ADD IMMEDIATE extends the sign of the value field (bit position 12 of the instruction word) 12 bit positions to the left, adds the resulting 32-bit value to the contents of register R, and loads the sum into register R.

Affected: (R), CC
$(R) + (I)_{12\text{-}31SE} \longrightarrow R$

Trap: Fixed-point overflow

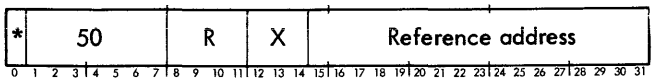
Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	-	-	fixed-point overflow
0	-	-	-	no carry from bit position 0
1	-	-	-	carry from bit position 0

If AI is indirectly addressed, it is treated as a nonexistent instruction, in which case the computer unconditionally aborts execution of the instruction (at the time of operation code decoding) and traps to location X'40' with the contents of register R and the condition code unchanged.

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after loading the sum into register R; otherwise, the computer executes the next instruction in sequence.

AH ADD HALFWORD
(Halfword addressing)



ADD HALFWORD extends the sign of the effective halfword 16 bit positions to the left (to form a 32-bit word in which bit positions 0-15 contain the sign of the effective halfword), adds the 32-bit result to the contents of register R, and loads the sum into register R.

Affected: (R), CC
$(R) + EH_{SE} \longrightarrow R$

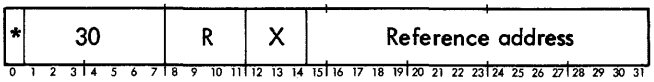
Trap: Fixed-point overflow

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	-	-	fixed-point overflow
0	-	-	-	no carry from bit position 0
1	-	-	-	carry from bit position 0

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after loading the sum into register R; otherwise, the computer executes the next instruction in sequence.

AW ADD WORD
(Word addressing)



ADD WORD adds the effective word to the contents of register R and loads the sum into register R.

Affected: (R), CC
$(R) + EW \longrightarrow R$

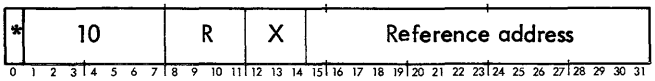
Trap: Fixed-point overflow

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	-	-	fixed-point overflow
0	-	-	-	no carry from bit position 0
1	-	-	-	carry from bit position 0

If CC2 is set to 1 and the fixed-point arithmetic trap mask (PSD_{11}) is 1, the computer traps to location X'43' after loading the sum into register R; otherwise, the computer executes the next instruction in sequence.

AD ADD DOUBLEWORD
(Doubleword addressing)



R must be an even value. ADD DOUBLEWORD adds the effective doubleword to the contents of registers R and Rul (treated as a single, 64-bit register), and then loads the 64-bit sum into registers R and Rul. If R is an odd value, the result in register R is unpredictable.

Affected: (R), (Rul), CC
(R, Rul) + ED ⟶ R, Rul

Trap: Fixed-point overflow

Condition code settings:

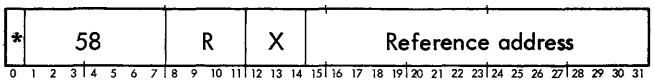
1	2	3	4	Result in R, Rul
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	-	-	fixed-point overflow
0	-	-	-	no carry from bit position 0
1	-	-	-	carry from bit position 0

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after loading the sum into registers R and Rul; otherwise, the computer executes the next instruction in sequence.

Example, even R field:

		Before execution	After execution
ED	=	X'33333333EEEEEEEE'	X'33333333EEEEEEEE'
(R)	=	X'11111111'	X'44444445'
(R+1)	=	X'33333333'	X'22222221'
CC	=	xxxx	0010

SH SUBTRACT HALFWORD
(Halfword addressing)



SUBTRACT HALFWORD extends the sign of the effective halfword 16 bit positions to the left (to form a 32-bit word in which bit positions 0-15 contain the sign of the effective halfword), forms the two's complement of the resulting word, adds the complemented word to the contents of register R, and loads the sum into register R.

Affected: (R), CC
$-EH_{SE}$ + (R) ⟶ R

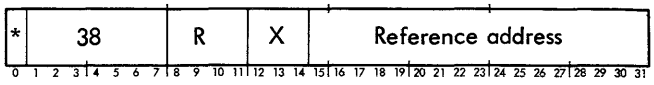
Trap: Fixed-point overflow

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	-	-	fixed-point overflow
0	-	-	-	no carry from bit position 0
1	-	-	-	carry from bit position 0

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after loading the sum into register R; otherwise, the computer executes the next instruction in sequence.

SW SUBTRACT WORD
(Word addressing)



SUBTRACT WORD forms the two's complement of the effective word, adds the complemented word to the contents of register R, and loads the sum into register R.

Affected: (R), CC
-EW + (R) ⟶ R

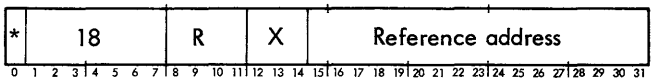
Trap: Fixed-point overflow

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	-	-	fixed-point overflow
0	-	-	-	no carry from bit position 0
1	-	-	-	carry from bit position 0

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after loading the sum into register R; otherwise, the computer executes the next instruction in sequence.

SD SUBTRACT DOUBLEWORD
(Doubleword addressing)



R must be an even value. SUBTRACT DOUBLEWORD forms the 64-bit two's complement of the effective doubleword, adds the complemented doubleword to the contents of registers R and Rul (treated as a single, 64-bit register), and then loads the 64-bit sum into registers R and Rul. If R is an odd value, the result in register R is unpredictable.

Affected: (R), (R+1), CC
-ED + (R, Rul) ⟶ R, Rul

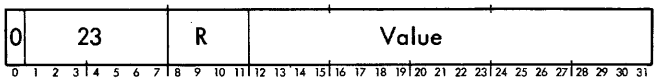
Trap: Fixed-point overflow

Condition code settings:

1	2	3	4	Result in R, Ru1
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	-	-	fixed-point overflow
0	-	-	-	no carry from bit position 0
1	-	-	-	carry from bit position 0

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after the result is loaded into registers R and Ru1; otherwise, the computer executes the next instruction in sequence.

MI MULTIPLY IMMEDIATE
(Immediate addressing)



The value field (bit positions 12-31) of the instruction word is treated as a 20-bit, two's complement integer. MULTIPLY IMMEDIATE extends the sign of the value field (bit position 12) of the instruction word 12 bit positions to the left and multiplies the resulting 32-bit value by the contents of register Ru1, loads the 32 high-order bits of the product into register R, and then loads the 32 low-order bits of the product into register Ru1.

If R is an odd value, the result in register R is the 32 low-order bits of the product. Thus, in order to generate a 64-bit product, the R field of the instruction must be even and the multiplicand must be in register R+1. The condition code settings are based on the 64-bit product formed during instruction execution, rather than on the final contents of register R. Overflow cannot occur.

Affected: (R), (Ru1), CC2, CC3, CC4
$(Ru1) \times (I)_{12-31\,SE} \longrightarrow R, Ru1$

Condition code settings:

1	2	3	4	64-bit product
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	result is correct, as represented in register Ru1
-	1	-	-	result is not correctly representable in register Ru1 alone.

If MI is indirectly addressed, it is treated as a nonexistent instruction, in which case the computer unconditionally aborts execution of the instruction (at the time of operation code decoding) and traps to location X'40' with the contents of register R, register Ru1, and the condition code unchanged.

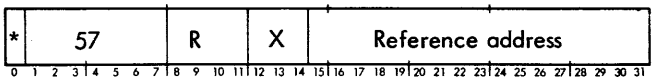
Example 1, even R field value:

		Before execution	After execution
$(I)_{12-31}$	=	X'70000'	X'70000'
(R)	=	xxxxxxxx	X'00007000'
(Ru1)	=	X'10001000'	X'70000000'
CC	=	xxxx	x110

Example 2, odd R field value:

$(I)_{12-31}$	=	X'01234'	X'01234'
(R)	=	X'00030002'	X'369C2468'
CC	=	xxxx	x010

MH MULTIPLY HALFWORD
(Halfword addressing)



MULTIPLY HALFWORD multiplies the contents of bit positions 16-31 of register R by the effective halfword, and stores the product in register Ru1, with both halfwords treated as signed, two's complement integers (overflow cannot occur). If R is an even value, the original multiplier in register R is preserved, allowing repetitive halfword multiplication with a constant multiplier; however, if R is an odd value, the product is loaded into the same register. Overflow cannot occur.

Affected: (Ru1), CC3, CC4
$(R)_{16-31} \times EH \longrightarrow Ru1$

Condition code settings:

1	2	3	4	Result in Ru1
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive

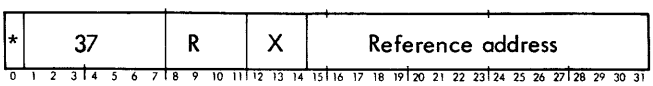
Example 1, even R field:

		Before execution	After execution
EH	=	X'FFFF'	X'FFFF'
(R)	=	X'xxxx000A'	X'xxxx000A'
(Ru1)	=	xxxxxxxx	X'FFFFFFF6'
CC	=	xxxx	xx01

Example 2, odd R field:

EH	=	X'FFFF'	X'FFFF'
(R)	=	X'xxxx000A'	X'FFFFFFF6'
CC	=	xxxx	xx01

MW MULTIPLY WORD
(Word addressing)



MULTIPLY WORD multiplies the contents of register Ru1 by the effective word, loads the 32 high-order bits of the

product into register R and then loads the 32 low-order bits of the product into register Rul (overflow cannot occur).

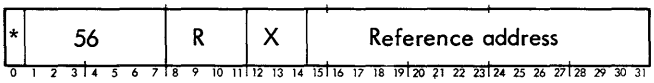
If R is an odd value, the result in register R is the 32 low-order bits of the product. Thus, in order to generate a 64-bit product, the R field of the instruction must be even and the multiplicand must be in register R+1. The condition code settings are based on the 64-bit product formed during instruction execution, rather than on the final contents of register R.

Affected: (R), (Rul), CC
(Rul) x EW ⟶ R, Rul

Condition code settings:

1	2	3	4	64-bit product
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	result is correct, as represented in register Rul
-	1	-	-	result is not correctly representable in register Rul alone

DH DIVIDE HALFWORD
(Halfword addressing)



DIVIDE HALFWORD divides the contents of register R (treated as a 32-bit fixed-point integer) by the effective halfword and loads the quotient into register R. If the absolute value of the quotient cannot be correctly represented in 32 bits, fixed point overflow occurs; in which case, CC2 is set to 1 and the contents of register R, CC1, CC3 and CC4 are unchanged.

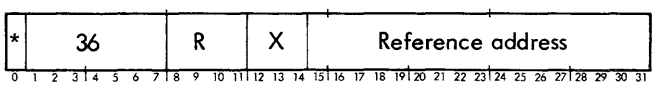
Affected: (R), CC2, CC3 CC4 Trap: Fixed-point overflow
(R) ÷ EH ⟶ R

Condition code settings:

1	2	3	4	Result in R
-	0	0	0	zero quotient, no overflow
-	0	0	1	negative quotient, no overflow
-	0	1	0	positive quotient, no overflow
-	1	-	-	fixed-point overflow

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' with the contents of register R, CC1, CC3, and CC4 unchanged; otherwise, the computer executes the next instruction in sequence.

DW DIVIDE WORD
(Word addressing)



DIVIDE WORD divides the contents of registers R and Rul (treated as a 64-bit fixed-point integer) by the effective word, loads the integer remainder into register R and then loads the integer quotient into register Rul. If a nonzero remainder occurs, the remainder has the same sign as the dividend (original contents of register R). Fixed-point overflow occurs if the absolute value of the quotient cannot be correctly represented in 32 bits, in which case, CC2 is set to 1 and the contents of register R, register Rul, CC1, CC3, and CC4 remain unchanged; otherwise, CC2 is reset to 0, CC3 and CC4 reflect the quotient in register Rul, and CC1 is unchanged.

If R is an odd value, DW divides the contents of register R by the effective word, and loads the quotient into register R (in this case, the remainder is lost).

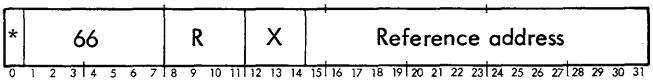
Affected: (R), (Rul), CC2, CC3, CC4 Trap: Fixed-point overflow
(R, Rul) ÷ EW ⟶ R (remainder), Rul (quotient)

Condition code settings:

1	2	3	4	Result in Rul
-	0	0	0	zero quotient, no overflow
-	0	0	1	negative quotient, no overflow
-	0	1	0	positive quotient, no overflow
-	1	-	-	fixed-point overflow

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' with the original contents of register R, register Rul, CC1, CC3, and CC4 unchanged; otherwise, the computer executes the next instruction in sequence.

AWM ADD WORD TO MEMORY
(Word addressing)



ADD WORD TO MEMORY adds the contents of register R to the effective word and stores the sum in the effective word location. The sum is stored regardless of whether or not overflow occurs.

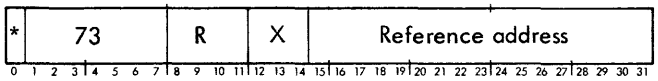
Affected: (EWL), CC Trap: Fixed-point overflow
EW + (R) ⟶ EWL

Condition code settings:

1	2	3	4	Result in EWL
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	-	-	fixed-point overflow
0	-	-	-	no carry from bit position 0
1	-	-	-	carry from bit position 0

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after the result is stored in the effective word location; otherwise, the computer executes the next instruction in sequence.

MTB MODIFY AND TEST BYTE
(Byte addressing)



If the value of the R field (bit positions 8-11) of the instruction word is zero, the effective byte is tested for being a zero, or nonzero value. The condition code is set according to the result of the test, but the effective byte is not affected, and no memory write-protection violation can occur.

If the value of the R field is nonzero, the high-order bit of the R field (bit position 8 of the instruction word) is extended 4 bit positions to the left, to form a byte with bit positions 0-4 of that byte equal to the high-order bit of the R field. This byte is then added to the effective byte, the sum replaces the previous contents of the effective byte location, and the condition code is set according to the value of the resultant byte. This process allows modification of a byte by any number in the range -8 through +7, followed by a test. (A memory write-protection violation can occur in this case.)

Affected: CC if $(I)_{8-11} = 0$;
(EBL) and CC if $(I)_{8-11} \neq 0$

If $(I)_{8-11} = 0$, test byte and set CC

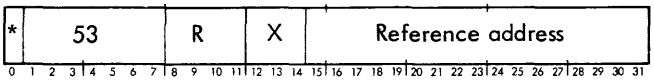
If $(I)_{8-11} \neq 0$, EB + $(I)_{8-11SE} \longrightarrow$ EBL and set CC

Condition code settings:

1	2	3	4	Result in EBL
-	0	0	0	zero
-	0	1	0	nonzero
0	-	-	-	no carry from byte
1	-	-	-	carry from byte

If MTB is executed in an interrupt location, the condition code is not affected (see "Interrupt System" in Chapter 2).

MTH MODIFY AND TEST HALFWORD
(Halfword addressing)



If the value of the R field (bit positions 8-11) of the instruction is zero, the effective halfword is tested for being a zero, negative, or positive value. The condition code is set, according to the result of the test, but the effective halfword is not affected, and no memory write-protection violation can occur.

If the value of the R field is nonzero, the high-order bit of the R field (bit position 8 of the instruction word) is extended 12 bit positions to the left, to form a halfword with bit positions 0-11 of that halfword equal to the high-order bit of the R field. This halfword is then added to the effective halfword, the sum replaces the previous contents of the effective halfword location, and the condition code is set according to the value of the resultant halfword. This process allows modification of a halfword by any number in the range -8 through +7, followed by a test. If no memory write-protection violation is detected, the sum is stored regardless of whether or not overflow occurs.

Affected: CC if $(I)_{8-11} = 0$; Trap: Fixed-point overflow (EHL) and CC if $(I)_{8-11} \neq 0$

If $(I)_{8-11} = 0$, test halfword and set CC

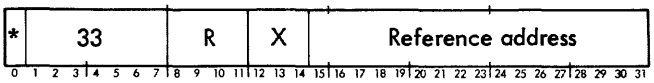
If $(I)_{8-11} \neq 0$, EH + $(I)_{8-11SE} \longrightarrow$ EHL and set CC

Condition code settings:

1	2	3	4	Result in EHL
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	-	-	fixed-point overflow
0	-	-	-	no carry from halfword
1	-	-	-	carry from halfword

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after the result is stored in the effective halfword location; otherwise, the computer executes the next instruction in sequence, However, if MTH is executed in an interrupt location, the condition code is not affected and no fixed-point overflow trap can occur (see "Interrupt System" in Chapter 2).

MTW MODIFY AND TEST WORD
(Word addressing)



If the value of the R field (bit positions 8-11) of the instruction word is zero, the effective word is tested for being a zero, negative, or positive value. The condition code is set according to the result of the test, but the effective word is not affected, and no memory write-protection violation can occur.

If the value of the R field is nonzero, the high-order bit of the R field (bit position 8 of the instruction word) is extended 28 bit positions to the left, to form a word with bit positions 0-27 of that word equal to the high-order bit of the R field. This word is then added to the effective word, the sum replaces the previous contents of the effective word location, and the condition code is set according to the value of the resultant word. This process allows modification of a word by any number in the range -8 through +7, followed by a test. If no memory write-protection violation is detected, the sum is stored regardless of whether or not overflow occurs.

Affected: CC if $(I)_{8-11} = 0$; Trap: Fixed-point overflow (EWL) and CC if $(I)_{8-11} \neq 0$

If $(I)_{8-11} = 0$, test word and set CC

If $(I)_{8-11} \neq 0$, EW+$I_{8-11SE} \longrightarrow$ EWL and set CC

Condition code settings:

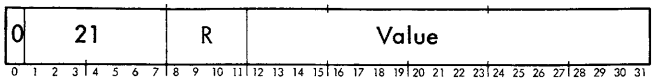
1	2	3	4	Result in EWL
-	-	0	0	zero
-	-	0	1	negative
-	-	1	0	positive
-	0	-	-	no fixed-point overflow
-	1	-	-	fixed-point overflow
0	-	-	-	no carry from word
1	-	-	-	carry from word

If CC2 is set to 1 and the fixed-point arithmetic trap mask (AM) is 1, the computer traps to location X'43' after the result is stored in the effective word location; otherwise, the computer executes the next instruction in sequence. However, if MTW is executed in an interrupt location, the condition code is not affected and no fixed-point overflow trap can occur (see "Interrupt System" in Chapter 2).

COMPARISON INSTRUCTIONS

All SIGMA 5 comparison instructions produce a condition code setting, which is indicative of the results of the comparison, without affecting the effective operand in memory and without affecting the contents of the designated register.

CI COMPARE IMMEDIATE
(Immediate addressing)



COMPARE IMMEDIATE extends the sign of the value field (bit position 12) of the instruction word 12 bit positions to the left, compares the 32-bit result with the contents of register R (with both operands treated as signed fixed-point quantities), and then sets the condition code according to the results of the comparison.

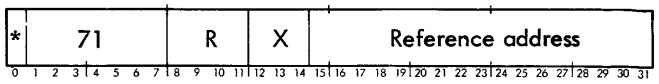
Affected: CC2, CC3, CC4
(R) : $(I)_{12-31SE}$

Condition code settings:

1	2	3	4	Result of Comparison
-	-	0	0	operands are equal
-	-	0	1	register value is arithmetically less than immediate value
-	-	1	0	register value is arithmetically greater than immediate value
-	0	-	-	logical product (AND) of the two operands is zero
-	1	-	-	logical product of the two operands is nonzero

If CI is indirectly addressed, it is treated as a nonexistent instruction, in which case the computer unconditionally aborts execution of the instruction (at the time of operation code decoding) and then traps to location X'40' with the condition code unchanged.

CB COMPARE BYTE
(Byte addressing)



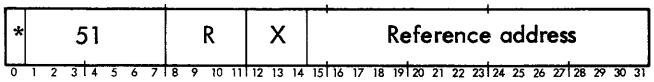
COMPARE BYTE compares the contents of bit positions 24-31 of register R with the effective byte, with both bytes treated as positive integer magnitudes, and sets the condition code according to the results of the comparison

Affected: CC2, CC3, CC4
$(R)_{24-31}$: EB

Condition code settings:

1	2	3	4	Result of Comparison
-	-	0	0	operands are equal
-	-	0	1	register byte is less in magnitude than effective byte
-	-	1	0	register byte is greater in magnitude than effective byte
-	0	-	-	logical product (AND) of the two operands is zero
-	1	-	-	logical product of the two operands is nonzero

CH COMPARE HALFWORD
(Halfword addressing)



COMPARE HALFWORD extends the sign of the effective halfword 16 bit positions to the left and then compares the resultant 32-bit word with the contents of register R, with both words treated as signed fixed-point quantities, and sets the condition code according to the results of the comparison.

Affected: CC2, CC3, CC4
(R) : EH_{SE}

Condition code settings:

1	2	3	4	Result of Comparison
-	-	0	0	operands are equal
-	-	0	1	register word is arithmetically less than effective halfword with sign extended
-	-	1	0	register word is arithmetically greater then effective halfword with sign extended
-	0	-	-	logical product (AND) of the two operands is zero
-	1	-	-	logical product of the two operands is nonzero

CW COMPARE WORD
(Word addressing)

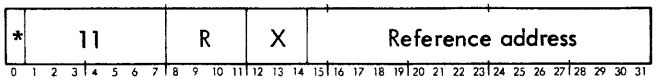
COMPARE WORD compares the contents of register R with the effective word, with both words treated as signed fixed-point quantities, and sets the condition code according to the results of the comparison.

Affected: CC2, CC3, CC4
(R) : EW

Condition code settings:

1	2	3	4	Result of Comparison
-	-	0	0	operands are equal
-	-	0	1	register word is arithmetically less than effective word
-	-	1	0	register word is arithmetically greater than effective word
-	0	-	-	logical product (AND) of the two operands is zero
-	1	-	-	logical product of the two operands is nonzero

CD COMPARE DOUBLEWORD
(Doubleword addressing)



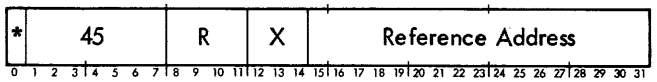
COMPARE DOUBLEWORD compares the effective doubleword with the contents of registers R and Ru1, with both doublewords treated as signed fixed-point quantities, and sets the condition code according to the results of the comparison. If the R field of CD is an odd value, CD forms a 64-bit register operand (by duplicating the contents of register R for both the 32 high-order bits and the 32 low-order bits) and compares the effective doubleword with the 64-bit register operand. The condition code settings are based on the 64-bit comparison.

Affected: CC3, CC4
(R, Ru1) : ED

Condition code settings:

1	2	3	4	Result of Comparison
-	-	0	0	operands are equal
-	-	0	1	register doubleword is arithmetically less than effective doubleword
-	-	1	0	register doubleword is arithmetically greater than effective doubleword

CS COMPARE SELECTIVE
(Word addressing)



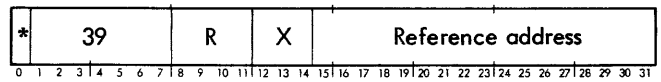
COMPARE SELECTIVE compares the contents of register R with the effective word in only those bit positions selected by a 1 in corresponding bit positions of register Ru1 (mask). The contents of register R and the effective word are ignored in those bit positions designated by a 0 in corresponding bit positions of register Ru1. The selected contents of register R and the effective word are treated as positive integer magnitudes, and the condition code is set according to the result of the comparison. If the R field of CS is an odd value, CS compares the contents of register R with the logical product (AND) of the effective word and the contents of register R.

Affected: CC3, CC4
If R is even: (R) n (Ru1) : EWn(Ru1)
If R is odd: (R) : EWn(R)

Condition code settings:

1	2	3	4	Results of Comparison under Mask in Ru1
-	-	0	0	operands are equal
-	-	0	1	register word is less in magnitude than effective word
-	-	1	0	register word is greater in magnitude than effective word

CLR COMPARE WITH LIMITS IN REGISTER
(Word addressing)



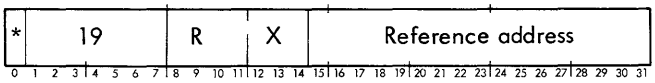
COMPARE WITH LIMITS IN REGISTER simultaneously compares the effective word with the contents of register R and with the contents of register Ru1, with all three words treated as signed fixed-point quantities, and sets the condition code according to the results of the comparisons. Note that if the R field of CLR is an odd value, the settings for CC1 and CC2 are identical (respectively) to the settings for CC3 and CC4.

Affected: CC
(R) : EW, (Ru1) : EW

Condition code settings:

1	2	3	4	Result of Comparison
-	-	0	0	contents of R equal to effective word
-	-	0	1	contents of R less than effective word
-	-	1	0	contents of R greater than effective word
0	0	-	-	contents of Ru1 equal to effective word
0	1	-	-	contents of Ru1 less than effective word
1	0	-	-	contents of Ru1 greater than effective word

CLM COMPARE WITH LIMITS IN MEMORY
(Doubleword addressing)



COMPARE WITH LIMITS IN MEMORY simultaneously compares the contents of register R with the 32 high-order bits of the effective doubleword and with the 32 low-order bits of the effective doubleword, with all three words treated as 32-bit signed quantities, and sets the condition code according to the results of the comparisons.

Affected: CC
(R) : ED_{0-31}; (R) : ED_{32-63}

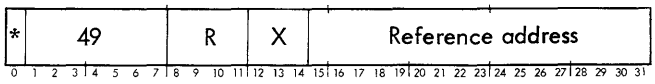
Condition code settings:

1	2	3	4	Result of Comparison
-	-	0	0	contents of R equal to most significant word, (R) = ED_{0-31}
-	-	0	1	contents of R less than most significant word, (R) < ED_{0-31}
-	-	1	0	contents of R greater than most significant word, (R) > ED_{0-31}
0	0	-	-	contents of R equal to least significant word, (R) = ED_{32-63}
0	1	-	-	contents of R less than least significant word, (R) < ED_{32-63}
1	0	-	-	contents of R greater than least significant word, (R) > ED_{32-63}

LOGICAL INSTRUCTIONS

All logical operations are performed bit by corresponding bit between two operands; one operand is in register R and the other operand is the effective word. The result of the logical operation is loaded into register R.

OR OR WORD
(Word addressing)



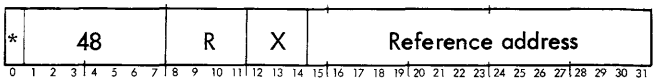
OR WORD logically ORs the effective word into register R. If the corresponding bits of register R and the effective word are both 0, a 0 remains in R; otherwise, a 1 is placed in the corresponding bit position of R. The effective word is not affected.

Affected: (R), CC3, CC4
(R) $\cup$ EW $\rightarrow$ R, where $0 \cup 0 = 0$, $0 \cup 1 = 1$, $1 \cup 0 = 1$, $1 \cup 1 = 1$

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	bit 0 of register R is a 1
-	-	1	0	bit 0 of register R is a 0 and bit positions 1-31 of register R contain at least one 1

EOR EXCLUSIVE OR WORD
(Word addressing)



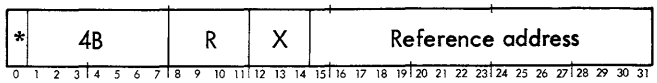
EXCLUSIVE OR WORD logically exclusive ORs the effective word into register R. If the corresponding bits of register R and the effective word are different, a 1 is placed in the corresponding bit position of R; if the contents of the corresponding bit positions are alike, a 0 is placed in the corresponding bit position of R. The effective word is not affected.

Affected: (R), CC3, CC4
(R) $\textcircled{\cup}$ EW $\rightarrow$ R, where $0 \textcircled{\cup} 0 = 0$, $0 \textcircled{\cup} 1 = 1$,
$1 \textcircled{\cup} 0 = 1$, $1 \textcircled{\cup} 1 = 0$

Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	bit 0 of register R is a 1
-	-	1	0	bit 0 of register R is a 0 and bit positions 1-31 of register R contain at least one 1

AND AND WORD
(Word addressing)



AND WORD logically ANDs the effective word into register R. If the corresponding bits of register R and the effective word are both 1, a 1 remains in R; otherwise, a 0 is placed in the corresponding bit position of R. The effective word is not affected.

Affected: (R), CC3, CC4
(R) $\cap$ EW $\rightarrow$ R, where $0 \cap 0 = 0$, $0 \cap 1 = 0$,
$1 \cap 0 = 0$, $1 \cap 1 = 1$

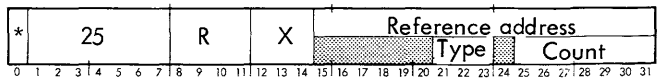
Condition code settings:

1	2	3	4	Result in R
-	-	0	0	zero
-	-	0	1	bit 0 of register R is a 1
-	-	1	0	bit 0 of register R is a 0 and bit positions 1-31 of register R contain at least one 1

SHIFT INSTRUCTIONS

The instruction format for logical, circular, and arithmetic shift operations is

S SHIFT
(Word addressing)



If neither indirect addressing nor indexing is called for in the instruction SHIFT, bit positions 21-31 of the reference address field determine the type, direction, and amount of

the shift. If only indirect addressing is called for in the instruction, bits 15-31 of the instruction are used to access the indirect word and then bits 21-31 of the indirect word determine the type, direction, and amount of the shift. If only indexing is called for in the instruction, bits 21-31 of the instruction word determine the type of shift; the direction and amount of shift are determined by the 7 low-order bits of the sum of bits 25-31 of the instruction and bits 25-31 of the specified index register. If both indirect adressing and indexing are called for in the instruction, bits 15-31 of the instruction are used to access the indirect word and then bits 21-23 of the indirect word determine the type of shift; the direction and amount of the shift are determined by the 7 low-order bits of the sum of bits 25-31 of the indirect word and bits 25-31 of the specified index register.

Bit positions 15-20 and 24 of the effective address are ignored. Bit positions 21, 22 and 23 of the effective address determine the type of shift, as follows:

Bit Positions 21	22	23	Shift Type
0	0	0	Logical, single register
0	0	1	Logical, double register
0	1	0	Circular, single register
0	1	1	Circular, double register
1	0	0	Arithmetic, single register
1	0	1	Arithmetic, double register
1	1	0	Undefined
1	1	1	Undefined

Bit positions 25 through 31 of the effective address are a shift count that determines the direction and amount of the shift. The shift count (C) is treated as a 7-bit signed binary integer, with the high-order bit (bit position 25) as the sign (negative integers are represented in two's complement form). A positive shift count causes a left shift of C bit positions. A negative shift count causes a right shift of |C| bit positions. The value of C is within the range: $-64 \leq C \leq +63$.

All double-register shift operations require an even value for the R field of the instruction, and treat registers R and Rul as a 64-bit register with the high-order bit (bit position 0 of register R) as the sign for the entire register. If the R field of SHIFT is an odd value and a double-register shift operation is specified, a register doubleword is formed by duplicating the contents of register R for both the 32 high-order bits and the 32 low-order bits of the doubleword. The shift operation is then performed and the 32 high-order bits of the result are loaded into register R.

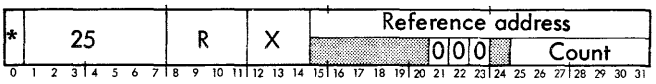
Overflow occurs (on left shifts only) whenever the value of the sign bit (bit position 0 of register R) changes. At the completion of logical left, circular left, and arithmetic left shifts, the condition code is set as follows:

1	2	3	4	Result of Shift
0	-	-	-	even number of 1's shifted off left end of register R
1	-	-	-	odd number of 1's shifted off left end of register R.
-	0	-	-	no overflow on left shift
-	1	-	-	overflow on left shift

At the completion of logical right, circular right, and arithmetic right shifts, the condition code is set as follows:

1	2	3	4
0	0	-	-

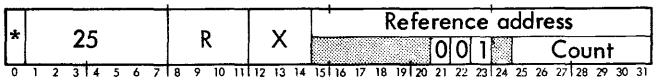
Logical Shift, Single Register



If the shift count, C, is positive, the contents of register R are shifted left C places, with 0's copies into vacated bit positions on the right. (Bits shifted past R_0 are lost.) If C is negative, the contents of register R are shifted right |C| places, with 0's copied into vacated bit positions on the left. (Bits shifted past R_{31} are lost.)

Affected: (R), CC1, CC2

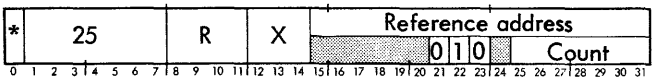
Logical Shift, Double Register



If the shift count, C, is positive, the contents of registers R and Rul are shifted left C places, with 0's copied into vacated bit positions on the right. Bits shifted past bit position 0 of register Rul are copied into bit position 31 of register R. (Bits shifted past R_0 are lost.) If C is negative, the contents of registers R and Rul are shifted right |C| places, with 0's copied into vacated bit positions on the left. Bits shifted past bit position 31 of register R are copied into bit position 0 of register Rul. (Bits shifted past Rul_{31} are lost.)

Affected: (R), (Rul), CC1, CC2

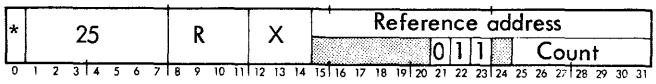
Circular Shift, Single Register



If the shift count, C, is positive, the contents of register R are shifted left C places. Bits shifted past bit position 0 are copied into bit position 31. (No bits are lost.) If C is negative, the contents of register R are shifted right |C| places. Bits shifted past bit position 31 are copied into bit position 0. (No bits are lost.)

Affected: (R), CC1, CC2

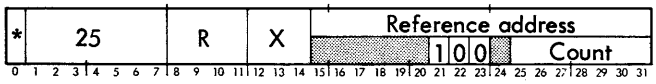
Circular Shift, Double Register



If the shift count, C, is positive, the contents of registers R and Rul are shifted left C places. Bits shifted past bit position 0 of register R are copied into bit position 31 of register Rul. (No bits are lost.) If C is negative, the contents of registers R and Rul are shifted right |C| places. Bits shifted past bit position 31 of register Rul are copied into bit position 0 of register R. (No bits are lost.)

Affected: (R), (Rul), CC1, CC2

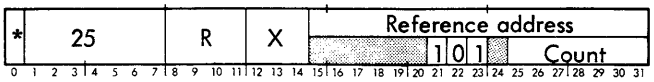
Arithmetic Shift, Single Register



If the shift count, C, is positive, the contents of register R are shifted left C places, with 0's copied into vacated bit positions on the right. (Bits shifted past R_0 are lost.) If C is negative, the contents of register R are shifted right |C| places, with the contents of bit position 0 copied into vacated bit positions on the left. (Bits shifted past R_{31} are lost.)

Affected: (R), CC1, CC2

Arithmetic Shift, Double Register



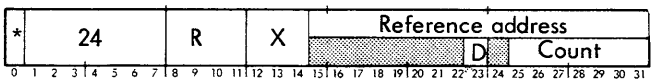
If the shift count, C, is positive, the contents of registers R and Rul are shifted left C places, with 0's copied into vacated bit positions on the right. Bits shifted past bit position 0 of register Rul are copied into bit position 31 of register R. (Bits shifted past R_0 are lost.) If C is negative, the contents of registers R and Rul are shifted right |C| places, with the contents of bit position 0 of register R copied into vacated bit positions on the left. Bits shifted past bit position 31 of register R are copied into bit position 0 of register Rul. (Bits shifted past Rul_{31} are lost.)

Affected: (R), (Rul), CC1, CC2

FLOATING-POINT SHIFT

Floating-point numbers are defined on page 44. The instruction format for floating-point shift operation is:

SF SHIFT FLOATING
(Word addressing)



If indirect addressing and/or indexing are called for in the instruction word, the effective address is computed as for the instruction SHIFT (see page 41) except that bit position 23 of the effective address determines the type of shift. If bit 23 is 0, the contents of register R are treated as a short-format floating-point number; if bit 23 is 1, the contents of registers R and Rul are treated as a long-format floating-point number.

The shift count, C, in bit positions 25 through 31 of the effective address determines the amount and direction of the shift. The shift count is treated as a 7-bit signed binary integer, with the high-order bit (bit position 25) as the sign (negative integers are represented in two's complement form). The absolute value of the shift count determines the number of hexadecimal digit positions the floating-point number is to be shifted. A positive shift count specifies a left shift; a negative shift count specifies a right shift.

SHIFT FLOATING loads the floating-point number from the register(s) specified by the R field of the instruction into a set of internal registers. If the number is negative, it is two's complemented. A record of the original sign is retained. The floating-point number is then separated into a characteristic and a fraction, and CC1 and CC2 are both reset to 0's.

A positive shift count produces the following left shift operations:

1. If the fraction is normalized (i.e., is less than 1 and is equal to or greater than 1/16, or the fraction is all 0's), CC1 is set to 1.
2. If the fraction field is all 0's, the entire floating-point number is set to all 0's (true zero), regardless of the sign and the characteristic of the original number.
3. If the fraction is not normalized, the fraction field is shifted 1 hexadecimal digit position (4 bit positions) to the left and the characteristic field is decremented by 1. Vacated digit positions at the right of the fraction are filled with hexadecimal 0's.

   If the characteristic field underflows (i.e., is all 1's as the result of being decremented), CC2 is set to 1. However, if the characteristic field does not underflow, the shift process (shift fraction, and decrement characteristic) continues until the fraction is normalized, until the characteristic field underflows, or until the fraction is shifted left C hexadecimal digit positions, whichever occurs first. (Any two, or all three, of the terminating conditions can occur simultaneously.)
4. At the completion of the left shift operation, the floating-point result is loaded back into the general register(s). If the number was originally negative, the two's complement of the resultant number is loaded into the general register(s).
5. The condition code settings following a floating-point left shift are as follows:

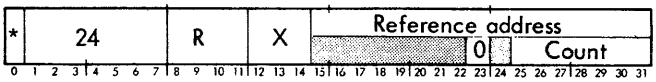
1	2	3	4	Result
-	-	0	0	true zero (all 0's)
-	-	0	1	negative
-	-	1	0	positive
0	0	-	-	C digits shifted (fraction unnormalized, no characteristic underflow)
1	-	-	-	fraction normalized (includes true zero)
-	1	-	-	characteristic underflow

A negative shift count produces the following right shift operations (again assuming that negative numbers are two's complemented before and after the shift operations):

1. The fraction field is shifted 1 hexadecimal digit position to the right and the characteristic field is incremented by 1. Vacated digit positions at the left are filled with hexadecimal 0's.
2. If the characteristic field overflows (i.e., is all 0's as the result of being incremented), CC2 is set to 1. However, if the characteristic field does not overflow, the shift process (shift fraction, and increment characteristic) continues until the characteristic field overflows or until the fraction is shifted right C hexadecimal digit positions, whichever occurs first. (Both terminating conditions can occur simultaneously.)
3. If the resultant fraction field is all 0's, the entire floating-point number is set to all 0's (true zero), regardless of the sign and the characteristic of the original number.
4. At the completion of the right shift operations, the floating-point result is loaded back into the general register(s). If the number was originally negative, the two's complement of the resultant number is loaded into the general register(s).
5. The condition code settings following a floating-point right shift are as follows:

1	2	3	4	Result
-	-	0	0	true zero (all 0's)
-	-	0	1	negative
-	-	1	0	positive
0	0	-	-	|C| digits shifted (no characteristic overflow)
0	1	-	-	characteristic overflow

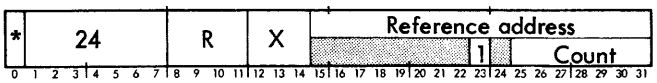
Floating Shift, Single Register



The short-format floating-point number in register R is shifted according to the rules established above for floating-point shift operations.

Affected: (R), CC

Floating Shift, Double Register



The long-format floating-point number in registers R and Rul is shifted according to the rules established above for floating point shift operations. (If the R field of the instruction word is an odd value, a long-format floating-point number is generated by duplicating the contents of register R, and the 32 high-order bits of the result are loaded into register R.)

Affected: (R), (Rul), CC

FLOATING-POINT INSTRUCTIONS

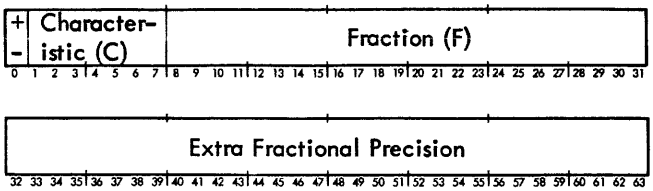
The following floating-point arithmetic instructions are available as optional SIGMA 5 instructions:

Instruction Name	Mnemonic	Page
Floating Add Short	FAS	47
Floating Add Long	FAL	47
Floating Subtract Short	FSS	47
Floating Subtract Long	FSL	48
Floating Multiply Short	FMS	48
Floating Multiply Long	FML	48
Floating Divide Short	FDS	48
Floating Divide Long	FDL	48

FLOATING-POINT NUMBERS

SIGMA 5 accommodates two number formats for floating-point arithmetic: short and long. A short-format floating-point number consists of a sign (bit 0), a biased, base 16 exponent, which is called a characteristic (bits 1-7), and a six-digit hexadecimal fraction (bits 8-31). A long-format floating-point number consists of a short-format floating-point number followed by an additional eight hexadecimal digits of fractional significance and occupies a doubleword memory location or an even-odd pair of general registers.

A SIGMA 5 floating-point number (N) has the following format:



A floating-point number (N) has the following formal definition:

1. $N = F \times 16^{C-64}$ where $F = 0$ or
   $16^{-6} \leq |F| < 1$ (short format) or
   $16^{-14} \leq |F| < 1$ (long format)
   and $0 \leq C \leq 127$
2. A positive floating-point number with a fraction of zero and a characteristic of zero is a "true" zero. A positive floating-point number with a fraction of zero and a nonzero characteristic is an "abnormal" zero. For floating-point multiplication and division, an abnormal zero is treated as a true zero. However, for addition and subtraction, an abnormal zero is treated the same as any nonzero operand.

3. A positive floating-point number is normalized if and only if the fraction is contained in the interval $1/16 \leq F < 1$.

4. A negative floating-point number is the two's complement of its positive representation.

5. A negative floating-point number is normalized if and only if its two's complement is a normalized positive number.

By this definition, a floating-point number of the form

1xxx xxxx 1111 0000 ... 0000

is normalized, and a floating-point number of the form

1xxx xxxx 0000 0000 ... 0000

is illegal and, whenever generated by floating-point instructions, is converted to the form

1yyy yyyy 1111 0000 ... 0000

where yy ... y is 1 less than xx ... x. Table 6 contains examples of floating-point numbers.

Modes of Operation

SIGMA 5 contains three mode control bits that are used to qualify floating-point operations. These mode control bits are identified as FS (floating significance), FZ (floating zero), and FN (floating normalize), and are contained in bit positions 5, 6, and 7, respectively, of the program status doubleword (PSD_{5-7}).

The floating-point mode is established by setting the three floating-point mode control bits. This can be performed by any of the following instructions:

Instruction Name	Mnemonic	Page
Load Conditions and Floating Control	LCF	30
Load Conditions and Floating Control Immediate	LCFI	30
Load Program Status Doubleword	LPSD	56
Exchange Program Status Doubleword	XPSD	56

The floating-point mode control bits are stored by executing either of the following instructions:

Instruction Name	Mnemonic	Page
Store Conditions and Floating Control	STCF	32
Exchange Program Status Doubleword	XPSD	56

UNIMPLEMENTED FLOATING-POINT INSTRUCTIONS

If the optional floating-point instruction set is not implemented in the computer and execution of a floating-point arithmetic instruction is attempted, the computer unconditionally aborts execution of the instruction (at the time of operation code decoding). The computer then traps to location X'41', with the contents of the condition code and

Table 6. Floating-point Number Representation

Decimal Number	Short Floating-point Format ±	C	F	Hexadecimal Value
$+(16^{+63})(1-2^{-24})$	0	111 1111	1111 1111 1111 1111 1111 1111	7F FFFFFF
$+(16^{+3})(5/16)$	0	100 0011	0101 0000 0000 0000 0000 0000	43 500000
$+(16^{-3})(209/256)$	0	011 1101	1101 0001 0000 0000 0000 0000	3D D10000
$+(16^{-63})(2047/4096)$	0	000 0001	0111 1111 1111 0000 0000 0000	01 7FF000
$+(16^{-64})(1/16)$	0	000 0000	0001 0000 0000 0000 0000 0000	00 100000
0 (called true zero)	0	000 0000	0000 0000 0000 0000 0000 0000	00 000000
$-(16^{-64})(1/16)$	1	111 1111	1111 0000 0000 0000 0000 0000	FF F00000
$-(16^{-63})(2047/4096)$	1	111 1110	1000 0000 0001 0000 0000 0000	FE 801000
$-(16^{-3})(209/256)$	1	100 0010	0010 1111 0000 0000 0000 0000	C2 2F0000
$-(16^{+3})(5/16)$	1	011 1100	1011 0000 0000 0000 0000 0000	BC B00000
$-(16^{+63})(1-2^{24})$	1	000 0000	0000 0000 0000 0000 0000 0001	80 000001
Special Case				
$-(16^{e})(1)$	1	$\overline{e}$	0000 0000 0000 0000 0000 0000	
is changed to				
$-(16^{e+1})(1/16)$	1	$\overline{e+1}$	1111 0000 0000 0000 0000 0000	

whenever generated as the result of a floating-point instruction.

all general registers unchanged. Location X'41' is the "unimplemented instruction" trap location.

FLOATING-POINT ADDITION AND SUBTRACTION

The floating normalize (FN), floating zero(FZ), and floating significance (FS) mode control bits determine the operation of floating-point addition and subtraction (if characteristic overflow does not occur) as follows:

FN Floating normalize:

- FN = 0 The results of additions and subtractions are to be postnormalized. If characteristic overflow occurs, if the result is zero, or if more than two postnormalization hexadecimal shifts are required, the settings for FZ and FS determine the resultant action. If none of the above conditions occur, the condition code is set to 0010 if the result is positive or to 0001 if the result is negative.
- FN = 1 Inhibit postnormalization of the results of additions and subtractions. The settings of FZ and FS have no effect on the instruction operation. If the result is zero, the result is set to true zero and the condition code is set to 0000. If the result is positive, the condition code is set to 0010. If the result is negative, the condition code is set to 0001.

FZ Floating zero: (applies only if FN = 0)

- FZ = 0 If the final result of an addition or subtraction operation cannot be expressed in normalized form because of the characteristic being reduced below zero, underflow has occurred, in which case the result is set equal to true zero and the condition code is set to 1100. (Exception: if a trap results from significance checking with FS = 1 and FZ = 0, an underflow generated in the process of postnormalizing is ignored.)
- FZ = 1 Characteristic underflow causes the computer to trap to location X'44' with the contents of the general registers unchanged. If the result is positive, the condition code is set to 1110. If the result is negative, the condition code is set to 1101.

FS Floating significance: (applies only if FN = 0)

- FS = 0 Inhibit significance trap. If the result of an addition or subtraction is zero, the result is set equal to true zero, the condition code is set to 1000, and the computer executes the next instruction in sequence. If more than two hexadecimal places of postnormalization shifting are required and characteristic underflow does not occur, the condition code is set to 1010 if the result is positive, or to 1001 if the result is negative; then, the computer executes the next instruction in sequence. (Exception: if characteristic underflow occurs with FS = 0, FZ determines the resultant action.)
- FS = 1 The computer traps to location X'44' if more than two hexadecimal places of postnormalization shifting are required or if the result is zero. The condition code is set to 1000 if the result is zero, to 1010 if the result is positive, or to 1001 if the result is negative; however, the contents of the general registers are not changed. (Exception: if a trap results from characteristic underflow with FZ = 1, the results of significance testing are ignored.)

If characteristic overflow occurs, the CPU always traps to location X'44' with the general registers unchanged and the condition code set to 0110 if the result is positive, or to 0101 if the result is negative.

FLOATING-POINT MULTIPLICATION AND DIVISION

The floating zero (FZ) mode control bit alone determines the operation of floating-point multiplication and division (if characteristic underflow does not occur and division by zero is not attempted) as follows:

FZ Floating zero:

- FZ = 0 If the final result of a multiplication or division operation cannot be expressed in normalized form because of the characteristic being reduced below zero, underflow has occurred. If underflow occurs or if the result is zero, the result is set equal to true zero and the condition code is set to 0000. Otherwise, the condition code is set to 0010 if the result is positive, or to 0001 if the result is negative.
- FZ = 1 Underflow causes the computer to trap to location X'44' with the contents of the general registers unchanged. The condition code is set to 1110 if the result is positive, or to 1101 if the result is negative. If underflow does not occur, the resultant action is the same as that for FZ = 0.

If the divisor is zero in a floating-point division, the computer always traps to location X'44' with the general register unchanged and the condition code set to 0100. If characteristic overflow occurs, the computer always traps to location X'44' with the general register unchanged and the condition code set to 0110 if the result is positive, or to 0101 if the result is negative.

CONDITION CODES FOR FLOATING-POINT INSTRUCTIONS

The condition code settings for floating-point instructions are summarized in Table. 7. The following provisions apply to all floating-point instructions:

1. Underflow and overflow detection apply to the final characteristic, not to any "intermediate" value.
2. If a floating-point operation results in a trap, the original contents of all general registers remain unchanged.
3. All shifting and truncation are performed on absolute magnitudes. If the fraction is negative, the two's complement is formed after shifting or truncation.

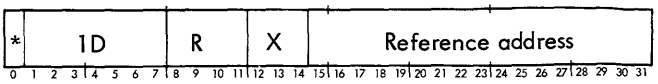
FAS FLOATING ADD SHORT
(Word addressing, optional)

The effective word and the contents of register R are loaded into a set of internal registers and a low-order hexadecimal zero (guard digit) is appended to both fractions, extending them to seven hexadecimal digits each. FAS then forms the floating-point sum ot the two numbers. If no floating-point arithemtic fault occurs, the sum is loaded into register R as a short-format floating-point number.

Affected: (R), CC
(R) + EW⟶R

Traps: Unimplemented instruction, floating-point arithmetic fault

FAL FLOATING ADD LONG
(Doubleword addressing, optional)



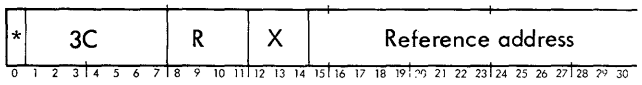
The effective doubleword and the contents of registers R and Ru1 are loaded into a set of internal registers.

The operation of FAL is identical to that of FLOATING ADD SHORT (FAS) except that the fractions to be added are each 14 hexadecimal digits long, guard digits are not appended to the fractions, and R must be an even value for correct results. If no floating-point arithmetic fault occurs, the sum is loaded into registers R and Ru1 as a long-format floating-point number.

Affected: (R), (Ru1), CC

Traps: Unimplemented instruction, floating-point arithmetic fault

FSS FLOATING SUBTRACT SHORT
(Word addressing, optional)



The effective word and the contents of register R are loaded into a set of internal registers.

FLOATING SUBTRACT SHORT forms the two's complement of the effective word and then operates identically to FLOATING ADD SHORT (FAS). If no floating-point arith-

Table 7. Condition Code Settings for Floating-point Instructions

Condition Code 1	2	3	4	Meaning if no trap to location X'44' occurs	Meaning if trap to location X'44' occurs
0	0	0	0	A x 0, 0/A, or -A + A① with FN=1 } normal results	*②
0	0	0	1	N < 0	*
0	0	1	0	N > 0	*
0	1	0	0	*②	divide by zero } always trapped
0	1	0	1	*	overflow, N < 0
0	1	1	0	*	overflow, N > 0
③ 1	0	0	0	-A + A①	-A + A
1	0	0	1	N < 0 } > 2 postnormalizing shifts } FS=0, FN=0, and no underflow	N < 0 } > 2 postnormalizing shifts } FS=1, FN=0, and no underflow with FZ=1
1	0	1	0	N > 0	N > 0
1	1	0	0	underflow with FZ=0 and no trap by FS=1①	*
1	1	0	1	*	underflow, N < 0 } FZ=1
1	1	1	0	*	underflow, N > 0

① result set to true zero

② "*" indicates impossible configurations

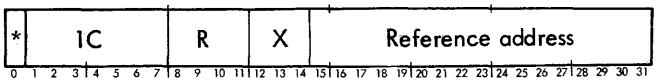
③ applies to add and subtract only where FN=0

metic fault occurs, the difference is loaded into register R as a short-format floating-point number.

Affected: (R), CC
(R) - EW⟶R

Traps: Unimplemented instruction, floating-point arithmetic fault

FSL FLOATING SUBTRACT LONG
(Doubleword addressing, optional)



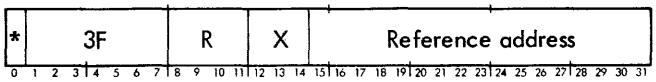
The effective doubleword and the contents of registers R and Ru1 are loaded into a set of internal registers.

FLOATING SUBTRACT LONG forms the two's complement of the effective doubleword and then operates identically to FLOATING ADD LONG (FAL). If no floating-point arithmetic fault occurs, the difference is loaded into registers R and Ru1 as a long-format floating-point number.

Affected: (R), (Ru1), CC
(R, Ru1) - ED⟶R, Ru1

Traps: Unimplemented instruction, floating-point arithmetic fault

FMS FLOATING MULTIPLY SHORT
(Word addressing, optional)



The effective word (multiplier) and the contents of register R (multiplicand) are loaded into a set of internal registers, and both numbers are then prenormalized (if necessary). The product of the fractions contains 14 hexadecimal digits (the lower two of which are 0's). If no floating-point arithmetic fault occurs, the product is loaded into registers R and Ru1 as follows:

1. If R is an even value, the product is loaded into registers R and R + 1 as a long-format floating-point number.

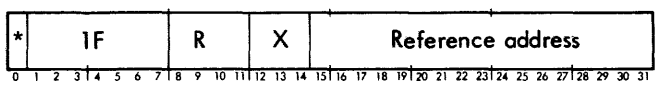
2. If R is an odd value, the product is loaded into register R as a properly truncated short-format floating-point number.

The result of floating multiply is always postnormalized. At most, one place of postnormalizing shift may be required. Truncation takes place after postnormalization.

Affected: (R), (Ru1), CC
(R) x EW⟶R, Ru1

Traps: Unimplemented instruction, floating-point arithmetic fault

FML FLOATING MULTIPLY LONG
(Doubleword addressing, optional)

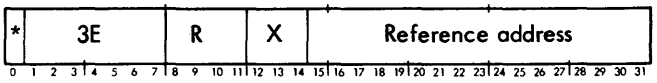


The effective doubleword (multiplier) and the contents of registers R and Ru1 (multiplicand) are loaded into a set of internal registers. FLOATING MULTIPLY LONG then operates identically to FLOATING MULTIPLY SHORT (FMS), except that the multiplier, the multiplicand, and the product fractions are each 14 hexadecimal digits long, and R must be an even value for correct results. If no floating-point arithmetic fault occurs, the postnormalized product is truncated to a long-format floating-point number and loaded into registers R and Ru1.

Affected: (R), (Ru1), CC
(R, Ru1) x ED⟶R, Ru1

Traps: Unimplemented instruction, floating-point arithmetic fault

FDS FLOATING DIVIDE SHORT
(Word addressing, optional)



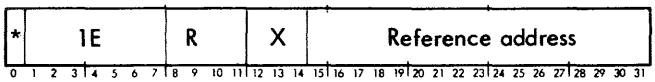
The effective word (divisor) and the contents of register R (dividend) are loaded into a set of internal registers and both numbers are then prenormalized (if necessary).

FLOATING DIVIDE SHORT then forms a floating-point quotient with a 6-digit, normalized hexadecimal fraction. If no floating-point arithmetic fault occurs, the quotient is loaded into register R as a short-format floating-point number.

Affected: (R), CC
(R) ÷ EW⟶R

Traps: Unimplemented instruction, floating-point arithmetic fault

FDL FLOATING DIVIDE LONG
(Doubleword addressing, optional)



The effective doubleword (divisor) and the contents of registers R and Ru1 (dividend) are loaded into a set of internal registers. FLOATING DIVIDE LONG then operates identically to FLOATING DIVIDE SHORT (FDS), except that the dividend, the divisor, and the quotient fractions are each 14 hexadecimal digits long, and R must be an even value for correct results. If no floating-point arithmetic fault occurs, the quotient is loaded into registers R and Ru1 as a long-format floating-point number.

Affected: (R), (Ru1), CC
(R, Ru1) ÷ ED ⟶ R, Ru1

Traps: Unimplemented instruction, floating-point arithmetic fault

PUSH-DOWN INSTRUCTIONS

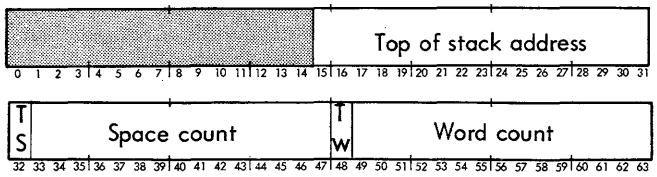
The term "push-down processing" refers to the programming technique (used extensively in recursive routines) of storing the context of a calculation in memory, proceeding with a new set of information, and then activating the previously

stored information. Typically, this process involves a reserved area of memory (stack) into which operands are pushed (stored) and from which operands are pulled (loaded) on a last-in, first-out basis. The SIGMA 5 computer provides for simplified and efficient programming of push-down processing by means of the following instructions:

Instruction Name	Mnemonic	Page
Push Word	PSW	50
Pull Word	PLW	50
Push Multiple	PSM	51
Pull Multiple	PLM	51
Modify Stack Pointer	MSP	52

STACK POINTER DOUBLEWORD

Each of these instructions operates with respect to a memory stack that is defined by a doubleword located at the effective address of the instruction. This doubleword, referred to as a stack pointer doubleword (SPD), has the following structure:



Bit positions 15 through 31 of the SPD contain a 17-bit address field that points to the location of the word currently at the top (highest-numbered address) of the operand stack. In a push operation, the top-of-stack address is incremented by 1 and then an operand in a general register is pushed (stored) into that location, thus becoming the contents of the new top of the stack; the contents of the previous top of the stack remain unchanged. In a pull operation, the contents of the current top of the stack are pulled (loaded) into a general register and then the top-of-stack address is decremented by 1; the previous stack contents remain unchanged.

Bit positions 33 through 47 of the SPD, referred to as the space count, contain a 15-bit count (0 to 32,767) of the number of word locations currently available in the region of memory allocated to the stack. Bit positions 49 through 63 of the SPD, referred to as the word count, contain a 15-bit count (0 to 32,767) of the number of words currently in the stack. In a push operation, the space count is decremented by 1 and the word count is incremented by 1; in a pull operation, the space count is incremented by 1 and the word count is decremented by 1. At the beginning of all push-down instructions, the space count and the word count are each tested to determine whether or not the instruction would cause either count field to be incremented above the upper limit of $2^{15}-1$ (32,767), or to be decremented below the lower limit of 0. If execution of the push-down instruction would cause either count limit to be exceeded, the computer unconditionally aborts execution of the instruction, with the stack, the stack pointer doubleword, and the contents of the general registers unchanged. Ordinarily, the computer traps to location X'42' after aborting a push-down instruction because of impending stack limit overflow or underflow, and with the condition code unchanged from the value it contained before execution of the instruction. However, this trap action can be selectively inhibited by setting either (or both) of the trap inhibit bits in the SPD to 1.

Bit position 32 of the SPD, referred to as the trap-on-space (TS) inhibit bit, determines whether or not the computer is to trap to location X'42' as a result of impending overflow or underflow of the space count (SPD_{33-47}), as follows:

TS	Space count overflow/underflow action
0	If the execution of a pull instruction would cause the space count to exceed $2^{15}-1$, or if the execution of a push instruction would cause the space count to be less than 0, the computer traps to location X'42' with the condition code unchanged

TS	Space count overflow/underflow action
1	Instead of trapping to location X'42', the computer sets CC1 to 1 and then executes the next instruction in sequence

Bit position 48 of the SPD, referred to as the trap-on-word (TW) inhibit bit, determines whether or not the computer is to trap to location X'42' as a result of impending overflow or underflow of the word count (SPD_{49-63}) as follows:

TW	Word count overflow/underflow action
0	If the execution of a push instruction would cause the word count to exceed $2^{15}-1$, or if the execution of a pull instruction would cause the word count to be less than 0, the computer traps to location X'42' with the condition code unchanged.
1	Instead of trapping to location X'42', the computer sets CC3 to 1 and then executes the next instruction in sequence.

PUSH-DOWN CONDITION CODE SETTINGS

If the execution of a push-down instruction is attempted and the computer traps to location X'42', the condition code remains unchanged from the value it contained immediately before the instruction was executed.

If execution of a push-down instruction is attempted and the instruction is aborted because of impending stack limit overflow or underflow (or both) but the push-down stack limit trap is inhibited by one (or both) of the inhibits (TS and TW), then CC1 and CC3 indicate the reason for aborting the push-down instruction, as follows:

1	2	3	4	Reason for abort
0	-	1	-	impending overflow of word count on a push operation or impending underflow of word count on a pull operation. The push-down stack limit trap was inhibited by the TW bit (SPD_{48})
1	-	0	-	impending overflow of space count on a pull operation or impending underflow of space count on a push operation. The

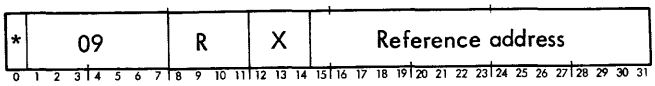
1	2	3	4	Reason for abort
				push-down stack limit trap was inhibited by the TS bit (SPD_{32})
1	-	1	-	impending overflow of word count and underflow of space count on a push operation or impending overflow of space count and underflow of word count on a pull operation. The push-down stack limit trap was inhibited by both the TW and the TS bits

If a push-down instruction is successfully executed, CC1 and CC3 are reset to 0 at the completion of the instruction. Also, CC2 and CC4 are independently set to indicate the current status of the space count and the word count, respectively, as follows:

1	2	3	4	Status of space and word counts
0	0	0	0	the current space count and the current word count are both greater than zero
0	0	0	1	the current space count is greater than zero, but the current word count is zero, indicating that the stack is now empty. If the next operation on the stack is a pull instruction, the instruction will be aborted
0	1	0	0	the current word count is greater than zero, but the current space count is zero indicating that the stack is now full. If the next operation on the stack is a push instruction, the instruction will be aborted.

If the computer does not trap to location X'42' as a result of impending stack limit overflow/underflow, CC2 and CC4 indicate the status of the space and word counts at the termination of the push-down instruction, regardless of whether or not the space and word counts were actually modified by the instruction. In the following descriptions of the push-down instruction, only those condition codes are given that can actually be produced by the instruction, provided the computer does not trap to location X'42'.

PSW PUSH WORD
(Doubleword addressing)



PUSH WORD stores the contents of register R into the push-down stack defined by the stack pointer doubleword located at the effective doubleword address of PSW. If the push operation can be successfully performed, the instruction operates as follows:

1. The current top-of-stack address (SPD_{15-31}) is incremented by 1, to point to the new top-of-stack location.

2. The contents of register R are stored in the location pointed to by the new top-of-stack address.

3. The space count (SPD_{33-47}) is decremented by 1 and the word count (SPD_{49-63}) is incremented by 1.

4. The condition code is set to reflect the new status of the space count.

Affected: (SPD), (TSA+1), CC Trap: Push-down stack limit

$(SPD)_{15-31} + 1 \longrightarrow SPD_{15-31}$

$(R) \longrightarrow (SPD_{15-31})$

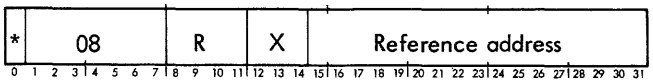
$(SPD)_{33-47} - 1 \longrightarrow SPD_{33-47}$

$(SPD)_{49-63} + 1 \longrightarrow SPD_{49-63}$

Condition code settings:

1	2	3	4	Result of PSW	
0	0	0	0	space count is greater than 0	instruction completed
0	1	0	0	space count is now 0	instruction completed
0	0	1	0	word count = $2^{15}-1$, TW = 1	instruction aborted
1	1	0	0	space count = 0, TS = 1	instruction aborted
1	1	0	1	space count = 0, word count = 0, TS = 1	instruction aborted
1	1	1	0	word count = $2^{15}-1$, space count = 0 TW = 1, and TS = 1	instruction aborted

PLW PULL WORD
(Doubleword addressing)



PULL WORD loads register R with the word currently at the top of the push-down stack defined by the stack pointer doubleword located at the effective doubleword address of PLW. If the pull operation can be performed successfully, the instruction operates as follows:

1. Register R is loaded with the contents of the location pointed to by the current top-of-stack address (SPD_{15-31}).

2. The current top-of-stack address is decremented by 1, to point to the new top-of-stack location.

3. The space count (SPD_{33-47}) is incremented by 1 and the word count (SPD_{49-63}) is decremented by 1.

4. The condition code is set to reflect the status of the new word count.

Affected: (SPD), (R), CC Trap: Push-down stack limit

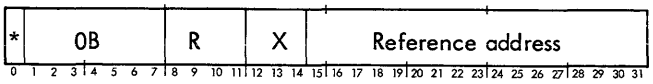
$((SPD)_{15-31}) \longrightarrow R$; $(SPD)_{15-31} - 1 \longrightarrow SPD_{15-31}$

$(SPD)_{33-47} + 1 \longrightarrow SPD_{33-47}$; $(SPD)_{49-63} - 1 \longrightarrow SPD_{49-63}$

Condition code settings:

1	2	3	4	Result of PLW	
0	0	0	0	word count is greater than 0	instruction completed
0	0	0	1	word count is now 0	
0	0	1	1	word count = 0, TW = 1	
0	1	1	1	space count = 0, word count = 0, TW = 1	
1	0	0	0	space count = 2^{15}-1, TS = 1	instruction aborted
1	0	1	1	space count = 2^{15}-1, word count = 0, TS = 1, and TW = 1	

PSM PUSH MULTIPLE
(Doubleword addressing)



PUSH MULTIPLE stores the contents of a sequential set of general registers into the push-down stack defined by the stack pointer doubleword located at the effective doubleword address of PSM. The condition code is assumed to contain a count of the number of registers to be pushed into the stack. (An initial value of 0000 for the condition code specifies that all 16 general registers are to be pushed into the stack.) The registers are treated as a circular set (with register 0 following register 15) and the first register to be pushed into the stack is register R. The last register to be pushed into the stack is register R + CC -1, and the contents of this register become the contents of the new top-of-stack location.

If there is sufficient space in the stack for all of the specified registers, PSM operates as follows:

1. The contents of registers R to R + CC -1 are stored in an ascending sequence, beginning with the location pointed to by the current top-of-stack address (SPD_{15-31}) plus 1 and ending with the current top-of-stack address plus CC.
2. The current top-of-stack address is incremented by the value of CC, to point to the new top-of-stack location.
3. The space count (SPD_{33-47}) is decremented by the value of CC and the word count is incremented by the value of CC.
4. The condition code is set to reflect the new status of the space count.

Affected: (SPD), (TSA+1 to TSA+CC), CC

Trap: Push-down stack limit

$(R) \longrightarrow (SPD_{15-31})+1 \ldots (R+CC-1) \longrightarrow (SPD_{15-31})+CC$

$(SPD)_{15-31}+CC \longrightarrow SPD_{15-31}$

$(SPD)_{33-47}-CC \longrightarrow SPD_{33-47}$

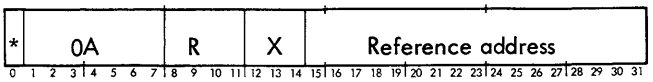
$(SPD)_{49-63}+CC \longrightarrow SPD_{49-63}$

If the instruction starts storing words into an accessible region of memory and then crosses a memory page boundary into an inaccessible region, either the memory protection trap or the nonexistent memory trap can occur. In either case, the trap is activated with the condition code unchanged from the value it contained before the execution of PSM. The effective address of the instruction permits the trap routine to compute how many words of memory have been changed. Since it is permissible to use indirect addressing through one of the affected locations, or even to execute an instruction located in one of the affected locations, a trapped PSM instruction may have already overwritten the direct address, or the PSM instruction itself, thus destroying any possibility of continuing the program successfully. If such programming must be done, it is advisable that the direct address, or the PSM instruction, occupy the last location in which the contents of a register are to be stored by the PSM instruction.

Condition code settings:

1	2	3	4	Result of PSM	
0	0	0	0	space count > 0	instruction completed
0	1	0	0	space count = 0	
0	0	1	0	word count + CC > 2^{15} - 1, TW = 1	instruction aborted
1	0	0	0	space count < CC, TS = 1	
1	0	0	1	space count < CC, word count = 0, TS = 1	
1	0	1	0	space count < CC, word count + CC > 2^{15}-1, TS = 1, and TW = 1	
1	1	0	0	space count = 0, TS = 1	
1	1	0	1	space count = 0, word count = 0, TS = 1	
1	1	1	0	space count = 0, word count + CC > 2^{15} -1, TS = 1, and TW = 1	

PLM PULL MULTIPLE
(Doubleword addressing)



PULL MULTIPLE loads a sequential set of general registers from the push-down stack defined by the stack pointer doubleword located at the effective doubleword address of PLM. The condition code is assumed to contain a count of the number of words to be pulled from the stack. (An initial value of 0000 for the condition code specifies that 16 words are to be pulled from the stack.) The registers are treated as a circular set (with register 0 following register 15), the first register to be loaded from the stack is register R + CC -1, and the contents of the current top-of-stack location becomes the contents of this register. The last register to be loaded is register R.

If there is a sufficient number of words in the stack to load all of the specified registers, PLM operates as follows:

1. Registers R + CC -1 to register R are loaded in a descending sequence, beginning with the contents of the location pointed to by the current top-of-stack address (SPD_{15-31}) and ending with the contents of the location pointed to by the current top-of-stack address minus (CC -1).
2. The current top-of-stack address is decremented by the value of CC, to point to the new top-of-stack location.
3. The space count (SPD_{33-47}) is incremented by the value of CC and the word count is decremented by the value of CC.
4. The condition code is set to reflect the new status of the word count.

Affected: (SPD), (R+CC-1) to (R), CC Trap: Push-down stack limit

$((SPD)_{15-31}) \longrightarrow R+CC-1, \ldots,$

$((SPD)_{15-31} - |CC-1|) \longrightarrow R$

$(SPD)_{15-31} - CC \longrightarrow SPD_{15-31}$

$(SPD)_{33-47} + CC \longrightarrow SPD_{33-47}$

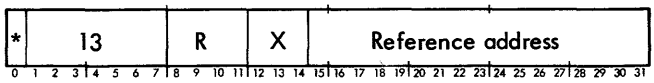
$(SPD)_{49-63} - CC \longrightarrow SPD_{49-63}$

If the instruction starts loading words from an existent region of memory and then crosses a memory page boundary into a nonexistent memory region, the nonexistent memory address trap occurs. In this case, the trap is activated with the condition code unchanged from the value it contained before the execution of PLM. The effective address of the instruction permits the trap routine to compute how many registers have been loaded. Since it is permissible to use indirect addressing through a general register, indexing, or even to execute an instruction located in a general register, a trapped PLM instruction may have already overwritten the index, direct address, or the PLM instruction itself, thus destroying any possibility of continuing the program successfully. If such programming must be done, it is advisable that the register containing the direct address, index displacement, or instruction be the last register loaded by the PLM instruction.

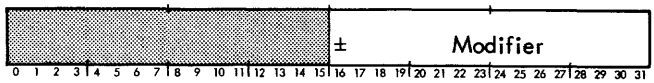
Condition code settings:

1	2	3	4	Result of PLM	
0	0	0	0	word count > 0	instruction completed
0	0	0	1	word count = 0	
0	0	1	0	word count < CC, TW = 1	instruction aborted
0	0	1	1	word count = 0, TW = 1	
0	1	1	0	space count = 0, word count < CC, TW = 1	
0	1	1	1	space count = 0, word count = 0, TW = 1	
1	0	0	0	space count + CC > 2^{15}-1, TS = 1	
1	0	1	0	space count + CC > 2^{15}-1, word count < CC, TS = 1, and TW = 1	
1	0	1	1	space count + CC > 2^{15}-1, word count = 0, TS = 1, and TW = 1	

MSP MODIFY STACK POINTER
(Doubleword addressing)



MODIFY STACK POINTER modifies the stack pointer doubleword, located at the effective doubleword address of MSP, by the contents of register R. Register R is assumed to have the following format:



Bit positions 16 through 31 of register R are treated as a signed integer, with negative integers in two's complement form (i.e., a fixed-point halfword). The modifier is algebraically added to the top-of-stack address, subtracted from the space count, and added to the word count in the stack pointer doubleword. If, as a result of MSP, either the space count or the word count would be decreased below 0 or increased above 2^{15}-1, the instruction is aborted. Then, the computer either traps to location X'42' or sets the condition code to reflect the reason for aborting, depending on the stack limit trap inhibits.

If the modification of the stack pointer doubleword can be successfully performed, MSP operates as follows:

1. The modifier in register R is algebraically added to the current top-of-stack address $(SPD)_{15-31}$, to point to a new top-of-stack location. (If the modifier is negative, it is extended to 17 bits by appending a high-order 1.)
2. The modifier is algebraically subtracted from the current space count (SPD_{33-47}) and the result becomes the new space count.
3. The modifier is algebraically added to the current word count (SPD_{49-63}) and the result becomes the new word count.

Affected: (SPD), CC Trap: Push-down stack limit

$(SPD)_{15-31} + (R)_{16-31SE} \longrightarrow SPD_{15-31}$

$(SPD)_{33-47} - (R)_{16-31} \longrightarrow SPD_{33-47}$

$(SPD)_{49-63} + (R)_{16-31} \longrightarrow SPD_{49-63}$

Condition code settings:

1	2	3	4	Result of MSP	
0	0	0	0	space count > 0, word count > 0	instruction completed
0	0	0	1	space count > 0, word count = 0	
0	1	0	0	space count = 0, word count > 0	
0	1	0	1	space count = 0, word count = 0, modifier = 0	

If CC1, or CC3, or both CC1 and CC3 are 1's after execution of MSP, the instruction was aborted but the push-down stack limit trap was inhibited by the trap-on-space inhibit (SPD_{32}), by the trap-on-word inhibit (SPD_{48}), or both. The condition code is set to reflect the reason for aborting as follows:

1	2	3	4	Status of space count and word count
-	-	-	0	word count > 0
-	-	-	1	word count = 0
-	-	0	-	$0 \leq$ word count + modifier $\leq 2^{15}-1$
-	-	1	-	word count + modifier < 0 and TW = 1, or word count + modifier > $2^{15}-1$ and TW = 1
-	0	-	-	space count > 0
-	1	-	-	space count = 0
0	-	-	-	$0 \leq$ space count - modifier $\leq 2^{15}-1$
1	-	-	-	space count - modifier < 0 and TS = 1, or space count - modifier > $2^{15}-1$ and TS = 1

EXECUTE/BRANCH INSTRUCTIONS

The EXECUTE instruction can be used to insert another instruction into the program sequence, and the branch instructions can be used to alter the program sequence, either unconditionally or conditionally. If a branch is unconditional (or conditional and the branch condition is satisfied), the instruction pointed to by the effective address of the branch instruction is normally the next instruction to be executed. If a branch is conditional and the condition for the branch is not satisfied, the next instruction is normally taken from the next location, in ascending sequence, after the branch instruction.

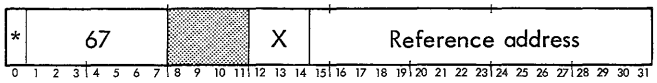
Prior to the time that an instruction is accessed from memory for execution, bit positions 15-31 of the program status doubleword contain the core memory address of the instruction, referred to as the instruction address. At this time, the computer traps to location X'40' if the instruction address is nonexistent. If the instruction address is existent, the instruction is accessed and the instruction address portion of the program status doubleword is incremented by 1, so that it now contains the address of the next instruction in sequence (referred to as the updated instruction address).

If a trap condition occurs during the execution sequence of any instruction, the computer decrements the updated instruction address by 1 and then traps to the location assigned to the trap condition. If neither a trap condition nor a satisfied branch condition occurs during the execution of an instruction, the next instruction is accessed from the location pointed to by the updated instruction address. If a satisfied branch condition occurs during the execution of a branch instruction (and no trap condition occurs), the next instruction is accessed from the location pointed to by the effective address of the branch instruction. Thus, during execution of a branch instruction, the updated instruction address is decremented, unchanged, or replaced, as determined by the following critera:

1. Trap condition. A nonallowed operation trap condition can occur during execution of a branch instruction, but only if an attempt is made to access a nonexistent memory address. The trap condition occurs in the following situations:
   a. The branch instruction is indirectly addressed, but the address of the location containing the direct address is nonexistent.
   b. The branch instruction is unconditional (or the branch is conditional and the condition for the branch is satisfied), but the effective address of the branch instruction is nonexistent.

   If either or both of the above situations occur, the computer aborts execution of the branch instruction, decrements the updated instruction address by 1, and traps to location X'40'. In this case, the instruction address value (IA) stored by the XPSD instruction in location X'40' is the address of the aborted branch instruction.
2. No branch condition. If the branch instruction is conditional, the condition for the branch is not satisfied, and no trap condition occurs, the updated instruction address remains unchanged. Then, instruction execution proceeds with the instruction pointed to by the updated instruction address.
3. Branch condition. If the branch instruction is unconditional (or if the branch instruction is conditional and the condition for the branch is satisfied) and no trap condition occurs, the updated instruction address is replaced by the effective address of the branch instruction. Then, instruction execution proceeds with the instruction located at the effective address of the branch instruction.

EXU EXECUTE
(Word addressing)



EXECUTE causes the computer to access the instruction in the location pointed to by the effective address of EXU and execute the subject instruction. The execution of the subject instruction, including the processing of trap and in-

terrupt conditions, is performed exactly as if the subject instruction were initially accessed instead of the EXU instruction. If the subject instruction is another EXU, the computer executes the subject instruction pointed to by the effective address of the second EXU as described above. Such "chains" of EXECUTE instructions may be of any length, and are processed (without affecting the updated instruction address) until an instruction other than EXU is encountered. After the final subject instruction is executed, instruction execution proceeds with the next instruction in sequence after the initial EXU (unless the subject instruction is an unconditional branch or is a conditional branch instruction and the branch condition is satisfied).

If an interrupt activation occurs between the beginning of an EXU instruction (or chain of EXU instructions) and the last interruptible point in the subject instruction, the computer processes the interrupt-servicing routine for the active interrupt level and then returns program control to the EXU instruction (or the initial instruction of a chain of EXU instructions), which is started anew. Note that a program is interruptible after every instruction access, including accesses made with the EXU instruction, and the interruptibility of the subject instruction is the same as the normal interruptibility for that instruction.

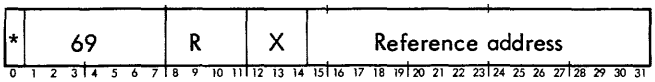
If a trap condition occurs between the beginning of an EXU instruction (or chain of EXU instructions) and the completion of the subject instruction, the computer traps to the appropriate trap location. The instruction address stored by the XPSD instruction in the trap location is the address of the EXU instruction (or the initial instruction of a chain of EXU instructions).

Affected: Determined by subject instruction

Traps: Determined by subject instruction

Condition code settings: Determined by subject instruction.

BCS BRANCH ON CONDITIONS SET
(Word addressing)



BRANCH ON CONDITIONS SET forms the logical product (AND) of the R field of the instruction word and the current condition code. If the logical product is nonzero, the branch condition is satisfied and instruction execution proceeds with the instruction pointed to by the effective address of the BCS instruction. However, if the logical product is zero, the branch condition is unsatisfied and instruction execution then proceeds with the next instruction in normal sequence.

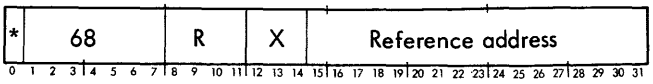
Affected: (IA) if CC n R $\neq$ 0

If CC n $(I)_{8-11} \neq 0$, $EA_{15-31} \longrightarrow IA$

If CC n $(I)_{8-11} = 0$, IA not affected

If the R field of BCS is 0, the next instruction to be executed after BCS is always the next instruction in ascending sequence, thus effectively producing a "no operation" instruction.

BCR BRANCH ON CONDITIONS RESET
(Word addressing)



BRANCH ON CONDITIONS RESET forms the logical product (AND) of the R field of the instruction word and the current condition code. If the logical product is zero, the branch condition is satisfied and instruction execution then proceeds with the instruction pointed to by the effective address of the BCR instruction. However, if the logical product is nonzero, the branch condition is unsatisfied and instruction execution then proceeds with the next instruction in normal sequence.

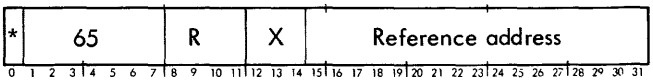
Affected: (IA) if CC n R = 0

If CC n $(I)_{8-11} = 0$, $EA_{15-31} \longrightarrow IA$

If CC n $(I)_{8-11} \neq 0$, IA not affected

If the R field of BCR is 0, the next instruction to be executed after BCR is always the instruction located at the effective address of BCR, thus effectively producing a "branch unconditionally" instruction.

BIR BRANCH ON INCREMENTING REGISTER
(Word addressing)



BRANCH ON INCREMENTING REGISTER increments the contents of general register R by 1. If the result is a negative value, the branch condition is satisfied and instruction execution then proceeds with the instruction pointed to by the effective address of the BIR instruction. However, if the result is zero or a positive value, the branch condition is not satisfied and instruction execution proceeds with the next instruction in normal sequence.

Affected: (R), (IA)

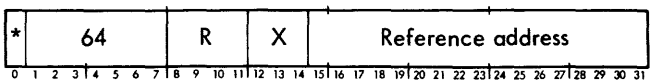
$(R) + 1 \longrightarrow R$

If $(R)_0 = 1$, $EA_{15-31} \longrightarrow IA$

If $(R)_0 = 0$, IA not affected

If the effective address of BIR is a nonexistent memory address and the result of incrementing register R is a negative value, the computer aborts execution of the BIR instruction (with register R containing the value that existed just before the BIR instruction) and traps to location X'40'. In this case, the instruction address stored by the XPSD instruction in location X'40' is the address of the aborted BIR instruction.

BDR BRANCH ON DECREMENTING REGISTER
(Word addressing)



BRANCH ON DECREMENTING REGISTER decrements the contents of general register R by 1. If the result is a positive value, the branch condition is satisfied and instruction execution then proceeds with the instruction pointed to by

the effective address of the BDR instruction. However, if the result is zero or a negative value, the branch condition is unsatisfied and instruction execution proceeds with the next instruction in normal sequence.

Affected: (R), (IA)

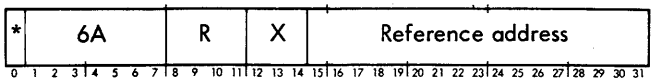
$(R) - 1 \longrightarrow R$

If $(R)_0 = 0$ and $(R)_{1-31} \neq 0$, $EA_{15-31} \longrightarrow IA$

If $(R)_0 = 1$ or $(R) = 0$, IA not affected

If the effective address of BDR is a nonexistent memory address and the result of decrementing register R is zero or is a positive value, the computer aborts execution of the BDR instruction (with register R containing the value that existed just before the BDR instruction) and traps to location X'40'. In this case, the instruction address stored by the XPSD instruction in location X'40' is the address of the aborted BDR instruction.

BAL BRANCH AND LINK
(Word addressing)



BRANCH AND LINK determines the effective address, loads the updated instruction address (the address of the next instruction in normal sequence after the BAL instruction) into bit positions 15-31 of general register R, clears bit position 0-14 of register R to 0's and then replaces the updated instruction address with the effective address. Instruction execution proceeds with the instruction pointed to by the effective address of the BAL instruction.

Affected: (R), (IA)

$IA \longrightarrow R_{15-31}$; $0 \longrightarrow R_{0-14}$; $EA_{15-31} \longrightarrow IA$

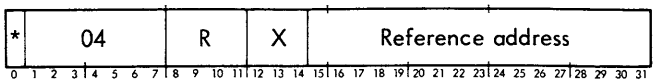
If the effective address of BAL is a nonexistent memory address, the computer aborts execution of the BAL instruction (after loading the updated instruction address into register R) and traps to location X'40'. In this case, the instruction address stored by the XPSD instruction in location X'40' is the address of the BAL instruction.

CALL INSTRUCTIONS

The four CALL instructions each cause the computer to trap to a specific location for the next instruction in sequence.

Each of these four trap locations must contain an EXCHANGE PROGRAM STATUS DOUBLEWORD (XPSD) instruction. Execution of XPSD in the trap location for a CALL instruction is descibed on page 57. If the XPSD instruction is coded with bit position 9 set to 1, the next instruction (executed after the XPSD) is taken from one of 16 possible locations, as designated by the value in the R field of the CALL instruction. Each of the 16 locations may contain an instruction that causes the computer to branch to a specific routine; thus the four CALL instructions can be used to enter any of as may as 64 unique routines

CAL1 CALL 1
(Word addressing)

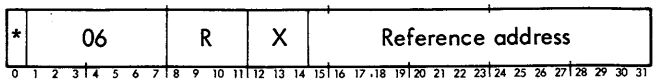


CALL 1 causes the computer to trap to location X'48'.

CAL2 CALL 2
(Word addressing)

CALL 2 causes the computer to trap to location X'49'.

CAL3 CALL 3
(Word addressing)



CALL 3 causes the computer to trap to location X'4A'.

CAL4 CALL 4
(Word addressing)

CALL 4 causes the computer to trap to location X'4B'.

CONTROL INSTRUCTIONS

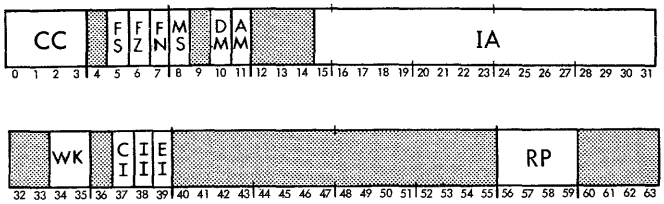
The following privileged instructions are used to control the basic operating conditions of the SIGMA 5 computer:

Instruction Name	Mnemonic	Page
Load Program Status Doubleword	LPSD	56
Exchange Program Status Doubleword	XPSD	56
Load Register Pointer	LRP	58
Move to Memory Control	MMC	58
Wait	WAIT	59
Read Direct	RD	59
Write Direct	WD	60

If execution of any control instruction is attempted while the computer is in the slave mode (i.e., while bit 8 of the current program status doubleword is a 1), the computer unconditionally aborts execution of the instruction (at the time of operation code decoding) and traps to location X'40'.

PROGRAM STATUS DOUBLEWORD

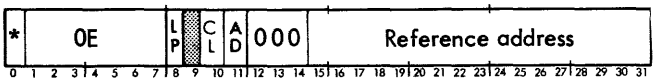
The SIGMA 5 program status doubleword has the following structure when stored in memory:



Bit Position	Designation	Function
0-3	CC	Condition code
5	FS	Floating significance mask
6	FZ	Floating zero mask
7	FN	Floating normalize mask
8	MS	Master/slave mode control
10[t]	DM	Decimal fault trap mask
11	AM	Fixed-point arithmetic overflow trap mask
15-31	IA	Instruction address
34, 35	WK	Write key
37	CI	Counter interrupt group inhibit
38	II	I/O interrupt group inhibit
39	EI	External interrupt inhibit
54-59	RP	Register pointer

The detailed functions of the various portions of the SIGMA 5 program status doubleword are described on page 12.

LPSD LOAD PROGRAM STATUS DOUBLEWORD
(Doubleword addressing, privileged)



LOAD PROGRAM STATUS DOUBLEWORD replaces bits 0 through 39 of the current program status doubleword with bits 0 through 39 of the effective doubleword. The following conditional operations are also performed:

1. If bit position 8 (LP) of LPSD contains a 1, bits 56 through 59 of the current program status doubleword (register pointer) are replaced by bits 56 through 59 of the effective doubleword; if bit 8 of LPSD is a 0, the current register pointer value remains unchanged.

[t]This bit position is used only to preserve the status of the decimal arithmetic fault trap mask when a SIGMA 7 program is being executed. The decimal trap mask bit does not affect the operation of the SIGMA 5 computer in any way.

2. If bit position 10 of LPSD contains a 1, the highest-priority interrupt level currently in the active state is cleared (i.e., reset to either the armed or disarmed state). The interrupt level is armed if bit 11 of LPSD is a 1, or is disarmed if bit 11 of LPSD is a 0. If bit 10 of LPSD is a 0, no interrupt level is affected in any way, regardless of whether bit 11 of LPSD is 1 or 0. (Interrupt levels are described in detail on page 15.)

Those portions of the effective doubleword that correspond to undefined fields in the program status doubleword are ignored.

Affected: (PSD), interrupt system if $(I)_{10} = 1$

$ED_{0-3} \rightarrow$ CC

$ED_{5-7} \rightarrow$ FS, FZ, FN

$ED_{8} \rightarrow$ MS

$ED_{10} \rightarrow$ DM; $ED_{11} \rightarrow$ AM

$ED_{15-31} \rightarrow$ IA

$ED_{34-35} \rightarrow$ WK

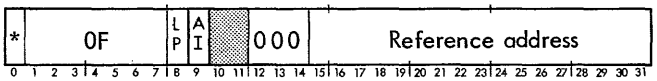
$ED_{37-39} \rightarrow$ CI, II, EI

If $(I)_8 = 1$, $ED_{56-59} \rightarrow$ RP

If $(I)_{10} = 1$ and $(I)_{11} = 1$, clear and arm interrupt

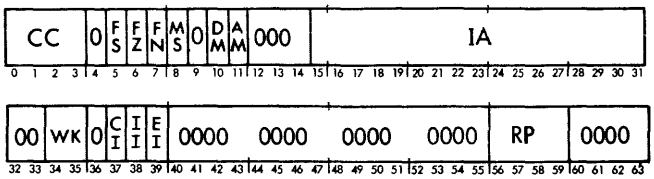
If $(I)_{10} = 1$ and $(I)_{11} = 0$, clear and disarm interrupt

XPSD EXCHANGE PROGRAM STATUS DOUBLEWORD
(Doubleword addressing, privileged)



EXCHANGE PROGRAM STATUS DOUBLEWORD stores the entire current program status doubleword and then replaces the current program status doubleword with a new program status doubleword.

The current program status doubleword is stored in the doubleword location pointed to by the effective address of XPSD in the following form:



The current program status doubleword is replaced by a new program status doubleword as follows:

1. The effective address of XPSD is incremented by 2, so that it points to the next doubleword location. The contents of the next doubleword location are referred to as the second effective doubleword, or ED2.

2. Bits 0 through 35 of the current program status doubleword are unconditionally replaced by bits 0 through 35

of the second effective doubleword. The affected portions of the program status doubleword are:

Bit Position	Designation	Function
0-3	CC	Condition code
5-7	FS, FZ, FN	Floating control
8	MS	Master/slave mode control
10	DM	Decimal trap mask
11	AM	Fixed-point arithmetic trap mask
15-31	IA	Instruction address
34-35	WK	Write key

3. A logical inclusive OR is performed between bits 37 through 39 of the current program status doubleword and bits 37 through 39 of the second effective doubleword.

Bit Position	Designation	Function
37	CI	Counter interrupt inhibit
38	II	I/O interrupt inhibit
39	EI	External interrupt inhibit

If any (or all) of bits 37, 38, or 39 of the second effective doubleword are 0's, the corresponding bits in the current program status doubleword remain unchanged; if any (or all) of bits 37, 38, or 39 of the second effective doubleword are 1's, the corresponding bits in the current program status doubleword are set to 1's. See page 15 for a detailed discussion of the interrupt inhibits.

4. If bit position 8 (LP) of XPSD contains a 1, bits 56-59 of the current program status doubleword (register pointer) are replaced by bits 56 through 59 of the second effective doubleword; if bit 8 of XPSD is a 0, the current register pointer value remains unchanged.

The following additional operations are performed on the new program status doubleword if, and only if, the XPSD is being executed as the result of a nonallowed operation (trap to location X'40') or a CALL instruction (trap to location X'48', X'49', X'4A', or X'4B'):

1. Nonallowed operations – the following additional functions are performed when XPSD is being exeucted as a result of a trap to location X'40':

   a. Nonexistent instruction – if the reason for the trap condition is an attempt to execute a nonexistent instruction, bit position 0 of the new program status doubleword (CC1) is set to 1. Then, if bit 9 (AI) of XPSD is a 1, bit positions 15-31 of the new program status doubleword (next instruction address) are incremented by 8.

   b. Nonexistent memory address – if the reason for the trap condition is an attempt to access or write into a nonexistent memory region, bit position 1 of the new program status doubleword (CC2) is set to 1. Then, if bit 9 of XPSD is a 1, the instruction address portion of the new program status doubleword is incremented by 4.

   c. Privileged instruction violation – if the reason for the trap condition is an attempt to execute a privileged instruction while the computer is in the slave mode, bit position 2 of the new program status doubleword (CC3) is set to 1. Then, if bit position 9 of XPSD is a 1, the instruction address portion of the new program status doubleword is incremented by 2.

   d. Memory protection violation – if the reason for the trap condition is an attempt to write into a memory region to which the program does not have proper access, bit position 3 of the new program status doubleword (CC4) is set to 1. Then, if bit 9 of XPSD is a 1, the instruction address portion of the new program status doubleword is incremented by 1.

   There are certain circumstances under which two of the above nonallowed operations can occur simultaneously. The following operation codes (including their indirect counterparts) are considered to be both nonexistent and privileged: X'0C', X'0D', X'2C', and X'2D'. If any of these operation codes is used as an instruction while the computer is in the slave mode, CC1 and CC3 are both set to 1's; if bit 9 of XPSD is a 1, the instruction address portion of the new program status doubleword is incremented by 10. If an attempt is made to write into a memory region that is both nonexistent and protected from the program by means of the memory protection feature, CC2 and CC4 are both set to 1's; if bit 9 of XPSD is a 1, the instruction address of the new program status doubleword is incremented by 5.

2. CALL instructions – the following additional functions are performed when XPSD is being executed as a resule of a trap to location X'48', X'49', X'4A', or X'4B':

   a. The R field (contents of bit positions 8-11) of the CALL instruction causing the trap is logically inclusively ORed into bit positions 0-3 (CC) of the new program status doubleword.

   b. If bit position 9 of XPSD contains a 1, the R field of the CALL instruction causing the trap is added to the instruction address portion of the new program status doubleword.

If bit position 9 of XPSD contains a 0, the instruction address portion of the new program status doubleword always remains at the value established by the second effective doubleword. Bit position 9 of XPSD is effective only if the instruction is being executed as the result of a nonallowed operation trap or a CALL instruction trap. Bit position 9 of XPSD must be coded with a 0 in all other cases; otherwise, the results of the XPSD instruction are undefined.

Affected: (EDL), (PSD)

PSD → EDL

$ED2_{0-3}$ → CC; $ED2_{5-7}$ → FS, FZ, FN

$ED2_{8}$ → MS; $ED2_{10}$ → DM; $ED2_{11}$ → AM

$ED2_{15-31}$ → IA; $ED2_{34-35}$ → WK

$ED2_{37-39}$ u CI, II, EI → CI, II, EI

If $(I)_8 = 1$, $ED2_{56-59}$ → RP

If $(I)_8 = 0$, RP not affected

If nonexistent instruction, 1 → CC1 then, if $(I)_9 = 1$, IA + 8 → IA

If nonexistent memory address, 1 → CC2 then, if $(I)_9 = 1$, IA + 4 → IA

If privileged instruction violation, 1 → CC3 then, if $(I)_9 = 1$, IA + 2 → IA

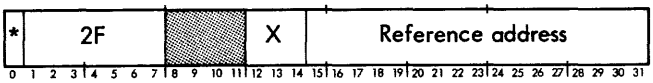
If memory protection violation, 1 → CC4 then, if $(I)_9 = 1$, IA + 1 → IA

If CALL instruction, CC u $CALL_{8-11}$ → CC then,

if $(I)_9 = 1$, IA + $CALL_{8-11}$ → IA

if $(I)_9 = 0$, IA not affected

LRP LOAD REGISTER POINTER
(Word addressing, privileged)

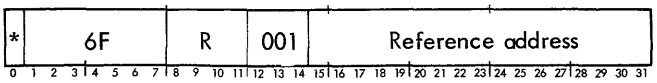


LOAD REGISTER POINTER loads bits 24 through 27 of the effective word into the register pointer (RP) portion of the current program status doubleword. Bits positions 0 through 23 and 28 through 31 of the effective word are ignored, and no other portion of the program status doubleword is affected. If the register pointer is loaded with a value that points to a nonexistent block of general registers, the computer subsequently generates either all 1's or all 0's as the contents of the nonexistent block of general registers whenever an instruction designates a general register by means of the R field of the reference address field.

Affected: RP

EW_{24-27} → RP

MMC MOVE TO MEMORY CONTROL
(Word addressing, privileged, continue after interrupt)



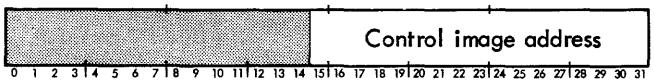
MOVE TO MEMORY CONTROL loads a string of one or more words into the memory control registers (memory control registers are described on page 12). Bit positions 12-14 of MMC are not used as an index register address; instead, they are used to specify that memory control registers are to be loaded. Bit positions 12-14 of MMC must be coded as 001, in order to load the memory control storage.

If bit positions 12-14 of MMC are not coded as 001, the instruction produces an undefined result. Also, if an attempt is made to load unimplemented memory control storage, the contents of the general registers specified by the MMC instruction are undefined at the completion of the instruction.

Bit positions 15-31 (reference address field) of MMC are ignored insofar as the operation of the instruction is concerned, and the results of the instruction are the same whether or not MMC is indirectly addressed. However, if MMC is indirectly addressed and the indirect reference address is nonexistent, the nonallowed operation trap (location X'40') is activated. The effective address of the MMC instruction however, is not used as a memory reference (thus does not affect the normal operation of the instruction).

The R field of MMC designates an even-odd pair of general registers (R and Ru1) that are used to control the loading of the memory control registers. Registers R and Ru1 are assumed to contain the following information:

Register R:



Register Ru1:

Bit positions 15 through 31 of register R contain the address of the first word of the control image to be loaded into the memory control registers. Bit positions 0 through 7 of register Ru1 contain a count of the number of words to be loaded. If bits 0-7 of register Ru1 are initially all 0's a word count of 256 is implied.

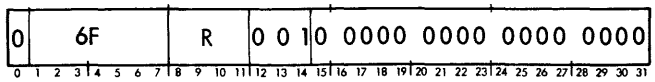
Bit positions 15 through 20 of register Ru1 point to the beginning of the memory region controlled by the registers to be loaded.

The R field of the MMC instruction must be an even value for proper operation of the instruction; if the R field of MMC is an odd value, the operation of the instruction is undefined.

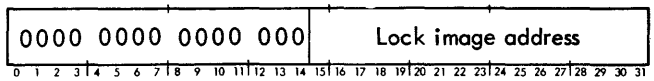
LOADING THE MEMORY WRITE PROTECTION LOCKS

The following diagrams represent the configuration of MMC, register R, and register Ru1 that are required to load the memory write-protection locks:

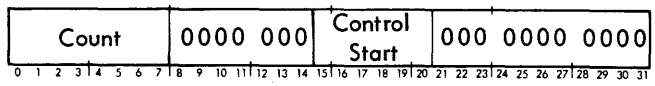
The instruction format is



The contents of register R are

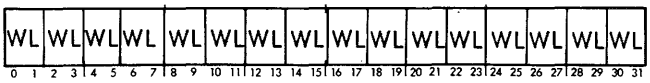


The contents of register Ru1 are



Memory Lock Control Image

The initial address value in register R is the address of the first word of the memory lock control image, and word length of the image is specified in the initial count in register Ru1. A word count of 16 is sufficient to load the entire block of memory locks. The memory lock registers are treated as a circular set, with the register for memory addresses 0 through X'1FF' immediately following the register for memory addresses X'1FFE00' through X'1FFFFF'; thus, a word count greater than 16 causes the first registers loaded to be overwritten. Each word of the lock image is assumed to be in the following format:



Memory Lock Loading Process

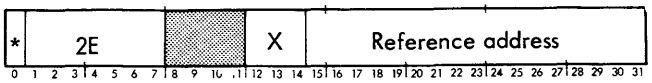
Bit positions 15-20 of register Ru1 initially point to the first 512-word page of core memory addresses that are to be controlled by the memory lock image. MMC moves the lock image into the lock registers 1 word at a time, thus loading the locks for 16 consecutive 512-word pages with each image word. As each word is loaded, the address of the lock image is incremented by 1, the word count is decremented by 1, and the value in bit positions 15-20 of register Ru1 is incremented by 4; this process continues until the word count is reduced to 0. When the loading process is completed, register R contains a value equal to the sum of the initial lock image address plus the initial word count. Also, the final word count is 0, and bit positions 15-20 of register Ru1 contain a value equal to the sum of the initial contents plus 4 times the initial word count.

INTERRUPTION OF MMC

The execution of MMC can be interrupted after each word of the control image has been moved into the specified control register. Immediately prior to the time that the instruction in the interrupt (or trap) location is executed, register R contains the address of the next word of the control image to be loaded, and register Ru1 contains a count of the number of control image words remaining to be moved and a value pointing to the next memory control register to be loaded.

Affected: (R), (Ru1), memory control registers

WAIT WAIT
(Word addressing, privileged)

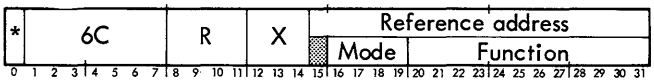


WAIT causes the central processing unit (CPU) of the SIGMA 5 system to cease all operations until an interrupt activation occurs, or until the computer operator manually moves the COMPUTE switch (on the processor control panel) from the RUN position to IDLE and then back to RUN. The instruction address portion of the program status doubleword is updated before the computer begins waiting; therefore, while the CPU is waiting, the program status doubleword contains the address of the next location in ascending sequence after WAIT and the contents of the next location are displayed in the DISPLAY indicators on the processor control panel (see Chapter 5). If any input/output operations are being performed when WAIT is executed, the operations proceed to their normal termination.

When an interrupt activation occurs while the CPU is waiting, the computer processes the interrupt-servicing routine. Normally, the interrupt-servicing routine begins with an XPSD instruction in the interrupt location, and ends with an LPSD instruction at the end of the routine. After the LPSD instruction is executed, the next instruction to be executed in the interrupted program is the next instruction in sequence after the WAIT instruction. If the interrupt is to a single-instruction interrupt location, the instruction in the interrupt location is executed and then instruction execution proceeds with the next instruction in sequence after the WAIT instruction. When the COMPUTE switch is moved from RUN to IDLE and back to RUN while the CPU is waiting, instruction execution proceeds with the next instruction in sequence after the WAIT instruction.

If WAIT is indirectly addressed and the indirect reference address is nonexistent, the nonallowed operation trap (location X'40') is activated. The effective address of the WAIT instruction, however, is not used as a memory reference (thus does not affect the normal operation of the instruction.

RD READ DIRECT
(Word addressing, privileged)



The CPU is capable of directly communicating with other elements of the SIGMA 5 system, as well as performing internal control operations, by means of the READ DIRECT/WRITE DIRECT (RD/WD) lines. The RD/WD lines consist of 16 address lines, 32 data lines, 2 condition code lines, and various control lines that are connected to various CPU circuits and to special systems equipment.

READ DIRECT causes the CPU to present bits 16 through 31 of the effective address to other elements of the SIGMA 5 system on the RD/WD address lines. Bits 16-31 of the effective address identify a specific element of the SIGMA 5 system that is expected to return information (2 condition code bits plus a maximum of 32 data bits) to the CPU. The significance and number of data bits returned to the CPU depend on the selected element. If the R field of RD is nonzero, up to 32 bits of the returned data are loaded into general register R; however, if the R field of RD is 0, the returned data is ignored and general register 0 is not changed. Bits CC3 and CC4 of the condition code are set by the addressed element, regardless of the value of the R field . (CC1 and CC2 are also set when the RD instruction is coded for the internal control mode.)

Bits 16-19 of the effective address of RD determine the mode of the RD instruction, as follows:

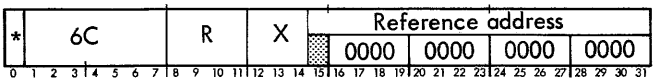
Bit position 16	17	18	19	Mode
0	0	0	0	Internal computer control
0	0	0	1	Unassigned
0	0	1	0	SDS testers
0	0	1	1	Assigned to various groups of standard SDS products
:	:	:	:	
1	1	1	0	
1	1	1	1	Special systems control (for customer use with specially designed equipment)

READ DIRECT, INTERNAL COMPUTER CONTROL (MODE 0)

In this mode, the condition code portion of the program status doubleword is unconditionally set according to the states of the four SENSE switches on the processor control panel. If a particular SENSE switch is set, the corresponding bit of the condition code is set to 1; if a SENSE switch is reset, the corresponding bit of the condition code is reset to 0.

Read SENSE Switches

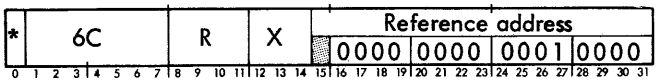
The following configuration of RD can be used to read the control panel SENSE switches:



In this case, only the condition code is affected.

Read MEMORY FAULT Indicators

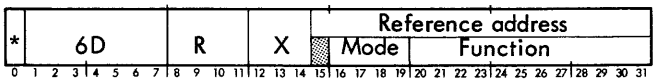
Each core memory module is associated with a MEMORY FAULT indicator that is turned on whenever a memory parity or overtemperature condition occurs. The following configuration of RD is used to record and reset the MEMORY FAULT indicators.



If the R field of RD is nonzero, bit positions 0-23 of register R are reset to all 0's, and bit positions 24-31 are set according to the current states of the MEMORY FAULT indicators; then all MEMORY FAULT indicators are reset. If a bit position in register R is set to 1, a memory fault has been detected in the corresponding core memory module. If the R field of RD is zero, the MEMORY FAULT indicators and the contents of register 0 remain unchanged (although the condition code is still set to the value of the SENSE switches). The MEMORY FAULT indicators are also reset by means of the SYS RESET/CLEAR switch on the processor control panel.

Affected: (R), CC, MEMORY FAULT indicators

WD WRITE DIRECT
(Word addressing, privileged)



WRITE DIRECT causes the CPU to present bits 16 through 31 of the effective address to other elements of the SIGMA 5 system on the RD/WD address lines (see READ DIRECT). Bits 16-31 of the effective address identify a specific element of the SIGMA 5 system that is to receive control information from the CPU. If the R field of WD is nonzero, the 32-bit contents of register R are transmitted to the specified element on the RD/WD data lines. If the R field of WD is 0, 32 0's are transmitted to the specified element (instead of the contents of register 0). The specified element may return information to set the condition code.

Bits 16-19 of the effective address determine the mode of the WD instruction, as follows:

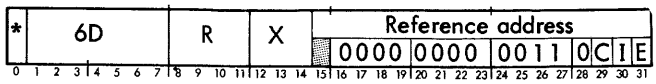
Bit position 16	17	18	19	Mode
0	0	0	0	Internal computer control
0	0	0	1	Interrupt control
0	0	1	0	SDS testers
0	0	1	1	Assigned to various groups of standard SDS products
:	:	:	:	
1	1	1	0	
1	1	1	1	Special systems control (for customer use with specially designed equipment)

WRITE DIRECT, INTERNAL COMPUTER CONTROL (MODE 0)

In this mode, the condition code portion of the program status doubleword (PSD_{0-3}) is unconditionally set according to the states of the four SENSE switches on the processor control panel. If a particular SENSE switch is set, the corresponding bit of the condition code is set to 1; if a SENSE switch is reset, the corresponding bit of the condition code is reset to 0.

Set Interrupt Inhibits

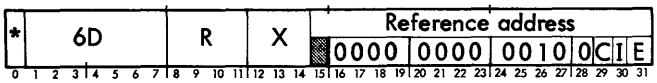
The following configuration of WD can be used to set the interrupt inhibits (bits 37-39 of the program status doubleword):



A logical inclusive OR is performed between bits 29-31 of the effective address and bits 37-39 of the program status doubleword. If any (or all of bits 29-31) of the effective address are 1's, the corresponding inhibit bits in the program status doubleword are set to 1's; the current state of an inhibit bit is not affected if a corresponding bit position of the effective address contains a 0.

Reset Interrupt Inhibits

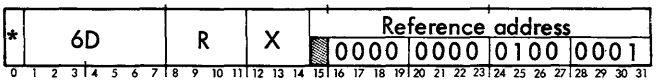
The following configuration of WD can be used to reset the interrupt inhibits:



If any (or all) of bits 29-31 of the effective address are 1's, the corresponding inhibit bits in the program status doubleword are reset to 0's; the current state of an inhibit bit is not affected if a corresponding bit position of the effective address contains a 0.

Set ALARM Indicator

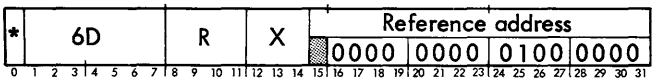
The following configuration of WD is used to set the ALARM indicator on the maintenance section of the processor control panel:



If the COMPUTE switch on the processor control panel is in the RUN position and the AUDIO switch on the maintenance section of the processor control panel in in the ON position, a 1000-Hz signal is transmitted to the computer speaker. The signal may be interrupted by moving the COMPUTE switch to the IDLE position, by moving the AUDIO switch to the OFF position, or by resetting the ALARM indicator.

Reset ALARM Indicator

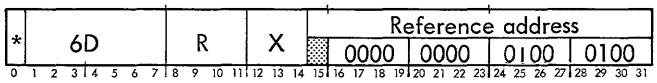
The following configuration of WD is used to reset the ALARM indicator:



The ALARM indicator is also reset by means of either the CPU RESET/CLEAR switch or the SYSTEM RESET/CLEAR switch on the processor control panel.

Reset Integral IOP Inhibit

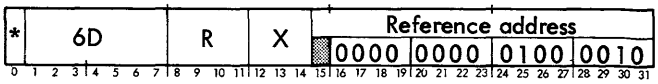
If the integral IOP is operating when the instruction watchdog timer runout trap is activated, the integral IOP is inhibited from further operation until the integral IOP inhibit is reset. The following configuration of WD is used to reset the integral IOP inhibit:



The integral IOP inhibit is also reset by means of the CPU RESET/CLEAR switch or the SYS RESET/CLEAR switch on the processor control panel.

Toggle Program-Controlled-Frequency Flip-Flop

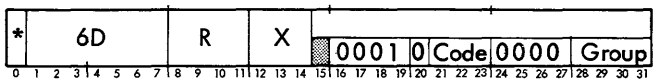
The following configuration of WD is used to "toggle" the CPU program-controlled-frequency (PCF) flip-flop:



The output of the PCF flip-flop is transmitted to the computer speaker through the AUDIO switch on the maintenance section of the processor control panel. If the PCF flip-flop is reset when the above configuration of WD is executed, the WD instruction sets the PCF flip-flop, if the PCF flip-flop was previously set, the WD instruction resets it. A program can thus generate a desired frequency by toggling (setting and resetting) the PCF flip-flop at the appropriate rate. Execution of the above configuration of WD also resets the ALARM indicator.

WRITE DIRECT, INTERRUPT CONTROL (MODE 1)

The following configuration of WD is used to control the alteration of the various states of the individual interrupt levels within the CPU interrupt system:



Bits 28 through 31 of the effective address specify the identification number (see page 14) of the group of interrupt levels to be controlled by the WD instruction.

The R field of the WD instruction specifies a general register that contains the selection bits for the individual interrupt levels within the specified group. Bit position 16 of register R contains the selection bit for the highest-priority (lowest numbered) interrupt level within the group, and bit position 31 of register R contains the selection bit for the lowest-priority (highest-numbered) interrupt level within the group. Each interrupt level in the designated group is operated on according to the function code specified by bits 21 through 23 of the effective address of WD. The codes and their associated functions are as follows:

Code	Function
000	Undefined
001	Disarm all levels selected by a 1; all levels selected by a 0 are not affected.
010	Arm and enable all levels selected by a 1; all levels selected by a 0 are not affected.
011	Arm and disable all levels selected by a 1; all levels selected by a 0 are not affected.
100	Enable all levels selected by a 1; all levels selected by a 0 are not affected.
101	Disable all levels selected by a 1; all levels selected by a 0 are not affected.
110	Enable all levels selected by a 1 and disable all levels selected by a 0.

Code	Function
111	Trigger all levels selected by a 1. All such levels that are currently armed advance to the waiting state. Those levels currently disarmed are not altered, and all levels selected by a 0 are not affected. The interrupt trigger is applied at the same input point as that used by the device connected to the interrupt level.

INPUT/OUTPUT INSTRUCTIONS

"Standard" SIGMA 5 I/O refers to the normal I/O system consisting of input/output processors, device controllers, and devices. This system handles normal communication with standard peripherals such as printers, discs, tapes, and so forth. When dealing with standard I/O operations, the CPU uses the following five instructions:

Instruction Name	Mnemonic	Page
Start Input/Output	SIO	63
Halt Input/Output	HIO	66
Test Input/Output	TIO	66
Test Device	TDV	67
Acknowledge Input/Output Interrupt	AIO	67

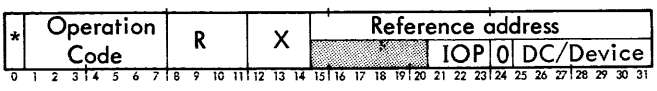
If execution of any input/output instruction is attempted while the computer is in the slave mode (i.e., while bit 8 of the current program status doubleword is a 1), the computer unconditionally aborts execution of the instruction (at the time of operation code decoding) and traps to location X'40'.

I/O ADDRESSES

The device to be operated on by an I/O instruction is selected by the effective address of the I/O instruction itself. Indirect addressing and/or indexing are performed, as for other word-addressing instructions, to compute the effective address of the I/O instruction. However, the effective address is not used as a memory reference (i.e., not subject to memory protection). For the SIO, HIO, TIO, and TDV instructions, the 11 low-order bits of the effective address constitute an I/O address. For the AIO instruction, the device causing the interrupt returns its 11-bit I/O address as part of the response to the AIO instruction.

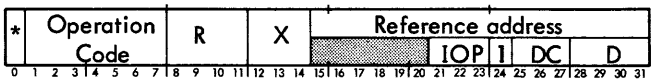
An I/O address occupies bit positions 21 through 31 of the effective address, with bits 21, 22, and 23 of the I/O address specifying one of eight possible IOPs that can be controlled by a CPU. The remainder of the I/O address is factored into one of two forms, depending on bit 24, as follows:

Case I: Single-unit device controllers (bit 24 is 0)



Bits 25 through 31 of the I/O address (DC/Device) constitute a single code specifying a particular combination of device controller and device. Normally, these codes refer to device controllers that drive only a single device, such as card readers, card punches, line printers, etc.

Case II: Multiunit device controllers (bit 24 is 1)



Bits positions 25 through 31 of the I/O address contain a 3-bit device controller code (DC) in bit positions 25-27 and a 4-bit device code (Device) in bit positions 28-31. This form of I/O address is used for device controllers (such as magnetic tape and rapid access data file controllers) that control information exchange with only one device at a time (out of a set of as many as 16 devices).

I/O UNIT ADDRESS ASSIGNMENT

Device controller numbers are normally assigned to a multiplexor IOP in numerical sequence, beginning with zero and continuing through the highest number recognized by the IOP (i.e., X'7', X'F', X'17', or X'1F'). In the case of multiunit device controllers, the device controller number must be in the range X'0' through X'7' because the I/O address field structure allows for a 3-bit multiunit device controller number. In the case of single-unit device controllers, any of the available numbers in the range X'0' through X'1F' maybe assigned to the device controller, providing that the same number has not already been assigned to a multiunit device controller. For example, if device controller number X'0' is assigned to a magnetic tape unit controller, the number X'0' cannot also be used for a card reader (although the coding of the I/O address field would be different in bit position 24). The I/O address codes used by standard SDS software are

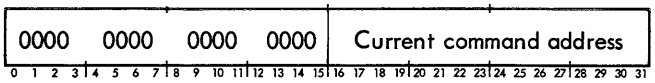
I/O address	Peripheral device designation
X'080'	IOP 0, device controller 0, magnetic tape unit 0
X'081'	IOP 0, device controller 0, magnetic tape unit 1
⋮	⋮
X'087'	IOP 0, device controller 0, magnetic tape unit 7
X'001'	IOP 0, device controller 1, keyboard/printer
X'002'	IOP 0, device controller 2, line printer
X'003'	IOP 0, device controller 3, card reader
X'004'	IOP 0, device controller 4, card punch
X'005'	IOP 0, device controller 5, paper tape reader/punch

I/O STATUS RESPONSE

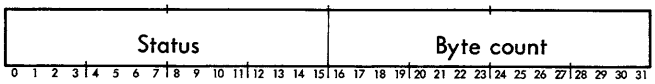
All I/O instructions result in the setting of condition code CC1 and CC2 to denote the nature of the I/O response. The R field of the I/O instruction specifies one of the gen-

eral registers that is to accept additional I/O response information during the execution of an I/O instruction. In some situations, the programmer may want two sets of response information loaded into the general registers, while in other situations he may want only one set, or even no information loaded into a general register. This control is achieved by coding the R field of the I/O instruction. One set of response information is loaded into register R and another set may be loaded into register Ru1. If the R field is an even, nonzero number, registers R and R + 1 are each loaded with response information. If the R field specifies an odd-numbered general register, then only register R is loaded with response information. However, if the R field is 0 or if the I/O address is not recognized by the I/O system, or if the device controller is attached to a "busy" selector IOP, no general registers are loaded with response information. The I/O response information loaded into the general register for SIO, HIO, TIO and TDV instructions is in the following format:

Word into register R



Word into register Ru1



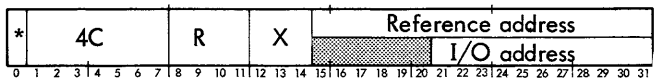
Current Command Doubleword Address. After the addressed device has received an order, this field contains the 16 high-order bits of the core memory address for the command doubleword (see page 70) currently being processed for the addressed device.

Status. The meaning of this field depends on the particular I/O instruction being executed and upon the selected I/O device (see Table 8).

Byte Count. After the addressed device has received an order, this field contains a count of the number of bytes yet to be transmitted by the operation called for by the order.

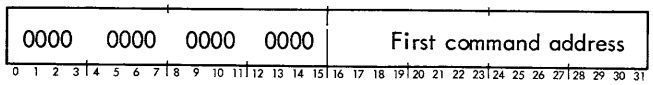
The format of I/O response information loaded into register R for the instruction AIO is described on page 68.

SIO START INPUT/OUTPUT
(Word addressing, privileged)



START INPUT/OUTPUT is used to initiate an input or output operation with the device selected by the I/O address (bits 21-31 of the effective address of the instruction).

SIO utilizes data in general register 0, which is assumed to have the following content when SIO is executed.



General register 0 is temporarily dedicated during the execution of an SIO instruction to specify the starting doubleword address for the IOP command list. The doubleword address in register 0 is the 16 high-order bits of a memory address; thus, the address in register 0 always specifies an even-numbered word location. (The IOP command list is described in "IOP Command Doublewords", Chapter 4.)

If I/O address recognition exists in the I/O system, the first command doubleword address is loaded into the IOP command address counter associated with the device controller specified by the I/O address of the SIO instruction. If, at this time, the device is in the "ready" condition and the device does not have an interrupt condition pending, the device is started (i.e., advanced to the "busy" condition). Then, if the device is in the "automatic" mode, it requests an order from the IOP. The IOP loads the first command doubleword of the I/O command list into its appropriate registers and transmits the order to the device.

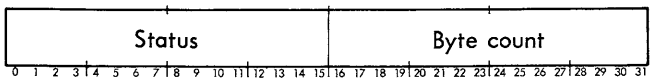
The CPU condition code provides an indication of whether or not the I/O address specified by the SIO instruction was recognized by the I/O system and whether the SIO instruction was or was not accepted by the device (i.e., whether the device did or did not advance to the "busy" condition).

The condition code settings for SIO are:

1	2	3	4	Result
0	0	-	-	I/O address recognized and SIO accepted
0	1	-	-	I/O address recognized but SIO not accepted
1	0	-	-	device controller is attached to a "busy" selector IOP
1	1	-	-	I/O address not recognized

STATUS INFORMATION FOR SIO

In the event that the SIO instruction was not accepted (i.e., CC1 = 0 and CC2 = 1), the status information returned as a part of the I/O response provides indications of why the SIO instruction was not accepted. If the SIO instruction has been coded with an R field value of 0, or if the I/O address is not recognized by the I/O system, or if the device controller is attached to a "busy" selector IOP, only the condition code settings are available. If the R field value is odd, register R contains the following information:



Bit Position	Function
0	Device interrupt pending: if this bit is 1, the addressed device has requested an interrupt and the interrupt has not been acknowledged by an AIO instruction. Device interrupts can be achieved by coding of the flag portion of the I/O command doubleword. Device interrupts can also be achieved by using M modifiers in the basic order to the device (M bits in the Order portion of the

Table 8. Status Bits for I/O Instructions

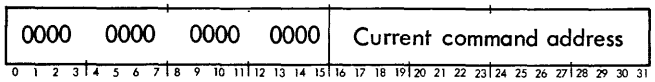
Position and State in Register Ru1																Meaning (SIO, HIO, TIO)	Meaning (TDV)
Device Status Byte								Operational Status Byte									
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	device interrupt pending	data overrun
-	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	device ready	unique to the device and the device controller
-	0	1	-	-	-	-	-	-	-	-	-	-	-	-	-	device not operational	
-	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	device unavailable	
-	1	1	-	-	-	-	-	-	-	-	-	-	-	-	-	device busy	
-	-	-	0	-	-	-	-	-	-	-	-	-	-	-	-	device manual	
-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	device automatic	
-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	device unusual end	
-	-	-	-	-	0	0	-	-	-	-	-	-	-	-	-	device controller ready	
-	-	-	-	-	0	1	-	-	-	-	-	-	-	-	-	device controller not operational	
-	-	-	-	-	1	0	-	-	-	-	-	-	-	-	-	device controller unavailable	
-	-	-	-	-	1	1	-	-	-	-	-	-	-	-	-	device controller busy	
-	-	-	-	-	-	-	0	-	-	-	-	-	-	-	-	unassigned	
-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	incorrect length	same as for SIO, HIO, and TIO
-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	transmission data error	
-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	transmission memory error	
-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	memory address error	
-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	IOP memory error	
-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	IOP control error	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	IOP halt	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	Selector IOP busy	

Position and State in Register R																Meaning (AIO)
Device Status Byte								Operational Status Byte								
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	data overrun
-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	unique to the device and the device controller
-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	
-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	
-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	
-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	
-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	
-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	
-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	incorrect length
-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	transmission data error
-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	zero byte count interrupt
-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	channel end interrupt
-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	unusual end interrupt
-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	unassigned
-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	

Bit Position	Function
	command doubleword). In either case, the device will not accept a new SIO instruction until the interrupt-pending condition is cleared (i.e., the condition code settings for the SIO instruction will indicate "SIO not accepted" if the interrupt-pending condition is present in the addressed device).
1,2	Device condition: if bits 1 and 2 are 00 (device "ready"), all device conditions required for proper operation are satisfied. If bits 1 and 2 are 01 (device "not operational"), the addressed device has developed some condition that will not allow it to proceed; in either case, operator intervention is usually required. If bits 1 and 2 are 10 (device "unavailable"), the device has more than one channel of communication available and it is engaged in an operation controlled by an IOP other than the one specified by the I/O address. If bits 1 and 2 are 11 (device "busy"), the device has accepted a previous SIO instruction and is already engaged in an I/O operation.
3	Device mode: if this bit is 1, the device is in the "automatic" mode; if this bit is 0, the device is in the "manual"mode and requires operator intervention. This bit can be used in conjunction with bits 1 and 2 to determine the type of action required. For example, assume that a card reader is able to operate, but no cards are in the hopper. The card reader would be in state 000 (device "ready", but manual intervention required), where the state is indicated by bits 1, 2, and 3 of the I/O status response. If the operator subsequently loads the card hopper and presses the card reader START switch, the reader would advance to state 001 (device "ready" and in automatic operation). If the card reader is in state 000 when an SIO instruction is executed, the SIO would be accepted by the reader and the reader would advance to state 110 (device "busy", but operator intervention required). Should the operator then place cards in the hopper and press the START switch, the card reader state would advance to 111 (device "busy" and in automatic operation), and the input operation would proceed. Should the card reader subsequently become empty (or the operator press the STOP switch) and command chaining is being used to read a number of cards, the card reader would return to state 110. If the card reader is in state 001 when an SIO instruction is executed, the reader advances to state 111, and the input operation continues as normal. Should the hopper subsequently become empty (or should the operator press the card reader STOP switch) and command chaining is being used to read a number of cards, the reader would go to state 110 until the operator corrected the situation.
4	Device unusual end occurred during last operation: if this bit is 1, the reason for the indication may be a normal end (such as an end of file) or a fault condition. For a fault condition, the device has halted at other than its normal stopping point. In either case, the device will not automatically request further action from its device controller. The specific details of this indication are a function of the particular device.
5, 6	Device controller condition: if bits 5 and 6 are 00 (device controller "ready"), all device controller conditions required for its proper operation are satisfied. If bits 5 and 6 are 01 (device controller "not operational"), some condition has developed that does not allow it to operate properly. In either case, operator intervention is usually required. If bits 5 and 6 are 10 (device controller "unavailable"), the device controller is currently engaged in an operation controlled by an IOP other than the one addressed by the I/O instruction. If bits 5 and 6 are 11 (device controller "busy"), the device controller has accepted a previous SIO instruction and is currently engaged in performing an operation for the addressed IOP.
7	Unassigned
8	Incorrect length: if this bit is 1, an incorrect length condition has been signaled to the IOP during the previous operation. Incorrect length is caused by a channel end (or end of record) condition occurring before the device controller has received a "count done" signal from the IOP, or is caused by the device controller receiving a count done signal before channel end (or end of record); e.g., count done before 80 columns have been read from a card. Normally, a count done signal is sent to the device controller by the IOP to indicate that the byte count associated with the current operation has been reduced to zero. The IOP is capable of suppressing an error condition on incorrect length, since there are many situations in which incorrect length is a legitimate situation and not a true error condition. Incorrect length is suppressed as an error by coding the SIL flag (a 1 in bit 38) of the IOP command doubleword (see page 72). At the end of the execution of an I/O command list, this status bit is 1 if an incorrect length condition occurred anywhere in the command list, regardless of the coding of the SIL flag.
9	Transmission data error: this bit is set to 1 if the IOP or device controller has detected a parity error or data overrun in the transmitted information.
10	Transmission memory error: this bit is set to 1 if a memory parity error has occurred during a data input/output operation. A parity error is detected on any output operation and on partial-word input operations. A device halt does not occur unless

Bit Position	Function
	The HTE flag in the IOP command doubleword is set to 1 (see page 72).
11	Memory address error: a nonexistent memory address has been encountered on either data or commands. Core memory locations 0 through 15 are not considered nonexistent because the IOP can work with these addresses as normal memory addresses.
12	IOP memory error: if a memory parity error has occurred while the IOP was fetching a command, this bit is set to 1.
13	IOP control error: this bit is set to 1 if the IOP has encountered two successive TRANSFER IN CHANNEL commands.
14	IOP halt: this bit is set to 1 if the IOP has issued a halt order to the addressed I/O device because of an error condition.
15	IOP busy: this bit is set to 1 if a selector IOP is addressed by the I/O instruction and the selector IOP is currently in use by some I/O device operating in conjunction with the selector IOP.
16-31	Byte count: a count of the number of bytes yet to be transmitted in the operation called for by the current command doubleword.

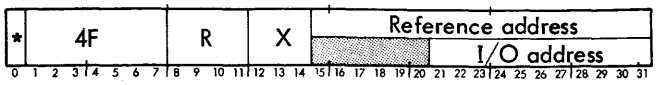
If the R field value of the SIO instruction is even and not 0, the condition code and register R+1 contain the information described above and register R contains the following information:



Bit Position	Function
16-31	Current command doubleword address: the 16 high-order bits of the core memory address from which the command doubleword for the I/O operation currently being processed by the addressed device controller was fetched.

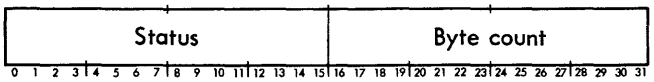
Ordinarily, on an SIO instruction, the programmer has no interest in where the IOP is in executing its command list, and thus will usually code the R field of the SIO instruction to specify an odd-numbered general register, loading only the byte count and status information into the CPU. The condition code is set regardless of the coding of the R field.

HIO HALT INPUT/OUTPUT
(Word addressing, privileged)

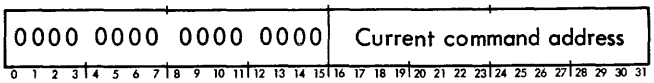


HALT INPUT/OUTPUT causes the addressed device to immediately halt its current operation (perhaps improperly, in the case of magnetic tape units, when the device is forced to stop at other than an interrecord gap). If the device is in an interrupt-pending condition, the condition is cleared.

If the R field of the HIO instruction is 0 or if no I/O address recognition exists, no general registers are affected, but the condition code is set. If the R field is an odd value, the condition code is set and the following information is loaded into register R.



The status information returned for HIO has the same interpretation as that returned for the instruction SIO (see page 64), and shows the I/O status at the time of the halt. The count information shows the number of bytes remaining to be transmitted at the time of the halt. If the R field of HIO is an even value and not 0, the condition code is set, register R+1 is loaded as shown above, and register R contains the following information:



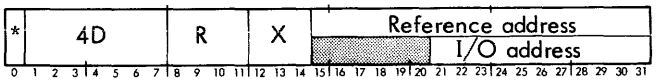
The current command doubleword address has the same interpretation as that for the instruction SIO.

Affected: (R), (Ru1), CC1, CC2

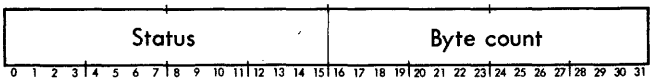
Condition code settings:

1	2	3	4	Result of HIO
0	0	-	-	I/O address recognized and device controller is not "busy"
0	1	-	-	I/O address recognized but device controller was "busy" at the time of the halt
1	1	-	-	I/O address not recognized

TIO TEST INPUT/OUTPUT
(Word addressing, privileged)

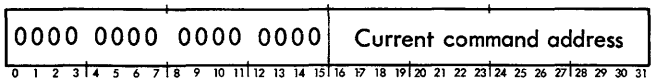


TEST INPUT/OUTPUT is used to make an inquiry on the status of data transmission. The operation of the selected IOP, device controller, and device are not affected, and no operations are initiated or terminated by this instruction. The responses to TIO provide the program with the information necessary to determine the current status of the device, device controller, and IOP, the number of bytes remaining to be transmitted in the operation, and the present point at which the IOP is operating in the command list. If the R field of the TIO instruction is 0 or if the device controller is attached to a "busy" selector IOP, no general registers are affected, but the condition code is set. If the R field of TIO is an odd value, the condition code is set and the I/O status and byte count are loaded into register R as follows:



The status information has the same interpretation as the status information returned for the instruction SIO (see page 64), and shows the I/O status at the time of sampling. The count information shows the number of bytes remaining

to be transmitted at the time of sampling. If the R field of the TIO instruction is an even value and not 0, the condition code is set, register R+1 is loaded as shown above, and register R is loaded as follows:



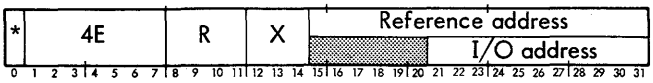
The current command doubleword address has the same interpretation as for the instruction SIO.

Affected: (R), (Ru1), CC1, CC2

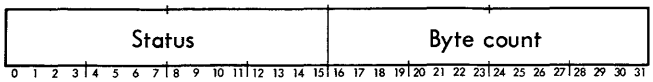
Condition code settings:

1	2	3	4	Result of TIO
0	0	-	-	I/O address recognized and acceptable SIO is currently possible
0	1	-	-	I/O address recognized but acceptable SIO is not currently possible
1	0	-	-	device controller is attached to "busy" selector IOP
1	1	-	-	I/O address not recognized

TDV TEST DEVICE
(Word addressing, privileged)

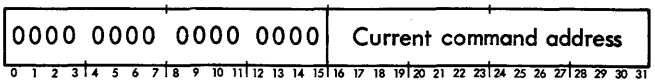


TEST DEVICE is used to provide information about a device other than that obtainable by means of the TIO instruction. The operation of the selected IOP, device controller, and device are not affected, and no operations are initiated or terminated. The responses to TDV provide the program with information giving details on the condition of the selected device, the number of bytes remaining to be transmitted in the current operation, and the present point at which the IOP is operating in the command list. If the R field of the TDV instruction is 0 or if no I/O address recognition exists, or if the device controller is attached to a "busy" selector IOP, the condition code is set, but no general registers are affected. If the R field of TDV is an odd value, the condition code is set and the device status and byte count are loaded into register R as follows:



Bit Position	Function
0	Data overrun: This bit is set to 1 if a data overrun has occurred in the current I/O operation. A data overrun is a situation wherein the device controller is ready to transmit data to the IOP but the IOP has not received the previous data, or the device controller requires data but cannot obtain it from the IOP. In either case, the condition is caused by an equipment malfunction or by the total I/O data rate exceeding system limits.
1-7	Unique to the device.
8-15	Same as for bits 8-15 of the status information for the instruction SIO

The count information shows the number of bytes remaining to be transmitted in the current operation at the time of the TDV instruction. If the value of the R field of TDV is an even value and not 0, the condition code is set, register R+1 is loaded as shown above, and register R is loaded as follows:



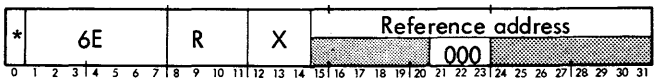
The current command doubleword address has the same interpretation as for the instruction SIO.

Affected: (R), (Ru1), CC1

Condition code settings:

1	2	3	4	Result of TDV
0	0	-	-	I/O address recognized
0	1	-	-	I/O address recognized and device-dependent condition is present
1	0	-	-	device controller is attached to "busy" selector IOP
1	1	-	-	I/O address not recognized

AIO ACKNOWLEDGE INPUT/OUTPUT INTERRUPT
(Word addressing, privileged)



AIO is used to acknowledge an input/output interrupt and to identify what I/O unit is causing the interrupt and why. Bits 21, 22, and 23 of the effective program address of the AIO instruction (the IOP portion of the I/O selection code field) specify the type of interrupt being acknowledged. These bits should be coded 000 to specify the standard I/O system interrupt acknowledgment (other codings of these bits are reserved for use with special I/O systems). The remainder of the I/O selection code field (bit positions 24-31) has no other use in the standard I/O interrupt acknowledgment because the identification of the interrupt source is one of the responses of the standard I/O system to the AIO instruction.

Standard I/O system interrupts can be initiated for the following conditions:

Condition	Interrupt prerequisite†	Status bit set
Zero byte count	IZC = 1	10
Channel end	ICE = 1	11

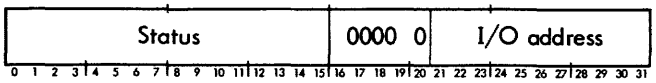
†IZC, ICE, IUE, HTE, and SIL refer to flag bits in the IOP command doublewords (see Chapter 4).

Condition	Interrupt prerequisite[†]	Status bit set
Transmission memory error	IUE = 1, HTE = 1	12
Incorrect length	IUE = 1, HTE = 1 and SIL = 0	8, 12
Memory address error (IOP memory error or IOP control error)	IUE = 1	12
Transmission data error	IUE = 1, HTE = 1	9, 12

When a device interrupt condition occurs, the IOP forwards the request to the CPU interrupt system I/O interrupt level. If this interrupt level is armed, enabled, and not inhibited (see page 16, "Control of the Interrupt System"), the CPU eventually acknowledges the interrupt request and executes the XPSD instruction in core memory location X'5C', which leads to the execution of an AIO instruction.

For the purpose of acknowledging standard I/O interrupts, the IOPs, device controllers, and devices are connected in a preestablished priority sequence that is customer-assigned and is independent of the physical locations of the portions of the I/O system in a particular installation.

If the R field of the AIO instruction is 0 or if no device interrupt request is present, the condition code is set but the general register is not affected. If the R field of AIO is not 0, the condition code is set and register R is loaded with the following information:



Bit Position	Function
0	Data overrun: This bit is set to 1 if a data overrun has occurred in the current I/O operation.
1-7	Unique to the device and the device controller.
8	Incorrect length: if this bit is 1, an incorrect length condition has been signaled to the IOP by the device controller during the previous operation. Incorrect length is suppressed as an error by coding the SIL flag (a 1 in bit 38) of the command doubleword. At the end of the execution of an I/O command list, this status bit is 1 if an incorrect length condition occurred anywhere in the command list, regardless of the coding of the SIL flag.
9	Transmission data error: this bit is set to 1 if the IOP or device controller has detected a parity error or data overrun in the transmitted information.
10	Zero byte count: if this bit is 1, the byte count for the operation being performed by the interrupting device has been reduced to 0, and the interrupt at zero byte count (IZC) flag in the command doubleword for the operation was coded with a 1.
11	Channel end: if this bit is 1, the device controller has signaled channel end to the IOP, and the interrupt at channel end (ICE) flag in the command doubleword for the operation was coded with a 1.
12	IOP unusual end interrupt: if this bit is 1, the IOP has originated the interrupt as a result of a fault or unusual condition reported by the device.
13-20	Unassigned
21-31	I/O address: this field identifies the highest-priority device requesting an interrupt. Bit positions 21-23 identify the IOP. If bit 24 is 0, bits 25-31 constitute a common device controller and device code; if bit 24 is 1, bits 25-27 constitute a device controller code and bits 28-31 identify a device attached to that device controller.

Affected: (R), CC1, CC2

Condition code settings:

1	2	3	4	Result of AIO
0	0	-	-	normal interrupt recognition
0	1	-	-	unusual interrupt recognition
1	1	-	-	no interrupt recognition

[†] IZC, ICE, IUT, HTE, and SIL refer to flag bits in the IOP command doublewords (see Chapter 4)

4. INPUT/OUTPUT OPERATIONS

In a SIGMA 5 system, input/output operations are primarily under control of one or more input/output processors (IOPs). This allows the CPU to concentrate on program execution, free from the time-consuming details of I/O operations. Any I/O events that require CPU intervention are brought to its attention by means of the interrupt system.

In the following discussion, the terminology conventions used are that the CPU executes instructions, the IOP executes commands, and the device controllers and/or I/O devices execute orders. To illustrate, the CPU will execute the START INPUT/OUTPUT (SIO) instruction to initiate an I/O operation. During the course of an I/O operation, the IOP might issue a command called Control, to transmit a byte to a device controller or I/O device that interprets the byte as an order, such as Rewind.

SIGMA 5 IOPs operate independently after they have been started by the central processor. They automatically pick up a chain of one or more commands from core memory and then execute these commands until the chain is completed.

The SIGMA 5 computer consists of an integrated CPU-IOP combination that utilizes a single memory bus. When an input/output service call is presented to the IOP, instruction execution is suspended only long enough to allow the IOP to complete the servicing. Since the IOP is capable of operating at the maximum rated speed of memory unit response, the instruction execution rate may approach zero for very high speed I/O operations. Additional (external) I/O processors have their own memory buses, thus providing for input/output of data simultaneous with computation. Also, the external I/O processors may take advantage of memory overlap, providing higher overall I/O data rates.

The multiplexor IOP can simultaneously operate up to 32 device controllers with a combined transfer rate of 250,000 bytes per second. Each device controller is assigned its own channel and chain of I/O commands. The selector IOP can handle any one of up to 32 high-speed device controllers at rates up to the full speed of the core memory (one 32-bit word/cycle).

The flexible SIGMA 5 I/O structure permits both command chaining (making possible multiple-record operations) and data chaining (making possible scatter-read and gather-write operations) without intervening CPU control. Command chaining refers to the execution of a sequence of I/O commands, under control of an IOP, on more than one physical record. Thus, a new command must be issued for each physical record even if the operation to be performed for a record is the same as that performed for the previous record. Data chaining refers to the execution of a sequence of I/O commands, under control of an IOP, that gather (or scatter information within one physical record from (or to) more than one region of memory. Thus, a new command must be issued for each portion of a physical record when the data associated with that physical record appears (or is to appear) in noncontiguous locations in memory. For example, if information in specific columns of two cards in a file are to be stored in specific regions of memory, the I/O command list might appear as follows:

1. Read card, store columns 1-10, data chain
2. Store columns 11-60, data chain
3. Store columns 61-80, command chain (end of data chain)
4. Read card, store columns 1-40, data chain
5. Store columns 41-80 (end of command chain, end of data chain)

The SIGMA 5 CPU itself plays a minor role in the execution of an I/O operation. The CPU-executed program is responsible for creating and storing the command list (prepared prior to the initiation of any I/O operation) and for supplying the IOP with a pointer to the first command in the I/O command list. Most of the communication between the CPU and the I/O system is carried out through memory.

The following is an example of the sequence of events that occurs during an I/O operation:

1. A CPU-executed program writes a sequence of I/O commands in core memory.

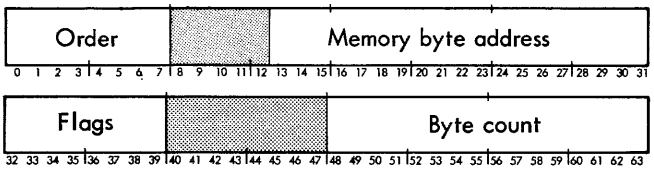
2. The CPU executes the instruction START INPUT/OUTPUT and furnishes the IOP with an 11-bit I/O address (designating the device to be started) and a 16-bit first command address (designating the actual core memory doubleword location where the first command for this device is located). At this point, either the device is started (if in the "ready" condition with no device interrupt pending) or an instruction reject occurs. The CPU is informed by condition code settings as to which of the two alternatives has occurred. If the START I/O instruction is accepted, the command counter portion of the IOP register associated with the designated device controller is loaded with the first command address. Assuming that the SIO instruction is accepted, from this time until the full sequence of I/O commands has been executed, the main program of the CPU need play no role in the I/O operation. At any time, however, it may obtain status information on the progress of the I/O operation without interfering with the operation.

3. The device is now in the "busy" condition. When the device determines that it has the highest priority for access to the IOP, it requests service from the IOP with a service call. The IOP obtains the address of the first command of the I/O command sequence (from the command counter associated with this device). The IOP then fetches an I/O command from a doubleword in core memory, loads the doubleword into another register associated with the device, and transmits the first order (extracted from the doubleword) to the device.

4. Each command counter contains the memory address of the current I/O command in the sequence for its device. When the device requires further servicing, it makes a request to the IOP, which then repeats a process similar to that of step 3.
5. If a data transmission order has been sent to a device, control of the transmission resides in the device. As each character is obtained by the I/O device, the IOP is signaled that data is available. The IOP uses the information stored in its own registers to control the information interchange between the I/O device and the memory, on either a word-by-word or character-by-character basis, depending on the nature of the device.
6. When all information exchanges called for by a single I/O command doubleword have been completed, the IOP uses the command counter to obtain the next command doubleword for execution. This process continues until all such command doublewords associated with the I/O sequence have been executed.

IOP COMMAND DOUBLEWORDS

All IOP command doublewords (except Transfer in Channel and Stop) are assumed to be in the following format:



ORDER

Bit positions 0 through 7 of the command doubleword contain the IOP order for the device controller or device. The IOP orders are shown below. Bits represented by the letter "M" specify orders or special conditions to the device and are unique for each type of device.

Bit positions 0 1 2 3 4 5 6 7	Order
M M M M M M 0 1	Write
M M M M M M 1 0	Read
M M M M M M 1 1	Control
M M M M 0 1 0 0	Sense
M M M M 1 1 0 0	Read Backward

Write. The Write order causes the device controller to initiate an output operation. Bytes are read in an ascending sequence from the memory location specified by the memory byte address field of the command doubleword. The output operation continues until the device signals "channel end", or until the byte count is reduced to 0 and no further data chaining is specified. Channel end occurs when the device has received all information associated with the output operation, has completed all checks, and no longer requires the use of IOP facilities for the operation. Data chaining is described on the following page.

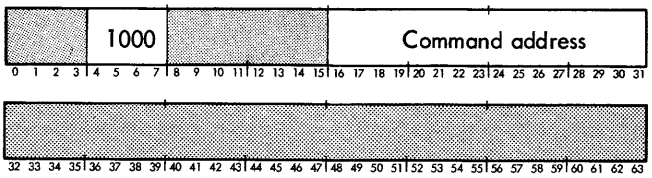
Read. The Read order causes the device controller to initiate an input operation. Bytes are stored in core memory in an ascending sequence, beginning at the location specified by the memory byte address field of the command doubleword. The input operation continues until the device signals channel end, or until the byte count is reduced to 0 and no further data chaining is specified. Channel end occurs when the device has transmitted all information associated with the input operation and no longer requires the use of IOP facilities for the operation.

Control. The Control order is used to initiate special operations by the device. For magnetic tape, it is used to issue orders such as rewind, backspace record, backspace file, etc. Most orders can be specified by the M bits of the Control order; however, if additional information is required for a particular operation (e.g., the starting address of a disc-seek), the memory byte address field of the command doubleword specifies the starting address of the bytes that are to be transmitted to the device controller for the additional information. When all bytes necessary for the operation have been transmitted, the device controller signals channel end.

Sense. The Sense order causes the device to transmit one or more bytes of information, describing its current state. The bytes are stored in core memory in an ascending sequence, beginning with the address specified by the memory byte address field of the command doubleword. The number of bytes transmitted is a function of the device and the condition it describes. The Sense order can be used to obtain the current sector address from a disc or drum unit.

Read Backward. The Read Backward order (for devices that can execute it) causes the device to be started in reverse, and bytes to be transmitted to the IOP for storage into core memory in a descending sequence, beginning at the location specified by the memory byte address field of the command doubleword. In all other respects, Read Backward is identical to Read, including reducing the byte count with each byte transmitted.

The Transfer in Channel command doubleword is assumed to be in the following format:



Transfer in Channel. The Transfer in Channel order is executed within the IOP, and it has no direct effect on any of the I/O system elements external to the addressed IOP. The primary purpose of Transfer in Channel is to permit branching within the command list so that the IOP can, for example, repeatedly transmit the same set of information a number of times. When the IOP executes Transfer in Channel, it loads the command counter for the device controller it is currently servicing with the command doubleword address field of the Transfer in Channel command, loads the new

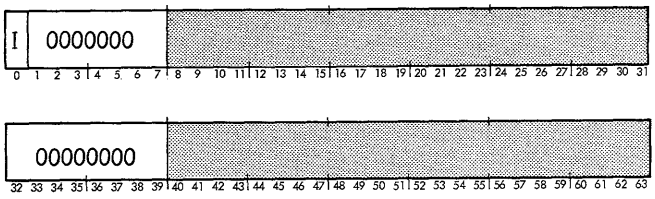
command doubleword specified by this address into the IOP registers associated with the device controller, and then executes the new command. (Bit positions 0-3, and 32-63 of the command doubleword for Transfer in Channel are ignored.) Transfer in Channel thus allows a command list to be broken into noncontiguous groups of commands. When used in conjunction with command chaining, Transfer in Channel facilitates the control of devices such as unbuffered card punches or unbuffered line printers. The current flags (see "Flags" below) are not altered during this command; thus, the type of chaining called for in the previous command doubleword is retained until changed by a command doubleword following Transfer in Channel.

For example, assume that it is desired to present the same card image twelve times to an unbuffered card punch. The punch counts the number of times that a record is presented to it and, when twelve rows have been punched, it causes the IOP to skip the command it would be executing next. Thus, a command list for punching two cards might look like the following example.

Location	Command
⋮	⋮
A	Punch row for card 1, command chain Transfer in Channel to A
B	Punch row for card 2, command chain Transfer in Channel to B Stop
⋮	

If the IOP encounters two successive Transfer in Channel commands, this is considered an IOP control error, resulting in the IOP setting the IOP control error status bit and issuing an "IOP halt" signal to the device controller. The IOP then halts further servicing of this command list.

The Stop command doubleword is assumed to be in the following format:



Stop. The Stop order causes certain devices to stop, generate a channel end condition, and also request an interrupt at location X'5C' if bit 0 in the Stop order is a 1. An AIO instruction, executed after the interrupt is acknowledged, results in a 1 in bit position 7 of Register R to indicate the reason for the interrupt. (Bit positions 32-39 of the command doubleword for stop must be zero; bit positions 8-21 and 40-63 are ignored.) The Stop order is primarily used to terminate a command chain for an unbuffered device, as illustrated in the example given for Transfer in Channel.

MEMORY BYTE ADDRESS

For all IOP commands (except Transfer in Channel and Stop), bit positions 13-31 of the command doubleword provide for a 19-bit core memory byte address, designating the memory location for the next byte of data. For the Write, Read, and Control orders, this field (as stored in an IOP register) is incremented by 1 as each byte is transmitted in the I/O operation; for the Read Backward command, the field is decremented by 1 as each byte is transmitted.

FLAGS

For all IOP commands (except Transfer in Channel and Stop) bit positions 32-39 of the command doubleword provide the IOP with eight flags that specify how to handle chaining, error, and interrupt situations. The functions of these flags are:

Bit Position	Function
32 (DC)	Data chain. If this flag is 1, data chaining is called for when the current byte count is reduced to 0. The next command doubleword is fetched and loaded into the IOP register associated with the device controller, but the new order code is not passed out to the device controller; thus, the operation called for by the previous order is continued. (Except for Transfer in Channel, the new command doubleword is used only to supply a new memory address, a new count, and new flags.) If the data chain flag is 0, no further data chaining is called for. Channel end is initiated either by the device running out of information, or by the byte count being reduced to 0. At channel end, the device may accept a new SIO instruction, providing that a device interrupt is not pending as a result of coding the IZC (bit 33), ICE (bit 35), or IUE (bit 37) flags, and no fault condition exists.
33 (IZC)	Interrupt at zero byte count. If this flag is 1, the IOP requests an interrupt at location X'5C' when the byte count of this command doubleword (as stored in the IOP register) is reduced to 0. An AIO instruction executed after the interrupt is acknowledged results in a 1 in bit position 10 of register R, to indicate the reason for the interrupt.
34 (CC)	Command chain. If this flag is 1, command chaining is called for when channel end occurs. The next command doubleword is fetched and loaded into the IOP register associated with the device controller, and the new order code is passed out to the device controller. If the CC flag is 0, no further command chaining is called for. If both data chaining and command chaining are called for in the same command doubleword, data chaining occurs if the byte count is reduced to 0 before channel end, and command chaining occurs if channel end occurs before the byte count is reduced to 0.
35 (ICE)	Interrupt at channel end. If this flag is 1, the IOP requests an interrupt at location X'5C' when channel end occurs for the operation being controlled by this command doubleword. An AIO instruction executed after the interrupt is acknowledged results

Bit Position Function

in a 1 in bit position 11 of the status information, to indicate the reason for the interrupt. If the ICE flag is 0, no interrupt is requested.

36 (HTE) Halt on transmission error. If this flag is 1, any error condition (transmission data error, transmission memory error, incorrect length error) detected in the device controller or IOP results in halting the I/O operation being controlled by this command doubleword. If the HTE flag is 0, an error condition does not cause the I/O operation to halt, although the error conditions are recorded in the IOP register and returned as part of the status information for the instructions SIO, HIO, and TIO.

37 (IUE) Interrupt on unusual end. If this flag is 1, the device controller requests an interrupt at location X'5C' when a fault condition or unusual termination is encountered. A fault is a condition requiring the device to halt, irrespective of the coding of the HTE flag. Examples of faults are torn magnetic tape and jammed cards. When unusual termination is signaled to the IOP, further servicing of the commands for that device is suspended. An AIO instruction executed after the interrupt is acknowledged results in a 1 in bit position 12 of register R, to indicate the reason for the interrupt. If the IUE flag is 0, no interrupt is requested.

38 (SIL) Suppress incorrect length. If this flag is 1, an incorrect length indication by the device controller is not to be classified as an error by the IOP, although the IOP retains the incorrect length indication and provides an indicator (bit 8 of the status response for SIO, HIO, and TIO) to the program. If the SIL flag is 0, an incorrect length is considered an error and the IOP performs as specified by the HTE and IUE flags. Incorrect length is caused by a channel end condition occurring before the device controller has received a count-done signal from the IOP, or is caused by the device controller receiving a count-done signal before end

Bit Position Function

of record; e.g., count-done before 80 columns have been read from a card. Normally, a count-done signal is sent to the device controller by the IOP to indicate that all data transfer associated with the current operation has been completed. The IOP is capable of suppressing an error condition on incorrect length, since there are many situations in which incorrect length is a legitimate condition and not a true error.

39 (S) Skip. If this flag is 1, the input operation (Read or Read Backward) controlled by this command doubleword continues normally, except that no information is stored in memory. When used in conjunction with data chaining, the skip operation provides the capability for selective reading of portions of a record.

If the S flag is 1 for an output (Write) operation, the IOP does not access memory, but transmits zeros as data instead (i.e., the IOP transmits the number of X'00' bytes specified in the byte count of the command doubleword). This allows a program to punch a blank card (by using the S bit and a Punch Binary order with a byte count of 120) without requiring memory access for data. If the S flag is 0, the I/O operation proceeds normally.

BYTE COUNT

For all commands except Transfer in Channel and Stop, bit positions 48-63 of the command doubleword provide for a 16-bit count of the number of bytes to be transmitted in the I/O operation; thus, 1 to 65,536 bytes (16,384 words) can be specified for transfer before command chaining or data chaining is required. This field (as stored in an IOP register) is decremented by 1 after each byte transmitted in the I/O operation; thus, it always contains a count of the number of bytes to be transmitted and this count is returned as part of the response information for the instructions, SIO, HIO, TIO, and TDV. An initial byte count of 0 is interpreted as 65,536 bytes.

5. OPERATOR CONTROLS

PROCESSOR CONTROL PANEL

The processor control panel (PCP) mounted in one of the CPU cabinets has two distinct functional sections (see Figure 7). The upper section (labeled MAINTENANCE SECTION) is reserved for controls and indicators related to computer maintenance and diagnostic operations. The lower section contains the controls and indicators for the computer operator and for program debugging.

POWER

The POWER switch controls all AC power to the central processor and to all units under its direct control. The POWER switch is unlighted when the AC power is off, and is lighted when AC power is on. The POWER switch is always operative (i.e., not affected by the position of the CONTROL MODE switch) to allow for situations in which power must be removed from the system.

CPU RESET/CLEAR

The CPU RESET/CLEAR switch is used to initialize the central processor. When this switch is pressed, the following operations are performed:

1. All interrupt levels are reset to the disarmed and disabled state.
2. The ALARM, WRITE KEY, INTRPT INHIBIT, POINTER, CONDITION CODE, FLOAT MODE, MODE, and TRAP indicators are all reset to 0's (turned off).
3. The INSTRUCTION ADDRESS indicators are set to X'25'.
4. The DISPLAY indicators are set to X'02000000', which is a LOAD CONDITIONS AND FLOATING CONTROL IMMEDIATE (LCFI) instruction with an R field of 0 to produce a "no operation" instruction.

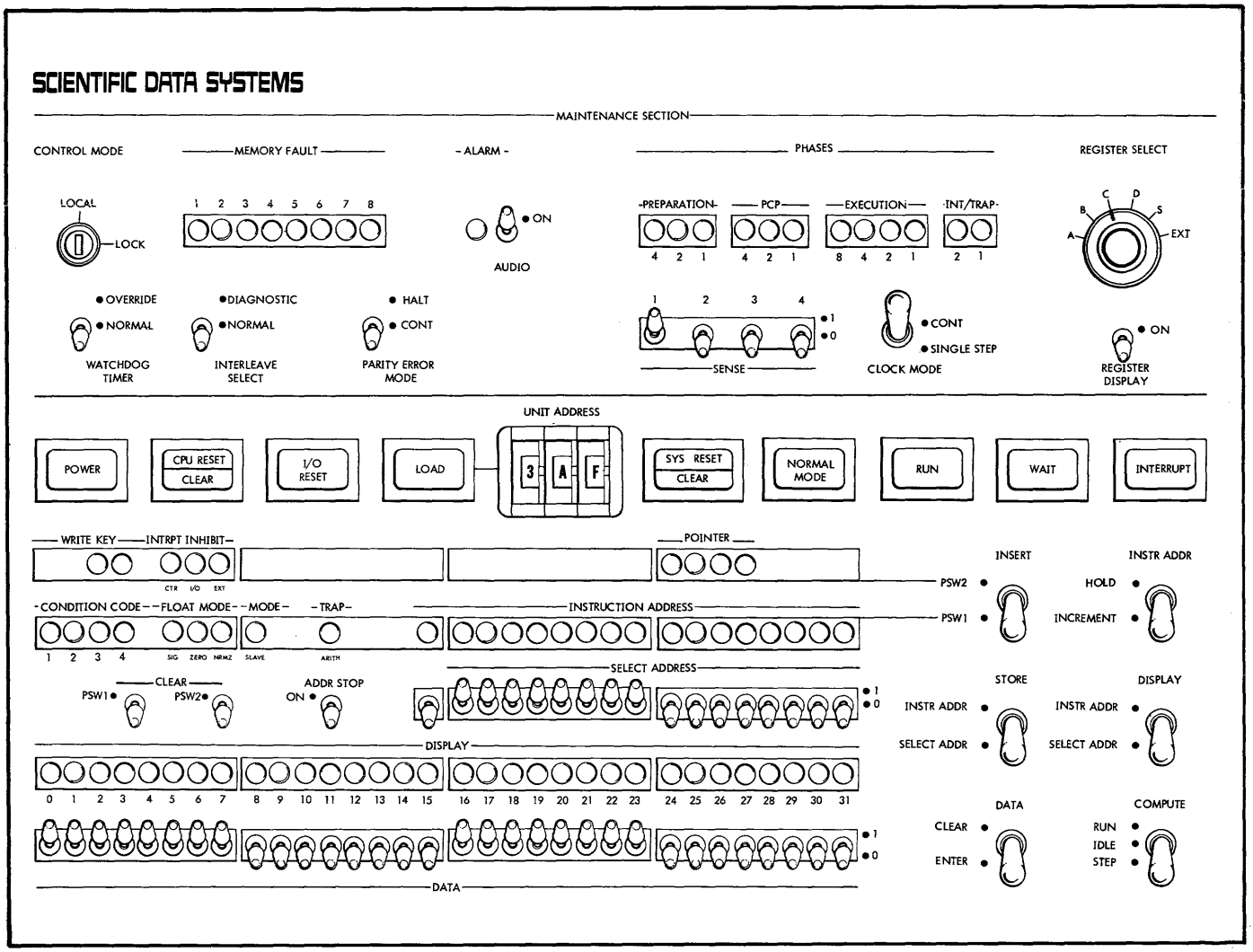


Figure 7. Processor Control Panel

The CPU RESET/CLEAR switch does not affect any operations that may be in process in the standard input/output system.

The CPU RESET/CLEAR switch is also used in conjunction with the SYS RESET/CLEAR switch to clear core memory (i.e., reset memory to all 0's). The two switches are interlocked so that both must be pressed simultaneously for the memory clear operation to occur. The memory clear operation does not affect any general register – core memory locations 0 through 15 are cleared instead. Also the clear operation does not affect the memory control storage (write locks). Note that pressing the SYS RESET/CLEAR switch affects the I/O system and the MEMORY FAULT indicators.

I/O RESET

The I/O RESET switch is used to initialize the standard input/output system. When this switch is pressed, all peripheral devices under control of the central processor are halted, and all status and control indicators in the input/output system are reset. The I/O RESET switch does not affect any operations that may be in process in the central processor.

LOAD

The LOAD switch initializes memory from an input operation that uses the peripheral unit selected by the UNIT ADDRESS switches. The detailed operation of the loading process is described in the section "Loading Operation".

UNIT ADDRESS

The three UNIT ADDRESS switches are used to select the peripheral unit to be used in the loading process. The left switch has eight positions, numbered 0 through 7, designating an input/output processor. The center and right switches each have 16 positions, numbered 0 through F (hexadecimal) that designate a device controller/device under the control of the selected input/output processor.

SYSTEM RESET/CLEAR

The SYS RESET/CLEAR switch is used to reset all controls and indicators in the SIGMA 5 system. Pressing this switch causes the computer to perform all operations described for the CPU RESET/CLEAR switch, perform all operations described for the I/O RESET switch, initialize the memory control logic, and reset the MEMORY FAULT indicators.

The SYS RESET/CLEAR switch is also used in conjunction with the CPU RESET/CLEAR switch to reset core memory to 0's.

NORMAL MODE

The NORMAL MODE indicator is lighted when all the following conditions are satisfied:

1. The WATCHDOG TIMER switch is in the NORMAL position
2. The INTERLEAVE SELECT switch is in the NORMAL position
3. The PARITY ERROR MODE switch is in the CONT (continue) position
4. The CLOCK MODE switch is in the CONT (continuous) position
5. All memory margins are "normal"

If any of the above conditions is not satisfied, the NORMAL MODE indicator is unlighted.

RUN

The RUN indicator is lighted when the COMPUTE switch is in the RUN position and no halt condition exists.

WAIT

The WAIT indicator is lighted when any of the following halt conditions exist:

1. The computer is executing a WAIT instruction
2. The program is stopped because of the ADDRESS STOP switch
3. The computer is halted because of the PARITY ERROR MODE switch.

INTERRUPT

The INTERRUPT switch is used by the operator to activate the control panel interrupt. If the control panel interrupt (level X'5D') is armed when the INTERRUPT switch is pressed, a single pulse is transmitted to the interrupt level, advancing it to the waiting state. The INTERRUPT switch is lighted when the control panel interrupt level is in the waiting state, and remains lighted until the interrupt level advances to the active state (at which time the INTERRUPT switch is turned off). If the control panel interrupt level is disarmed (or already in the active state) when the INTERRUPT switch is pressed, no computer or control panel action occurs. If the control panel interrupt level advances to the waiting state and the level is disabled, the INTERRUPT switch remains lighted until the level is either enabled and allowed to advance to the active state or is returned to the armed or disarmed state. The INTERRUPT switch is always operative.

Two rows of binary indicators are used to display the current program status doubleword (PSD). For the convenience of use and display, the second portion of the PSD, labeled PSW2, is arranged above the first portion, labeled PSW1. The PSD display consists of the indicators shown in Table 9.

INSERT

The INSERT switch is used to make changes in the program status doubleword. The switch is inactive in the center position and is momentary in the upper (PSW2) and lower (PSW1) positions. When the INSERT switch is moved to the PSW1 or PSW2 position, the corresponding indicators in the program status doubleword are altered (according to current state of the 32 DATA switches below the DISPLAY indicators) as follows: if a DATA switch is in the 1 position, the corresponding program status indicator is changed to a 1 (if not already 1); otherwise, the program status indicator remains unchanged.

Table 9. Program Status Doubleword Display

Indicator		Function	PSD Bit Position	PSD Designation
PSW2	WRITE KEY	Write key	34-35	WK
	INTRPT INHIBIT	Interrupt inhibits		
	CTR	Counter interrupt group inhibit	37	CI
	I/O	Input/output interrupt group inhibit	38	II
	EXT	External interrupts inhibit	39	EI
	POINTER	Register block pointer	56-59	RP
PSW1	CONDITION CODE	Condition code	0-3	CC
	FLOAT MODE	Floating-point mode controls		
	SIG	Significance trap mask	5	FS
	ZERO	Zero trap mask	6	FZ
	NRMZ	Normalize mask	7	FN
	MODE			
	SLAVE	Master/slave mode control	8	MS
	TRAP			
	ARITH	Fixed-point arithmetic overflow trap mask	11	AM
	INSTRUCTION ADDRESS	Address of next instruction to be executed	15-31	IA

INSTR ADDR

The INSTR ADDR (instruction address) switch is inactive in the center position; the upper position (HOLD) is latching and the lower position (INCREMENT) is momentary. When the switch is placed in the HOLD position, the normal process of incrementing the instruction address portion of the program status doubleword with each instruction execution is inhibited. If the COMPUTE switch is placed in the RUN position while the INSTR ADDR switch is at HOLD, the instruction in the location pointed to by the value of the INSTRUCTION ADDRESS indicators is executed, repeatedly, with the INSTRUCTION ADDRESS indicators remaining unchanged. If the COMPUTE switch is moved to the STEP position while the INSTR ADDR switch is at HOLD, the instruction is executed once each time the COMPUTE switch is moved to STEP; the INSTRUCTION ADDRESS indicators remain unchanged unless the instruction is LPSD, XPSD, or a branch instruction with the branch condition satisfied.

The following operations are performed each time the INSTR ADDR switch is moved from the center position to the INCREMENT position:

1. The current value of the INSTRUCTION ADDRESS indicators is incremented by 1.
2. Using the new value of the INSTRUCTION ADDRESS indicators, the contents of the location pointed to by the INSTRUCTION ADDRESS is displayed in the DISPLAY indicators.

CLEAR

The two CLEAR toggle switches below the program status doubleword display are used to clear the program status doubleword. When the left CLEAR toggle switch is moved to the PSW1 position, the CONDITION CODE, FLOAT MODE, MODE, TRAP, and INSTRUCTION ADDRESS indicators are all reset to 0's (turned off). When the right CLEAR toggle switch is moved to the PSW2 position, the WRITE KEY, INTRPT INHIBIT, and POINTER indicators are all reset to 0's.

ADDR STOP

The ADDR STOP (address stop) switch is used (with the COMPUTE switch in the RUN position) to cause the central processor to establish a halt condition and turn on the WAIT indicator whenever the CPU accesses the memory location whose address is equal to the SELECT ADDRESS value.

When the halt condition occurs, the instruction in the location pointed to by the INSTRUCTION ADDRESS indicators appears in the DISPLAY indicators. The displayed instruction is the one that would have been executed next, had the halt condition not occurred. If the halt condition is caused by an instruction access, the value of the INSTRUCTION ADDRESS indicators (at the time of the halt) is equal to the SELECT ADDRESS value. If the halt condition is caused by execution of an instruction with an indirect reference address equal to the SELECT ADDRESS value (i.e., by a direct address fetch), is caused by an instruction operand fetch, or is caused by an unsatisfied conditional branch instruction whose effective address is equal to the SELECT ADDRESS value, the value of the INSTRUCTION ADDRESS indicators (at the time of the halt) is 1 greater than the address of the instruction.

If an interrupt or trap condition is detected after the ADDRESS STOP halt condition is detected and before the CPU reaches the normal ADDRESS STOP halt phase, the CPU executes the instruction in the appropriate interrupt or trap location and then enters the ADDRESS STOP halt phase. In

this case; the value of the INSTRUCTION ADDRESS indicators (at the time of the halt) is equal to the address of the next instruction in logical sequence after the instruction in the interrupt or trap location.

The ADDRESS STOP halt condition is reset when the COMPUTE switch is moved from RUN to IDLE; if the COMPUTE switch is then moved back to RUN (or to STEP), the instruction shown in the DISPLAY indicators is the next instruction executed.

SELECT ADDRESS

The SELECT ADDRESS switches select the address at which a program is to be halted (when used in conjunction with the ADDR STOP switch), select the address of a location to be altered (when used in conjunction with the STORE switch), and select the address of a word to be displayed (when used in conjunction with the DISPLAY switch). Each SELECT ADDRESS switch represents a 1 when it is in the upper position, and represents a 0 in the lower position.

STORE

The STORE switch is used to alter the contents of a general register or a memory location. The switch is inactive in the center position and is momentary in the INSTR ADDR and SELECT ADDR positions. When the switch is moved to the INSTR ADDR position, the current value of the DISPLAY indicators is stored in the location pointed to by the INSTRUCTION ADDRESS indicators; when the switch is moved to the SELECT ADDR position, the current value of the DISPLAY indicators is stored in the location pointed to by the SELECT ADDRESS switches.

DISPLAY

The DISPLAY switch is used to display the contents of a general register or memory location. The switch is inactive in the center position and is momentary in the INSTR ADDR and SELECT ADDR positions. When the switch is moved to the INSTR ADDR or SELECT ADDR position, the word in the location pointed to by the indicators or switches, respectively, is loaded into the instruction register and displayed with the DISPLAY indicators.

The 32 DISPLAY indicators are used to display a computer word, when used together with the INSTR ADDR, STORE, DISPLAY, and DATA switches. The DISPLAY indicators represent the current contents of the internal CPU instruction register.

DATA

The 32 DATA switches beneath the DISPLAY indicators are used to alter the contents of the program status doubleword (when used in conjunction with the INSERT switch) and to alter the value of the DISPLAY indicators (when used in conjunction with the single DATA switch). Each of the 32 DATA switches is latching in both the upper (1) and lower (0) positions. In the upper position it represents a 1; in the lower, a 0. The single DATA switch is used to change the state of the DISPLAY indicators. The switch is inactive in the center position and is momentary in the CLEAR and ENTER positions. When the switch is moved to the CLEAR position, all the DISPLAY indicators are reset (turned off). When the switch is moved to the ENTER position, the display indicators are not affected in those positions corresponding to DATA switches that are in the 0 position, but if a DATA switch is in the 1 position, that value is inserted into the corresponding indicator.

COMPUTE

The COMPUTE switch is used to control the execution of instructions. The center position (IDLE) and the upper position (RUN) are both latching, and the lower position (STEP) is momentary. When the COMPUTE switch is in the IDLE position, all other control panel switches are operative and the ADDRESS STOP halt and the WAIT instruction halt conditions are reset (cleared). If the computer is in a halt condition as a result of a memory parity error, moving the COMPUTE switch to IDLE does not clear the memory parity halt condition. This condition can be cleared only by pressing the SYSTEM RESET/CLEAR switch.

When the COMPUTE switch is moved from IDLE to RUN, the RUN indicator is lighted and the computer begins to execute instructions (at machine speed) as follows:

1. The current setting of the DISPLAY indicators is taken as the next instruction to be executed, regardless of the contents of the location pointed to by the current value of the INSTRUCTION ADDRESS indicators.
2. The value of the INSTRUCTION ADDRESS indicators is incremented by 1 unless the instruction in the DISPLAY indicators was LPSD, XPSD, or a branch instruction and the branch should occur (in which case the INSTRUCTION ADDRESS indicators are set to the value established by the LPSD, XPSD, or branch instruction).
3. Instruction execution continues with the instruction in the location pointed to by the new value of the INSTRUCTION ADDRESS indicators.

When the COMPUTE switch is in the RUN position, the only switches that are operative are the POWER switch, the INTERRUPT switch, the ADDR STOP switch, the INSTR ADDR switch (in the HOLD position), and the switches in the maintenance section.

Each time the COMPUTE switch is moved from the IDLE to the STEP position, the following operations occur:

1. The current setting of the DISPLAY indicators is taken as an instruction, and the single instruction is executed.
2. The current value of the INSTRUCTION ADDRESS indicators is incremented by 1 unless the "stepped" instruction was LPSD, XPSD, or a branch instruction and the branch should occur (in which case the INSTRUCTION ADDRESS indicators are set to the value established by the LPSD, XPSD, or branch instruction).
3. The instruction in the location pointed to by the new value of the INSTRUCTION ADDRESS indicators is displayed in the DISPLAY indicators.

If an instruction is being stepped (executed by moving the COMPUTE switch from IDLE to STEP), all interrupt levels are temporarily inhibited while the instruction is being executed; however, a trap condition can occur while the instruction is being executed. In this case, the XPSD instruction in the appropriate trap location is executed as if the COMPUTE switch were in the RUN position. Thus, if a trap condition occurs during a stepped instruction, the program status doubleword display automatically reflects the effects of the XPSD instruction and the DISPLAY indicators then contain the first instruction of the trap routine.

CONTROL MODE

The CONTROL MODE switch is a two-position key lock. When the switch is at LOCAL, all controls and indicators on the processor control panel are operative.

When the CONTROL MODE switch is in the LOCK position, most of the controls in the lower portion of the processor control panel are inoperative, although all indicators on the central processor control panel continue to indicate the various computer states.

The following switches on the processor control panel remain operative when the CONTROL MODE switch is in the LOCK position:

1. The POWER switch remains operative to allow for situations in which power must be removed from the system
2. The INTERRUPT switch remains operative to allow the operator to interrupt the program being executed
3. The SENSE switches remain operative to allow the operator to provide information to the program being executed
4. The AUDIO switch remains operative to allow the operator to control the computer speaker

The following switches on the processor control panel are interlocked to specific states when the CONTROL MODE switch is in the LOCK position:

Switch	Interlock State
COMPUTE	RUN
WATCHDOG TIMER	NORMAL
INTERLEAVE SELECT	NORMAL
PARITY ERROR MODE	CONT
CLOCK MODE	CONT

MEMORY FAULT

The MEMORY FAULT indicators each correspond to a specific memory module. Whenever a memory parity error occurs or an overtemperature condition exists in a memory module, the appropriate indicator is lighted and remains lighted until the indicators are reset. When a memory parity error occurs, an interrupt pulse is also transmitted to the memory parity interrupt level.

The MEMORY FAULT indicators are reset whenever the SYS RESET/CLEAR switch is pressed or whenever the computer executes a READ DIRECT instruction coded to read the MEMORY FAULT indicators. If the reason for a MEMORY FAULT indicator being on is overtemperature, and the condition still exists when the indicators are reset, the indicator is immediately turned on again.

ALARM

The ALARM indicator is used to attract the computer operator's attention, and is turned on and off (under program control) by executing a properly coded WRITE DIRECT instruction. When the ALARM indicator is lighted and the AUDIO switch is ON, a 1000-Hz signal is sent to the computer speaker; when the AUDIO switch is not in the ON position, the speaker is disconnected. (The AUDIO switch does not affect the state of the ALARM indicator.) The ALARM indicator is reset (turned off) whenever either the CPU RESET/CLEAR or the SYS RESET/CLEAR switch is pressed.

AUDIO

The AUDIO switch controls all signals to the computer speaker, whether from the ALARM indicator or from the program-controlled frequency flip-flop.

WATCHDOG TIMER

The WATCHDOG TIMER switch is used to override the instruction watchdog timer. When this switch is at NORMAL, the watchdog timer is operative; when the switch is in the OVERRIDE position, the watchdog timer is inactive.

INTERLEAVE SELECT

The INTERLEAVE SELECT switch is used to override the normal operation of interleaved memory modules. When this switch is in the NORMAL position, memory address interleaving occurs normally; however, when the switch is in the DIAGNOSTIC position, memory addresses are not interleaved between core memory modules.

PARITY ERROR MODE

The PARITY ERROR MODE switch controls the action of the computer when a memory parity error occurs. If the PARITY ERROR MODE switch is in the CONT (continue) position when a parity error occurs, the appropriate MEMORY FAULT indicator is turned on and an interrupt pulse is transmitted to the memory parity interrupt level. If the switch is in the HALT position when a parity error occurs, the appropriate MEMORY FAULT indicator is turned on and the computer enters a "halt" state; the memory module in which the parity error occurred is unavailable to any access until the MEMORY FAULT indicators are reset. If the COMPUTE switch is in the RUN position during a halt, the WAIT indicator is lighted; however, the COMPUTE switch cannot be used alone to proceed from a halt caused by a parity error. In order to proceed, the SYS RESET/CLEAR switch must first be pressed.

PHASES

The PHASES indicators, used for maintenance functions, display certain internal operating phases of the computer. The PREPARATION indicators display computer phases during the preparation portion of an instruction cycle. The PCP (processor control panel) indicators display computer phases during processor control panel operations. The EXECUTION indicators display computer phases during the execution portion of an instruction cycle. The INT/TRAP (interrupt/trap) indicators are individually lighted when an interrupt, or trap condition occurs. When the COMPUTE switch is in the IDLE position, all of the PHASES indicators are normally off except for the center PCP indicator (phase 2 is the "idle" phase for processor control panel functions).

REGISTER SELECT

The REGISTER SELECT switch is used to display the contents of selected internal registers. When the REGISTER DISPLAY switch is in the inactive position, the DISPLAY indicators display the current contents of the internal instruction register. When the COMPUTE switch is in the IDLE position, the register selected by the REGISTER SELECT switch may be shown in the DISPLAY indicators by moving the REGISTER DISPLAY switch to the ON position.

SENSE

The four SENSE switches are used, under program control, to set the condition code portion of the program status doubleword. When a READ DIRECT or WRITE DIRECT instruction is executed in the internal control mode, the condition code is set according to the state of the four SENSE switches. If a SENSE switch is in the set (1) position, the corresponding bit of the condition code is set to 1; if a SENSE switch is in the reset (0) position, the corresponding bit of the condition code is reset to 0. The SENSE switches are always operative.

CLOCK MODE

The CLOCK MODE switch controls the internal computer clock. When the switch is in the CONT (continuous) position, the clock operates at normal speed. However, when the CLOCK MODE is in the inactive (center) position, the clock enters an idle state and can be made to generate one clock pulse each time the switch is moved to the SINGLE STEP position. When the clock is pulsed by the CLOCK MODE switch, the PHASE indicators reflect the computer phase during each pulse of the clock.

LOADING OPERATION

This section describes the procedure for initially loading programs into core memory from certain peripheral units attached to an input/output processor in the SIGMA 5 system. The computer operator may initiate a loading operation from the processor control panel only when the CONTROL MODE switch is in the LOCAL position.

The LOAD switch and the UNIT ADDRESS switches are used to prepare a SIGMA 5 computer for a load operation. When the LOAD switch is pressed, the following bootstrap program is stored in core memory locations X'20' through X'29':

Location (Hex.)	Location (Dec.)	Contents (Hexadecimal)	Symbolic form of Instruction	
20	32	00000000		
21	33	00000000		
22	34	020000A8		
23	35	0E000058		
24	36	00000011		
25	37	00000xxx[t]		
26	38	32000024	LW,0	36
27	39	CC000025	SIO,0	*37
28	40	CD000025	TIO,0	*37
29	41	69C00028	BCS,12	40

When the LOAD switch is pressed, the selected peripheral device is not activated, and no other indicators or controls are affected; only core memory is altered.

LOAD PROCEDURE

To assure correct operation of the loading process, the following sequence should always be used when initiating a load operation:

1. Place the COMPUTE switch in the IDLE position.
2. Press the SYS RESET/CLEAR switch.
3. Set the UNIT ADDRESS switches to the address of the desired peripheral unit.
4. Press the LOAD switch.
5. Place the COMPUTE switch in the RUN position.

After the COMPUTE switch is placed in the RUN position, in step 5, the following actions occur:

1. The first record on the selected peripheral device is read into memory locations X'2A' through X'3F'. (The previous contents of general register 0 are destroyed as a result of executing the bootstrap program in locations X'26' through X'29'.)
2. After the record has been read, the next instruction is taken from location X'2A' (provided that no error condition has been detected by the device or the IOP).
3. When the instruction in location X'2A' is executed, the unit device and device controller selected for loading are in a "ready" condition.
4. Further I/O operations from the load unit may be accomplished by coding subsequent I/O instructions to indirectly address location X'25'.

[t] The x's in location X'25' represent the value of the UNIT ADDRESS switches at the time the LOAD switch is pressed.

LOAD OPERATION DETAILS

The first executed instruction of the bootstrap program (in location X'26') loads general register 0 with the doubleword address of the first I/O command doubleword. The I/O address for the SIO instruction in location X'27' is the 11 low-order bits of location X'25' (which have been set equal to the load unit address as a result of pressing the LOAD switch). During the SIO instruction, general register 0 points to locations X'22' and X'23' as the first I/O command doubleword for the selected device. This command doubleword contains an order that instructs the selected peripheral device to read 88 (X'58') bytes into consecutive memory locations starting at word location X'2A' (byte location X'A8'). At the completion of the read operation, neither data chaining nor command chaining is called for in the I/O command doubleword. Also, the suppress incorrect length flag is set to 1 so that an incorrect length indication will not be considered an error. (This means that no transmission error halt will result if the first record is either less than or greater than 88 bytes. If the record is greater than 88 bytes, only the first 88 bytes will be stored in memory.) After the SIO instruction, the computer executes a TIO instruction with the same effective address the SIO instruction. The TIO instruction is coded to accept only condition code data from the IOP. The BCS instruction in location X'29' will cause a branch back to the TIO instruction as long as either CC1 or CC2 (or both) is set to 1. In normal operation, CC1 is reset to 0 and CC2 remains set to 1 until the device can accept another SIO instruction, at which time the next instruction will be taken from location X'2A'.

If a transmission error or equipment malfunction is detected by either the device or the IOP, the IOP instructs the device to halt and initiate an unusual end interrupt signal (as specified by the appropriate flags in the I/O command doubleword). The unusual end interrupt will be ignored, however, since all interrupt levels have been disarmed by pressing the SYS RESET/CLEAR switch prior to loading. The device will not accept another SIO while the device interrupt is pending and, therefore, the BCS instruction in location X'29' will continue to branch to location X'28'. The correct operator action at this point is to repeat the load procedure. If there is no I/O address recognition of the load unit, the SIO instruction will not cause any I/O action and CC1 will continue to be set to 1 by the SIO and TIO instructions; thus causing the BCS instruction to branch.

APPENDIX A. REFERENCE TABLES

This appendix contains the following reference material:

SDS STANDARD SYMBOLS AND CODES

The symbol and code standards described in this publication are applicable to all SDS products, both hardware and software. They may be expanded or altered from time to time to meet changing requirements.

The symbols listed here include two types: graphic symbols and control characters. Graphic symbols are displayable and printable; control characters are not. Hybrids are SP, the symbol for a blank space, and DEL, the delete code which is not considered a control command.

Three types of code are shown: (1) the 8-bit SDS Standard Computer Code, i.e., the SDS Extended Binary-Coded-Decimal Interchange Code (EBCDIC); (2) the 7-bit United States of America Standard Code for Information Interchange (USASCII); and (3) the SDS standard card code.

SDS STANDARD CHARACTER SETS

1. EBCDIC

   57-character set: uppercase letters, numerals, space, and & - / . < > ( ) + | $ * : ; , % # @ ' =

   64
   ~~63~~-character set: same as above plus ¢ ! _ ? " ¬ ^

   89-character set: same as 63-character set plus lowercase letters

2. USASCII

   64-character set: upper case letters, numerals, space, and ! " $ % & ' ( ) * + , - . /\ ; : = < > ? @ _ [ ] ^ #

   95-character set: same as above plus lowercase letters and { } | ~ `

CONTROL CODES

In addition to the standard character sets listed above, the SDS symbol repertoire includes 37 control codes and the hybrid code DEL (hybrid code SP is considered part of all character sets). These are listed in the table titled SDS Standard Symbol-Code Correspondences.

SPECIAL CODE PROPERTIES

The following two properties of all SDS standard codes will be retained for future standard code extensions:

1. All control codes, and only the control codes, have their two high-order bits equal to "00". DEL is not considered a control code.

2. No two graphic EBCDIC codes have their seven low-order bits equal.

SDS STANDARD 8-BIT COMPUTER CODES (EBCDIC)

Least Significant Digits	Hexadecimal	Binary	Most Significant Digits 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
			0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0	0000		NUL	DLE	ds		SP	&	-									0
1	0001		SOH	DC1	ss				/		a	j	.	\ [1]	A	J		1
2	0010		STX	DC2	fs						b	k	s	{ [1]	B	K	S	2
3	0011		ETX	DC3	si						c	l	t	} [1]	C	L	T	3
4	0100		EOT	DC4							d	m	u	[[1]	D	M	U	4
5	0101		HT	LF NL			Will not be assigned				e	n	v	] [1]	E	N	V	5
6	0110		ACK	SYN							f	o	w		F	O	W	6
7	0111		BEL	ETB							g	p	x		G	P	X	7
8	1000		EOM BS	CAN							h	q	y		H	Q	Y	8
9	1001		ENQ	EM							i	r	z		I	R	Z	9
A	1010		NAK	SS			¢ [2]	!	¬ [1]	:								
B	1011		VT	ESC			.	$	,	#								
C	1100		FF	FS			<	*	%	@					Will not be assigned			
D	1101		CR	GS			(	)	_	'								
E	1110		SO	RS			+	;	>	=								
F	1111		SI	US	PE		| [2]	¬ [2]	?	"								DEL
					3			4					5					

NOTES:

1 The characters ^ \ { } [ ] are USASCII characters that do not appear in any of the SDS EBCDIC-based character sets, though they are shown in the EBCDIC table.

2 The characters ¢ | ¬ appear in the SDS 63- and 89-character EBCDIC sets but not in either of the SDS USASCII-based sets. However, SDS software translates the characters ¢ | ¬ into USASCII characters as follows:

EBCDIC	=	UASCII
¢		` (6-0)
|		¦ (7-12)
¬		~ (7-14)

3 The EBCDIC control codes in columns 0 and 1 and their binary representation are exactly the same as those in the USASCII table, except for two interchanges: LF/NL with NAK, and HT with ENQ.

4 Characters enclosed in heavy lines are included only in the SDS standard 63- and 89-character EBCDIC sets.

5 These characters are included only in the SDS standard 89-character EBCDIC set.

SDS STANDARD 7-BIT COMMUNICATION CODES (USASCII) [1]

Least Significant Digits	Decimal (rows) (col's.) →	Binary [1]	Most Significant Digits 0	1	2	3	4	5	6	7
	↓		x000	x001	x010	x011	x100	x101	x110	x111
0	0000		NUL	DLE	SP	0	@	P	`	p
1	0001		SOH	DC1	! [5]	1	A	Q	a	q
2	0010		STX	DC2	"	2	B	R	b	r
3	0011		ETX	DC3	#	3	C	S	c	s
4	0100		EOT	DC4	$	4	D	T	d	t
5	0101		ENQ	NAK	%	5	E	U	e	u
6	0110		ACK	SYN	&	6	F	V	f	v
7	0111		BEL	ETB	'	7	G	W	g	w
8	1000		BS	CAN	(	8	H	X	h	x
9	1001		HT	EM	)	9	I	Y	i	y
10	1010		LF NL	SS	*	:	J	Z	j	z
11	1011		VT	ESC	+	;	K	[[5]	k	{
12	1100		FF	FS	,	<	L	\	l	|
13	1101		CR	GS	-	=	M	] [5]	m	}
14	1110		SO	RS	.	>	N	^ [4] [5]	n	~ [4]
15	1111		SI	US	/	?	O	_ [4]	o	DEL
					2			3		

NOTES:

1 Most significant bit, added for 8-bit format, is either 0 or an even-parity bit for the remaining 7 bits.

2 Columns 0-1 are control codes.

3 Columns 2-5 correspond to the SDS 64-character USASCII set.
Columns 2-7 correspond to the SDS 95-character USASCII set.

4 On many current teletypes, the symbol

^ is ↑ (5-14)
_ is ← (5-15)
~ is ESC or ALTMODE control (7-14)

and none of the symbols appearing in columns 6-7 are provided. Except for the three symbol differences noted above, therefore, such teletypes provide all the characters in the SDS 64-character USASCII set. (The SDS 7015 Remote Keyboard Printer provides the 64-character USASCII set also, but prints ^ as ∧.)

5 On the SDS 7670 Remote Batch Terminal, the symbol

! is | (2-1)
[is ¢ (5-11)
] is ! (5-13)
^ is ¬ (5-14)

and none of the symbols appearing in columns 6-7 are provided. Except for the four symbol differences noted above, therefore, this terminal provides all the characters in the SDS 64-character USASCII set.

SDS STANDARD SYMBOL-CODE CORRESPONDENCES

EBCDIC†	Symbol	Card Code	USASCII††	Meaning	Remarks
00	NUL	12-0-9-8-1	0-0	null	00 through 23 and 2F are control codes.
01	SOH	12-9-1	0-1	start of header	
02	STX	12-9-2	0-2	start of text	
03	ETX	12-9-3	0-3	end of text	
04	EOT	12-9-4	0-4	end of transmission	
05	HT	12-9-5	0-9	horizontal tab	
06	ACK	12-9-6	0-6	acknowledge (positive)	
07	BEL	12-9-7	0-7	bell	
08	BS or EOM	12-9-8	0-8	backspace or end of message	EOM is used only on SDS Keyboard/ Printers Models 7012, 7020, 8091, and 8092.
09	ENQ	12-9-8-1	0-5	enquiry	
0A	NAK	12-9-8-2	1-5	negative acknowledge	
0B	VT	12-9-8-3	0-11	vertical tab	
0C	FF	12-9-8-4	0-12	form feed	
0D	CR	12-9-8-5	0-13	carriage return	
0E	SO	12-9-8-6	0-14	shift out	
0F	SI	12-9-8-7	0-15	shift in	
10	DLE	12-11-9-8-1	1-0	data link escape	
11	DC1	11-9-1	1-1	device control 1	
12	DC2	11-9-2	1-2	device control 2	
13	DC3	11-9-3	1-3	device control 3	
14	DC4	11-9-4	1-4	device control 4	
15	LF or NL	11-9-5	0-10	line feed or new line	
16	SYN	11-9-6	1-6	sync	
17	ETB	11-9-7	1-7	end of transmission block	
18	CAN	11-9-8	1-8	cancel	
19	EM	11-9-8-1	1-9	end of medium	
1A	SS	11-9-8-2	1-10	start of special sequence	
1B	ESC	11-9-8-3	1-11	escape	
1C	FS	11-9-8-4	1-12	file separator	
1D	GS	11-9-8-5	1-13	group separator	
1E	RS	11-9-8-6	1-14	record separator	
1F	US	11-9-8-7	1-15	unit separator	
20	ds	11-0-9-8-1		digit selector	20 through 23 are used with Sigma 7 EDIT BYTE STRING (EBS) instruction — not input/output control codes. 24 through 2E are unassigned.
21	ss	0-9-1		significance start	
22	fs	0-9-2		field separation	
23	si	0-9-3		immediate significance start	
24		0-9-4			
25		0-9-5			
26		0-9-6			
27		0-9-7			
28		0-9-8			
29		0-9-8-1			
2A		0-9-8-2			
2B		0-9-8-3			
2C		0-9-8-4			
2D		0-9-8-5			
2E		0-9-8-6			
2F	PE	0-9-8-7		parity error	If parity checking is requested.
30		12-11-0-9-8-1			30 through 3F are unassigned.
31		9-1			
32		9-2			
33		9-3			
34		9-4			
35		9-5			
36		9-6			
37		9-7			
38		9-8			
39		9-8-1			
3A		9-8-2			
3B		9-8-3			
3C		9-8-4			
3D		9-8-5			
3E		9-8-6			
3F		9-8-7			

†Hexadecimal notation.

††Decimal notation (column-row).

SDS STANDARD SYMBOL-CODE CORRESPONDENCES (Cont.)

EBCDIC†	Symbol	Card Code	USASCII††	Meaning	Remarks
40	SP	blank	2-0	blank	
41		12-0-9-1			41 through 49 will not be assigned.
42		12-0-9-2			
43		12-0-9-3			
44		12-0-9-4			
45		12-0-9-5			
46		12-0-9-6			
47		12-0-9-7			
48		12-0-9-8			
49		12-8-1			
4A	¢ or `	12-8-2	6-0	cent or accent grave	Accent grave used for left single quote. On model 7670, ` not available, and ¢ = USASCII 5-11.
4B	.	12-8-3	2-14	period	
4C		12-8-4	3-12	less than	
4D	(	12-8-5	2-8	left parenthesis	
4E	+	12-8-6	2-11	plus	
4F	| or ¦	12-8-7	7-12	vertical bar or broken bar	On Model 7670, ¦ not available, and | = ASASCII 2-1.
50	&	12	2-6	ampersand	
51		12-11-9-1			51 through 59 will not be assigned.
52		12-11-9-2			
53		12-11-9-3			
54		12-11-9-4			
55		12-11-9-5			
56		12-11-9-6			
57		12-11-9-7			
58		12-11-9-8			
59		11-8-1			
5A	!	11-8-2	2-1	exclamation point	On Model 7670, ! is |.
5B	$	11-8-3	2-4	dollars	
5C	*	11-8-4	2-10	asterisk	
5D	)	11-8-5	2-9	right parenthesis	
5E	;	11-8-6	3-11	semicolon	
5F	~ or ¬	11-8-7	7-14	tilde or logical not	On Model 7670, ~ is not available, and ¬ = USASCII 5-14.
60	-	11	2-13	minus, dash, hyphen	
61	/	0-1	2-15	slash	
62		11-0-9-2			62 through 69 will not be assigned.
63		11-0-9-3			
64		11-0-9-4			
65		11-0-9-5			
66		11-0-9-6			
67		11-0-9-7			
68		11-0-9-8			
69		0-8-1			
6A	^	12-11	5-14	circumflex	On Model 7670 ^ is ¬. On Model 7015 ^ is ∧ (caret).
6B	,	0-8-3	2-12	comma	
6C	%	0-8-4	2-5	percent	
6D	_	0-8-5	5-15	underline	Underline is sometimes called "break character"; may be printed along bottom of character line.
6E	>	0-8-6	3-14	greater than	
6F	?	0-8-7	3-15	question mark	
70		12-11-0			70 through 79 will not be assigned.
71		12-11-0-9-1			
72		12-11-0-9-2			
73		12-11-0-9-3			
74		12-11-0-9-4			
75		12-11-0-9-5			
76		12-11-0-9-6			
77		12-11-0-9-7			
78		12-11-0-9-8			
79		8-1			
7A	:	8-2	3-10	colon	
7B	#	8-3	2-3	number	
7C	@	8-4	4-0	at	
7D	'	8-5	2-7	apostrophe (right single quote)	
7E	=	8-6	3-13	equals	
7F	"	8-7	2-2	quotation mark	

†Hexadecimal notation

††Decimal notation (column-row).

EBCDIC†	Symbol	Card Code	USASCII††	Meaning	Remarks
80		12-0-8-1			80 is unassigned.
81	a	12-0-1	6-1		81-89, 91-99, A2-A9 comprise the
82	b	12-0-2	6-2		lowercase alphabet. Available
83	c	12-0-3	6-3		only in SDS standard 89- and 95-
84	d	12-0-4	6-4		character sets.
85	e	12-0-5	6-5		
86	f	12-0-6	6-6		
87	g	12-0-7	6-7		
88	h	12-0-8	6-8		
89	i	12-0-9	6-9		
8A		12-0-8-2			8A through 90 are unassigned.
8B		12-0-8-3			
8C		12-0-8-4			
8D		12-0-8-5			
8E		12-0-8-6			
8F		12-0-8-7			
90		12-11-8-1			
91	j	12-11-1	6-10		
92	k	12-11-2	6-11		
93	l	12-11-3	6-12		
94	m	12-11-4	6-13		
95	n	12-11-5	6-14		
96	o	12-11-6	6-15		
97	p	12-11-7	7-0		
98	q	12-11-8	7-1		
99	r	12-11-9	7-2		
9A		12-11-8-2			9A through A1 are unassigned.
9B		12-11-8-3			
9C		12-11-8-4			
9D		12-11-8-5			
9E		12-11-8-6			
9F		12-11-8-7			
A0		11-0-8-1			
A1		11-0-1			
A2	s	11-0-2	7-3		
A3	t	11-0-3	7-4		
A4	u	11-0-4	7-5		
A5	v	11-0-5	7-6		
A6	w	11-0-6	7-7		
A7	x	11-0-7	7-8		
A8	y	11-0-8	7-9		
A9	z	11-0-9	7-10		
AA		11-0-8-2			AA through B0 are unassigned.
AB		11-0-8-3			
AC		11-0-8-4			
AD		11-0-8-5			
AE		11-0-8-6			
AF		11-0-8-7			
B0		12-11-0-8-1			
B1	\	12-11-0-1	5-12	backslash	
B2	{	12-11-0-2	7-11	left brace	
B3	}	12-11-0-3	7-13	right brace	
B4	[	12-11-0-4	5-11	left bracket	On Model 7670, [is ¢.
B5	]	12-11-0-5	5-13	right bracket	On Model 7670,] is !.
B6		12-11-0-6			B6 through BF are unassigned.
B7		12-11-0-7			
B8		12-11-0-8			
B9		12-11-0-9			
BA		12-11-0-8-2			
BB		12-11-0-8-3			
BC		12-11-0-8-4			
BD		12-11-0-8-5			
BE		12-11-0-8-6			
BF		12-11-0-8-7			

†Hexadecimal notation.

††Decimal notation (column-row).

SDS STANDARD SYMBOL-CODE CORRESPONDENCES (Cont.)

EBCDIC[†]	Symbol	Card Code	USASCII[††]	Meaning	Remarks
C0		12-0			C0 is unassigned.
C1	A	12-1	4-1		C1-C9, D1-D9, E2-E9 comprise the uppercase alphabet.
C2	B	12-2	4-2		
C3	C	12-3	4-3		
C4	D	12-4	4-4		
C5	E	12-5	4-5		
C6	F	12-6	4-6		
C7	G	12-7	4-7		
C8	H	12-8	4-8		
C9	I	12-9	4-9		
CA		12-0-9-8-2			CA through CF will not be assigned.
CB		12-0-9-8-3			
CC		12-0-9-8-4			
CD		12-0-9-8-5			
CE		12-0-9-8-6			
CF		12-0-9-8-7			
D0		11-0			D0 is unassigned.
D1	J	11-1	4-10		
D2	K	11-2	4-11		
D3	L	11-3	4-12		
D4	M	11-4	4-13		
D5	N	11-5	4-14		
D6	O	11-6	4-15		
D7	P	11-7	5-0		
D8	Q	11-8	5-1		
D9	R	11-9	5-2		
DA		12-11-9-8-2			DA through DF will not be assigned.
DB		12-11-9-8-3			
DC		12-11-9-8-4			
DD		12-11-9-8-5			
DE		12-11-9-8-6			
DF		12-11-9-8-7			
E0		0-8-2	11-0-9-1		E0, E1 are unassigned.
E1		11-0-9-1			
E2	S	0-2	5-3		
E3	T	0-3	5-4		
E4	U	0-4	5-5		
E5	V	0-5	5-6		
E6	W	0-6	5-7		
E7	X	0-7	5-8		
E8	Y	0-8	5-9		
E9	Z	0-9	5-10		
EA		11-0-9-8-2			EA through EF will not be assigned.
EB		11-0-9-8-3			
EC		11-0-9-8-4			
ED		11-0-9-8-5			
EE		11-0-9-8-6			
EF		11-0-9-8-7			
F0	0	0	3-0		
F1	1	1	3-1		
F2	2	2	3-2		
F3	3	3	3-3		
F4	4	4	3-4		
F5	5	5	3-5		
F6	6	6	3-6		
F7	7	7	3-7		
F8	8	8	3-8		
F9	9	9	3-9		
FA		12-11-0-9-8-2			FA through FE will not be assigned.
FB		12-11-0-9-8-3			
FC		12-11-0-9-8-4			
FD		12-11-0-9-8-5			
FE		12-11-0-9-8-6			
FF	DEL	12-11-0-9-8-7		delete	Special – neither graphic nor control symbol.

[†]Hexadecimal notation.

[††]Decimal notation (column-row).

HEXADECIMAL ARITHMETIC

ADDITION TABLE

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

MULTIPLICATION TABLE

1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	04	06	08	0A	0C	0E	10	12	14	16	18	1A	1C	1E
3	06	09	0C	0F	12	15	18	1B	1E	21	24	27	2A	2D
4	08	0C	10	14	18	1C	20	24	28	2C	30	34	38	3C
5	0A	0F	14	19	1E	23	28	2D	32	37	3C	41	46	4B
6	0C	12	18	1E	24	2A	30	36	3C	42	48	4E	54	5A
7	0E	15	1C	23	2A	31	38	3F	46	4D	54	5B	62	69
8	10	18	20	28	30	38	40	48	50	58	60	68	70	78
9	12	1B	24	2D	36	3F	48	51	5A	63	6C	75	7E	87
A	14	1E	28	32	3C	46	50	5A	64	6E	78	82	8C	96
B	16	21	2C	37	42	4D	58	63	6E	79	84	8F	9A	A5
C	18	24	30	3C	48	54	60	6C	78	84	90	9C	A8	B4
D	1A	27	34	41	4E	5B	68	75	82	8F	9C	A9	B6	C3
E	1C	2A	38	46	54	62	70	7E	8C	9A	A8	B6	C4	D2
F	1E	2D	3C	4B	5A	69	78	87	96	A5	B4	C3	D2	E1

TABLE OF POWERS OF SIXTEEN$_{10}$

16^n	n	16^{-n}
1	0	0.10000 00000 00000 00000 × 10
16	1	0.62500 00000 00000 00000 × 10^{-1}
256	2	0.39062 50000 00000 00000 × 10^{-2}
4 096	3	0.24414 06250 00000 00000 × 10^{-3}
65 536	4	0.15258 78906 25000 00000 × 10^{-4}
1 048 576	5	0.95367 43164 06250 00000 × 10^{-6}
16 777 216	6	0.59604 64477 53906 25000 × 10^{-7}
268 435 456	7	0.37252 90298 46191 40625 × 10^{-8}
4 294 967 296	8	0.23283 06436 53869 62891 × 10^{-9}
68 719 476 736	9	0.14551 91522 83668 51807 × 10^{-10}
1 099 511 627 776	10	0.90949 47017 72928 23792 × 10^{-12}
17 592 186 044 416	11	0.56843 41886 08080 14870 × 10^{-13}
281 474 976 710 656	12	0.35527 13678 80050 09294 × 10^{-14}
4 503 599 627 370 496	13	0.22204 46049 25031 30808 × 10^{-15}
72 057 594 037 927 936	14	0.13877 78780 78144 56755 × 10^{-16}
1 152 921 504 606 846 976	15	0.86736 17379 88403 54721 × 10^{-18}

TABLE OF POWERS OF TEN$_{16}$

10^n	n	10^{-n}
1	0	1.0000 0000 0000 0000
A	1	0.1999 9999 9999 999A
64	2	0.28F5 C28F 5C28 F5C3 × 16^{-1}
3E8	3	0.4189 374B C6A7 EF9E × 16^{-2}
2710	4	0.68DB 8BAC 710C B296 × 16^{-3}
1 86A0	5	0.A7C5 AC47 1B47 8423 × 16^{-4}
F 4240	6	0.10C6 F7A0 B5ED 8D37 × 16^{-4}
98 9680	7	0.1AD7 F29A BCAF 4858 × 16^{-5}
5F5 E100	8	0.2AF3 1DC4 6118 73BF × 16^{-6}
3B9A CA00	9	0.44B8 2FA0 9B5A 52CC × 16^{-7}
2 540B E400	10	0.6DF3 7F67 5EF6 EADF × 16^{-8}
17 4876 E800	11	0.AFEB FF0B CB24 AAFF × 16^{-9}
E8 D4A5 1000	12	0.1197 9981 2DEA 1119 × 16^{-9}
918 4E72 A000	13	0.1C25 C268 4976 81C2 × 16^{-10}
5AF3 107A 4000	14	0.2D09 370D 4257 3604 × 16^{-11}
3 8D7E A4C6 8000	15	0.480E BE7B 9D58 566D × 16^{-12}
23 8652 6FC1 0000	16	0.734A CA5F 6226 F0AE × 16^{-13}
163 4578 5D8A 0000	17	0.B877 AA32 36A4 B449 × 16^{-14}
DE0 B6B3 A764 0000	18	0.1272 5DD1 D243 ABA1 × 16^{-14}
8AC7 2304 89E8 0000	19	0.1D83 C94F B6D2 AC35 × 16^{-15}

HEXADECIMAL-DECIMAL INTEGER CONVERSION TABLE

The table below provides for direct conversions between hexadecimal integers in the range 0—FFF and decimal integers in the range 0—4095. For conversion of larger integers, the table values may be added to the following figures:

Hexadecimal	Decimal	Hexadecimal	Decimal
01 000	4 096	20 000	131 072
02 000	8 192	30 000	196 608
03 000	12 288	40 000	262 144
04 000	16 384	50 000	327 680
05 000	20 480	60 000	393 216
06 000	24 576	70 000	458 752
07 000	28 672	80 000	524 288
08 000	32 768	90 000	589 824
09 000	36 864	A0 000	655 360
0A 000	40 960	B0 000	720 896
0B 000	45 056	C0 000	786 432
0C 000	49 152	D0 000	851 968
0D 000	53 248	E0 000	917 504
0E 000	57 344	F0 000	983 040
0F 000	61 440	100 000	1 048 576
10 000	65 536	200 000	2 097 152
11 000	69 632	300 000	3 145 728
12 000	73 728	400 000	4 194 304
13 000	77 824	500 000	5 242 880
14 000	81 920	600 000	6 291 456
15 000	86 016	700 000	7 340 032
16 000	90 112	800 000	8 388 608
17 000	94 208	900 000	9 437 184
18 000	98 304	A00 000	10 485 760
19 000	102 400	B00 000	11 534 336
1A 000	106 496	C00 000	12 582 912
1B 000	110 592	D00 000	13 631 488
1C 000	114 688	E00 000	14 680 064
1D 000	118 784	F00 000	15 728 640
1E 000	122 880	1 000 000	16 777 216
1F 000	126 976	2 000 000	33 554 432

Hexadecimal fractions may be converted to decimal fractions as follows:

1. Express the hexadecimal fraction as an integer times 16^{-n}, where n is the number of significant hexadecimal places to the right of the hexadecimal point.

$$0.\,CA9BF3_{16} = CA9\,BF3_{16} \times 16^{-6}$$

2. Find the decimal equivalent of the hexadecimal integer

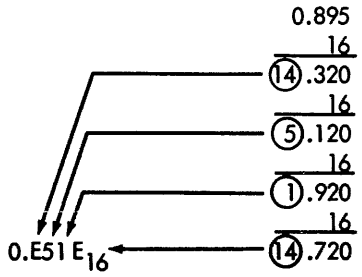
$$CA9\,BF3_{16} = 13\,278\,195_{10}$$

3. Multiply the decimal equivalent by 16^{-n}

$$\begin{array}{r} 13\,278\,195 \\ \times\ 596\,046\,448 \times 10^{-16} \\ \hline 0.791\,442\,096_{10} \end{array}$$

Decimal fractions may be converted to hexadecimal fractions by successively multiplying the decimal fraction by 16_{10}. After each multiplication, the integer portion is removed to form a hexadecimal fraction by building to the right of the hexadecimal point. However, since decimal arithmetic is used in this conversion, the integer portion of each product must be converted to hexadecimal numbers.

Example: Convert 0.895_{10} to its hexadecimal equivalent



	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
010	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
020	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
030	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
040	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
050	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
060	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
070	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
080	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
090	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
0A0	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
0B0	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
0C0	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
0D0	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
0E0	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
0F0	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
100	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
110	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
120	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
130	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
140	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
150	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
160	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
170	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
180	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
190	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
1A0	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
1B0	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
1C0	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
1D0	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
1E0	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
1F0	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511
200	0512	0513	0514	0515	0516	0517	0518	0519	0520	0521	0522	0523	0524	0525	0526	0527
210	0528	0529	0530	0531	0532	0533	0534	0535	0536	0537	0538	0539	0540	0541	0542	0543
220	0544	0545	0546	0547	0548	0549	0550	0551	0552	0553	0554	0555	0556	0557	0558	0559
230	0560	0561	0562	0563	0564	0565	0566	0567	0568	0569	0570	0571	0572	0573	0574	0575
240	0576	0577	0578	0579	0580	0581	0582	0583	0584	0585	0586	0587	0588	0589	0590	0591
250	0592	0593	0594	0595	0596	0597	0598	0599	0600	0601	0602	0603	0604	0605	0606	0607
260	0608	0609	0610	0611	0612	0613	0614	0615	0616	0617	0618	0619	0620	0621	0622	0623
270	0624	0625	0626	0627	0628	0629	0630	0631	0632	0633	0634	0635	0636	0637	0638	0639
280	0640	0641	0642	0643	0644	0645	0646	0647	0648	0649	0650	0651	0652	0653	0654	0655
290	0656	0657	0658	0659	0660	0661	0662	0663	0664	0665	0666	0667	0668	0669	0670	0671
2A0	0672	0673	0674	0675	0676	0677	0678	0679	0680	0681	0682	0683	0684	0685	0686	0687
2B0	0688	0689	0690	0691	0692	0693	0694	0695	0696	0697	0698	0699	0700	0701	0702	0703
2C0	0704	0705	0706	0707	0708	0709	0710	0711	0712	0713	0714	0715	0716	0717	0718	0719
2D0	0720	0721	0722	0723	0724	0725	0726	0727	0728	0729	0730	0731	0732	0733	0734	0735
2E0	0736	0737	0738	0739	0740	0741	0742	0743	0744	0745	0746	0747	0748	0749	0750	0751
2F0	0752	0753	0754	0755	0756	0757	0758	0759	0760	0761	0762	0763	0764	0765	0766	0767
300	0768	0769	0770	0771	0772	0773	0774	0775	0776	0777	0778	0779	0780	0781	0782	0783
310	0784	0785	0786	0787	0788	0789	0790	0791	0792	0793	0794	0795	0796	0797	0798	0799
320	0800	0801	0802	0803	0804	0805	0806	0807	0808	0809	0810	0811	0812	0813	0814	0815
330	0816	0817	0818	0819	0820	0821	0822	0823	0824	0825	0826	0827	0828	0829	0830	0831
340	0832	0833	0834	0835	0836	0837	0838	0839	0840	0841	0842	0843	0844	0845	0846	0847
350	0848	0849	0850	0851	0852	0853	0854	0855	0856	0857	0858	0859	0860	0861	0862	0863
360	0864	0865	0866	0867	0868	0869	0870	0871	0872	0873	0874	0875	0876	0877	0878	0879
370	0880	0881	0882	0883	0884	0885	0886	0887	0888	0889	0890	0891	0892	0893	0894	0895
380	0896	0897	0898	0899	0900	0901	0902	0903	0904	0905	0906	0907	0908	0909	0910	0911
390	0912	0913	0914	0915	0916	0917	0918	0919	0920	0921	0922	0923	0924	0925	0926	0927
3A0	0928	0929	0930	0931	0932	0933	0934	0935	0936	0937	0938	0939	0940	0941	0942	0943
3B0	0944	0945	0946	0947	0948	0949	0950	0951	0952	0953	0954	0955	0956	0957	0958	0959
3C0	0960	0961	0962	0963	0964	0965	0966	0967	0968	0969	0970	0971	0972	0973	0974	0975
3D0	0976	0977	0978	0979	0980	0981	0982	0983	0984	0985	0986	0987	0988	0989	0990	0991
3E0	0992	0993	0994	0995	0996	0997	0998	0999	1000	1001	1002	1003	1004	1005	1006	1007
3F0	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

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400	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
410	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
420	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
430	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
440	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
450	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
460	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
470	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
480	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
490	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A0	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B0	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C0	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D0	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E0	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F0	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
500	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
510	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
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560	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
570	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
580	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
590	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
5A0	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
5B0	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C0	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D0	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E0	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F0	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535
600	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
610	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
620	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
630	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
640	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
650	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
660	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
670	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
680	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
690	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
6A0	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
6B0	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727
6C0	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
6D0	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
6E0	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
6F0	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791

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700	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
710	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
720	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
730	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
740	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
750	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
760	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
770	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
780	1920	1921	1922	1923	1924	1925	1926	1927	1928	1929	1930	1931	1932	1933	1934	1935
790	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
7A0	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B0	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C0	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D0	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E0	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F0	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047
800	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063
810	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079
820	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
830	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111
840	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127
850	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143
860	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159
870	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175
880	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191
890	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207
8A0	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223
8B0	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239
8C0	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255
8D0	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271
8E0	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287
8F0	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303
900	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319
910	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335
920	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351
930	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367
940	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383
950	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399
960	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415
970	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431
980	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447
990	2448	2449	2450	2451	2452	2453	2454	2455	2456	2457	2458	2459	2460	2461	2462	2463
9A0	2464	2465	2466	2467	2468	2469	2470	2471	2472	2473	2474	2475	2476	2477	2478	2479
9B0	2480	2481	2482	2483	2484	2485	2486	2487	2488	2489	2490	2491	2492	2493	2494	2495
9C0	2496	2497	2498	2499	2500	2501	2502	2503	2504	2505	2506	2507	2508	2509	2510	2511
9D0	2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524	2525	2526	2527
9E0	2528	2529	2530	2531	2532	2533	2534	2535	2536	2537	2538	2539	2540	2541	2542	2543
9F0	2544	2545	2546	2547	2548	2549	2550	2551	2552	2553	2554	2555	2556	2557	2558	2559

HEXADECIMAL - DECIMAL INTEGER CONVERSION TABLE (cont.)

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A10	2576	2577	2578	2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
A20	2592	2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605	2606	2607
A30	2608	2609	2610	2611	2612	2613	2614	2615	2616	2617	2618	2619	2620	2621	2622	2623
A40	2624	2625	2626	2627	2628	2629	2630	2631	2632	2633	2634	2635	2636	2637	2638	2639
A50	2640	2641	2642	2643	2644	2645	2646	2647	2648	2649	2650	2651	2652	2653	2654	2655
A60	2656	2657	2658	2659	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671
A70	2672	2673	2674	2675	2676	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686	2687
A80	2688	2689	2690	2691	2692	2693	2694	2695	2696	2697	2698	2699	2700	2701	2702	2703
A90	2704	2705	2706	2707	2708	2709	2710	2711	2712	2713	2714	2715	2716	2717	2718	2719
AA0	2720	2721	2722	2723	2724	2725	2726	2727	2728	2729	2730	2731	2732	2733	2734	2735
AB0	2736	2737	2738	2739	2740	2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751
AC0	2752	2753	2754	2755	2756	2757	2758	2759	2760	2761	2762	2763	2764	2765	2766	2767
AD0	2768	2769	2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782	2783
AE0	2784	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796	2797	2798	2799
AF0	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815
B00	2816	2817	2818	2819	2820	2821	2822	2823	2824	2825	2826	2827	2828	2829	2830	2831
B10	2832	2833	2834	2835	2836	2837	2838	2839	2840	2841	2842	2843	2844	2845	2846	2847
B20	2848	2849	2850	2851	2852	2853	2854	2855	2856	2857	2858	2859	2860	2861	2862	2863
B30	2864	2865	2866	2867	2868	2869	2870	2871	2872	2873	2874	2875	2876	2877	2878	2879
B40	2880	2881	2882	2883	2884	2885	2886	2887	2888	2889	2890	2891	2892	2893	2894	2895
B50	2896	2897	2898	2899	2900	2901	2902	2903	2904	2905	2906	2907	2908	2909	2910	2911
B60	2912	2913	2914	2915	2916	2917	2918	2919	2920	2921	2922	2923	2924	2925	2926	2927
B70	2928	2929	2930	2931	2932	2933	2934	2935	2936	2937	2938	2939	2940	2941	2942	2943
B80	2944	2945	2946	2947	2948	2949	2950	2951	2952	2953	2954	2955	2956	2957	2958	2959
B90	2960	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2971	2972	2973	2974	2975
BA0	2976	2977	2978	2979	2980	2981	2982	2983	2984	2985	2986	2987	2988	2989	2990	2991
BB0	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC0	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD0	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE0	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF0	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071
C00	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C10	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C20	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C30	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C40	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C50	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C60	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C70	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C80	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C90	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA0	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB0	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC0	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD0	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE0	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF0	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327

HEXADECIMAL - DECIMAL INTEGER CONVERSION TABLE (cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
D00	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D10	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D20	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D30	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D40	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D50	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D60	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D70	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D80	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D90	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA0	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB0	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC0	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD0	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE0	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF0	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583
E00	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E10	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E20	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E30	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E40	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E50	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E60	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E70	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E80	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E90	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA0	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB0	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775
EC0	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791
ED0	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807
EE0	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823
EF0	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839
F00	3840	3841	3842	3843	3844	3845	3846	3847	3848	3849	3850	3851	3852	3853	3854	3855
F10	3856	3857	3858	3859	3860	3861	3862	3863	3864	3865	3866	3867	3868	3869	3870	3871
F20	3872	3873	3874	3875	3876	3877	3878	3879	3880	3881	3882	3883	3884	3885	3886	3887
F30	3888	3889	3890	3891	3892	3893	3894	3895	3896	3897	3898	3899	3900	3901	3902	3903
F40	3904	3905	3906	3907	3908	3909	3910	3911	3912	3913	3914	3915	3916	3917	3918	3919
F50	3920	3921	3922	3923	3924	3925	3926	3927	3928	3929	3930	3931	3932	3933	3934	3935
F60	3936	3937	3938	3939	3940	3941	3942	3943	3944	3945	3946	3947	3948	3949	3950	3951
F70	3952	3953	3954	3955	3956	3957	3958	3959	3960	3961	3962	3963	3964	3965	3966	3967
F80	3968	3969	3970	3971	3972	3973	3974	3975	3976	3977	3978	3979	3980	3981	3982	3983
F90	3984	3985	3986	3987	3988	3989	3990	3991	3992	3993	3994	3995	3996	3997	3998	3999
FA0	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012	4013	4014	4015
FB0	4016	4017	4018	4019	4020	4021	4022	4023	4024	4025	4026	4027	4028	4029	4030	4031
FC0	4032	4033	4034	4035	4036	4037	4038	4039	4040	4041	4042	4043	4044	4045	4046	4047
FD0	4048	4049	4050	4051	4052	4053	4054	4055	4056	4057	4058	4059	4060	4061	4062	4063
FE0	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF0	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095

HEXADECIMAL-DECIMAL FRACTION CONVERSION TABLE

Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal
.00 00 00 00	.00000 00000	.40 00 00 00	.25000 00000	.80 00 00 00	.50000 00000	.C0 00 00 00	.75000 00000
.01 00 00 00	.00390 62500	.41 00 00 00	.25390 62500	.81 00 00 00	.50390 62500	.C1 00 00 00	.75390 62500
.02 00 00 00	.00781 25000	.42 00 00 00	.25781 25000	.82 00 00 00	.50781 25000	.C2 00 00 00	.75781 25000
.03 00 00 00	.01171 87500	.43 00 00 00	.26171 87500	.83 00 00 00	.51171 87500	.C3 00 00 00	.76171 87500
.04 00 00 00	.01562 50000	.44 00 00 00	.26562 50000	.84 00 00 00	.51562 50000	.C4 00 00 00	.76562 50000
.05 00 00 00	.01953 12500	.45 00 00 00	.26953 12500	.85 00 00 00	.51953 12500	.C5 00 00 00	.76953 12500
.06 00 00 00	.02343 75000	.46 00 00 00	.27343 75000	.86 00 00 00	.52343 75000	.C6 00 00 00	.77343 75000
.07 00 00 00	.02734 37500	.47 00 00 00	.27734 37500	.87 00 00 00	.52734 37500	.C7 00 00 00	.77734 37500
.08 00 00 00	.03125 00000	.48 00 00 00	.28125 00000	.88 00 00 00	.53125 00000	.C8 00 00 00	.78125 00000
.09 00 00 00	.03515 62500	.49 00 00 00	.28515 62500	.89 00 00 00	.53515 62500	.C9 00 00 00	.78515 62500
.0A 00 00 00	.03906 25000	.4A 00 00 00	.28906 25000	.8A 00 00 00	.53906 25000	.CA 00 00 00	.78906 25000
.0B 00 00 00	.04296 87500	.4B 00 00 00	.29296 87500	.8B 00 00 00	.54296 87500	.CB 00 00 00	.79296 87500
.0C 00 00 00	.04687 50000	.4C 00 00 00	.29687 50000	.8C 00 00 00	.54687 50000	.CC 00 00 00	.79687 50000
.0D 00 00 00	.05078 12500	.4D 00 00 00	.30078 12500	.8D 00 00 00	.55078 12500	.CD 00 00 00	.80078 12500
.0E 00 00 00	.05468 75000	.4E 00 00 00	.30468 75000	.8E 00 00 00	.55468 75000	.CE 00 00 00	.80468 75000
.0F 00 00 00	.05859 37500	.4F 00 00 00	.30859 37500	.8F 00 00 00	.55859 37500	.CF 00 00 00	.80859 37500
.10 00 00 00	.06250 00000	.50 00 00 00	.31250 00000	.90 00 00 00	.56250 00000	.D0 00 00 00	.81250 00000
.11 00 00 00	.06640 62500	.51 00 00 00	.31640 62500	.91 00 00 00	.56640 62500	.D1 00 00 00	.81640 62500
.12 00 00 00	.07031 25000	.52 00 00 00	.32031 25000	.92 00 00 00	.57031 25000	.D2 00 00 00	.82031 25000
.13 00 00 00	.07421 87500	.53 00 00 00	.32421 87500	.93 00 00 00	.57421 87500	.D3 00 00 00	.82421 87500
.14 00 00 00	.07812 50000	.54 00 00 00	.32812 50000	.94 00 00 00	.57812 50000	.D4 00 00 00	.82812 50000
.15 00 00 00	.08203 12500	.55 00 00 00	.33203 12500	.95 00 00 00	.58203 12500	.D5 00 00 00	.83203 12500
.16 00 00 00	.08593 75000	.56 00 00 00	.33593 75000	.96 00 00 00	.58593 75000	.D6 00 00 00	.83593 75000
.17 00 00 00	.08984 37500	.57 00 00 00	.33984 37500	.97 00 00 00	.58984 37500	.D7 00 00 00	.83984 37500
.18 00 00 00	.09375 00000	.58 00 00 00	.34375 00000	.98 00 00 00	.59375 00000	.D8 00 00 00	.84375 00000
.19 00 00 00	.09765 62500	.59 00 00 00	.34765 62500	.99 00 00 00	.59765 62500	.D9 00 00 00	.84765 62500
.1A 00 00 00	.10156 25000	.5A 00 00 00	.35156 25000	.9A 00 00 00	.60156 25000	.DA 00 00 00	.85156 25000
.1B 00 00 00	.10546 87500	.5B 00 00 00	.35546 87500	.9B 00 00 00	.60546 87500	.DB 00 00 00	.85546 87500
.1C 00 00 00	.10937 50000	.5C 00 00 00	.35937 50000	.9C 00 00 00	.60937 50000	.DC 00 00 00	.85937 50000
.1D 00 00 00	.11328 12500	.5D 00 00 00	.36328 12500	.9D 00 00 00	.61328 12500	.DD 00 00 00	.86328 12500
.1E 00 00 00	.11718 75000	.5E 00 00 00	.36718 75000	.9E 00 00 00	.61718 75000	.DE 00 00 00	.86718 75000
.1F 00 00 00	.12109 37500	.5F 00 00 00	.37109 37500	.9F 00 00 00	.62109 37500	.DF 00 00 00	.87109 37500
.20 00 00 00	.12500 00000	.60 00 00 00	.37500 00000	.A0 00 00 00	.62500 00000	.E0 00 00 00	.87500 00000
.21 00 00 00	.12890 62500	.61 00 00 00	.37890 62500	.A1 00 00 00	.62890 62500	.E1 00 00 00	.87890 62500
.22 00 00 00	.13281 25000	.62 00 00 00	.38281 25000	.A2 00 00 00	.63281 25000	.E2 00 00 00	.88281 25000
.23 00 00 00	.13671 87500	.63 00 00 00	.38671 87500	.A3 00 00 00	.63671 87500	.E3 00 00 00	.88671 87500
.24 00 00 00	.14062 50000	.64 00 00 00	.39062 50000	.A4 00 00 00	.64062 50000	.E4 00 00 00	.89062 50000
.25 00 00 00	.14453 12500	.65 00 00 00	.39453 12500	.A5 00 00 00	.64453 12500	.E5 00 00 00	.89453 12500
.26 00 00 00	.14843 75000	.66 00 00 00	.39843 75000	.A6 00 00 00	.64843 75000	.E6 00 00 00	.89843 75000
.27 00 00 00	.15234 37500	.67 00 00 00	.40234 37500	.A7 00 00 00	.65234 37500	.E7 00 00 00	.90234 37500
.28 00 00 00	.15625 00000	.68 00 00 00	.40625 00000	.A8 00 00 00	.65625 00000	.E8 00 00 00	.90625 00000
.29 00 00 00	.16015 62500	.69 00 00 00	.41015 62500	.A9 00 00 00	.66015 62500	.E9 00 00 00	.91015 62500
.2A 00 00 00	.16406 25000	.6A 00 00 00	.41406 25000	.AA 00 00 00	.66406 25000	.EA 00 00 00	.91406 25000
.2B 00 00 00	.16796 87500	.6B 00 00 00	.41796 87500	.AB 00 00 00	.66796 87500	.EB 00 00 00	.91796 87500
.2C 00 00 00	.17187 50000	.6C 00 00 00	.42187 50000	.AC 00 00 00	.67187 50000	.EC 00 00 00	.92187 50000
.2D 00 00 00	.17578 12500	.6D 00 00 00	.42578 12500	.AD 00 00 00	.67578 12500	.ED 00 00 00	.92578 12500
.2E 00 00 00	.17968 75000	.6E 00 00 00	.42968 75000	.AE 00 00 00	.67968 75000	.EE 00 00 00	.92968 75000
.2F 00 00 00	.18359 37500	.6F 00 00 00	.43359 37500	.AF 00 00 00	.68359 37500	.EF 00 00 00	.93359 37500
.30 00 00 00	.18750 00000	.70 00 00 00	.43750 00000	.B0 00 00 00	.68750 00000	.F0 00 00 00	.93750 00000
.31 00 00 00	.19140 62500	.71 00 00 00	.44140 62500	.B1 00 00 00	.69140 62500	.F1 00 00 00	.94140 62500
.32 00 00 00	.19531 25000	.72 00 00 00	.44531 25000	.B2 00 00 00	.69531 25000	.F2 00 00 00	.94531 25000
.33 00 00 00	.19921 87500	.73 00 00 00	.44921 87500	.B3 00 00 00	.69921 87500	.F3 00 00 00	.94921 87500
.34 00 00 00	.20312 50000	.74 00 00 00	.45312 50000	.B4 00 00 00	.70312 50000	.F4 00 00 00	.95312 50000
.35 00 00 00	.20703 12500	.75 00 00 00	.45703 12500	.B5 00 00 00	.70703 12500	.F5 00 00 00	.95703 12500
.36 00 00 00	.21093 75000	.76 00 00 00	.46093 75000	.B6 00 00 00	.71093 75000	.F6 00 00 00	.96093 75000
.37 00 00 00	.21484 37500	.77 00 00 00	.46484 37500	.B7 00 00 00	.71484 37500	.F7 00 00 00	.96484 37500
.38 00 00 00	.21875 00000	.78 00 00 00	.46875 00000	.B8 00 00 00	.71875 00000	.F8 00 00 00	.96875 00000
.39 00 00 00	.22265 62500	.79 00 00 00	.47265 62500	.B9 00 00 00	.72265 62500	.F9 00 00 00	.97265 62500
.3A 00 00 00	.22656 25000	.7A 00 00 00	.47656 25000	.BA 00 00 00	.72656 25000	.FA 00 00 00	.97656 25000
.3B 00 00 00	.23046 87500	.7B 00 00 00	.48046 87500	.BB 00 00 00	.73046 87500	.FB 00 00 00	.98046 87500
.3C 00 00 00	.23437 50000	.7C 00 00 00	.48437 50000	.BC 00 00 00	.73437 50000	.FC 00 00 00	.98437 50000
.3D 00 00 00	.23828 12500	.7D 00 00 00	.48828 12500	.BD 00 00 00	.73828 12500	.FD 00 00 00	.98828 12500
.3E 00 00 00	.24218 75000	.7E 00 00 00	.49218 75000	.BE 00 00 00	.74218 75000	.FE 00 00 00	.99218 75000
.3F 00 00 00	.24609 37500	.7F 00 00 00	.49609 37500	.BF 00 00 00	.74609 37500	.FF 00 00 00	.99609 37500

HEXADECIMAL - DECIMAL FRACTION CONVERSION TABLE (cont.)

Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal
.00 00 00 00	.00000 00000	.00 40 00 00	.00097 65625	.00 80 00 00	.00195 31250	.00 C0 00 00	.00292 96875
.00 01 00 00	.00001 52587	.00 41 00 00	.00099 18212	.00 81 00 00	.00196 83837	.00 C1 00 00	.00294 49462
.00 02 00 00	.00003 05175	.00 42 00 00	.00100 70800	.00 82 00 00	.00198 36425	.00 C2 00 00	.00296 02050
.00 03 00 00	.00004 57763	.00 43 00 00	.00102 23388	.00 83 00 00	.00199 89013	.00 C3 00 00	.00297 54638
.00 04 00 00	.00006 10351	.00 44 00 00	.00103 75976	.00 84 00 00	.00201 41601	.00 C4 00 00	.00299 07226
.00 05 00 00	.00007 62939	.00 45 00 00	.00105 28564	.00 85 00 00	.00202 94189	.00 C5 00 00	.00300 59814
.00 06 00 00	.00009 15527	.00 46 00 00	.00106 81152	.00 86 00 00	.00204 46777	.00 C6 00 00	.00302 12402
.00 07 00 00	.00010 68115	.00 47 00 00	.00108 33740	.00 87 00 00	.00205 99365	.00 C7 00 00	.00303 64990
.00 08 00 00	.00012 20703	.00 48 00 00	.00109 86328	.00 88 00 00	.00207 51953	.00 C8 00 00	.00305 17578
.00 09 00 00	.00013 73291	.00 49 00 00	.00111 38916	.00 89 00 00	.00209 04541	.00 C9 00 00	.00306 70166
.00 0A 00 00	.00015 25878	.00 4A 00 00	.00112 91503	.00 8A 00 00	.00210 57128	.00 CA 00 00	.00308 22753
.00 0B 00 00	.00016 78466	.00 4B 00 00	.00114 44091	.00 8B 00 00	.00212 09716	.00 CB 00 00	.00309 75341
.00 0C 00 00	.00018 31054	.00 4C 00 00	.00115 96679	.00 8C 00 00	.00213 62304	.00 CC 00 00	.00311 27929
.00 0D 00 00	.00019 83642	.00 4D 00 00	.00117 49267	.00 8D 00 00	.00215 14892	.00 CD 00 00	.00312 80517
.00 0E 00 00	.00021 36230	.00 4E 00 00	.00119 01855	.00 8E 00 00	.00216 67480	.00 CE 00 00	.00314 33105
.00 0F 00 00	.00022 88818	.00 4F 00 00	.00120 54443	.00 8F 00 00	.00218 20068	.00 CF 00 00	.00315 85693
.00 10 00 00	.00024 41406	.00 50 00 00	.00122 07031	.00 90 00 00	.00219 72656	.00 D0 00 00	.00317 38281
.00 11 00 00	.00025 93994	.00 51 00 00	.00123 59619	.00 91 00 00	.00221 25244	.00 D1 00 00	.00318 90869
.00 12 00 00	.00027 46582	.00 52 00 00	.00125 12207	.00 92 00 00	.00222 77832	.00 D2 00 00	.00320 43457
.00 13 00 00	.00028 99169	.00 53 00 00	.00126 64794	.00 93 00 00	.00224 30419	.00 D3 00 00	.00321 96044
.00 14 00 00	.00030 51757	.00 54 00 00	.00128 17382	.00 94 00 00	.00225 83007	.00 D4 00 00	.00323 48632
.00 15 00 00	.00032 04345	.00 55 00 00	.00129 69970	.00 95 00 00	.00227 35595	.00 D5 00 00	.00325 01220
.00 16 00 00	.00033 56933	.00 56 00 00	.00131 22558	.00 96 00 00	.00228 88183	.00 D6 00 00	.00326 53808
.00 17 00 00	.00035 09521	.00 57 00 00	.00132 75146	.00 97 00 00	.00230 40771	.00 D7 00 00	.00328 06396
.00 18 00 00	.00036 62109	.00 58 00 00	.00134 27734	.00 98 00 00	.00231 93359	.00 D8 00 00	.00329 58984
.00 19 00 00	.00038 14697	.00 59 00 00	.00135 80322	.00 99 00 00	.00233 45947	.00 D9 00 00	.00331 11572
.00 1A 00 00	.00039 67285	.00 5A 00 00	.00137 32910	.00 9A 00 00	.00234 98535	.00 DA 00 00	.00332 64160
.00 1B 00 00	.00041 19873	.00 5B 00 00	.00138 85498	.00 9B 00 00	.00236 51123	.00 DB 00 00	.00334 16748
.00 1C 00 00	.00042 72460	.00 5C 00 00	.00140 38085	.00 9C 00 00	.00238 03710	.00 DC 00 00	.00335 69335
.00 1D 00 00	.00044 25048	.00 5D 00 00	.00141 90673	.00 9D 00 00	.00239 56298	.00 DD 00 00	.00337 21923
.00 1E 00 00	.00045 77636	.00 5E 00 00	.00143 43261	.00 9E 00 00	.00241 08886	.00 DE 00 00	.00338 74511
.00 1F 00 00	.00047 30224	.00 5F 00 00	.00144 95849	.00 9F 00 00	.00242 61474	.00 DF 00 00	.00340 27099
.00 20 00 00	.00048 82812	.00 60 00 00	.00146 48437	.00 A0 00 00	.00244 14062	.00 E0 00 00	.00341 79687
.00 21 00 00	.00050 35400	.00 61 00 00	.00148 01025	.00 A1 00 00	.00245 66650	.00 E1 00 00	.00343 32275
.00 22 00 00	.00051 87988	.00 62 00 00	.00149 53613	.00 A2 00 00	.00247 19238	.00 E2 00 00	.00344 84863
.00 23 00 00	.00053 40576	.00 63 00 00	.00151 06201	.00 A3 00 00	.00248 71826	.00 E3 00 00	.00346 37451
.00 24 00 00	.00054 93164	.00 64 00 00	.00152 58789	.00 A4 00 00	.00250 24414	.00 E4 00 00	.00347 90039
.00 25 00 00	.00056 45751	.00 65 00 00	.00154 11376	.00 A5 00 00	.00251 77001	.00 E5 00 00	.00349 42626
.00 26 00 00	.00057 98339	.00 66 00 00	.00155 63964	.00 A6 00 00	.00253 29589	.00 E6 00 00	.00350 95214
.00 27 00 00	.00059 50927	.00 67 00 00	.00157 16552	.00 A7 00 00	.00254 82177	.00 E7 00 00	.00352 47802
.00 28 00 00	.00061 03515	.00 68 00 00	.00158 69140	.00 A8 00 00	.00256 34765	.00 E8 00 00	.00354 00390
.00 29 00 00	.00062 56103	.00 69 00 00	.00160 21728	.00 A9 00 00	.00257 87353	.00 E9 00 00	.00355 52978
.00 2A 00 00	.00064 08691	.00 6A 00 00	.00161 74316	.00 AA 00 00	.00259 39941	.00 EA 00 00	.00357 05566
.00 2B 00 00	.00065 61279	.00 6B 00 00	.00163 26904	.00 AB 00 00	.00260 92529	.00 EB 00 00	.00358 58154
.00 2C 00 00	.00067 13867	.00 6C 00 00	.00164 79492	.00 AC 00 00	.00262 45117	.00 EC 00 00	.00360 10742
.00 2D 00 00	.00068 66455	.00 6D 00 00	.00166 32080	.00 AD 00 00	.00263 97705	.00 ED 00 00	.00361 63330
.00 2E 00 00	.00070 19042	.00 6E 00 00	.00167 84667	.00 AE 00 00	.00265 50292	.00 EE 00 00	.00363 15917
.00 2F 00 00	.00071 71630	.00 6F 00 00	.00169 37255	.00 AF 00 00	.00267 02880	.00 EF 00 00	.00364 68505
.00 30 00 00	.00073 24218	.00 70 00 00	.00170 89843	.00 B0 00 00	.00268 55468	.00 F0 00 00	.00366 21093
.00 31 00 00	.00074 76806	.00 71 00 00	.00172 42431	.00 B1 00 00	.00270 08056	.00 F1 00 00	.00367 73681
.00 32 00 00	.00076 29394	.00 72 00 00	.00173 95019	.00 B2 00 00	.00271 60644	.00 F2 00 00	.00369 26269
.00 33 00 00	.00077 81982	.00 73 00 00	.00175 47607	.00 B3 00 00	.00273 13232	.00 F3 00 00	.00370 78857
.00 34 00 00	.00079 34570	.00 74 00 00	.00177 00195	.00 B4 00 00	.00274 65820	.00 F4 00 00	.00372 31445
.00 35 00 00	.00080 87158	.00 75 00 00	.00178 52783	.00 B5 00 00	.00276 18408	.00 F5 00 00	.00373 84033
.00 36 00 00	.00082 39746	.00 76 00 00	.00180 05371	.00 B6 00 00	.00277 70996	.00 F6 00 00	.00375 36621
.00 37 00 00	.00083 92333	.00 77 00 00	.00181 57958	.00 B7 00 00	.00279 23583	.00 F7 00 00	.00376 89208
.00 38 00 00	.00085 44921	.00 78 00 00	.00183 10546	.00 B8 00 00	.00280 76171	.00 F8 00 00	.00378 41796
.00 39 00 00	.00086 97509	.00 79 00 00	.00184 63134	.00 B9 00 00	.00282 28759	.00 F9 00 00	.00379 94384
.00 3A 00 00	.00088 50097	.00 7A 00 00	.00186 15722	.00 BA 00 00	.00283 81347	.00 FA 00 00	.00381 46972
.00 3B 00 00	.00090 02685	.00 7B 00 00	.00187 68310	.00 BB 00 00	.00285 33935	.00 FB 00 00	.00382 99560
.00 3C 00 00	.00091 55273	.00 7C 00 00	.00189 20898	.00 BC 00 00	.00286 86523	.00 FC 00 00	.00384 52148
.00 3D 00 00	.00093 07861	.00 7D 00 00	.00190 73486	.00 BD 00 00	.00288 39111	.00 FD 00 00	.00386 04736
.00 3E 00 00	.00094 60449	.00 7E 00 00	.00192 26074	.00 BE 00 00	.00289 91699	.00 FE 00 00	.00387 57324
.00 3F 00 00	.00096 13037	.00 7F 00 00	.00193 78662	.00 BF 00 00	.00291 44287	.00 FF 00 00	.00389 09912

Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal
.00 00 00 00	.00000 00000	.00 00 40 00	.00000 38146	.00 00 80 00	.00000 76293	.00 00 C0 00	.00001 14440
.00 00 01 00	.00000 00596	.00 00 41 00	.00000 38743	.00 00 81 00	.00000 76889	.00 00 C1 00	.00001 15036
.00 00 02 00	.00000 01192	.00 00 42 00	.00000 39339	.00 00 82 00	.00000 77486	.00 00 C2 00	.00001 15633
.00 00 03 00	.00000 01788	.00 00 43 00	.00000 39935	.00 00 83 00	.00000 78082	.00 00 C3 00	.00001 16229
.00 00 04 00	.00000 02384	.00 00 44 00	.00000 40531	.00 00 84 00	.00000 78678	.00 00 C4 00	.00001 16825
.00 00 05 00	.00000 02980	.00 00 45 00	.00000 41127	.00 00 85 00	.00000 79274	.00 00 C5 00	.00001 17421
.00 00 06 00	.00000 03576	.00 00 46 00	.00000 41723	.00 00 86 00	.00000 79870	.00 00 C6 00	.00001 18017
.00 00 07 00	.00000 04172	.00 00 47 00	.00000 42319	.00 00 87 00	.00000 80466	.00 00 C7 00	.00001 18613
.00 00 08 00	.00000 04768	.00 00 48 00	.00000 42915	.00 00 88 00	.00000 81062	.00 00 C8 00	.00001 19209
.00 00 09 00	.00000 05364	.00 00 49 00	.00000 43511	.00 00 89 00	.00000 81658	.00 00 C9 00	.00001 19805
.00 00 0A 00	.00000 05960	.00 00 4A 00	.00000 44107	.00 00 8A 00	.00000 82254	.00 00 CA 00	.00001 20401
.00 00 0B 00	.00000 06556	.00 00 4B 00	.00000 44703	.00 00 8B 00	.00000 82850	.00 00 CB 00	.00001 20997
.00 00 0C 00	.00000 07152	.00 00 4C 00	.00000 45299	.00 00 8C 00	.00000 83446	.00 00 CC 00	.00001 21593
.00 00 0D 00	.00000 07748	.00 00 4D 00	.00000 45895	.00 00 8D 00	.00000 84042	.00 00 CD 00	.00001 22189
.00 00 0E 00	.00000 08344	.00 00 4E 00	.00000 46491	.00 00 8E 00	.00000 84638	.00 00 CE 00	.00001 22785
.00 00 0F 00	.00000 08940	.00 00 4F 00	.00000 47087	.00 00 8F 00	.00000 85234	.00 00 CF 00	.00001 23381
.00 00 10 00	.00000 09536	.00 00 50 00	.00000 47683	.00 00 90 00	.00000 85830	.00 00 D0 00	.00001 23977
.00 00 11 00	.00000 10132	.00 00 51 00	.00000 48279	.00 00 91 00	.00000 86426	.00 00 D1 00	.00001 24573
.00 00 12 00	.00000 10728	.00 00 52 00	.00000 48875	.00 00 92 00	.00000 87022	.00 00 D2 00	.00001 25169
.00 00 13 00	.00000 11324	.00 00 53 00	.00000 49471	.00 00 93 00	.00000 87618	.00 00 D3 00	.00001 25765
.00 00 14 00	.00000 11920	.00 00 54 00	.00000 50067	.00 00 94 00	.00000 88214	.00 00 D4 00	.00001 26361
.00 00 15 00	.00000 12516	.00 00 55 00	.00000 50663	.00 00 95 00	.00000 88810	.00 00 D5 00	.00001 26957
.00 00 16 00	.00000 13113	.00 00 56 00	.00000 51259	.00 00 96 00	.00000 89406	.00 00 D6 00	.00001 27553
.00 00 17 00	.00000 13709	.00 00 57 00	.00000 51856	.00 00 97 00	.00000 90003	.00 00 D7 00	.00001 28149
.00 00 18 00	.00000 14305	.00 00 58 00	.00000 52452	.00 00 98 00	.00000 90599	.00 00 D8 00	.00001 28746
.00 00 19 00	.00000 14901	.00 00 59 00	.00000 53048	.00 00 99 00	.00000 91195	.00 00 D9 00	.00001 29342
.00 00 1A 00	.00000 15497	.00 00 5A 00	.00000 53644	.00 00 9A 00	.00000 91791	.00 00 DA 00	.00001 29938
.00 00 1B 00	.00000 16093	.00 00 5B 00	.00000 54240	.00 00 9B 00	.00000 92387	.00 00 DB 00	.00001 30534
.00 00 1C 00	.00000 16689	.00 00 5C 00	.00000 54836	.00 00 9C 00	.00000 92983	.00 00 DC 00	.00001 31130
.00 00 1D 00	.00000 17285	.00 00 5D 00	.00000 55432	.00 00 9D 00	.00000 93579	.00 00 DD 00	.00001 31726
.00 00 1E 00	.00000 17881	.00 00 5E 00	.00000 56028	.00 00 9E 00	.00000 94175	.00 00 DE 00	.00001 32322
.00 00 1F 00	.00000 18477	.00 00 5F 00	.00000 56624	.00 00 9F 00	.00000 94771	.00 00 DF 00	.00001 32918
.00 00 20 00	.00000 19073	.00 00 60 00	.00000 57220	.00 00 A0 00	.00000 95367	.00 00 E0 00	.00001 33514
.00 00 21 00	.00000 19669	.00 00 61 00	.00000 57816	.00 00 A1 00	.00000 95963	.00 00 E1 00	.00001 34110
.00 00 22 00	.00000 20265	.00 00 62 00	.00000 58412	.00 00 A2 00	.00000 96559	.00 00 E2 00	.00001 34706
.00 00 23 00	.00000 20861	.00 00 63 00	.00000 59008	.00 00 A3 00	.00000 97155	.00 00 E3 00	.00001 35302
.00 00 24 00	.00000 21457	.00 00 64 00	.00000 59604	.00 00 A4 00	.00000 97751	.00 00 E4 00	.00001 35898
.00 00 25 00	.00000 22053	.00 00 65 00	.00000 60200	.00 00 A5 00	.00000 98347	.00 00 E5 00	.00001 36494
.00 00 26 00	.00000 22649	.00 00 66 00	.00000 60796	.00 00 A6 00	.00000 98943	.00 00 E6 00	.00001 37090
.00 00 27 00	.00000 23245	.00 00 67 00	.00000 61392	.00 00 A7 00	.00000 99539	.00 00 E7 00	.00001 37686
.00 00 28 00	.00000 23841	.00 00 68 00	.00000 61988	.00 00 A8 00	.00001 00135	.00 00 E8 00	.00001 38282
.00 00 29 00	.00000 24437	.00 00 69 00	.00000 62584	.00 00 A9 00	.00001 00731	.00 00 E9 00	.00001 38878
.00 00 2A 00	.00000 25033	.00 00 6A 00	.00000 63180	.00 00 AA 00	.00001 01327	.00 00 EA 00	.00001 39474
.00 00 2B 00	.00000 25629	.00 00 6B 00	.00000 63776	.00 00 AB 00	.00001 01923	.00 00 EB 00	.00001 40070
.00 00 2C 00	.00000 26226	.00 00 6C 00	.00000 64373	.00 00 AC 00	.00001 02519	.00 00 EC 00	.00001 40666
.00 00 2D 00	.00000 26822	.00 00 6D 00	.00000 64969	.00 00 AD 00	.00001 03116	.00 00 ED 00	.00001 41263
.00 00 2E 00	.00000 27418	.00 00 6E 00	.00000 65565	.00 00 AE 00	.00001 03712	.00 00 EE 00	.00001 41859
.00 00 2F 00	.00000 28014	.00 00 6F 00	.00000 66161	.00 00 AF 00	.00001 04308	.00 00 EF 00	.00001 42455
.00 00 30 00	.00000 28610	.00 00 70 00	.00000 66757	.00 00 B0 00	.00001 04904	.00 00 F0 00	.00001 43051
.00 00 31 00	.00000 29206	.00 00 71 00	.00000 67353	.00 00 B1 00	.00001 05500	.00 00 F1 00	.00001 43647
.00 00 32 00	.00000 29802	.00 00 72 00	.00000 67949	.00 00 B2 00	.00001 06096	.00 00 F2 00	.00001 44243
.00 00 33 00	.00000 30398	.00 00 73 00	.00000 68545	.00 00 B3 00	.00001 06692	.00 00 F3 00	.00001 44839
.00 00 34 00	.00000 30994	.00 00 74 00	.00000 69141	.00 00 B4 00	.00001 07288	.00 00 F4 00	.00001 45435
.00 00 35 00	.00000 31590	.00 00 75 00	.00000 69737	.00 00 B5 00	.00001 07884	.00 00 F5 00	.00001 46031
.00 00 36 00	.00000 32186	.00 00 76 00	.00000 70333	.00 00 B6 00	.00001 08480	.00 00 F6 00	.00001 46627
.00 00 37 00	.00000 32782	.00 00 77 00	.00000 70929	.00 00 B7 00	.00001 09076	.00 00 F7 00	.00001 47223
.00 00 38 00	.00000 33378	.00 00 78 00	.00000 71525	.00 00 B8 00	.00001 09672	.00 00 F8 00	.00001 47819
.00 00 39 00	.00000 33974	.00 00 79 00	.00000 72121	.00 00 B9 00	.00001 10268	.00 00 F9 00	.00001 48415
.00 00 3A 00	.00000 34570	.00 00 7A 00	.00000 72717	.00 00 BA 00	.00001 10864	.00 00 FA 00	.00001 49011
.00 00 3B 00	.00000 35166	.00 00 7B 00	.00000 73313	.00 00 BB 00	.00001 11460	.00 00 FB 00	.00001 49607
.00 00 3C 00	.00000 35762	.00 00 7C 00	.00000 73909	.00 00 BC 00	.00001 12056	.00 00 FC 00	.00001 50203
.00 00 3D 00	.00000 36358	.00 00 7D 00	.00000 74505	.00 00 BD 00	.00001 12652	.00 00 FD 00	.00001 50799
.00 00 3E 00	.00000 36954	.00 00 7E 00	.00000 75101	.00 00 BE 00	.00001 13248	.00 00 FE 00	.00001 51395
.00 00 3F 00	.00000 37550	.00 00 7F 00	.00000 75697	.00 00 BF 00	.00001 13844	.00 00 FF 00	.00001 51991

HEXADECIMAL - DECIMAL FRACTION CONVERSION TABLE (cont.)

Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal
.00 00 00 00	.00000 00000	.00 00 00 40	.00000 00149	.00 00 00 80	.00000 00298	.00 00 00 C0	.00000 00447
.00 00 00 01	.00000 00002	.00 00 00 41	.00000 00151	.00 00 00 81	.00000 00300	.00 00 00 C1	.00000 00449
.00 00 00 02	.00000 00004	.00 00 00 42	.00000 00153	.00 00 00 82	.00000 00302	.00 00 00 C2	.00000 00451
.00 00 00 03	.00000 00006	.00 00 00 43	.00000 00155	.00 00 00 83	.00000 00305	.00 00 00 C3	.00000 00454
.00 00 00 04	.00000 00009	.00 00 00 44	.00000 00158	.00 00 00 84	.00000 00307	.00 00 00 C4	.00000 00456
.00 00 00 05	.00000 00011	.00 00 00 45	.00000 00160	.00 00 00 85	.00000 00309	.00 00 00 C5	.00000 00458
.00 00 00 06	.00000 00013	.00 00 00 46	.00000 00162	.00 00 00 86	.00000 00311	.00 00 00 C6	.00000 00461
.00 00 00 07	.00000 00016	.00 00 00 47	.00000 00165	.00 00 00 87	.00000 00314	.00 00 00 C7	.00000 00463
.00 00 00 08	.00000 00018	.00 00 00 48	.00000 00167	.00 00 00 88	.00000 00316	.00 00 00 C8	.00000 00465
.00 00 00 09	.00000 00020	.00 00 00 49	.00000 00169	.00 00 00 89	.00000 00318	.00 00 00 C9	.00000 00467
.00 00 00 0A	.00000 00023	.00 00 00 4A	.00000 00172	.00 00 00 8A	.00000 00321	.00 00 00 CA	.00000 00470
.00 00 00 0B	.00000 00025	.00 00 00 4B	.00000 00174	.00 00 00 8B	.00000 00323	.00 00 00 CB	.00000 00472
.00 00 00 0C	.00000 00027	.00 00 00 4C	.00000 00176	.00 00 00 8C	.00000 00325	.00 00 00 CC	.00000 00474
.00 00 00 0D	.00000 00030	.00 00 00 4D	.00000 00179	.00 00 00 8D	.00000 00328	.00 00 00 CD	.00000 00477
.00 00 00 0E	.00000 00032	.00 00 00 4E	.00000 00181	.00 00 00 8E	.00000 00330	.00 00 00 CE	.00000 00479
.00 00 00 0F	.00000 00034	.00 00 00 4F	.00000 00183	.00 00 00 8F	.00000 00332	.00 00 00 CF	.00000 00481
.00 00 00 10	.00000 00037	.00 00 00 50	.00000 00186	.00 00 00 90	.00000 00335	.00 00 00 D0	.00000 00484
.00 00 00 11	.00000 00039	.00 00 00 51	.00000 00188	.00 00 00 91	.00000 00337	.00 00 00 D1	.00000 00486
.00 00 00 12	.00000 00041	.00 00 00 52	.00000 00190	.00 00 00 92	.00000 00339	.00 00 00 D2	.00000 00488
.00 00 00 13	.00000 00044	.00 00 00 53	.00000 00193	.00 00 00 93	.00000 00342	.00 00 00 D3	.00000 00491
.00 00 00 14	.00000 00046	.00 00 00 54	.00000 00195	.00 00 00 94	.00000 00344	.00 00 00 D4	.00000 00493
.00 00 00 15	.00000 00048	.00 00 00 55	.00000 00197	.00 00 00 95	.00000 00346	.00 00 00 D5	.00000 00495
.00 00 00 16	.00000 00051	.00 00 00 56	.00000 00200	.00 00 00 96	.00000 00349	.00 00 00 D6	.00000 00498
.00 00 00 17	.00000 00053	.00 00 00 57	.00000 00202	.00 00 00 97	.00000 00351	.00 00 00 D7	.00000 00500
.00 00 00 18	.00000 00055	.00 00 00 58	.00000 00204	.00 00 00 98	.00000 00353	.00 00 00 D8	.00000 00502
.00 00 00 19	.00000 00058	.00 00 00 59	.00000 00207	.00 00 00 99	.00000 00356	.00 00 00 D9	.00000 00505
.00 00 00 1A	.00000 00060	.00 00 00 5A	.00000 00209	.00 00 00 9A	.00000 00358	.00 00 00 DA	.00000 00507
.00 00 00 1B	.00000 00062	.00 00 00 5B	.00000 00211	.00 00 00 9B	.00000 00360	.00 00 00 DB	.00000 00509
.00 00 00 1C	.00000 00065	.00 00 00 5C	.00000 00214	.00 00 00 9C	.00000 00363	.00 00 00 DC	.00000 00512
.00 00 00 1D	.00000 00067	.00 00 00 5D	.00000 00216	.00 00 00 9D	.00000 00365	.00 00 00 DD	.00000 00514
.00 00 00 1E	.00000 00069	.00 00 00 5E	.00000 00218	.00 00 00 9E	.00000 00367	.00 00 00 DE	.00000 00516
.00 00 00 1F	.00000 00072	.00 00 00 5F	.00000 00221	.00 00 00 9F	.00000 00370	.00 00 00 DF	.00000 00519
.00 00 00 20	.00000 00074	.00 00 00 60	.00000 00223	.00 00 00 A0	.00000 00372	.00 00 00 E0	.00000 00521
.00 00 00 21	.00000 00076	.00 00 00 61	.00000 00225	.00 00 00 A1	.00000 00374	.00 00 00 E1	.00000 00523
.00 00 00 22	.00000 00079	.00 00 00 62	.00000 00228	.00 00 00 A2	.00000 00377	.00 00 00 E2	.00000 00526
.00 00 00 23	.00000 00081	.00 00 00 63	.00000 00230	.00 00 00 A3	.00000 00379	.00 00 00 E3	.00000 00528
.00 00 00 24	.00000 00083	.00 00 00 64	.00000 00232	.00 00 00 A4	.00000 00381	.00 00 00 E4	.00000 00530
.00 00 00 25	.00000 00086	.00 00 00 65	.00000 00235	.00 00 00 A5	.00000 00384	.00 00 00 E5	.00000 00533
.00 00 00 26	.00000 00088	.00 00 00 66	.00000 00237	.00 00 00 A6	.00000 00386	.00 00 00 E6	.00000 00535
.00 00 00 27	.00000 00090	.00 00 00 67	.00000 00239	.00 00 00 A7	.00000 00388	.00 00 00 E7	.00000 00537
.00 00 00 28	.00000 00093	.00 00 00 68	.00000 00242	.00 00 00 A8	.00000 00391	.00 00 00 E8	.00000 00540
.00 00 00 29	.00000 00095	.00 00 00 69	.00000 00244	.00 00 00 A9	.00000 00393	.00 00 00 E9	.00000 00542
.00 00 00 2A	.00000 00097	.00 00 00 6A	.00000 00246	.00 00 00 AA	.00000 00395	.00 00 00 EA	.00000 00544
.00 00 00 2B	.00000 00100	.00 00 00 6B	.00000 00249	.00 00 00 AB	.00000 00398	.00 00 00 EB	.00000 00547
.00 00 00 2C	.00000 00102	.00 00 00 6C	.00000 00251	.00 00 00 AC	.00000 00400	.00 00 00 EC	.00000 00549
.00 00 00 2D	.00000 00104	.00 00 00 6D	.00000 00253	.00 00 00 AD	.00000 00402	.00 00 00 ED	.00000 00551
.00 00 00 2E	.00000 00107	.00 00 00 6E	.00000 00256	.00 00 00 AE	.00000 00405	.00 00 00 EE	.00000 00554
.00 00 00 2F	.00000 00109	.00 00 00 6F	.00000 00258	.00 00 00 AF	.00000 00407	.00 00 00 EF	.00000 00556
.00 00 00 30	.00000 00111	.00 00 00 70	.00000 00260	.00 00 00 B0	.00000 00409	.00 00 00 F0	.00000 00558
.00 00 00 31	.00000 00114	.00 00 00 71	.00000 00263	.00 00 00 B1	.00000 00412	.00 00 00 F1	.00000 00561
.00 00 00 32	.00000 00116	.00 00 00 72	.00000 00265	.00 00 00 B2	.00000 00414	.00 00 00 F2	.00000 00563
.00 00 00 33	.00000 00118	.00 00 00 73	.00000 00267	.00 00 00 B3	.00000 00416	.00 00 00 F3	.00000 00565
.00 00 00 34	.00000 00121	.00 00 00 74	.00000 00270	.00 00 00 B4	.00000 00419	.00 00 00 F4	.00000 00568
.00 00 00 35	.00000 00123	.00 00 00 75	.00000 00272	.00 00 00 B5	.00000 00421	.00 00 00 F5	.00000 00570
.00 00 00 36	.00000 00125	.00 00 00 76	.00000 00274	.00 00 00 B6	.00000 00423	.00 00 00 F6	.00000 00572
.00 00 00 37	.00000 00128	.00 00 00 77	.00000 00277	.00 00 00 B7	.00000 00426	.00 00 00 F7	.00000 00575
.00 00 00 38	.00000 00130	.00 00 00 78	.00000 00279	.00 00 00 B8	.00000 00428	.00 00 00 F8	.00000 00577
.00 00 00 39	.00000 00132	.00 00 00 79	.00000 00281	.00 00 00 B9	.00000 00430	.00 00 00 F9	.00000 00579
.00 00 00 3A	.00000 00135	.00 00 00 7A	.00000 00284	.00 00 00 BA	.00000 00433	.00 00 00 FA	.00000 00582
.00 00 00 3B	.00000 00137	.00 00 00 7B	.00000 00286	.00 00 00 BB	.00000 00435	.00 00 00 FB	.00000 00584
.00 00 00 3C	.00000 00139	.00 00 00 7C	.00000 00288	.00 00 00 BC	.00000 00437	.00 00 00 FC	.00000 00586
.00 00 00 3D	.00000 00142	.00 00 00 7D	.00000 00291	.00 00 00 BD	.00000 00440	.00 00 00 FD	.00000 00589
.00 00 00 3E	.00000 00144	.00 00 00 7E	.00000 00293	.00 00 00 BE	.00000 00442	.00 00 00 FE	.00000 00591
.00 00 00 3F	.00000 00146	.00 00 00 7F	.00000 00295	.00 00 00 BF	.00000 00444	.00 00 00 FF	.00000 00593

TABLE OF POWERS OF TWO

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	40	0.000 000 000 000 909 494 701 772 928 237 915 039 062 5
2 199 023 255 552	41	0.000 000 000 000 454 747 350 886 464 118 957 519 531 25
4 398 046 511 104	42	0.000 000 000 000 227 373 675 443 232 059 478 759 765 625
8 796 093 022 208	43	0.000 000 000 000 113 686 837 721 616 029 739 379 882 812 5
17 592 186 044 416	44	0.000 000 000 000 056 843 418 860 808 014 869 689 941 406 25
35 184 372 088 832	45	0.000 000 000 000 028 421 709 430 404 007 434 844 970 703 125
70 368 744 177 664	46	0.000 000 000 000 014 210 854 715 202 003 717 422 485 351 562 5
140 737 488 355 328	47	0.000 000 000 000 007 105 427 357 601 001 858 711 242 675 781 25
281 474 976 710 656	48	0.000 000 000 000 003 552 713 678 800 500 929 355 621 337 890 625
562 949 953 421 312	49	0.000 000 000 000 001 776 356 839 400 250 464 677 810 668 945 312 5
1 125 899 906 842 624	50	0.000 000 000 000 000 888 178 419 700 125 232 338 905 334 472 656 25
2 251 799 813 685 248	51	0.000 000 000 000 000 444 089 209 850 062 616 169 452 667 236 328 125
4 503 599 627 370 496	52	0.000 000 000 000 000 222 044 604 925 031 308 084 726 333 618 164 062 5
9 007 199 254 740 992	53	0.000 000 000 000 000 111 022 302 462 515 654 042 363 166 809 082 031 25
18 014 398 509 481 984	54	0.000 000 000 000 000 055 511 151 231 257 827 021 181 583 404 541 015 625
36 028 797 018 963 968	55	0.000 000 000 000 000 027 755 575 615 628 913 510 590 791 702 270 507 812 5
72 057 594 037 927 936	56	0.000 000 000 000 000 013 877 787 807 814 456 755 295 395 851 135 253 906 25
144 115 188 075 855 872	57	0.000 000 000 000 000 006 938 893 903 907 228 377 647 697 925 567 626 953 125
288 230 376 151 711 744	58	0.000 000 000 000 000 003 469 446 951 953 614 188 823 848 962 783 813 476 562 5
576 460 752 303 423 488	59	0.000 000 000 000 000 001 734 723 475 976 807 094 411 924 481 391 906 738 281 25
1 152 921 504 606 846 976	60	0.000 000 000 000 000 000 867 361 737 988 403 547 205 962 240 695 953 369 140 625
2 305 843 009 213 693 952	61	0.000 000 000 000 000 000 433 680 868 994 201 773 602 981 120 347 976 684 570 312 5
4 611 686 018 427 387 904	62	0.000 000 000 000 000 000 216 840 434 497 100 886 801 490 560 173 988 342 285 156 25
9 223 372 036 854 775 808	63	0.000 000 000 000 000 000 108 420 217 248 550 443 400 745 280 086 994 171 142 578 125

MATHEMATICAL CONSTANTS

Constant	Decimal Value	Hexadecimal Value
π	3.14159 26535 89793	3.243F 6A89
π^{-1}	0.31830 98861 83790	0.517C C1B7
$\sqrt{\pi}$	1.77245 38509 05516	1.C5BF 891C
$\ln \pi$	1.14472 98858 49400	1.250D 048F
e	2.71828 18284 59045	2.B7E1 5163
e^{-1}	0.36787 94411 71442	0.5E2D 58D9
$\sqrt{e}$	1.64872 12707 00128	1.A612 98E2
$\log_{10} e$	0.43429 44819 03252	0.6F2D EC55
$\log_2 e$	1.44269 50408 88963	1.7154 7653
γ	0.57721 56649 01533	0.93C4 67E4
$\ln \gamma$	-0.54953 93129 81645	-0.8CAE 9BC1
$\sqrt{2}$	1.41421 35623 73095	1.6A09 E668
$\ln 2$	0.69314 71805 59945	0.B172 17F8
$\log_{10} 2$	0.30102 99956 63981	0.4D10 4D42
$\sqrt{10}$	3.16227 76601 68379	3.298B 075C
$\ln 10$	2.30258 40929 94046	2.4D76 3777

APPENDIX B. REFERENCE DIAGRAMS

This appendix contains flow diagrams that are intended to illustrate the major operations involved during the execution of instructions by the SIGMA 5 computer. The flow diagrams are not intended to depict actual computer operations and sequences, but the operations and sequences shown are valid representations of the internal computer operations. The symbolic notation used in the flow diagrams is consistent with that used in other portions of this reference manual. The symbolic terms used are:

Term	Meaning
A	An internal CPU register used to hold an operand obtained from the general register that is specified by the R field value in the instruction word.
ADDR	Address – any reference address.
B	An internal CPU register used to hold an operand obtained from the general register that is specified by the value produced by performing a logical OR between the R field of the instruction and the value 1.
C	An internal CPU register used to hold an immediate operand obtained from the instruction, or a byte, halfword, or word operand obtained from the memory (or general register) location specified by the effective address of the instruction. For doubleword operations, the register holds the 32 high-order bits of the effective doubleword.
D	An internal CPU register used to hold the 32 low-order bits of the effective doubleword in a doubleword operation.
EB	Effective byte.
EBL	Effective byte location.
ED	Effective doubleword.
EDL	Effective doubleword location.
EH	Effective halfword.
EHL	Effective halfword location.
EW	Effective word.
EWL	Effective word location.
I	Instruction register.
IA	Instruction address.
IRA	Indirect reference address.
MA	Memory address – an actual core memory address.
OP	Operation code – bits 1-7 of an instruction word.
R	General register address value.
TCC	Trap condition code – the code that is used during the EXCHANGE PROGRAM STATUS DOUBLEWORD (XPSD) instruction.
TYPE	Memory access type – the following values are used to indicate the reason for accessing memory: 0 = write 1 = read
WK	Write key
WL	Write lock
X	Index register designator.

BASIC SIGMA 5 INSTRUCTION EXECUTION CYCLE

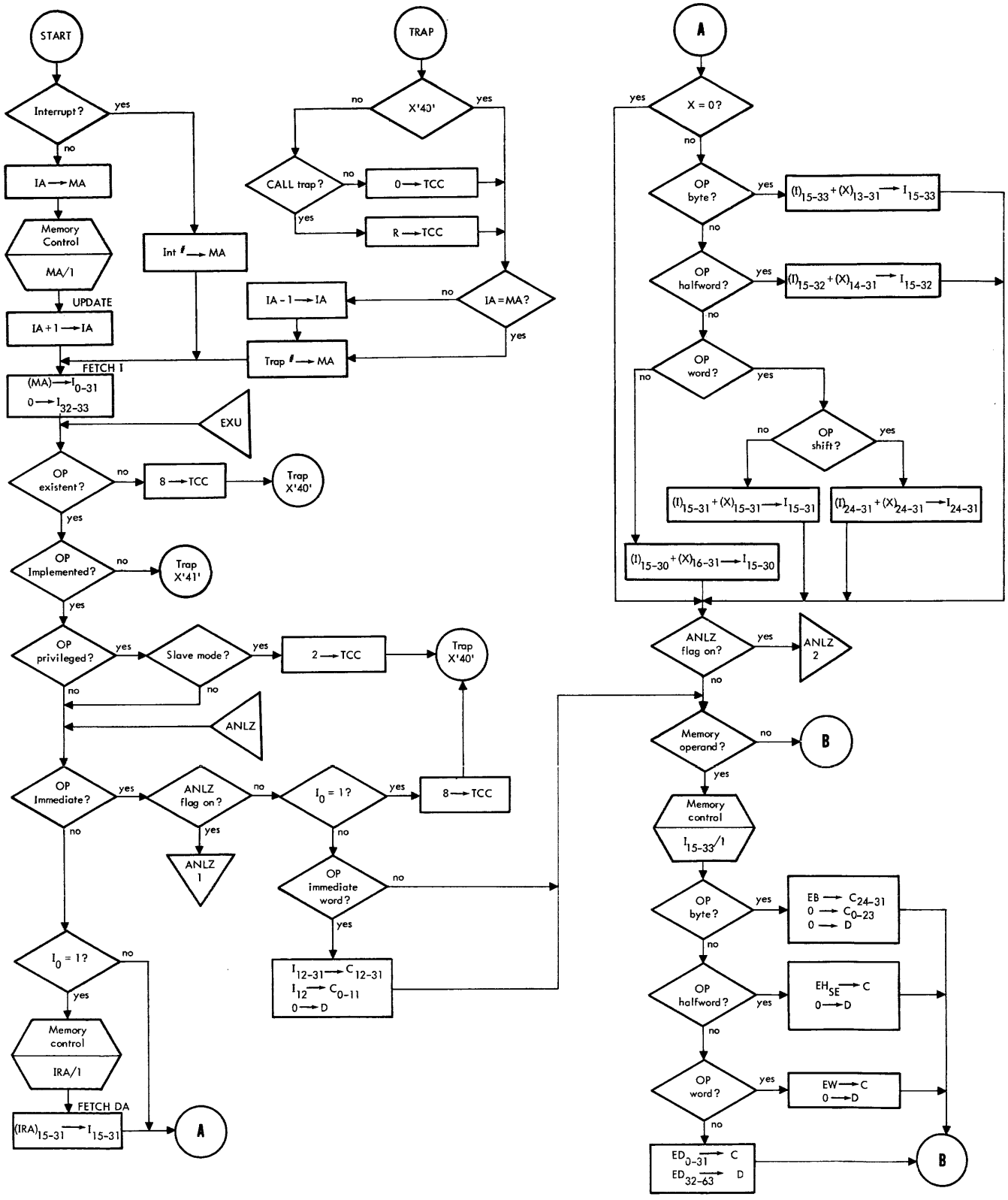
The hexagonal elements in the flow diagram labeled "Memory Control" refer to the memory request process shown at the right of the basic flow diagram. The memory request process is represented as a subroutine with two inputs: an address value (ADDR) and a memory access TYPE, separated by a slash, that correspond to the values shown in the "Memory Control" elements of the basic flow diagram.

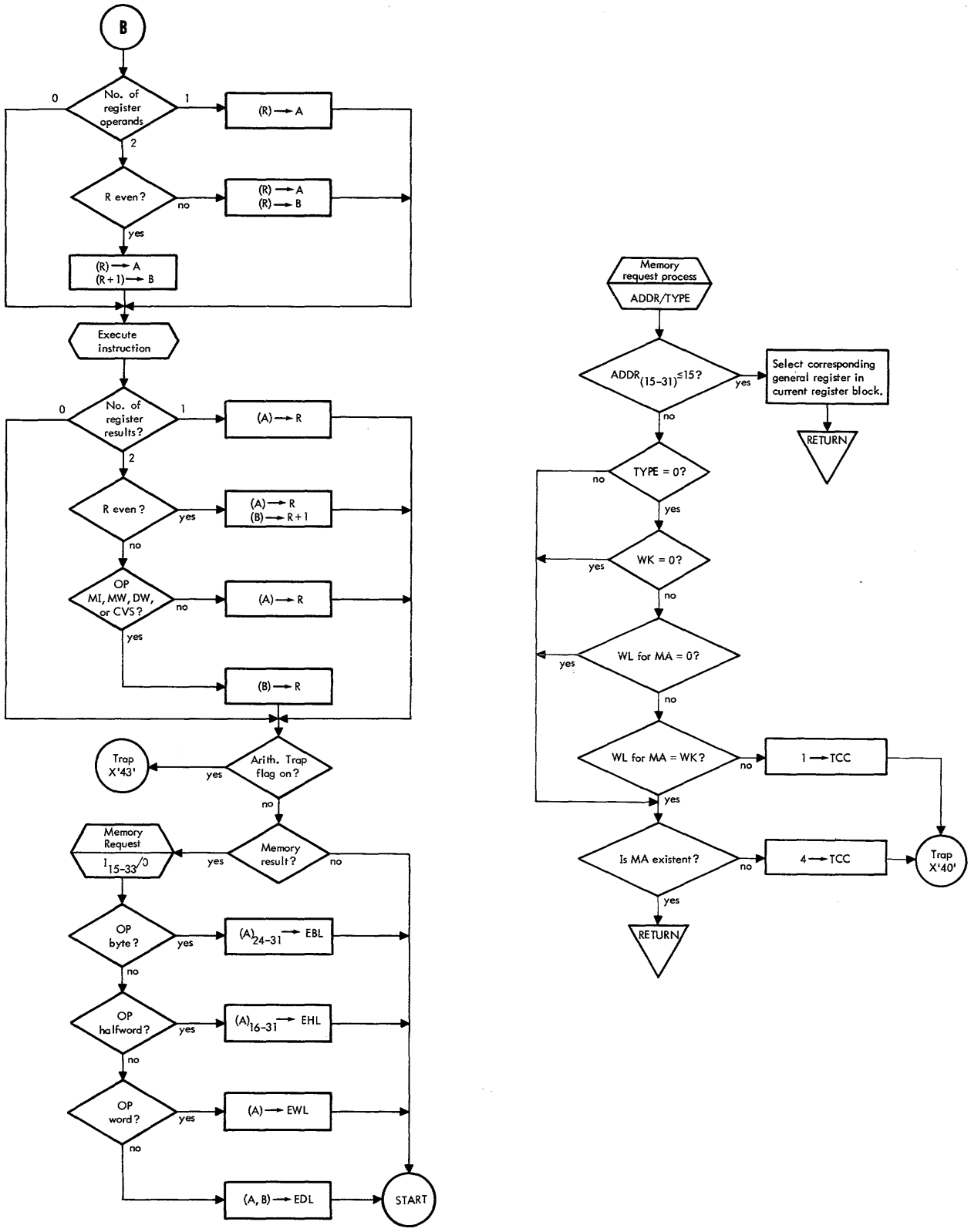
The circular entry point labeled "TRAP" is a continuation of the circular exit points labeled "Trap X'n'", where n is the appropriate trap location.

The triangular entry point labeled "EXU" indicates the point in the basic flow diagram at which an instruction (being executed as an operand of the EXECUTE instruction) is started.

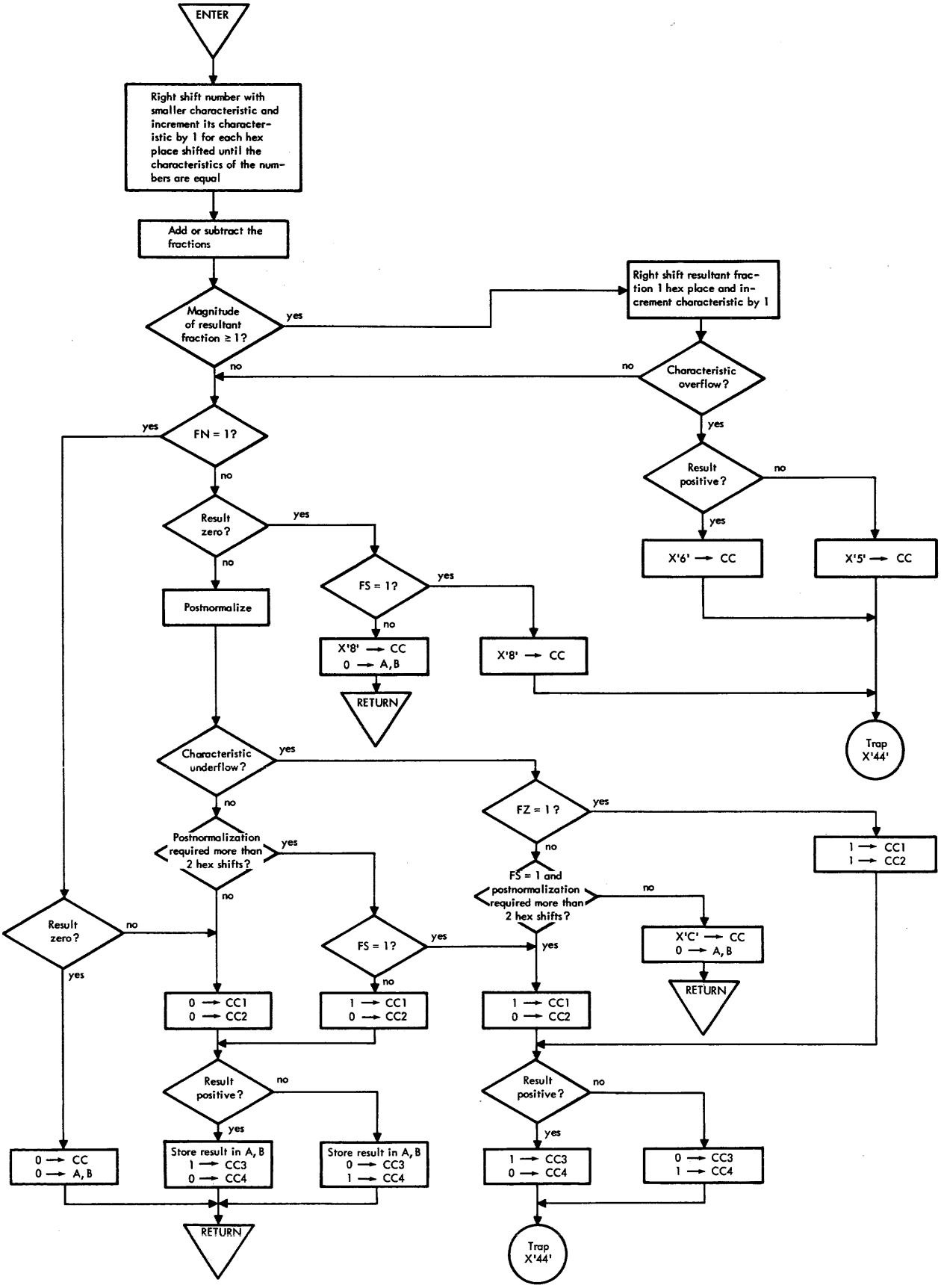
The triangular entry point labeled "ANLZ" indicates the point in the basic flow diagram at which the effective address computation for the instruction being analyzed is started; the triangular exit points indicate the completion of the effective address calculation.

BASIC SIGMA 5 INSTRUCTION EXECUTION CYCLE

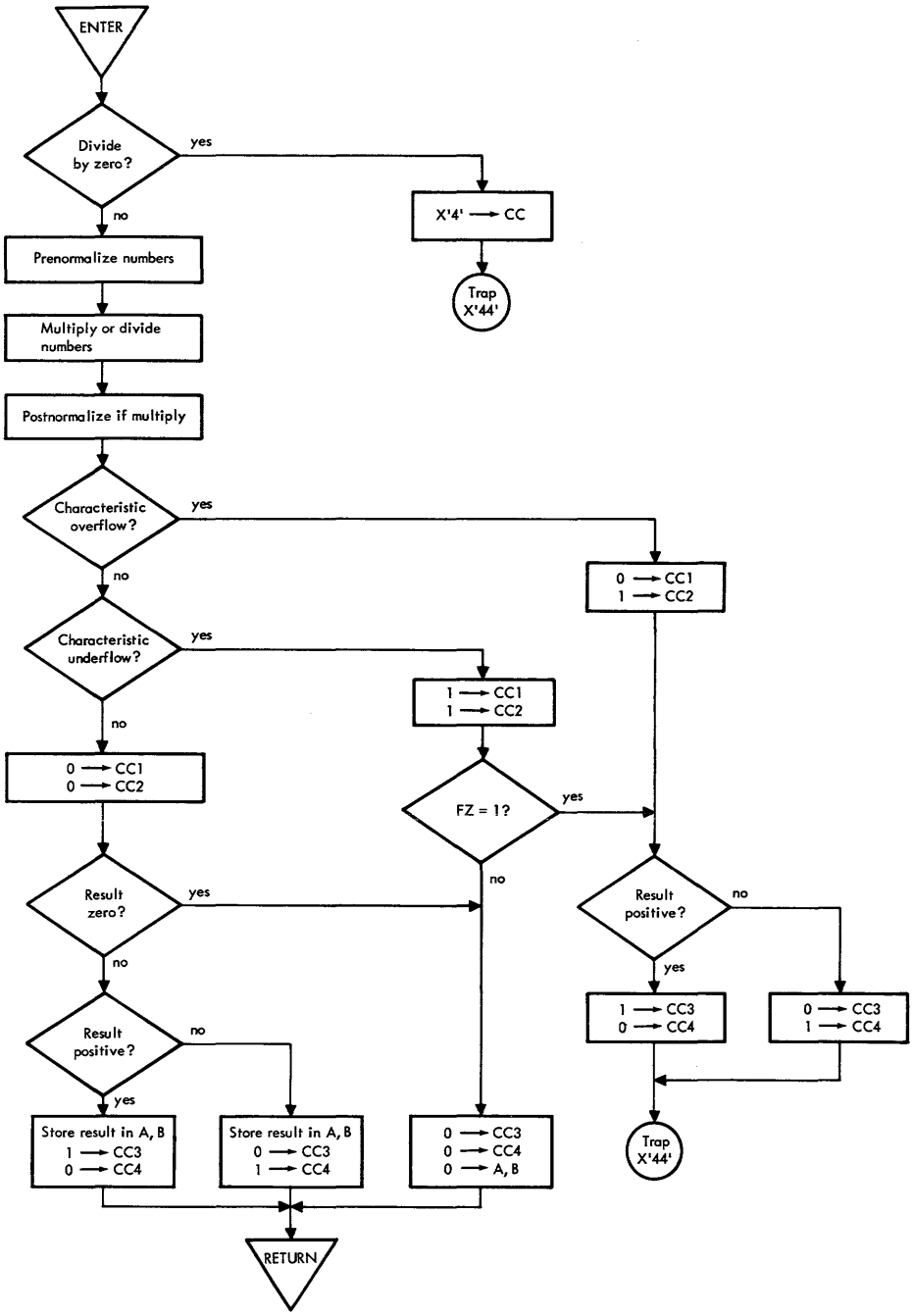



B
No. of register operands
0
1
2
(R) → A
R even?
no
yes
(R) → A
(R) → B
(R) → A
(R+1) → B
Execute instruction
No. of register results?
0
1
2
(A) → R
R even?
yes
no
(A) → R
(B) → R+1
OP MI, MW, DW, or CVS?
no
yes
(A) → R
(B) → R
Arith. Trap flag on?
yes
no
Trap X'43'
Memory Request
I15-33/0
Memory result?
yes
no
OP byte?
yes
no
(A)24-31 → EBL
OP halfword?
yes
no
(A)16-31 → EHL
OP word?
yes
no
(A) → EWL
(A, B) → EDL
START
Memory request process
ADDR/TYPE
ADDR(15-31)≤15?
yes
no
Select corresponding general register in current register block.
RETURN
TYPE = 0?
no
yes
WK = 0?
yes
no
WL for MA = 0?
yes
no
WL for MA = WK?
no
yes
1 → TCC
Is MA existent?
no
yes
4 → TCC
Trap X'40'
RETURN

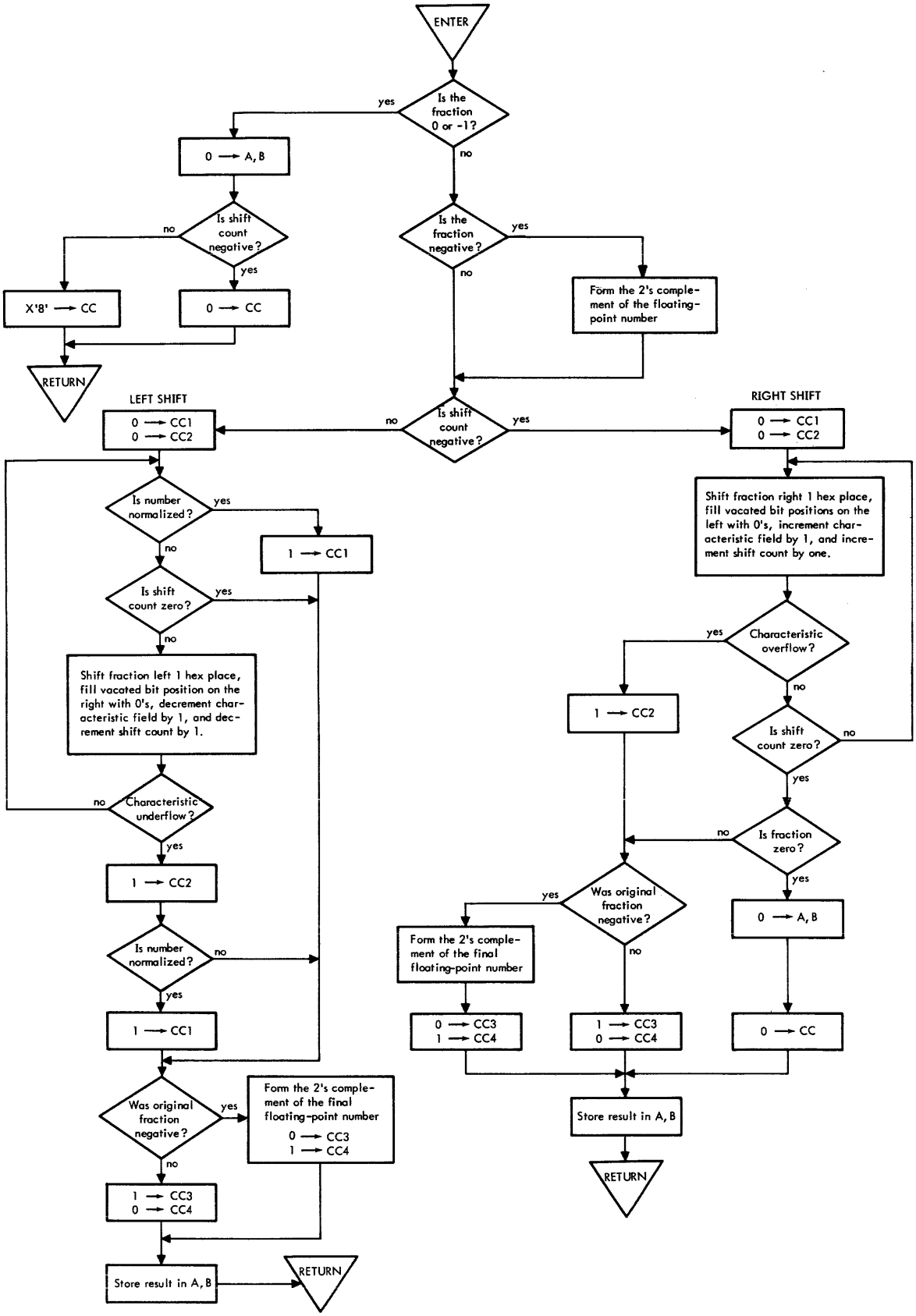
FLOATING-POINT ADDITION AND SUBTRACTION



FLOATING-POINT MULTIPLICATION AND DIVISION



FLOATING-POINT SHIFT



APPENDIX C. INSTRUCTION LIST

Mnemonic	Code	Instruction Name	Addressing Type	Page
AD	10	Add Doubleword	Doubleword	35
AH	50	Add Halfword	Halfword	34
AI	20	Add Immediate	Immediate	34
AIO	6E	Acknowledge Input/Output Interrupt	Word	67
AND	4B	AND Word	Word	41
ANLZ	44	Analyze	Word	32
AW	30	Add Word	Word	34
AWM	66	Add Word to Memory	Word	37
BAL	6A	Branch and Link	Word	55
BCR	68	Branch on Conditions Reset	Word	54
BCS	69	Branch on Conditions Set	Word	54
BDR	64	Branch on Decrementing Register	Word	54
BIR	65	Branch on Incrementing Register	Word	54
CAL1	04	Call 1	Word	55
CAL2	05	Call 2	Word	55
CAL3	06	Call 3	Word	55
CAL4	07	Call 4	Word	55
CB	71	Compare Byte	Byte	39
CD	11	Compare Doubleword	Doubleword	40
CH	51	Compare Halfword	Halfword	39
CI	21	Compare Immediate	Immediate	39
CLM	19	Compare with Limits in Memory	Doubleword	40
CLR	39	Compare with Limits in Register	Word	40
CS	45	Compare Selective	Word	40
CW	31	Compare Word	Word	40
DH	56	Divide Halfword	Halfword	37
DW	36	Divide Word	Word	37
EOR	48	Exclusive OR Word	Word	41
EXU	67	Execute	Word	53
FAL	1D	Floating Add Long	Doubleword	47
FAS	3D	Floating Add Short	Word	47
FDL	1E	Floating Divide Long	Doubleword	48
FDS	3E	Floating Divide Short	Word	48
FML	1F	Floating Multiply Long	Doubleword	48
FMS	3F	Floating Multiply Short	Word	48
FSL	1C	Floating Subtract Long	Doubleword	48
FSS	3C	Floating Subtract Short	Word	47
HIO	4F	Halt Input/Output	Word	66
INT	6B	Interpret	Word	33
LAD	1B	Load Absolute Doubleword	Doubleword	28
LAH	5B	Load Absolute Halfword	Halfword	27
LAW	3B	Load Absolute Word	Word	28
LB	72	Load Byte	Byte	26
LCD	1A	Load Complement Doubleword	Doubleword	28
LCF	70	Load Conditions and Floating Control	Byte	30
LCFI	02	Load Conditions and Floating Control Immediate	Immediate	30
LCH	5A	Load Complement Halfword	Halfword	27
LCW	3A	Load Complement Word	Word	28
LD	12	Load Doubleword	Doubleword	27
LH	52	Load Halfword	Halfword	27
LI	22	Load Immediate	Immediate	26
LM	2A	Load Multiple	Word	29
LPSD	0E	Load Program Status Doubleword	Doubleword	56
LRP	2F	Load Register Pointer	Word	58
LS	4A	Load Selective	Word	29
LW	32	Load Word	Word	27

Mnemonic	Code	Instruction Name	Addressing Type	Page
MH	57	Multiply Halfword	Halfword	36
MI	23	Multiply Immediate	Immediate	36
MMC	6F	Move to Memory Control	Word	58
MSP	13	Modify Stack Pointer	Doubleword	52
MTB	73	Modify and Test Byte	Byte	38
MTH	53	Modify and Test Halfword	Halfword	38
MTW	33	Modify and Test Word	Word	38
MW	37	Multiply Word	Word	37
OR	49	OR Word	Word	41
PLM	0A	Pull Multiple	Word	51
PLW	08	Pull Word	Word	50
PSM	0B	Push Multiple	Word	51
PSW	09	Push Word	Word	50
RD	6C	Read Direct	Word	59
S	25	Shift	Word	41
SD	18	Subtract Doubleword	Doubleword	35
SF	24	Shift Floating	Word	43
SH	58	Subtract Halfword	Halfword	35
SIO	4C	Start Input/Output	Word	63
STB	75	Store Byte	Byte	30
STCF	74	Store Conditions and Floating Control	Byte	32
STD	15	Store Doubleword	Doubleword	31
STH	55	Store Halfword	Halfword	31
STM	2B	Store Multiple	Word	31
STS	47	Store Selective	Word	31
STW	35	Store Word	Word	31
SW	38	Subtract Word	Word	35
TDV	4E	Test Device	Word	67
TIO	4D	Test Input/Output	Word	66
WAIT	2E	Wait	Word	59
WD	6D	Write Direct	Word	60
XPSD	0F	Exchange Program Status Doubleword	Doubleword	56
XW	46	Exchange Word	Word	30

APPENDIX D. SIGMA 5 EXECUTION TIMES

This appendix shows the timing (in microseconds) for executing individual Sigma 5 computer instructions under a variety of circumstances. All of the times are based on the assumption that whenever the CPU requests a service cycle from a particular memory bank, there is never a wait due to other devices (such as IOPs) being connected to that memory bank.

Basic timing information is summarized in Table D-1. A dash entry for any item indicates a nonapplicable or impossible condition for the instruction. Special notes (identified by numbers in the "Notes" column) are given at the end of the table. Execution times shown are for instructions under the most common conditions the user can expect to encounter in his program. The basic timing differences for indexed byte and halfword instructions are due to the alignment of bytes or halfwords in the specified register. For example, to load byte zero into register R, the computer must

1. access the byte from core;
2. align the byte three byte positions to the right;
3. load it into the register.

Also shown are the additional times that must be added to the basic times if the instruction performs a register-to-register operation (i.e., accesses one or more of the general registers for one or more operands or a direct address). The following conditions are assumed:

1. All instructions are in core memory.
2. In the case of an instruction with a direct address, its operand is in one or more of the general registers. For a push-down instruction with a direct address, however, its stack pointer doubleword is in the general registers and the stack is in core memory.
3. In the case of an instruction with an indirect address, the indirect reference is to one of the general registers, which contain the direct address of the operand. For all indirect address references, add 0.16 microseconds to the indirect address execution times. The resultant virtual address is assumed to be a core memory address. For a push-down instruction with an indirect address, therefore, both the stack pointer doubleword and the stack are assumed to be in core memory.

Note: 1. All times are subject to change.

2. Execution times are considered to be on the C port of memory.
3. A + 10% tolerance should be allowed for all execution times.
4. Sigma 5 attains memory overlap in the Push Multiple Instruction only.

BASIC INSTRUCTION TIMING TABLE

Mnemonic	Notes	Direct						Indirect						Additional Times, Register-to-Register Operation
		No Index or Immed	Word Index	Indexing with Byte or Halfword Alignment				No Index or Immed	Word Index	Indexing with Byte or Halfword Alignment				
				HW 0 Byte 0	Byte 1	Byte 2	HW 1 Byte 3			HW 0 Byte 0	Byte 1	Byte 2	HW 1 Byte 3	
AD		2.8	3.5					3.9	4.0					.82
AH		2.8		3.5			2.9	4.0		4.1			3.5	.16
AI		1.8												0
AIO		6.9	7.3					9.1	9.2					0
AND		2.0	2.4					3.1	3.2					.16
ANLZ	minimum	4.3	4.7					5.5	5.6					.16
ANLZ	maximum	5.6	5.9					6.7	6.8					.16
AW		2.0	2.4					3.1	3.2					.16
AWM		3.3	3.7					4.5	4.6					.40
BAL		1.3	1.7					2.4	2.5					.72
BCR BCS	branch	1.2	1.6					2.4	2.5					.72
BCR BCS	no branch	2.0	2.4					3.1	3.2					.72
BDR BIR	branch	1.5	1.8					2.6	2.7					.72
BDR BIR	no branch	2.0	2.4					3.1	3.2					.72
CALL		1.0												0
CB		3.0		3.8	3.5	3.2	2.9	4.2		4.3	4.0	3.8	3.5	.16
CD		2.8	3.5					3.9	4.0					.78
CH		2.8		3.5			2.9	4.0		4.1			3.5	.16
CI		1.8												0
CLM		2.8	3.5					3.9	4.0					.82
CLR		2.7	3.1					3.8	3.9					.16
CS		2.8						3.9	4.0					.16
CW		2.0	2.4					3.1	3.2					.16
DH		16.0		16.5			16.1	17.1		17.2			16.6	.16
DW		15.8	16.2					17.0	17.1					.16
EOR		2.0	2.4					3.1	3.2					.16
EXU		1.4	1.8					2.6	2.7					.54
FAL FSL	minimum	4.9	5.3					6.0	6.1					.78
FAL FSL	maximum	14.8	15.2					15.9	16.0					.78
FAS FSS	minimum	4.9	5.3					6.0	6.1					.16
FAS FSS	maximum	9.5	9.9					10.6	10.7					.16
FDL	minimum	26.7	27.0					27.7	27.8					.78
FDL	maximum	37.2	37.6					38.3	38.4					.78
FDS	minimum	14.4	14.8					15.5	15.6					.16
FDS	maximum	10.0	19.4					20.1	20.2					.16
FML	minimum	15.5	15.9					16.6	16.7					.78
FML	maximum	21.6	22.0					22.7	22.8					.78
FMS	minimum	9.5	9.9					10.6	10.7					.16
FMS	maximum	12.5	12.9					13.6	13.7					.16

BASIC INSTRUCTION TIMING TABLE (Cont.)

Mnemonic	Notes	Direct						Indirect						Additional Times, Register-to-Register Operation
		No Index or Immed	Indexing with Byte or Halfword Alignment					No Index or Immed	Indexing with Byte or Halfword Alignment					
			Word Index	HW 0 Byte 0	Byte 1	Byte 2	HW 1 Byte 3		Word Index	HW 0 Byte 0	Byte 1	Byte 2	HW 1 Byte 3	
HIO	internal	7.8	8.2					10.0	10.1					0
HIO	external	9.7	9.1					11.9	12.0					0
INT		2.6	3.0					3.8	3.9					.16
LAD		3.1	3.8					4.2	4.3					.70
LAH		3.1		3.8			3.2	4.2		4.3			3.8	.16
LAW		2.3	2.6					3.4	3.5					.16
LB		2.9		3.6	3.3	3.0	2.7	4.0		4.1	3.8	3.6	3.3	.16
LCF		2.9		3.6	3.3	3.0	2.7	4.0		4.1	3.8	3.6	3.3	.16
LCD		2.8	3.5					3.9	4.0					.70
LCH		2.6		3.3			2.7	3.7		3.8			3.3	.16
LCFI		1.4												0
LCW		2.0	2.4					3.1	3.2					.16
LD		2.8	3.5					3.9	4.0					.70
LH		2.6		3.3			2.7	3.7		3.8			3.3	.16
LI		1.4												0
LM	1	2.2+ 0.84N	2.6+ 0.84N					3.3+ 0.84N	3.4+ 0.84N					.16N
LRP		2.0	2.4					3.1	3.2					.16
LPSD		3.2	3.6					4.2	4.3					.32
LS		2.8	3.2					3.9	4.0					.16
LW		2.0	2.4					3.1	3.2					.16
MH	minimum	5.3						6.4						.16
MH	maximum	6.1						7.2						.16
MI	minimum	7.2												0
MI	maximum	8.9												0
MMC	1	2.1+ 3.52N												.16N
MSP		6.0	6.4					7.1	7.2					1.18
MTB	R≠0	6.1		6.8	6.2	5.6	5.1	7.2		7.3	6.8	6.2	5.7	.08
MTB	R=0	4.5		5.1	4.8	4.5	4.3	5.6		5.7	5.4	5.1	4.8	.08
MTH	R≠0	5.5		6.2			5.1	6.7		6.8			5.7	.08
MTH	R=0	4.1		4.8			4.3	5.3		5.4				.08
MTW	R≠0	3.6	4.0					4.7	4.8					.40
MTW	R=0	3.1	3.5					4.2	4.3					.40
MW	minimum	7.2	7.6					8.3	8.4					.16
MW	maximum	8.9	9.3					10.0	10.1					.16
OR		2.0	2.4					3.1	3.2					.16
PLM	1	9.8+ 0.84N	10.2+ 0.84N					11.0+ 0.84N	11.1+ 0.84N					1.88
PLW		10.7	11.1					11.8	11.9					1.88
PSM	1	9.7+ 0.84N	10.1+ 0.84N					10.9+ 0.84N	11.0+ 0.84N					1.88
PSW		10.6	11.0					11.7	11.8					1.88
RD	internal	1.8	2.2					2.9	3.0					0
RD	external 2	4.0+D	4.4+D					5.1+D	5.2+D					0
S	left 3	1.1+ .28NB	1.5+ .28NB					2.2+ .28NB	2.3+ .28NB					0

BASIC INSTRUCTION TIMING TABLE (Cont.)

Mnemonic	Notes	Direct						Indirect						Additional Times, Register-to-Register Operation
		No Index or Immed	Indexing with Byte or Halfword Alignment					No Index or Immed	Indexing with Byte or Halfword Alignment					
			Word Index	HW 0 Byte 0	Byte 1	Byte 2	HW 1 Byte 3		Word Index	HW 0 Byte 0	Byte 1	Byte 2	HW 1 Byte 3	
S	right 3	1.1+ .14NB	1.5+ .14NB					2.2+ .14NB	2.3+ .14NB					0
SD		2.8	3.5					3.9	4.0					.82
SF	short left 4	2.3+ 1.1NH	2.7+ 1.1NH					3.4+ 1.1NH	3.5+ 1.1NH					0
SF	short right 4	2.3+ .56NH	2.7+ .56NH					2.4+ .56NH	3.5+ .56NH					0
SF	long left 4	3.0+ 1.1NH	3.4+ 1.1NH					4.1+ 1.1NH	4.2+ 1.1NH					0
SF	long right 4	3.0+ .56NH	3.4+ .56NH					4.1+ .56NH	4.2+ .56NH					0
SH		2.3		3.5			2.9	3.4						.16
SIO	internal	8.5	8.9					10.7	10.8					0
SIO	external	10.6	11.0					12.8	12.9					0
STB		2.8		4.3	4.0	3.7	3.4	3.9		4.9	4.6	4.3	4.0	-.08
STCF		2.8		4.3	4.0	3.7	3.4	3.9		4.9	4.6	4.3	4.0	-.08
STD		3.4	4.0					4.5	4.6					.48
STH		2.8		4.0			3.4	3.9		4.6			4.0	-.08
STM	1	2.0+ 0.84N	2.4+ 0.84N					3.1+ 0.84N	3.2+ 0.84N					.24N
STS		3.5	3.9					4.7	4.8					.24
STW		2.5	2.9					3.6	3.7					.24
SW		2.0	2.4											.16
TDV	internal	7.8	8.2					10.0	10.1					0
TDV	external	9.7	9.1					11.9	12.0					0
TIO	internal	7.8	8.2					10.0	10.1					0
TIO	external	9.7	9.1					11.9	12.0					0
WAIT		1.5	1.9					2.6	2.7					0
WD	internal	1.8	2.2					2.9	3.0					0
WD	external 2	4.0+D	4.4+D					5.1+D	5.2+D					0
XPSD		4.8	5.1					5.9	6.0					.80
XW		3.4	3.7					4.5	4.6					.40

Notes:

1. N = Number of words.
2. D = Delay caused by an external device returning the Function Strobe Acknowledge (FSA), which is the ready/resume signal.
3. NB = Number of bits shifted.
4. NH = Number of Hex (4-bits) positions shifted.

INDEX

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SDS SIGMA 5 BASIC OPERATION CODES

Code	Mnemonic	Instruction Name	Page
02	LCFI	Load Conditions and Floating Control Immediate	30
04	CAL1	Call 1	55
05	CAL2	Call 2	55
06	CAL3	Call 3	55
07	CAL4	Call 4	55
08	PLW	Pull Word	50
09	PSW	Push Word	50
0A	PLM	Pull Multiple	51
0B	PSM	Push Multiple	51
0E	LPSD	Load Program Status Doubleword	56
0F	XPSD	Exchange Program Status Doubleword	56
10	AD	Add Doubleword	35
11	CD	Compare Doubleword	40
12	LD	Load Doubleword	27
13	MSP	Modify Stack Pointer	52
15	STD	Store Doubleword	31
18	SD	Subtract Doubleword	35
19	CLM	Compare with Limits in Register	40
1A	LCD	Load Complement Doubleword	28
1B	LAD	Load Absolute Doubleword	28
1C	FSL	Floating Subtract Long (optional)	48
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1E	FDL	Floating Divide Long (optional)	48
1F	FML	Floating Multiply Long (optional)	48
20	AI	Add Immediate	34
21	CI	Compare Immediate	39
22	LI	Load Immediate	26
23	MI	Multiply Immediate	36
24	SF	Shift Floating	43
25	S	Shift	41
2A	LM	Load Multiple	29
2B	STM	Store Multiple	31
2E	WAIT	Wait	59
2F	LRP	Load Register Pointer	58
30	AW	Add Word	34
31	CW	Compare Word	40
32	LW	Load Word	27
33	MTW	Modify and Test Word	38
35	STW	Store Word	31
36	DW	Divide Word	37
37	MW	Multiply Word	37
38	SW	Subtract Word	35
39	CLR	Compare with Limits in Register	40
3A	LCW	Load Complement Word	28
3B	LAW	Load Absolute Word	28
3C	FSS	Floating Subtract Short (optional)	47
3D	FAS	Floating Add Short (optional)	47
3E	FDS	Floating Divide Short (optional)	48
3F	FMS	Floating Multiply Short (optional)	48
44	ANLZ	Analyze	32
45	CS	Compare Selective	40
46	XW	Exchange Word	30
47	STS	Store Selective	31
48	EOR	Exclusive OR Word	41
49	OR	OR Word	41
4A	LS	Load Selective	29
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4D	TIO	Test Input/Output	65
4E	TDV	Test Device	67
4F	HIO	Halt Input/Output	66
50	AH	Add Halfword	34
51	CH	Compare Halfword	39
52	LH	Load Halfword	27
53	MTH	Modify and Test Halfword	38
55	STH	Store Halfword	31
56	DH	Divide Halfword	37
57	MH	Multiply Halfword	36
58	SH	Subtract Halfword	35
5A	LCH	Load Complement Halfword	27
5B	LAH	Load Absolute Halfword	27
64	BDR	Branch on Decrementing Register	54
65	BIR	Branch on Incrementing Register	54
66	AWM	Add Word to Memory	37
67	EXU	Execute	53
68	BCR	Branch on Conditions Reset	54
69	BCS	Branch on Conditions Set	54
6A	BAL	Branch and Link	55
6B	INT	Interpret	33
6C	RD	Read Direct	59
6D	WD	Write Direct	60
6E	AIO	Acknowledge Input/Output Interrupt	67
6F	MMC	Move to Memory Control	58
70	LCF	Load Conditions and Floating Control	30
71	CB	Compare Byte	39
72	LB	Load Byte	26
73	MTB	Modify and Test Byte	38
74	STCF	Store Conditions and Floating Control	32
75	STB	Store Byte	30

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