Reference Manual
October 1984
P/N 39409-1

Shugart 455/465
Flexible Disk
Storage Drive

Shugart

Shugart 455/465 Flexible Disk Storage Drive

Reference Manual

For
Half-Height
Double-Sided
Minifloppy™
Applications

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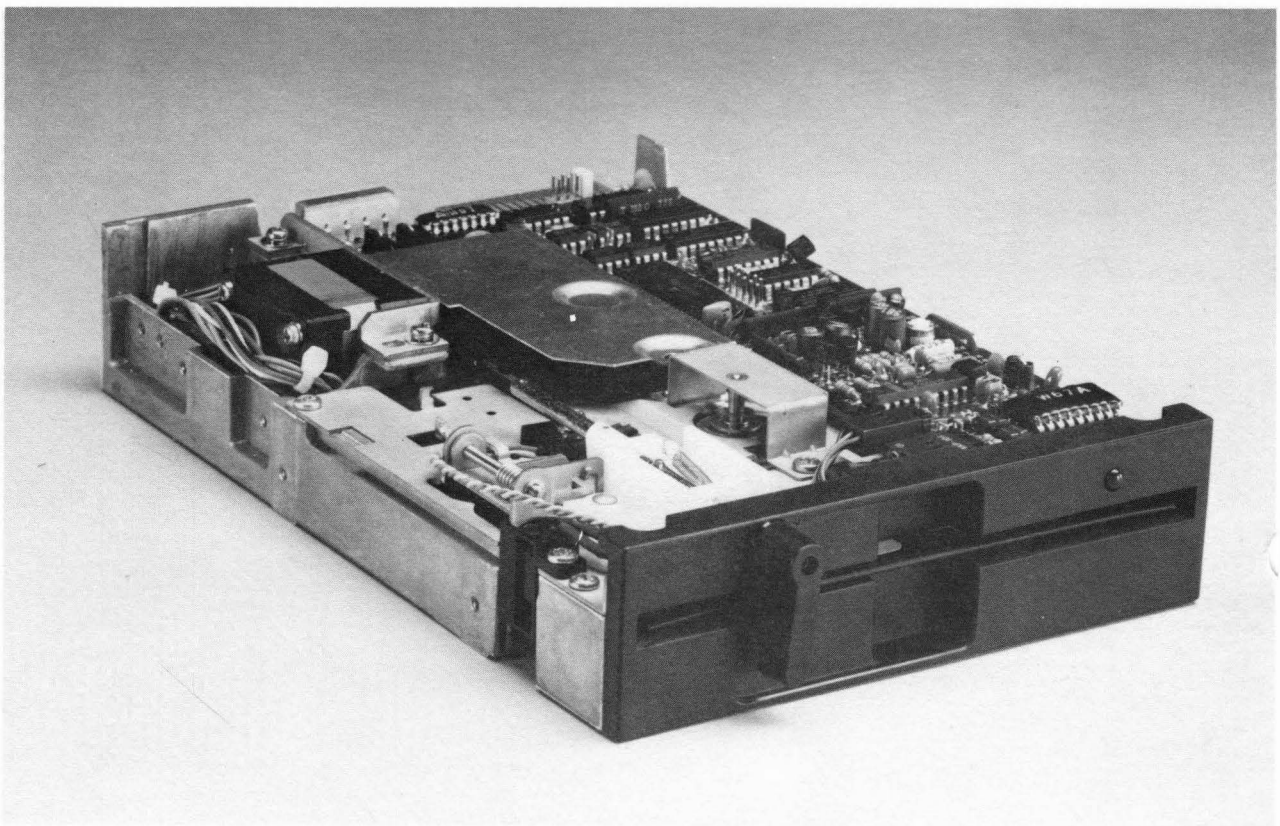

FIGURE 1-1. SHUGART 455/465

LIST OF TABLES

ABBREVIATIONS/MNEMONICS

AM	Address Mark	**NRZ**	Non Return to Zero
bpi	Bits Per Inch	**PCB**	Printed Circuit Board
CRC	Cyclic Redundancy Check	**PM**	Preventive Maintenance
fci	Flux Changes Per Inch	**POH**	Power On Hours
FM	Frequency Modulation	**PSI**	Product Selection Index
GND	Ground	**TP**	Test Point
ID	Index	**tpi**	Tracks Per Inch
I/O	Input/Output	**TRK**	Track
MFM	Modified FM	**WG OFF**	Write Gate Off
MTBF	Mean Time Between Failures	**1F**	Single Density
MTTR	Mean Time to Repair	**2F**	Double Density

NOTICE TO USERS

This manual P/N 39409-1, replaces the 455/465 Preliminary manual, P/N 39409-0, published in June 1984. All technical changes have been indicated with a change bar in the text margin or a star symbol in the illustration.

While every effort has been made to ensure that the information provided herein is correct, please notify us in the event of an error or inconsistency. Make any comments on the Technical Publication Suggestion forms provided on the back of this manual. If the forms have already been used, write your comments, include your name, address, and telephone number and mail to:

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SECTION I
INTRODUCTION

1.1 PURPOSE

This manual for the Shugart 455/465 disk drives is designed as a reference source for the OEM engineers, system integrators, maintenance technicians, and knowledgeable end users.

This document contains all the information that is normally required to integrate the Shugart 455/465 disk drives into a system. It also contains the depot level maintenance information that is necessary to maintain, troubleshoot, and repair the product. It is recommended that the maintenance and service be performed only by trained personnel.

1.2 GENERAL DESCRIPTION

The Shugart 455/465 Minifloppy™ disk drives are half-height, double-sided disk drives. These provide up to four times the on-line storage capacity and faster access time of full-height Shugart minifloppy drives. The 455/465 read and write in single and double density on both sides of a standard 5.25-inch diskette. In addition, these are plug compatible with the Shugart 400, 410/460, and 450 disk drives.

The standard features of the 455/465 include: compact size; a weight of 3.3 pounds (1.5 kg); low heat dissipation; dc drive motor; band positioner; proprietary glass-bonded ferrite/ceramic read/write heads, and internal write protect circuitry.

Typical applications for the 455/465 are: word processing systems; entry level microprocessor systems; intelligent calculators; program storage; low end computer systems, and other applications where low cost random access data storage is required.

The 455/465 has been listed with Underwriters Laboratories, Inc., (E55114(S)) and the Canadian Standards Association (LR55467-1 and LR55468-1).

Key Features

- 0.5 Mbytes (455) or 1.0 Mbytes (465) storage capacity (unformatted)
- 3 (455) or 6 (465) msec track-to-track access time
- 125/250 kbits/second data transfer rate
- DC drive motor that eliminates ac requirements

1.3 SPECIFICATIONS SUMMARY

1.3.1 Performance Specifications

	455 (40 Track)		465 (80 Track)	
Capacity (in bytes)	Single Density (FM)	Double Density (MFM)	Single Density (FM)	Double Density (MFM)
Unformatted				
Per Disk	250,000	500,000	500,000	1,000,000
Per Surface	125,000	250,000	250,000	500,000
Per Track	3,125	6,250	3,125	6,250
Formatted (16 Records/Track)				
Per Disk	163,840	327,680	327,680	655,360
Per Track	2,048	4,096	2,048	4,096
Per Sector	128	256	128	256

	455 (40 Track)		465 (80 Track)	
	Single Density	Double Density	Single Density	Double Density
Formatted (10 Records/Track)				
Per Disk	204,800	409,600	409,600	819,200
Per Track	2,560	5,120	2,560	5,120
Per Sector	256	512	256	512
Transfer Rate	125 kbits/sec	250 kbits/sec	125 kbits/sec	250 kbits/sec
Latency (avg.)	100 msec	100 msec	100 msec	100 msec
Access Time				
Track to Track	6 msec	6 msec	3 msec	3 msec
Average	93 msec	93 msec	94 msec	94 msec
Settling Time	15 msec	15 msec	15 msec	15 msec

1.3.2 Functional Specifications

Typical Motor Start Time	300 msec	300 msec	300 msec	300 msec
Worst Case Motor Start Time	500 msec	500 msec	500 msec	500 msec
Rotational Speed	300 rpm	300 rpm	300 rpm	300 rpm
Recording Density	2938 bpi	5876 bpi	2961 bpi	5922 bpi
Flux Density	5876 fci	5876 fci	5922 fci	5922 fci
Track Density	48 tpi	48 tpi	96 tpi	96 tpi
Media Requirements				
Soft-sectored	Shugart 154	Shugart 154	Shugart 164	Shugart 164
16 sectors hard-sectored	Shugart 155	Shugart 155	Shugart 165	Shugart 165
10 sectors hard-sectored	Shugart 157	Shugart 157	Shugart 167	Shugart 167

Industry standard flexible diskette
Oxide on 0.003 in. (0.08 mm) Mylar
5.25 in. (133.4 mm) square jacket

1.3.3 Physical Specifications

Environmental Limits	Operating	Shipping	Storage
Ambient Temperature	50° to 115°F (10.0° to 46.1°C)	-40° to 144°F (-40° to 62.2°C)	-8° to 117°F -22.2° to 47.2°C)
Relative Humidity	20 to 80%	1 to 95%	1 to 95%
Maximum Wet Bulb	78°F (25.6°C)	No Condensation	No Condensation
Shock	0.5G 10 msec	35G 10 msec	15G 10 msec
Vibration	0.5G 5-600Hz	3G 5-600 Hz	3G 5-600 Hz

DC Voltage Requirements
+12 V ± 10% @ 1.2 A (max), 0.6 A (typ), 100 mV ripple
+5 V ± 5% @ 0.9 A (max), 0.6 A (typ), 50 mV ripple

Mechanical Dimensions (exclusive of front panel)
Width = 5.75 inches (146.1 mm)
Height = 1.62 inches (41.1 mm)
Depth = 7.96 inches (202.0 mm)
Weight = 3.3 lbs (1.5 kg)
Power Dissipation = 9.6 Watts (34.0 BTU) continuous typical
3.6 Watts (13.5 BTU) standby

NOTE

Standby: Drive motor off, drive select off, and stepper at reduced current.

1.3.4 Reliability Specifications

MTBF: 10,000 POH under typical usage.
PM: Not required.
MTTR: 30 minutes.

Error Rates:
Soft Read Errors: 1 per 10^9 bits read.
Hard Read Errors: 1 per 10^{12} bits read.
Seek Errors: 1 per 10^6 seeks

Media Life:
Passes per Track: 3.0×10^6
Insertions: 30,000+

1.4 FUNCTIONAL CHARACTERISTICS

The 455/465 consist of read/write and control electronics, drive mechanism, read/write heads, and precision track positioning mechanism. These components performs the following functions:

a. Interpret and generate control signals.

b. Move read/write heads to the desired track.

c. Read and write data.

The interface signals and their relationship to the internal functions are shown in figure 1-2.

1.4.1 Read/Write and Control Electronics

The electronics package contains:

a. Index detector circuits

b. Head position actuator driver

c. Read/write amplifier and transition detector

d. Write protect detector

e. Drive select circuit

f. Drive motor control

1.4.2 Drive Mechanism

The dc drive motor under servo speed control (using an integral tachometer) rotates the spindle at 300 rpm through a direct drive system. An expandable collet/spindle assembly provides precision media positioning to ensure data interchange.

1.4.3 Positioning Mechanics

The read/write head assembly is accurately positioned through the use of a band positioner which is attached to the head carriage assembly. Precise track location is accomplished as this positioner is rotated in discrete increments by a stepping motor.

1.4.4 Read/Write Heads

The proprietary heads are a single element glass-bonded ceramic read/write, with tunnel erase elements to provide erased areas between data tracks. The normal interchange tolerances between media and drives will not degrade the signal-to-noise ratio and diskette interchangeability is ensured.

The read/write heads are mounted on a carriage which is located on precision carriage ways. The diskette is held in a plane perpendicular to the read/write heads by a platen located on the base casting. This precise registration assures perfect compliance with the read/write heads. The read/write heads are in direct contact with the diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the diskette with minimum head/diskette wear.

1.4.5 Recording Formats

The formats of the data recorded on the diskette are totally a function of the host system. These formats can be designed around the user's application to take maximum advantage of the total available bits that can be written on any one track. Refer to Section VI for details.

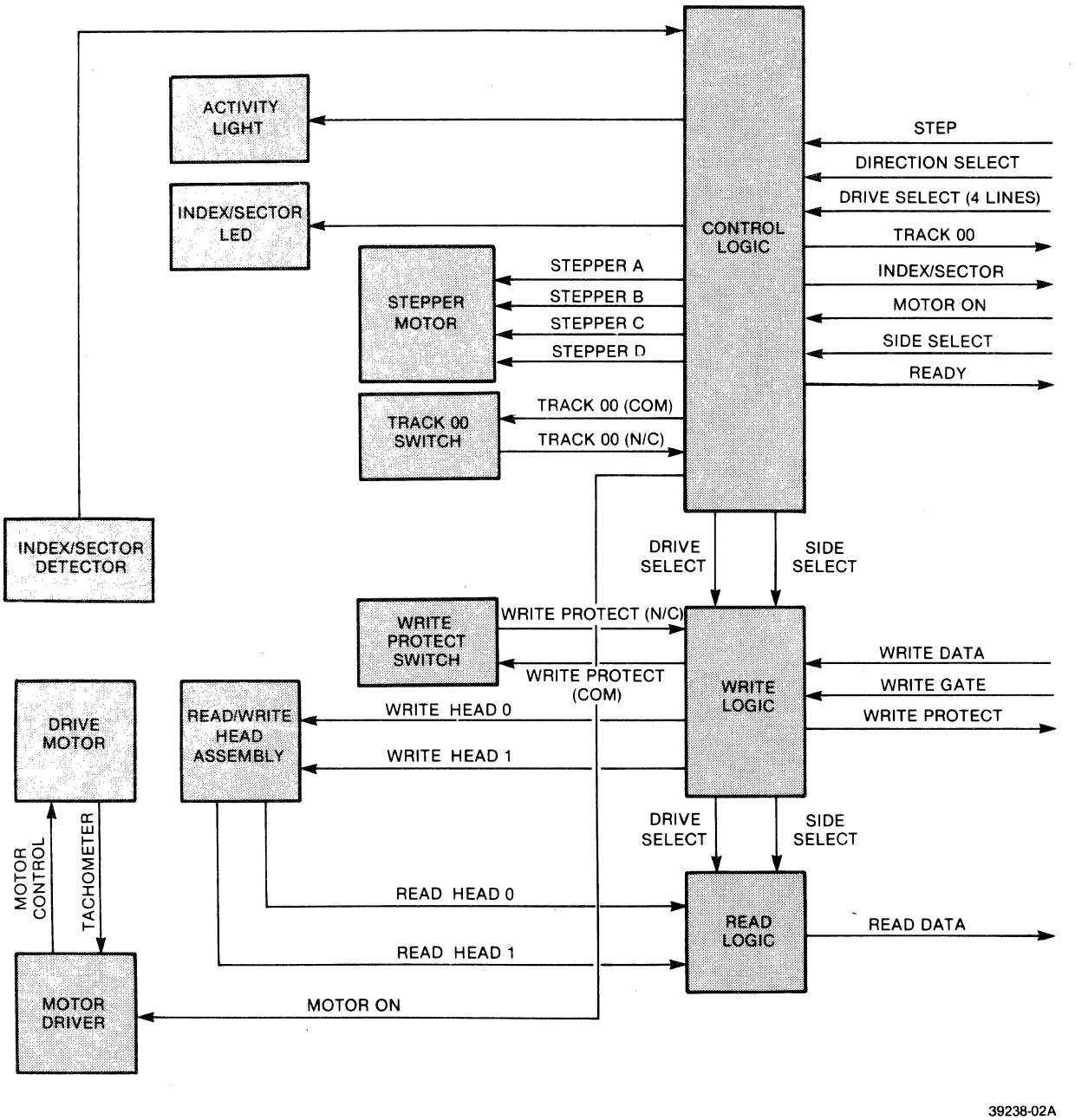


FIGURE 1-2. 455/465 FUNCTIONAL DIAGRAM

1.5 RECOMMENDED INCOMING INSPECTION

1.5.1 Necessary Equipment

Although all Shugart drives are 100 percent adjusted and tested before leaving the factory, incomming inspection may be done at the buyers discretion to inspect for shipping damage. For this purpose Shugart recommends the following incomming inspection procedure. The inspection is simple and the test equipment is kept to a minimum. The following equipment is recommended:

a. Shugart 809 Exerciser (P/N 54157)

b. Exerciser Instruction Manual (P/N 50686)

c. Power supply for Exerciser and Drive (+5, +12 V)

d. Oscilloscope

e. Shugart 128/126 Alignment diskettes

f. Shugart 455/465 Reference Manual (P/N 39409-0)

g. Shugart 154/164 diskettes

1.5.2 Procedure

1. Unpack drive and inspect for physical shipping damage. (If shipping damage is found, see note below).
2. Check the contents of the container against the packing slip.
3. Make sure all power is off.
4. Attach exerciser cables to appropriate drive connectors.
5. Power up.
6. Insert alignment diskette (Shugart 128 for 455 and Shugart 126 for 465).
7. Set track addresses of 00 and 39 (455) or 00 and 79 (465) into exerciser.
8. Select drive.
9. Start motor and let the drive seek automatically for five minutes.
10. Check that activity light is on.
11. Using 455/465 Reference Manual and the Exerciser Manual as guides, perform the following checks:
    - Index Timing Adjustment (refer to paragraph 10.4.5).
    - Head Radial Alignment, side 0 and 1 (refer to paragraph 10.4.1).
    - Ensure that Track 0 switch is on at track 00 and off at 01 and 02.
12. Remove alignment diskette and insert Shugart 154/164 diskette.
13. Seek to track 39 (455) or track 79 (465), and write a 2F signal. Minimum read back should be 90 mV.
14. Check write protect sensor adjustment (refer to paragraph 10.4.8 for test point locations).

15. Power off.

16. Remove connectors.

This procedure verifies that the critical functions of the drive are working properly (i.e., the drive will read and write, the diskette will rotate at the proper speed, and critical adjustments are within specifications).

NOTE

Inspect all containers for shipping damage. If the containers are damaged, the contents should be checked and units verified electrically. If a unit is found damaged inside the packaging container without outside damage, call the nearest Shugart Corporation Customer Service Center. If the unit is damaged due to mishandling during shipping, call the freight service. Please retain all shipping labels and documents.

1.6 FUNCTIONAL OPERATIONS

1.6.1 Power Sequencing

Applying dc power to the drive(s) can be done in any sequence. However, during power up, the WRITE GATE line must be held inactive or at a high level. This will prevent possible "glichting" of the media. After application of dc power, a 100 msec delay should be introduced before any operation is performed. After powering on, initial position of the read/write heads with respect to the data tracks on the media is indeterminant. In order to assure proper positioning of the read/write heads after power on, a Step Out operation should be performed until the TRACK 00 line becomes active (Recalibrate).

1.6.2 Drive Selection

Drive selection occurs when the proper DRIVE SELECT line is activated. With this line jumpered, the drive will respond to input lines or gate output lines.

1.6.3 Motor On

For the host system to read or write data, the dc drive motor must be turned on. This is accomplished by activating the line -MOTOR ON. A 500 msec delay must be introduced after activating this line or the Ready line must be monitored to allow the motor to come up to speed before reading or writing can be accomplished.

The motor must be turned off by the host system by deactivating the MOTOR ON line. The control electronics keep the motor active for three seconds, after MOTOR ON is deactivated. This allows reselecting during copy operations and will ensure maximum motor and media life.

1.6.4 Track Accessing

Seeking the read/write heads from one track to another is accomplished by:

a. Activating the DRIVE SELECT line.

b. Selecting desired direction using the DIRECTION SELECT line.

c. WRITE GATE being inactive.

d. Pulsing the STEP line.

Multiple track accessing is accomplished by repeated pulsing of the STEP line (with direction valid) until the desired track has been reached. Each pulse on the STEP line will cause the read/write heads to move one track either in or out depending on the DIRECTION SELECT line. Head movement is initiated on the trailing edge of the step pulse.

1.6.5 Step Out

With the DIRECTION SELECT line at a plus logic level (2.4 to 5.25 V), a pulse on the STEP line will cause the read/write heads to move one track closer to the center of the disk. The pulse(s) applied to the STEP line must have the timing characteristics shown in figures 1-3 and 1-4.

1.6.6 Side Selection

Head selection is controlled via the I/O signal line designated SIDE SELECT. A plus logic level on the SIDE SELECT line selects the read/write head on the side 0 surface of the diskette. A minus logic level selects the side 1 read/write head. When switching from one side to the other, a 100 μsec delay is required after SIDE SELECT changes state before a read or write operation can be initiated. Figure 1-5 shows the use of SIDE SELECT prior to a read operation.

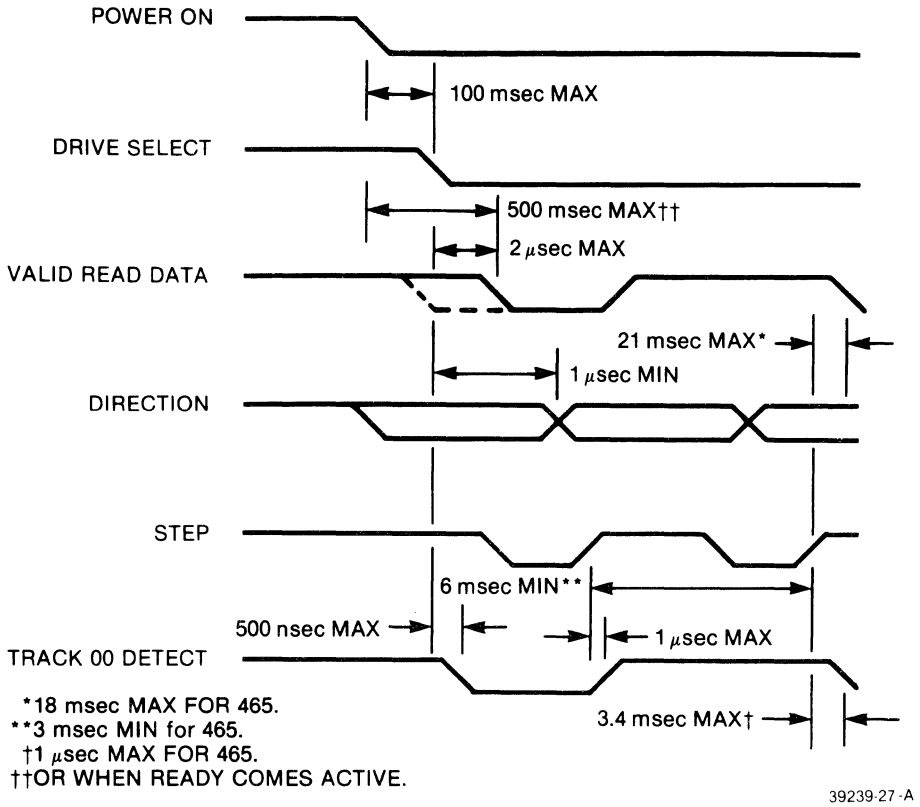


FIGURE 1-3. STEP TO READ

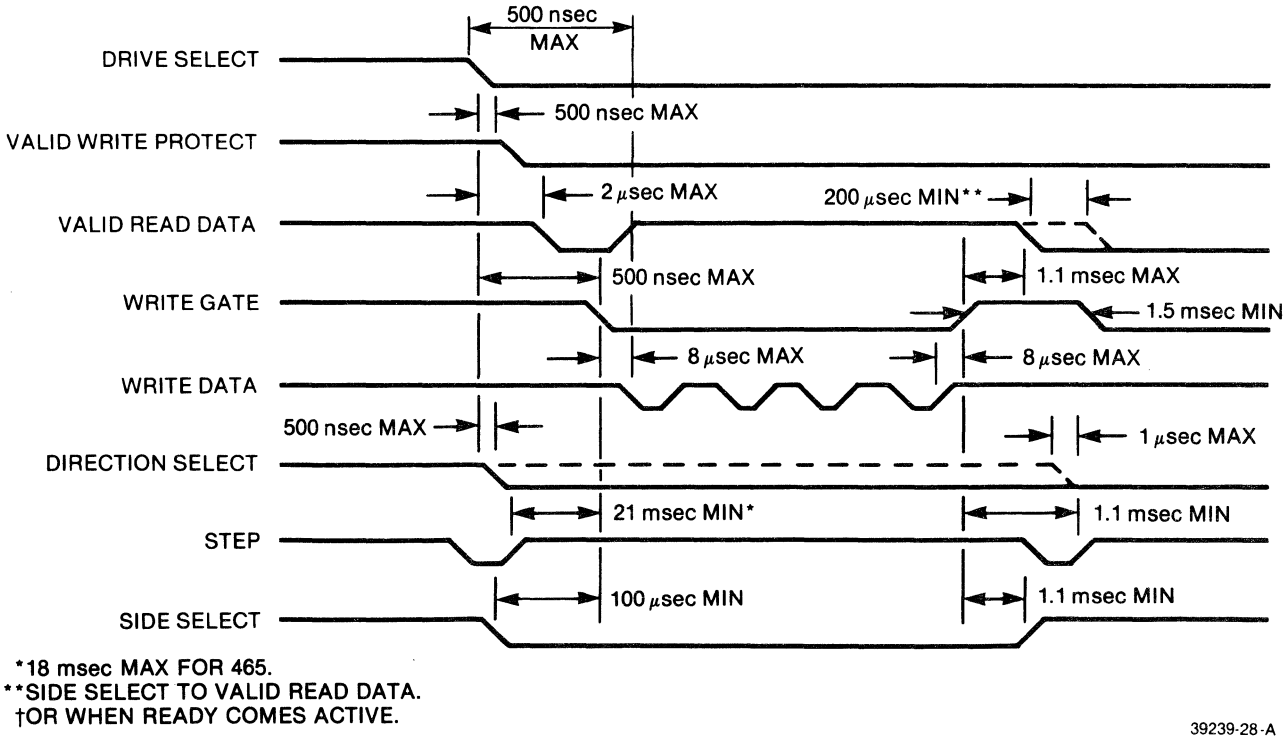


FIGURE 1-4. WRITE TO STEP

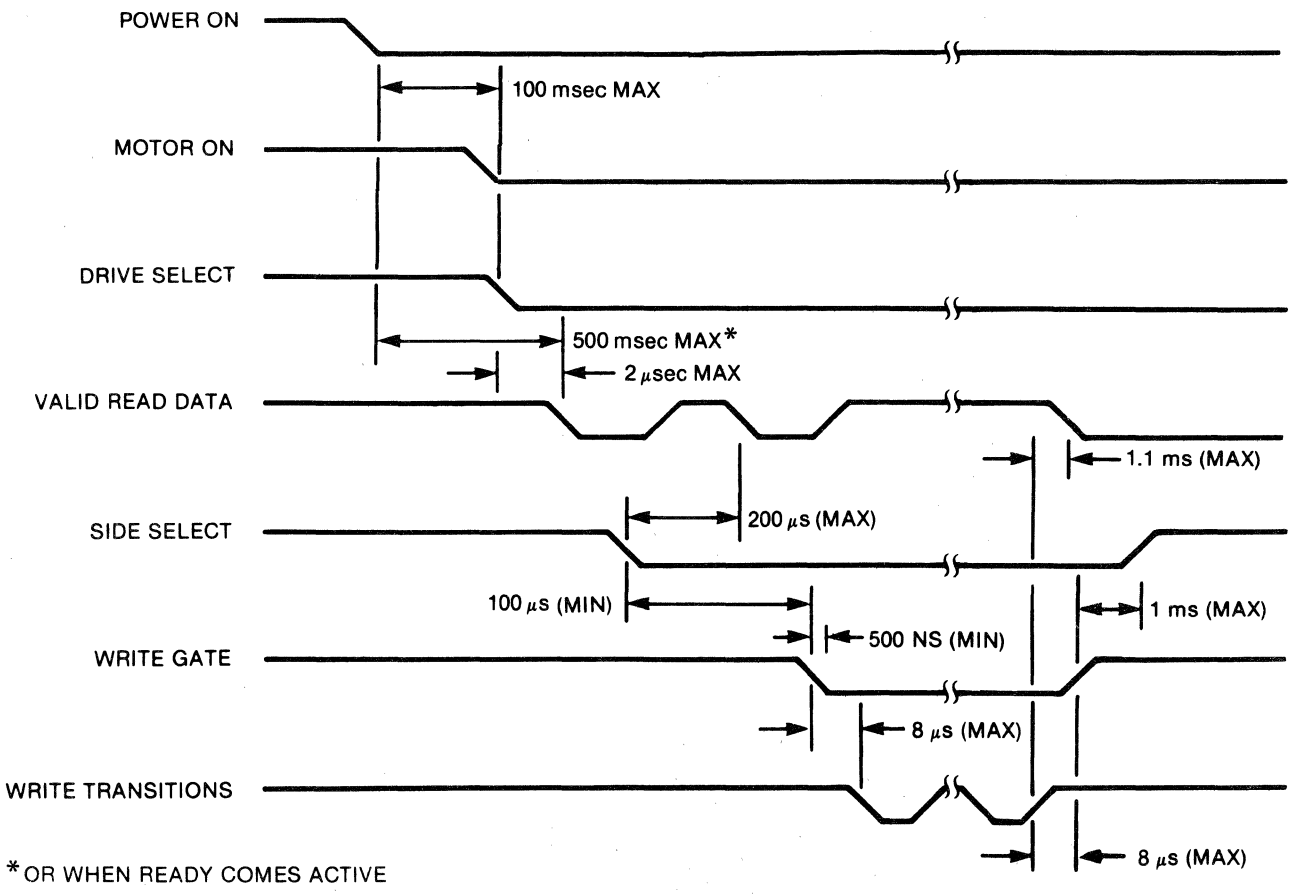


FIGURE 1-5. READ TO WRITE (FM)

1.6.7 Read Operation

Reading data from the drive(s) is accomplished by:

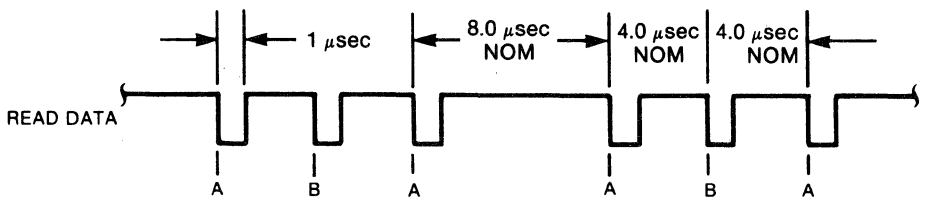
a. Activating the DRIVE SELECT line.

b. Selecting the head.

c. WRITE GATE being inactive.

The timing relationships required to initiate a read sequence are shown in figure 1-5. These timing specifications are required to guarantee that the position of the read/write heads has stabilized prior to reading.

The timing of Read Data (FM) is shown in figure 1-6.



A = LEADING EDGE OF BIT MAY BE ± 800 nsec FROM ITS NOMINAL POSITION.
B = LEADING EDGE OF BIT MAY BE ± 400 nsec FROM ITS NOMINAL POSITION.

39238-05

FIGURE 1-6. READ DATA TIMING (FM)

ıe encoding scheme of the recorded data can be FM or MFM. FM encoding rules specify a clock bit at the start of ıery bit cell and a data bit at the center of the bit cell if this cell contains a one data bit, (see figure 1-7). MFM en-ıding rules allow clock bits to be omitted form some bit cells with the following prerequisites:

a. The clock bit is omitted from the current bit cell if either the preceding bit cell or the current bit cell contains a one data bit. See figure 1-7.

b. In the above mentioned encoding schemes, clock bits are written at the start of their respective bit cells and data bits at the center of their bit cells.

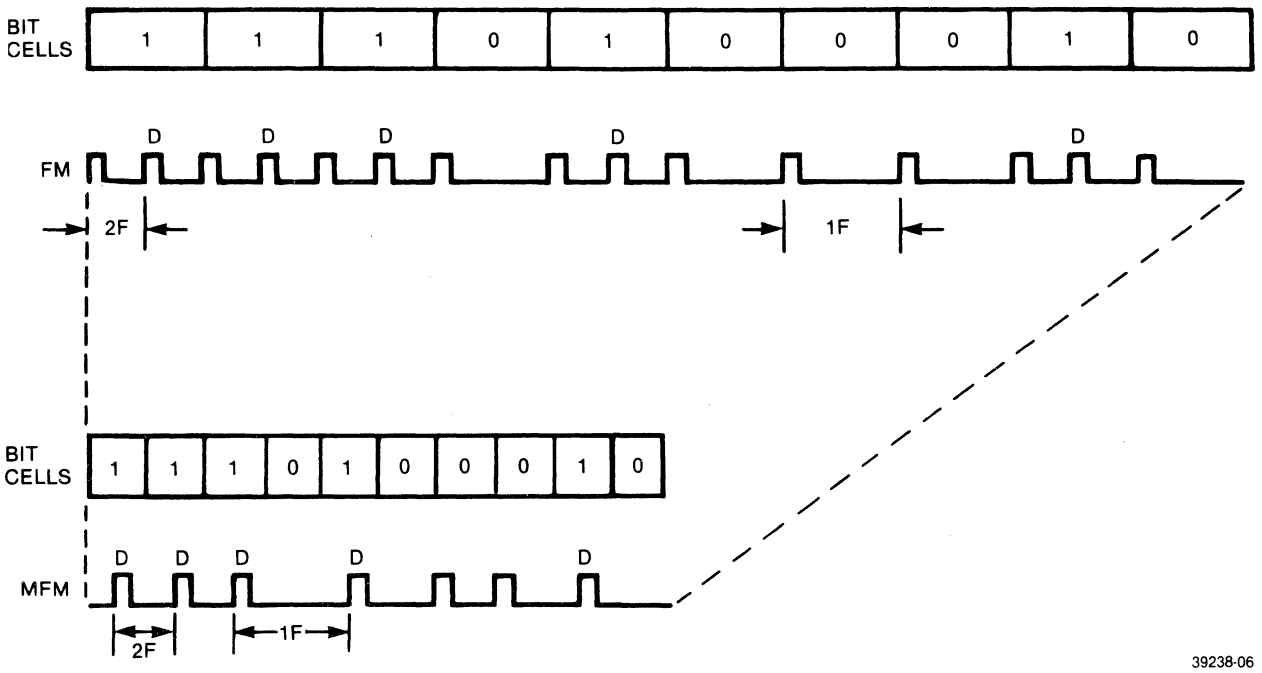


FIGURE 1-7. FM AND MFM CODE COMPARISONS

.6.8 Write Operation

Vriting data to the drive(s) is accomplished by:

a. Activating the DRIVE SELECT line.

b. Selecting the head.

c. Activating the WRITE GATE line.

d. Pulsing the WRITE DATA line with the data to be written.

ˆhe timing relationships required to initiate a Write Data sequence are shown in figure 1-5. These timing specifica-ıons are required in order to guarantee that the position of the read/write heads has stabilized prior to writing.

ˆhe timing specifications for the write data pulses are shown in figure 1-8. Write data encoding can be FM or MFM. ˆhe write data should be precompensated 125 nsec starting at track 22 (455) or track 40 (465) to counter the ef-ects of bit shift. The direction of compensation required for any given bit in the data stream depends on the pattern : forms with nearby bits.

ı.6.9 Sequence of Events

ˆhe timing diagrams shown in figures 1-3, 1-4, 1-5, and 1-9 show the necessary sequence of events with ıssociated timing requirements for proper operation.

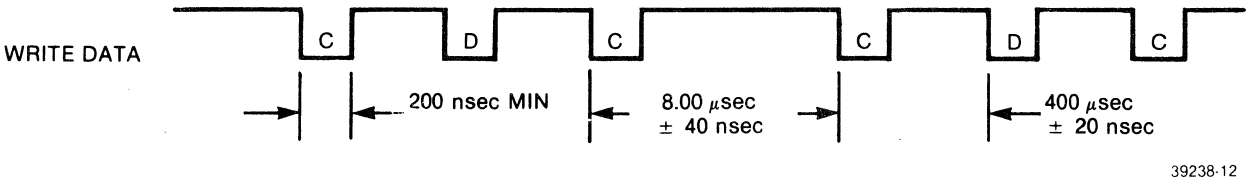


FIGURE 1-8. WRITE DATA TIMING (FM)

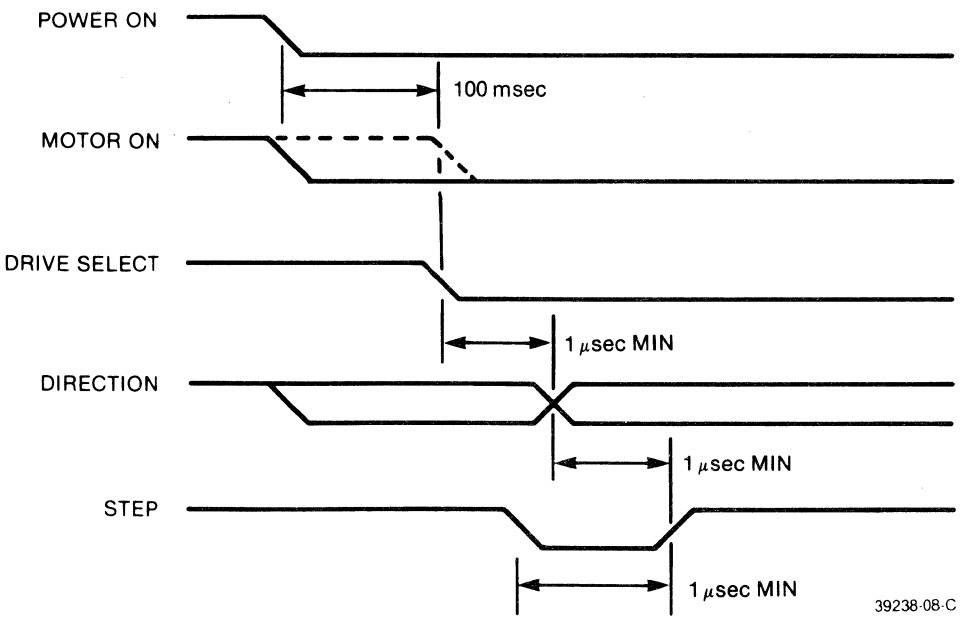


FIGURE 1-9. POWER ON TO STEP

SECTION II
ELECTRICAL INTERFACE

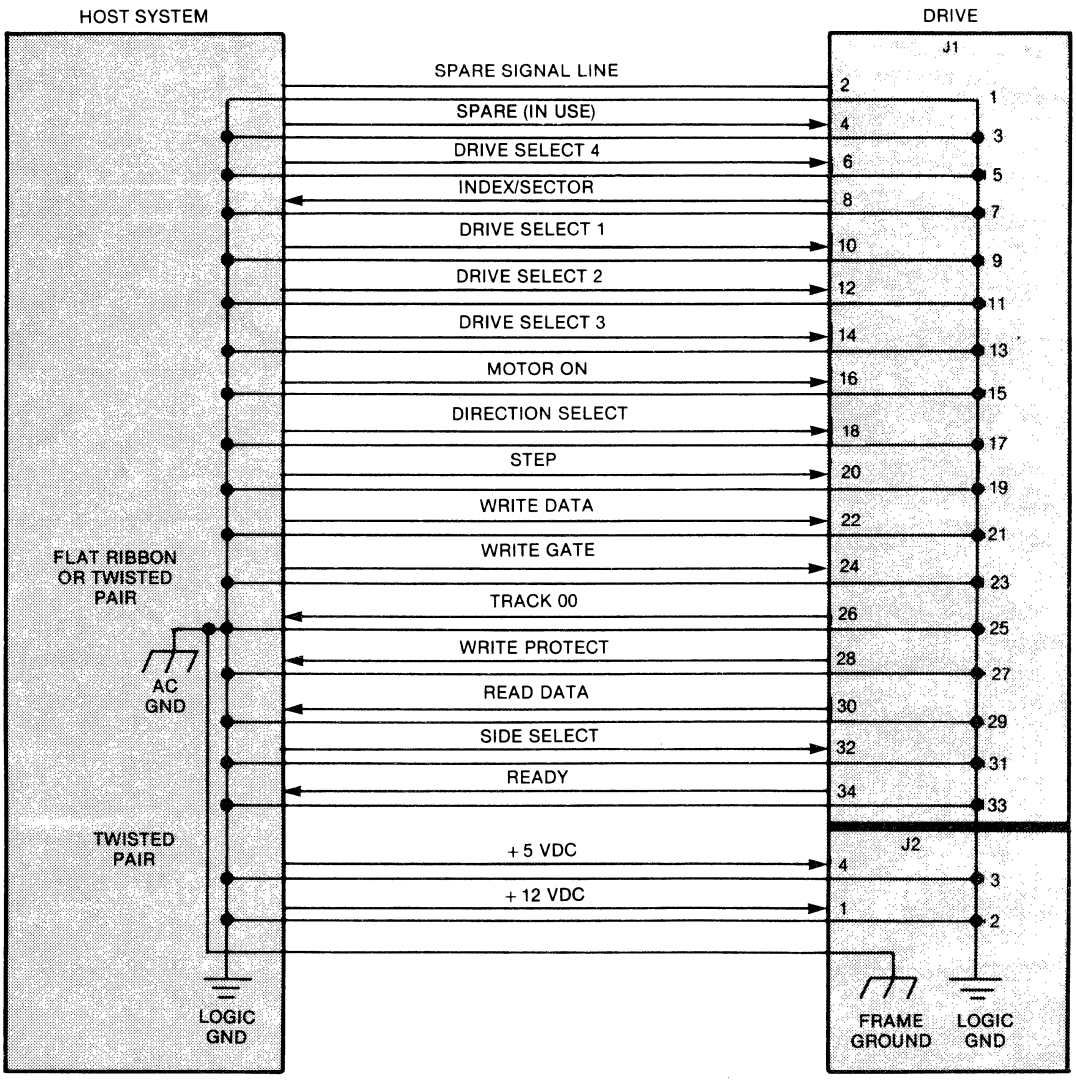
2.1 INTRODUCTION

The interface of the 455/465 can be divided into two categories:

a. Signal Lines

b. Power Lines

The following sections provide the electrical definition for each line. See figure 2-1 for all interface connections.



☆ **FIGURE 2-1.** INTERFACE CONNECTIONS

2.2 SIGNAL INTERFACE

The signal interface consists of two categories:

a. Control Lines

b. Data Transfer Lines

All lines in the signal interface are digital in nature and either provide signals to the drive (input), or provide signals to the host (output), via interface connector P1/J1.

2.2.1 Input Lines

The input signals are of three types: those intended to be multiplexed in a multiple drive system, those which will perform the multiplexing, and those signals which are not multiplexed and affect all the drives in a daisy chain system.

The input signals to be multiplexed are:

a. DIRECTION SELECT

b. STEP

c. WRITE DATA

d. WRITE GATE

e. SIDE SELECT

The input signals which are intended to do the multiplexing are:

a. DRIVE SELECT 1

b. DRIVE SELECT 2

c. DRIVE SELECT 3

d. DRIVE SELECT 4

MOTOR ON is not multiplexed.

The input lines have the following electrical specifications. See figure 2-2 for the recommended circuit.

True = Logical zero = V_{IN} ±0.0 to +0.4 V @ I_{IN} = 40 mA (max)

False = Logical one = V_{IN} +2.5 to +5.25 V @ I_{IN} = 250 μA (open)

Input impedance = 150 ohms

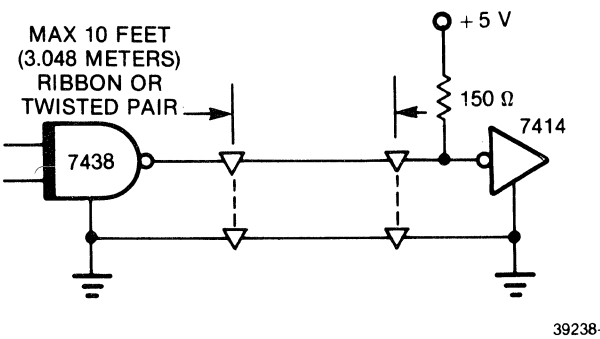


FIGURE 2-2. INTERFACE SIGNAL DRIVER/RECEIVER

2.2.2 Input Line Terminations

The 455/465 has been provided with the capability of terminating the six input lines listed below.

1. MOTOR ON
2. DIRECTION SELECT
3. STEP
4. WRITE DATA
5. WRITE GATE
6. SIDE SELECT

These lines are terminated through a 150 ohm resistor pack. In a single drive system, this resistor pack should be kept in place to provide the proper terminations.

In a multiple drive system, only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed. External terminations may also be used. However, the user must provide the terminations beyond the last drive and each of the five lines must be terminated to +5 V dc through a 150 ohm, 1/4-watt resistor.

2.2.3 Drive Select 1–4

The 455/465, as shipped from the factory, is configured to operate in a single drive system. The 455/465 can be easily modified by the user to operate with other drives in a multiplexed multiple-drive system.

In a multiple drive system, the four input lines (DRIVE SELECT 1 through DRIVE SELECT 4) are provided so that the using system may select which drive on the interface is to be used. In this mode of operation, only the drive with its DRIVE SELECT line active will respond to the input lines and gate the output lines.

2.2.4 Motor On

This input, when activated to a logical zero level, will turn on the drive motor allowing reading or writing on the drive. A 500 msec delay after activating this line must be allowed before reading or writing. This line should be deactivated for maximum motor life, if no commands have been issued to the drives within two seconds (ten revolutions of the media) after completion of a previous command.

2.2.5 Direction Select

This interface line defines the direction of motion the read/write heads will take when the STEP line is pulsed. An open circuit or logical one defines the direction as out. If a pulse is applied to the STEP line, the read/write heads will move away from the center of the disk. Conversely, if this input is shorted to ground or a logical zero leve, the direction of motion is defined as in. If a pulse is applied to the STEP line, the read/write heads will move towards the center of the disk.

2.2.6 Step

This interface line is a control signal which causes the read/write heads to move in the direction of motion defined by the DIRECTION SELECT line. This signal must be a logical low going pulse with a minimum pulse width of one μsec and then logically high for five msec minimum between adjacent pulses. Each subsequent pulse must be delayed by six msec (455) minimum of three msec (465) minimum from the preceding pulse.

The access motion is initiated on each logical zero to logical one transition, or at the trailing edge of the signal pulse. Any change in the DIRECTION SELECT line must be made at least one μsec before the trailing edge of the STEP pulse. The DIRECTION SELECT logic level must be terminated one μsec after the trailing edge of STEP pulse. See figure 2-3 for these timings.

2.2.7 Write Gate

The active state of this signal, or logical zero, enables write data to be written on the diskette. The inactive state or logical one, enables the read data logic and stepper logic. See figure 2-4 for timings.

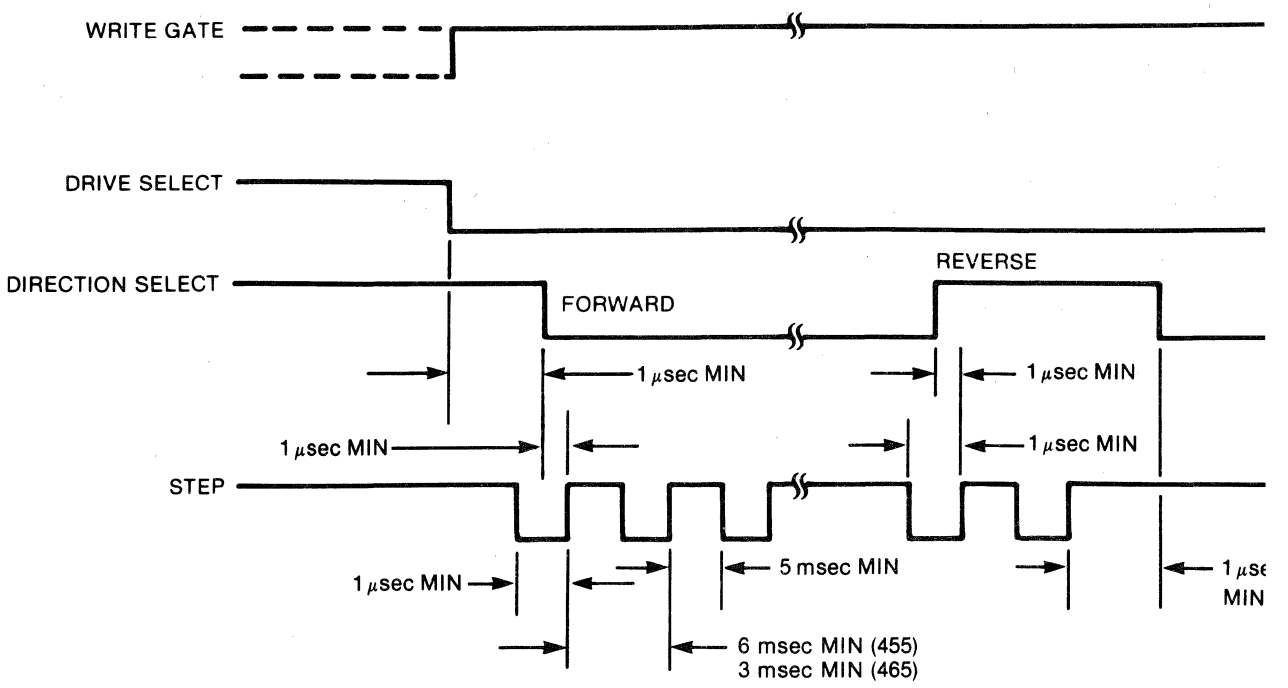


FIGURE 2-3. STEP TIMING

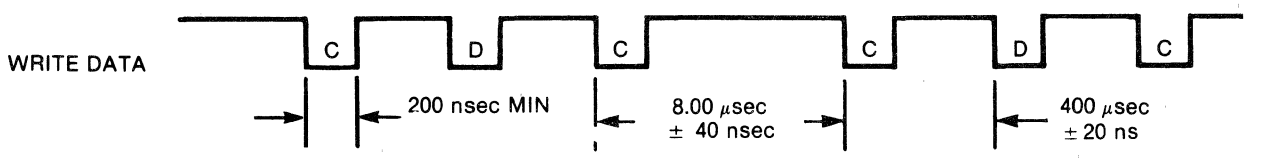


FIGURE 2-4. WRITE DATA TIMING

2.2.8 Write Data

This interface line provides the data to be written on the diskette. Each transition from a logical one to a logical zer level, will cause the current through the read/write heads to be reversed thereby writing a data bit. This line enabled by WRITE GATE being active. Write data must be inactive during a read operation. A write data clamp provided on the PCB at the interface which holds the WRITE DATA line at a logical zero whenever WRITE GAT is inactive. See figure 2-4 for timings.

2.2.9 Side Select

This signal defines which side of a two-sided diskette is to be written on or read from. A logical one selects the side head. When switching from one side to the other, a 100 μsec delay is required before a read or write operation ca be initiated.

2.2.10 Output Lines

The output control lines have the following electrical specifications.

True = Logical zero = +0.0 to +0.4 V @ I_{OUT} = 40 mA (max)

False = Logical one = +5 to +2.5 V (open collector) @ I_{OUT} = 250 μA (max)

2.2.11 Track 00

The active or logical zero state of this interface signal indicates when the read/write heads are positioned at track zero (the outermost track) and the access circuitry is driving current through phase A of the stepper motor. This signal is at a logical one level, or inactive state, when the read/write heads are not at track zero. When the read/write heads are at track zero and an additional step out pulse is issued to the drive, a mechanical stop will keep the read/write heads at track zero. However, the TRACK 00 signal will go inactive. This is because the stepper motor will go to phase C and not phase A. One more step out pulse will put the stepper motor back into phase A and the TRACK 00 signal will go active again.

2.2.12 Index/Sector

This interface signal is provided by the drive each time an index or sector hole is sensed at the Index/Sector photo detector. Normally, this signal is at a logical one level and makes the transition to the logical zero level each time a hole is sensed.

When using 154/164 media (soft-sectored), there will be 17 or 11 pusles on this interface line per revolution (200 msec). This pulse indicates the physical beginning of a track. See figure 2-5 for the timing.

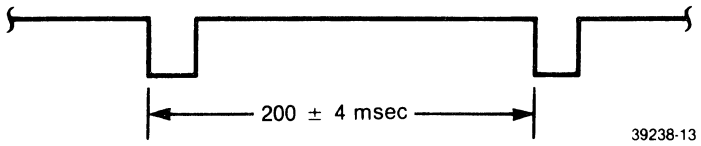


FIGURE 2-5. INDEX TIMING (SHUGART 154/164 MEDIA)

When using 155/165 or 157/167 media (hard-sectored), there will be 17 or 11 pulses on this interface line per revolution (200 msec). To indicate the beginning of a track, once per revolution there is one index transition between 16 or ten equally spaced sector transitions. The timing for these signals is shown in figures 2-6 and 2-7.

When using the Index/Sector signal, look for an edge or transition rather than a level for determining the status. With no diskette inserted, this signal remains active or at a logical zero level which is an erroneous status.

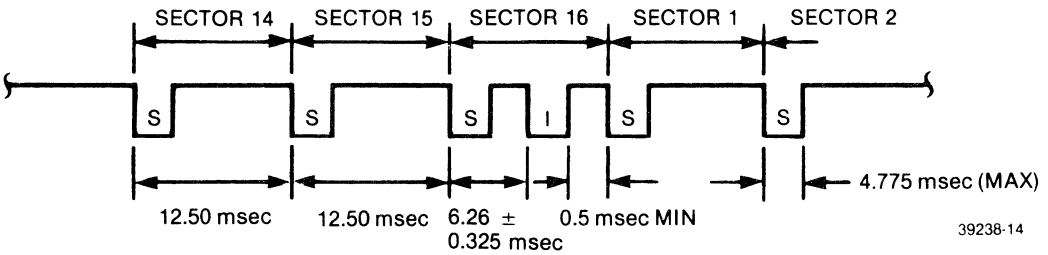


FIGURE 2-6. INDEX/SECTOR TIMING (SHUGART 155/165 MEDIA)

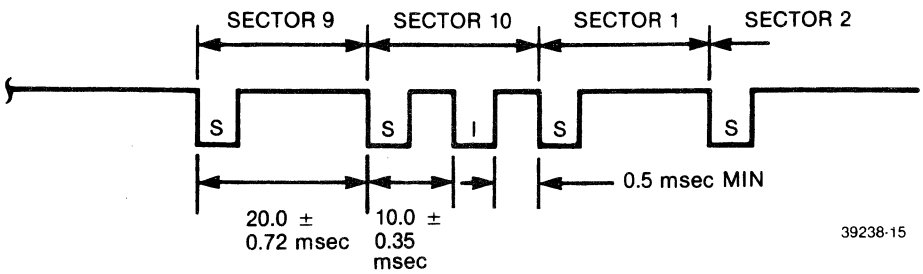


FIGURE 2-7. INDEX/SECTOR TIMING (SHUGART 157/167 MEDIA)

2.2.13 Read Data

This interface line provides the raw data (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. See figures 1-5 and 1-6 for the timing and bit shift tolerance within normal media variations.

2.2.14 Write Protect

This interface signal is provided by the drive to give the user an indication when a write protected diskette is installed. The signal is a logical zero level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition to notifying the interface.

2.2.15 Ready

READY informs the controller that a diskette is properly inserted and that the drive motor is up to speed. 500 msec is required for starting the motor and an additional 200 msec is required for one revolution at the rated speed. Thus, READY is available 700 msec after power is applied to the motor. The 455/465 generate READY by sensing index pulses and measuring their frequency of occurence. When the index pulses are 200 msec apart, READY becomes active.

2.3 POWER INTERFACE

The 455/465 require only dc power for operation. DC power to the drive is provided via P2/J2. The two dc voltages, their specifications, and their P2/J2 pin designators are outlined in table 2-1. The specifications outlined on current requirements are for one drive. For multiple drive systems, the current requirements are a multiple of the maximum current times the number of drives in the system.

TABLE 2-1. DC POWER REQUIREMENTS

P2 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+ 12 VDC	± 1.2 VDC	1.2 A MAX 0.6 A TYP	50 mV MAX ALLOWABLE
2	+ 12 RETURN	*		
3	+ 5 RETURN	*		
4	+ 5 VDC	± 0.25 VDC	0.9 A MAX 0.6 A TYP	50 mV MAX ALLOWABLE

* + 12 VDC AND + 5 VDC GROUND RETURNS ARE TIED TOGETHER AT DRIVE PCB.

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2.4 FRAME GROUNDING

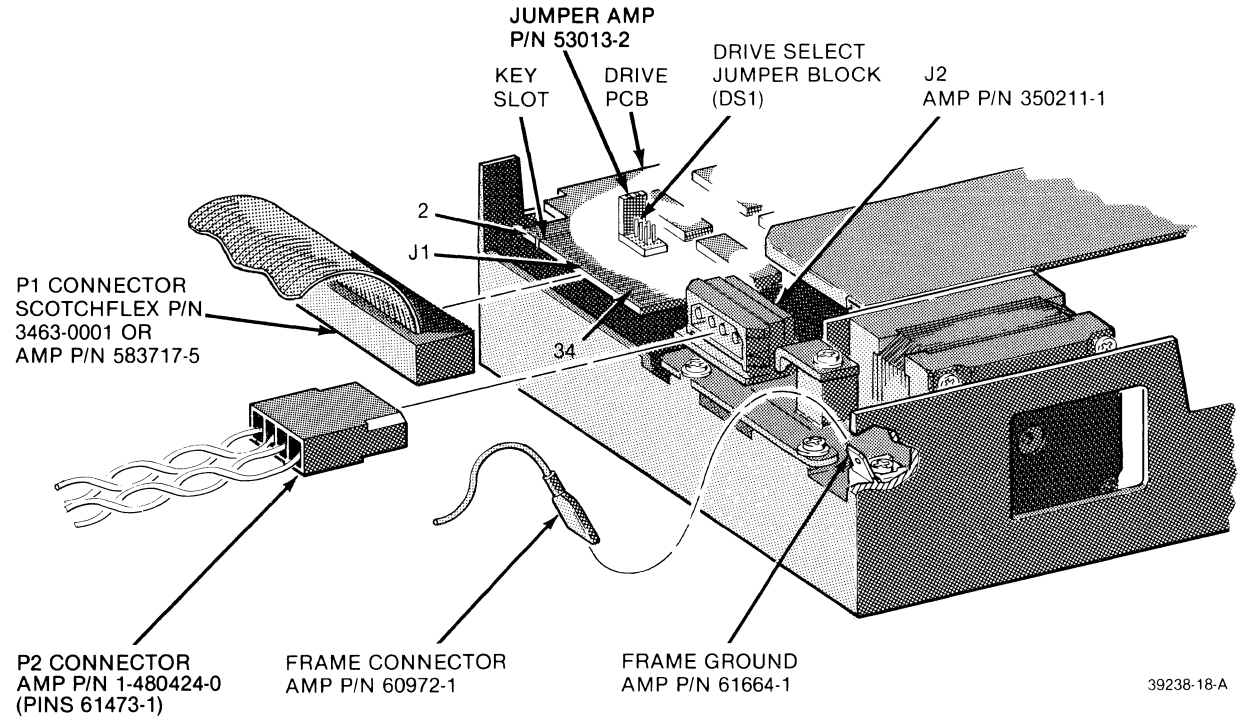
It is important that the drive be frame grounded to the host system ac ground or frame ground. Failure to do so may result in drive noise susceptibility. Refer to paragraph 3.2 for frame grounding procedure.

SECTION III
PHYSICAL INTERFACE

3.1 INTRODUCTION

This section describes the physical locations of the connectors used on the drive and recommended connectors to be used with them.

The electrical interface between the 455/465 and the host system is via two connectors. The first connector, J1, provides the signal interface. The second connector, J2, provides the dc power. See figure 3-1 for connector locations.



☆**FIGURE 3-1.** INTERFACE CONNECTORS PHYSICAL LOCATIONS

3.1.1 J1/P1 Connector

Connection to J1 is through a 34 pin PCB edge connector. The dimensions for this connector are shown in figure 3-2. The pins are numbered 1 through 34 with the even numbered pins on the component isde of the PCB. The odd numbered pins are on the non-component side. Pin 2 is located on the end of the PCB connector closest to the corner and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying.

3.1.2 J2/P2 Connector

The dc power connector, J2, is a 4-pin AMP Mate-N-Lok connector (P/N 350211-1). The recommended mating connector, P2, is AMP P/N 1-480424-0 using AMP pins P/N 61473-1. J2, pin 1, is labeled on the component side of the PCB. Wire used should be #18 AWG. Figure 3-3 illustrates the J2 connector as seen on the drive PCB from the non-component side.

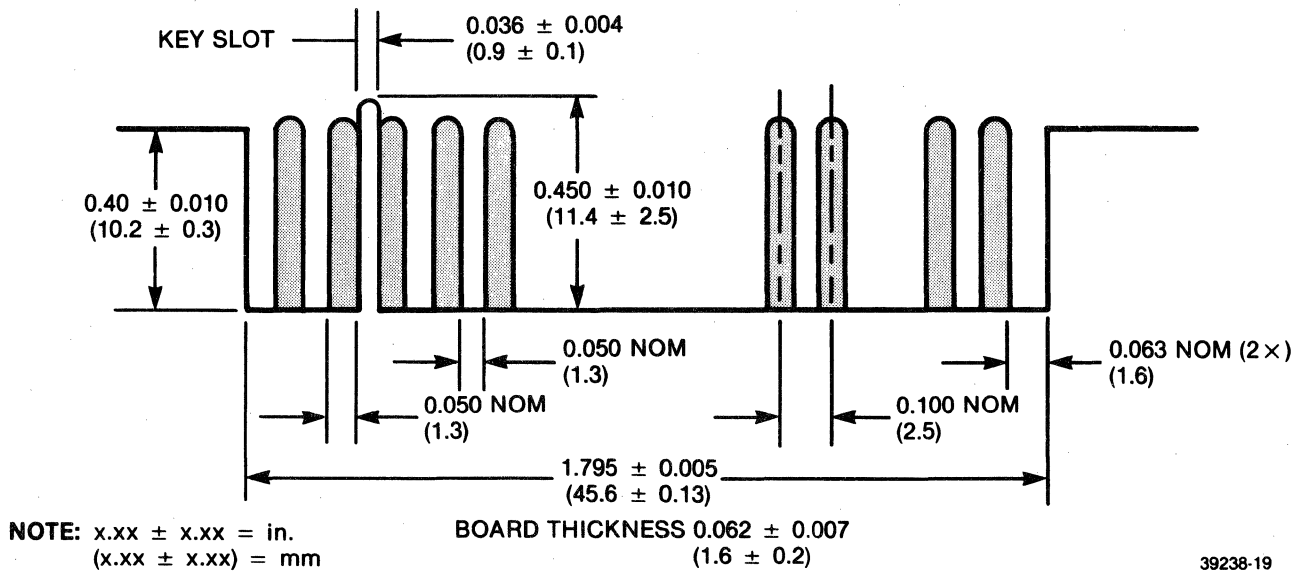


FIGURE 3-2. J1 CONNECTOR DIMENSIONS

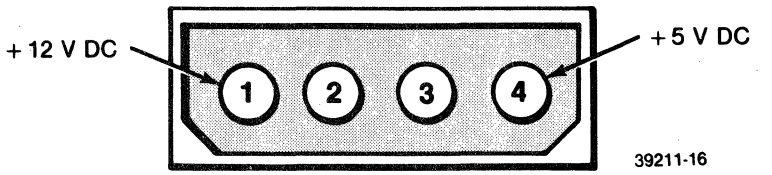


FIGURE 3-3. J2 CONNECTOR

3.2 FRAME GROUNDING

CAUTION

The drive(s) must be frame grounded to the host system to ensure proper operation. If the frame of the drive is not fastened directly to the frame of the host system with a good ac ground, a wire from the system ac frame ground must be connected to the drive(s). For this purpose, a faston tab is provided on the drive near the motor control PCB where a faston connector can be attached or soldered. The tab is AMP P/N 61664-1 and its mating connector is AMP P/N 60972-1.

SECTION IV
PHYSICAL SPECIFICATIONS

4.1 GENERAL

These paragraphs contain the mechanical dimensions and mounting recommendations for the Shugart 455/465.

4.2 MECHANICAL DIMENSIONS

See figure 4-1 for dimensions of the 455/465.

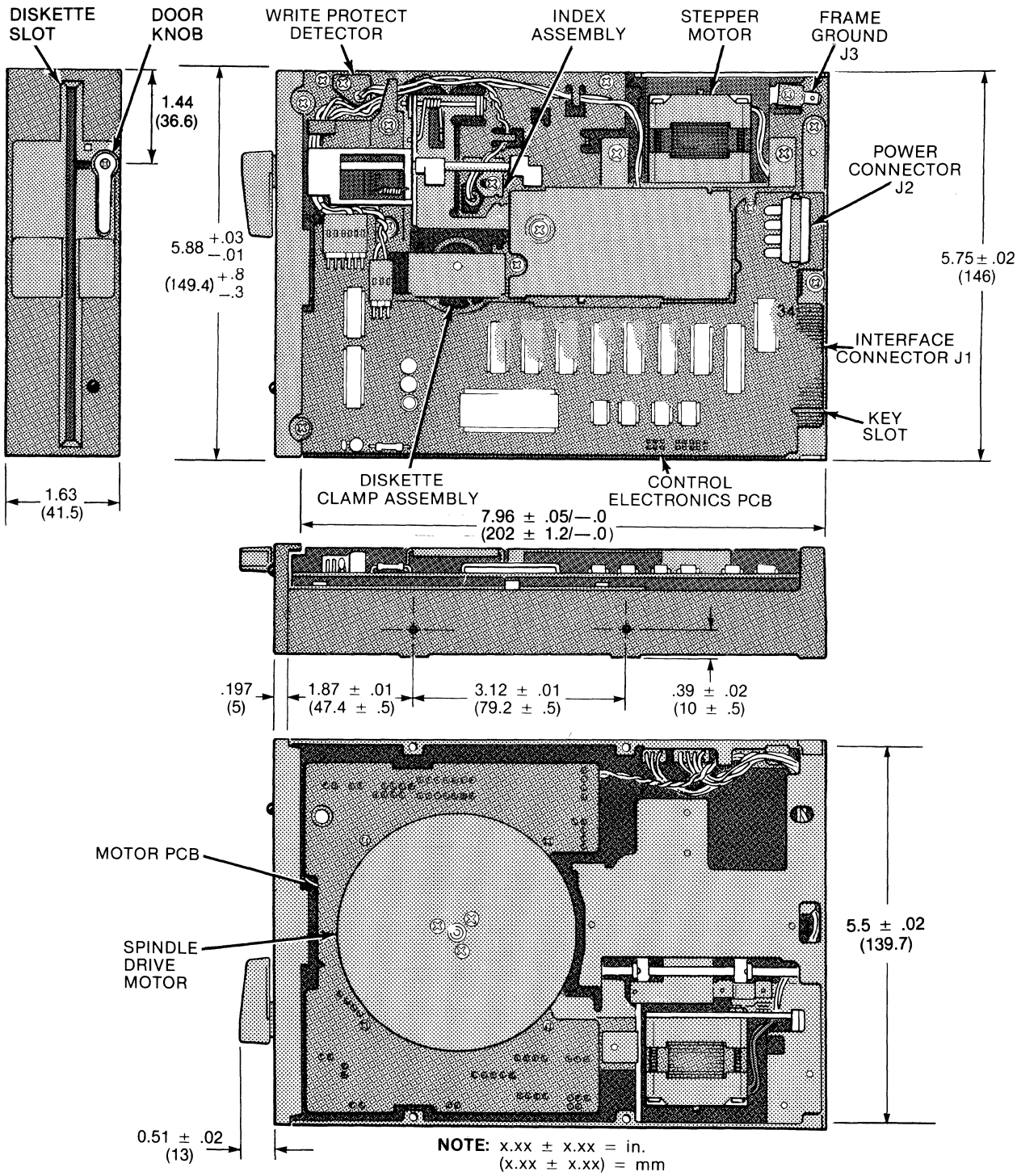
4.3 MOUNTING

CAUTION

Do not mount horizontal with PCB down. Failure to do so may damage the drive.

The 455/465s are capable of being mounted in one of the following positions:

1. Top Loading — mounted upright.
2. Front Loading — mounted vertical with door opening left or right.
   — mounted horizontal with PCB up.
3. Mounting hardware for bottom and side holes is #3 metric.



NOTE: SCREW SIZE: #3 METRIC
d = 3 mm
L = 5 mm

39238-20-A

☆FIGURE 4-1. 455/465 PHYSICAL DIMENSIONS

SECTION V
ERROR RECOVERY

5.1 WRITE ERROR

If an error occurs during a write operation, this error will be detected on the next revolution by doing a read operation (commonly called a write check). To correct the error, another write and write check operation must be done. If the write operation is not successful after ten attempts have been made, a write and write check operation should be attempted on another track. This is done to determine if the media or the drive is failing. If the error persists, the disk should be considered defective and discarded.

5.2 READ ERROR

Most errors that occur will be soft errors. Soft errors are usually caused by the following:

a. Airborne contaminants passing between the read/write head and the disk. The contaminants will generally be removed by the cartridge self-cleaning wiper.

b. Random electrical noise which usually lasts for a few microseconds.

c. Small defects in the written data and/or track not detected during the write operation which may cause a soft error during a read.

The following procedure is recommended to recover from errors:

a. Reread the track ten times or until such time as the data is recoverd.

b. If data is not recovered after doing step "a", access the head to the adjacent track in the same direction it was previously moved. Return to the desired track.

c. Repeat step "a".

d. If data is not recovered, the error is not recoverable.

5.3 SEEK ERROR

Seek errors are detected by reading an ID field after the seek is completed. The ID field contains the track address. If a seek error is detected, the host system should issue a recalibrate operation (step out until Track 00 line goes active) and seek back to the original track.

SECTION VI
RECORDING FORMAT

6.1 GENERAL

The format of the data recorded on the diskette is totally a function of the host system. As discussed in paragraph 1.6.8, data can be recorded on the diskette using FM or MFM encoding. In these encoding techniques, clock bits are written at the start of their respective bit cells and bits at the centers of their bit cells.

6.2 BYTE

A byte, when referring to serial data (being written onto or read from the disk drive), is defined as eight consecutive bit cells. The most significant bit cell is defined as bit cell 0. The least significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e., data bit 3), it is with respect to the corresponding bit cell (bit cell 3).

During a write operation, bit cell 0 of each byte is transferred to the disk drive first with bit cell 7 being transferred last. Correspondingly, the most significant byte of data is transferred to the disk first and the least significant byte is transferred last.

When data is being read back from the drive, bit cell 0 of each byte will be transferred first with bit cell 7 last. As with reading, the most significant byte will be transferred first from the drive to the user.

Figure 6-1 illustrates the relationship of the bits within a byte. Figure 6-2 illustrates the relationship of the bytes for read and write data.

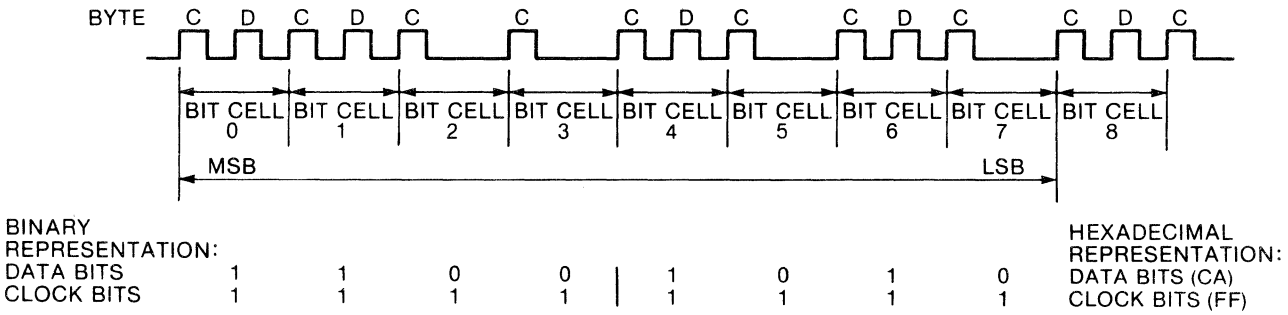


FIGURE 6-1. BYTE (FM ENCODING)

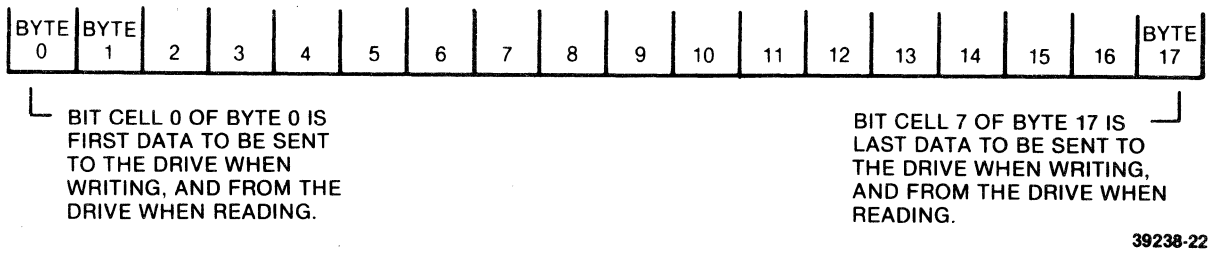


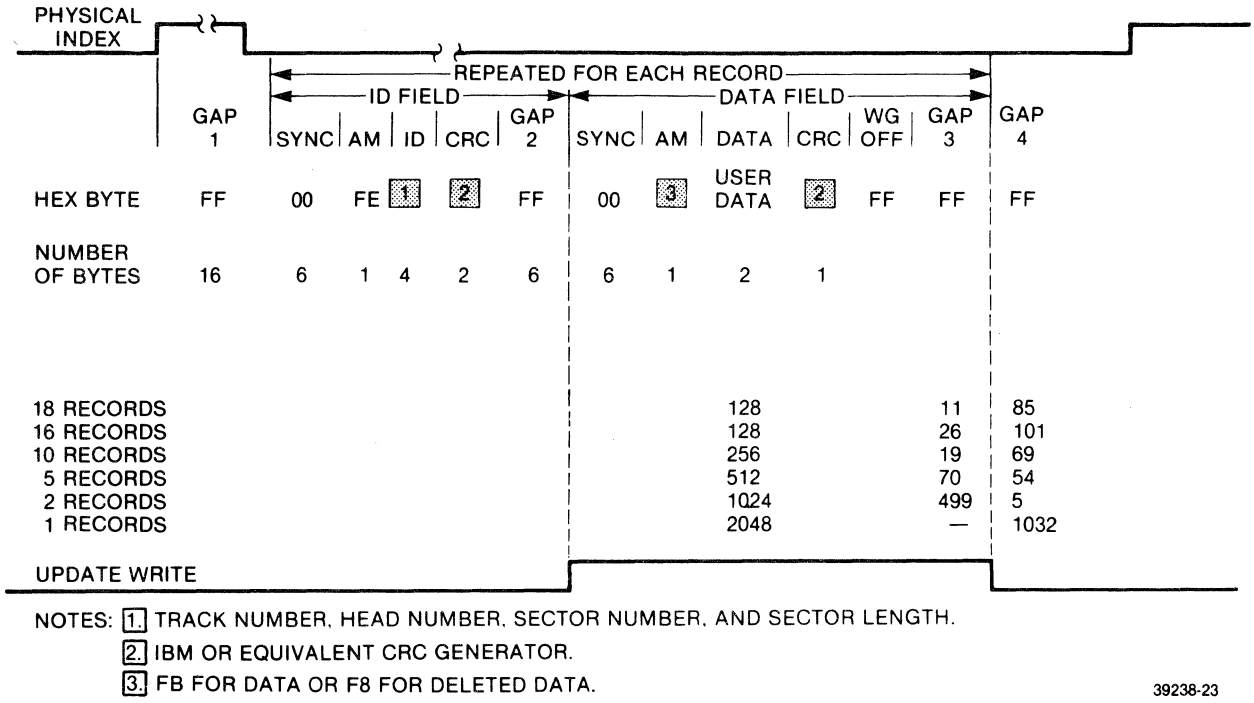
FIGURE 6-2. DATA BYTES

6.3 FORMATS

Tracks may be formatted in numerous ways and are dependent on the using system. The drive(s) can use eith hard or soft-sectored formats.

6.3.1 Soft-Sectored Recording Format

In this format, the using system may record one long record or several smaller records. Each track is started by physical index pulse and then each record is preceded by a unique recorded identifier. This type of recording is ca ed soft-sectoring. Figure 6-3 illustrates the recommended single density (FM) formats. Figure 6-4 illustrates tl recommended double density (MFM) formats.



NOTES: 1. TRACK NUMBER, HEAD NUMBER, SECTOR NUMBER, AND SECTOR LENGTH.
2. IBM OR EQUIVALENT CRC GENERATOR.
3. FB FOR DATA OR F8 FOR DELETED DATA.

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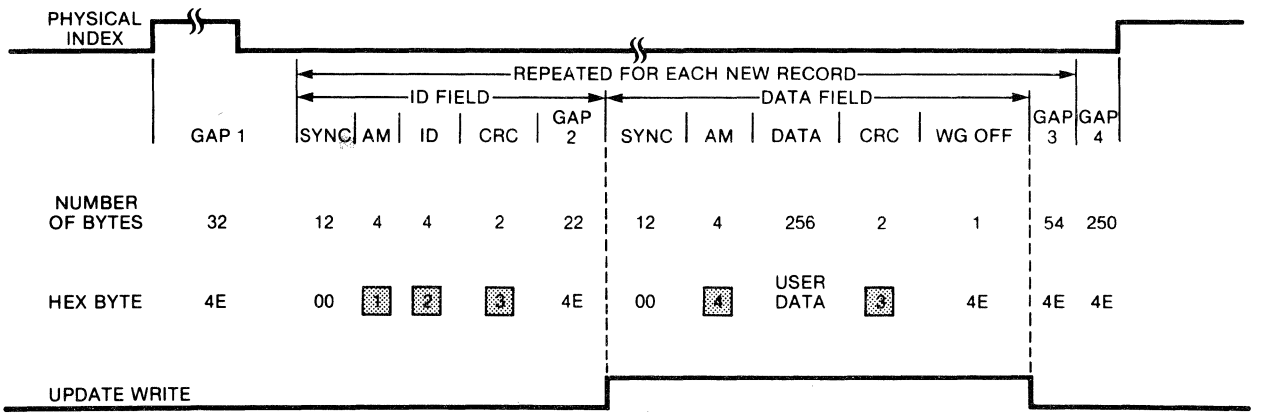
FIGURE 6-3. FM TYPICAL SOFT SECTOR SINGLE DENSITY (EVEN BOUNDARIES)



NOTES: 1. FIRST THREE BYTES ARE HEX A1 WITH MISSING CLOCK TRANSITIONS BETWEEN BITS 4 AND 5. LAST BYTE IS HEX FE.
2. TRACK NUMBER, HEAD NUMBER, SECTOR NUMBER, AND SECTOR LENGTH (HEX 01).
3. IBM OR EQUIVALENT CRC GENERATOR.
4. SAME AS NOTE 1, EXCEPT LAST BYTE = HEX FB.

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FIGURE 6-4. MFM TYPICAL FORMAT - 256 BYTES/16 RECORDS PER TRACK (IBM TYPE)

6.3.2 Track Layout

Index is the physical detector indicating one revolution of the media. Index is used to initiate format operations, to generate the READY signal in the storage device, to ensure one complete revolution of the media has been searched, and as a deselect storage device signal, after a certain number of revolutions.

Gap 1 — Gap 1 is from the physical index mark to the ID field address mark sync. Gap 1 allows for physical index variation, speed variation, and interchange between storage devices.

ID Field — Sync is a fixed number of bytes for Separator synchronization prior to AM. Sync includes a minimum of two bytes plus worst case Separator sync up requirements.

ID Pre Address Mark (MFM) is three bytes of A1 with unique clock bits not written per encode rules.

ID Address Mark (FM) is a unique byte to identify the ID field and is not written per encode rules.

ID Address Mark (MFM) is one byte of FE and is written per encode rules.

ID is a four byte address containing track number, head number, record number, and record length.

CRC is two bytes for cyclic redundancy check.

Gap 2 — Gap 2 is from ID CRC to data AM sync. Gap 2 allows for speed variation, oscillator variation, and erase core clearance of ID CRC bytes prior to Write Gate turn on for an update write.

Data Field — Sync is a fixed number of bytes for Separator synchronization prior to AM. Sync includes a minimum of two bytes plus worst case separator sync up requirements.

Pre Data Address Mark (MFM) is three bytes of A1 with unique clock bits not written per encode rules.

Data Address Mark (FM) is a unique byte to identify the data field and is not written per encode rules.

Data Address Mark (MFM) is one bytes of FB or F8 and is written per encode rules.

Data is the area for user data.

CRC is two bytes for cyclic redundancy check.

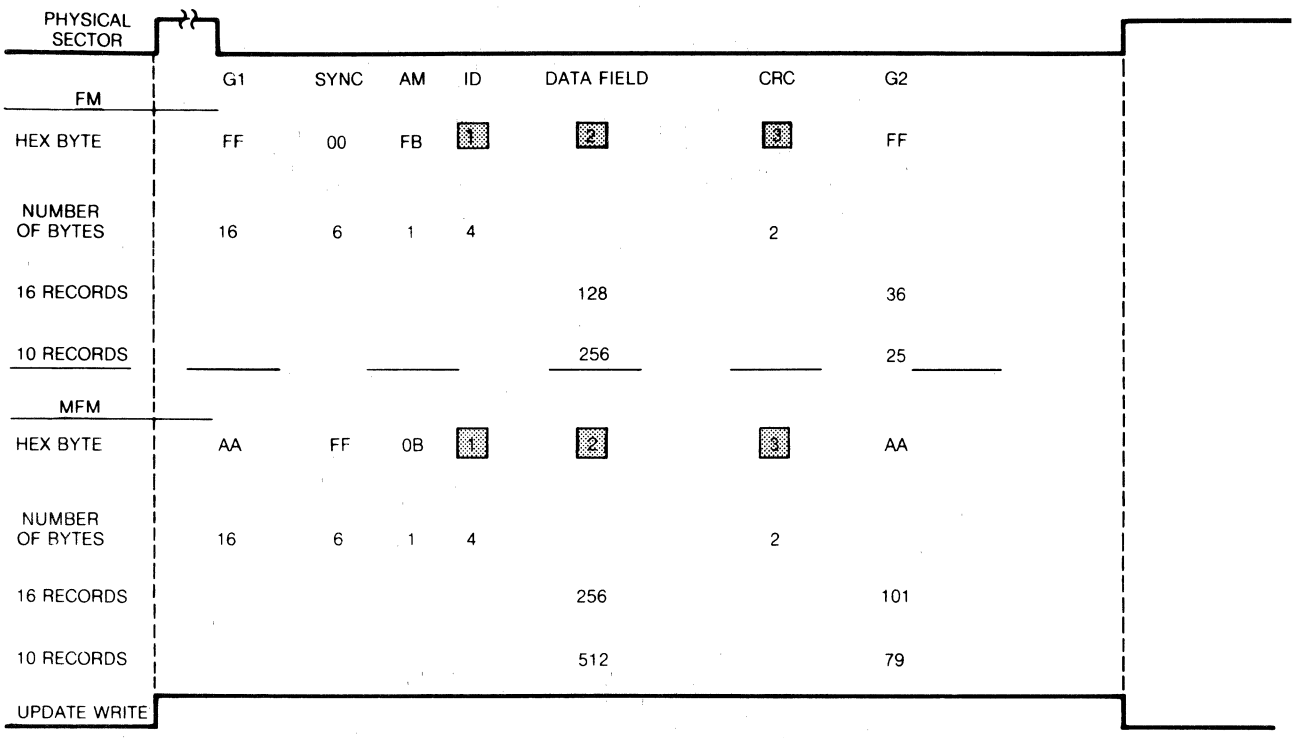
WG OFF (Write Gate Off) is one byte to allow for Write Gate turn off after an update write.

Gap 3 — Gap 3 is from WG OFF to the next ID AM sync. Gap 3 allows for erase core to clear the data field CRC bytes, speed and write oscillator variation, read preamplifier recovery time, and system turnaround time to read the following ID field.

Gap 4 — Gap 4 is the last gap prior to physical index. Gap 4 allows for speed and write oscillator variation during a format write and physical index variation.

6.3.3 Hard-Sectored Recording Format

In this format, the using system may record up to 16 or ten sectors (records) per track. Each track is started by a physical index pulse. Each sector is started by a physical sector pulse. This type of recording is called hard-sectoring. Figure 6-5 illustrates the hard-sectored formats. The Hard-Sectored minidiskette is to be used for these formats. All drive tolerances were accounted for in developing these formats.



NOTES: 1. Track Number, Head Number, Record Number, Record Length.

2. User Data.

3. Generated by CRC Generator (IBM or Equivalent).

39238-25

FIGURE 6-5. TYPICAL HARD SECTOR FM AND MFM FORMATS

SECTION VII
CUSTOMER INSTALLABLE OPTIONS

7.1 INTRODUCTION

This section discusses examples of modifications and how to implement them.

7.2 PLUGGABLE/TRACE OPTIONS

The Shugart 455/465 can be modified by the user to suit individual needs. These modifications can be implemented by adding, changing, or deleting connections.These changes can be accomplished by the use of a shorting plug (see Table 7-1) of by shorting a trace (see Table 7-2).

7.3 TERMINATOR RESISTOR PACK

The terminator resistor pack (RP1) provides terminations for multiplexed inputs. The resistor pack is pluggable and should be removed from all drives except the drive physically furthest from the controller. (see Figure 7-1)

7.4 FACTORY TRACE JUMPERS

Jumpers MDHLD, MD1, MD2, MD3, MDR are factory configured to control the Microprocessor operations and can not be altered. They are not a customer instalable option.

TABLE 7-1. PLUGGABLE OPTIONS

JUMPER/ DESIGNATION	DESCRIPTION	SHIPPED FROM FACTORY	
		OPEN	SHORT
DS1	DRIVE SELECT 1		
DS2,3,4	DRIVE SELECT 2,3,4		
DS	ENABLE DRIVE SELECT IN A MULTI-DRIVE SYSTEM		
MX	CONSTANT DRIVE SELECT USED IN A SINGLE DRIVE SYSTEM ONLY		
MS	ENABLES DRIVE MOTOR WITH DRIVE SELECT		
MM	ENABLES DRIVE MOTOR WITH MOTOR ON		
HL	HEAD LOAD (Not Used)		
HM	HEAD LOAD WITH MOTOR ON (Not Used)		
HS	HEAD LOAD WITH DRIVE SELECT (Not Used)		
IU	IN USE, ACTIVITY LIGHT WITH "UO" AND HEAD LOAD		

SHUGART DOES NOT OFFER HEAD LOAD

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TABLE 7-2. TRACE OPTIONS

JUMPER/ DESIGNATION	DESCRIPTION	SHIPPED FROM FACTORY	
		OPEN	SHORT
DR	ENABLES DRIVE READY WITH DRIVE SELECT		
RR	RADIAL READY		
RY	CONNECTS READY TO INTERFACE		
SS	SIDE SELECT NOT DELAYED		
SO	SIDE SELECT DELAYED TO ALLOW ERASE TO COMPLETE BEFORE SWITCHING SIDES		
UO	ACTIVITY LIGHT WITH "IN USE" AND HEAD LOAD		
DS	ACTIVITY LIGHT WITH DRIVE SELECT		
HD	PROVIDES PULL UP FOR HEAD LOAD INTERFACE LINE		

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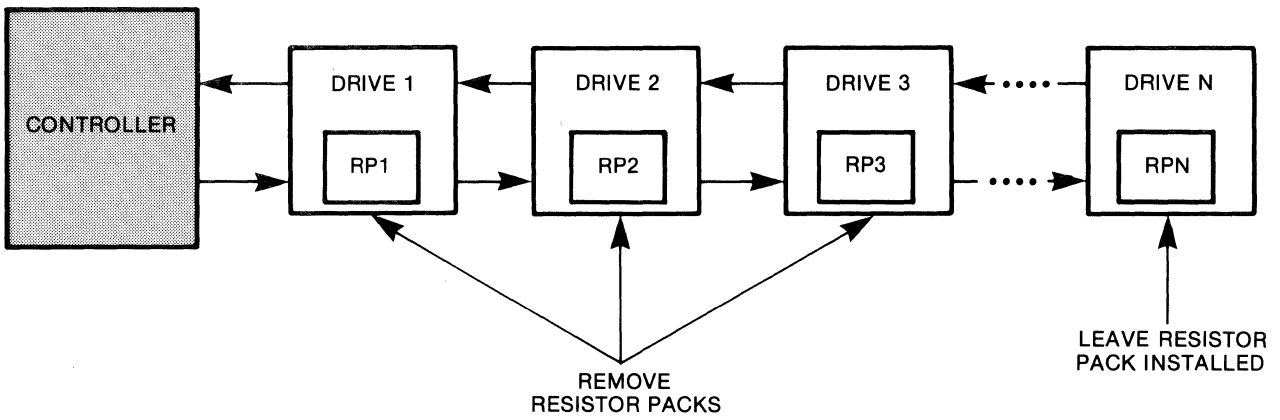
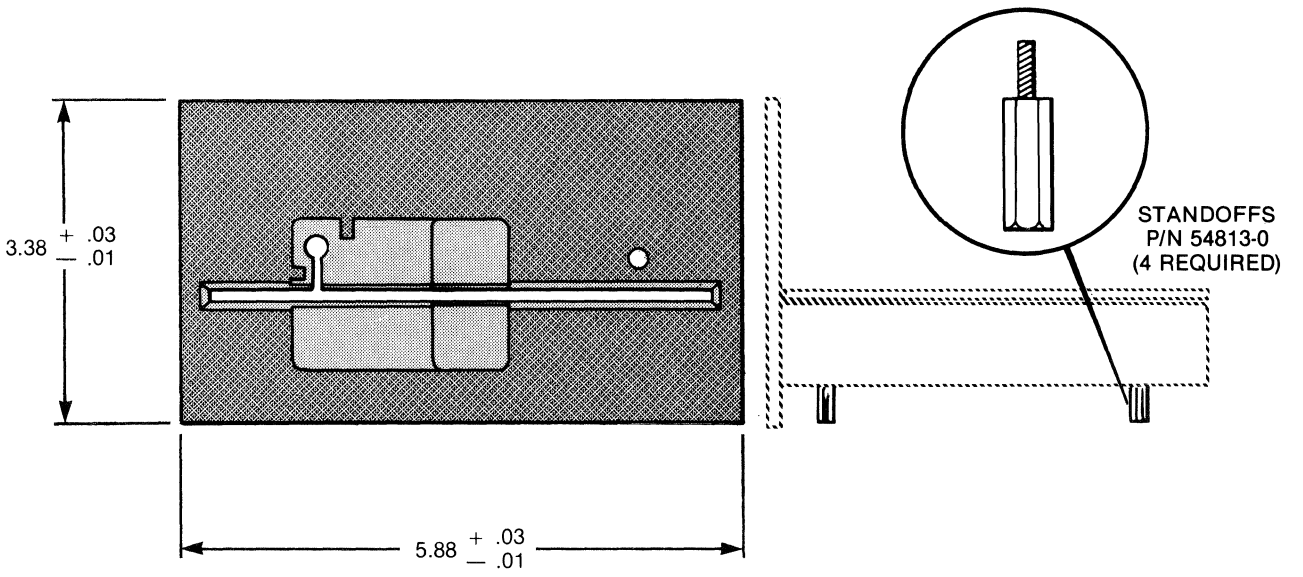


39238-41

FIGURE 7-1. RESISTOR PACK TERMINATION



FULL HEIGHT FACEPLATE, P/N 54755

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FIGURE 7-2. FULL HEIGHT FACEPLATE OPTION

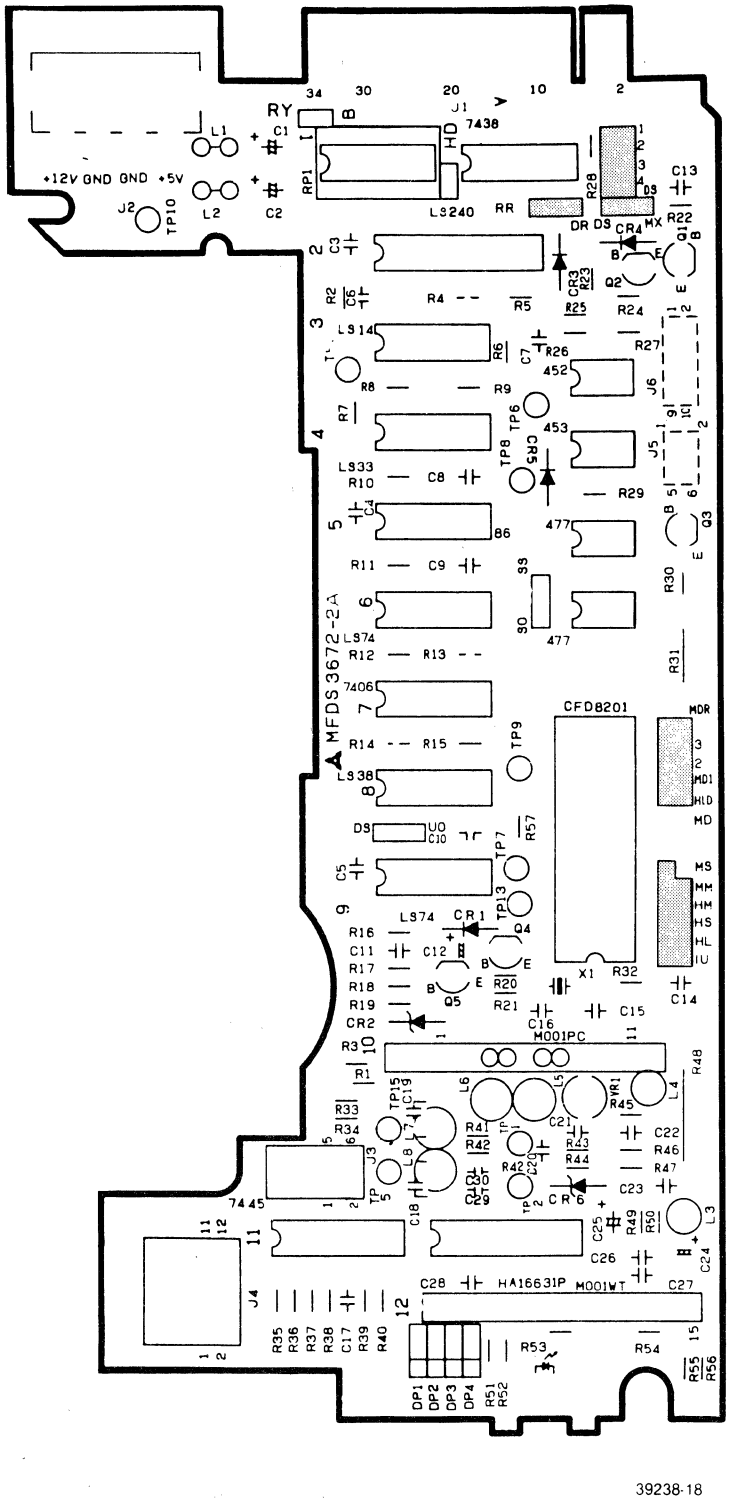


FIGURE 7-3. MLC 2 PCB COMPONENT LOCATIONS

SECTION VIII
THEORY OF OPERATION

8.1 THEORY OF OPERATION

The Shugart 455/465 floppy diskette drive electronics are packaged on one PCB which contains:

a. Read/Write Amplifier and Transition Detector

b. Spindle Motor Control

c. Drive Select Circuits

d. Index Detector Circuits

e. Track Zero Circuits

f. Track Accessing Circuits

g. Power On Reset Control

h. Write Protect Circuits

i. Drive Status Circuits

The head positioning actuator moves the read/write heads to the desired track on the diskette. The heads are loaded onto the diskette when the door is closed.

The following paragraphs describe each of the above functions in detail.

8.2 READ/WRITE OPERATIONS

a. The 455/465 use the double frequency non return to zero (NRZ) recording method.

b. The read/write head, in general, is a ring with a gap and a coil wound at some point on the ring.

c. During a write operation, a bit is recorded when the flux direction in the ring is reversed by rapidly reversing the current in the coil.

d. During a read operation, a bit is read when the flux direction in the ring is reversed as a result of a flux reversal on the diskette surface.

The 455/465 drives use the double-frequency (2F) longitudinal NRZ method of recording. Double frequency is the term given to the recording system that inserts a clock bit at the beginning of each bit cell thereby doubling the frequency of recorded bits. This clock bit, as well as the data bit, is provided by the using system. See figure 8-1.

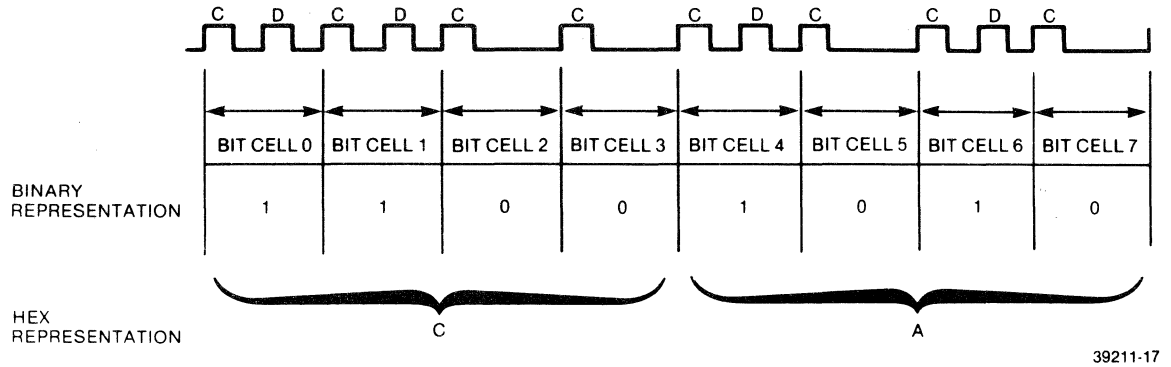


FIGURE 8-1. BYTE

The read/write head is a ring with a gap and a coil wound at some point on the ring. When current flows through the coil, the flux induced in the ring fringes at the gap. As the diskette recording surface passes by the gap, the fringe flux magnetizes the surface in a longitudinal direction. See figure 8-2.

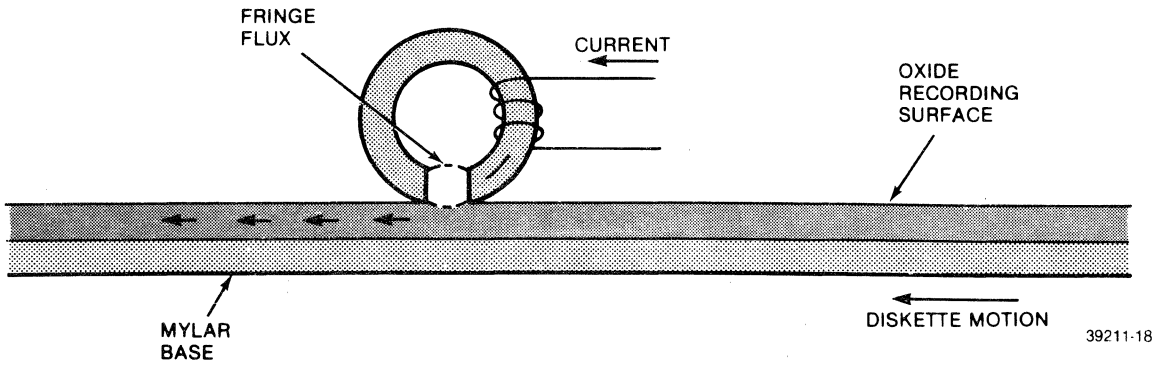


FIGURE 8-2. BASIC READ/WRITE HEAD

The drive writes two frequencies: 1F 62.5 k Hz and 2F 125 k Hz. During a write operation a bit is recorded when the flux direction in the ring is reversed by rapidly reversing the current in the coil. The fringe flux is reversed in the gap and hence the portion of the flux flowing through the oxide recording surface is reversed. If the flux reversal is instantaneous in comparison to the motion of the diskette, it can be seen that the portion of the diskette surface that just passed under the gap is magnetized one direction while the portion under the gap is magnetized in the opposite direction. This flux reversal represents a bit. See figure 8-3.

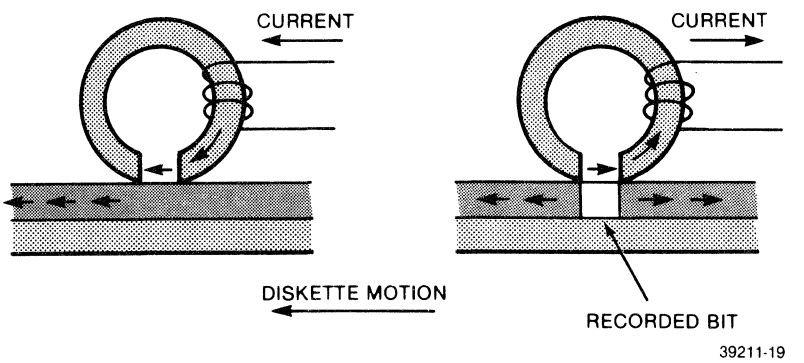


FIGURE 8-3. RECORDED BIT

During a read operation, a bit is read when the flux direction in the ring is reversed as a result of a flux reversal on the diskette surface. The gap first passes over an area that is magnetized in one direction and a constant flux flows through the ring and coil. The coil registers no output voltage at this point. When a recorded bit passes under the gap, the flux flowing through the ring and coil will make a 180° reversal. This means that the flux reversal in the coil will cause a voltage output pulse. See figure 8-4.

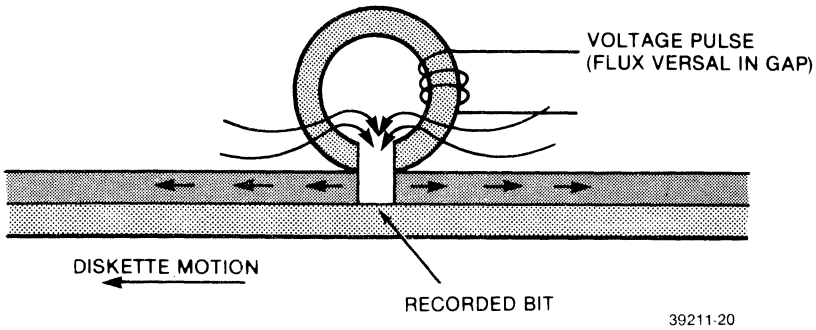


FIGURE 8-4. READING A BIT

These flux reversals produce an FM waveform which transmits data to and from the diskette. See figure 8-5.

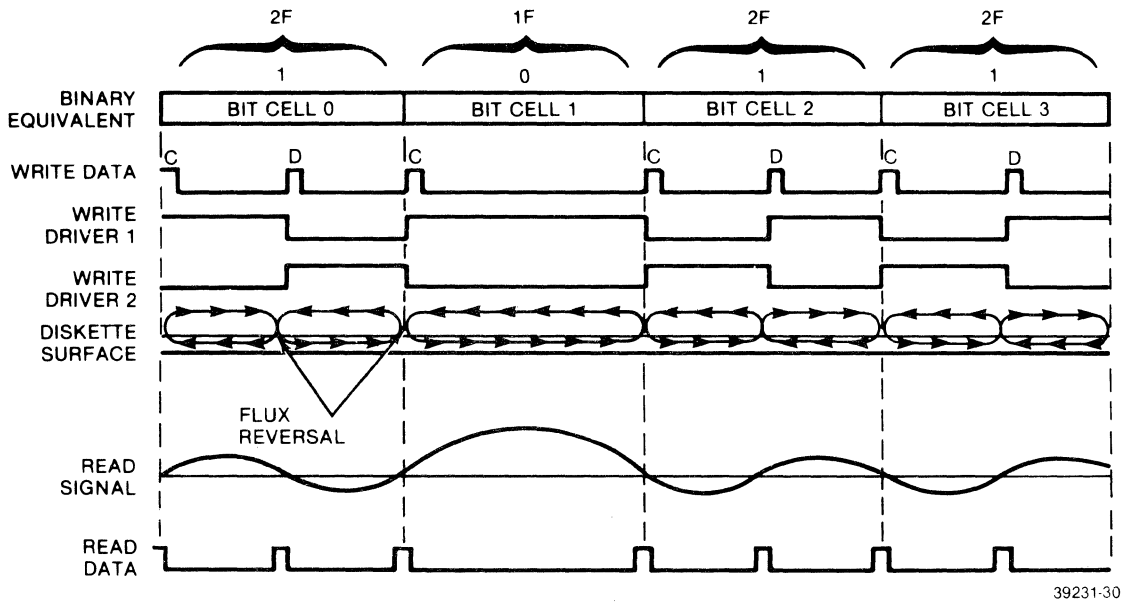


FIGURE 8-5. 1F AND 2F RECORDING FLUX AND PULSE RELATIONSHIP

8.3 READ/WRITE HEAD

a. The ceramic read/write heads each contain three coils.

b. When writing, the head erases the outer edges of the track to ensure that the data recorded will not exceed the 0.012 in. (455) or 0.006 (465) track width.

The read/write head contains three coils. Two read/write coils are wound on a single core, center tapped, and one erase coil is wound on a yoke that spans the track being written. The read/write and erase coils are connected as shown in figure 8-6.

During a write operation, the erase coil is energized. This causes the outer edges of the track to be trim erased so that the track being recorded will not exceed 0.012 in. (455) or 0.006 in (465) track width. Tunnel erasing allows for minor deviations in read/write head current so as one track is recorded, it will not "splash over" to adjacent tracks.

Each bit written will be directed to alternate read/write coils, thus causing a change in the direction of current flow through the read/write head. This will cause a change in the flux pattern for each bit. The current through either of the read/write coils will cuase the old data to be erased as new data is recorded.

During a read operation, the direction of flux changes on the diskette surface as it passes under the gap and current is induced into one of the windings of the read/write head. This results in a voltage output pulse. When the next data bit passes under the gap, another flux change takes place in the recording surface. This causes current to be induced in the other coil, producing another voltage output pulse of the opposite polarity.

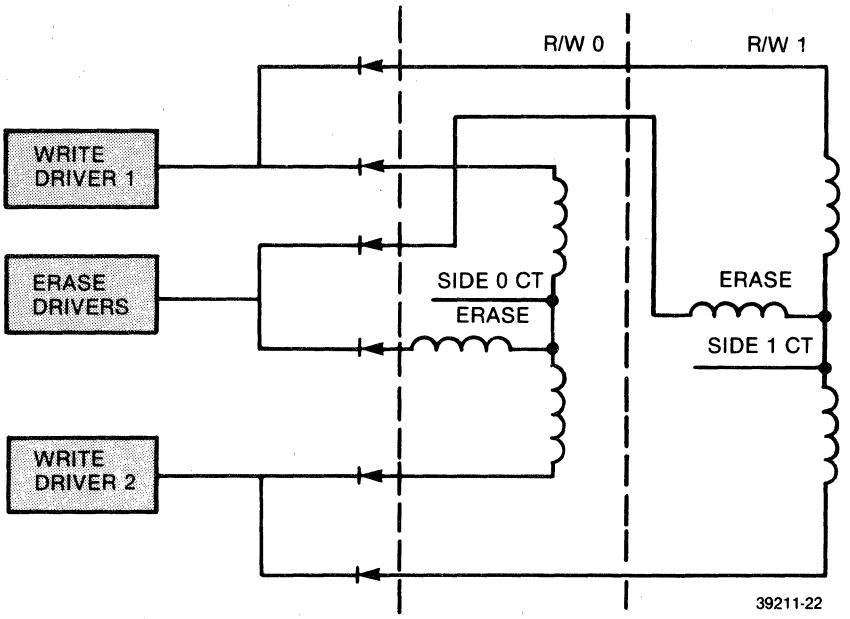


FIGURE 8-6. READ/WRITE HEADS

8.4 WRITE CIRCUIT OPERATION

a. The write data trigger flips with each pulse on the WRITE DATA line.

b. The write data trigger alternately drives one or the other of the write drivers.

c. WRITE GATE allows write current to flow to the write driver circuits if the diskette is not write protected.

d. Write current sensed allows erase coil current.

e. Heads are selected by grounding the appropriate center tap.

WRITE DATA pulses (clock and data bits) are supplied by the using system. The write trigger "flips" with each pulse. The outputs are fed to alternate write drivers.

WRITE GATE and NOT WRITE PROTECT are ANDed together and will cause write current to flow to the write driver circuits, which in turn causes the center tap switch to close and erase current to flow after the turn on delay of 400 μsec.

The output of one of the write drivers allows write current to flow through one half of the read/write coil. When the writer trigger "flips," th other write driver provides write current to the other half of the read/write coil.

The removal of WRITE GATE causes the turn off delay circuit to time out for 1.1 msec. At the end of the delay the center tap switch opens and the erase current source is turned off. See figure 8-7.

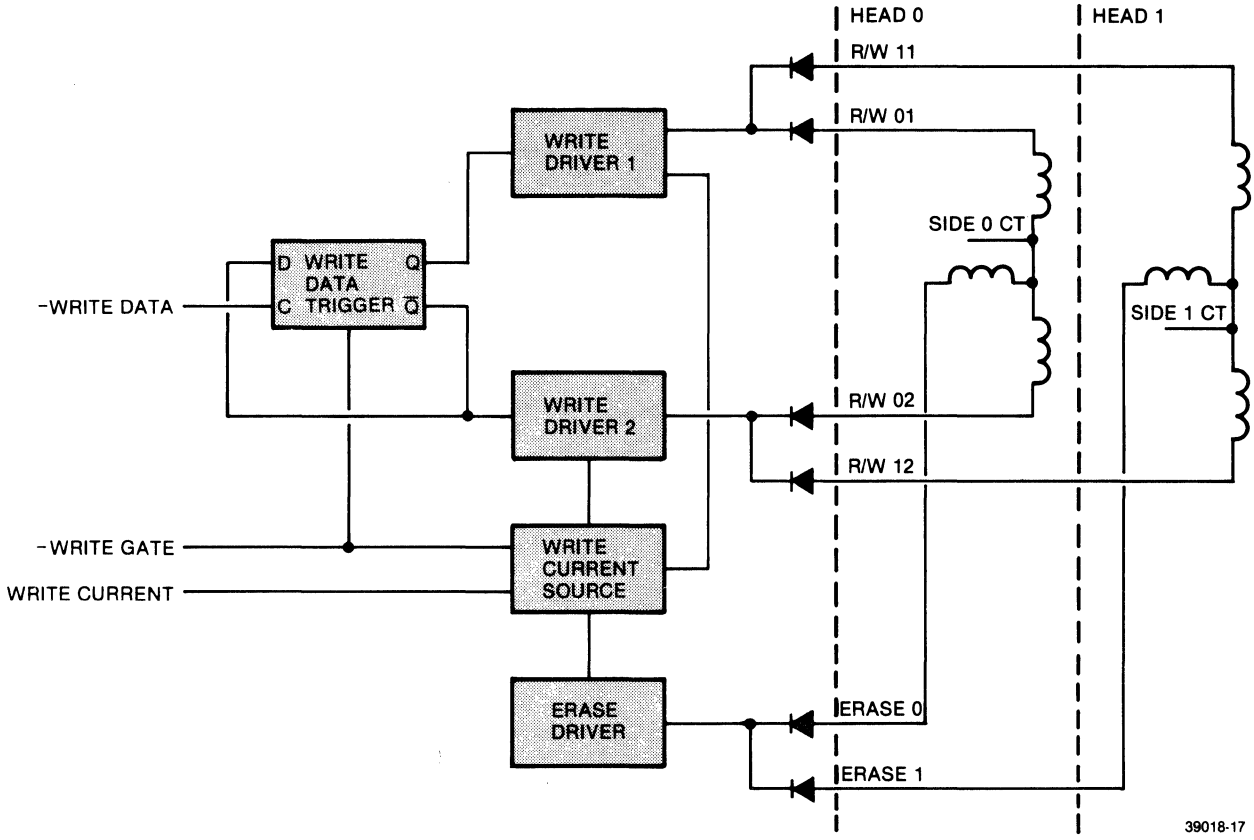


FIGURE 8-7. WRITE CIRCUIT FUNCTIONAL DIAGRAM

8.5 READ CIRCUIT OPERATION

a. Duration of all read operations is under control of the using system.

b. As long as the drive is selected and WRITE GATE is not active, the read signal is amplified and shaped and the square wave signals are sent to the interface as READ DATA.

When the using system requires data from the diskette drive, the using system must select the head and disable WRITE GATE. The read signal is then fed to the amplifier section of the read circuit. After amplification, the read signal is fed to a filter where the out of band noise is removed. The read signal is then fed to the differentiator amplifier.

Since a clock pulse occurs at least once every eight μsec and data bits are present once every four μsec, the frequency of the READ DATA varies (FM encoding only). The read signal amplitude decreases as the frequency increases. Note the signals in figure 8-8. The differential amplifier will amplify, differentiate, limit, and digitize the read signals (sine waves).

The drive has no data separator, only a pulse standardizer for the READ DATA signals.

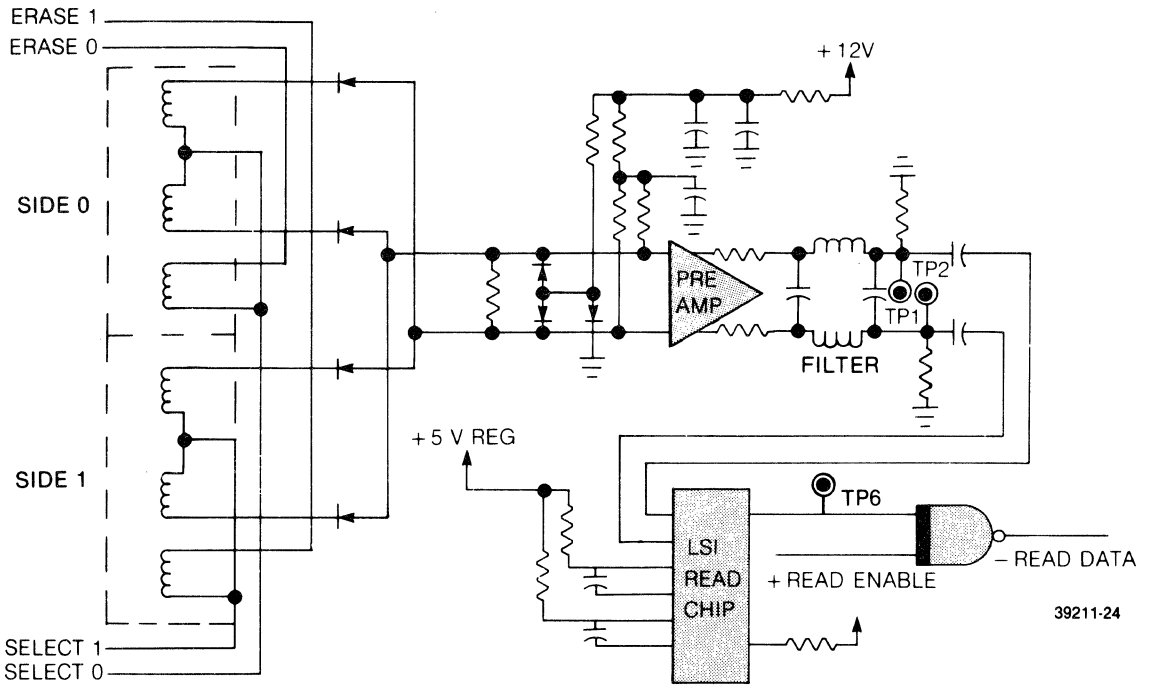


FIGURE 8-8. READ CIRCUIT

8.6 DRIVE MOTOR CONTROL

a. Start/Stop

b. Speed Control

c. Over Current Protection

d. Speed Adjustment

The motor used in the 455/465 is a dc drive motor with a separate motor on and off interface line. After activating the MOTOR ON line, a 500 msec delay must be introduced or the Ready line must be monitored to allow proper motor speed before reading or writing.

When MOTOR ON is activated at pin 16 of the interface, the mode will start by means of current flow through the motor windings. The motor speed control utilizes an integral brushless tachometer. The output voltage/frequency comparator will control the necessary current to maintain a constant motor speed of 300 rpm. Motor speed adjustment changes the voltage reference through a potentiometer.

8.7 INDEX DETECTOR

Each time an index or sector hole is moved past the index photo detector, a pulse is formed. This pulse is present on the interface as index/sector pin eight. Without a diskette in the drive, the ouptut line will be low and the using system must look for a transition to be a valid signals. The detector output is fed into a schmidt trigger with a level trigger latch back to maintain pulse stability while shaping the pulse. With output enable true, this pulse will be on the interface as a negative going pulse. See figure 8-9.

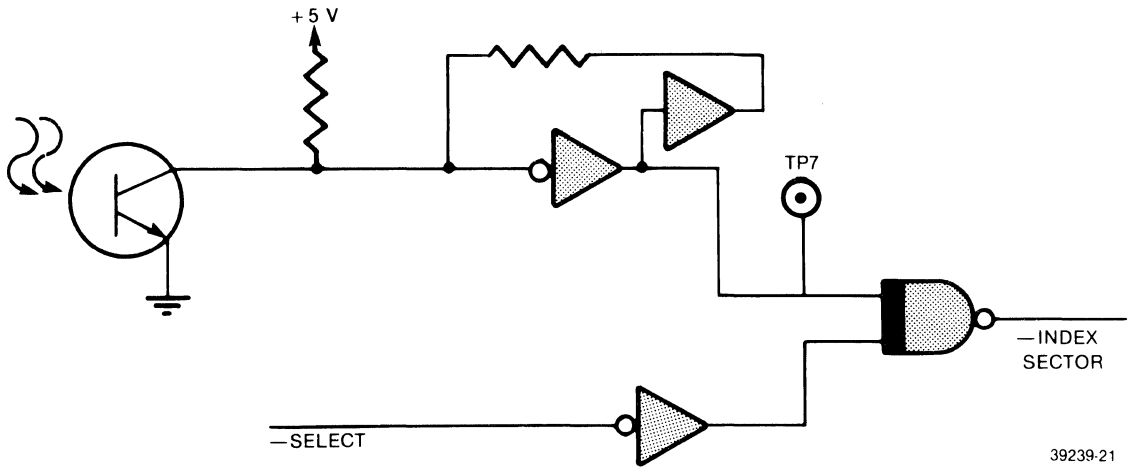


FIGURE 8-9. INDEX DETECTOR

8.8 TRACK ZERO INDICATION

Track 00 signal (pin 26) is provided to the using system to indicate when the read/write head is positioned on track 00. The track 00 indication is provided when the flag attached to the head carriage passes between the photo transistor and the photo detector. On track, DRIVE SELECT is ANDed with the photo detector output. These conditions will cause a track 00 indication to the interface.

8.9 TRACK ACCESSING

a. Stepper Motor (Four Phase)

b. Stepper Control Logic

c. Reverse Seek

d. Forward Seek

Seeking the read/write head from one track to another is accomplished by selecting the desired direction utilizing the DIRECTION SELECT interface line, loading the read/write head, and pulsing the STEP line. Mulitple track accessing is accomplished by repeated pulsing of the STEP line with WRITE GATE inactive until the desired track has been reached. Each pulse on the STEP line will cause the read/write head to move one track either in or out, depending on the DIRECTION SELECT line.

8.9.1 Stepper Motor

The four phase stepper motor turns the head actuator cam in two step increments per track for the 455 and one step increments for the 465. The band actuator and capstan move the heads track to track.

Two current modes are automatically enabled. The first step pulse will enable full current to the stepper motor. Within 35 msec after the last step pulse is issued, stepper motor current is automatically decreased to approximately 50 percent of its full value.

8.9.2 Stepper Control

During power on reset time, the stepper control counter is reset to zero. This causes phases -B and -A to be energized in the stepper. Figures 8-10 and 8-11 show the stepper control logic and timing.

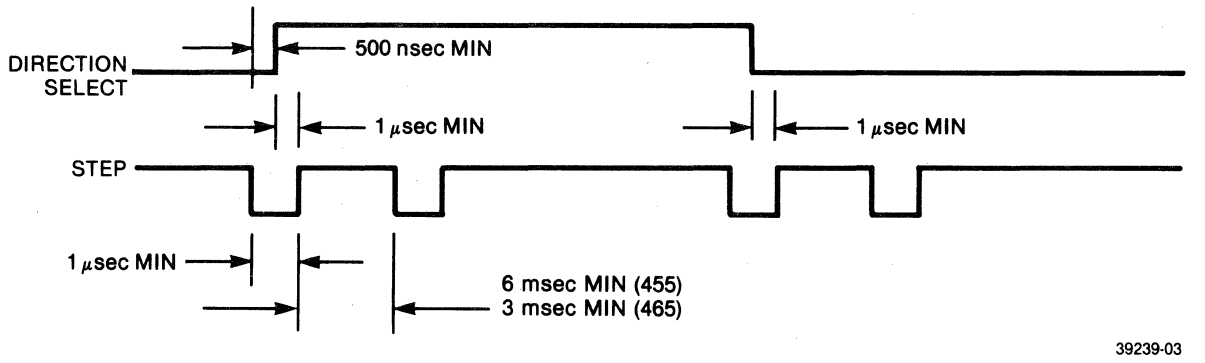


FIGURE 8-10. STEPPER TIMING

8.10 DRIVE SELECT

The 455/465 is configured to operate alone in a single drive system. It can be easily modified to operate with other drives in a daisy chained multiplexed drive system. This is done by selecting the specific drive address and jumpering the appropriate DRIVE SELECT line. See figure 8-12.

The "MX" option is used for single drive systems. By shorting "MX," the I/O lines are always enabled.

The "MS" option allows the motor to be enabled from DRIVE SELECT.

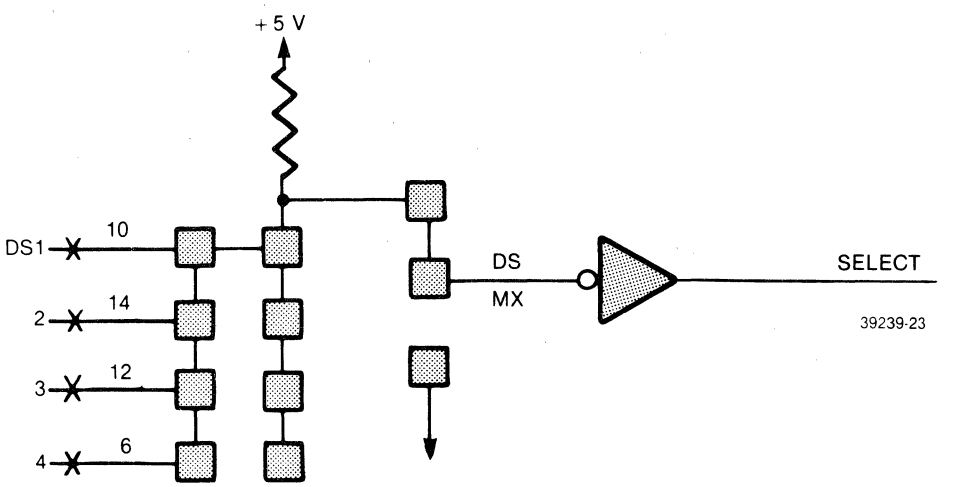


FIGURE 8-11. DRIVE SELECT

8.11 WRITE PROTECT

This interface signal is provided by the drive to indicate to the user when a write protected diskette is installed. The signal is logical 0 level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition to notifying the interface. If the "WP" trace is cut, writing to the diskette is inhibited unless a write protect label is installed over the notch. See figure 8-13.

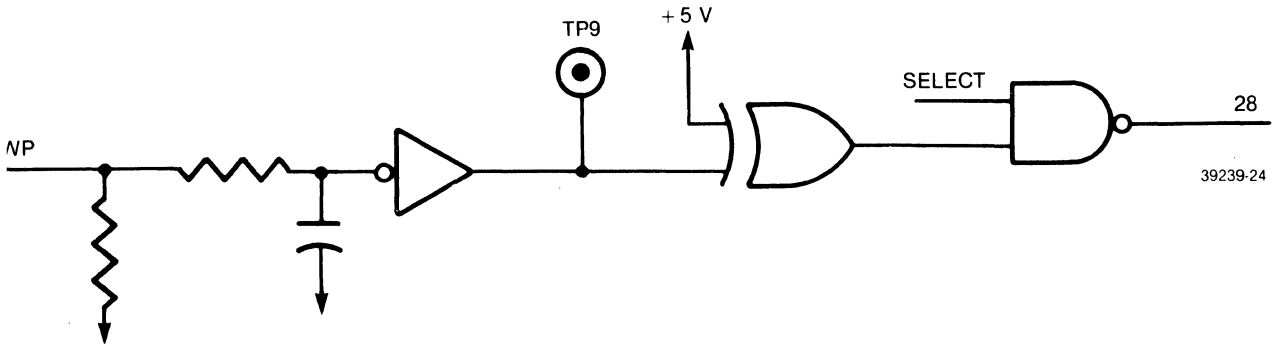


FIGURE 8-12. WRITE PROTECT

.12 READY

his interface signal gives the user an indication that a diskette is inserted correctly, the door is closed, and the drive up to speed.

SECTION IX
OPERATION PROCEDURES

1 INTRODUCTION

ıe Shugart 455/465 drives are designed for ease of use to facilitate a wide range of applications. The following ction is a guide for handling procedures on the minidiskette and minifloppy drive.

2 MINIDISKETTE LOADING

› load the diskette, open the door on the front panel, insert the diskette with label towards the door handle and ›se the door. A mechanical interlock prevents door closure without media insertion. This prevents head damage.

3 MINIDISKETTE HANDLING

› protect the diskette, the same care and handling procedures specified for computer magentic tape apply. These ecautionary procedures are as follows:

a. Return diskette to storage envelope whenever it is removed from drive.

b. Do not bend or fold diskette.

c. Store diskettes not for immediate use in their box.

d. Keep diskettes away from magnetic fields and from ferromagnetic materials which might become magnetized. Strong magnetic fields can distort data on disk.

e. Replace storage envelopes when worn, cracked, or distorted. Envelopes are designed to protect disk.

f. Place ID labels in correct location, never use in layers.

g. Do not write on plastic jacket with lead pencil or ball point pen. Use felt tip pen.

h. Do not use erasers.

i. Heat and contamination from a carelessly dropped ash can damage disk.

j. Do not expose diskette to heat or sunlight.

SECTION X
MAINTENANCE

10.1 MAINTENANCE AND MAINTENANCE EQUIPMENT

This section describes the necessary maintenance equipment, troubleshooting and maintenance procedures.

10.1.1 Alignment Diskette

The alignment diskette is used for verifying and adjusting the Shugart 455/465. Two alignment diskettes are available. The 455/465 has two read/write heads and requires written information on both surfaces. The Shugart 128 (48 tpi) alignment diskette should be used when performing service checks on the 455. The 465 requires the Shugart 126 (96 tpi) alignnment diskette.

The following adjustments and checks can be made using the Shugart 128/126 alignment diskettes.

		Shugart 455–128	**Shugart 465–126**
a.	Read/Write Head Radial Alignment	TRK 16	TRK 64
b.	Index Photo Detector Alignment	Set at TRK 38 Verified at TRK 01	Set at TRK 76 Verified at TRK 02
c.	Track 00 Head Position	TRK 00	TRK 00
d.	Azimuth Angle (not field adjustable)	TRK 33	TRK 64
e.	125 k Hz Signal Recorded to Check Head Position on Inside Track	TRK 34	TRK 79

Caution should be used not to destroy prerecorded alignment tracks. The write protect tab must be installed to prevent accidental writing on the alignment diskette. If the write protect option is used, remove the write protect tab.

10.1.2 Exerciser PCB

The exerciser PCB can be used in a stand alone mode, built into a test station, or used in a test for field service.

The exerciser will enable the user to make all adjustments and checkouts required on the 455/465 minidiskette drive. It has no intelligent data handling capabilities but can write a 2F 125 k Hz signal which is the recording frequency used for amplitude checks on the 455/465 drive. The exerciser can start and stop the drive motor, and enable read in the 455/465 to allow checking for proper read back signals.

10.1.3 Special Tools

The following special tools are available for performing maintenance on the 455/465.

Description	Part Number
Shugart 128 Alignment Diskette	54573
Shugart 126 Alignment Diskette	54382
Exerciser PCB	54157
Head Cable Extender	54578
Phillips Screw Drivers	Medium and Small
Oscilloscope	Textronix 465 or equivalent

10.2 DIAGNOSTIC TECHNIQUES

10.2.1 Introduction

Incorrect operating procedures, faulty programming, damaged diskettes, and "soft errors" created by airborne contaminants, random electrical noise, and other external causes can produce error falsely attributed to drive failure or misadjustment. Unless visual inspection of the drive discloses an obvious misalignment or broken part, attempt to repeat the fault with the original diskette, then attempt to duplicate the fault on a second diskette.

10.2.2 "Soft Error" Detection and Correction

Soft errors are usually caused by:

a. Airborne contaminants that pass between read/write heads and disk. Usually these contaminants can be removed by cartridge self-cleaning wiper.

b. Random electrical noise that usually lasts for a few microseconds.

c. Small defects in written data and/or track not detected during write operation may cause soft errors during read.

d. Improper grounding of power supply, drive, and/or host system. Refer to paragraph 3.2 for proper grounding requirements.

e. Improper motor speed.

The following procedures are recommended to recover from the above mentioned soft errors:

a. Reread track ten times or until such time as data is recovered.

b. If data is not recovered after using step "a", access head to adjacent track in same direction previously moved, then return to desired track.

c. Repeat step "a".

d. If data is not recovered, error is not recoverable.

10.2.3 Write Error

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a "write check." To correct the error, another write and check operation must be done. If the write operation isnot successful after ten attempts have been made, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error persists, the diskette should be replaced and the above procedure repeated. If the failure still exists, consider the drive defective. If the failure disappears, consider the original diskette defective and discard it.

10.2.4 Read Error

Most errors that occur will be "soft errors." In these cases, performing an error recovery procedure will recover the data.

10.2.5 Seek Error

a. Stepper malfunction.

b. Carriage binds.

c. To recover from a seek error, recalibrate to track 00 and perform another seek to the original track or do a read ID to find on which track the head is located.

10.3 TROUBLESHOOTING

Figures 10-1 through 10-5 provide troubleshooting procedures for the 455/465.

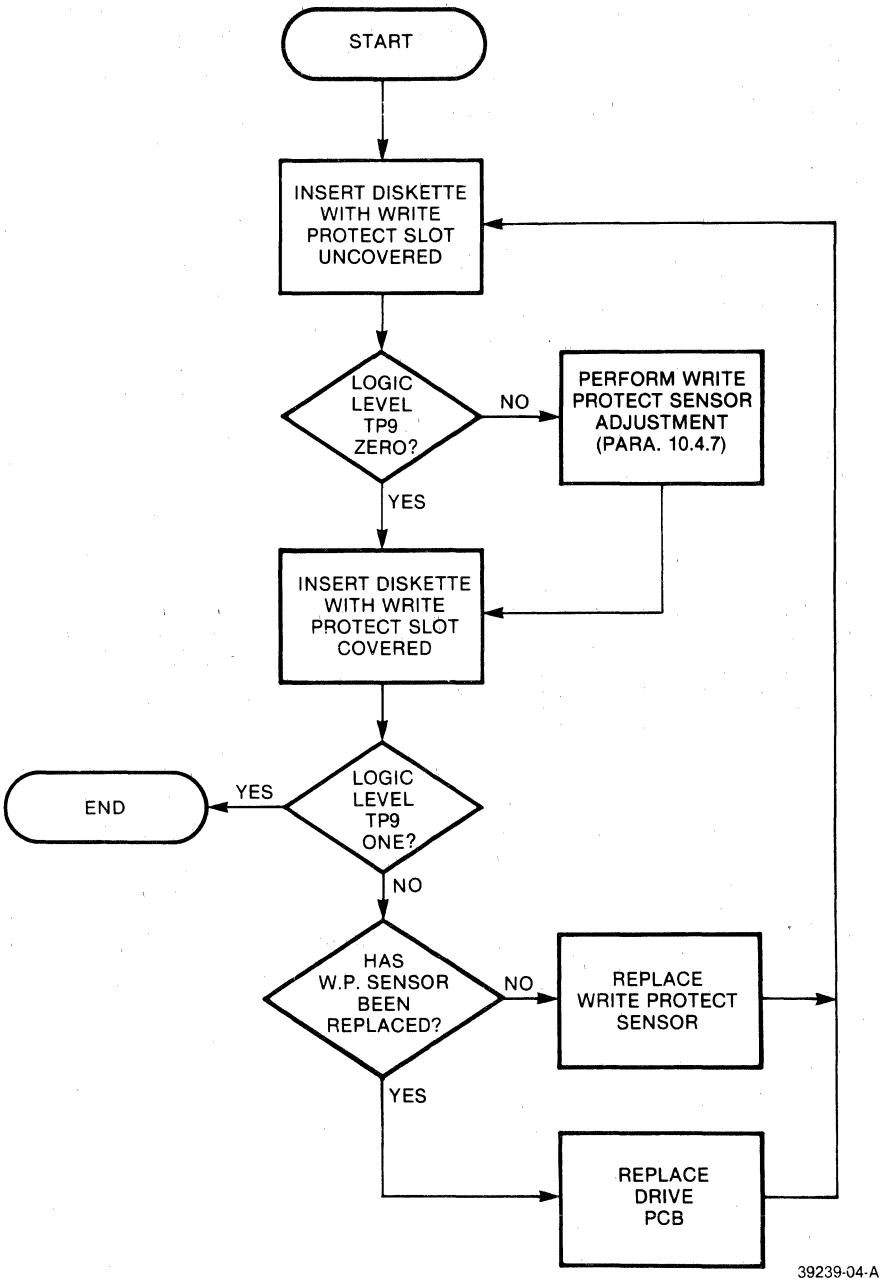


FIGURE 10-1. WRITE PROTECT INOPERATIVE

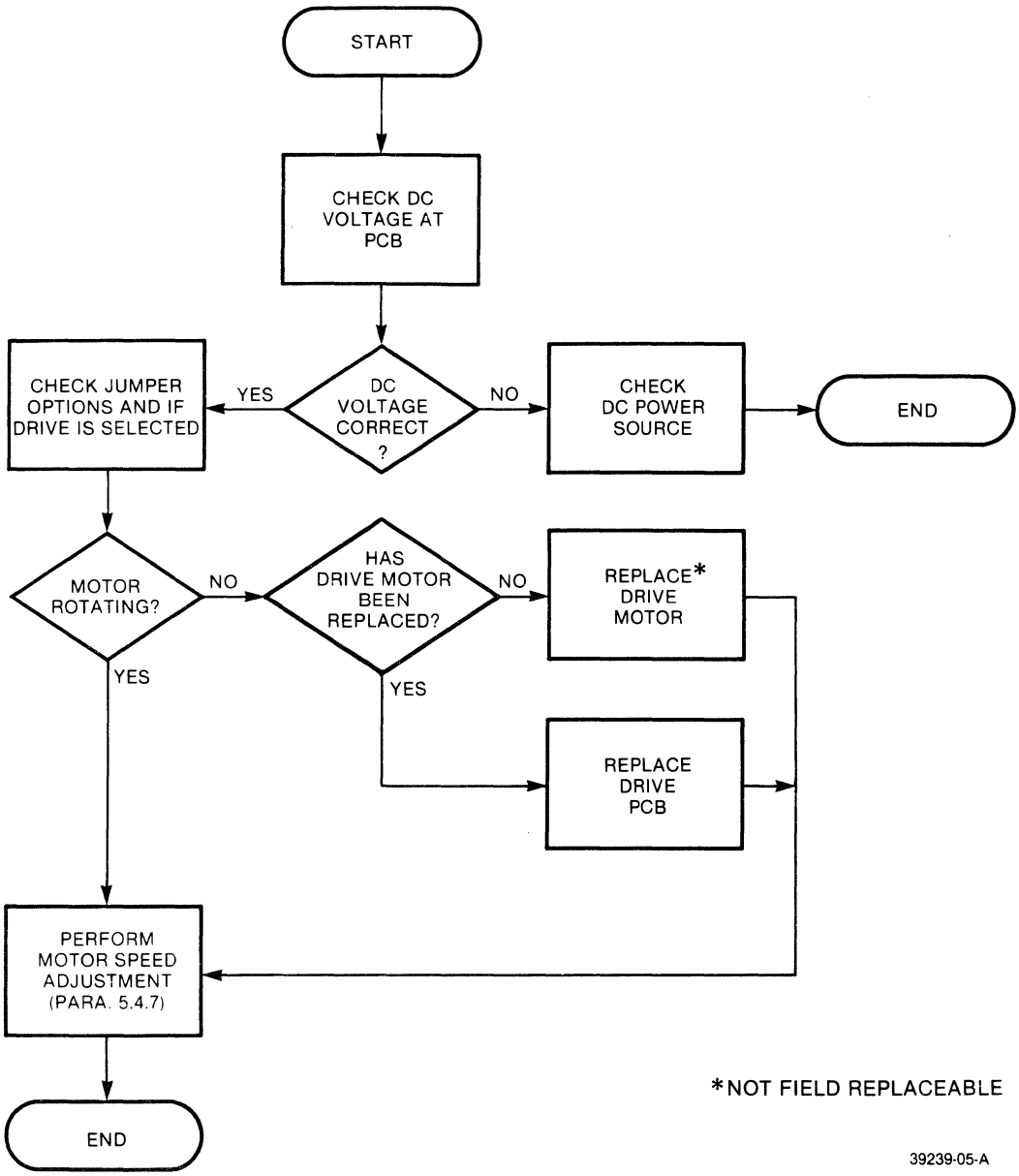


FIGURE 10-2. DISKETTE NOT ROTATING

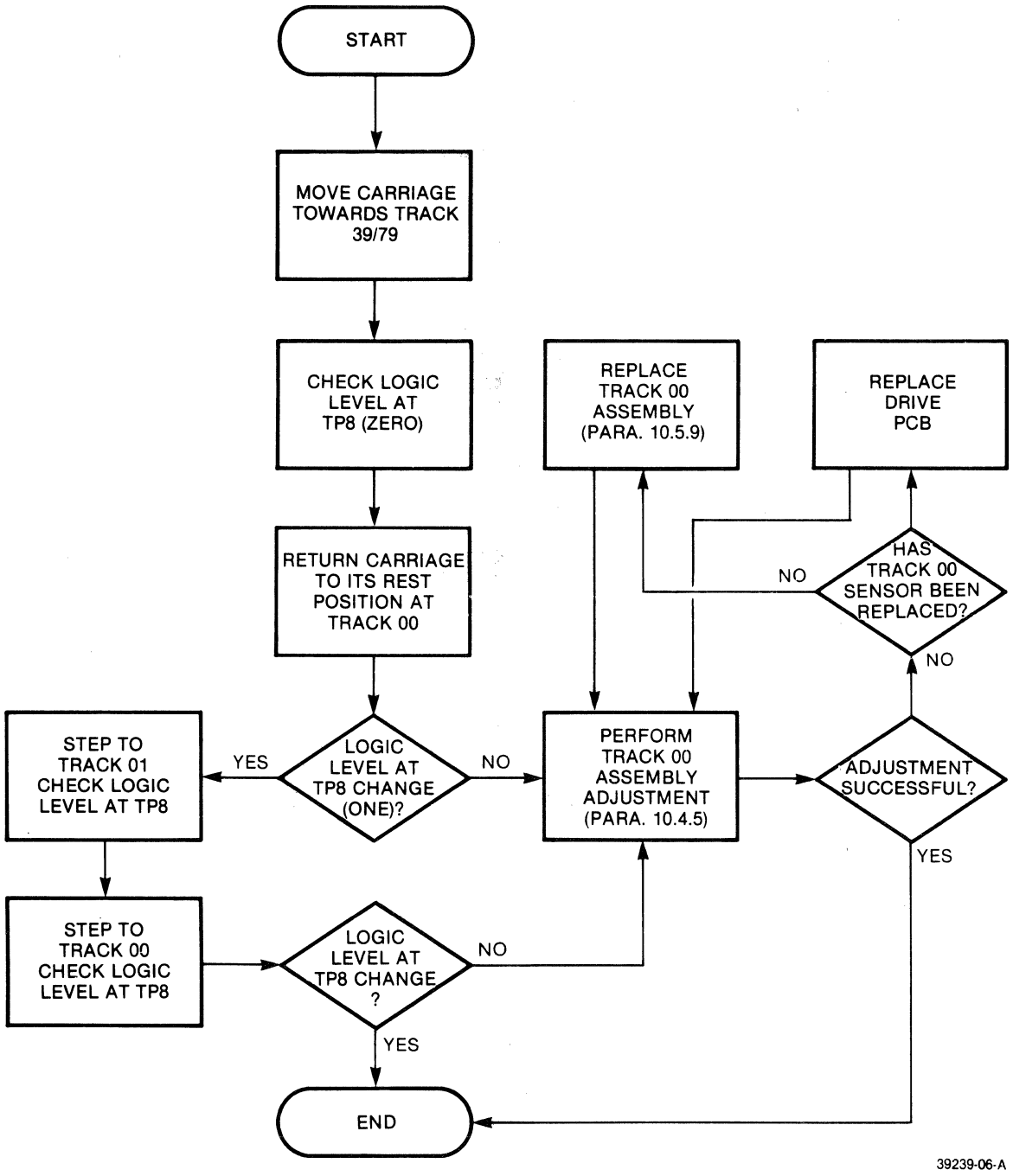


FIGURE 7-2. MLC 2 PCB COMPONENT LOCATIONS

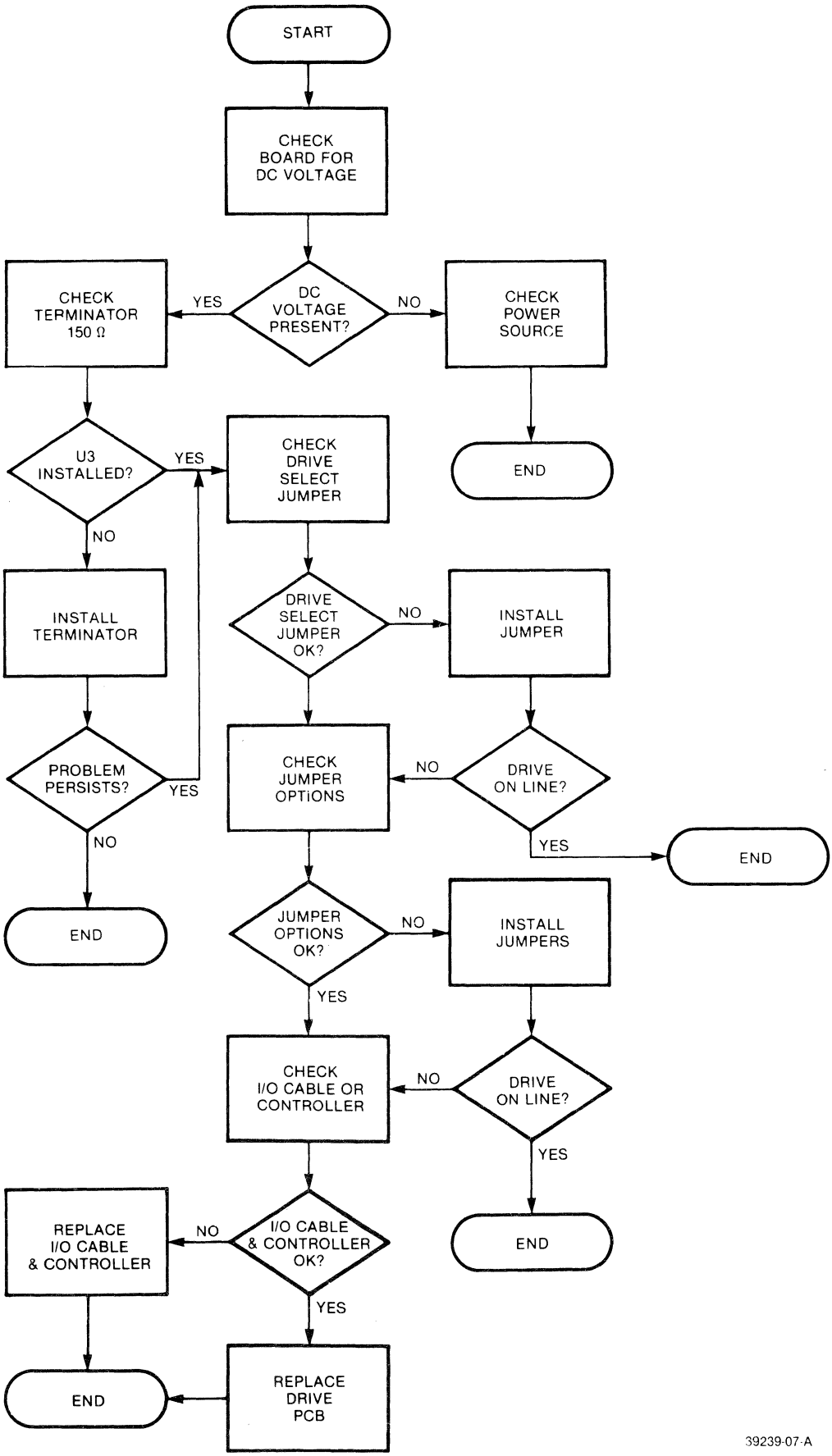


FIGURE 10-4. DRIVE NOT COMING ON LINE

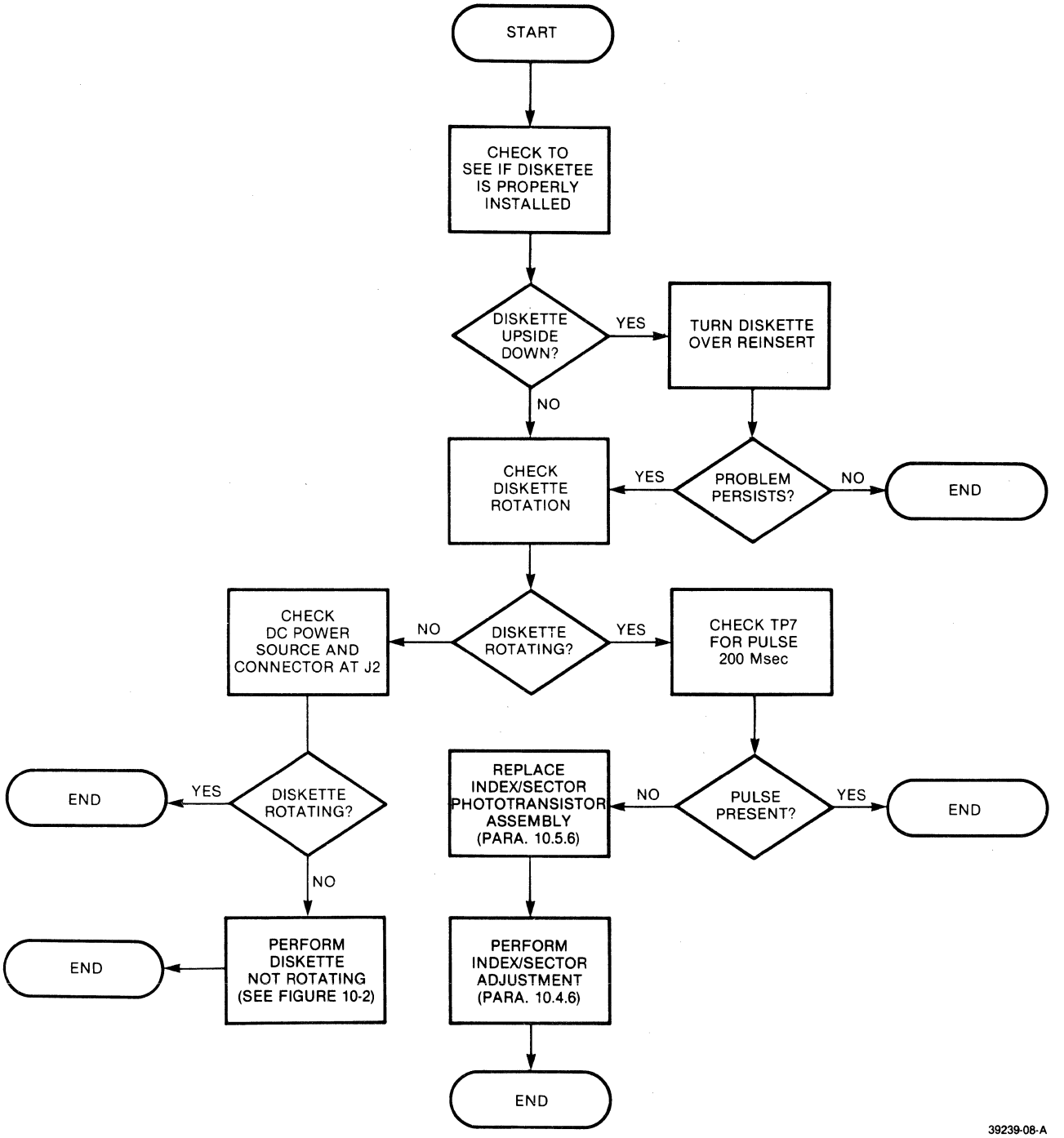


FIGURE 10-5. INDEX PULSE INOPERATIVE

10.4 ADJUSTMENTS

10.4.1 Head Radial Alignment

NOTE

The 465 read/write head assembly is aligned at factory and adjustment of head to head alignment is not field adjustable.

a. Insert alignment diskette (Shugart 128 for 455 and Shugart 126 for 465)

NOTE

Alignment diskette should be at room conditions for at least 24 hours before alignment checks.

b. Select drive and step head(s) to track 16 (455) or track 64 (465).

c. Sync oscilloscope external negative on TP7 (-INDEX). Set time base to 20 msec per division. This will display over one revolution.

d. Connect one probe to TP1 and other to TP2. Ground probes to PCB. Set inputs to ac, ADD, and invert one channel. Set vertical deflection to 50 mV/division.

e. Amplitude of two lobes must be within 70 percent of each other. If lobes do not fall within specification, continue with procedure (see figure 10-6).

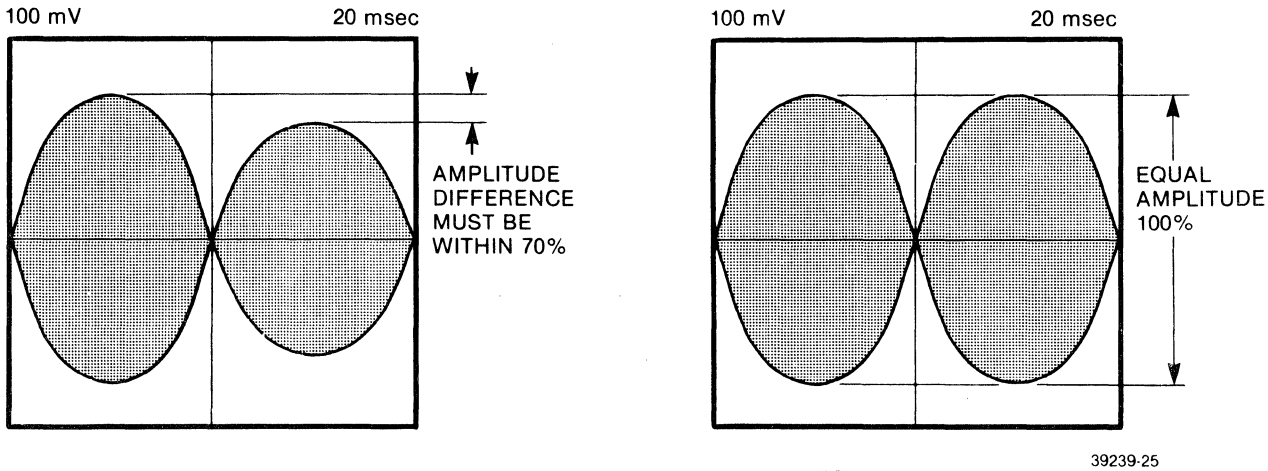


FIGURE 10-6. ALIGNMENT LOBES

f. Loosen two mounting screws, which hold stepper motor to base casting (see figure 10-7).

g. Adjust stepper motor.

h. When lobes are of equal amplitude, tighten motor plate mounting screws (see figure 10-7).

i. Check adjustment by stepping off track and returning. Check in both direction and readjust as required.

j. Whenever head radial alignment has been adjusted, track 00 detector must be checked. Refer to paragraph 10.4.4.

CAUTION

When tightening mounting screws, pressure *must* be applied to the rear of the stepper motor through the rectangular hole in the side of the casting to keep the motor bracket against the registering surfaces of the casting. Failure to do this will angle the band positioner causing track-to-track problems.

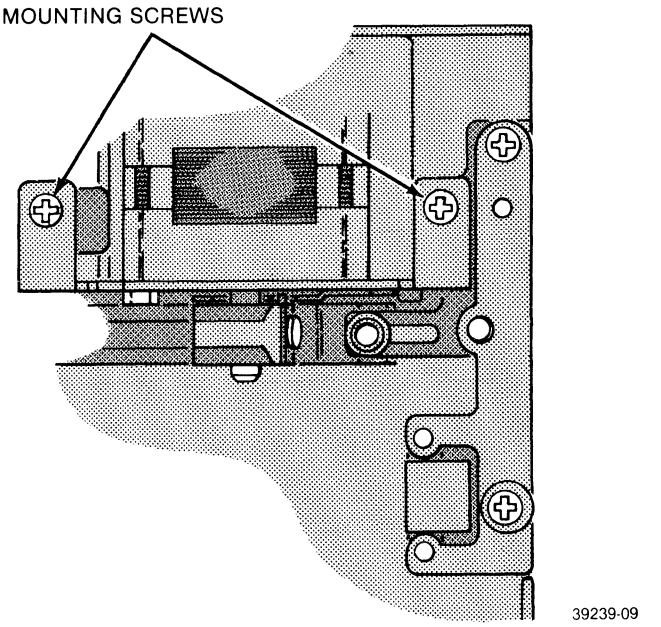


FIGURE 10-7. STEPPER MOTOR MOUNTING SCREWS

10.4.2 Read/Write Head(s) Azimuth Check

The azimuth is not field adjustable. If after performing this check the waveform on the oscilloscope is not within ±18 minutes (455) or ±21 minutes (465), the drive must be returned for replacement of read/write head assembly.

a. Install alignment diskette (Shugart 128 for 455 and Shugart 126 for 465).

b. Select drive and step to track 33 (455) or track 64 (465).

c. Sync oscilloscope external negative on TP7, set time base to 0.5 msec per division.

d. Connect one probe to TP1 and other to TP2. Invert one channel and ground probes to PCB. Set inputs to ac, ADD, and set vertical deflection to 50 mV per division.

e. Compare waveform to figure 10-8. If not within range shown, replace read/write head assembly.

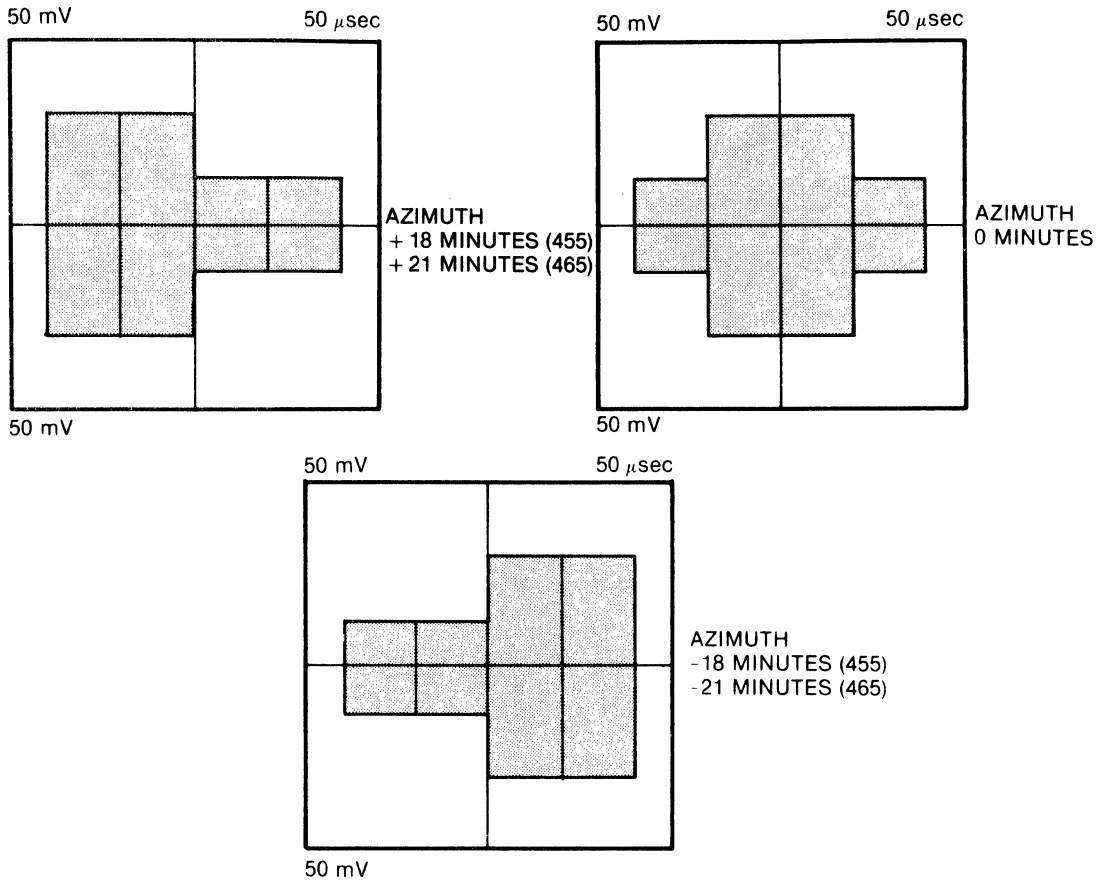


FIGURE 10-8. AZIMUTH CHECK

10.4.3 Head Amplitude Check

These checks are only valid when writing and reading back as described below. Ensure the diskette used for this check is not "worn" or otherwise shows evidence of damage on either side.

a. Install good media.

b. Start motor.

c. Select drive and step to track 39 (455) or track 79 (465).

d. Sync oscilloscope external on TP7 (+Index); connect one probe to TP2 and TP1 on drive PCB. Ground probes to PCB, ADD, and invert one input. Set volts per division to 50 mV and time base to 20 msec per division.

e. Select head 0 and write a 2F pattern on entire track. Average minimum amplitude peak-to-peak should be 100 mV.

f. Select head 1 and write a 2F pattern on entire track. Average minimum amplitude peak-to-peak should be 100 mV.

g. If either head fails to meet minimum amplitude specifications, continue with procedure.

h. Install fresh media and recheck.

i. Check motor speed as per paragraph 10.4.6.

10.4.4 Track Zero Detector Assembly Adjustment

a. Apply power to drive and install alignment diskette Shugart 128/126.

b. Select drive and step to track 00.

c. Sync oscilloscope external negative on TP7 (-Index). Set time base to 20 msec per division.

d. Connect one probe to TP1 and other to TP2. Ground probes to PCB. Set input to ac, ADD, and invert one channel. Set vertical deflection to 100 mV/division.

e. The 125 k Hz signal recorded should be observed at this time.

f. If 125 k Hz signal is not present, step forward one track at a time and verify 125 k Hz signal is present. Step only five tracks.

g. Step back towards track 00 detector and verify presence of 125 k Hz signal. Repeat stepping until signal is found.

h. Once 125 k Hz signal is present on oscilloscope, carriage is located at track 00. Disconnect probes from TP1, TP2, and TP7. Connect one channel to TP8 and set input to dc. Set vertical deflection to 2 V per division. Trigger oscilloscope on selected input channel.

i. Step to track 01 and verify that TP8 goes to zero.

j. If not, loosen track 00 bracket.

k. Set drive to seek alternately between tracks 01 and 02 (455); 02 and 03 (465).

l. Adjust eccentric until a 50 percent duty cycle is obtained (see figure 10-9).

m. Tighten track 00 bracket and recheck timing.

n. If same signal is obtained, remove alignment diskette, power down drive, and reinstall PCB. If same signal is not obtained, repeat steps "k" through "n".

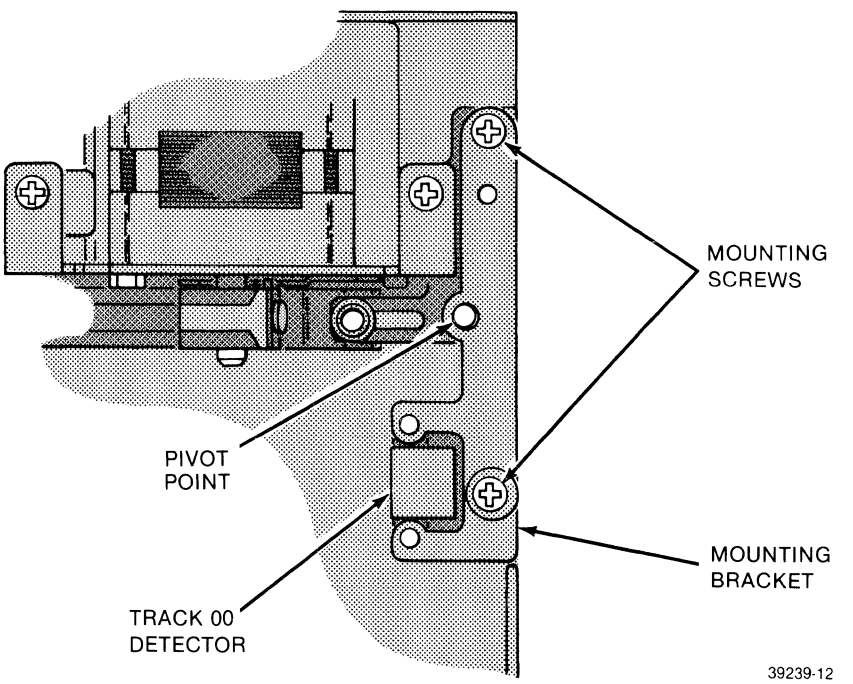


FIGURE 10-9. TRACK ZERO ADJUSTMENT

10.4.5 Index/Sector Timing Adjustment

a. Insert alignment diskette Shugart 128/126.

b. Start motor and select head 0.

c. Step carriage to track 01 (455) or track 02 (465).

d. Sync oscilloscope external positive on TP7 (+Index). Set time base to 50 μsec/division.

e. Connect one probe to TP1 and other to TP2. Ground probes to PCB. Set inputs to ac, ADD, and invert one channel. Set vertical deflection to 500 mV/division.

f. Observe timing between start of sweep and first data pulse. This should be 250 ± 150 μsec. If timing is not within tolerance, continue on with adjustment. See figure 10-10.

g. Loosen mounting screw in index detector block until assembly is just able to be moved. See figure 10-11.

h. Step carriage to track 38 (455) or track 76 (465).

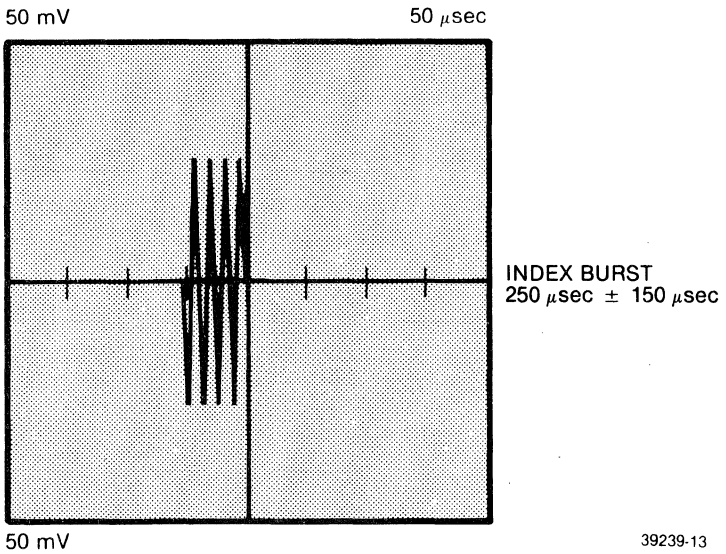
i. Observing timing, adjust detector until timing is 250 ± 150 μsec. Ensure that detector assembly is against registration surface on hub frame.

j. Tighten mounting screw.

k. Step carriage to track 01 (455) or track 02 (465).

l. Recheck timing.

m. Repeat for head 1.



☆ **FIGURE 10-10.** INDEX BURST

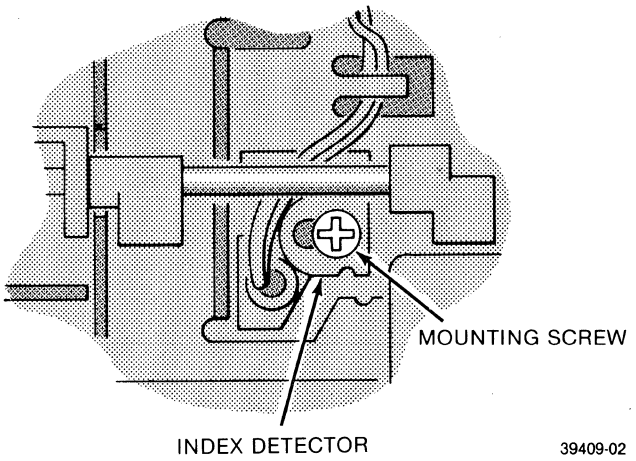


FIGURE 10-11. INDEX DETECTOR

10.4.6 Motor Speed Adjustment (Using a Frequency Counter)

a. Install 128/126 or 154/155 diskette; start motor and step to track 32.

b. Connect frequency counter to TP7 (+Index) on drive PCB.

c. Adjust pot located on the motor PCB for 5 ± 0.05 Hz (Period = 200 ± 4 msec).

10.4.7 Write Protect Detector

a. Insert diskette into drive. Write protect notch must be open.

b. Set oscilloscope to AUTO SWEEP, 2 V/division. Monitor TP9.

c. Check to see if logic level changes when diskette is removed.

10.4.8 PCB Test Point Locations

Test points on the 455 and 465 are as follows:

Title	Designation	Description
+Read Waveform -Read Waveform	TP-1 TP-2	Differential head voltage waveform after amplification and low-pass filter
	TP-3	Not used
	TP-4	Not used
Ground	TP-5	Tied to ground plane
+Digital Read Data	TP-6	A positive pulse with the leading edge corresponding to the transition time of the recorded signal
+Index Pulse	TP-7	A positive pulse corresponding to the time which the index detector transistor is turned on by the index LED
-Track 00 Detector	TP-8	A negative level corresponding to the track 00 detector being off
+Write Protect Detector	TP-9	A positive level corresponding to write protect dectector being off, (i.e., disk protected)
Signal Ground	TP-10	Tied to ground plane
	TP-11	Not used
-Step Pulse	TP-12	A buffered negative pulse equal to pin 20 of interface connector J-1
-Motor On	TP-13	A buffered negative level equal to pin 16 of interface connector J-1
	TP-14	Not used
Ground (dc)	TP-15	Tied to ground plane

See figure 10-12 for test point locations.

NOTE

PCB component locations for P/N 25287 (465) will be supplied at a later date. Test point locations for both the PCB's are the same. See figure 13-2 (schematic) for details.

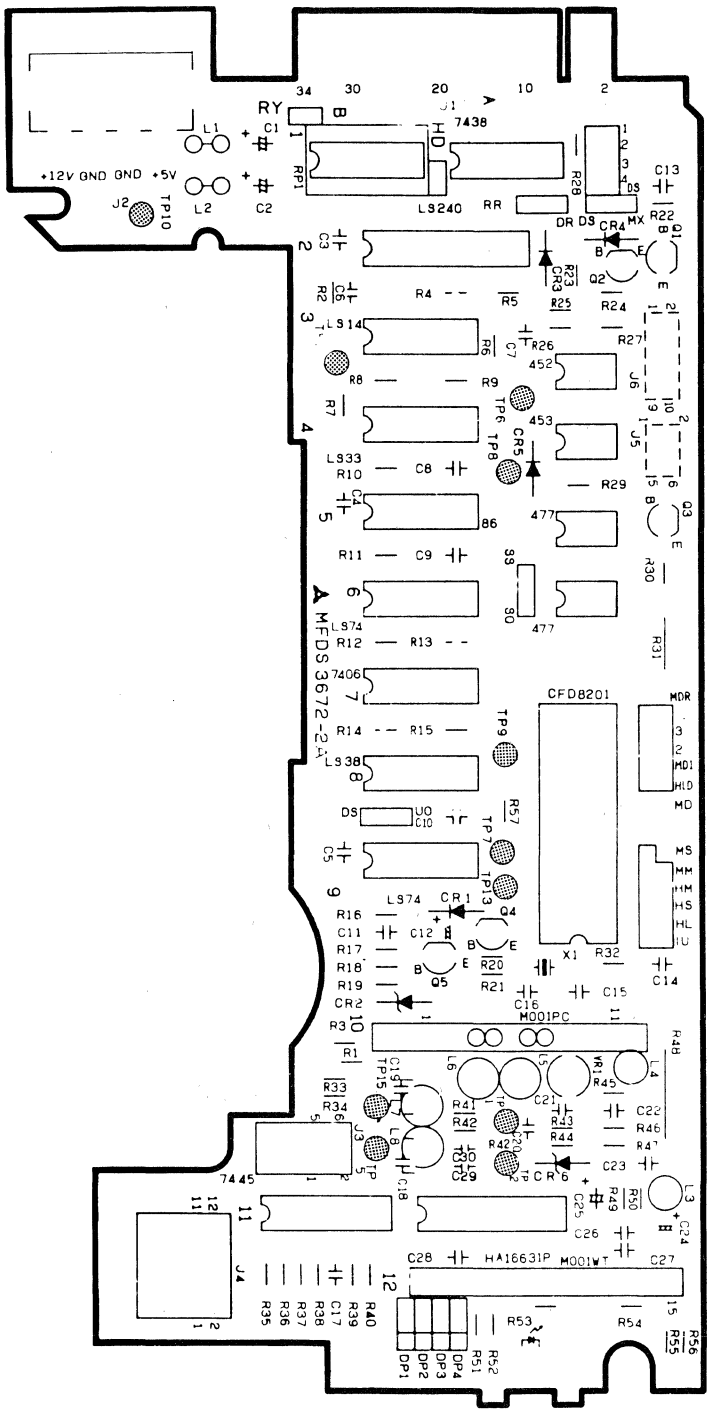


FIGURE 10-12. PCB COMPONENT/TEST POINT LOCATIONS, P/N 25284 (455), P/N 25286 (465)

10.5 REMOVALS AND REPLACEMENTS

NOTE

Read the entire procedure before attempting a removal or replacement.

10.5.1 Faceplate Latch

a. Open door. Remove door latch.

b. Remove mounting screw on each side of faceplate. Pull faceplate forward and away from drive casting.

c. To reinstall, reverse the above procedure.

d. No re-adjustment is required after replacement.

10.5.2 Direct Drive Motor Assembly

This assembly is not recommended for field replacement.

10.5.3 Head and Carriage Assembly

This assembly is not recommended for field replacement.

10.5.4 Stepper Motor and Actuator Assembly

This assembly is not recommended for field replacement.

10.5.5 Clamp Hub Assembly

a. Remove PCB.

b. Open door.

c. Remove clamp assembly front and rear screws.

d. To reinstall: Position hub clamp with spacer and spring in place onto spindle hub. (Large end of spring is placed against hub frame.)

e. Press hub frame down towards spindle until hub shaft is pushed through mounting hole in hub frame.

f. Reinstall faceplate. Re-adjustment is not required.

10.5.6 Write Protect Sensor and Index Detector Assembly

a. Remove connector from PCB.

b. Remove mounting screw from write protect assembly. This will free assembly.

c. Remove index detector screw to free detector.

d. Reverse instructions to reinstall.

10.5.7 Track Zero Photo Detector Assembly

a. Remove PCB and shields from drive.

b. Remove: white wire from J6 Pin 2,
green wire from J6 Pin 12,
yellow wire from J6 Pin 10.

c. Loosen mounting bracket screws.

d. Remove two screws securing LED housing to track 00 plate.

e. To reinstall, reverse above procedure.

f. Adjust as directed in paragraph 10.4.5.

SECTION XI
SPARE PARTS

Shugart Corporation, in its commitment to provide quality service to its customers, has available a dedicated and professional Spare Parts/Logistic support group to support the OEM customer base as well as the end user.

11.1 ROUTINE ORDER ENTRY

Routine orders (domestic open accounts) in the U.S. may be placed with Shugart Corporation by phone, facsimile, TWX or by mail. All verbal orders will be booked as received but will require confirming purchase documents before the order is processed for confirmation or shipment.

PHONE: (408) 733-7900 (Ask operator for Spares)

TWX: (910) 339-9355

FACSIMILE: (408) 735-7486

MAIL: Shugart Corporation
475 Oakmead Parkway
Sunnyvale, CA 94086 (U.S.A.)
ATTN: Spare Parts Department

11.2 EMERGENCY ORDER ENTRY

Request for parts required on an emergency basis should be communicated to Shugart Corporation by either TWX or phone. Be particularly careful to ensure that all applicable information is communicated.

11.3 OPTIONAL SOURCING

Spare parts for Shugart products are additionally available from Hamilton/Avnet for customers in the United States and Canada. Orders may be placed by phone to the following numbers:

(800) 521-3387

(800) 521-7088 (California only)

SECTION XII
ILLUSTRATED PARTS CATALOG

12.1 DESCRIPTION

The Illustrated Parts Catalog (IPC) is provided for the users to identify parts in an assembly. The figures precede the parts listing and appear either directly above the list or on the next page. The first column of the IPC lists the referenced part in the figures. The second column refers to the Shugart part number for that part. The third column describes the name and description of the part. The fourth column describes the quantity used for that assembly.

12.2 QUANTITY PER ASSEMBLY

The quantity listed is the quantity used on basic drive assembly as shown in the figure.

12.3 RECOMMENDED SPARE PARTS STOCKING GUIDE

The spare parts stocking guide is broken down into three levels. These levels are: Site or Field Support Engineer (level 1), Branch Office (level 2), and Depot or Headquarters (level 3). It is assumed that the Site is replenished by the Branch immediately, and the Branch is replenished by the Depot within 30 days.

The inventories that the three levels should maintain are:

Site	1 to 20 machines
Branch	1 to 100 machines
Depot	Unlimited
Depot Parts Only	
Branch Replenishment	Same as Branch ratio

Table 12-2 shows the spare parts required to support the Shugart 455/465 drives in the field.

NOTE

Some Depot parts are only unique to the depot. Stocking levels to back up Branch stocks are shown. These quantities are only a guide and may exceed or not meet each individual requirement. Requirements can vary due to usage, applications, and repair philosophies. This guide should be modified as required.

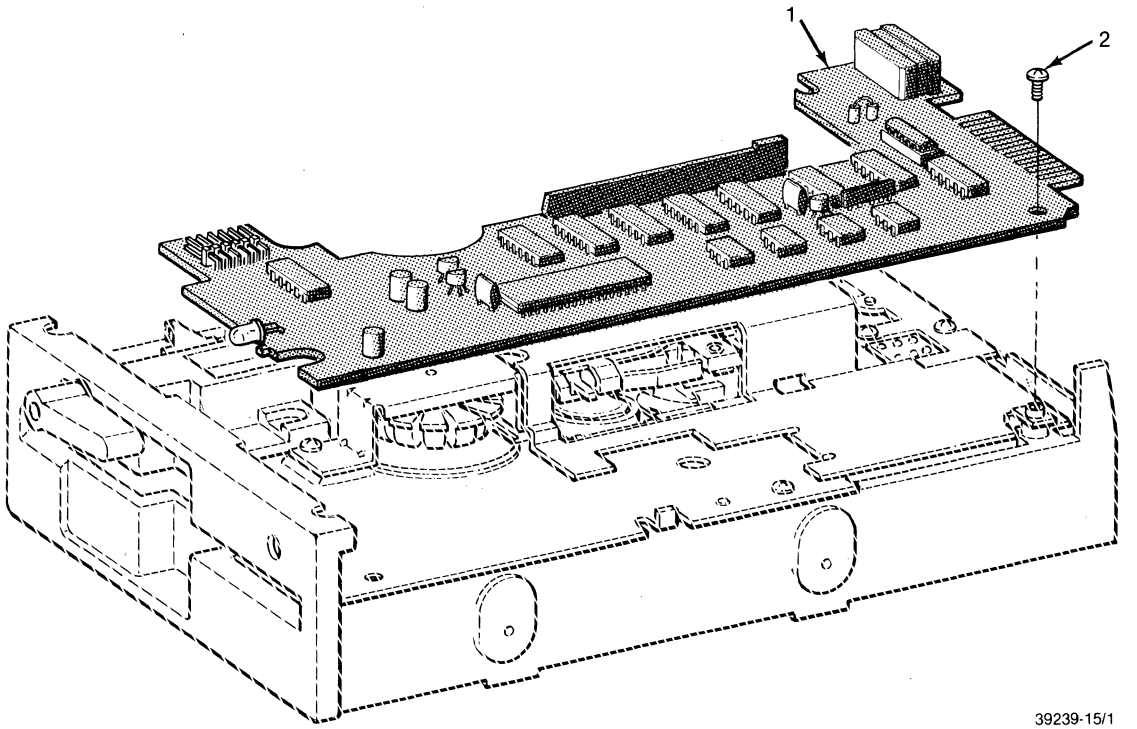


FIGURE 12-1. 455/465 BASIC DRIVE ASSEMBLY (SHEET 1 OF 4)

455/465 BASIC DRIVE ASSEMBLY

REFERENCE NUMBER	PART NUMBER	DESCRIPTION	QTY
Ref	51756	455/465 MINIFLOPPY™ DRIVE	
1	25284	455 PCB	1
	25286	465 PCB	1
2	11477	SCREW	2

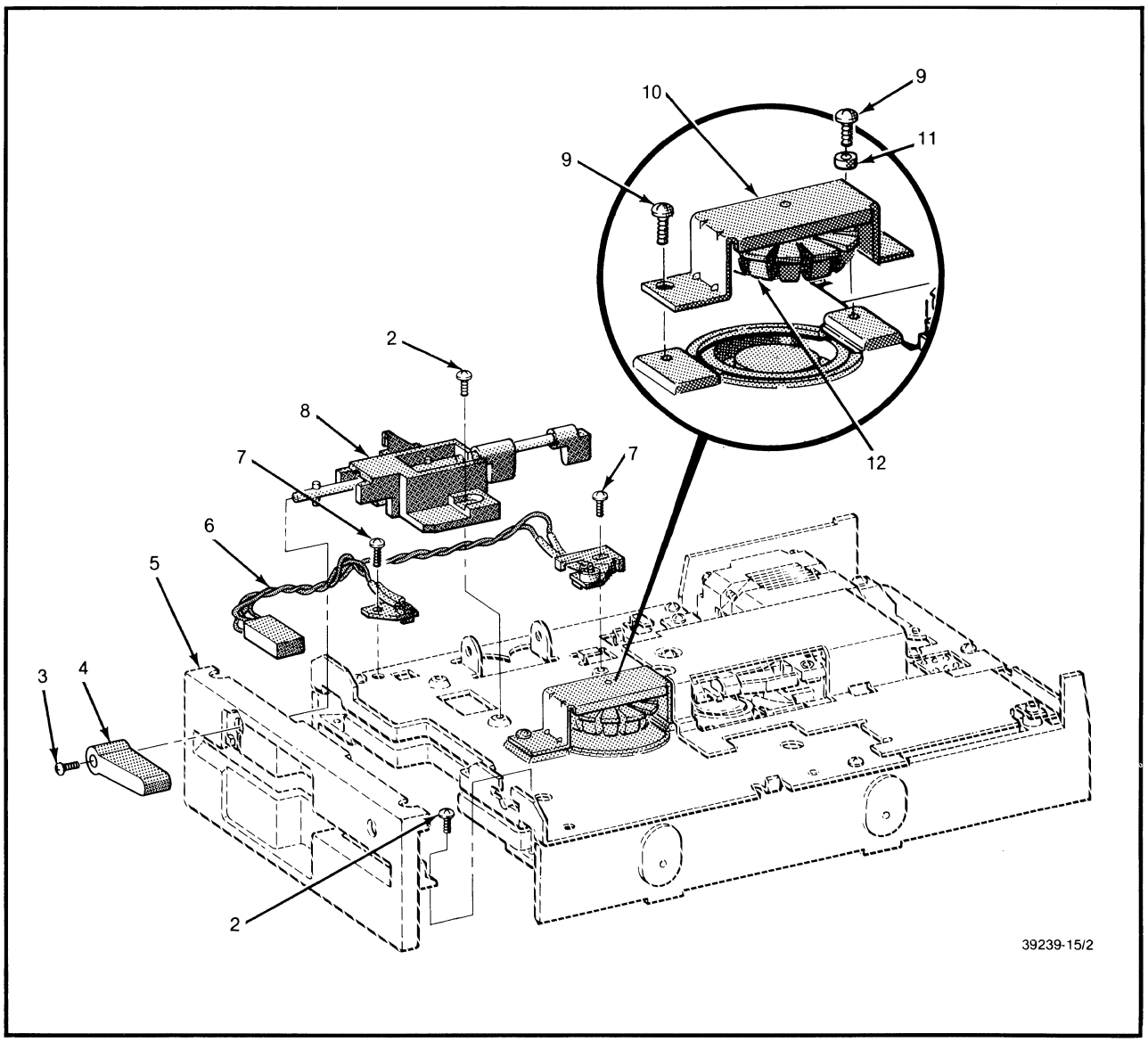


FIGURE 12-1. 455/465 BASIC DRIVE ASSEMBLY (SHEET 2 OF 4)

455/465 BASIC DRIVE ASSEMBLY (CONT.)

REFERENCE NUMBER	PART NUMBER	DESCRIPTION	QTY
3	11464	SCREW	1
4	51782	CLAMP HANDLE	1
5	52446	FACEPLATE	1
6	54758	WRITE PROTECT/INDEX DETECTOR	1
7	11475	SCREW	2
8	51896	GUIDE SHAFT ASSEMBLY	1
9	11450	SCREW	2
10	51898	CLAMP CAM ASSEMBLY	1
11	51788	SPACER	1
12	54765	COLLET	1

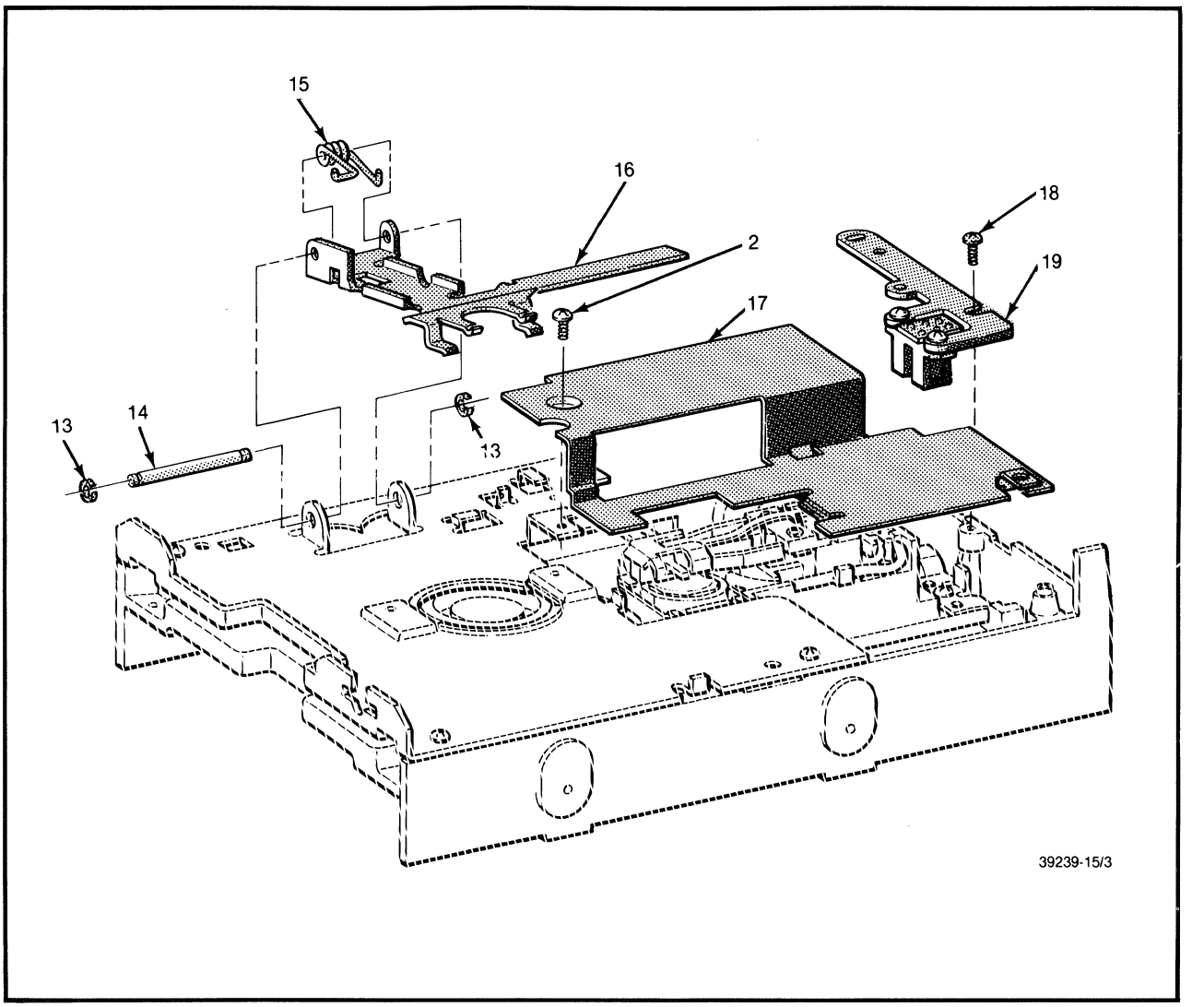


FIGURE 12-1. 455/465 BASIC DRIVE ASSEMBLY (SHEET 3 OF 4)

455/465 BASIC DRIVE ASSEMBLY (CONT.)

REFERENCE NUMBER	PART NUMBER	DESCRIPTION	QTY
13	11461	E-RING	2
14	51785	LIFT SHAFT	1
15	51784	LIFT SPRING	1
16	51786	LIFTER	1
17	54768	SHIELD PLATE	1
18	11468	SCREW	1
19	54762	TRACK 00 SENSOR	1

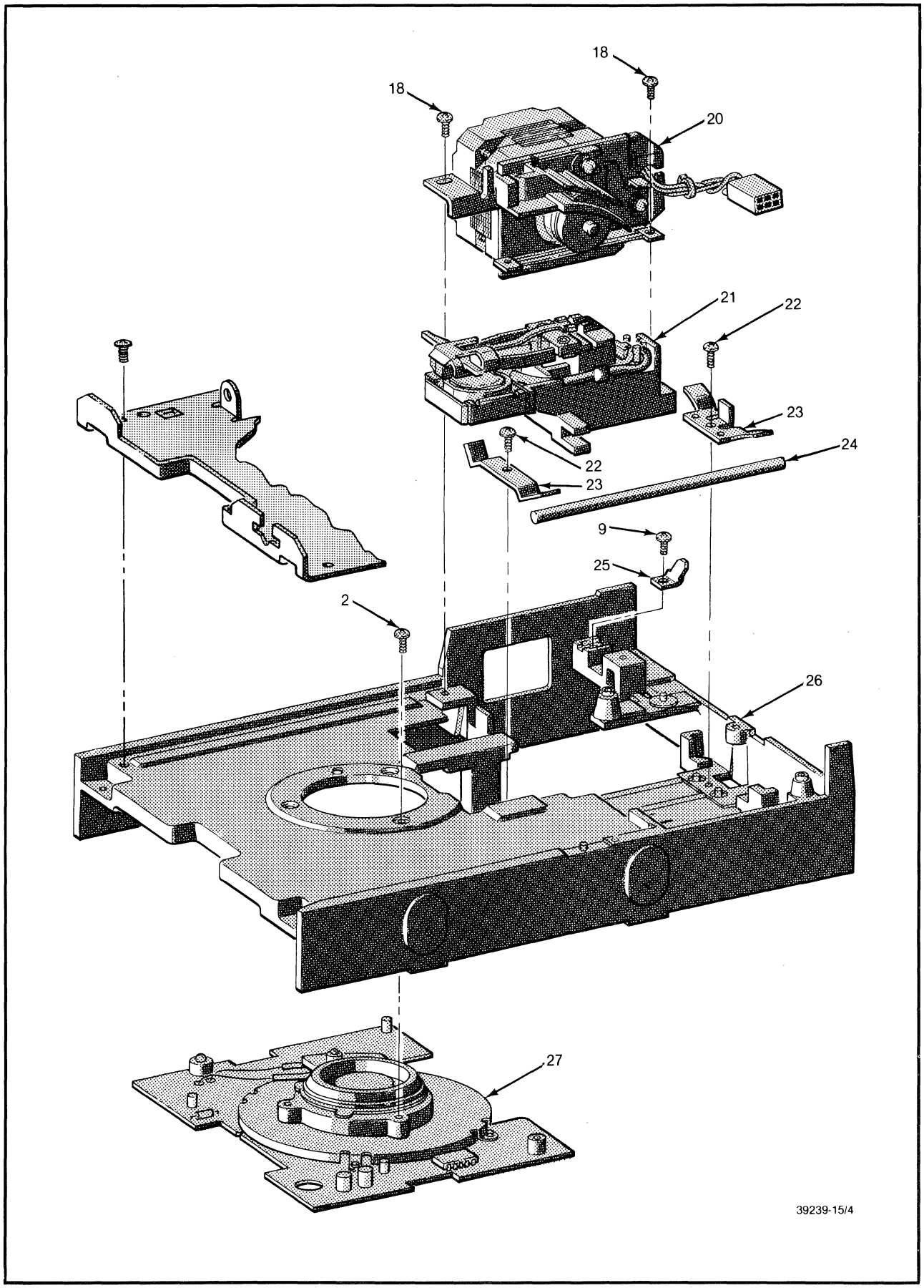


FIGURE 12-1. 455/465 BASIC DRIVE ASSEMBLY (SHEET 4 OF 4)

455/465 BASIC DRIVE ASSEMBLY (CONT.)

REFERENCE NUMBER	PART NUMBER	DESCRIPTION	QTY
20	52445*	STEPPER MOTOR ASSEMBLY	1
21	54773*	455 HEAD CARRIAGE ASSEMBLY	1
	54814*	465 HEAD CARRIAGE ASSEMBLY	1
22	11476	SCREW	2
23	51895	CLAMP, Guide Rod	2
24	54771	GUIDE ROD	2
25	11456	FASTEN TAB	1
26	51887	BASE	1
27	54770*	DRIVE MOTOR	1
28	54767	CARTRIDGE GUIDE	1

*** NOT FIELD REPLACEABLE**

☆ TABLE 12-1. 455/465 SPARE PARTS STOCKING GUIDE

PART NUMBER	DESCRIPTION	QUANTITY PER LEVEL		
		SITE	BRANCH	DEPOT
25284	PCB, 455	1	3	4
25286	PCB, 465	1	3	4
51781	LOCK CAM			2
51782	CLAMP HANDLE	1	4	4
51733	LOCK SPRING	1	2	2
51784	LIFTER SPRING	1	2	2
51785	LIFTER SHAFT		2	2
51896	GUIDE SHAFT ASSEMBLY			2
51899	CLAMP BEARING			2
52446	FACEPLATE		2	3
54755	FACEPLATE (FULL HEIGHT)		2	3
54758	WRITE PROTECT/INDEX DETECTOR ASSEMBLY	1	3	3
54762	TRACK 00 ASSEMBLY	1	3	3
54765	COLLET ASSEMBLY		2	2
54768	SHIELD PLATE		1	2
54771	GUIDE ROD			2

39239-20A

SECTION XIII
SCHEMATIC DIAGRAMS

The following schematic diagrams are furnished as an aid to malfunction analysis of PCB's 25284 (455) and 25287 (465).

IC TYPE	REF. DES.	QUAT.
7438	1A	1
7406	7B (4/6)	1
74LS14	3B	1
74S38	8B	1
74LS33	4B	1
7445	11B	1
74LS74	6B,9B	2
75452	3A	1
75453	4A	1
75477	5A,6A	2
74LS240	2B	1
53286	5B (2/4)	1
HA16631P	11A	1
CFD8201C		1
M002WT	12A	1
OR M001WT	12A	1

MODE SELECTION	
MD1	SHORT
MD2	OPEN
MD3	SHORT
MD4	OPEN
MDHLD	SHORT

REFERENCE DESIGNATION	
LAST USED	NOT USED
R57	R41,R42,R23,R24,R27
C28	
CR6	CR3.CR4
Q5	Q1,Q2
L6	
TP15	3,4,11,14

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REV. A

☆ **FIGURE 13-1.** SCHEMATIC DIAGRAM (455 PCB)

39409-03

IC TYPE	REF. DES.	QUAT.
7438	1A	1
7406	7B (4/6)	1
74LS14	3B	1
74LS38	8B	1
74LS33	4B	1
7445	11B	1
74LS74	6B,9B	2
75452	3A	1
75453	4A	1
75477	5A,6A	2
74LS240	2B	1
53286	5B (2/4)	1
HA16631P	11A	1
CFD8201C		1
M00IPC	10A	1
M002WT	12A	1

MODE SELECTION	
MD1	OPEN
MD2	OPEN
MD3	SHORT
MD4	OPEN
MDHLD	SHORT

REFERENCE DESIGNATION	
LAST USED	NOT USED
R57	R41,R42,R23,R24,R27
C32	C18,C19.C21
CR6	CR3.CR4
Q5	Q1.Q2
L8	
TP15	3,4,11,14

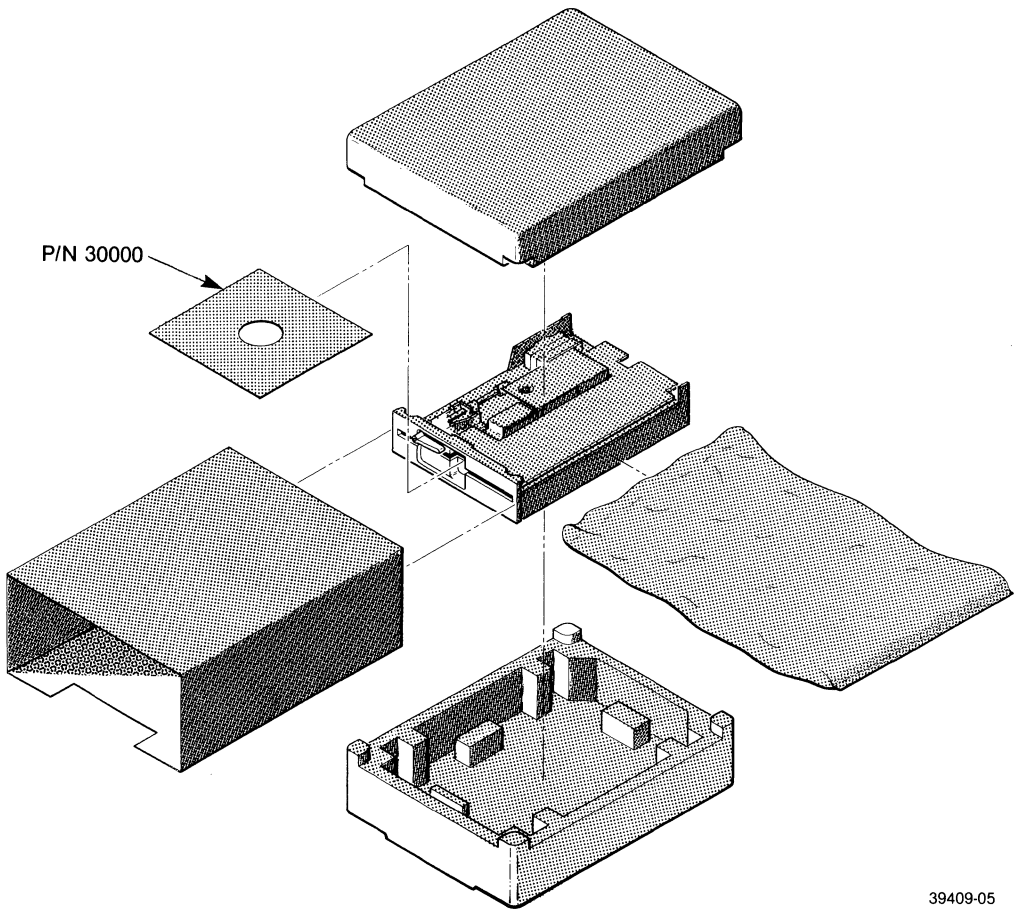
FIGURE 13-2. SCHEMATIC DIAGRAM (465 PCB)

39409-04

SECTION XIV
PACKAGING

14.1 PACKING FOR RESHIPMENT

It is suggested that packing material be kept, in case the unit must be returned to Shugart for repair. Regardless, the unit must be individually packaged in comparable packing as shipped to prevent damage in shipping and handling. *Damage to the unit as a result of inadequate packaging will void the warranty on the unit.*



☆ **FIGURE 14-1.** PACKAGING CONFIGURATION

To prepare a drive for shipment:

a. Locate the head carriage at Track 00.

b. Insert the carriage stop in the same manner as a diskette. Ensure that the tab is under the head carriage.

c. Place the drive in its packing container (see figure 14-1).

Failure to follow this procedure may result in damage to the drive.

APPENDIX A
ORDERING INFORMATION

The tables A-1 and A-2 shown below can be used to construct a part number for a unique drive configuration. These tables are interim and not complete. Further information will be furnished later.

TABLE A-1. SHUGART 455 PSI

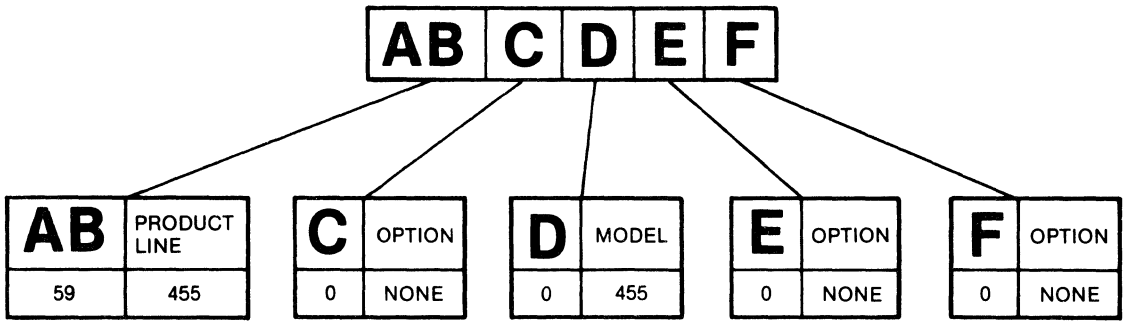


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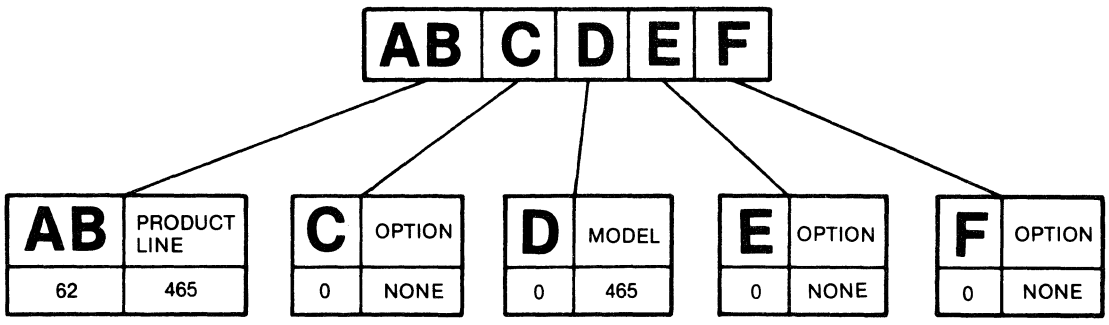
TABLE A-2. SHUGART 465 PSI



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