SBC-100/SBC-100S

Product Description Manual

Version 1.1

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Appendix A SIO Programming Manual

Appendix B PIO Programming Manual

Appendix C CTC Programming Manual

I. Description

The Sierra Data Sciences SBC-100 is the first "true" single board computer designed to operate on the S-100 Buss. It does not, however, require a buss structure to operate in other environments.

The term "single board computer" usually infers that all of the resources necessary to operate a computer exist on a single PC board. In the past, PC boards of this type have been introduced, however they did not contain an adequate amount of resources to perform significant tasks without the need to rely on other supporting PC boards.

The SBC-100 is a "complete" computer on a board, i.e. all of the resources necessary to run CP/M (or other Z80/8080 based operating system) exist on this single card. The features of the SBC-100 are as follows:

Z80A (Z80B optional) Processor.

Zilog Dart (SIO optional) Serial I/O chip. This part provides two (2) RS-232 ports.

ZPIO Parallel I/O chip. Two full parallel ports are provided with this chip.

NEC 765 Floppy disk controller chip. This LSI Floppy Disk Controller contains the circuitry and control funtions for the support of up to four (4) full size (8") or mini (5 1/4") drives.

64K Dynamic Random Access Memory. 64K of RAM is provided with the board. The SBC-100 is designed to permit the on-board RAM to execute with **no** wait states.

One 2732 EPROM is supported by the board. The 2732 EPROM provides up to 4K of user PROM space. The prom address space may be "phantomed" on or off by a simple output command to a special on-board global control port.

Intelligent Winchester Interface. (Optional) An interface is available for a number of intelligent 8" and 5 1/4" winchester drives. A special "Intelligent" drive cable is provided to interface certain winchester drives to the parallel ports on the SBC-100. Driver and formatter software is also provided with the purchase of this option.

Adherence to the IEEE-696 proposed standards. The SBC-100 was designed to meet the proposed IEEE-696 standard.

The SBC-100 was designed to meet the needs of single-user systems as well as multi-user systems in a number of configurations (i.e. Time sliced single processor operation, loosely-coupled multi-processor operation, etc.). This flexibility provides SBC-100 users with a natural growth path without the need to discard previous system components in most cases. In turn, users with larger requirements may build sophisticated multi-user systems right from the start.

To assist in the implementation of multi-processor implementations, Sierra Data Sciences has designed the SBC-100S Satellite (or "Slave") Processor PC Board. The SBC-100S is a separate implementation that can operate in tandom with the SBC-100 or other S100-based host processor PCB. Only four I/O mapped ports on the S100 buss are recognized by the SBC-100S processor board, hence, any number of separately addressed SBC-100S processors can simultaneously be operating on a single motherboard. This design flexibility makes it possible to build multi-processor based systems utilizing other host processors, such as the 8086, Z8000, M68000, etc.

The SBC-100S has an additional buss available for extended processing (The X-Buss). Located at the top of the card, this xx pin buss provides all the pin-out signals of the Z80 processor chip in addition to a number of selected support signals. The X-Buss provides a natural interface for computer controlled peripheral processors. Sierra Data Sciences has plans to introduce additional products for use on the X-Buss. The features of the SBC-100S are as follows:

Z80A (Z80B optional) Processor.

Zilog Dart (SIO optional) Serial I/O chip. This part provides two (2) RS-232 ports.

Two (2) ZPIO Parallel I/O chips. Four full parallel ports are provided with this chip. Two ports are available through a connector located at the top of the board. The remaining two ports operate on the S100 Buss as a high-speed data channel, and are used for I/O transfer operations during multi-processor communications.

64K Dynamic Random Access Memory. 64K of RAM is provided with the board. The SBC-100S is designed to permit the on-board RAM to execute with no wait states.

Four (4) 2732 EPROMs are supported by the board. The EPROMs provide up to 16K of user PROM space. The PROM address space may be "phantomed" on or off by a simple output command to a special on-board global control port.

EPROM Programmer (Optional). This option allows the user to program his or her own 2732 EPROMs. EPROM programming software is provided with the purchase of this option.

Software Controlled Reset Inhibit. This feature permits any hardware reset (i.e. front-panel reset key) to be ignored or recognized via a software controlled global control port.

Intelligent Winchester Interface. (Optional) An interface is available for a number of intelligent 8" and 5 1/4" winchester drives. A special "Intelligent" drive cable is provided to interface certain winchester drives to the parallel ports on the SBC-100S. Driver and formatter software is also provided with the purchase of this option.

Adherence to the IEEE-696 proposed standards. The SBC-100 was designed to meet the proposed IEEE-696 standard for the lines that it accesses.

Software for the SBC-100 can be purchased from Sierra Data Sciences to run in combination with the Digital Research CP/M operating system. The CP/M drivers are quite comprehensive, and are designed to take full advantage of the SBC-100's versatile features. (See Section III CP/M 2.2 Implementation).

MP/M and CP/Net can be configured on the SBC-100 and SBC-100S processors.

In addition, the powerful TurboDOS multi-user operating system can be configured to operate with the SBC-100 either as a single user system, a time-sliced multi-user system, or as a full implementation using dedicated satellite processors such as the Sierra Data Sciences SBC-100S Satellite processor.

For those users with special requirements, the SBC-100 and SBC-100S are ideal candidates for the nucleus of a powerful computer system for business, scientific, educational, or just about any computing requirements.

II. Interfacing - Master

A. SBC-100 Internal Port Assignments

This section describes the port assignments and function of the SBC-100 Master. The SBS-100 occupies thirty-two I/O mapped ports addressed at 80H through 9FH. The following table contains a description of ports.

Port Address	Port Identification
Serial Channels	
80H	Channel A Data Input and Output
81H	Channel A Status and Commands
82H	Channel B Data Input and Output
83H	Channel B Status and Commands
Parallel Channels	
84H	Channel A Data
85H	Channel A Command
86H	Channel B Data
87H	Channel B Command
CTC Channels	
88H	Channel 0 Used for baud rate generator for serial channel A
89H	Channel 1 Used for baud rate generator for serial channel B
8AH	Channel 2 Output is connected to CTC Channel 3 input
8BH	Channel 3 Used for RTC

II. Interfacing (continued)- Master

Floppy Disk Controller

8CH	Status and Commands
8DH	Input and Output Data
8EH	DMA Acknowledge Port
8FH	Same as 8EH
90H	Forced Terminal Count
91H	Same as 90H
92H	Forced Wait During Data Transfer
93H	Same as 92H
94H	Auxiliary Control Port
95H	Same as 94H
96H - 9FH	Reserved for Future Use

CTC Baud Table:

13D - 9600
26D - 4800
52D - 2400 etc.

II. Interfacing - Master

B. Auxiliary Control Port Definition

The Auxiliary Control Port on the SBC-100 Master is used for memory mapping,interrupt daisy chain control, and S-100 Buss DMA control. On reset or power up all eight bits of this port are set to 0.

Bits 0 through 4 control the memory mapping on the SBC-100. After reset, memory between 0 and C000H is accessed from the on-board ram. The other 16K between C000H and FFFFH is taken up by the 4K 2732 Prom which is mapped at all four 4K boundaries. Writing a 1 to bit 4 will turn the prom area off and at that time all of memory is accessed from on-board ram.

Bits 3 through 0 turn off 16K blocks of memory, Bit 3 being the top 16K and bit 0 the low bank of memory. Turning one of these bits on will enable the SBC-100 to access other memory on the S-100 buss.

For example if a 13H was written to the Auxiliary Control Port, the prom would be turned off as well as memory between 0 and 8000H. At this time the user would have access to S-100 buss memory. In order to use this memory banking scheme, bank switchable memory must be used in the system.

Bit 5 of the Auxiliary Control Port is used to disable interrupts from the SIO, PIO, and CTC simultaneously, and could be used during disk I/O transfers or any other operation that requires that the SIO and CTC chips do not gen interrupts. Note that the interrupts from the FDC cannot be disabled by this bit. Writing a one to this bit disables the interrupt daisy chain.

Bits 6 and 7 are used for DMA operations with the SBC-100. If bit 6 is turned on, a DMA request will cause a non-maskable interrupt on the SBC-100. The interrupt routine should then turn on bit 7 which is the DMA Acknowledge signal (pin 26 on the S-100 buss). At this time any S-100 accesses must be prohibited. The DMA device must access bank switchable memory as is the case with memory mapping. After the DMA device is finished, it will lower the DMA request. At this time another non-maskable interrupt will be presented to the SBC-100. The interrupt routine can then lower DMA ACK by turning off bit 7, and through the memory switching capability of the board, access the memory that was serviced by the DMA device.

II. Interfacing - Slave

C. S-100 Buss to SBC-100S Interface

This section describes how the SBC-100S interfaces with the 696 (S-100) Buss. The SBC-100S internal port assignments and description can be found in this section under "D. SBC-100S Internal".

The SBC-100S occupies a total of four I/O mapped ports on the S100 buss. Address bits A7 through A3 are decoded and used to set the board base address. A jumper inserted in shorting block #4 (SB4) represents a binary one setting for that bit, and conversely, a removed jumper represents a binary zero setting for that bit. For example, if the area is configured with address bit jumpers A7 and A6 inserted, then the base address would be C0H and the SBC-100S would occupy ports C0H, C1H, C2H, and C3H.

The SBC-100S can be used in two modes of operation, both of which are determined by the jumpers in SB3. In the following example, the six bit base address will be represented as XXXXXX.

In both modes of operation, output to any of the four ports in the block will write data from the S100 buss to the SBC-100S.

OUTPUT In Mode 1 and 2

XXXXXX00 Port used to transfer data and commands from the S100 to the SBC-100S

XXXXXX01 SAME function

XXXXXX10 SAME function

XXXXXX11 SAME function

INPUT From SBC-100S In Mode 1: Interrupt Vector Mode

XXXXXX00 Input data and commands from the SBC-100S to the S100 buss

XXXXXX10 Same as XXXXXX00

XXXXXX01 Disabled in this mode of operation. The SBC-100S will not respond to an input from this port

XXXXXX11 Same as XXXXXX01

In this mode of operation, an interrupt vector (which can be modified by the SBC-100S) is placed onto the data buss for interrupt processing. This vector can be used as an indirect displacement into an interrupt processing routine. When using more than one SBC-100S in the same motherboard, the daisy chain jumpers must be inserted such that only one board places its vector onto the buss during INTA. The daisy chain area is adjacent to S-100 pins 4 through 11. Also see sheet 3 of slave schematic.

The value of the vector that is placed onto the buss is determined by SB5 and the six bits that the SBC-100S can modify under sottware control. This is illustrated as follows:

INTERRUPT ACKNOWLEDGE VECTOR

BITS 7 through 3: Programmed by SBC-100S

BIT 2: (Shorting Block #5)

If a jumper is inserted, this bit gives the status of the BRDY bit. If on, data is ready to be transferred from the SBC-100S to the S100 buss. If off, data from the SBC-100S is not ready to be sent to the S100 buss.

This jumper is prewired on the SBC-100S PC card.

BIT 1: (Shorting Block #5)

If a jumper is inserted here, bit 1 gives the status of the ARDY line. If on, data can be written to the SBC-100S from the S100 buss. If off, data cannot be written to the SBC-100S from the S-100 buss.

This jumper is prewired on the SBC-100S PC card.

INPUT FROM SBC-100S IN MODE 2: Status Port Mode

In this mode of operation, the SBC-100S will not respond to interrupt acknowledge. The INTA byte described above can be accessed by reading a status port. It should be noted that though the SBC-100S will not place a vector onto the buss during INTA, it can still be programmed to generate an interrupt whenever it has data or commands to send or receive from the S100 buss. The status port can then be interrogated to determine the cause of the interrupt.

The input ports in this mode of operation are:

XXXXXX00	Data and command input
XXXXXX10	Same as XXXXXX00
XXXXXX01	Input from this port presents SBC-100S status to the S100 buss
XXXXXX11	Same as port XXXXXX01

II. Interfacing - Slave

D. SBC-100S Internal Port Assignments

This section describes the internal port assignments and functions of the SBC-100S.

PORT ADDRESS	PORT IDENTIFICATION
80H	Serial Channel A data input and output
81H	Serial Channel A status and commands
82H	Serial Channel B data input and output
83H	Serial Channel B status and commands
84H	Parallel Channel A data (External Access)
85H	Parallel Channel A command (External Access)
86H	Parallel Channel B data (External Access)
87H	Parallel Channel B command (External Access)
88H	CTC Channel 0 - baud rate generator for serial channel A
89H	CTC Channel 1 - baud rate generator for serial channel B
8AH	CTC Channel 2 - output connected to CTC 3 input
8BH	CTC Channel 3 - available for RTC
9CH	Parallel Channel C input data (S-100 to Slave Data Port)
9DH	Parallel Channel C command (Program for Input)
9EH	Parallel Channel D output data (Slave to S-100 Data Port)
9FH	Parallel Channel D command (Program for Output)

II. Interfacing

B. Internal (CONTINUED)

PORT ADDRESS	PORT IDENTIFICATION
90H	Auxiliary Control Port A (Output Only)
91H	Same as Port 90
92H	Auxiliary Control Port B (Output Only)
93H	Same as Port 92

The remaining ports on the SBC-100S are not used, although several ports are reserved for planned X-buss expansion boards. Expansion boards are attached via two overhead connection cables located at the top of the SBC-100S. (Consult factory if expansion boards other than those manufacterd by Sierra Data Sciences are to be used).

Details on programming the Zilog SIO, PIO, and CTC support chips can be found as Appendices to this manual.

1. Programming The Auxiliary Control Ports

Auxiliary Control Port A

External or Internal reset will initialize all bits to zero.

Bit7: Interrupt On Input Available (Slave to Master Data Transfer)

When this bit is enabled, an interrupt will be generated whenever the S-100 PIO has a character ready to be read by the host processor.

When this bit is disabled, interrupts from the S-100 PIO are disabled.

Bit 6: Interrupt On Input Receiver Ready (Master to Slave Data Transfer)

When this bit is enabled, the SBC-100S will generate an interrupt whenever it is ready to receive a character from a host S100 buss processor. When this bit is disabled, interrupts on input receiver ready are disabled.

Bits 5 through 0 Interrupt Vector Control Address

These bits control the interrupt vector that is placed on the S100 buss during INTA (When the SBC-100S is configured in Z80 interrupt mode 2). The following table defines the bit mapping for the INTA byte value.

AUXILIARY PORT BIT	CORRESPONDING INTA BYTE BIT
Bit 4	Bit 7
Bit 3	Bit 6
Bit 2	Bit 5
Bit 1	Bit 4
Bit 0	Bit 3
Bit 5	Bit 0

When the SBC-100S is configured in Mode 2, the above bit assignments correspond to the value that will be read from the S100 buss whenever an input from the SBC-100S status port is performed.

2. **Auxiliary Output Port B**

External or internal reset initializes all bits to zero.

Bits 7 and 6: 16K Memory Disable

These two bits determine which 16K bank is disabled on the SBC-100S when EPROM on the board is enabled.

BIT 7	BIT 6	Disabled Bank Address
0	0	C000H - FFFFH
0	1	8000H - C000H
1	0	4000H - 8000H
1	1	0000H - 4000H

Bit 0: Bank Switch Enable

When this bit is zero, the bank switching feature of the SBC-100S is enabled. When this bit is a one, the bank switching feature is disabled.

Bit 1: EPROM/RAM Enable

When this bit is zero, the on-board EPROM is enabled and occupies memory as defined by bits 6 and 7 of any port B. When this bit is a one, the on-board EPROM is disabled and RAM locations C000H through FFFFH are enabled.

The following table illustrates the means by which bits 7, 6, 1, and 0 are used to control different 16K banks of on-board memory.

				Memory Map			
BIT 7	**BIT 6**	**BIT 1**	**BIT 0**	**0**	**16**	**32**	**48K Bank**
0	0	0	0	R	R	R	P
0	0	0	1	R	R	R	E
0	0	1	0	R	R	R	R
0	0	1	1	R	R	R	R
0	1	0	0	R	R	E	P
0	1	0	1	R	R	E	R
0	1	1	0	R	R	R	R
0	1	1	1	R	R	R	R
1	0	0	0	R	E	R	P
1	0	0	1	R	E	R	R
1	0	1	0	R	R	R	R
1	0	1	1	R	R	R	R
1	1	0	0	E	R	R	P
1	1	0	1	E	R	R	R
1	1	1	0	R	R	R	R
1	1	1	1	R	R	R	R

R=ON-BOARD RAM P=ON-BOARD EPROM E=EXTENDED MEMORY

NOTE: The extended memory refers to banks of memory accessable through the overhead X-Buss connector.

Bits 5 and 4: Block Move Enable

If bit 5 is set to one, the wait line is enabled when the host (or "master") processor attempts to read data from the SBC-100S.

If Bit 4 is set to one, the wait line is enabled when the host processor attempts to write data to the SBC-100S.

Bit 0: Bank Switch Enable

When this bit is zero, the bank switching feature of the SBC-100S is enabled. When this bit is a one, the bank switching feature is disabled.

Bit 1: EPROM/RAM Enable

When this bit is zero, the on-board EPROM is enabled and occupies memory as defined by bits 6 and 7 of any port B. When this bit is a one, the on-board EPROM is disabled and RAM locations C000H through FFFFH are enabled.

The following table illustrates the means by which bits 7, 6, 1, and 0 are used to control different 16K banks of on-board memory.

				Memory Map			
BIT 7	**BIT 6**	**BIT 1**	**BIT 0**	**0**	**16**	**32**	**48K Bank**
0	0	0	0	R	R	R	P
0	0	0	1	R	R	R	E
0	0	1	0	R	R	R	R
0	0	1	1	R	R	R	R
0	1	0	0	R	R	E	P
0	1	0	1	R	R	E	R
0	1	1	0	R	R	R	R
0	1	1	1	R	R	R	R
1	0	0	0	R	E	R	P
1	0	0	1	R	E	R	R
1	0	1	0	R	R	R	R
1	0	1	1	R	R	R	R
1	1	0	0	E	R	R	P
1	1	0	1	E	R	R	R
1	1	1	0	R	R	R	R
1	1	1	1	R	R	R	R

R=ON-BOARD RAM P=ON-BOARD EPROM E=EXTENDED MEMORY

NOTE: The extended memory refers to banks of memory accessable through the overhead X-Buss connector.

Bits 5 and 4: Block Move Enable

If bit 5 is set to one, the wait line is enabled when the host (or "master") processor attempts to read data from the SBC-100S.

If Bit 4 is set to one, the wait line is enabled when the host processor attempts to write data to the SBC-100S.

Bits 4 and 5 are used to synchronize block move transfers on the S100 buss (to and from the SBC-100S). Note that, before these bits are enabled, the S100 PIO must be in the ready state. This prevents unsolicited wait states from being placed on the buss.

Bit 2: EPROM Power Enable

When this bit is enabled, the EPROM programmer will be activated for EPROM 4 (position U13). To successfully program an EPROM, the user must repeatedly write to it 2000 times.

Each memory write requires 25 micro-seconds (4MZ version). For example, burning an EPROM area of 1K will take 1024 * 25 usec * 2000, or 51 seconds. During the time that this bit is on, reading from the EPROM being programmed is inhibited. Hence, to verify the program just burned, this bit must first be reset.

Bit 3: Reset Disable

When this bit is enabled, the S100 buss reset line will be ignored by the SBC-100S. If this bit is disabled, after being enabled, an on-board CPU reset will be invoked immediately.

This is an on-board only hardware reset.

E. Reset/Start Sequence - The following pertains to both master and slave:

When the processor is reset, the on-board PROM is enabled at addresses 0C000 to 0FFFF and the CPU is forced to execute the first 3 bytes of the PROM installed at 0C000. This should be a JMP to the start of the code in the PROM. If the code in the PROM immediately follows the initial JMP, then this would be JMP 0C003H. Following this JMP, memory from 0000 to 0BFFF is RAM.

III. CP/M 2.2 Implementation

A. General

The Sierra Data Sciences CP/M 2.2 interface is one of the most comprehensive implementations available.

It was designed specifically to fully utilize the features available on the SBC-100. The major features of this software are listed below:

1. Interrupt Driven I/O

All peripheral devices under the control of the system executive are fully buffered and interrupt driven. Interrupts are not reentrant, and are serviced on a first-in first-out basis. Interrupts are disabled only while and interrupt is being processed, and in addition, when a sector is being read from or written to the NEC 765 floppy disk controller chip.

Additional entries are available in the interrupt vector table for the user to write customized interrupt driven routines if required.

2. Auto-Boot

During a cold system start, a diskette may be placed in any one of the floppy disk drives attached to the system.

The system executive will first determine if the diskette inserted has a system header recorded on it.

If it is determined that the diskette is not a system diskette, the read/write head will be unloaded, and the system executive will wait for another diskette to be inserted.

Please note that a system diskette cannot be created on a single density diskette. Hence, all system diskettes must be either single-sided/double-density, or double-sided/double-density.

When a system diskette has been inserted in an available floppy disk drive, the system configuration header is read and the SBC-100 is initialized based upon the parameters in the header. (See D. System Configuration Operating Procedure). The Sierra Data Sciences Copyright will then appear after the CRT screen is cleared.

If your system has the Sierra Data Sciences Intelligent Winchester Interface installed, and one of the available platters is configured as Drive A, then system start-up will proceed as follows:

a. The system executive will look for the first available ("ready") disk device on the system.

b. If the first device to become ready is the winchester disk ("drive A"), then a system initialization header will attempt to be read from the drive. If no header is found on the drive, then an attempt will be made to read a system header from the first "ready" floppy disk drive. If a system disk was not inserted in the floppy disk drive and additional floppy disk devices are available on the system, an attempt will be made to read a system header from the first available floppy disk device in the daisy-chain. If at the end of the daisy-chain a system diskette was not located, the system executive will start all over by looking for a system header on the winchester drive A. This sequence will continue until a system diskette has been inserted, or until a hard disk SYSGEN (See Hard Disk SYSGEN) has been performed on the winchester drive.

When a successfull system boot has been performed, the Sierra Data Sciences Copyright will appear as the CRT screen is cleared.

3. Password Protection

After a system cold-boot has been performed and the Sierra Data Sciences Copyright has appeared, an asterisk will appear in the bottom left-hand corner of the CRT display.

The asterisk indicates that a password must be entered to gain access to the system (See Config).

If nothing is entered from the keyboard within a short period of time, the audible alarm on the CRT will be sounded requesting you to enter your password and thereby log on to the system. The alarm will be sounded a maximum of two (2) times, and if still no action has been taken, the system will be halted, and a cold-boot operation will be necessary in order to continue.

If action is taken at the keyboard, i.e. a password is entered followed by depressing the carriage return key, the system executive will determine if the password you entered matches the one recorded on the diskette or hard disk drive.

If the password does not match, the audible alarm will be sounded indicating that an incorrect password has been entered.

This process will continue for an additional two (2) times, and if an incorrect password has still been entered, the system will enter a halt state. A cold boot operation will be necessary in order to continue.

If the password entered matches the one entered, the system will respond by logging on to the drive containing the system header. (i.e. if a diskette was placed in floppy drive B, the system would display B> and await a CP/M command.

4. Buffered I/O Devices

In addition to being interrupt driven, the System Executive also utilizes input and output buffering on all on-board peripherals.

As a character is typed at the CRT console, it is placed in an input buffer and processed by another task reading characters from the same buffer. Conversely, as a character is written to the CRT, it is placed in an output buffer and processed by another task reading and echoing characters from the buffer.

This feature is very useful when utilizing a word processing system that also spools output to a printer device. If the printer requires more time to print characters than those being entered at the keyboard, no data is lost since it is buffered with interrupt routines.

5. Cylinder Formatting

The system executive uses a cylinder technique for storing data on double sided diskettes.

Sectors in many CP/M systems are usually sequenced on the lower side of the diskette from track 0 through 76, and then on the upper side again, from track 0 through track 76. This technique is inefficient since the read/write head has to perform a seek operation 77 times for the lower side of the diskette, then a home operation, then 77 additional seeks for the upper side of the diskette.

The system executive treats double sided diskettes as a cylinder, i.e. track 0, head 0, track 0 head 1, etc. This technique cuts seek time in half, since twice as much data is available under the read/write heads at each track.

6. Time-of-day Clock

The system executive uses one of the counter-timer channels (Channel 3) on the SBC-100 as a real-time clock.

Both the Date (Month, Day, and Year), and Time of day (AM and PM) are constantly maintained after being set by the utility program (See TAD Utility Program).

7. Timer Event Interrupt

A user may cause an interrupt routine to be called by the system executive after every second has elapsed (See System Executive Internals).

This feature permits time dependent functions to be implemented easily within the powerful interrupt structure of the system executive.

An optional fast-timer (interrupt every 1/60th of a second) is available when your system is equipped with the Sierra Data Sciences ZSIO extension card.

8. Format Disk Utility Program

This utility program will format the following types of diskettes:

Single Sided / Single Density

Single Sided / Double Density

Double Sided / Single Density

Double Sided / Double Density

Diskettes are not only formatted, but the formatted tracks are also verified after formatting.

If the Intelligent Winchester Interface is installed on your system, the format program also supports the formatting of the hard disk, on a per platter basis.

9. Disk Copy Utility Program

The disk copy utility program supports the following types of copy operations:

Single Drive Full Diskette Copies (Full Track)

From / To Full Diskette Copies (Full Track)

System Tracks Only (Full Track)

Data Tracks Only (Full Track)

Diskettes are not only copied but verified as well, providing confident backup for system and data.

10. System Configuration Utility Program

Perhaps the most powerful utility program provided, the System Configuration Program, provides the user with a tool to tailor a system to his or her exact needs. Some of the functions provided are:

Change Baud Rate (Serial Channels)

Change Stop Bits (Asynchronous Serial Channels)

Select DTR on Protocol

Select ETX/ACK Protocol

Select X-on/X-off Protocol

Set step time on floppy disk drives

Assign logical devices to physical devices

Assign logical disk drives to physical disk drives

Assign passwords to a disk drive

See System Configuration Utility Program, Section X, for the operation of this program.

11. MOVCPM CP/M Utility Program

This program is provided and "works" when creating different size versions of a CP/M system. NOTE: It is only provided when a copy of CP/M 2.2 from Digital Research has been purchased by the user.

12. SYSGEN Utility Program

    A utility program to create new copies of a system diskette is provided with CP/M purchase.

13. Hard Disk SYSGEN

    A utility program that performs a system generation on a winchester hard disk is provided if the Intelligent Winchester Option has been installed on your system.

    Since this utility places a system boot record on the hard disk, the system may "booted" directly from it, eliminating the need to have a diskette mounted at all times.

B. System Executive Internals

1. Memory Allocation

The system executive resides at the top of memory and includes all memory from 0ED30H through 0FFFH.

Supplied in a 2732 EPROM, the system executive gets control on reset at location 0F000H. It then relocates itself into the proper memory location, "phantoms" out the EPROM, and jumps to its new relocated entry address.

Memory is allocated as follows:

PAGE ZERO:

The system executive utilizes several locations in page zero to interface itself to CP/M.

PAGE ZERO ADDRESS	Description Of Use By Executive
08H - 0AH	Interrupt Response Entry (RST 1)
10H - 12H	Main Executive Entry Point (RST 2)
40H	Time and date initialization flag. A value of 69H (105.) at this location indicates that the time and date are initialized. Any other value indicates that the time and date are not initialized, and hence, the time and date locations contain random information.
41H - 48H	Time and Date (If Initialized).

The System Time and date are mapped and available to the user in the following locations:

LOCATION	CONTENTS
41H	Seconds (0-59)
42H	Minutes (0-59)
43H	Hours (1-12)
44H	AM/PM (0=AM,0FH=PM)
45H	Weekday (0-06) 0=Sunday,1=Monday,etc.
46H	Day Of Month (1-31)

LOCATION	CONTENTS	
47H	Month	(1-12)
48H	Year	(1-99)

The above time and date values are all byte binary values, and are updated once each second by the system clock interrupt driver routine in the system executive.

The following locations are a copy of data maintained within the system executive and will be restored following a hardware reset provided that the original data has not been destroyed by power loss or application program errors.

PAGE ZERO ADDRESS	Description Of Use By Executive
49H	General Purpose Timer Byte. The value stored in this location is decremented once each second by the system clock interrupt driver.
4AH	Head Load Timer. This location is also decremented once each second. Each time this location reaches zero, the floppy disk heads are unloaded (8" Drives only). To unload the heads under program control, the user should store an 01H into this location.
4BH	Not Currently Used, (Reserved)
4CH - 4DH	Timer Event Control Block (TECB). On each timer interrupt, control is transferred to the routine whose address is stored in this location. Entry to the routine is made while in the system executive interrupt routine itself. Upon Entry, registers AF, BC, DE, and HL have been saved. In addition, a 20 level stack is available at the address of SP. Alternate Registers and Index registers have NOT been saved. Care should be taken to perform as little processing as possible while in this

PAGE ZERO ADDRESS	Description Of Use By Executive
4CH - 4DH (cont.)	routine, since interrupts are disabled until return is made to the system executive. Initially, this address points to a return instruction, and therefore, performs no further processing. To utilize this routine, store the address of your subset interrupt driver at location 4CH. Your routine must terminate with a "RET" instruction. If your routine makes use of the Index and/or alternate registers, it is your responsibility to save and restore them before returning to the system executive.
4EH - 4FH	Fast TECB. Similar to the TECB above, this timer interrupt subset routine is called by the system executive 60 times per second. NOTE: the Sierra Data Sciences CTC expansion via the ZSIO card must be installed to utilize this feature.

FREE AREA:

The area between the end of the BIOS and the start of the system executive is not used by the system and is available for user programming. This area is referred to as the BIOS Expansion area. For the largest CP/M supported on this system, the last location used by the BIOS is 0EC5DH. The space from 0EC5EH through 0ED2FH (0D2H / 210. bytes) is available for BIOS expansion. If more space is required, you may create more in 1K (1024. byte) increments by using MOVCPM to create smaller CP/M systems. In a "63K" system, the last byte used by the BIOS would be 0E85DH.

TRANSIENT PROGRAM AREA (TPA)

In the maximum size CP/M system ("64K"), the TPA extends from 100H through 0CBFFH if you do not wish to overwrite the CCP (Console Command

TRANSIENT PROGRAM AREA (TPA) - (continued...)

Processor). If the CCP is overwritten, the top of it extends to 0D3FFH. This leaves available space of 0CB00H (51,968. bytes) or 0D300H (54,016. bytes) for TPA use. For smaller sized CP/M systems, these values become smaller in 1K (1024. byte) increments.

2. System Executive Interfacing And Access

REGISTER USAGE

The System Executive, BIOS, and CP/M do not use the Index or Alternate registers available on the Z80 microprocessor; therefore, it is not necessary to save and/or restore these registers when making calls to these modules.

When making direct system executive calls, unless specified, entry and exit register values are unpredictable. For CP/M calls, check your CP/M manuals.

STACK REQUIREMENTS

System Executive functions utilize internal stacks, and except for the minimum external stack required for interrupt handling and making the initial System Executive call, no further stack is required.

User Stack	: n bytes
Interrupt Handling	: 4 bytes
System Executive or CP/M call	: 2 bytes
Total	: n + 6 bytes

DIRECT SYSTEM EXECUTIVE CALLS

A direct System Executive call consists of storing a function code in the accumulator, appropriate data in other specified registers, and finally transferring control to location 10H (RST 2).

There follows a list of each function and what data/actions are required /expected for each function. In some cases, additional interfacing information is provided.

Function 0 (00H) Cold Boot

Entry Parameters: None

Resultant Action: All system I/O hardware is re-initialized to parameters stored in a configuration table. The CP/M operating system is reloaded, and control is transferred to the BIOS entry point.

Exit Parameters: None. The system is rebooted.

==========

Function 1 (01H) Warm Boot

Entry Parameters: None

Resultant Action: CP/M operating system is reloaded and control is transferred to the BIOS boot entry point.

Exit Parameters: None. The system is rebooted.

NOTE: It is not recommended that user programs use functions 0 and 1, since they do not flush the disk write buffer back out to disk before reloading the operating system. It is recommended instead to use the more standard CP/M warm boot exit to location 0000H which does flush the disk write buffer before reloading the operating system.

==========

Functions 2 through 5 access the physical I/O ports of the system. The desired port is passed in the B register according to the following table. Note that serial and parallel ports C and D are available only if the I/O expansion ZSIO board is installed.

B Register Value	Port Accessed
0	Serial Port A (System Console)
1	Serial Port B
2	Serial Port C
3	Serial Port D
4	Parallel Port A
5	Parallel Port C
6	Parallel Port D

Parallel port B is reserved for internal

Function 2 (02H) Get Input Port Status

Entry Parameters: B = Port Number

Resultant Action: The input buffer corresponding to the port is tested for the availability of input characters. If a character is available, a non-zero value is returned in the Accumulator and the Z flag is cleared. If a character is not available, a zero is stored in the accumulator, and the Z-flag is set.

Exit Parameters: A and Z-Flag.

==========

Function 3 (03H) Get Output Port Status

Entry Parameters: B = Port Number

Resultant Action: The output port is tested to determine if it can accept characters. If a character can be accepted, a non-zero value is returned in the accumulator, and the Z-flag is cleared. In addition, the number of characters presently in the output buffer is stored in the C register. If a character cannot be accepted, a zero is stored in the accumulator, and the Z-flag is set. The C Register has no meaning.

Exit Parameters: A and Z-Flag
C = Number of bytes in output buffer if accumulator <> 0

==========

Function 4 (04H) Input Character From Port

Entry Parameters: B = Port Number

Resultant Action: A character is extracted from the appropriate input buffer and returned in the accumulator. In this case, the Z-Flag will be cleared. If no character is available, the Z-Flag will be set.

Exit Parameters: A and Z-Flag

==========

Function 5 (05H) Output Character To Port

Entry Parameters: B = Port Number
C = character

The character in the C register is placed in the appropriate buffer for transmission to the port specified in the C register. If the output buffer is full, this function will wait until space is available to load the character into the buffer.

Exit Parameters: None

==========

Functions 6 and 7 are the System Executive disk I/O calls. Drive selects are made by selecting the physical drive, NOT the logical drive. Sectors are PHYSICAL sectors NOT CP/M record numbers. Physical sectors are written on floppy diskettes in sequential order. Skewing translation is performed within the System Executive. When transferring data, the minimum size for transfer is one PHYSICAL sector, NOT a 128 byte CP/M record. Sector sizes are as follows:

Single Density Floppy Disk	: 128 Bytes
Double Density Floppy Disk	: 256 Bytes
Hard Disk	: 512 Bytes

NOTE: Track zero (0) on all floppy disk formats is single density.

The BIOS contains deblocking algorithms to manage the larger sector sizes as groups of 128 byte records. The System Executive does not perform any deblocking.

Since a logical drive (A:, B:, ..n:, etc.) can be mapped to any physical drive, it may be necessary to access the nine (9) byte logical to physical drive map resident in the BIOS to obtain the physical drive designation corresponding to the desired logical drive selection.

In addition, if the system has been configured correctly, the list will also show which logical and physical drives are available. The list is arranged so that the first byte gives the physical assignment for logical drive A:, the second for drive B:, and so on through drive I:. A value of 0FFH indicates that the corresponding logical drive has not been assigned. For floppy disk drives, the values are zero (0) through three (3),

For hard disks, the high-order (MSB) bit is set. In addition, bits zero (0), and one (1) assume values zero (0) through three (3) indicating the unit. Moreover, bits four (4) through six (6) assume values zero (0) through four (4) indicating the head (or platter) within the unit and bits two (2) and three (3) are always zero (0). For Example:

10000000 (80H) Indicates:

Hard disk drive
Unit zero (0)
Head zero (0)

In turn,

10110010 (B2H) Indicates:

Hard disk drive
Unit two (2)
Head three (3)

A routine resident in the BIOS returns the physical drive number in the accumulator corresponding to the logical drive number in the CP/M current drive byte (location 0004H). Upon return from that routine, the HL register pair points to the address from which the physical assignment was taken. To find the base of the list, store a 00H (corresponding to Drive A:) in the current drive location (0004H) and call the BIOS routine. Upon return, the HL register pair will contain the address of the start of the list.

The current drive value should be saved at the start of this process and restored at the end. The address of the BIOS routine is equal to the address of the warm boot jump located at 0001H + 0033H. An Example Follows:

```
.           .
.           .
LD          A,(0004H) ; SAVE PRESENT CURRENT DRIVE
PUSH        AF        ; *
XOR         A         ; *
LD          (004H),A  ; TEMPORARILY SET TO 0 (A:)
LD          HL,0001H  ; WARM BOOT ADDRESS
LD          DE,0033H  ; OFFSET
ADD         HL,DE     ; ADD OFFSET
CALL        BIOJMP    ; CALL BIOS ROUTINE
POP         AF        ; RESTORE CURRENT DRIVE
LD          A,(0004H) ; *
LD          HL,DRVMAP ; SAVE BASE ADDRESS OF DRIVE MAP
.           .
```

```
          .         .
EXAMPLE (continued....)

          .         .
          .         .
BIOJMP:   JP   (HL)
          .         .
          .         .
          .         .
DRVMAP:   DS   2              ; BASE ADDRESS STORAGE
          .         .
          .         .
          .         .
```

==========

Function 6 (06H) Select Physical Drive

Entry Parameters: C = Physical Drive Number

Resultant Action: The requested drive is selected for subsequent System Executive disk operations. This function must be successfully executed before any disk operations are requested. This insures that the disk operations that follow are performed on the correct drive. If the operation was successful, the Z-Flag will be set upon return from the routine. If unsuccessful, the Z-Flag will be cleared.

Exit Parameters: Z-Flag

==========

Function 7 (07H) Disk I/O (Read/Write)

Entry Parameters: B = Bits 0-3 => Track MSB
Bit 4 => 0=Read,1=Write
Bit 5 => (Floppy Only)
0=Compute Sector Skew
1=Disable Sector Skew
Bit 6 => (Floppy Only)
0=No Recalibrate
1=Perform Recalibrate
before read/write
Bit 7 => Not used

C = Track LSB
D = Number of sectors to R/W
(Floppy Only AND sector skew disabled)
E = Sector Number To Start
(0 to n-1, where n=the number of
physical sectors per track)
HL= Address from which data transfer
is to begin.

Function 7 (continued.....)

Resultant Action: A seek to the specified track is performed, and data is read to or written from sequential memory locations starting at the address passed in the HL register pair. If the operation was successful, upon return, the Z-Flag will be set and the HL register pair will contain the next address that would be read or written should the sequential operation be continued. If the operation was unsuccessful, the Z-Flag will be cleared and the accumulator will contain an error code. If an error has occurred, then the HL register pair has no meaning.

Error Codes Are As Follows:

CODE	ERROR DESCRIPTION
0	Home error. (Recalibration Failure)
1	Seek Error
2	Read Error
3	Write Error

Exit Parameters: Accumulator and Z-Flag
HL (If Successful)

==========

Function 8 (08H) Print String To Console

Entry Parameters: HL=Address Of String Start

Resultant Action: The ASCII string pointed to by the HL register pair is outputted to the system console byte-by-byte, until a byte with bit 7 set is encountered. The byte with bit 7 set is also output to the system console. Upon return, the HL register pair points to the last byte written to the console.

Exit Parameters: HL

==========

Function 9 (09H) Set Cursor Position

Entry Parameters: H (1-80) = X or column
L (1-24) = Y or row

If terminal control functions have been initialized with the system configuration utility program, the values in H, and L will be converted to the proper sequence to position the cursor on the CRT console. Upon return, the Z-Flag will be cleared. If terminal controls have not been initialized, the Z-Flag will be set upon return.

Exit Parameters: Z-Flag

==========

Function 10 (0AH) Clear Screen And Home Cursor

Entry Parameters: None

If terminal control functions have been initialized with the system configuration utility program, the sequence to clear and home the cursor will be generated and sent to the CRT console. Upon return, the Z-Flag will be cleared. If terminal controls have not been implemented, this function will return with the Z-Flag set.

Exit Parameters: Z-Flag

==========

Function 11 (0BH) Set Baud Rate

Entry Parameters: C = Serial Port (0-3)
E = Baud Rate (0-7)

The port designations correspond to those already defined for functions 2 through 5.

Baud Rate Values Are Defined as Follows:

Register E Value	Baud Rate
0	9600
1	4800
2	2400
3	1200
4	600
5	300
6	150
7	110

Function 11 (continued....)

When called with valid parameters, the baud rate will be set for the port designated by the value in register C. An invalid port designation will result by the routine returning with no action taken. An invalid baud rate will result in a default to 9600 baud.

Exit Parameters: None

==========

Function 12 (0CH) 16 BIT X 16 BIT Multiply (Binary Integer)

Entry Parameters: HL = Multiplicand
DE = Multiplier

Exit Parameters: HLDE=Product (H=MSB)

==========

Function 13 (0DH) 16 BIT X 16 BIT Divide (Binary Integer)

Entry Parameters: HL = Dividend
DE = Divisor

Exit Parameters: DE = Quotient
HL = Remainder

Division by zero (0) will result in a remainder equal to the dividend, and a quotient of -1 (0FFFFH).

==========

Functions 14, 15, and 16 are reserved for system use.

==========

Function 17 (11H) Get Base Address Of Time & Date

Entry Parameters: None

Resultant Action: The address of a nine (9) byte time and date data area is returned in the HL register pair. This data area is identical in format to the time and date data at locations 40H-48H.

Exit Parameters: HL

==========

Function 18 (12H) Get Base Address Of 15 Byte Disk Parameter Block

Entry Parameters: B = Physical Drive Designation

Resultant Action: The address of the 15 byte disk parameter block corresponding to the physical drive in the B register is returned in the HL register pair. The data in that area will be valid for floppy disk drives only if it has been initialized by the monitor after reading the disk header from a diskette inserted in that drive.

Exit Parameters: Accumulator = Physical Drive Designation
HL=Address of disk parameter block corresponding to the drive.

==========

Function 19 (13H) Get Floppy Drive Ready List Pointer

Entry Parameters: None

Resultant Action: The address of the first byte of a three byte floppy disk drive status area is returned in the HL resigter pair. In each byte, four (4) possible physical floppy drives (0-3) are represented by the corresponding bits 0-3.

Byte Zero (0) Ready List. A 1 in bit positions 0-3 indicates that the corresponding physical floppy disk drive has a diskette inserted and the diskette is operational in the drive.

Byte One (1) Initialized List. A 1 in bit positions 0-3 indicates that the corresponding disk parameter header has been read and the appropriate data used for disk access has been installed in memory.

Byte Two (2) System List. A 1 in bit positions 0-3 indicates that the diskette in the corresponding physical drive is a "system" diskette. i.e. the diskette may be used to boot the system.

Exit Parameters: HL

Function 19 (continued....)

The user should take care not to store data in these memory locations. They are set and reset by internal System Executive routines whenever diskettes are inserted and removed and any time Function 6 (Select Physical Drive) is executed.

==========

Function 20 (14H) Get Floppy Disk Sense Data Address

Entry Parameters: None

Resultant Action: Each floppy disk operation produces result data showing the status of the operation upon completion. This function returns the HL register pair, the address of a seven byte area in which these results are stored. For information on the meaning of the data stored in this area, consult the NEC UPD765 floppy disk controller manual.

Exit Parameters: HL = Base Address Of Sense Data

==========

Function 21 (15H) Get Hard Disk Sense Data

Entry Parameters: None

Resultant Action: Each hard disk operation produces an eight byte completion code that indicates drive status at the completion of the I/O operation. Consult the appropriate Hard Disk Manual to properly interpret the meaning of this data. This function loads the HL register pair with the address of this eight byte area.

Exit Parameters: Hl = Address Of Hard Disk Sense Data

==========

Function 22 (16H) Get Base Of Month Length Table

Entry Parameters: None

Exit Parameters: HL contains the address of a 12 byte table of month lengths.

==========

System Executive Function Call Summary

Function Code	Function Description
0	Cold Boot
1	Warm Boot
2	Get Input Status Of Port
3	Get Output Status Of Port
4	Input Character From Port
5	Output Character From Port
6	Select Physical Drive
7	Disk Read/Write
8	Print String To Console CRT
9	Position Cursor
10	Clear and Home the Cursor
11	Set Baud Rate
12	Multiply HL By DE
13	Divide HL By DE
14	Reserved
15	Reserved
16	Reserved
17	Return HL=Address of Date & Time
18	Return HL=Address Of Disk Parameter Block
19	Return HL=Address Of Floppy Ready List
20	Return HL=Address Of Floppy Drive Sense Dat
21	Return HL=Address Of Hard Disk Sense Data
22	Return HL=Address Of Month Length Table

System Interrupt Theory

System Interrupts are handled in Z80 interrupt Mode 2. Locations 0008H is the interrupt entry routine which saves AF, BC, DE and HL. This routine also saves the stack pointer and sets the stack to a separate interupt routine stack with a return to an interrupt exit routine pushed on the stack. The exit routine recovers the registers, restores the stack pointer and returns control to the interrupted program. The return is made via a Z80 RETI instruction which informs Z80 peripherals that interrupt servicing has been completed.

Adding Interrupt Routines to the System Executive

Several locations in the Mode 2 interrupt vector table are available to the user who needs to add peripheral interrupt service routines. Your hardware must supply the low-order (LSB) address vector in response to "interrupt acknowledge" from the Z80 CPU. The following table shows which vectors are available to the user.

```
*    EEC0 - OFFBOARD CTC 4
*    EEC2 - OFFBOARD CTC 5
*    EEC4 - OFFBOARD CTC 6
     EEC6 - OFFBOARD CTC 7 (REAL TIME CLOCK)
*    EEC3 - UNUSED
*    EECA - UNUSED
*    EECC - UNUSED
*    EECE - UNUSED
*    EED0 - OFFBOARD SIO D
*    EED2 - OFFBOARD SIO D    AVAILABLE TO USER
*    EED4 - OFFBOARD SIO D
*    EED6 - OFFBOARD SIO D
*    EED8 - OFFBOARD SIO C
*    EEDA - OFFBOARD SIO C
*    EEDC - OFFBOARD SIO C
*    EEDE - OFFBOARD SIO C
     EEE0 - PRINTER SIO
     EEE2 - PRINTER SIO
     EEE4 - PRINTER SIO
     EEE6 - PRINTER SIO
     EEE8 - CONSOLE SIO
     EEEA - CONSOLE SIO
     EEEC - CONSOLE SIO
     EEEE - CONSOLE SIO
*    EEF0 - ONBOARD CTC 0
*    EEF2 - ONBOARD CTC 1
*    EEF4 - ONBOARD CTC 2
     EEF6 - ONBOARD CTC 3 (REAL TIME CLOCK)
     EEF8 - ONBOARD PIO A
*    EEFA - OFFBOARD PIO C
*    EEFC - OFFBOARD PIO D
```

After a system hardware reset, these locations contain a vector to a null routine which merely re-enables interrupts and performs a RETI instruction. However, they may be reloaded to point to other interrupt processing routines if you so desire. To process the interrupt, you may use the RST 1 instruction to save registers and stack, and exit the routine with a RET instruction which will restore the registers and stack. Interrupt processing is NOT re-entrant. This means that the current interrupt must be processed before another interrupt can be serviced. DO NOT re-enable interrupts from within an interrupt service routine.

The user must follow a few simple conventions to avoid conflict with the monitor and its interrupt routines. During initialization, the monitor will put the Z80 into interrupt Mode 2 and define an interrupt table, which is located at EECO in the current (version 3.10) monitor. This table is illustrated above. All the unused vectors (indicated by an asterisk) are initially set up to point at a routine within the monitor. This routine is located at F5B4 in the current revision of the monitor. In order to use the interrupt vector table, routines similar to those shown below are recommended. Note that if you define a vector to point within the TPA (transient program area), then return to CP/M. The next occurance of that interrupt will have unpredictable results. Usually the entire system crashes. To avoid this problem, we strongly recommend that you save the vectors before altering them, then restore them before returning to CP/M. The routines shown below will define a Zilog SIO chip to use the unused vectors (EEC8 through EECE) in the table. Please note when extending the interrupt daisy chain to other S-100 buss boards, Engineering Change No. 002 must be implemented on the SBC-100 Master (see ECN No. 002 in this book.)

Sample routines to define a ZSIO Chip:

```
INIT:     DI                        ; Disable interrupts while
                                        changing tables
          LD        DE,SAVECT       ; Index the vector save area
          LD        HL,0EEC8H       ; and the vectors to save
          LD        BC,4*2          ; 4 vectors, 2 bytes each
          LDIR                      ; vectors are saved
          LD        DE,0EEC8H       ; not put the new vectors in
          LD        HL,NEWVCT
          LD        BC,4*2
          LDIR                      ; new vectors installed
          .
SETUP THE ZSIO CHIP FOR INTERRUPTS AND ENABLE THEM
          .
          EI                        ;allow the new routines to run
          .
```

```
MAIN PROGRAM
          .
EXIT:     DI                        ;disable interrupts while changing table
          LD        HL,SAVECT       ;index the vector save area
          LD        DE,0EEC8H       ;and the vectors to restore
          LD        BC,4*2          ;4 vectors, 2 bytes each
          LDIR                      ;vectors are now restored
          JP        0               ;re-boot CP/M

TRANS:    EX        AF,AF'          ;save interrupted registers
          EXX
          .
  PERFORM TRANSMITTER BUFFER EMPTY INTERRUPT PROCESSING
          .
RETI:     EXX                       ;restore interrupted registers
          EX        AF,AF'
          EI                        ;allow interrupts again
          RETI                    ;reset interrupt system, return

EXTRNL:   EX        AF,AF'
          EXX
          .
          .
  PERFORM EXTERNAL/STATUS INTERRUPT PROCESSING
          .
          .
          JP        RETI            ;use common return from interrupt code

RECEIV:   EX        AF,AF'
          EXX
          .
          .
  PERFORM CHARACTER RECEIVED INTERRUPT PROCESSING
          .
          .
          JP        RETI

SPECAL:   EX        AF,AF'
          EXX
          .
          .
  PERFORM SPECIAL RECEIVE CONDITION PROCESSING
          .
          .
          JP        RETI

NEWVCT:   DW        TRANS           ;the new interrupt table
          DW        EXTRNL
          DW        RECEIV
          DW        SPECAL

SAVECT:   DS        4*2             ;the saved interrupt table
END
```

C. Format Disk Operating Procedure

The Format Disk Utility Program is provided for the purpose of formatting floppy diskettes. The program supports diskette formatting for the following recording formats:

1. Single Sided, Single Density
2. Single Sided, Double Density
3. Double Sided, Single Density
4. Double Sided, Double Density

It is important to note, that this utility program not only formats the specified diskette, but verifies as it formats by reading the sectors just formatted.

To execute the format utility program, enter the word FORMAT and then depress the RETURN key on your terminal keyboard.

The following menu will appear then appear on the CRT screen:

```
                    DISK FORMATTER V1.05
**************************************************
                    FORMAT MAIN MENU
**************************************************


                    <1>   EXIT TO CP/M.
                    <2>   FORMAT FLOPPY DISKETTES



                    Desired Selection _
```

If option 1 is selected, the system will exit to CP/M and the A> prompt will subsequently appear.

C. Format Disk Operating Procedure (continued)

If option 2 is selected, the following sub-menu will appear on your CRT screen:

```
                DISK FORMATTER V1.05
************************************************
                  FLOPPY DISKETTE
************************************************
```

Based on the contents of your floppy disk drives, one of the following messages will appear:

- Remove All floppy diskettes! ((Return) To exit.)

  This message will appear if any floppy disk drive attached to the system has a floppy diskette loaded. This safety feature of the system guards against unintentional formatting of user diskettes.

- Insert a diskette to be FORMATTED.

  If no drives contain diskettes at the time the FORMAT program is executed, then this message will appear. It is directing you to insert a diskette in any drive attached to the system. The FORMAT program will automatically "sense" the insertion of the diskette, and then will continue with the next menu screen display:

```
                DISK FORMATTER V1.05

************************************************
                  FLOPPY DISKETTE
************************************************

   >>  Entry: Drive D:, XXXXXXX sided  <<


        (S)ingle or (D)ouble density? _
```

C. Format Disk Operating Procedure (continued)

The XXXXXXX in the above menu will contain either single, or double, based upon the type of drive being utilized. The SBC-100 automatically determines if the diskette is double sided, or single sided and modifies the above menu to reflect the type of diskette sensed.

The acceptable replies to the message are S for single density, or D for double density.

After a valid reply to the message prompt has been accepted by the FORMAT program, the following sub-menu will appear on the CRT screen:

```
                    DISK FORMATTER V1.05
**********************************************************
                      FLOPPY DISKETTE
**********************************************************

 >> Entry: Drive D:, XXXXXX sided, XXXXXX density  <<

<1>  Cancel and Start Again.
<2>  Format Disk header only. (will not destroy data.)
<3>  Format entire disk.  (Destroys ALL previous data.)



                    Desired Selection? _
```

The above menu presents three options to the user. Option <1> allows you to start the program again from the main menu. Option <2> permits the formatting of the first track of the the diskette only. Option <3> formats the entire surface of the diskette, thereby destroying all data that may have been previously recorded on the diskette.

Th status line shown above, will depict the number of sides selected for formatting as well as the density. (Shown above as XXXXXXX sided, XXXXXXXX density).

At this point, the format program will begin formatting and then verifying each track of the diskette. Each side and track are shown on the display screen as it is being formatted.

C. Format Disk Operating Procedure (continued)

When the last track of the diskette has been successfully formatted, the following message will then appear on the CRT screen:

```
                    DISK FORMATTER V1.05

**********************************************************
                      FLOPPY DISKETTE
**********************************************************

 >> Entry: Drive D:, XXXXXX sided, XXXXXX density  <<
```

```
                  Remove Formatted Diskette!
```

The format program will wait for the formatted diskette to be removed from the drive before proceeding. When the diskette has been removed from the drive, the following sub-menu will appear:

```
                    DISK FORMATTER V1.05

**********************************************************
                      FLOPPY DISKETTE
**********************************************************

 >> Entry: Drive D:, XXXXXX sided, XXXXXX density  <<
```

```
          Format (A)nother diskette or e(X)it? _
```

Valid replies to the above prompt are A to specify another diskette be formatted, or X to exit to the main format program menu.

D. Disk Copy Operating Procedure

The DISKCOPY utility program provides the floppy disk user with an efficient means of creating duplicate copies of his or her diskette library.

This utility will copy either from one diskette to another, or permit owners of single drive systems to copy a diskette utilizing only a single drive. The latter is accomplished by prompting the user to change diskettes after a number of sectors have been read into memory, writing those sectors to the destination diskette, and finally re-prompting the user to re-insert the source diskette. This operation is repeated until all sectors have been copied.

Unlike other copy programs, this utility program not only reads and writes source and destination data, but actually performs full verification of the data written to the destination diskette. This is accomplished by first reading a number of sectors from the source diskette into memory, writing the data to the destination diskette, reading the sectors just written to the destination diskette into memory, and finally comparing the sectors read from both the source and destination diskette.

Since data is read on a track basis, the copy completes in a very short period of time.

To invoke the disk copy utility program, enter the program name DISKCOPY and depress the carriage return key. After the program has been loaded, the following menu will appear:

```
                    FLOPPY DISKETTE COPY V1.00
**********************************************************
                     COPY OPERATION SELECT
**********************************************************

                     <1>  Normal Copy.
                     <2>  Exit To CP/M.
                     <3>  Single Drive Copy.


                     Desired Selection? _
```

D. Disk Copy Operating Procedure (continued).

If option 2 (Exit To CP/M) is selected, control will be returned to the CP/M operating system.

If option 3 (Single Drive Copy) is selected, the appropriate prompts will assist the user in making a copy of a diskette utilizing a single drive.

If option 1 (Normal Copy) is selected, the following sub menu will appear on the CRT display screen:

```
                    FLOPPY DISKETTE COPY V1.00
**************************************************************
                         NORMAL COPY
**************************************************************
```

Source Drive (a,b) or e(x)it? _

The lower case letters a, and b designate the floppy diskette drive identification assigned to the drives via the CONFIG utility program (normally A, and B in a two drive system).

The user must reply by entering the source drive to be used in the diskette copy program. After accepting and validating the user reply, the disk copy program will ask the user to to insert the diskette in the specified drive. This is accomplished by prompting the user with the following message:

Source in x: then type <Return> or <X> to exit.

The lower case x: depicts the drive id entered in the preceding prompt. After the return key is depressed, the program will validate the diskette in the specified drive, and subsequently ask for the output drive with the following prompt:

Destination in x: then type <Return> or <X> to exit.

D. Disk Copy Operating Procedure (continued).

After the destination diskette is inserted, the program will validate the diskette in the destination drive and then display the following menu on the user CRT screen:

```
                    FLOPPY DISKETTE COPY V1.00
**********************************************************
                         NORMAL COPY
**********************************************************

          Ready to copy from Drive a: to Drive b:


                    (E)xecute or e(X)it? _
```

At this time, the program is ready to copy as specified in the status line. The user can proceed by entering E, or return to the main menu by entering X.

If an E is entered, the following screen will be displayed on the user's CRT terminal:

```
                    FLOPPY DISKETTE COPY V1.00
**********************************************************
                         NORMAL COPY
**********************************************************

          Copying a: to b: with Verify.


                                    Side      Track
Destination Read

Destination Write

Verify
```

D. Disk Copy Operating Procedure (continued).

During execution of the copy program, the sides and tracks are displayed as read and written. Further, the Destination Read, Destination Write, and Verify messages are alternated as the applicable operation is actually taking place.

At the conclusion of this disk copy operation, the following screen is displayed on the user's CRT Terminal:

```
                    FLOPPY DISKETTE COPY V1.00
**********************************************************
                         NORMAL COPY
**********************************************************

                         COPY COMPLETED



                    (A)nother copy or e(X)it? _
```

The user has the option of returning to CP/M, or proceeding with additional copy procedures.

E. System Configuration Operating Procedure

The Sierra Data Sciences Configuration Utility Program is a powerful tool in that can be used for integrating the SBC-100 into a user-tailored configuration.

It is completely menu driven, thereby providing a simplistic means of system implementation without the need to know the internals of CP/M or assembler language. This section explains in detail the usage of CONFIG, and shows common examples.

To invoke the program, enter CONFIG at the CP/M prompt ">". The following menu will then appear on the CRT screen:

```
                    SDS Configurator Version 1.00

**********************************************************************

                        Parameter Change Menu

**********************************************************************


        <0> Parameter Storage. (Exit via this selection)
        <1> I/O port configuration.
        <2> Logical to Physical I/O assignments.
        <3> Terminal controls. (Clear & home and Cursor)
        <4> Logical to Physical drive assignments.
        <5> Disk specification
        <6> Passwords.

                        Desired selection? _
```

E. System Configuration Operating Procedure (continued)

<0> Parameter Storage. (Exit via this selection).

Selecting this option will cause the following sub-menu to appear to be displayed:

```
                    SDS Configurator Version 1.00

**********************************************************************

                        Parameter Storage Menu

**********************************************************************


              <1> Return to change menu. (More changes)
              <2> Exit to CP/M - No changes.
              <3> Exit to CP/M - Change running system.
              <4> Change system tracks on disk.

                Possible Disk Selections

                        A:
                        B:
Desired selection? _
```

Selection 1 - Return to change menu. This selection will return you to the main menu, allowing you to make additional changes in the configuration.

Selection 2 - Exit to CP/M with no changes. This selection will return control to CP/M, without altering the running system. It is used after selection 4 below, or to abort the configuration process.

Selection 3 - Change running system, Exit to CP/M. This selection will also return control to CP/M, but in addition will activate the new configuration immediately. It is important to note that selecting this option does not change the system as it exists on disk. This option may be used to test a new configuration before actually recording it onto a diskette.

Selection 4 - Change system tracks on disk. This selection will alter the copy of CP/M that is resident on disk. This means that all further cold boot operations will contain the new configuration. This command does not alter the running system.

E. System Configuration Operating Procedure (continued)

<1> I/O port configuration. Selecting this option from the main menu will bring up the prompt

"<1>I/O; (S)erial, (P)arallel or e(X)it? _".

Entering an X will return you to the main menu. Entering S or P will take you to either the Serial I/O sub-menu or the Parallel I/O sub-menu respectively. Both sub-menus and their corresponding explanations follow:

SDS Configurator Version 1.00

****

Serial Port Parameters

****

		Present Serial Configuration					New Serial Configuration			
	Port	A	B	C	D	*	A	B	C	D
	Parameter									
<1>	Speed.....:	9600	1200	9600	9600	*	9600	1200	9600	9600
<2>	Parity....:	None	None	None	None	*	None	None	None	None
<3>	Stop bits.:	2	2	2	2	*	2	2	2	2
<4>	*SRTS.....:	No	No	No	No	*	No	No	No	No
<5>	*DTR.....:	No	Yes	No	No	*	No	Yes	No	No
<6>	Protocol..:	Xon	Etx	None	None	*	Xon	Etx	None	None

*RS-232 control signals SRTS & DTR. EIA pins 19 and 20 respectively.

<1>I/O, S-port; Which port? _

You may respond with A,B,C,D or X to this prompt. X will return you back to the "(S)erial, (P)arallel or e(X)it" prompt. Note that the A and B ports are the onboard SIO ports, and the C and D ports are external to the SBC-100. The BIOS may be configured expanded to use additional off-board Serial Ports, such as the Sierra Data Sciences ZSIO (4-port Serial Communications Card), provided they are located at ports B0 through B3. The configuration shown above is for an ASCII CRT utilizing X-on/X-off protocol on port A and a Diablo Letter Quality Printer on port B. Ports C and D are unused, and hence, show default values.

After entering a port number, the system prompts for the parameter to be changed via the following prompt:

"<1>I/O, S-port, X; Which parameter? _"

X; is the port that you have selected.

E. System Configuration Operating Procedure (continued)

The valid responses to this prompt and their respective descriptions are:

<1> Speed. This parameter controls the speed or baud rate of the port. Both transmission and reception occur at the same rate. The valid rates are: 110, 150, 300, 600, 1200, 2400, 4800, and 9600. To change the baud rate, enter one of the above values.

<2> Parity. This parameter controls whether the SBC-100 will transmit and check parity on each character as it is processed. The valid options are: O - Odd parity is used; E - Even parity is used; N - There is no parity checking.

<3> Stop bits. This parameter controls the number of bits used to indicate the end of each character. Either 1 or 2 is valid. (2 is most commonly used).

<4> SRTS - System Request To Send. This parameter determines whether the computer will activate the RTS line in the EIA interface whenever data is to be sent to the port. Some terminals and many printers require this feature. Valid responses are:

Y - RTS is used.
N - RTS is not used. (See note below)

<5> DTR - Data Terminal Ready. This parameter is essentially the reversal of SRTS. It is used by the terminal device to indicate to the computer that the device is ready to accept more data. It is often used with SRTS above. The valid responses are the same as for SRTS. (See note below)

<6> Protocol. This parameter determines what protocol, if any, is used by the SIO port. Essentialy, protocol is a software form of handshake, with the terminal device sending commands to the effect of "Send more data" and "Wait, processing data". The valid options are: N - No protocol is used; X - Xon/Xoff protocol is used; E - Etx/Ack protocol is used. (NOTE: It is suggested that Etx/Ack be used for Diablo type letter quality printers, and that Xon/Xoff be used for NEC Spinwriters. In addition, if a word processing package such as WordStar is used for a letter quality printer, select the CP/M list device option when using either Etx/Ack, or Xon/Xoff).

NOTE: In order to use the SRTS and DTR lines, the SBC-100 serial ports must be strapped for their use. Refer to the configuration section of the SBC-100 hardware manual for strapping information. Additionally, if the ETX/ACK option is used, SRTS and DTR cannot be used.

E. System Configuration Operating Procedure (continued)

Refer to the owners manual for the terminal to determine exactly what software configuration should be used, how your particular terminal should be configured, and what interface lines are required. The cable supplied with the SBC-100 contains all of the interface lines required for both async and sync operation, and in most cases a simple cable is called for. Note that in order for the onboard serial ports to function in sync mode, the ZSIO option must be installed on the SBC-100.

E. System Configuration Operating Procedure (continued)

SDS Configurator Version 1.00

****

Parallel Port Parameters

****

Old Parallel Configuration	New Parallel Configuration
PioA	PioA
Output	Output

<1>I/O, p-port, A; (I)n or (O)ut? _

This menu is self-explanatory. The only options available are I for Input, O for Output or X to return to the "(S)erial, (P)arallel..." prompt. Note that if the Winchester hard disk option is in use, the parallel port is not available, and must NEVER be changed with CONFIG.

E. System Configuration Operating Procedure (continued)

Choosing Logical to Physical I/O assignments (Main menu selection 2) will bring up the following sub-menu:

```
                    SDS Configurator Version 1.00

**********************************************************************

                Logical device to Physical Port Assignment

**********************************************************************

      Old assignments                      New assignments
RDR:     PUN:     LST:          RDR:     PUN:     LST:
SioA     SioA     SioB          SioA     SioA     SioB

    Logical devices                    Physical devices
        (R)eader                           Sio(A)
        (P)unch                            Sio(B)
        (L)ist                             Sio(C)
                                           (P)arallel

                <2>L/P-I/O; Logical device? _
```

This option allows you to assign the CP/M logical devices to any of the I/O ports available to the system. The valid responses are R for the RDR device; P for the PUN device; L for the LST device; and X to return to the main menu. After selecting one of the logical devices, the system will prompt for the physical device with the following message:

"<2>L/P-I/O, XXX:; Physical device? _".

Where XXX is either RDR, PUN or LST, depending upon which logical device is being assigned. The valid responses for this prompt are: A,B,C for the serial I/O ports and P for the parallel I/O port. See the notes in the I/O configuration section regarding the SioC and parallel ports.

E. System Configuration Operating Procedure (continued)

Selecting option <3> (terminal controls), prompts the user with the following sub-menu:

```
                    SDS Configurator Version 1.00

**************************************************************************

                            Terminal Control

**************************************************************************

        Terminal Type       Clear and Home       Absolute Cursor Positioning
                            Sequence    Delay      Lead-in      Order   Offset

<1>     SOROC IQ-120        <ESC>*        5        <ESC>=        X,Y      31
<2>     (Unassigned)
<3>     (Unassigned)
<4>     (Unassigned)
<5>     (Unassigned)
<6>     (Unassigned)
<7>     (Unassigned)
<8>     None
<9>     Add or change

* = Match on Old and New, # = match on New only, % = Match on Old only.

<3>T-Ctrl; Which entry (1-9)? _
```

This feature of the system configuration program provides the user with a means to become terminal independent even though different terminals may be used on the system. This is accomplished through the definition of the clear screen, position cursor, and delay parameters with this menu screen.

To make this option useful however, the user must code all calls for clear screen, and position cursor through the system executive internal command structure. (See Terminal Controls of System Executive Internals Section).

Selecting option 9 permits the user to add, change and or delete from one to seven different terminal types.

After selecting option 9, the program will prompt you to enter the terminal name, clear sequence, delay sequence, and position cursor sequence for the terminal.

The delay is expressed in milliseconds, and the offset is expressed in decimal.

E. System Configuration Operating Procedure (continued)

Selecting option 4 of the main menu will bring up the following sub-menu:

```
                    SDS Configurator Version 1.00

**************************************************************************

                    Logical to Physical Drive Assignments

**************************************************************************

   Old assignments                      New assignments

     A: = U0,H0                           A: = U0,H0
     B: = U0,H1                           B: = U0,H1
     C: = U0,H2                           C: = U0,H2
     D: = 0                               D: = 0
     E: = 1                               E: = 1
     F: =  (Unassigned)                   F: =  (Unassigned)
     G: =  (Unassigned)                   G: =  (Unassigned)
     H: =  (Unassigned)                   H: =  (Unassigned)
     I: =  (Unassigned)                   I: =  (Unassigned)

                <4>L/P-drv; Logical drive (A-I)? _
```

This menu shows the configuration for a 21 Megabyte Micropolis Winchester and two floppy disk drives. In a floppy based system, Ux,Hy will be replaced by a single digit, as is shown for the D and E drives. At this point, the system is expecting either one of the letters A through I or X (Which returns you to the main menu). The following two sections are for the hard disk system, and the floppy system respectively.

Defining Winchester Hard Disks to the system:

In a hard disk system, the next prompt will be:

"<4>L/P-drv, L-drv X; (F)loppy or (H)ard disk? _",

to which you may respond with F if the drive is a floppy, H if it is a Winchester hard disk drive. If you respond with F for floppy, the prompts will continue as in the section below on floppies. In a hard disk system, the next prompt will be :

"<4>L/P-drv, L-drvX; Unit number (0-3)? _".

The reply to this prompt, is the single digit (0-3) corresponding to one of the four possible hard disk drives.

E. System Configuration Operating Procedure (continued)

The next prompt is:

"<4>L/P-drv, L-drv X, H-dsk Y; Headnumber (0-4)? _".

The head number of the platter that will represent the drive X should be entered. Note that each platter is considered a distinct drive. For example, in the menu shown above, platter 0 of unit 0 is considered to be the A: drive at all times. After entering the head number, the sub-menu is redisplayed showing the changed drive assignment, and you are returned to the "logical drive..." prompt.

Defining Floppy Disk Drives to the system:

In a floppy based system, or if you respond with F to the Floppy/Hard disk prompt in a hard disk system, you will receive the prompt:

"<4>L/P-drv, L-drv X, F-dsk; Physical drive (0-3)? _".

You must respond with the drive number (0-3) of the floppy disk drive that will correspond to the logical device selected.

NOTE: If you re-assign a physical unit to another logical unit, the old logical unit becomes "Unassigned" and will not be available to the system.

E. System Configuration Operating Procedure (continued)

By selecting option 5 on the main menu, you may alter the disk specifications of the floppy drives in your system.

NOTE: This section applies only to floppy drives systems.

The following sub-menu appears when this option is selected:

```
                    SDS Configurator Version 1.00

**********************************************************************

                          Disk Specification

**********************************************************************

          Old assignments                          New assignements
Tracks  Step Rate  Head Load                Tracks  Step Rate   Head Load
  77        3         36                      77        3          36

                  <5>D-spec; Which spec (T,S,H)? _
```

This sub-menu allows you to alter the number of tracks per floppy drive, the rate at which the drives step from track to track, and the amount of delay required from the time the head load command is issued until the drive is ready to access data.

Both the step speed and the head load time are expressed in milliseconds. The Shugart 80x series uses an 8 msec step time. Qume DataTrak 8s (DT8), Shugart 85X series, and Tandon 8 inch Slimline Drives can run with a 3 msec step time. All of these drives use a 36 msec head load delay. Other drives may require different timing. Consult the hardware manual for the specific drives that you are using.

NOTE: If different drives are mixed in your system, e.g. Shugart 801Rs and Qume DataTrack 8s, then the step time of the slowest drive must be selected (i.e. this is a global system parameter).

E. System Configuration Operating Procedure (continued)

The final option available on the main menu is #6, Passwords. This option controls the security used when accessing the system. Choosing option 6 brings up the following sub-menu:

SDS Configurator Version 1.00

****

Passwords

****

Password Number	Access Level
<1>	1
<2>	2
<3>	3
<4>	4
<5>	(Unassigned)
<6>	(Unassigned)
<7>	(Unassigned)

<6>PWD; Which password entry? _

By entering a number from 1-7, you may alter the security at any one of seven levels.

NOTE: You may not alter the password or security level of any password that has a higher security level than the one that you are currently running under.

After entering a password number, the following prompt will appear:

"<6>PWD, #X; Change (P)wd or (L)evel? _",

This prompt requests whether you desire to change the password or security level of password X.

If an L (Level) is entered, you will receive the prompt:

"<6>PWD, #X, C-lvl; New level (1-7)? _"

after which you may enter the new security level desired.

If the password is being changed, you will receive the prompt:

"Change pwd, #7; New entry? _____"

E. System Configuration Operating Procedure (continued)

after which you may enter the new password. NOTE: Once a password has been entered, there is no way to inquire as to what a particular password is, so REMEMBER YOUR PASSWORD.

F. TAD (Time/Date Set/Report) Utility Operating Procedure

The TAD Utility Program provides for the setting and reporting of the current date and time utilizing the on-board capabilities of the SBC-100.

Once the date and time have been set using this program, the current date and time will be maintained utilizing the interrupt-driven real time clock features on the SBC-100 PCB. These fields (Time & Date) are available to the user in the Page Zero area maintained by the system executive (See System Executive Internals).

To invoke this program, enter the program name as shown below, followed by a carriage return:

```
TAD
```

In a few seconds, the following message will appear if the time and date have not been set since the computer was powered on:

```
Time not initialized.  Set?  (Y/N)
```

If "N" is the reply to this message prompt, the program will exit to CP/M. If "Y" is entered, the following message prompt will appear:

```
Present Setting:

NOT INITIALIZED.

Set DATE and TIME

Month (1-12)?
```

The program is informing the user that the timer facilities have not yet been initialized and requesting that the current month be entered. Valid response to this message are a month-of-year value, i.e. 01 (January) through 12 (December).

After the month has been entered, the program will ask for the Day-of-Year, Year-of-Century, Hour-of-Day, Minute-of-Hour, Second-of-Minute, and AM or PM with the respective message prompts as shown below:

```
Day?

Year (1901-2099)?

Hour (1-12)?

Minutes (0-59)?
```

F. TAD (Time/Date Set/Report) Utility Operating Procedure (cont.)

Seconds (0-59)? (or <Return> to ignore.)

(A)m or (P)m?

After all of the replies have been made to the above message prompts, the following message prompt will appear:

<Return> to start clock, then <Return> to exit.
Or <R> to (R)e-Set time.

If a carriage return is entered in response to the above prompt, the date and time will be displayed every second in the format as shown below:

8:55:00 AM ; Friday : January 1, 1982

To exit the program, simply enter an additional carriage return. The system time is now active. The time and date will be updated until the next power-off/power-on sequence.

If it is desired to start again and reset the time and date, then an "R" response will return to the Set Date and Time sequence, thereby permitting the user to re-set the time and/or date.

Once the system timer facilities have been activated, to report the date and time enter:

TAD <Return>

The time and date will be displayed as above, and then the program will exit to CP/M.

Once the system timer has been activated, and it is required that it be reset, enter:

TAD SET <Return>

Again, the present date and time will be displayed, but in addition, the set time and date logic of the program will be invoked allowing the user to Re-Set these values if required.

The SDS BACKUP utility is designed for quick backup of a large capacity disk drive, such as a Winchester, onto a smaller drive such as a floppy disk drive. It allows the user to copy an entire Winchester platter of 7 Meg in about 15 minutes. The program is designed to automatically prompt for diskette changes when the current disk is full. The general format for its use is as follows:

BACKUP source-files dest-drive

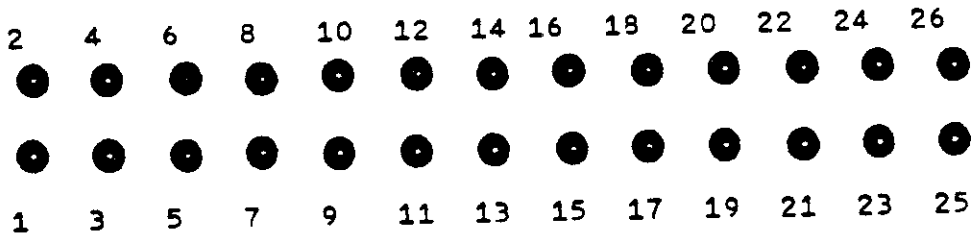
Where source-files is any valid CP/M filespec, and dest-drive is the drive name (letter) of the floppy drive that will contain the backed up copy. For example, to copy all the files from the A: platter of a Winchester onto a floppy drive C you would enter:

A>BACKUP A:*.* C<cr>

Special Notes:

1) BACKUP only recognizes the drives A-D, so if you have your floppy drives setup as E-P, you must run CONFIG and re-assign them before using BACKUP.

2) BACKUP will not copy read-only files. In order to backup R/O files, they must be changed to Read/Write using the STAT command first. See the Digital Research document "CP/M 2 Users Guide" for information on the STAT command.



	Master	Slave
1 - B3	2 - Ground	22 - BRDY
3 - B4	4 - N.C.	26 - ARDY
5 - B7	6 - B1	
7 - B6	8 - B2	
9 - B5	10 - B0	
11 - A7	12 - Reset	
13 - A6	14 - N.C.	
15 - A5	16 - +5V @100 ma	
17 - A4	18 - Ground	
19 - A3	20 - BSTB	
21 - A2	22 - ARDY	
23 - A1	24 - ASTB	
25 - A0	26 - BRDY	

Figure 1.
PIO Connections
Master Connector H4
Slave Connector J3

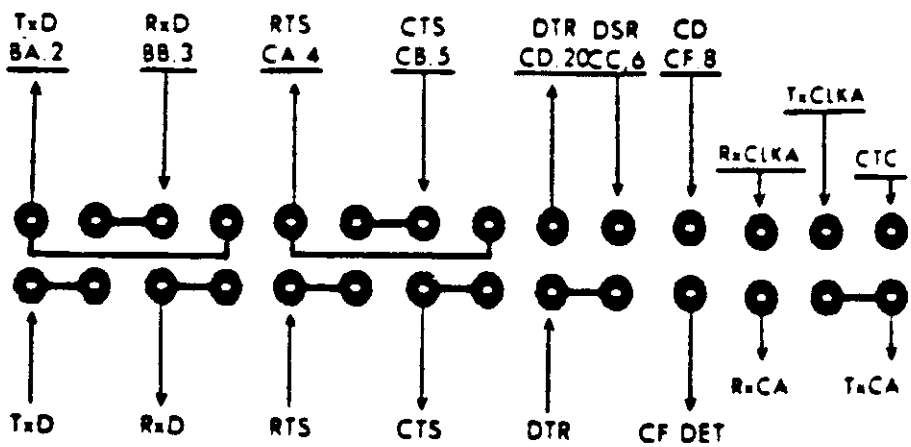


Figure 2.
SIO Configuration
Header connections
Shorting Blocks
1 and 2.

SLAVE ONLY

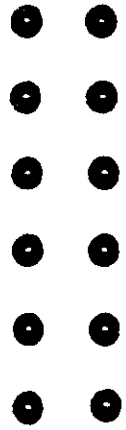


Figure 3.
Shorting Block 4
Port address selection

A Shunt in place indicates a 1 in the appropriate bit of the address. Note that bits A0 and A1 are not decoded.

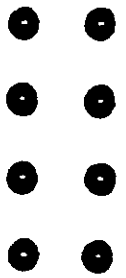


Figure 4.
Interrupt Configuration Area
Shorting Block 3

Place shunts in either Interrupt or No Interrupt Locations to control Interrupts to the S100 Master Processor. Note that two shunts are needed for both configurations.

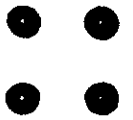


Figure 5.
Shorting Block 5

If shunt is in place, appropriate line will be readable in the interrupt vector to the S100 buss/

Figure 6.

X-Buss Expansion Interface Connector J1

Slave Only

Pin #*	Name	Function
1	A7	
3	A6	
5	A5	
7	A4	Low order address lines
9	A3	
11	A2	
13	A1	
15	A0	
17	IORQ	I/O Request
19	RD	Read cycle
21	WR	Write cycle
23	$WAIT_{OC}$	Processor wait
25	INT	Processor interrupt
27	D1	Non-maskable interrupt
29	D0	
31	D7	Data lines
33	D2	
35	M1	M1 cycle
37	D6	
39	D5	Data lines
41	D3	
43	D4	
45	CLOCK	System Clock (2/4 Mhz)
47	RESET	Board reset
49	IORQ	Delayed IORQ
50	IEO	Interrupt out for daisy chain

*All even numbered connectors (Except 50) are grounded.

Figure 7.

X-Buss Expansion Interface Connector J2

Slave Only

Pin #*	Name	Function
1	A15	
2	RFRSH	Memory refresh
3	A14	
5	A13	
7	A12	High order address lines
9	A11	
11	A8	
13	A9	
15	A10	
17	EXTRAM	X-Buss Extended Memory
19	MREQ	Memory Request

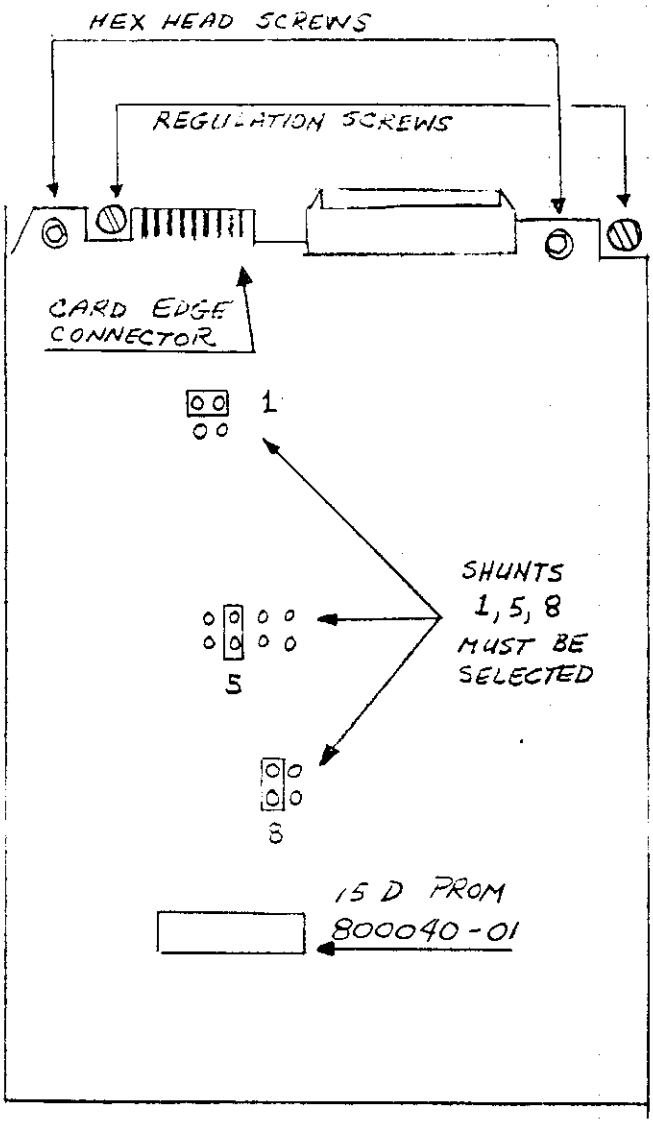
* All even-numbered pins (except 2) are grounded.

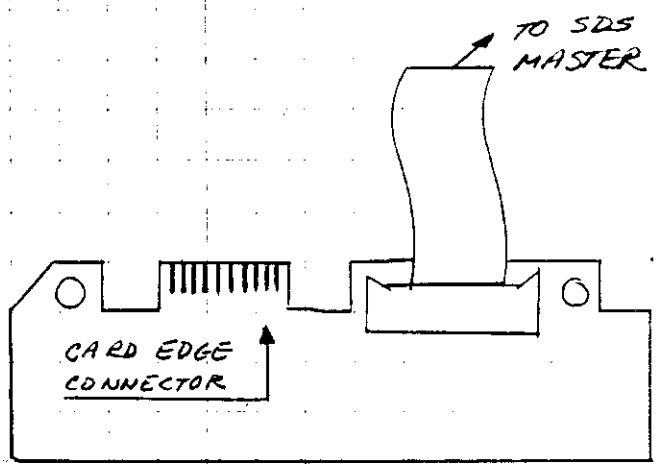
Note: None of the lines on the X-Buss are buffered, requiring buffers on any expansion boards used to avoid excessive loading of the Z80.

MICROPOLIS DISK INTERFACE

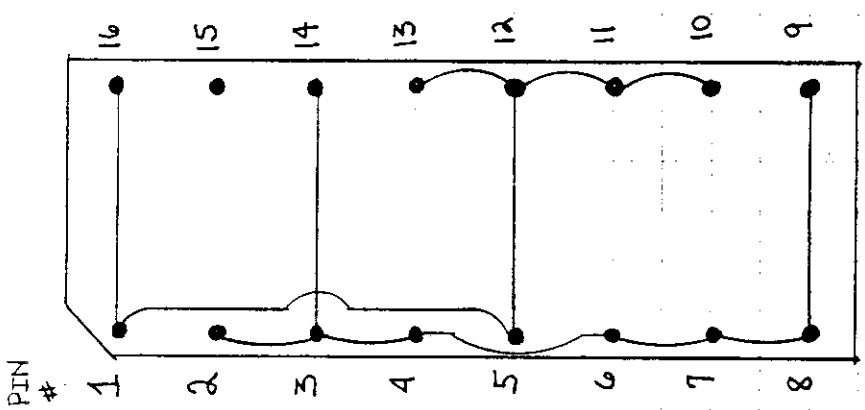
Supplied parts
1. Interface PC Board
2. 2 Screws with spacers
3. Twin cardedge connector
4. Interface cable

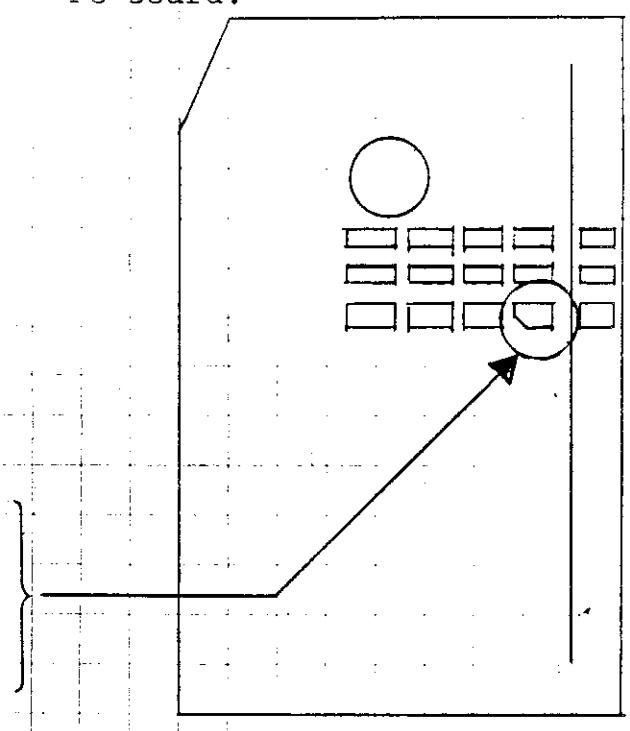
SIERRA DATA SCIENCES
21162 Lorain Avenue
Fairview Park, Ohio 44126
(216) 331-8500





Step 1: Remove hex head screws from drive as pictured.
Step 2: Set shunts as shown.
Step 3: Place SDS PC Board ontop of drive, aligned properly.
Step 4: Connect both cardedge from SDS PC Board to disk cardedge connector with supplied part.
Step 5: Insert supplied screws with spacers and tighten.
Step 6: Insert interface cable on SDS PC Board.





By removing regulation screws as pictured, and center screw, the drive PC Boards may be lifted showing the underside of PC Board 3 of the Micropolis drive. Check the header shown above to assure it being correct.

Figure 10. Hierarchy of Interrupt Priority

Highest:	CTC Channel 0
	CTC Channel 1
	CTC Channel 2
	CTC Channel 3
	S100 PIO Channel A - Slave Only
	S100 PIO Channel B - Slave Only
	External PIO Channel A
	External PIO Channel B
	SIO Channel A
	SIO Channel B]
Lowest:	X-Buss - Slave Only

Shugart 800 Drive

1. X - jumper
2. DC - not used
3. D - open
4. C - jumper
5. I - trace intact
6. R - trace intact
7. S - trace intact
8. DS1, 2, 3, 4 - select appropriate drive address
9. T1, 3, 4, 5, 6 - jumpered on last drive in system
   T2 - jumpered on all drives
10. HL - open
11. DS - open
12. RI - trace intact
13. RR - trace intact
14. Y - open
15. Z - jumper
16. 800 - jumper
17. 801 - open
18. A - jumper
19. B - open

Figure 8. Shugart 800/801 jumper configuration for use with SBC-100.

OUME DataTrak 8 Configuration

The following shunts should be inserted:

2S

DC

C

DSx (Drive select)

U1E - All connections should be intact with the exception of B and HL.

NOTE: The last drive in the daisy chain MUST have the terminator resistor packs installed. All other drives MUST NOT have the resistor packs installed.

SHUGART 850 DRIVE

DS1 through DS4	Select Appropriate Drive
1B through 4B	All Open
RR	Trace Intact
RI	Trace Intact
*R	Closed
2S	Jumper
850/851	850 Jumpered
*I	Closed
*S	Don't Care
DC	Don't Care
*HL	Open
DS	Open
WP	Trace Intact
NP	Open
D	Don't Care
M	Open
DL	Open
*A	Closed
*B	Open
*X	Closed
C	Closed
*Z	Closed
Y	Open
S1	Open
S2	Closed
S3	Open
TS	Don't Care
FS	Don't Care
IW	Closed
RS	Closed
RM	Open
HLL	Open
IT	Closed
HI	Open
F	Open
AF	Closed
NF	Open

* A 16-pin programmable shunt is provided for these eight signals.

#001

ENGINEERING CHANGE NOTICE

Subject: Reset on Power Up

Reason for Change: This modification will allow the SDS SBC-100 to boot on power up. If this feature is needed or desired, carefully follow the instructions below.

1. Cut S-100 Pin 75 free from R11, Pin 5. (This cut is on the next to last layer under U54.) On the solder side of the board, this trace goes from U54 Pin 13 through U54 Pins 1 and 2 and is shown in Figure 1 as a horizontal trace. Cut to inner layer as shown in Figure 1 until trace is broken. A Dremil tool is ideal for this type of cut.

2. Cut S-100 Pin 75 free between first and second feed through as shown in Figure 1.

3. Cut CTC Pin 17 free as shown in Figure No. 2.

4. Jumper U54 Pin 13 to U28 Pin 6, Figure No. 3.

5. Jumper U28 Pin 6 to CTC (U37) Pin 17, Figure No. 3.

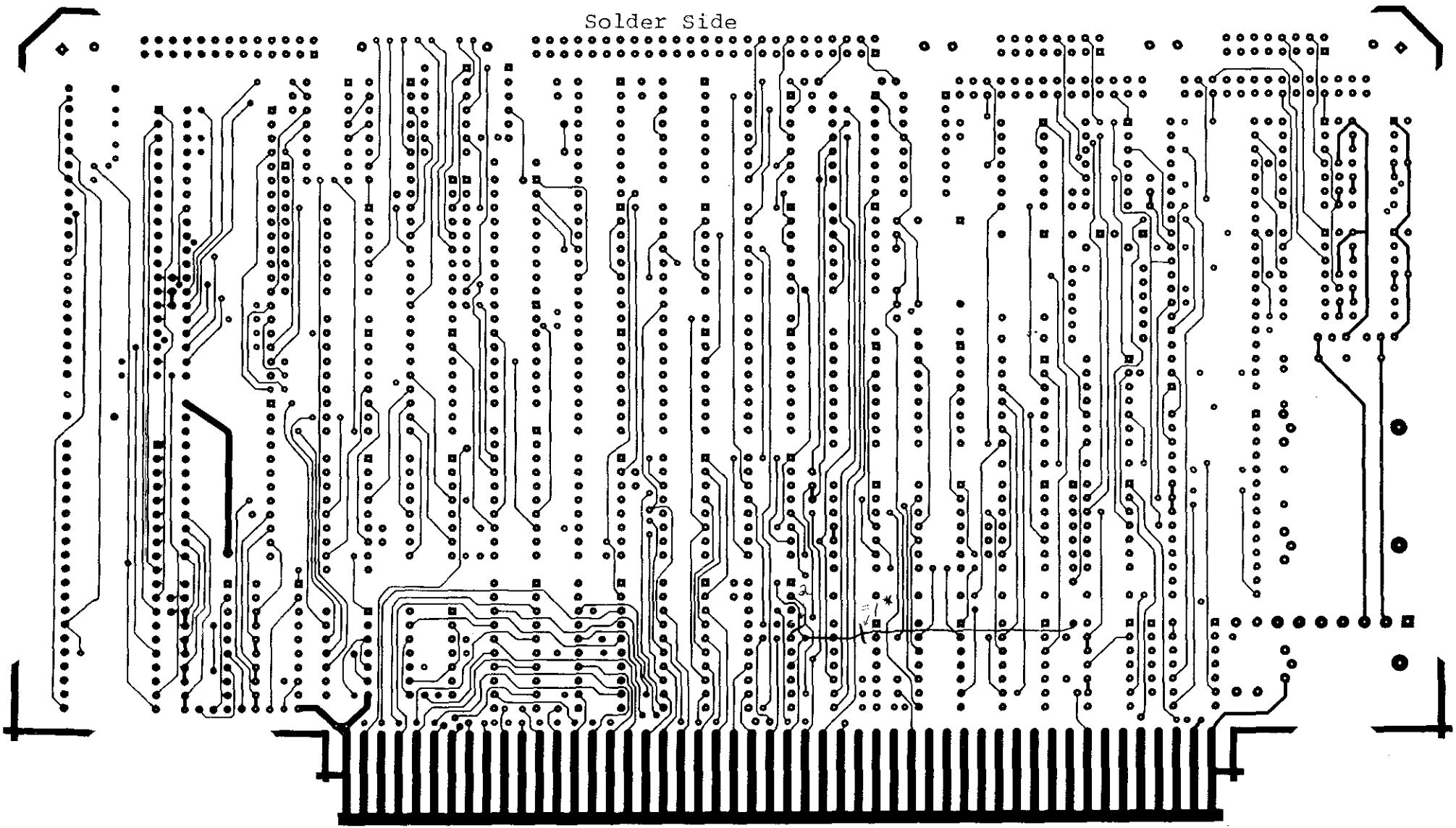
6. Jumper R11 Pin 5 to first feed through from S-100 Pin 75, Figure No. 3.

7. On Schematic, change as shown in Figure No. 4.

ECN No. 001

Reset on Power Up

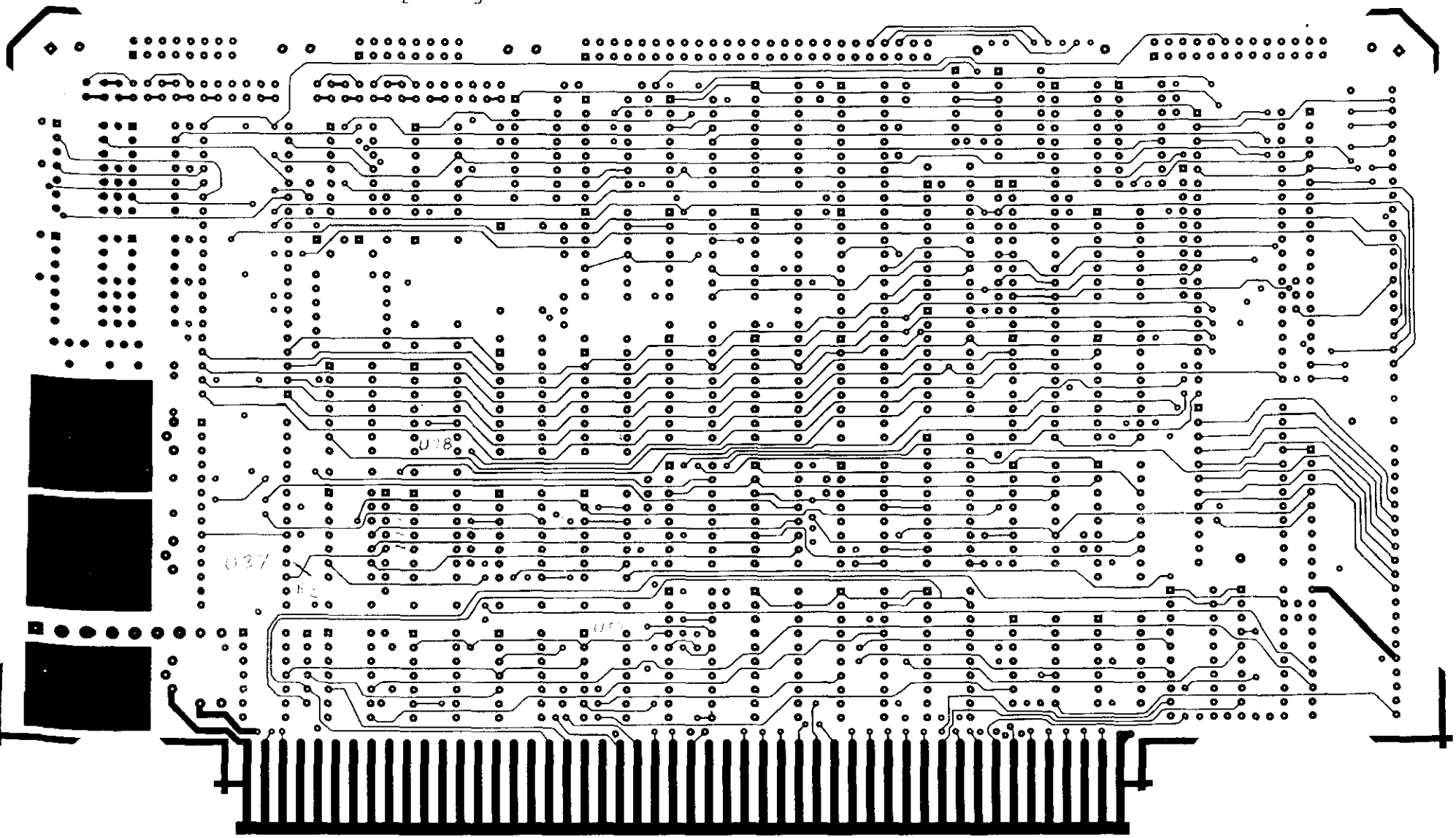
Figure 1 of 4



REDUCE 50%

ECN No. 001

Reset on Power Up Figure 2 of 4



LAYER 1

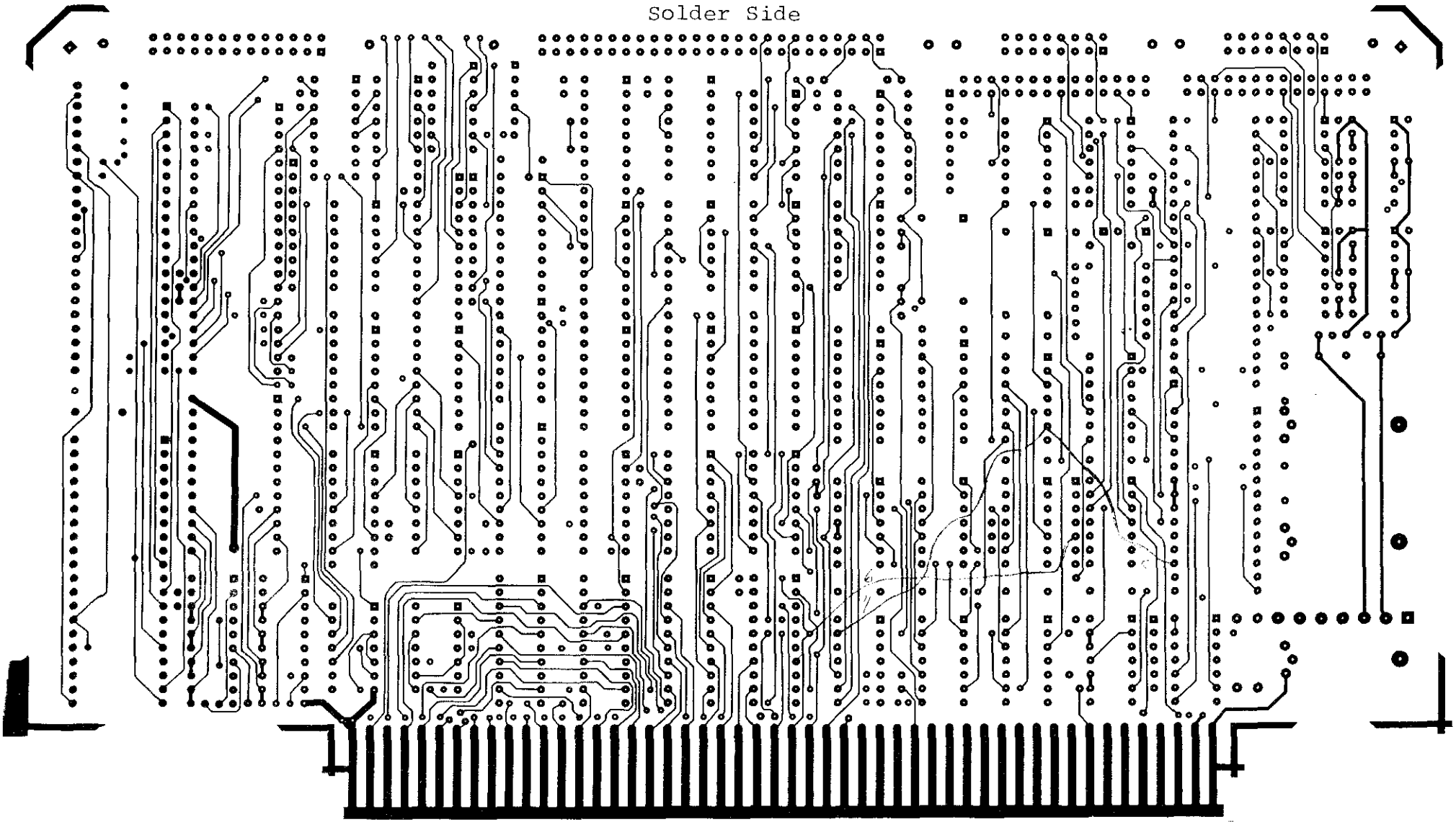
COMP SIDE

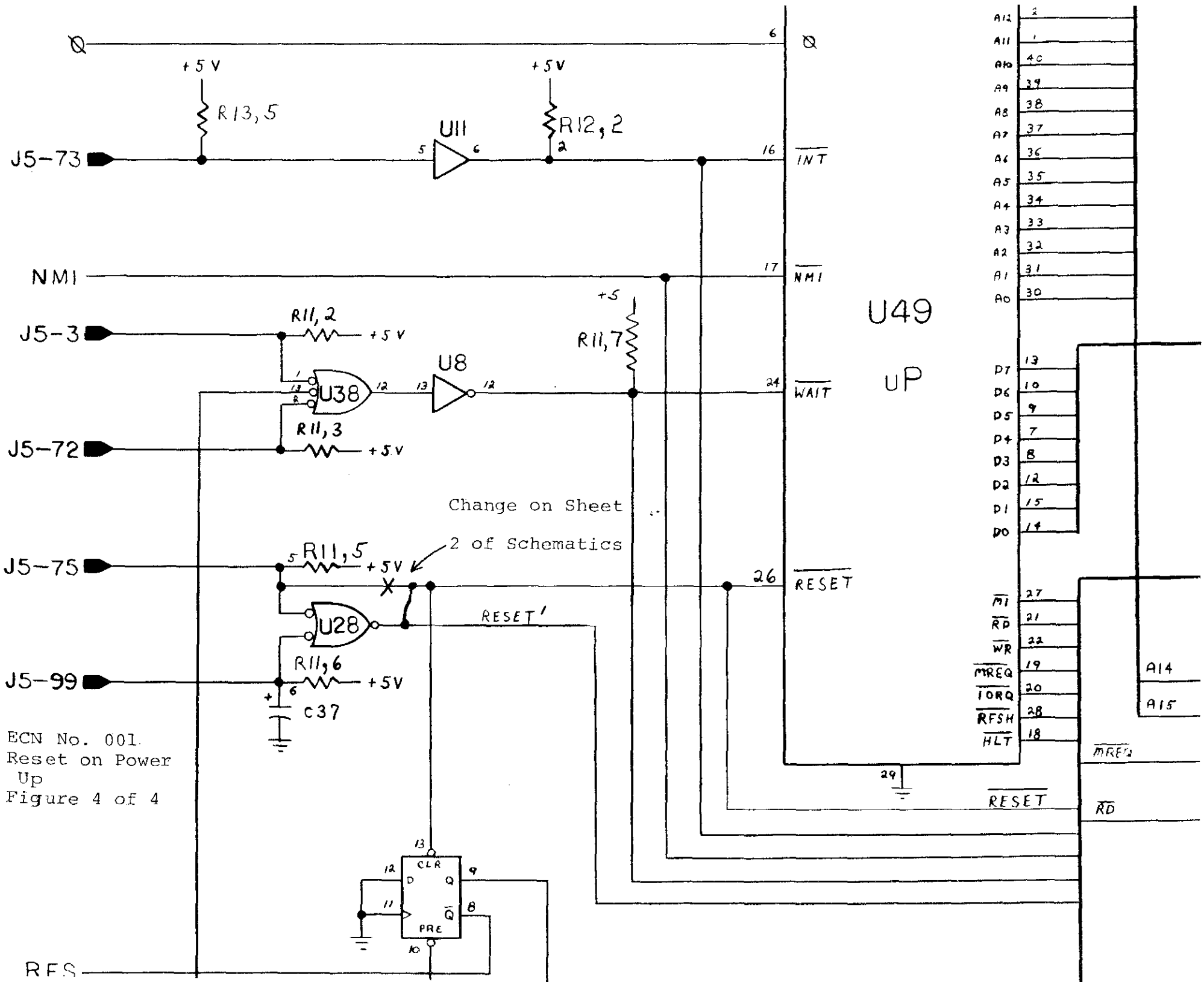
ECN No. 001

Reset on Power Up

Figure 3 of 4

Solder Side




Ø
+5V
R13,5
J5-73
U11
+5V
R12,2
INT
NMI
R11,2
J5-3
+5V
U38
U8
R11,7
+5
NMI
WAIT
R11,3
J5-72
+5V
U49
uP
Change on Sheet 2 of Schematics
R11,5
J5-75
+5V
RESET
U28
RESET'
R11,6
J5-99
+5V
C37
CLR
D
Q
PRE
RESET
RD
A14
A15
MREQ
ECN No. 001
Reset on Power Up
Figure 4 of 4

#002

ENGINEERING CHANGE NOTICE

Subject: Extend interrupt Daisy Chain to S-100 Bus.

Reason for change: This change will allow the interrupt Daisy Chain from the SDS-SBC-100 board to be extended to other boards on the S-100 Bus.

1. Connect U41 pin 1 to U11 pin 11, Figure No. 1.

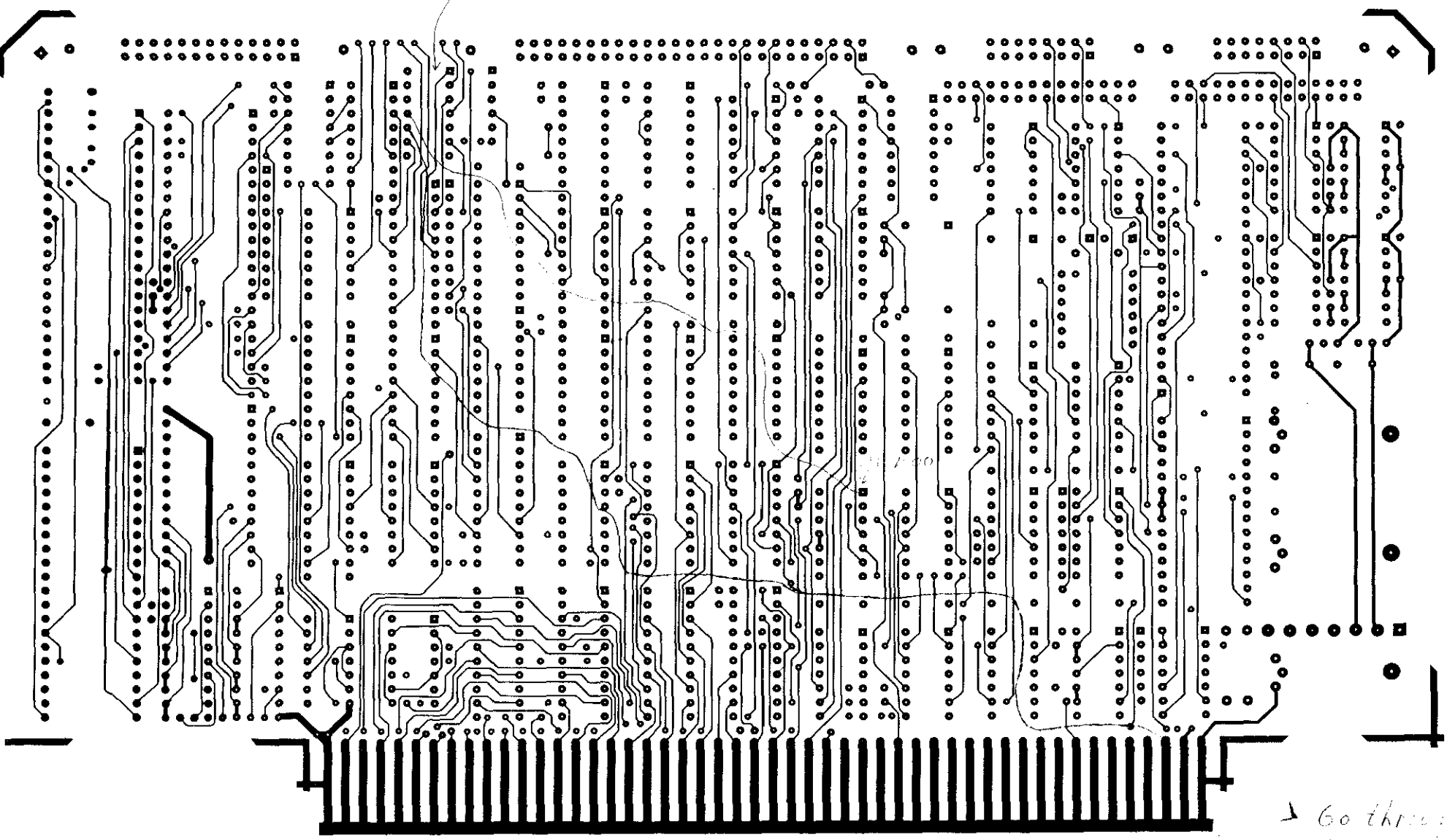
2. Connect U11 pin 10 to S-100 pin 4, Figure No. 1.

ECN No. 002

Extending the Interrupt Structure

Figure 1 of 2

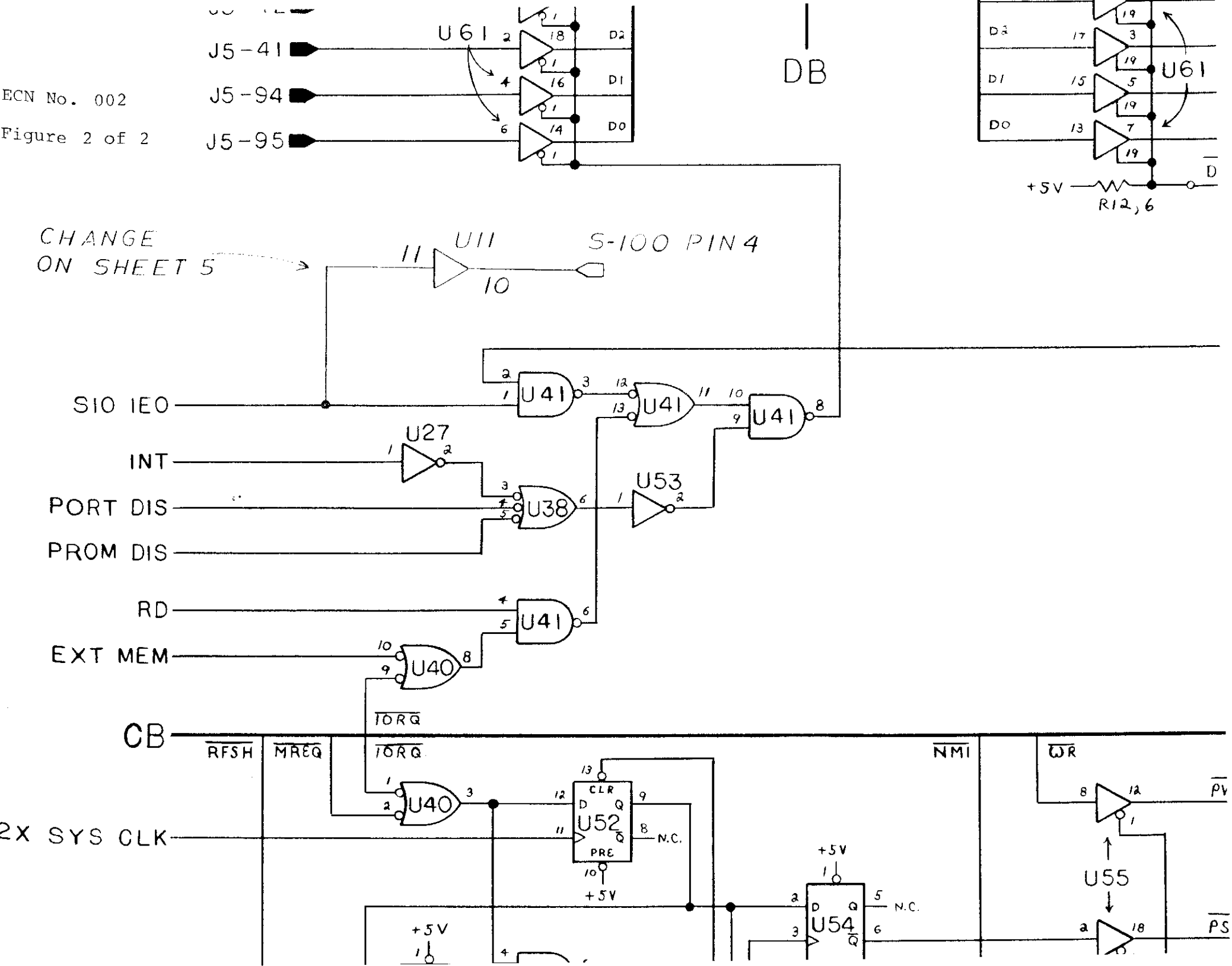
Solder Side



1 Go through this and ADD ATTACH to S-100 - Pin 4

ECN No. 002

Figure 2 of 2



#003

ENGINEERING CHANGE NOTICE

Subject: 19.2K Baud Option.

Reason for change: This change will allow the SDS-SBC-100 board to run the serial channels at 19.2K baud.

1. Insert 1.8432 mhz. crystal oscillator at location U18.
2. Cut W8 pins 2 and 3 free.
3. Connect W5 pin 3 to W8 pin 2.

The time constant for the CTC is as follows:

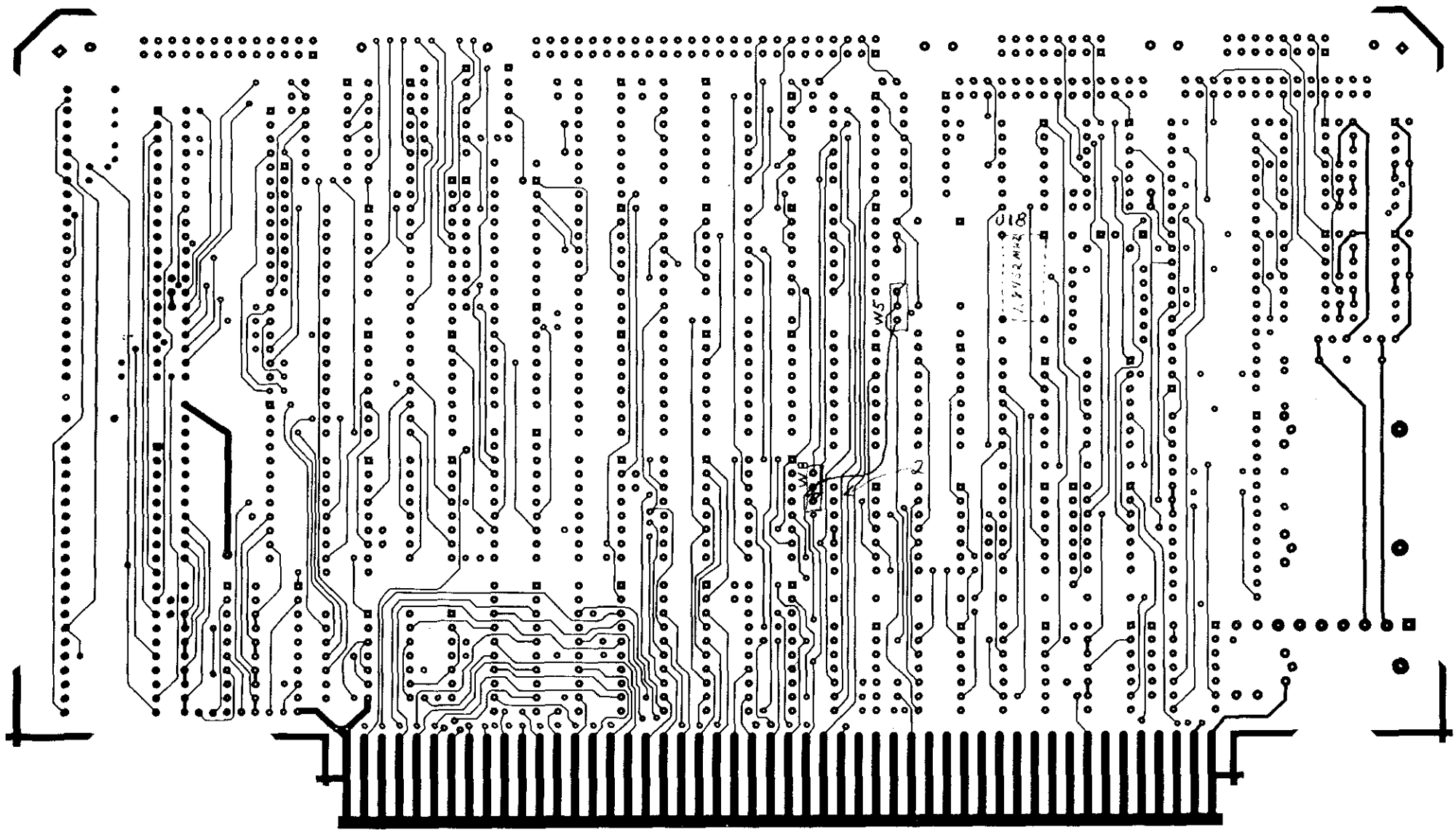
19.2K	6
9600	12D
4800	24D
etc.	

ECN No. 003

19.2K Baud Option

Figure 1 of 1

Solder Side



#004

ENGINEERING CHANGE NOTICE

Subject: ARDY on PIO inverted.

Reason for change: This change allows the ARDY from PIO Port A to be inverted so that it can be used directly as a Centronics Strobe Line.

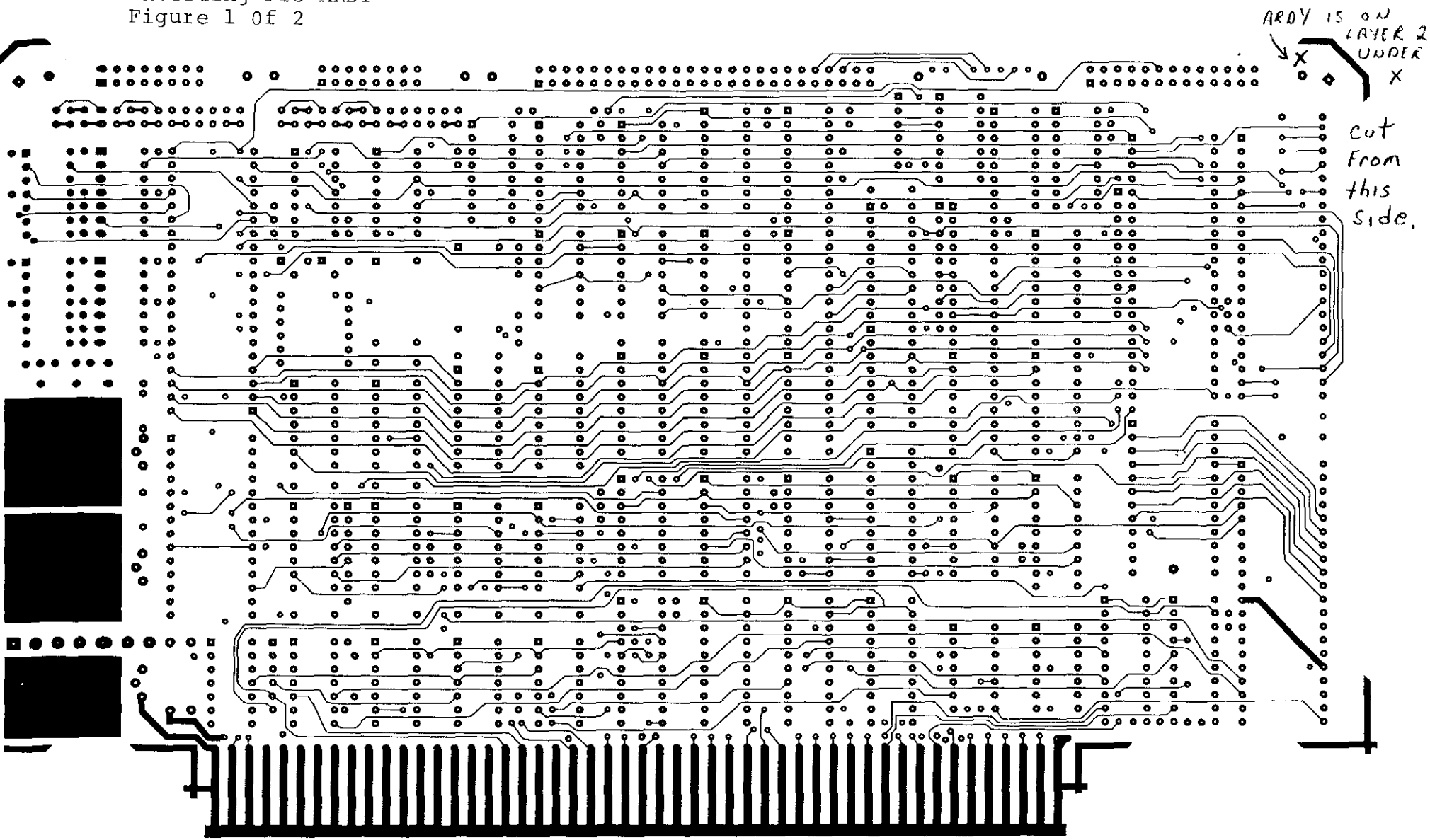
1. Cut PIO ARDY (pin 18) tree from H4 pin 22. This is an inner layer cut, which is done from the component side of the board as shown in Figure No. 1.

2. Connect U26 pin 11 to PIO ARDY. The ARDY feed through is directly under PIO pin 21, Figure 2.

3. Connect U26 pin 10 to H4 pin 22, Figure 2.

REDUCE 50%

ECN No. 004
Inverting PIO ARDY
Figure 1 0f 2

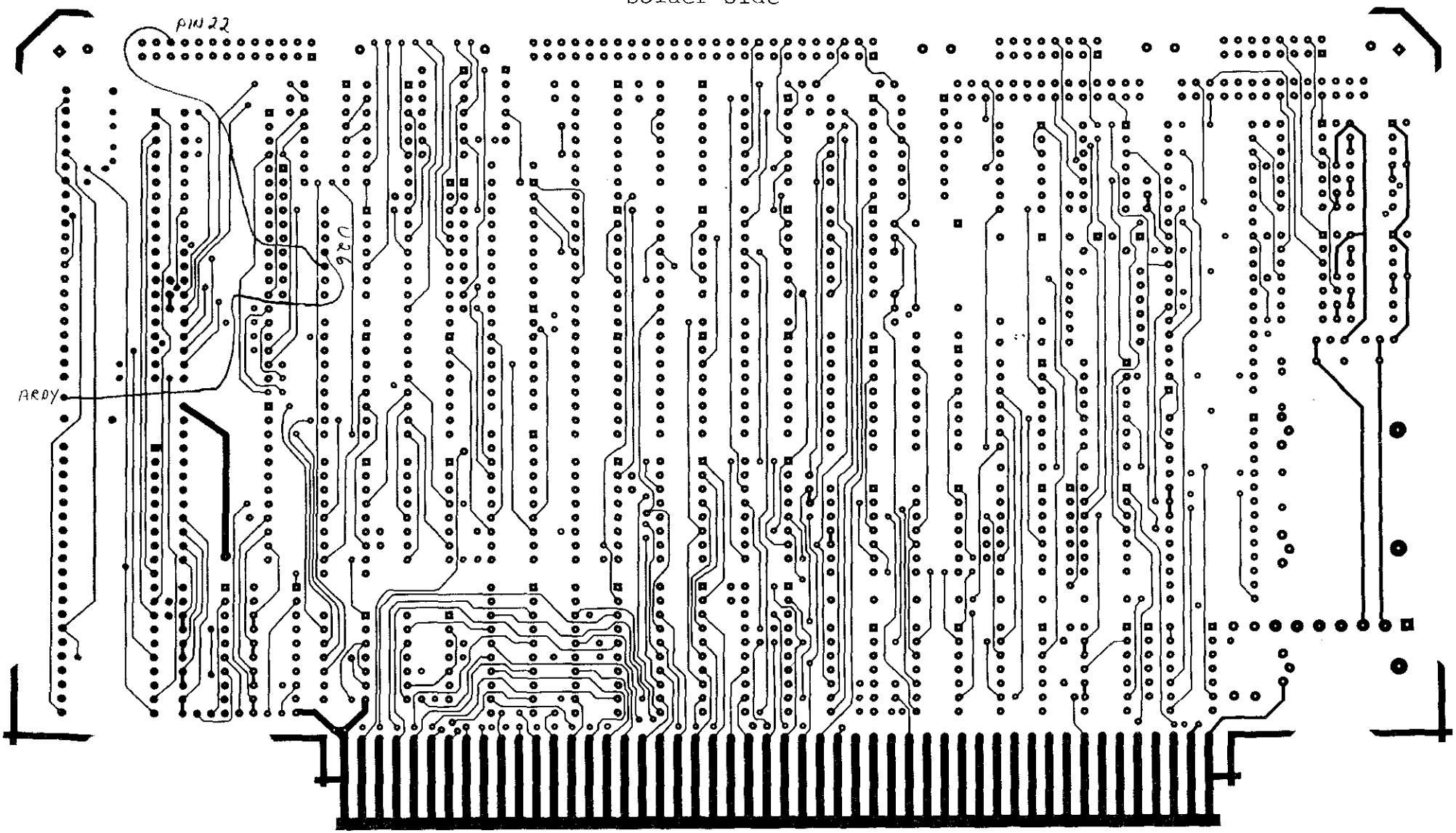


LAYER 1

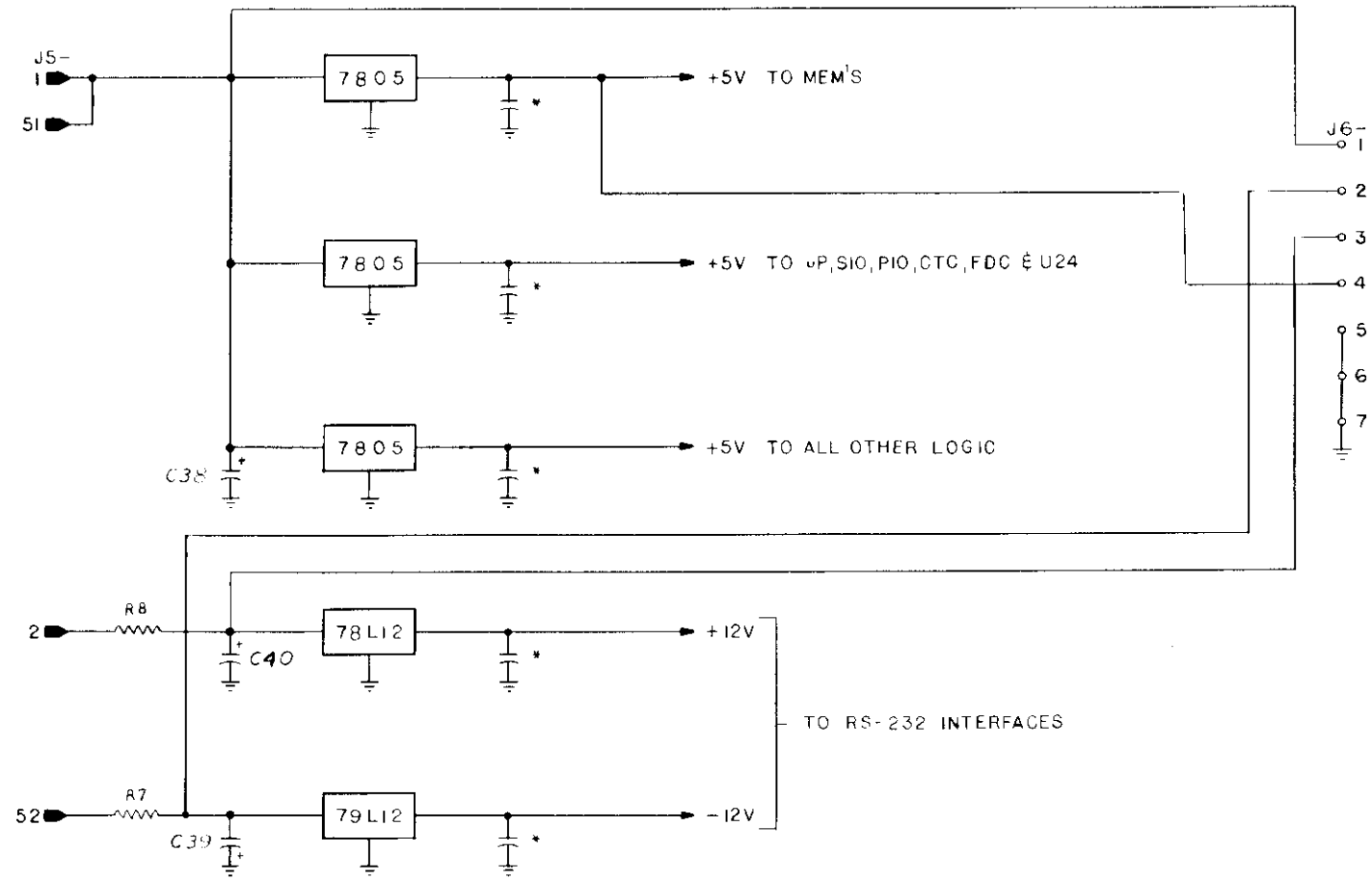
COMP SIDE

ECN No. 004
Inverting PIO ARDY
Figure 2 of 2

Solder Side



REVISIONS					
LTR	DESCRIPTION	DATE	AUTH	DR	CK



* BY-PASS CAPS SPREAD THROUGHOUT BOARD

DESIGN	DATE	SDS MASTER I - SBC-100
DRAWN JMF		
APPROVED SAB		TITLE: POWER SUPPLY
CHECKED		
MADE FROM		
REMARKS		DRAWING NUMBER — REV: A
		SCALE — RELEASED EM NO — SHEET — OF

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		—	A, EN 1057 PROD. REL; B, EN 1404 R/R; B1, EN 1689; C, EN 1824; D, ECN 2042A R/R; E, ECN 2094A R/R	—	—
		F	ECN 2168 R/R	5-27-82	R. W.

DEC 16 1982

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.		MICROPOLIS™		
	DR BY	T. Burton 5/27/82			
MATERIAL	CHK BY	B. Weisberg 5/27/82	MICRODISK UNPACKING & INSTALLATION GUIDELINES		
FINISH	APPROVED BY		SIZE	CODE IDENT NO.	DWG NO.	REV
	R. Weisberg 5/27/82		A	RD	100315	F
DO NOT SCALE DRAWING			SCALE		SHEET 1 OF 12	

DIETERICH-POST CLEARPRINT 1825-10 FORM 7704

This document gives unpacking and damage inspection procedures, configuration verification instructions, mounting instructions, guidelines for connecting power and interface cables, and procedures for repacking the drive for shipment. These instructions MUST be followed to prevent damage to the drive.

CAUTION

The drive must not UNDER ANY CIRCUMSTANCES be subjected to mechanical shock in excess of 20 G's in any axis. Shock greater than this level can cause permanent damage. For further information, contact Micropolis Technical Support.

Unpacking the Drive

The MicroDisk drive is packaged so as to minimize the possibility of damage during shipping. Inside the shipping carton is an "inner wrapper" structure of foam blocks, which provides shock isolation for an inner package (consisting of a two-part carton with foam pads for further shock insulation, sealed in a polyethylene bag). Use the following procedure to unpack the drive, and save ALL packing material in case it is necessary to repack the drive for shipping.

a. Place the shipping carton on a clean, flat work surface.

b. Slit the sealing tape on the carton top, then open the top flaps.

c. Fold back the foam block on the top of the inner wrapper.

CAUTION

Use extreme care when handling the inner package; the drive (inside it) is subject to damage if dropped.

d. Carefully remove the inner package and place it on the work surface (observe the TOP UP marking).

e. Remove the polyethylene bag from the inner package.

f. Remove the top portion of the carton.

CAUTION

The drive should be left in the lower carton until it is ready to be mounted. The disk media and heads are very shock sensitive, and without the carton's foam pads, even a short drop onto a hard work surface could cause a shock of over 20 G's, resulting in permanent damage.

g. Visually inspect the drive for damage. If shipping damage of any kind is evident, notify the carrier at once. Do not return a damaged drive until the shipping company inspector has reviewed the damage, since an insurance claim may be involved. Verify that the model number on the identification label is as ordered and agrees with the shipping paperwork. Bring any discrepancy to the attention of the supplier.

h. At this point a visual inspection may be performed to verify the proper circuit board configurations. If this is to be done, loosen the three captive retaining screws securing the printed circuit boards to the base casting. Swivel the board set up (the board set is mounted on pivots at the front of the drive). Being very careful to not strain any of the connectors or cables, pivot the boards over center until they come to rest against the pivot stops. See the next section for the actual configuration information. Then swivel the board set back down to their original position (against the frame), and tighten the three board-retaining screws.

NOTE

Some customers order drives and controllers shipped separately, and install the controllers on selected drives themselves. If this is the case, and if a controller is to be installed on this drive, it should be installed either at this point or later at system-integration time (procedure is included with the controller).

Before applying power for an operational receiving inspection, the shipping latch must be unlocked. To do this, replace the top portion of the inner carton on the drive, turn the drive over, and rest it (upside down) on the top portion of the carton. Remove the lower portion of the carton, and rotate the slotted head of the shipping latch (see Figure 1) to the UNLOCK position. Replace the lower carton, turn the drive back over, and remove the upper carton. After testing is completed, repeat this procedure to set the shipping latch to the LOCK position to prevent head and media damage.

i. Before mounting the drive, it should always be transported in the lower portion of the inner carton. When it is removed for mounting, the drive must be handled very carefully to ensure that it is not subjected to mechanical shock.

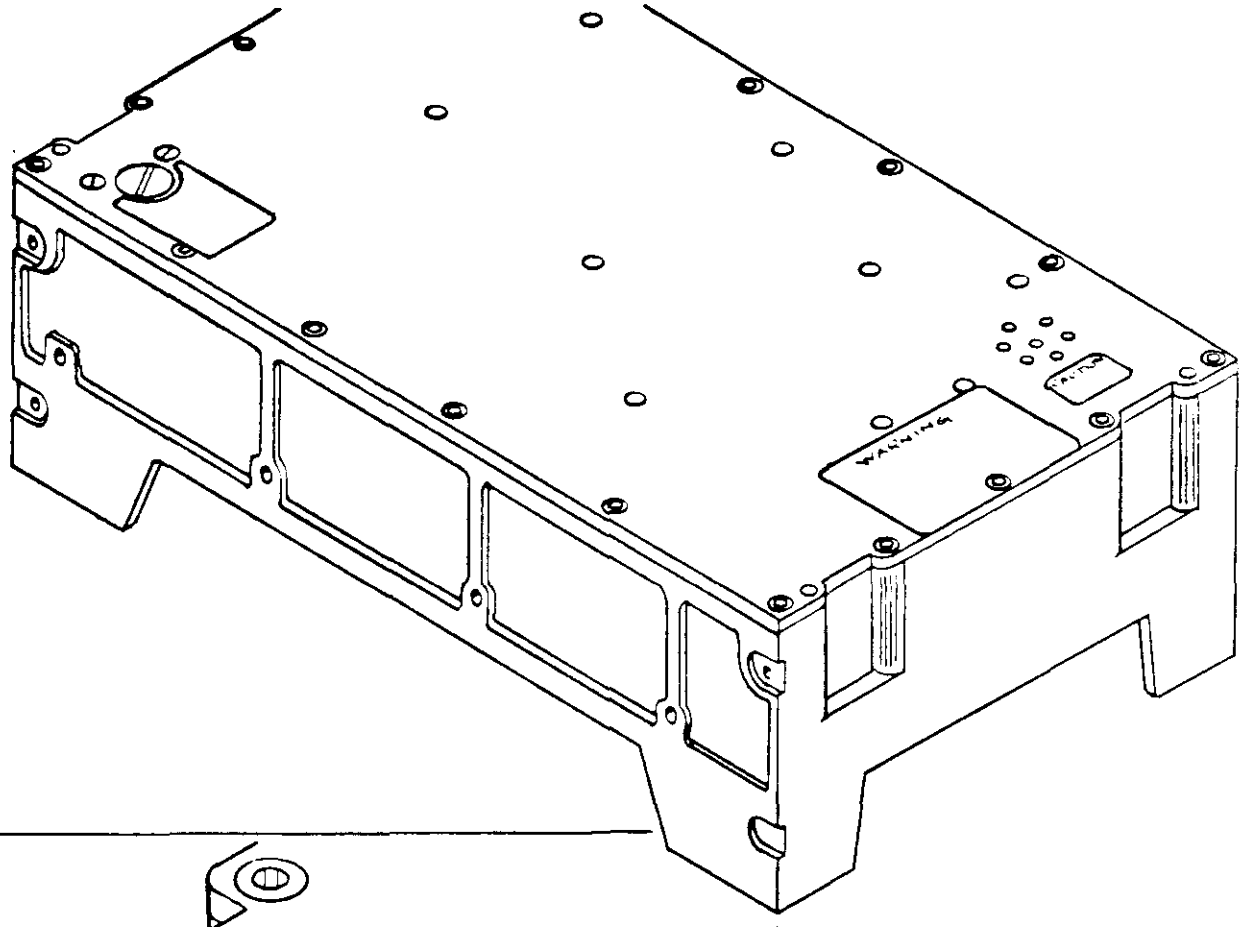
CAUTION

When removing the drive from the lower carton, hold it by the sides or ends of the base casting. Do NOT pull on the circuit boards.

j. Prior to utilization, uncouple the shipping latch by rotating the slotted head to the UNLOCK position (see figure 1). Do not uncouple the shipping latch until the drive is ready to mount. Head and media damage may result.

k. Save ALL shipping material and the cartons.

APPLICATION	REVISIONS



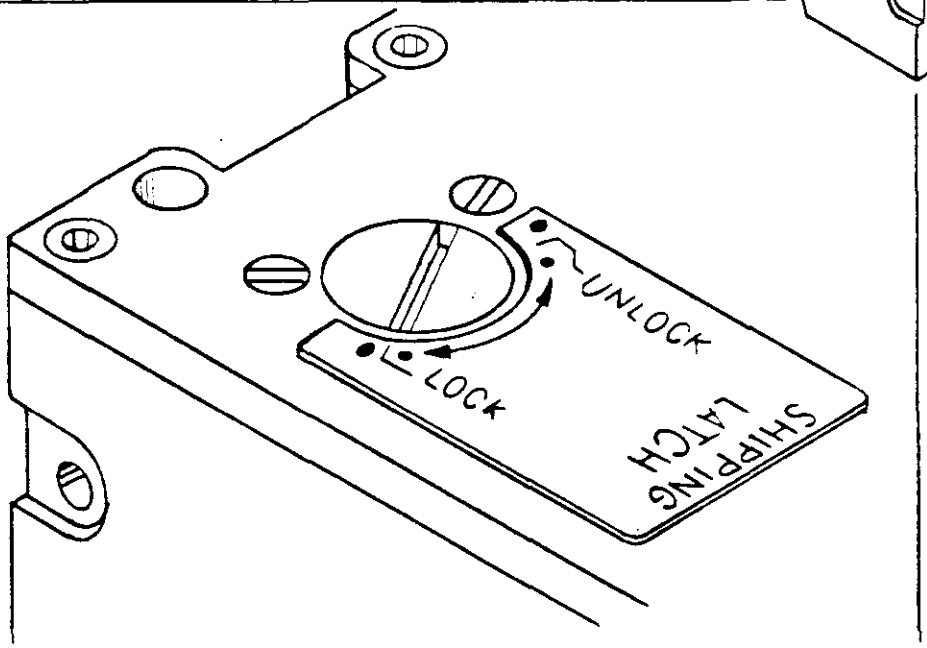


Figure 1. Shipping Latch

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	REV
A	RD	100315	F
SCALE		SHEET 4 OF 12	

FORM 7706A

Configuration Verification

Verify the correct configuration of the drive unit's Device Electronics Board (and Controller Board, if a 122X Subsystem), by checking the board against the appropriate configuration table (make sure the part number and revision letter agree). The figures that follow will aid in locating the specified components.

Device Electronics Board P/N 100280 Configurations

Part No. 100280-XX-X XX-A-TVSRI-XX
Option Codes (see below)

Option	Option Characteristic	Option Code	Description (* see below)	Option Methodology
A	Drive Address			Jumper 680-0202-1 at: W3 / W4 / W5 / W6
		0	Unit 0 *	X
		1	Unit 1	X
		2	Unit 2	X
		3	Unit 3	X
T	Interface Termination	1	Used *	RP1: P/N 115-0001-4, SIP1: P/N 116-0003-8, and SIP2, P/N 116-0001-2 installed.
		2	Not Used	RP1, SIP1, and SIP2 omitted.
V	Interface Terminator Voltage			Jumper 680-0202-1 at: W2 / W1
		1	Local *	X
		2	Remote	X
S	Sector/ Address Mark			Jumper 680-0202-1 at: W10 / W11
		1	Sector Pulse *	X
		2	Add. Mark Found	X (future NRZ Option)
R	Remote Start/Stop			Jumper 680-0202-1 at: W12 / W13
		1	Disabled *	X
		2	Enabled	X
I	Sector Pulse at Index Time	1	Generate *	Jumper 680-0202-1 at W16
		2	Omit	W16 omitted.
XX	Number of Sectors/ Revolution	0-98	Program Sector Pulse Generator for Desired No. of Sectors XX.	Sector Program Plug Assy 100411-XX (specified when ordered), factory installed in JX3.

* Asterisk shows the "normal" (i.e., unless-otherwise-specified) configuration. If the unit is daisy-chained with other drives, remove the interface terminators except on the last drive and configure each drive to a different drive address.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	REV
A	RD	100315	F

SCALE | SHEET 5 OF 12

APPLICATION	REVISIONS

Device Electronics Board "B" P/N 100482 Configurations

Part No. 100482-XX-X XX-A-TVIC-XX

Option Codes (see below)

Option	Option Characteristic	Option Code	Description (* see below)	Option Methodology
A	Drive Address			Jumper 680-0202-1 at: W3 W4 W5 W6
		0	Unit 0 *	X
		1	Unit 1	X
		2	Unit 2	X
		3	Unit 3	X
T	Interface Termination	1	Used *	RP1: P/N 115-0001-4, SIP1: P/N 116-0003-8, and SIP2, P/N 116-0001-2 installed.
		2	Not Used	RP1, SIP1, and SIP2 omitted.
V	Interface Terminator Voltage			Jumper 680-0202-1 at: W2 W1
		1	Local *	X
		2	Remote	X
I	Sector Pulse at Index Time	1	Generate *	Jumper 680-0202-1 at W16
		2	Omit	W16 omitted.
C	Control Program Firmware	1	Standard Firmware per Spec. 100198.	Jumper 680-0202-1 at W9 and W17; no jumper at W14 or W15. PROM 800063-01 at U73.
XX	Number of Sectors/ Revolution	0-98	Program Sector Pulse Generator for Desired No. of Sectors XX.	Sector Program Plug Assy 100411-XX (specified when ordered), factory installed in JX3.

* Asterisk shows the "normal" (i.e., unless-otherwise-specified) configuration. If the unit is daisy-chained with other drives, remove the interface terminators except on the last drive and configure each drive to a different drive address.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	REV
A	RD	100315	F
SCALE		SHEET 6 OF 12	

Controller Board Configurations

Part No. 100295-51-8-XX-A-TC-FF

- XX: Option Codes (see below)
- A: Board Revision Identifier (see below)

Option	Option Characteristic	Option Code	Description (* see below)	Option Methodology
A	Controller Address	0	Controller 0 *	Jumper 680-0202-1 at: W1 X, W2 X
		1	Controller 1	Jumper 680-0202-1 at: W2 X
				(and always at W9 for Rev. D or E Boards only)
T	Host Interface Termination	1	Used *	RN1: P/N 115-0001-4 installed.
		2	Not Used	RN1 omitted.
C	Control Program Firmware	1	Standard Firmware per Spec. 100292.	For Revision C Boards: A3: P/N 800042-01-2, and A4: P/N 800042-02-0 both installed. For Revision D or E Boards: A3 omitted; A4: P/N 800060-01-4
FF	Format		Configured for Desired Sector Format	Specified when ordered. See Format Selection table below.

* Asterisk shows the "normal" (i.e., unless-otherwise-specified) configuration. If the Controller is daisy-chained with another Controller, remove the host interface termination except on the last drive and configure each Controller to a different Controller address.

Controller Format Selection Table

Format	Sectors	Length	Jumper 680-0202-1 W3	W4	W5	W6	W7	W8	Format PROM D15	RAM B5 and C5
00	42	256						X	800040-01-6	Not Used
01	40	268				X		X	800040-01-6	Not Used
02	24	512			X			X	800040-01-6	Not Used
03	--	---								
04	66	128		X				X	800043-01-1	Not Used
05	24	514		X		X		X	800043-01-1	Not Used
06	12	1024		X	X		X		800043-01-1	421-0001-6

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	REV
A	RD	100315	F

SCALE | SHEET 7 OF 12

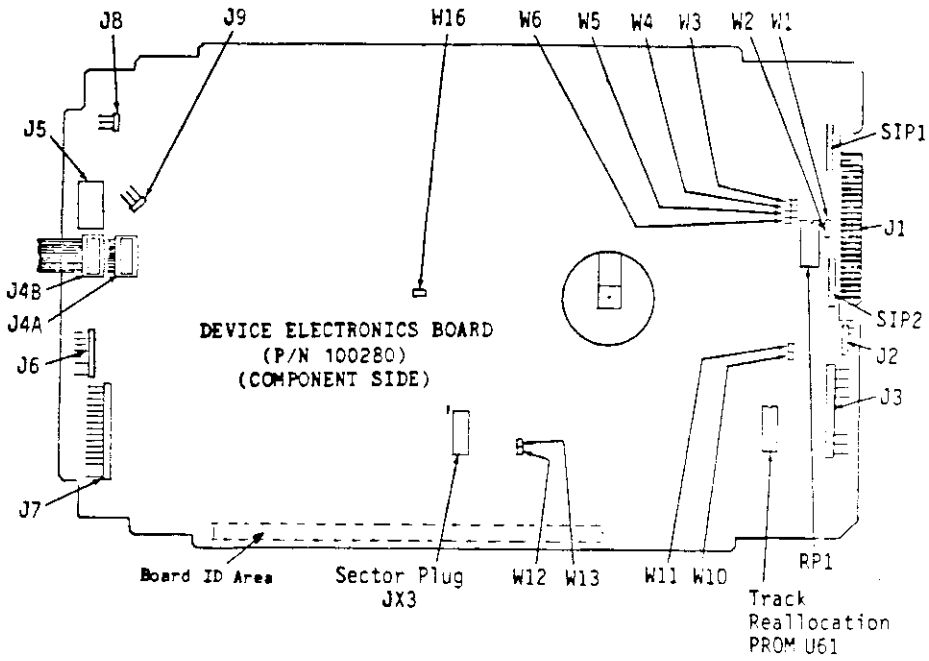


Figure 2. Device Electronics Board (P/N 100280) Configuration Components

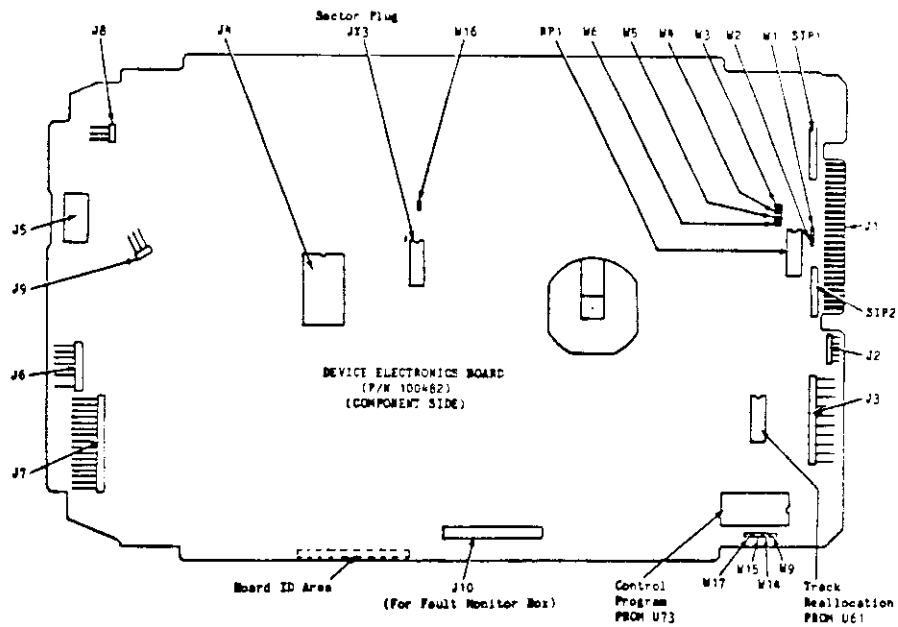


Figure 3. Device Electronics "B" Board (P/N 100482) Configuration Components

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SIZE	CODE IDENT NO.	DWG NO.	REV
A	RD	100315	F
SCALE		SHEET 8 OF 12	

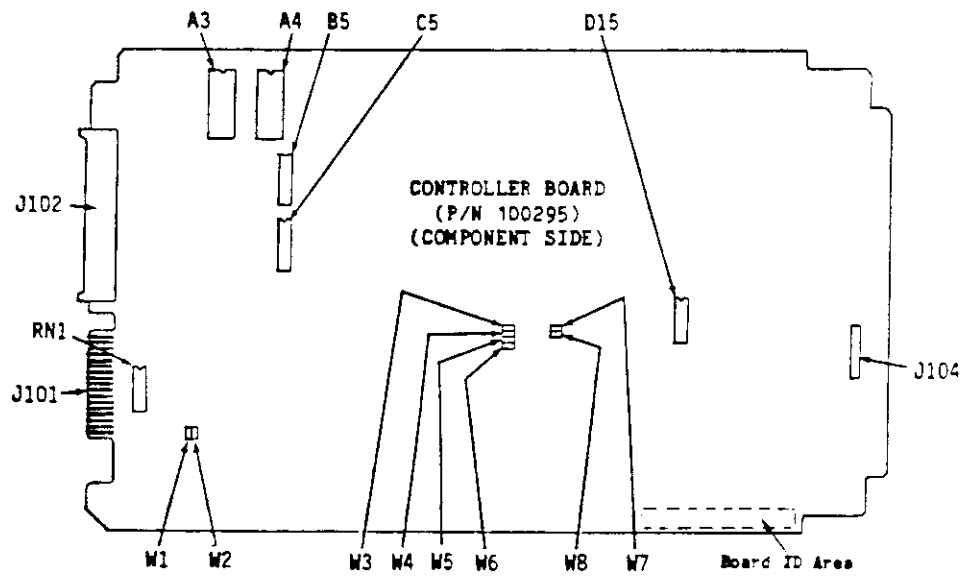

Figure 4. Controller Board Configuration Components

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SIZE A	CODE IDENT NO. RD	DWG NO. 100315	REV F
SCALE		SHEET 9 OF 12	

Mounting Instructions

The following guidelines should be adhered to when planning the installation:

a. The drive may be mounted in any orientation except with the circuit boards down. This mounting would result in inadequate cooling.

b. The breather holes on the base plate must not be obstructed. The breather holes permit pressure equalization inside and outside the sealed clean area, therefore the air flow is very small. It is sufficient to ensure that any adjacent flat surface is at least 0.050 inches from the breather holes.

c. The drive can be mounted using either the eight mounting holes along the long sides of the casting or the four 10-32 threaded holes in the bottom. Eight 8-32 thread-rolling screws are provided for use in the side holes. Screws should be torqued to 30 plus or minus 5 inch-pounds. If the four holes in the bottom are to be used, care must be taken to prevent any stress or distortion from being imparted to the drive. Careful consideration must be given to the mounting method and selection of shock isolators to suit each individual application. Micropolis recommends the use of shock isolators in all applications. Refer to the drive specification for shock isolators suitable for an office environment.

d. Free air circulation must not be blocked from the cutaway areas on all four sides of the drive. Ambient air temperature should be in the range 50° to 104° F (10° - 40° C). If the unit is installed in a small enclosure, a fan may be required to maintain the ambient air below 104° F.

e. The drive will perform satisfactorily with natural air convection cooling when mounted as follows:

The drive can be mounted with the base or either long side down. Mounting brackets may touch or cover the frame below the circuit board area (see figure 5a). Under no circumstances should the cutaway areas in the frame be obstructed. If the drive is mounted base down, a 3/4" to 1" air space must be provided on each side of the circuit board area (see figure 5b), to ensure proper circuit board cooling. If the drive is mounted with either long side down, the remaining three sides must be open to air flow. If the drive is mounted in an enclosure with mounting brackets on both long sides, at least one side must be open or grated for air flow (see figure 5c).

CAUTION

The end of the drive with the hinge blocks for the printed circuit boards is a critical heat dissipation area. Do not restrict air flow in any way.

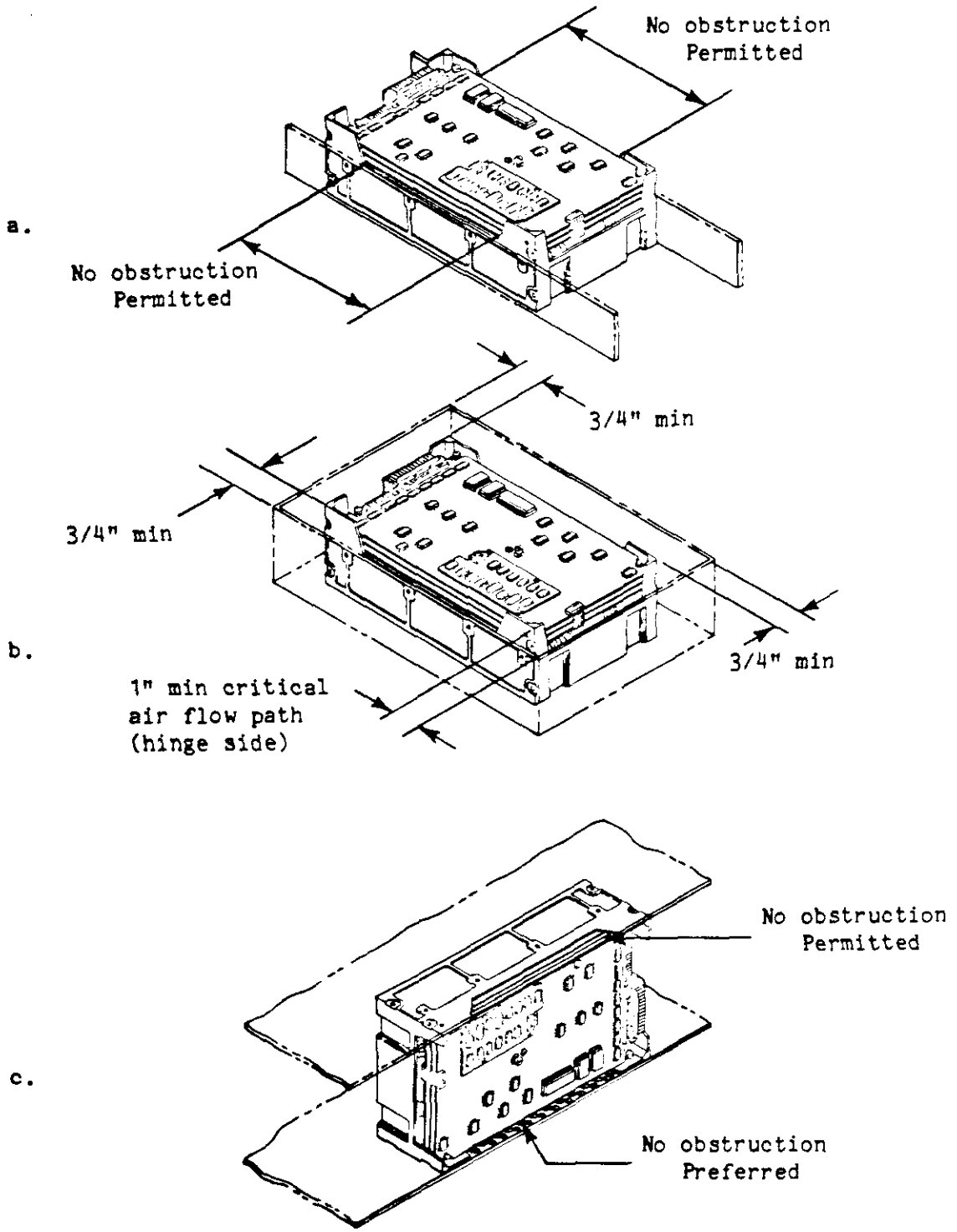

Figure 5. Drive Mounting for Natural Convection

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SIZE	CODE IDENT NO.	DWG NO.	REV
A	RD	100315	F
SCALE		SHEET 11 OF 12	

Connecting Power and Interface Cables

Connect the dc power connector to J3 on the Device Electronics Board (pin 1 toward 50-pin connector J1).

For a Model 120X Drive Unit (without controller), connect the interface cable to 50-pin connector J1 on the Device Electronics Board (pin 1 toward the edge of the board).

For a Model 122X MicroDisk Subsystem (with Micropolis Controller), connect the interface cable to J101 on the Controller Board (pin 2 on top, toward the Device Electronics/Controller 50-pin interconnect cable).

Repacking the Drive for Shipment

If it is necessary to repack the drive for shipment, the following procedure must be used. Contact Micropolis Customer Service to obtain a Return Goods Authorization (RGA) prior to returning any drive.

CAUTION

Do not attempt to ship the drive except in the original packing. If any of the packing material is lost or otherwise unavailable, contact Micropolis Customer Service for new material.

a. Engage the shipping latch to the LOCK position (see figure 1).

b. Put the drive into the (lower) inner carton, and place the upper inner carton (which is marked "TOP UP") over the circuit boards of the drive. The cartons are a snug-enough fit that they will stay in place by themselves.

c. Place the drive (in its pair of cartons) into the polyethylene bag, and seal with tape.

d. Put the sealed package (from step c) into the inner wrapper structure within the shipping carton. Fold the top flap of the inner wrapper down over the package, close the shipping carton flaps and tape securely.