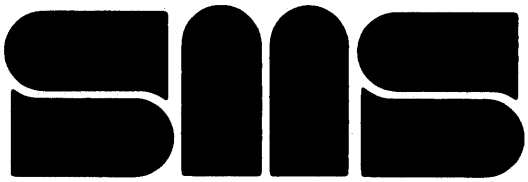

OMTI5510
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SECTION 1

INTRODUCTION

1.1 PURPOSE

This manual provides the information needed to install, configure, program, operate, and maintain the OMTI5510 Data Controller. The manual is a reference source for OEM engineers, system integrators, and service and maintenance technicians.

1.2 GENERAL

The OMTI5510 is an intelligent Winchester Disk controller for IBM PC/XT and compatible systems contained on a single PCB that plugs into the system motherboard. The Winchester Disk Drives can be up to two 3-1/2 inch or 5-1/4 inch fixed, removable, or fixed/removable ST506/412 compatible drives. Each drive can have up to 16 heads and 1,024 cylinders.

The 5510 Data Controller uses SMS's advanced VLSI chips to provide state-of-the-art data management. A single chip data separator circuit ensures data integrity with Winchester disk drives. Efficient error detection/correction is accomplished by a powerful "computer generated" 32-bit error correction code polynomial.

The OMTI5510 Controller supports a Basic I/O System (BIOS) software driver to control the Winchester disk drive. Ths BIOS is stored in an 64K EPROM module located on the controller's PCB.

1.3 FUNCTIONAL ORGANIZATION

Figure 1-1 is the functional block diagram for the OMTI5510 Data Controller.

1.3.1 System Interface

The System Interface is accomplished by a special purpose CMOS VLSI component (OMTI5090) that provides an interface between the Winchester disk controller and the system bus. The chip provides a buffered data path, address decoding for access to

4 I/O ports, and bus control for interrupts and DMA transfers.

1.3.2 Microprocessor

The controller board contains an 8MHz ROMless Zilog Z8 Microcomputer. The Z8 provides a powerful instruction set, simplified system expansion off chip, and flexible serial and parallel I/O capabilities. It contains a 16-bit program counter and a separate 16-bit stack pointer. The Z8 has 128 internal registers. Sixty-four registers are used for drive status and drive parameters for up to two LUNs. The remaining registers are used for system status and command parameters.

1.3.3 OMTI Sequencer

Disk data functions are handled by the OMTI5050 Data Sequencer chip. The Sequencer manages the flow of block-level information between the Winchester disk and the RAM Buffer. The OMTI5050 provides the bit-serial data management, format control, error detection, and serialization/ deserialization functions for interfacing the controller and Winchester disk drives.

1.3.4 OMTI DATA SEPERATOR

These functions are handled by the OMTI5070 VCO/Encode/Decode chip. The 5070 provides the necessary functions to convert between MFM serial data and NRZ data and clock translations. The chip contains an internal VCO, phase-locked loop, encoder/decoder logic, Address Mark generation and detection, and all the circuitry required for write precompensation.

1.3.5 OMTI Buffer Controller

Data control functions are handled by the OMTI5060 Four Channel Buffer Controller. The OMTI5060 manages the flow of block-level information between buffer memory, host processor and Winchester disk drives.

1.3.6 RAM Buffer

The controller's 2K static RAM data buffer is used for temporary storage of blocks of data during data transfers. This buffer does not store controller firmware constants and variables.

EXAMPLE OF BUFFER USE:

The following case is a multi-block READ command from the disk:

- the first block, specified as the starting block address in the command is read from the disk and written into the buffer, (controlled

by the "Sequencer chip" channel of the 5060 chip).
- when the ECC is calculated, the data block is available for transfer to the host bus;
- The data block is then transferred asynchronously at the host memory speed (Handshake Timing).
- the next block on the disk is stored in the buffer (at the address, in the buffer, below the previous block), as soon as it is read, independently of the access from the host. Reading of data from the Disk and sending data to the Host are independent, and take place at the same time.
- blocks are stored below each other in the buffer, until the maximum address is reached; then the channel wraps around to the first address in the buffer (assuming that the first block has already been transferred to the Host).
- if the host is too slow to empty all data blocks stored in the buffer, from the disk, and another block is ready to be stored into the buffer, with no space available, an overrun situation occurs. In this case, the controller will stop reading from the disk, wait one or more revolutions, until the buffer is completely empty. This will occur only if the host transfer rate is much slower than the 5 Mbits/sec rate at which data is stored into the buffer, from the disk.

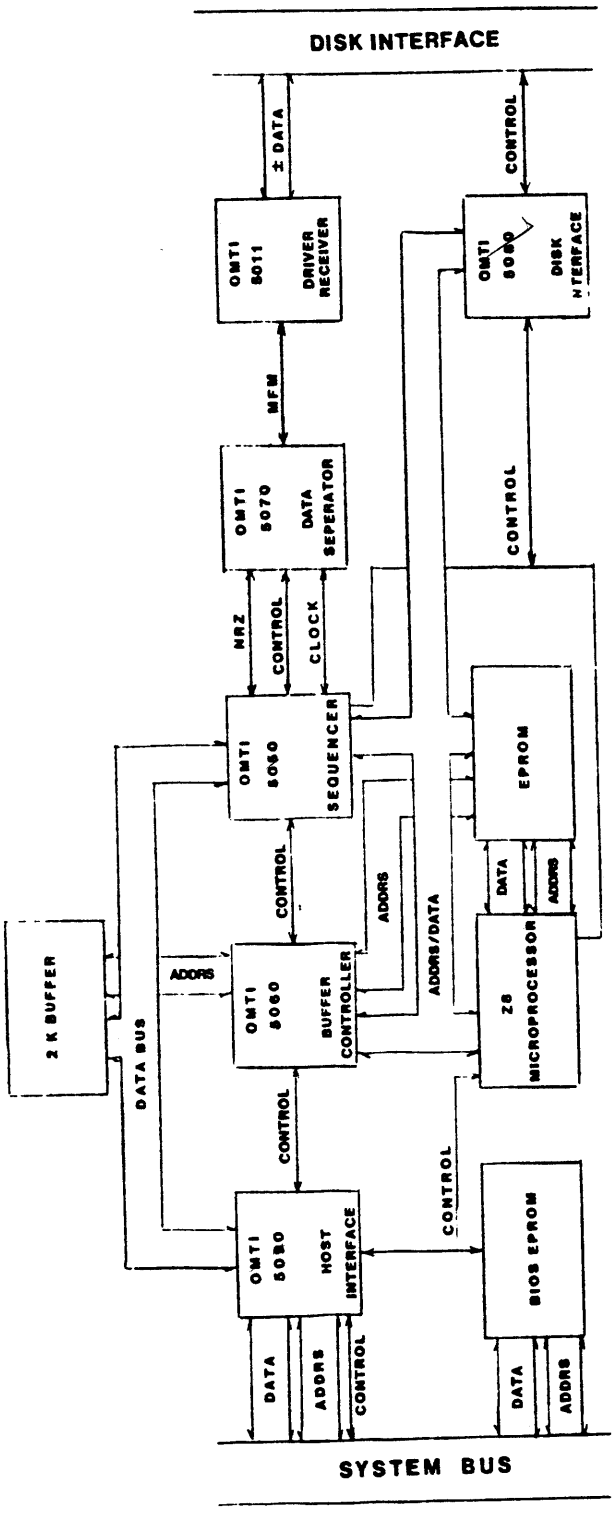

Figure 1-1. Functional Block Diagram, OMTI5510 Controllers

1.4 SPECIFICATIONS

Table 1-1 lists the specifications for the OMTI5510 Data Controller. Included are environmental and power requirements, as well as dimensional characteristics.

Table 1-1 OMTI5510 Specifications.

Physical Specifications

	With Bracket	Without Bracket
Width	5.0 inches (12.7 cm)	4.2 inches (10.7 cm)
Length	6.3 inches (16.0 cm)	5.5 inches (14.0 cm)
Height	1.0 inches (2.5 cm)	0.4 inches (1.0 cm)

Environmental Specifications

	Operating	Storage
Temperature	0 to 50C	-40 to 75C
Relative Humidity	10% to 95%	10% to 95%
Max. Wet Bulb	30C	Noncondensing
Altitude	0-10000 ft	0-15000 ft

Power Requirements

The OMTI5510 requires +5 V (+/-5%) power only. The maximum ripple and noise (P/P) is 100 mV. The maximum current drawn is 0.5 Amp.

SECTION 2

STANDARD FEATURES

2.1 GENERAL

This section contains a list and a brief description of the standard features for the OMTI5510 Data Controller. Table 2-1 covers general standard features, Table 2-2 covers Winchester Disk specific standard features. Section 3 through Section 7 of this manual contain more detailed information.

Table 2-1 OMTI5510 Standard Features

FEATURE	DESCRIPTION
COMPACT BOARD	The 5510 Controller is a single 4.2 x 5.5 inch printed circuit board equiped with Surface Mounted Technology devices. The controller plugs directly into IBM PC/XT or compatible system buses.
ERROR RETRY	Error retry on SEEK or READ errors is performed automatically unless disabled.
BUFFER TYPE	Ring Buffer (Wraps Around) with 3 Independent Ports.
BUFFER SIZE	2K Bytes.
POWER	0.5 Amps Maximum, Requires 5 Volts only.
LIMITED PART COUNT	Only eleven IC's, 6 of which are SMS Special Purpose Proprietary VLSI Chips.

Table 2-2 Winchester Disk Specific Features

FEATURE	DESCRIPTION
TRANSFER RATE	5 M bits/Sec
INTERFACE	ST506/412 Compatible
SELECTABLE DRIVE TYPES	Various drive types can be selected by jumper allocation.
MULTIPLE DRIVE TYPES SUPPORTED	The 5510 Controller supports any combination of Fixed, Removable or Fixed/Removable drives.
CONSECUTIVE SECTOR TRANSFER	Capable of transfering a full Track In a Single Disk Revolution.
MULTIPLE SECTOR BUFFER	A 2 KByte buffer can contain up to four 512 byte sectors.
PROGRAMMABLE DISK PARAMETERS	The parameters for the Winchester Disks can be passed to the controller with the ASSIGN DISK PARAMETERS command.
SECTOR METHOD	Hard or Soft Sectored type of drives.
NUMBER OF HEADS	Up To 16 Heads Supported.
NUMBER OF CYLINDERS	Up To 1024 Cylinders Supported.
SECTOR INTERLEAVING	One-to-One or Programmable.
TRACK FORMAT	Compatible with the OMTI5000 and OMTI20 Series.
BLOCK OR SECTOR SIZE	Jumper Selectable, 128, 256, 512, or 1024 Bytes per Sector.
SECTORS PER TRACK	Number of sectors per track corresponds to the specified block size (55,32,17,OR 9).
IMPLIED SEEK	Supported, with all Data Transfer Commands.
AUTOMATIC HEAD OR CYLINDER SWITCHING	Supported.

MULTI-BLOCK TRANSFER	Up To 256 Blocks per command (with any block size listed above).
AUTOMATIC READ RETRIES	User Selectable.
AUTOMATIC HANDLING OF MEDIA DEFECTS	Supported at Track Level with Alternate Track Assignment.
OVERLAPPED SEEK	Allows multiple drives to be positioned simultaneously. While a seek is being performed on one drive, other operations can be performed on the other LUN.
ECC	32 bit Error Correction Code for Header and Data Fields. Polynomial - "Computer Generated" Code "x}31{+x}24{+x}23{+x}20{+ x}17{+x}16{+x}13{+x}7{+x}0{" Correction Capability - 5 Bits Detection Capability - 19 Bits
STEP RATE	Programmable and accepts a Minimum of 25 us.
COPY COMMAND	Between Disks (of any type). Uses the Internal Controller Buffer.

SECTION 3

3.1 UNPACKING AND INSPECTION

Upon receipt of your OMTI5510 Data Controller, inspect the packaging for evidence of damage during transit. Open the package and inspect the controller board for visible damage such as scratches, loose components, or broken connectors. If there is damage, immediately notify the carrier's agent and your OMTI Products Division customer service representative. Compare the items listed on your original Purchase Order to the actual contents of the package and the packing list. If discrepencies exist, notify your OMTI Products Division customer service representative.

Retain the shipping container and packing material for examination (if it has been damaged), or for reuse when returning the controller board to the factory.

3.2 SYSTEM CONFIGURATION

The OMTI5510 Data Controller is designed to plug directly into any unused location on the system motherboard. The Winchester disk(s) are connected to the controller by ribbon cables. If the Winchester drive(s) are external to the system enclosure, the cables should not exceed 20 feet (six meters), or the drive manufacturer's limit, whichever is less.

After your board is mounted, connect the cables to the disk drive. Refer to Figure 3-1 for the location of connectors on your board. Pin 1 on all connectors is specified by a square solder pad, visible on the soldered side of the board.

Typical OMTI5510 system configuration is presented in block diagram form in Figure 3-1

The connector's recommended part numbers are as follows:

J2 - AMP P/N 88373-3 (-34)
J3 and J4 - AMP P/N 86904-1 (-20)

3.3 BOARD PREPARATION

The appropriate board layout, connector locations, and jumper locations for the OMTI5510 Controller are illustrated in Figure 3-2. Use Table 3-1 to ensure that the factory installed jumpers are correctly in place.

The OMTI5510 has 16 jumpers which allow the controller to be easily integrated into different systems. Jumpers W1 through W8 specify parameters of the system-controller interface typically used by a BIOS. Jumpers W9 through W16 specify drive parameters to be used by the controller. Table 3-1 defines the jumpers in detail.

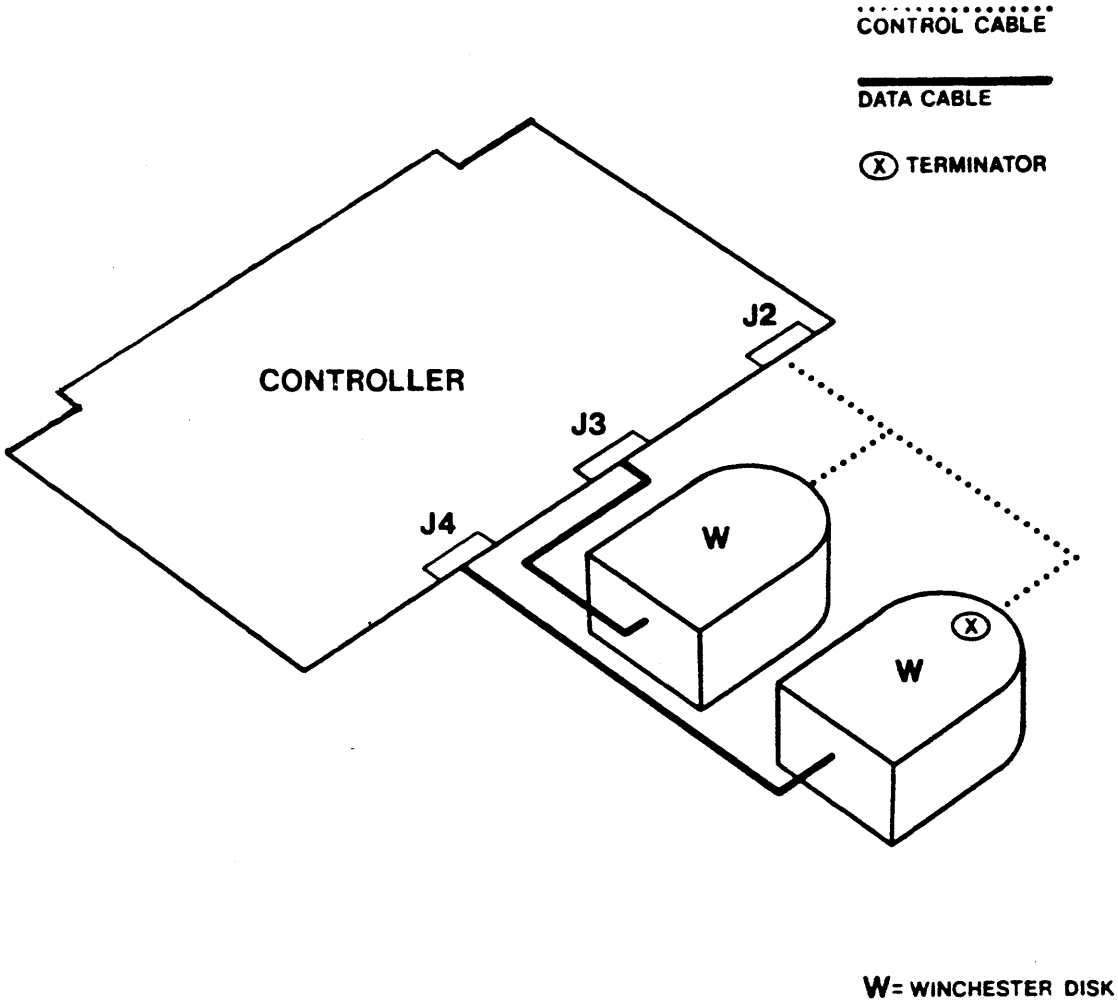

Figure 3-1. Model 5510 System Configuration

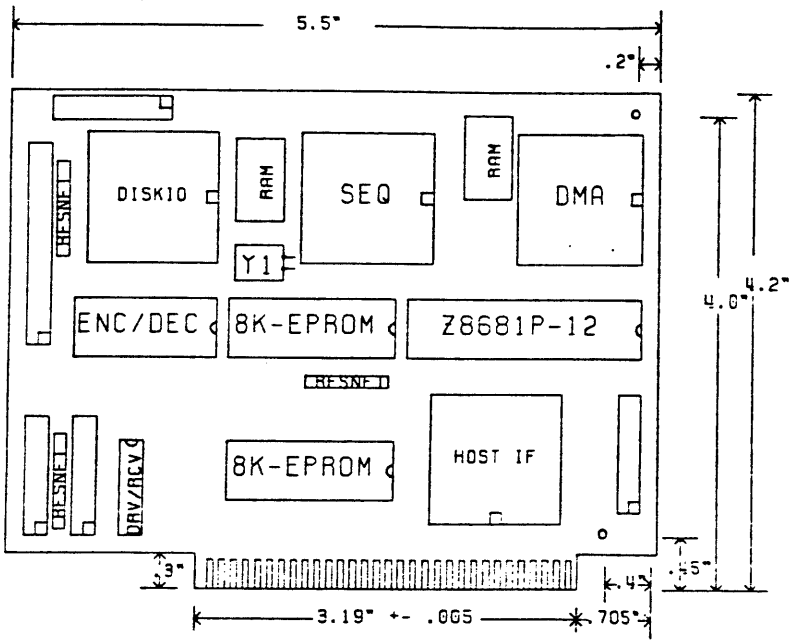

Figure 3-2. Model 5510 Board Layout

Table 3-1 Jumper Definitions

0 = No jumper installed
1 = Jumper installed
* = As shipped

W4	W3	W2	W1	Drive configuation jumpers
*0	0	0	0	Used by BIOS. (See Appendix A for details)

W6	W5	I/O Port Base Address
*0	0	320
0	1	324
1	0	328
1	1	32C

W7	BIOS EPROM Control
*0	Enable BIOS EPROM
1	Disable BIOS EPROM

W8	BIOS EPROM Base Address
*0	C8000
1	CA000

W10	W9	Bytes Per Sector
0	0	128
0	1	256
*1	0	512 (note: required for use with SMS/OMTI BIOS)
1	1	1024

W11	LUN 0 Sector Type
*0	Soft sectored
1	Hard sectored

W13	W12	LUN 0 Drive Type
*0	0	Fixed
0	1	Reserved
1	0	Fixed/Removable (Removable platter)
1	1	Removable

W14	LUN 1 Sector Type
*0	Soft sectored
1	Hard sectored

W16	W15	LUN 1 Drive Type
*0	0	Fixed
0	1	Reserved
1	0	Fixed/Removable (Fixed platter)
1	1	Removable

3.4 Connector and Pin Assignments

3.4.1 System Interface

The following table defines the signals on the system interface.

COMPONENT SIDE

Pin	Signal	Description
A1	-I/O Ch Ck	I/O or Mem failure
A2	+D7	Data Bit 7 (MSB)
A3	+D6	Data Bit 6
A4	+D5	Data Bit 5
A5	+D4	Data Bit 4
A6	+D3	Data Bit 3
A7	+D2	Data Bit 2
A8	+D1	Data Bit 1
A9	+D0	Data Bit 0
A10	+I/O CH RDY	I/O Channel Ready
A11	+AEN	DMA Channel on
A12	+A19	Address Bit 19
A13	+A18	Address Bit 18
A14	+A17	Address Bit 17
A15	+A16	Address Bit 16
A16	+A15	Address Bit 15
A17	+A14	Address Bit 14
A18	+A13	Address Bit 13
A19	+A12	Address Bit 12
A20	+A11	Address Bit 11
A21	+A10	Address Bit 10
A22	+A9	Address Bit 9
A23	+A8	Address Bit 8
A24	+A7	Address Bit 7
A25	+A6	Address Bit 6
A26	+A5	Address Bit 5
A27	+A4	Address Bit 4
A28	+A3	Address Bit 3
A29	+A2	Address Bit 2
A30	+A1	Address Bit 1
A31	+AQ	Address Bit 0

3.4.1 (Continued)

SOLDER SIDE

Pin	Signal	Description
B1	GND	Ground
B2	+Reset DRV	Positive I/O Reset
B3	+5V	+5 Volt Supply
B4	+IRQ2	Interrupt Request 2
B5	-5V	-5 Volt Supply
B6	+DRQ2	DMA Request 2
B7	-12V	-12 Volt Supply
B8	CRD SLCTD	Card Selected
B9	+12V	+12 Volt Supply
B10	GND	Ground
B11	-MEMW	Memory Write Strobe
B12	-MEMR	Memory Read Strobe
B13	-IOW	I/O Write Strobe
B14	-IOR	I/O Read Strobe 3
B15	-DACK3	DMA Acknowledge 1
B16	+DRQ3	DMA Request 1
B17	-DACK1	DMA Acknowledge 1
B18	+DRQ1	DMA Request 1
B19	-DACK0	DMA Ack 0 (Refresh)
B20	CLOCK	4.77 Mhz Sys. Clock
B21	+IRQ7	Interrupt Request 7
B22	+IRQ6	Interrupt Request 6
B23	+IRQ5	Interrupt Request 5
B24	+IRQ4	Interrupt Request 4
B25	+IRQ3	Interrupt Request 3
B26	-DACK2	DMA Acknowledge 2
B27	+T/C	DMA Terminal Count
B28	+ALE	Address Latch Enable
B29	+5V	+5 Volt Supply
B30	+OSC	14.31818 Mhz Clock
B31	GND	Ground

3.4.2 WINCHESTER DISK DRIVE INTERFACE

The following tables define the various Winchester Disk Drive's pin assignments.

WINCHESTER DISK CONTROL CABLE SIGNALS (CONNECTOR J2)

GROUND RETURN	SIGNAL PIN	SIGNAL NAME
1	2	HEAD SELECT 3/WSI/Chng Cart.
3	4	HEAD SELECT 2
5	6	WRITE GATE
7	8	SEEK COMPLETE
9	10	TRACK 000
11	12	WRITE FAULT
13	14	HEAD SELECT 0
15	16	RESERVED Sector Pulse
17	18	HEAD SELECT 1
19	20	INDEX
21	22	READY
23	24	STEP
25	26	DRIVE SELECT 1
27	28	DRIVE SELECT 2
29	30	DRIVE SELECT 3
31	32	DRIVE SELECT 4
33	34	DIRECTION SELECT

WINCHESTER DISK DATA CABLE SIGNALS (CONNECTORS J3,J4)

GROUND RETURN	SIGNAL PIN	SIGNAL NAME
2	1	DRIVE SELECTED
4	3	RESERVED
6	5	WRITE PROTECTED
8	7	RESERVED
10	9	CARTRIDGE CHANGED
12	11	GROUND
	13	+MFM WRITE DATA
	14	-MFM WRITE DATA
16	15	GROUND
	17	+MFM READ DATA
	18	-MFM READ DATA
20	19	GROUND

3.5 DEFAULT PARAMETERS FOR WINCHESTER DISK DRIVES

Upon power-on or any Reset operation, the controller sets default drive parameters based on the type of drive selected by jumpers W12 and W13 (for LUN 0) and jumpers W15 and W 16 (for LUN 1). These parameters can be overriden by issuing an Initialize Drive Characterists command (see chap 7).

	FIXED	FIXED/REMOV.	REMOV.
STEP PULSE WIDTH (in microseconds)	15	15	15
STEP PULSE PERIOD (in milliseconds)	3	.025	.025
NUMBER OF HEADS	4	2	2
MAXIMUM CYLINDER ADDRESS	153	320	612
REDUCED WRITE CURRENT CYLINDER	128	N/A	N/A
WRITE PRECOMPENSATION CYLINDER	128	157	400

The default number of sectors per track is based on jumpers W10 and W9.

W10	W9	Number of Bytes Per Sector (W10,W9)	Number of Sectors Per Track
0	0	128	55
0	1	256	32
1	0	512	17
1	1	1024	9

SECTION 4

WINCHESTER TRACK AND SECTOR FORMAT

4.1 SOFT SECTORED TRACK FORMAT

The standard track format for soft sectored Winchester Disk drives is organized into numbered data segments, or sectors (See Figure 4-1).

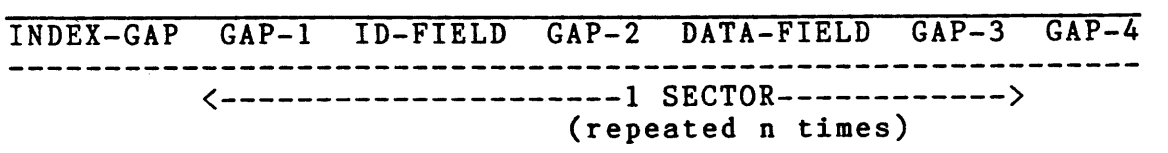

Figure 4-1 Standard Winchester Disk Sector Format

The nominal Winchester Disk track capacity is 10,416 bytes. The method of encoding used is Modified Frequency Modulation (MFM).

4.1.1 Winchester Soft Sectored Fields

INDEX GAP	=	11 BYTES of 4E	Head Switching Recovery Period
GAP 1	=	12 BYTES of 00	Sync for ID Field
ID FIELD	=	14 BYTES	
GAP 2	=	12 BYTES of 00	Write Update Splice and Sync for Data Field
DATA FIELD	=	XX BYTES	
GAP 3	=	14 BYTES of 4E	Speed Tolerance at Sector Level
GAP 4	=	XX BYTES of the	Speed Tolerance for the Track
	=	340 BYTES of 4E	(128 BYTES/SECTOR)
	=	325 BYTES of 4E	(256 BYTES/SECTOR)
	=	698 BYTES of 4E	(512 BYTES/SECTOR)
	=	667 BYTES of 4E	(1024 BYTES/SECTOR)

4.1.2 Sector ID Field

The beginning of each sector is defined by a prewritten identification (ID) field. This field is registered during the Format operation, and contains the Cylinder Address (MSB), Cylinder Address (LSB), Head Address, and Sector Address (See Figure 4-2).

BYTE #	
1	A1 Address Mark (Drop Clock Bit)
2	FE Address Mark
3	Cylinder (MSB)
4	Cylinder (LSB)
5	Head and Flags
6	Sector
7-10	ECC
11-12	00

Figure 4-2 Sector ID Field

4.1.3 Sector Data Field

The data field contains the user data bytes, selectable as 128, 256, 512, or 1024 Bytes per sector. The format for this field varies with the field size (See Figure 4-3).

128 BYTE DATA FIELD	
BYTE 1	A1*
2	F8
3-130	Data
131-134	ECC
135-136	00

256 BYTE DATA FIELD	
1	A1*
2	F8
3-258	Data
259-262	ECC
263-264	00

512 BYTE DATA FIELD	
BYTE 1	A1*
2	F8
3-514	Data
515-518	ECC
519-520	00

1024 BYTE DATA FIELD	
1	A1*
2	F8
3-1026	Data
1027-1030	ECC
1031-1032	00

* = Drop Clock Bit

4.2 HARD SECTORED TRACK FORMAT

The standard track format for hard sectored Winchester Disk drives is organized into numbered data segments, or sectors (See Figure 4-3).

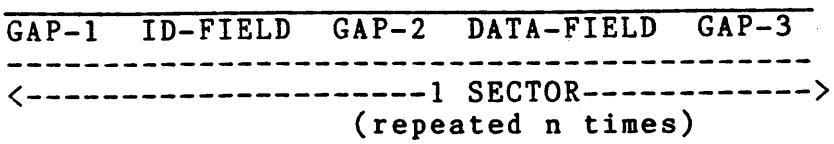

Figure 4-3 Standard Winchester Disk Sector Format

4.2.1 Winchester Hard Sectored Fields

GAP 1	=	12 BYTES of 00	Sync for ID Field
ID FIELD	=	14 BYTES	
GAP 2	=	12 BYTES of 00	Write Update Splice and Sync for Data Field
DATA FIELD	=	XX BYTES	
GAP 3	=	14 BYTES of 4E	Speed Tolerance at Sector Level

4.2.2 Sector ID Field

The beginning of each sector is defined by a prewritten identification (ID) field. This field is registered during the Format operation, and contains the Cylinder Address (MSB), Cylinder Address (LSB), Head Address, and Sector Address (See Figure 4-4).

BYTE #	
1	A1 Address Mark (Drop Clock Bit)
2	FE Address Mark
3	Cylinder (MSB)
4	Cylinder (LSB)
5	Head and Flags
6	Sector
7-10	ECC
11-12	00

Figure 4-4 Sector ID Field

4.1.3 Sector Data Field

The data field contains the user data bytes, selectable as 128, 256, 512, or 1024 Bytes per sector. The format for this field varies with the field size (See Figure 4-3).

128 BYTE DATA FIELD		256 BYTE DATA FIELD	
BYTE 1	A1*	1	A1*
2	F8	2	F8
3-130	Data	3-258	Data
131-134	ECC	259-262	ECC
135-136	00	263-264	00

512 BYTE DATA FIELD		1024 BYTE DATA FIELD	
BYTE 1	A1*	1	A1*
2	F8	2	F8
3-514	Data	3-1026	Data
515-518	ECC	1027-1030	ECC
519-520	00	1031-1032	00

* = Drop Clock Bit

4.3 Defective Track Format

If a track is found to be defective, the host can assign an alternate track for the defective track. When the controller encounters a defective track that has been assigned an alternate track, the alternate track will be accessed. The address of the alternate track is contained in the first three bytes of the data field in all sectors of the defective track. The ID fields of the defective track contain a flag indicating that the track has been alternated. The ID fields of the alternate track are formatted with a flag indicating that the track has been assigned as an alternate.

SECTION 5

5.1 GENERAL

This section describes the hardware and software features of the OMTI5510 Data Controller. The description includes a discussion of direct and indirect I/O interface. Direct access is accomplished by reading and writing four I/O Ports. Indirect access is achieved by executing pre-written I/O subroutines contained in a BIOS (Basic Input Output System).

Host commands are issued to the controller over the host bus using a predefined protocol. The host initiates a command sequence by selecting the controller. The controller accepts the selection, and requests the appropriate command bytes. If data transfer is required by the command, it can be transferred in either Programmed I/O or DMA mode. Data is transferred to or from a 2k buffer to optimize throughput during multiple sector operations. Upon command completion, the controller issues completion status to indicate whether the command was sucessfully completed or terminated because of an error.

5.2 Direct Control Operations

Direct access operations are controlled through four I/O ports (assigned default addresses 320, 321, 322, and 323). The Port addresses may be altered by jumpers W5 and W6. Each port is assigned one Read register and one Write register. Table 5-1 lists the four I/O ports and their correspoding registers and functions. Table 5-2 lists the registers and contains a brief desription of each registers.

Table 5-1 OMTI5510 I/O Port Addresses

PORT	REGISTERS READ	WRITE
320	DATA IN	DATA OUT
321	STATUS	RESET (Function)
322	CONFIGURATION	SELECT (Function)
323	N/A	MASK

Table 5-2 ONMTI5510 I/O Registers

REGISTER	DEFINITION
Data In	Used to read data and status from the controller to the system.
Data Out	Used to write data and commands from the system to the controller.
Status	Used to send bit significant control information from the controller to the system. Bit 7 Not Used (Set to 1) Bit 6 Not Used (Set to 1) Bit 5 IREQ (Interrupt Request) 0 = No Interrupt 1 = Command Complete If the Interrupt Enable bit of the MASK byte has been previously set, this bit is set when the controller enters the STATUS State. This bit is set with IRQ5 on the System Bit 4 DREQ (DMA Request) 0 = No DMA Request 1 = DMA Cycle Requested If the DMA ENABLE bit of the MASK BYTE has been previously set, and if the controller is in the DATA State, this bit is set along with DRQ3 on the System Bus when a byte transfer is required to or from the system. Bit 3 BSY (Busy) 0 = Controller is Idle 1 = Controller Selected Bit 2 C/D (Command/Data) 0 = Byte being transferred is command or status. 1 = Byte being transferred is data. Bit 1 I/O (In/Out) 0 = Direction of transfer is from the host to the controller. 1 = Direction of transfer is from the controller to the Host. Bit 0 REQ (Request) 0 = No Transfer Required 1 = Request transfer of one byte via Data In or Data Out register.

RESET — Writing any value to this register will cause the controller to be reset.

CONFIG-URATION — Used to send the status of the drive configuration jumpers to the system. Typically, these are used by a BIOS to specify the type of drive(s) attached to the controller.
Bits 7-4 = not used (Set to 1)
Bit 3 = W4
Bit 2 = W3
Bit 1 = W2
Bit 0 = W1

SELECT — Writing any value to this register will cause the controller to begin a Selection Sequence and request a command transfer.

MASK — Enables and disables interrupts and DMA transfers.
Bits 7-2 Not used.
Bit 1 INTERRUPT ENABLE
0 = No system interrupt at data transfer completion.
1 = System interrupt at data transfer completion.
Bit 0 DMA ENABLE
0 = No DMA enabled.
1 = DREQ is gated onto system bus on DRQ3 and DREQ set in STATUS register.

5.2.1 CONTROLLER STATES

At any given time, the controller will be in one of six states:
RESET
IDLE
SELECTION
COMMAND
DATA
STATUS

The RESET STATE is entered by applying power to the controller (power - on -reset), by the reset signal on the system bus, or by writing the STATUS Register (port 321). During this phase, the controller will initialize itself, will set default parameters (ST506) to the LUNs, will de-assert all control functions and clear all bits in the STATUS register. It will then enter the idle state.

The IDLE STATE is the only time the controller will respond to a select request. When the SELECT register (port 322) is written by the system, the controller enters the selection state.

During the SELECTION STATE, the controller responds to a

selection request by asserting the BSY bit (bit 3) in the STATUS register (port 321). The controller then enters the command state.

The COMMAND STATE is when the controller requests the command bytes to be transferred from the system. First, the C/D bit (bit 2) of the STATUS register is set. Then the REQ bit (bit 0) of the STATUS register is set, asking for the first command byte to be written to the DATA OUT register (port 320). When the command byte is written, the controller de-asserts the REQ bit and moves the command byte into its buffer. This handshaking is repeated until all command bytes are transferred. C/D is then de-asserted and the data state is entered.

The DATA STATE is when data is transferred to or from the system. If no data is required, the status state is entered. Data can be transferred in either programmed I/O mode or DMA mode, as defined by the DMA ENABLE bit in the MASK register. In the programmed I/O mode, data is transferred by handshaking in the same fashion as the command transfer. When the controller requires a byte to be transferred, it will set the REQ bit in the STATUS byte. Depending on the direction of transfer (as defined by the I/O bit in the STATUS byte), the system must either write a byte to the DATA OUT register or read a byte from the DATA IN register. Either action will cause REQ to be cleared. These steps will be repeated until all the data required by the controller has been transferred.

If the DMA ENABLE bit in the MASK byte has been previously set, data will be transferred in DMA mode. When the controller requires a byte to be transferred, it will set the DRQ3 bit on the system bus, requesting a DMA cycle. The DREQ bit of the STATUS byte is also set. After the data byte has been transferred, DACK3 from the system will clear DRQ3. The DMA transfer will proceed in this fashion until all of the data required by the controller has been transferred.

During the STATUS STATE, the controller will place a STATUS byte in the data in register. It contains the following bit significant information:

Bit 7 0
Bit 6 0
Bit 5 LUN
Bit 4 0
Bit 3 0
Bit 2 0
Bit 1 Command Error
Bit 0 0

The controller sets the C/D bit and the I/O bit in the STATUS byte. If the INTERRUPT ENABLE bit was previously set in the MASK register, the REQ bit is set in the STATUS byte, along with IRQ5 on the system bus. When the STATUS byte is read from

the DATA IN register, the controller clears the IREQ and IRQ5 (if enabled), clears C/D, I/O, and BSY bits in the STATUS Registers, and enters the idle state.

The controller sets the C/D bit and the I/O bit in the STATUS byte. If the INTERRUPT ENABLE bit was previously set in the MASK register, the REQ bit is set in the STATUS byte, along with IRQ5 on the system bus. When the STATUS byte is read from the DATA IN register, the controller clears the IREQ and IRQ5 (if enabled), clears C/D, I/O, and BSY bits in the STATUS Registers, and enters the idle state.

5.3 BIOS OPERATIONS

The OMTI5500 controller includes an EPROM containing an IBM PC-DOS compatible BIOS (Basic Input/Output System). Although it is physically located on the controller, it is addressable as a block of system memory starting at address C800(HEX). It's primary function is to serve as a driver, converting PC-DOS disk I/O functions into controller commands, issuing those commands, and reporting PC-DOS of the drive type (or types) attached to the controller. This involves the use of configuration jumpers to indicate an entry to a table of drive parameters. The BIOS also reads the configuration jumpers and issues ASSIGN PARAMETERS commands to configure the controller appropriate to the jumpers. SMS supplies different BIOS'S to support different drive configurations. Refer to appendix A for further details.

SECTION 6

6 DIRECT CONTROL PROGRAMMING CONSIDERATIONS

6.1.1 Command Descriptor Block

The processor specifies the operation or command to be executed by the controller by sending 6 or 10 bytes called a Command Descriptor Block (CDB) as follows.

6 BYTE COMMAND FORMAT

	7	6	5	4	3	2	1	0
BYTE 0	Command Class				Opcode			
BYTE 1	0	0	LUN		Head Number			
BYTE 2	Cyl. High					Sector Number		
BYTE 3	Cylinder Low							
BYTE 4	Interleave or Block Count							
BYTE 5	Control Byte							

Byte 0 - Bits 7,6 and 5 identify the class of the command.
Bits 4 through 0 contain the command Opcode.
Byte 1 - Bits 5 identifies the Logical Unit Number.
Bits 4 through 0 contain the disk head number to be selected.
Bit 7 and 6 are not used.
Byte 2 - Bits 7 and 6 contain the two most significant bits of the disk cylinder number.
Bits 5 through 0 contain the disk sector number
Byte 3 - Bits 7 through 0 are the eight least significant bits of the disk cylinder number.
Byte 4 - Bits 7 through 0 specify the Interleave factor for the the disk drives or the block count.
Byte 5 - Bits 7 through 0 contain the Control Byte.

10 BYTE COMMAND FORMAT

Copy Command

	7	6	5	4	3	2	1	0
BYTE 0	Command Code							
BYTE 1	0	0	SRC LUN		Head Number			
BYTE 2	Cyl Hi				Sector Number			
BYTE 3	Cyl Low							
BYTE 4	Block Count							
BYTE 5	0	0	DEST LUN		Head Number			
BYTE 6	Cyl Hi				Sector number			
BYTE 7	Cyl Low							
BYTE 8	Zero value							
BYTE 9	Control Byte							

Note: The copy command specifies both Source and Destination LUNs and starting sector addresses.

6.1.2 Control Byte

The control Byte is the last Byte of all commands.

CONTROL BYTE FORMAT

Bits	7	6	5	4	3	2	1	0
	r	a/d	0	0	0	s	s	s

r = Retries
a = Retry option on data ECC error (read cmds)
d = data from buffer or "6C" (format cmds)
s = Step option

BIT 7 - Disable Retry. If set to one, will disable controller automatic retries. This bit 7 is valid for those commands involving retries. This bit is typically used for media evaluation of the drives.

BIT 6 - Disable ECC. If set to zero during read commands, a read retry is attempted when an ECC error occurs. If no errors occurs during read retry, the command will complete with no error status reported. If this bit is set to one, no read retry is attempted, this is used for diagnostic purposes.

Format with data in buffer. If set to zero, format commands will fill data fields with "6C"(hex). If set to one, format commands will fill data fields with whatever data is in the data buffer.

BITS 5,4,3 - Set to zero.

BITS 2,1,0 - These bits define the step option.

2	1	0	
0	0	0	3 milliseconds per step.
0	0	1	N/A
0	1	0	25 microseconds, buffered step
0	1	1	50 microseconds, buffered step
1	0	0	200 microseconds, buffered step
1	0	1	70 microseconds, buffered step
1	1	0	3 milliseconds per step
1	1	1	3 milliseconds per step

6.2 Status Register

Status is available to the host in the Data Register during the Status State at the end of a command. It indicates whether or not an error was detected during execution of the command.

STATUS BYTE FORMAT

BITS	7	6	5	4	3	2	1	0
	0	0	LUN	0	0	0	e	0

e = Command status

Bit 1 A value of zero indicates a successfully completed command.
A value of one indicates an abnormal condition was encountered during the command execution and caused command termination and ending status with the Command Status Condition (bit 1) set to one.

Bit 5 indicates the LUN address of the device associated with this command.

Bits 7,6,4,3,2,0, set to zero.

SECTION 7

DISK COMMAND SET

7.1 TEST DRIVE READY Command (HEX 00)

This command selects the LUN specified and returns a zero status in the Status Register to indicate that the unit is selected, ready and seek complete. In the case of a unit with a removable disk, zero status also indicates that a cartridge is installed. For Fixed and Fixed/Removable drives, the controller will wait up to 50 seconds for the drive to come ready.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	0	0	0	0
BYTE 1	0	0	LUN	0	0	0	0	0
BYTE 2			ZERO VALUE					
BYTE 3			ZERO VALUE					
BYTE 4			ZERO VALUE					
BYTE 5			ZERO VALUE					

7.2 RECALIBRATE Command (HEX 01)

The drive specified by the LUN is stepped toward the outside cylinder until either:

1. Track Zero signal is detected or
2. More steps have been issued than available cylinders for the device type.

The controller issues one step pulse, waits for seek complete, and tests the Track 000 signal.

For LUNs assigned as Removable or Fixed/Removable, the recalibrate is performed by issuing the number of step pulses equal to the number of cylinders specified for this drive plus 5 at the buffered rate and then waiting for the Track 000 signal.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	0	0	0	1
BYTE 1	0	0	LUN	0	0	0	0	0
BYTE 2			ZERO VALUE					
BYTE 3			ZERO VALUE					
BYTE 4			ZERO VALUE					
BYTE 5	0	0	0	0	0	S	S	S

7.3 REQUEST SENSE Command (HEX 03)

The sense information to be returned during the Data In phase of this command execution is valid for the Check Condition Status just presented to the host during the previous unsuccessfully completed command. Sense data will be cleared upon reception of any subsequent command issued to the controller. Four sense bytes are returned during the data in phase the command execution.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	0	0	1	1
BYTE 1	0	0	LUN	0	0	0	0	0
BYTE 2	ZERO VALUE							
BYTE 3	ZERO VALUE							
BYTE 4	ZERO VALUE							
BYTE 5	ZERO VALUE							

SENSE DATA FORMAT

	7	6	5	4	3	2	1	0
BYTE 0	ERROR				CODE			
BYTE 1	0	0	LUN		HEAD NUMBER			
BYTE 2	CYL HI				SECTOR NUMBER			
BYTE 3	CYLINDER LOW							

7.4 FORMAT DRIVE Command (HEX 04)

This command causes the specified LUN to be formatted using the interleave factor specified in byte 4. Formatting starts at the specified track and proceeds until the last track of the unit is formatted. The track is written starting with the index. The first sector after index is always sector Zero. An interleave factor of Zero is set equal to one. Track and cylinder overflow is handled automatically by the controller. If bit 6 of the control byte is cleared, all the data fields are written with "6C". If bit 6 of the control byte is set, all the data fields are written with whatever data is is the data buffer. This allows "worst case" patterns to be written by first executing a WRITE DATA BUFFER command.

Note: This command does not check data, and does not handle media defects. For verification of format, see CHECK TRACK FORMAT command. For media defect handling, see the ASSIGN ALTERNATE TRACK, and the FORMAT BAD TRACK command.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	0	1	0	0
BYTE 1	0	LUN			HEAD NUMBER			
BYTE 2	CYL HI		0	0	0	0	0	0
BYTE 3	CYLINDER LOW							
BYTE 4	0	0	0		INTERLEAVE VALUE			
BYTE 5	r	d	0	0	0	s	s	s

7.5 READ VERIFY Command (HEX 05)

This command is used to check the integrity of the recorded data of a formatted disk. ID fields and data fields are verified against ECC value recorded. No data is transferred to the host.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	0	1	0	1
BYTE 1	0	LUN			HEAD NUMBER			
BYTE 2	CYL. HI				SECTOR NUMBER			
BYTE 3				CYLINDER LOW				
BYTE 4					BLOCK COUNT			
BYTE 5	r	a	0	0	0	s	s	s

7.6 FORMAT TRACK Command (HEX 06)

This command causes the track specified to be formatted using the interleave factor defined in Byte 4. The track is written starting with index. The first sector after index is always sector zero. Interleave factor of Zero is set to one. If bit 6 of the control byte is cleared, all the data fields are written with "6C". If bit 6 of the control byte is set, all the data fields are written with whatever data is is the data buffer. This allows "worst case" patterns to be written by first executing a WRITE DATA BUFFER command.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	0	1	0	0
BYTE 1	0	LUN			HEAD NUMBER			
BYTE 2	CYL HI		0	0	0	0	0	0
BYTE 3				CYLINDER LOW				
BYTE 4	0	0	0		INTERLEAVE VALUE			
BYTE 5	r	d	0	0	0	s	s	s

7.7 FORMAT BAD TRACK Command (HEX 07)

This command is identical to the FORMAT TRACK command except that the defective track flag is set in the ID field. All subsequent accesses to the sectors on this track will result in Bad track Flag set errors.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	0	1	0	0
BYTE 1	0	LUN			HEAD NUMBER			
BYTE 2	CYL HI		0	0	0	0	0	0
BYTE 3				CYLINDER LOW				
BYTE 4	0	0	0		INTERLEAVE VALUE			
BYTE 5	r	d	0	0	0	s	s	s

7.8 READ Command (HEX 08)

This command causes the number of blocks specified by byte 4 to be transferred from the LUN to the host. The command executes an implied seek to the starting sector specified. Up to 256 blocks can be transferred with a single READ command (If byte 4 is equal to zero, 256 sectors will be transferred).

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	1	0	0	0
BYTE 1	0	LUN			HEAD NUMBER			
BYTE 2	CYL HI				SECTOR NUMBER			
BYTE 3					CYLINDER LOW			
BYTE 4				BLOCK COUNT				
BYTE 5	r	a	0	0	0	s	s	s

7.9 WRITE Command (HEX 0A)

This command causes the number of blocks specified by byte 4 to be transferred from the host to the LUN. The command executes an implied seek to the starting sector specified. Up to 256 blocks can be transferred with a single WRITE command (If byte 4 is equal to zero, 256 sectors will be transferred).

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	1	0	1	0
BYTE 1	0	LUN			HEAD NUMBER			
BYTE 2	CYL HI				SECTOR NUMBER			
BYTE 3					CYLINDER LOW			
BYTE 4				BLOCK COUNT				
BYTE 5	r	0	0	0	0	s	s	s

7.10 SEEK Command (HEX 0B)

This command causes the device addressed by the LUN to be physically positioned to the cylinder as defined in bytes one to three. No attempt to verify seek position is made until a READ or WRITE command is issued. Completion status is returned to the host immediately after issuing all .required step pulses. This allows overlap seek operations.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	1	0	1	1
BYTE 1	0	LUN			HEAD NUMBER			
BYTE 2	CYL HI		0	0	0	0	0	0
BYTE 3					CYLINDER LOW			
BYTE 4	0	0	0	0	0	0	0	0
BYTE 5	r	0	0	0	0	s	s	s

7.11 INITIALIZE DRIVE CHARACTERISTICS Command (HEX 0C)

This command allows the host to specify disk drive parameters for the specified LUN. This allows the controller to communicate with a wide variety of drives from the same or different vendors. The associated Parameter List, including all characteristics of the drive connected, is sent to the controller during the Data Out phase of the command execution. There is no access to the drive during execution of this command.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	1	1	0	0
BYTE 1	0	LUN		0	0	0	0	0
BYTE 2	ZERO VALUE							
BYTE 3	ZERO VALUE							
BYTE 4	ZERO VALUE							
BYTE 5	ZERO VALUE							

Once the Device Control Block has been sent, the command enters a Data Out phase for 8 additional bytes configured as follows:

Parameter Block

	7	6	5	4	3	2	1	0
BYTE 0	Maximum Number of Cylinders (MSB)							
BYTE 1	Maximum Number of Cylinders (LSB)							
BYTE 2	Maximum Number of Heads							
BYTE 3	Start Reduced Write Current Cylinder (MSB)							
BYTE 4	Start Reduced Write Current Cylinder (LSB)							
BYTE 5	Start Write Precompensation Cylinder (MSB)							
BYTE 6	Start Write Precompensation Cylinder (LSB)							
BYTE 7	Set to zero.							

BYTES 0-1 - NUMBER OF CYLINDERS : These 2 bytes specify the maximum number of cylinders on the Disk drive. The controller is capable to address up to 1024 cylinders.

BYTE 2 - NUMBER OF HEADS : The value of this byte specifies the number of user heads on the Disk drive. The controller accepts a maximum of up to 16 heads with a value of 15 (HEX 0F). Any value greater than HEX 07 causes the reduced write current (WSI) function to be disabled.

BYTE 3-4 - START REDUCED WRITE CURRENT CYLINDER : These 2 bytes specify the cylinder address where reduced write current is first applied. Reduced write current is applied to all cylinders greater than or equal to the value of these 2 bytes. This function is disabled for Removable and Fixed/Removable drives.

BYTE 5-6 - START WRITE PRECOMPENSATION CYLINDER : These 2 bytes specify the cylinder address where write precompensation is first applied. Write precompensation is applied to all cylinders greater than or equal to the value of these 2 bytes. The amount of write precompensation is 12 nsecs.

7.12 READ DATA FROM SECTOR BUFFER Command (HEX OE)

The controller data buffer is transferred to the host as if a single sector READ has occured. The number of bytes returned is determined by the jumper selected block size. This command issued after a WRITE DATA TO SECTOR BUFFER command can be used as diagnostic function to check the controller buffer data integrity. No access to the drives occur during the command execution.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	1	1	1	0
BYTE 1			ZERO VALUE					
BYTE 2			ZERO VALUE					
BYTE 3			ZERO VALUE					
BYTE 4			ZERO VALUE					
BYTE 5			ZERO VALUE					

7.13 WRITE DATA TO SECTOR BUFFER Command (HEX OF)

This command causes data to be written from the host to the controller data buffer as if a single sector WRITE has occured. This command issued before a READ DATA TO SECTOR BUFFER command can be used as diagnostic function to check the controller buffer data integrity. No access to the drives occur during the command execution.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	1	1	1	1
BYTE 1			ZERO VALUE					
BYTE 2			ZERO VALUE					
BYTE 3			ZERO VALUE					
BYTE 4			ZERO VALUE					
BYTE 5			ZERO VALUE					

7.14 ASSIGN ALTERNATE TRACK Command (HEX 10)

This command is used to assign an alternate track to the track specified in bytes 1 to 3, so that any future accesses to the blocks on the specified track cause the controller to automatically access those blocks on the alternate track. This command sets flags in the ID field and writes the alternate track address in all blocks on the specified track. The alternate track is then formatted with flags set to indicate that this track has been assigned as an alternate track. Future direct accesses to the alternate track will result in an error. Interleave factor of zero is set to one.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	1	0	0	0	0
BYTE 1	0	LUN			HEAD NUMBER			
BYTE 2	CYL HI		0	0	0	0	0	0
BYTE 3	CYLINDER LOW							
BYTE 4	0	0	0		INTERLEAVE VALUE			
BYTE 5	r	0	0	0	0	s	s	s

The following 4 bytes, representing the alternate track address, are sent to the controller during the Data Out phase of the command execution.

ALTERNATE TRACK ADDRESS Descriptor Block

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	HEAD NUMBER				
BYTE 1	CYL HI		0	0	0	0	0	0
BYTE 2	CYLINDER LOW							
BYTE 3	0	0	0	0	0	0	0	0

Note : Data written on the original track as well as on the alternate track will be destroyed. The controller does not check if the track assigned as alternate track has been previously used as alternate track for another track. A track assigned as an alternate may not have an alternate track assigned to it.

7.15 CHANGE CARTRIDGE Command (HEX 1B)

This command is valid only for Removable disk drives. The command causes the "Change Cartridge " line (J2-Pin 2) to be asserted for a period of one (1) millisecond.

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	1	1	0	1	1
BYTE 1	0	LUN		0	0	0	0	0
BYTE 2 TO 5 SET TO ZERO								

7.16 COPY Command (HEX 20)

This command copies a specified number of blocks (byte 4) from a Source LUN to a Destination LUN. Source and Destination LUN's may be the same. Block sizes on both Source and Destination LUN's must be identical. Because the controller uses its internal buffer, no data is transferred to the host.

COPY Device Control Block

	7	6	5	4	3	2	1	0
BYTE 0	0	0	1	0	0	0	0	0
BYTE 1	0	SOURCE LUN			HEAD NUMBER			
BYTE 2	CYL HI		SECTOR NUMBER					
BYTE 3			CYLINDER LOW					
BYTE 4			BLOCK COUNT					
BYTE 5	0	DEST. LUN			HEAD NUMBER			
BYTE 6	CYL HI		SECTOR NUMBER					
BYTE 7			CYLINDER LOW					
BYTE 8			NOT USED					
BYTE 9	r	A	0	0	0	s	s	s

Note: If source and destination LUNs have different step rates, the step rate specified in the control byte should be the slower of the two.

7.17 RAM DIAGNOSTIC Command (HEX E0)

This command performs a pattern test on the internal controller buffer.

	7	6	5	4	3	2	1	0
BYTE 0	1	1	1	0	0	0	0	0
BYTE 1			ZERO VALUE					
BYTE 2			ZERO VALUE					
BYTE 3			ZERO VALUE					
BYTE 4			ZERO VALUE					
BYTE 5			ZERO VALUE					

7.18 READ ID Command (HEX E2)
This command returns 4 bytes of the ID field of the sector specified during the Data In phase of the command execution. Only one sector is processed per READ ID command.

	7	6	5	4	3	2	1	0
BYTE 0	1	1	1	0	0	0	1	0
BYTE 1	0	LUN			HEAD NUMBER			
BYTE 2	CYL HI		0	0	0	0	0	0
BYTE 3	CYLINDER LOW							
BYTE 4	0	0	0	0	0	0	0	0
BYTE 5	r	0	0	0	0	s	s	s

READ ID Descriptor Block

	7	6	5	4	3	2	1	0
BYTE 0	0	0	0	0	0	0	CYL HI	
BYTE 1	CYLINDER LOW							
BYTE 2	HEAD							
BYTE 3	SECTOR							

7.19 DRIVE DIAGNOSTIC Command (HEX E3)
This command causes the controller to perform drive diagnostics including recalibrate and reading sector 0 on all tracks.

	7	6	5	4	3	2	1	0
BYTE 0	1	1	1	0	0	0	1	1
BYTE 1	0	LUN		0	0	0	0	0
BYTE 2	ZERO VALUE							
BYTE 3	ZERO VALUE							
BYTE 4	ZERO VALUE							
BYTE 5	r	0	0	0	0	s	s	s

7.20 CONTROLLER INTERNAL DIAGNOSTICS Command (HEX E4)
This command causes the controller to perform some internal diagnostics including ROM Checksum and Sequencer self-test.

	7	6	5	4	3	2	1	0
BYTE 0	1	1	1	0	0	1	0	0
BYTE 1	ZERO VALUE							
BYTE 2	ZERO VALUE							
BYTE 3	ZERO VALUE							
BYTE 4	ZERO VALUE							
BYTE 5	ZERO VALUE							

7.21 READ LONG Command (HEX E5)

This command returns the Block size equal to the jumper selected sector size (128, 256, 512 or 1024) of data plus 4 bytes of ECC data.

READ LONG Device Control Block

	7	6	5	4	3	2	1	0
BYTE 0	1	1	1	0	0	1	0	1
BYTE 1	0	LUN			HEAD NUMBER			
BYTE 2	CYL HI				SECTOR NUMBER			
BYTE 3					CYLINDER LOW			
BYTE 4				BLOCK COUNT				
BYTE 5	r	0	0	0	0	s	s	s

7.22 WRITE LONG Command (HEX E6)

This command requires the Block size to be equal to the jumper selected sector size (128, 256, 512 or 1024) of data plus 4 bytes of ECC data.

	7	6	5	4	3	2	1	0
BYTE 0	1	1	1	0	0	1	1	0
BYTE 1	0	LUN			HEAD NUMBER			
BYTE 2	CYL HI				SECTOR NUMBER			
BYTE 3					CYLINDER LOW			
BYTE 4				BLOCK COUNT				
BYTE 5	r	0	0	0	0	s	s	s

APPENDIX A

BIOS CONFIGURATIONS (PRELIMINARY) 3/1/85

A.1 INTRODUCTION

This Appendix defines the drive types supported by each BIOS. Several versions of BIOS are supported by SMS-OMTI Controllers. The firmware to determine which configuration is supported is contained in a BIOS-EPROM. This firmware interprets the jumper configurations on the controller.

A.2 BIOS #1002411 (MODEL 5510-2) Configuration

Each LUN can independently support one of four drive types.

LUN 0						
W4	W3	DRIVE/MODEL	#CYL	#HEADS	WSI	PComp
1	1	DMA 360 (removable)	612	2	-	400
1	0	MINISCRIBE 3012	612	2	-	128
0	1	SEAGATE 419	306	6	-	128
*0	0	SEAGATE 412/212	306	4	-	128

LUN 1						
W2	W1					
1	1	DMA 360 (removable)	612	2	-	400
1	0	MINISCRIBE 3012	612	2	-	128
0	1	SEAGATE 419	306	6	-	128
*0	0	SEAGATE 412/212	306	4	-	128

Jumper Definitions:

0 = No jumper installed
1 = Jumper installed
* = As shipped

A.3 BIOS #1002450 MODEL 5510-3 Configuration

Both LUNs are assigned the same drive parameters, selected from one of sixteen drive types.

W1	W2	W3	W4	DRIVE/MODEL	#CYL	#HEADS	WSI	Pcomp
1	1	1	1	MAXTOR 1140	918	15	-	-
1	1	1	0	CMI 6426	640	4	-	255
1	1	0	1	ATASI 3030	645	5	-	319
1	1	0	0	QUANTUM Q520	512	4	-	255
1	0	1	1	VERTEX 170	987	7	-	-
1	0	1	0	DMA 360 (REMOV.)	612	2	-	399
1	0	0	1	MINISCRIBE 3012	612	2	-	127
1	0	0	0	SEAGATE ST419	306	6	-	127
0	1	1	1	MAXTOR 1105	918	11	-	-
0	1	1	0	QUANTUM Q540	512	8	-	255
0	1	0	1	FUGITSU 2243	754	11	-	-
0	1	0	0	COGITO ST225,PT925	612	4	-	255
0	0	1	1	CDC 9415-36	697	5	-	255
0	0	1	0	MINISCRIBE 3012	612	2	-	127
0	0	0	1	CMI 6640	640	6	-	255
0	0	0	0	SEAGATE ST412,ST212	306	4	-	128

Jumper Definitions:

0 = No jumper installed
1 = Jumper installed
* = As shipped

A.4 BIOS #1002451 MODEL 5510-4 Configuration

This version supports both LUNs on one physical drive. The drive is divided so that the outer cylinders are assigned to LUN 0 and the inner cylinders are assigned to LUN 1. The jumpers select one of sixteen drive types.

W1	W2	W3	W4	DRIVE/MODEL	#CYL	#HEADS	WSI	Pcomp
1	1	1	1	MAXTOR 1140	918	15	-	-
1	1	1	0	CMI 6426	640	4	-	255
1	1	0	1	ATASI 3030	645	5	-	319
1	1	0	0	QUANTUM Q520	512	4	-	255
1	0	1	1	VERTEX 170	987	7	-	-
1	0	1	0	DMA 360 (REMOV.)	612	2	-	399
1	0	0	1	MINISCRIBE 3012	612	2	-	127
1	0	0	0	SEAGATE ST419	306	6	-	127
0	1	1	1	MAXTOR 1105	918	11	-	-
0	1	1	0	QUANTUM Q540	512	8	-	255
0	1	0	1	FUGITSU 2243	754	11	-	-
0	1	0	0	COGITO ST225,PT925	612	4	-	255
0	0	1	1	CDC 9415-36	697	5	-	255
0	0	1	0	MINISCRIBE 3012	612	2	-	127
0	0	0	1	CMI 6640	640	6	-	255
0	0	0	0	SEAGATE ST412,ST212	306	4	-	128

Jumper Definitions:

0 = No jumper installed
1 = Jumper installed
* = As shipped

APPENDIX B
ERROR CODE SUMMARY AND DESCRIPTION

Sense Bytes

At completion of a command, if the Status register reports an error condition (Bit 1 set), the system may issue a REQUEST SENSE command (HEX 03) during which four bytes are returned (Byte 0 through 3 as follows).

SENSE BYTES FORMAT

BITS	7	6	5	4	3	2	1	0
BYTE0	AV	0	ERROR TYPE			ERROR CODE		
BYTE1	0	0	LUN			HEAD NUMBER		
BYTE2	CYL HI				SECTOR NUMBER			
BYTE3	CYLINDER LOW							

AV = Address Valid. If set, indicates that the error code in byte 0 applies to the sector address in bytes 1,2,3.

ERROR TYPE (Bits 5 and 4):

5	4	
0	0	Drive Errors
0	1	Data errors
1	0	Command Errors
1	1	Diagnostic Errors

TYPE 0 - Drive Error

5	4	3	2	1	0	
0	0	0	0	0	0	No error
0	0	0	0	0	1	No Index
0	0	0	0	1	0	No seek complete
0	0	0	0	1	1	Write Fault
0	0	0	1	0	0	Drive not ready
0	0	0	1	1	0	No track zero found
0	0	1	0	0	0	Seek in progress
0	0	1	0	0	1	Cartridge changed

TYPE 1 - DATA ERRORS

5	4	3	2	1	0	
0	1	0	0	0	0	ID Read error
0	1	0	0	0	1	Uncorrectable Data Error
0	1	0	0	1	0	ID address Mark not found
0	1	0	0	1	1	Data address mark found
0	1	0	1	0	0	Sector not found
0	1	0	1	0	1	Seek error
0	1	0	1	1	0	Sequencer/DMA failure
0	1	0	1	1	1	Write protected
0	1	1	0	0	0	Correctable Data Error
0	1	1	0	0	1	Bad track
0	1	1	1	0	0	Unable to read Alt. Track Data
0	1	1	1	1	0	Illegal Direct Access to Alt Trk

TYPE 2 - COMMAND ERRORS

5	4	3	2	1	0	
1	0	0	0	0	0	Invalid Command
1	0	0	0	0	1	Illegal Disk Address
1	0	0	0	1	0	Illegal Function for Drive Type
1	0	0	0	1	1	Volume Overflow

TYPE 3 - DIAGNOSTIC ERRORS

5	4	3	2	1	0	
1	1	0	0	0	0	RAM error
1	1	0	0	0	1	EPROM checksum error

DESCRIPTION OF ERROR CODES

TYPE 0 - ERROR CODE DESCRIPTION

00 No error or no sense information. Indicates that there is no specific sense information to be reported for the designated Logical Unit Number. This is the case for the successful completion of the previous command.

01 No Index signal from the disk drive. The drive was ready but the controller did not detect the Index signal coming from the drive interface control cable indicating the beginning of the track. The controller waited at least three seconds. This error may occur during the following commands; FORMAT DRIVE, FORMAT TRACK, FORMAT BAD TRACK, ASSIGN ALTERNATE TRACK. Verify the cable and connector before investigating drive or controller problems.

02 No Seek Complete. The controller did not receive the Seek Complete signal coming from the drive, indicating that the step function issued has been completed. The controller waited at least three seconds before reporting this error.

03 Write Fault received from the drive. The Write Fault signal is sampled before turning on Write Gate on and after turning Write Gate off. Consult the disk drive specifications for all possible conditions reporting this error. Check the drive power supply voltage and drive connector.

04 Drive Not Ready. This status occurs when the selected drive is not ready. The drive may not be at its optimum speed. Absence of cartridge or media inserted in the drive will also cause this status. Check the drive power supply and drive connector if this status persists.

06 No Track zero found. During a RECALIBRATE command the controller issues step pulses and checks for Track zero after every step. This error occurs if the controller issued 5 more steps than the total number of cylinders, as currently defined for this LUN, and did not detect the Track zero signal from the drive.

08 Seek in progress. This error code is returned only in response to a REQUEST SENSE (HEX 00) command. The drive does not indicate "seek complete" and may be busy seeking to the location defined by the previous SEEK command. This error code is to be expected when overlapping seeks to the different drives connected to the controller are issued. The controller will keep reporting this code until the disk drive sends the Seek Complete signal.

09 Cartridge Changed. The controller received the Cartridge Changed signal from the drive indicating that the door was opened and closed (with the possibility that the cartridge was changed).

TYPE 1 - ERROR CODE DESCRIPTION

10 ID Read error. The controller was not able to find the specified sector. The controller was able to read at least one ID field and determined that it was on the right track, but detected an ID field ECC error. The disk may have a flaw in this particular location.

11 Uncorrectable Data error. The controller detected a data field error that could not be corrected by the ECC. The burst error length might be greater than the limits of capability of the ECC, or the error might have involved a multiple burst on the media. The data block is not transferred to the host. The command stops its execution when encountering this condition, and does not exhaust the block count. The last data block sent to the host was the last good block for which no error was encountered. The Sense Bytes of the REQUEST SENSE command sent following this error will report the Logical Block address at which the error occured. The data block that contains the error can be accessed by a Read Data from Sector Buffer command. This command will return the block involved, provided that no other command (including REQUEST SENSE command) has been issued since the Uncorrectable Data error occured.

12 ID Address Mark not found. The controller was not able to read any ID fields on this track. The selected disk head might be over an unformatted track or there is a failure in the read circuitry.

13 Data Address Mark not Found. The controller was able to read the sector ID but the Data Address Mark was not detected after 512 byte times or an address mark was detected but the byte value did not compare with the expected value.

14 Sector not found. The controller was able to read at least one ID field and determined that it was on the right track, but could not find the specified Address Mark. The disk may have a flaw in this particular location.

15 Seek error. The controller could not find the specified ID field, and there was a mis-compare of the cylinder or head address between the recorded and the target ID fields.

16 Sequencer/DMA Failure. Data overrun/underrun internal to the controller.

17 Write Protected. During WRITE commands, the Removeable Disk drive sent the Write Protect signal to the controller indicating that the media is protected for write operations.

18 Correctable ECC error. This error indicates that the block which contains an error could have been corrected by the ECC algorithm but ECC correction has been disabled. The data block involved is sent to the host with the error corrected. The command execution is stopped at this sector and the block count is not exhausted. Note that if correction is enabled and if the error was corrected by the ECC, the controller will not report any error.

19 Bad Track. The controller detected that the specified sector is on a track that has been flagged in the ID field as bad by the FORMAT BAD TRACK command. It is not possible to access the sectors on a flagged bad track.

1C Unable to read Alternate Track Data. During an access to a specified sector, the controller found a track with the "Bad track" Flag and the "Alternate track assigned" Flag set in the ID field. The controller stepped the drive to the alternate track but was unable to locate the specified sector on the alternate track, or found that the Alternate Track Flag was not set in the ID field.

1E Illegal Direct access to Alternate Track. The controller received a command with the Sector Address corresponding to an alternate track, and found the "Alternate track" Flag set in the ID field. Tracks reserved as alternates may not be accessed directly by a data transfer command. These tracks are only accessed by the controller's automatic handling of media defects.

TYPE 2 - ERROR CODE DESCRIPTION

20 Invalid Command. The controller decoded a command code that it does not support.

21 Illegal Disk Address. The controller received a command with a Sector Address beyond the capacity of the drive. Check the number of cylinders, heads and sector size that the drive is configured for.

22 Illegal Function for Drive Type. A Change Cartridge command (HEX 1B) was issued to a LUN assigned as a Fixed drive type.

23 Volume Overflow. After the commencement of a multiblock command, the end of volume was reached.

TYPE 3 - ERROR CODE DESCRIPTION

30 RAM error. The controller detected a data error with its internal RAM buffer of 2K bytes.

31 EPROM Checksum error. A checksum error was detected in the EPROM.