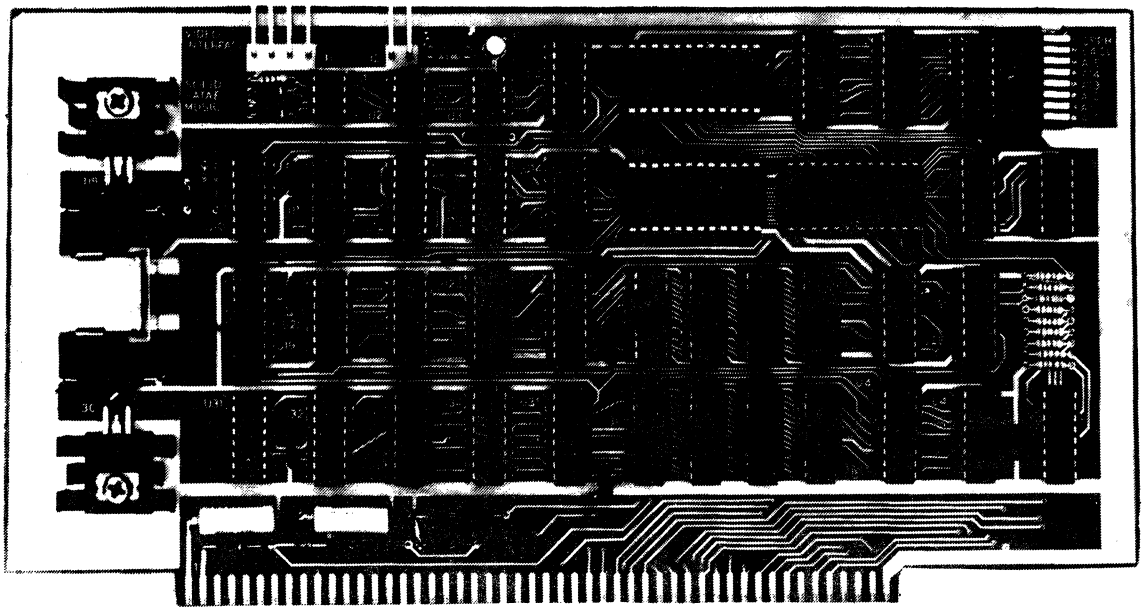
Solid State Music

VB1-B

VIDEO INTERFACE



FEATURES

- S100 Bus Compatible
- 32 or 64 Characters per line
- 16 Lines
- Graphics (128 x 48 matrix)
- Left & Right horizontal margins of about 8% of the full raster width
- Upper vertical margin of about 6%
- Vertical rate- 60.0Hz, Horizontal rate- 16.20KHz
- Parallel & Composite video
- On board low power memory
- Powerful software included for cursor, home, EOL, scroll, Graphics/Character, etc.
- Upper case, lower case & Greek
- Output to video monitor or video amplifier in T.V. set
- Black-on-white & white-on-black
- Sockets included

PARTS

1-	PC board	7-	100 ohm $\frac{1}{4}$w
1-	copy software	1-	220 ohm $\frac{1}{4}$w
1-	MCM6571AP	2-	470 ohm $\frac{1}{4}$w
1-	74LS00	9-	2.7K $\frac{1}{4}$w
1-	74S04	2-	1K $\frac{1}{4}$w
1-	7408	2-	15 ohm 3w
1-	7432	10-	.01 discs
4-	7474	1-	50pf disc
1-	7486	2-	2.7uf 20v Tantalum
2-	74150	3-	39uf 10v Tantalum
1-	74153	1-	1N746A ZD 3.3v
2-	74157	1-	1N4742/1N716 ZD 12v
1-	74166	1-	12.44MHz crystal
2-	74161	2-	heatsinks
4-	74193	2-	sets No. 6 hardware
6-	74367/8097	3-	24 pin sockets
1-	8131	3-	8 pin sockets
3-	75451	25-	16 pin sockets
2-	340T-5/7805	9-	14 pin sockets
8-	2102AL-2	1-	8 POS DIP switch
2-	Plug sets	1-	Instruction set
1-	2N2222		

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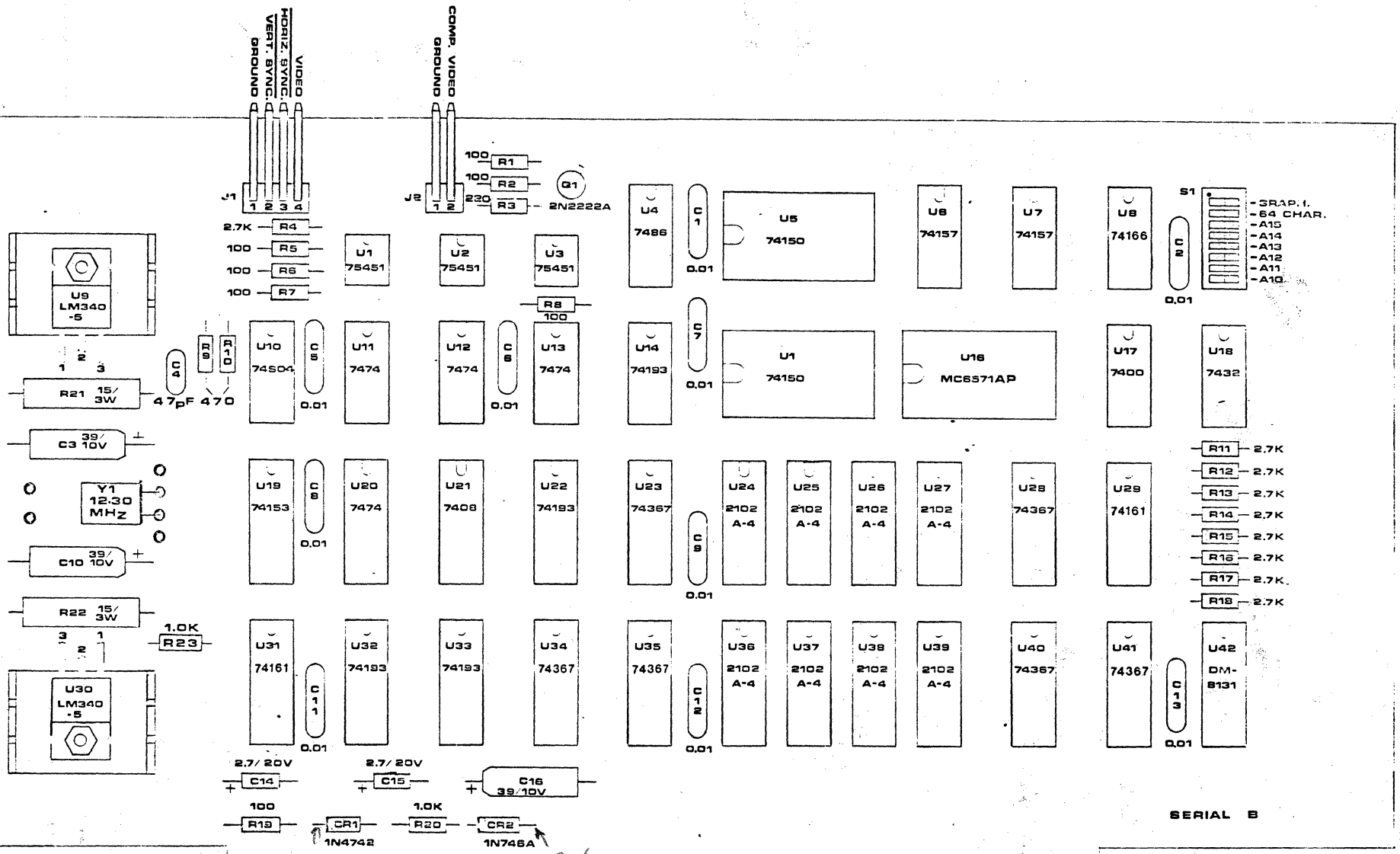

NOTES: UNLESS SPECIFIED OTHERWISE:

1. ALL CAPACITORS ARE IN UF
2. ALL RESISTORS ARE IN Ω

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES		Solid State Music, Inc.
		ASSEMBLY DRAWING. VB1 VIDEO BOARD
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	11-11-77	DO NOT SCALE DRAWING / SHEET 7

VB1 VIDEO INTERFACE BOARD

1.0 Assembly Instructions (Refer to VB1 Assy. Dwg.)

- [ ] Check kit contents against parts list.
- [ ] Check PC board for possible warpage & straighten if required
- [ ] Insert the 25 sixteen-pin sockets into the component side of the board with the "pin 1" index toward the top of the board.(The component side is the side on which "Solid State Music" is printed.) DON'T SOLDER.
- [ ] Insert the 9 fourteen-pin sockets. DON'T SOLDER.
- [ ] Insert the 3 eight-pin sockets. DON'T SOLDER.
- [ ] Insert the 3 twentyfour-pin sockets with "pin 1" toward the left of the board. DON'T SOLDER.
- [ ] Place a flat piece of stiff cardboard of appropriate size on top of the sockets to hold them in place.
- [ ] Holding the cardboard in place against the sockets, turn the board over and lay it on a flat surface. (Be sure that all the socket pins are thru the holes.)

  NOTE: Keep soldering iron tip clean to prevent rosin and sludge from being deposited on traces. Wipe tip frequently on a damp cloth or steel wool.

- [ ] On each socket, solder two of the corner pins,choosing two that are diagonally opposite of each other.
- [ ] Once the sockets are secured, lift the board and check to see if they are flat against the board. If not, seat the sockets by pressing on top while reheating each solder pin.
- [ ] Complete soldering the remaining pins on each socket. Touch pin and pad with iron tip, allowing enough solder to flow to form a filet between pin and pad. Keep the tip against the pin and pad just long enough to produce the filet. Too much heat can cause separation of pad and trace from the board. A 600 degree iron tip is recommended.
- [x] Observing polarity, insert and solder the 5 tantalum capacitors.
- [x] Observing polarity, insert and solder the 2 zener diodes.
- [ ] Insert and solder the 21 one-fourth watt resistors. DO NOT insert the 2 three-watt resistors.

1.0 Assembly Instructions (cont'd)

- [x] Observing polarity, insert and solder the transistor.
- [ ] Insert and solder the crystal.
- [ ] Insert and solder the DIP switch with the word "OPEN" to the left of the board.
- [ ] Insert and solder the 2 connectors. Be sure the teflon bases sit flat against the board.
- [ ] Insert and solder the 10 0.01μF capacitors and the 50pf capacitor.
- [ ] Place regulators on the board so the mounting hole in the regulator is in line with the hole in the board. Mark leads for proper bending to match the board holes--allow for bend radius.
- [ ] Bend regulator leads to match holes in board.
- [ ] If available, apply thermal compound to the back side of each regulator case (the side that will contact the heat sink). Use just a little thermal compound. Too much is worse than none at all.
- [ ] On the front (component side) of the board, first put on the heat sink (See VB1 Assy. Dwg.), next the regulator, and finally insert the #6 screws for each of 2 regulators. Secure firmly from front side with lock nuts. Be sure the screws are tight and the regulator, heat sink, and board all fit together flatly for a good thermal connection. Now solder the regulator leads.
- [ ] At this point the only parts yet to be mounted are the two power resistors and all the IC's. DO NOT MOUNT THESE YET.
- [ ] Apply power (+8 volts approx.) to board by plugging into computer or by connection from a suitable power supply. Measure the regulated output of each regulator. If less than 4.8 volts is measured (allowing for meter accuracy) check for shorts or wiring errors. CAUTION: WHILE IT HAS NEVER HAPPENED TO US, SHORTED REGULATORS HAVE BEEN KNOWN TO EXPLODE WITH POSSIBLE INJURY TO EYES OR HANDS. BETTER SAFE THAN SORRY-KEEP FACE AND HANDS CLEAR OF THE REGULATOR SIDE OF THE BOARD DURING THIS AND SUBSEQUENT TESTS!
- [ ] Apply power (+16 volts) to the board by plugging into computer or by connection to a suitable power supply. Check for voltage on zener D1 of approx. 12 volts.

[ ] Apply power (-16 volts) to the board by plugging into computor or by connection to a suitable power supply. Check for voltage on D2 of approx. -3 volts.

[ ] Insert and solder the 2 power resistors. Important; mount these resistors up off the board about one-eighth inch. This gives the resistors better cooling and keeps them from discoloring the circuit board.

[ ] Finally, insert the IC's into their sockets, observing polarity.

[ ] Now, look the board over carefully. Check for poor solder joints or bridges. Using the component layout drawing, look for improper part location or polarity. A few minutes of careful inspecion may save a few hours of troubleshooting.

2.0 SET-UP

2.1 HARDWARE REQUIREMENTS

Computer with S-100 bus. (Altair 8800, IMSAI, etc.)
ASCII keyboard or teletype
Two parallel input ports (for keyboard)
1K of RAM (located at 3C00 hex)

2.2 KEYBOARD INTERFACE

The Console Input (CI) and Console Status (CSTS) subroutines contained within the Demo programs supplied assume a standard (MITS rev. 1) keyboard interface. This interface uses Input Port 1 for data input, and Input Port 0 bit 0 (lsl) for a status bit (data available). Other input configurations can be accommodated by modifying these subroutines.

2.3 BOARD ADDRESSING

VB1 RAM address space is EC00 hex to EFFF hex for specifed software.
Set address selection switches on VB1 as follows:

A15	OFF	A12	ON
A14	OFF	A11	OFF
A13	OFF	A10	OFF

2.4 SYSTEM OPERATION (Demo Programs)

A. Load programs in specified locations.
B. Momentarily set the RESET.
C. EXAMINE starting address of program to set program counter.
D. Turn off sense switches (A15-AØ) & hit the RUN switch.

2.5 PROGRAM LOADING

The software supplied may be loaded into the computer by any one of the following methods:

1) Paper-tape Program:
   a. Put an Intel-format loader program into computer (user supplied).
   b. Run object program tape (supplied with VB1)
2) PROM Program:
   Run program from PROM (pre-programmed PROMs are available from Solid State Music with a 2K 8Ø8Ø monitor program)
3) Source Listing:
   a. Load an Assembler program into computer.
   b. Enter Source program in software listing.
4) Object Listing:
   Enter Object program in software listing directly into memory.

2.6 SENSE SWITCH FUNCTIONS:

Additional control flexability is provided for thru the use of the sense switches on the front panel of your mainframe. Setting sense switches to the "0" position will perform functions as defined below:

A8: output stops at bottom of page

A9: truncate line after 63 characters

2.7 MONITORS

CAUTION: HIGH VOLTAGE may be present in set even if unplugged. Service or modifications should be preformed ONLY by qualified personnel.

2.7.1 MONITOR CONNECTION

CAUTION: DO NOT USE A TRANSFORMERLESS TV FOR A MONITOR.

1) Most monitors can be connected directly to the composite video output with a single coax.

2) Some monitors may require the parallel video outputs provided.

3) Most TV sets will require one of the following:

   A. The addition of a jack connected to the input of the video amplifier (other inputs must be disconnected).

   B. Use of an RF Modulator to process the composite video signal for connection directly to antenna terminals.

2.7.2 MONITOR ADJUSTMENTS

The monitor or TV may need to have the horizontal and vertical size adjusted in order to get all of the data field on the screen. (Monitors set-up for TV pictures run the picture off the screen in order to eliminate "borders".)

3.0 TROUBLE SHOOTING HINTS

a. Check for proper settings of DIP switches.

b. Verify that all ICs are in the correct sockets.

c. Visually inspect all ICs to be sure that leads are in the sockets and not bent under.

d. Verify that the output voltage of each regulator is correct.

e. Inspect back side of board for solder bridges, running a small sharp knife blade between traces that appear suspicious. A magnifying glass is a must for this.

f. If you have an addressing problem:
   1) Check U42 (DM 8131) for addresses A10 thru A15.
   2) Check inputs & outputs of address buffers U23, U35, & U40 for shorts as well as proper operation.

g. If you have a problem with data output (consistent missing bits):
   1) Check inputs & outputs of buffers U28, U40, & U41 for shorts as well as proper operation.
   2) Check memory chips U24-U27 & U36-U39.

h. If you have a problem with horizontal sync:
   1) Check signals on U20, U31, U32, U19 & U1Ø.

i. If you have problems with the vertical sync:
   1) Check signals on U12, U33, U29 & U17.

4.0 THEORY OF OPERATION

(Design improvements over VB-1A by LYNN COCHRAN)

4.1 GENERAL

The VB1 video interface is essentially a computer memory combined with an interface circuit that connects the memory to a video monitor. The memory data may be displayed in either alphanumeric form using the internal character generator, or in a direct form (graphics). Characters may be presented either white-on-black or black-on-white. Mixing characters and graphics is also possible.

4.0 THEORY OF OPERATION (cont'd)

4.1 GENERAL

The MCM6571AP Character Generator can display 128 different characters. Other generators with different character sets are available.

Sixteen lines of characters are produced and either 32 or 64 characters per line may be selected. Total memory consists of eight 1024-bit RAMs. Ten of the computer's memory address lines are connected to these RAMs, allowing the computer to selectively address each display position. The computer's remaining 6 address lines are used for addressing the board's memory location, as selected by a DIP switch on the circuit board.

4.2 SYNC GENERATION

Figure 1 shows the 12.4MHz crystal oscillator feeding a series of two counters, U31 and U32. Counter U31 divides the 12.44MHz signal by eight and passes the resulting 1.5375MHz signal to U32 for further division by sixteen. The DOT CLOCK is a square wave timing signal used in shifting out video. The LOAD signal is a pulse occurring once every eight DOT CLOCKs. Both the DOT CLOCK and the LOAD signal must be selected for either 32 or 64 character-per-line operation. If the "64/32" switch is open, the 6.22MHz from U31, QA is selected to be the DOT CLOCK; if the switch is closed, 12.4MHz from the oscillator is selected.

For the LOAD signal, switch "open" selects a 777.5 KHz signal and switch "closed" selects a +5 volt level. The LOAD signal is modified by the 1.5550 MHz pulse signal from the output of U10, pin 1Ø, to become a series of narrow pulses at either 777.5 KHz

4.2 SYNC GENERATION (cont'd)

(64/32 switch open) or 1.5550 MHz (switch closed).

The 97.2 KHz carry signal from U32 is the input for the horizontal timing circuitry shown in figure 2. Both U11 flipflops and U20, pins 8-13, are used to divide the 97.2KHz from U32 by six to give horizontal blanking signals at 16.20 KHz. U13 generates a delayed horizontal sync pulse from U21, but only during horizontal blanking. U20, pins 1-6, develops the horizontal drive signal. Waveforms are shown as aids to troubleshooting in figures 1 thru 3.

In figure 3, the BIT SELECTOR CLOCK (16.20KHz) goes to the bit select counter U29. The outputs from U29, QA thru QD, give the row select address for the character generator. When address 1110_2 is reached, U29 is loaded with 0000_2 on the next clock pulse to start a new cycle. The load signal is a negative pulse at 1079.9 Hz which is sent to flipflop U12 and vertical line counter U33. In addition to 4 bits of RAM address, U33 puts out negative pulses at 60.0 Hz on $\overline{CY}$. U12 derives negative pulses at 60.0 Hz for both VERT DRIVE (1ms pulse width) and $\overline{\text{VERT BLANK}}$ (2ms pulse width). $\overline{\text{VERT BLANK}}$ and $\overline{\text{HORIZ BLANK}}$ are combined by an AND gate to give a composite $\overline{\text{BLANKING}}$ signal. The other 6 bits of RAM address come from counters U14 and U22 (on sheet 2), which are reset by $\overline{\text{HORIZ BLANK}}$. U22's clock is the LOAD signal from fig. 1.

4.3 ADDRESSING

The eight 1024-bit RAMs are addressed by the computer

4.3 ADDRESSING (cont'd)

using the 10 address lines AØ thru A9. 6 additional lines form a prefix to specify the video board's address. This 6 bit prefix is set by the DIP switch on the board. U42 compares the address sent by the computer against the switch. If they agree the $\overline{\text{SELECT}}$ signal goes low actuating the 10 address gates (AØ thru A9), the output gates, (D10 thru D17), and the write gate U17. $\overline{\text{SELECT}}$ signal low also turns off the output gates of counters U14, U22, and U33. With the memory now "listening", the computer may store data on the video board to be displayed. When the address from the computer no longer matches the switch the $\overline{\text{SELECT}}$ line goes high and the memory is isolated once again.

4.4 PICTURE FORMATION

When in the normal character display mode, the memory is continully addressed by the counters U14, U22, and U33. The memory puts out an 8-bit word for each address. Only 7 bits go into the character generater data input to specify a character or into the multiplexers U5 and U15 for graphical output. Both the output of the character generator and the graphics multiplexers are fed into two data selectors, U6 and U7. If the $\overline{\text{GRAPHICS}}$ signal is low it passes the graphics data from U5 and U15. If $\overline{\text{GRAPHICS}}$ is high it passes the character generator output. In either case the data selectors' output are loaded into parallel-in/serial-out shift register U8. The data is then shifted out to the display monitor.

4.0 THEORY OF OPERATION (cont'd)

4.4 PICTURE FORMATION (cont'd)

That eighth bit of memory is a control bit whose function depends on the VID REV/$\overline{\text{GRAPHICS}}$ switch. If the switch is open, $\overline{\text{GRAPHICS}}$ is high and the character generator output is going into output shift register U8. The eighth bit then turns the video reverse on or off by setting flipflop U13. This controls the VIDEO REVERSE signal thru gate U2. If VIDEO REVERSE is low the shift register output is unchanged, but if VIDEO REVERSE is high then gate U4 inverts the output giving a reversed video effect on the monitor. If the VID REV/$\overline{\text{GRAPHICS}}$ switch is closed the VIDEO REVERSE signal stays low unaffecting the shift register output. Now the eighth bit directly controls the GRAPHICS signal. If GRAPHICS is high then the character generator output is selected. If GRAPHICS is low then the graphics data is used.

4.5 POWER SUPPLIES

Power supply voltages of +8V and +16V are used to run the video board. The +8V input is regulated down to +5V by two 3-terminal regulators. R21 and R22 power resistors keep the power dissipation low in the regulators. Typical 8V current drain is 1.3A. The +16V input is regulated down to 12V by zener diode D1. The 16V current is about 40mA. Similarly, the -16V input is zener regulated down to -3V by D2. The -16V current is about 13mA.

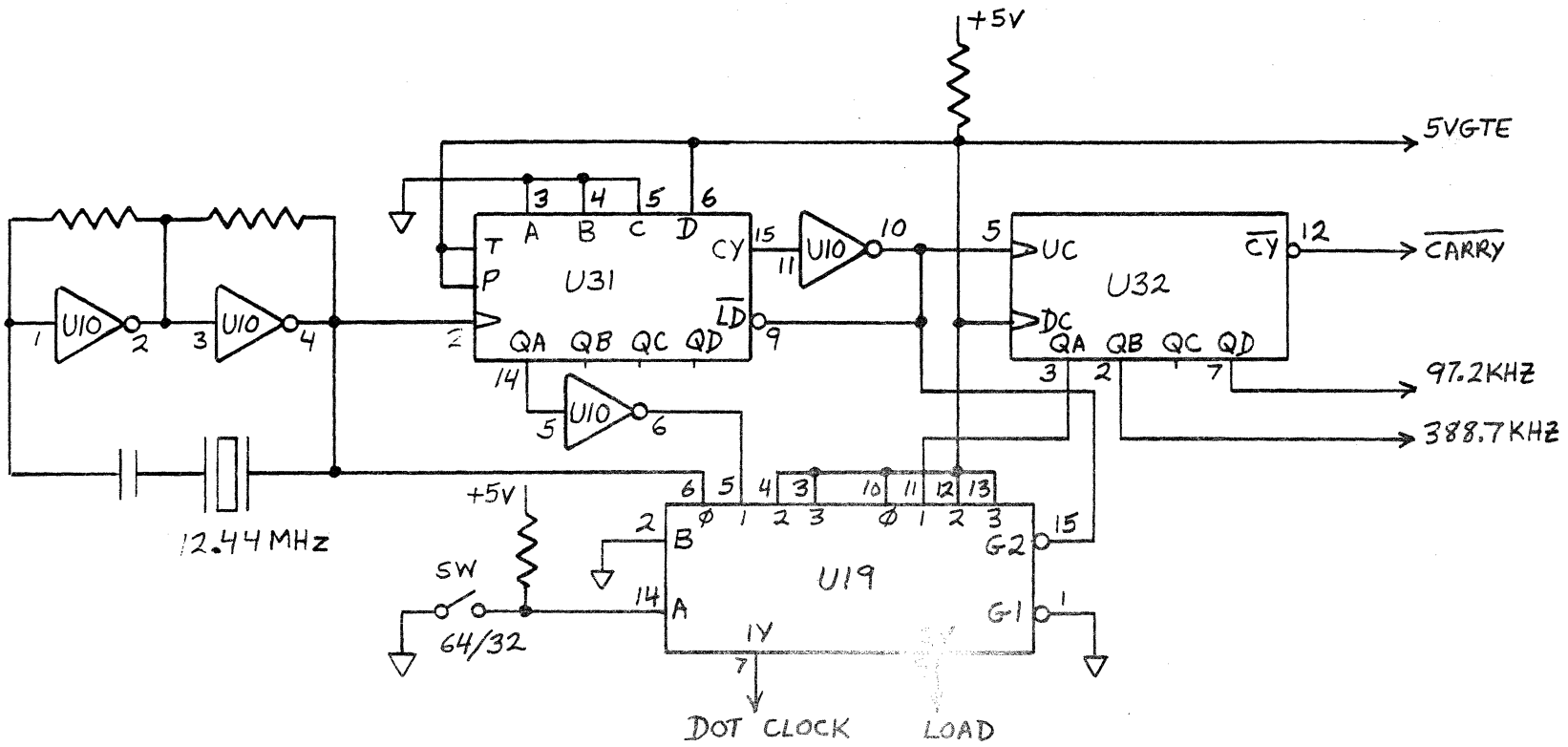
5.0 WARRANTY

Parts guaranteed to original purchaser for 90 days, unless failure is due to misuse or failure of purchaser to excercise caution in assembly and operation. Registration card must be returned at

5.0 WARRANTY (cont'd)

time of purchase to validate warranty.

Assembled boards may be returned for service. A service charge will be made unless, in our judgement, the problem is due to a defective board or parts.



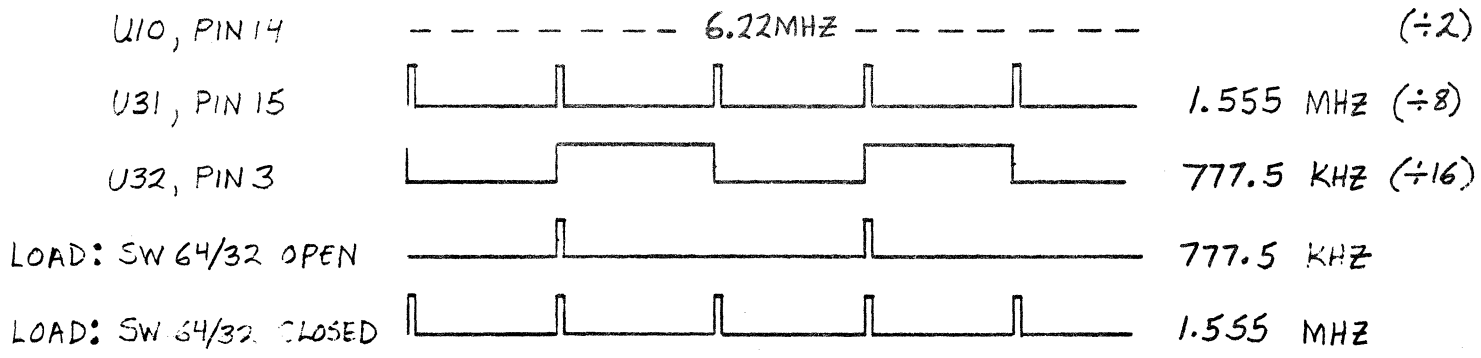
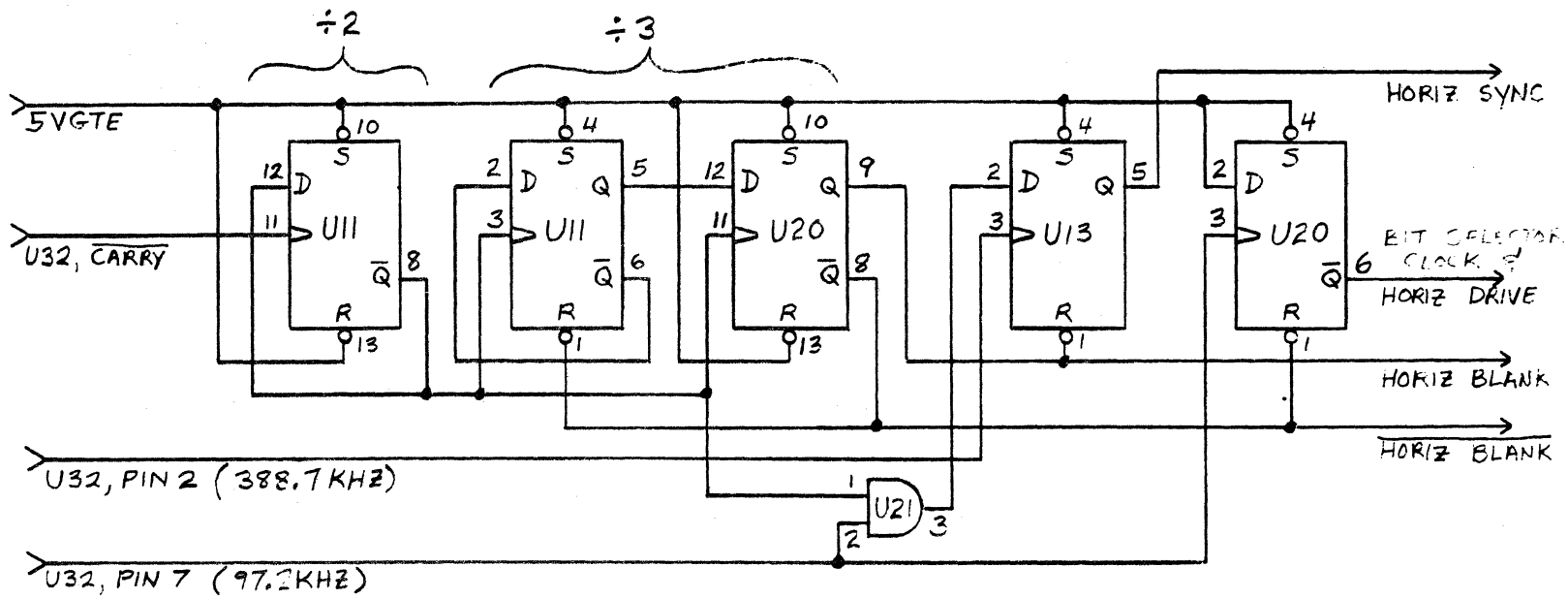


FIGURE 1

TW 11-15-77



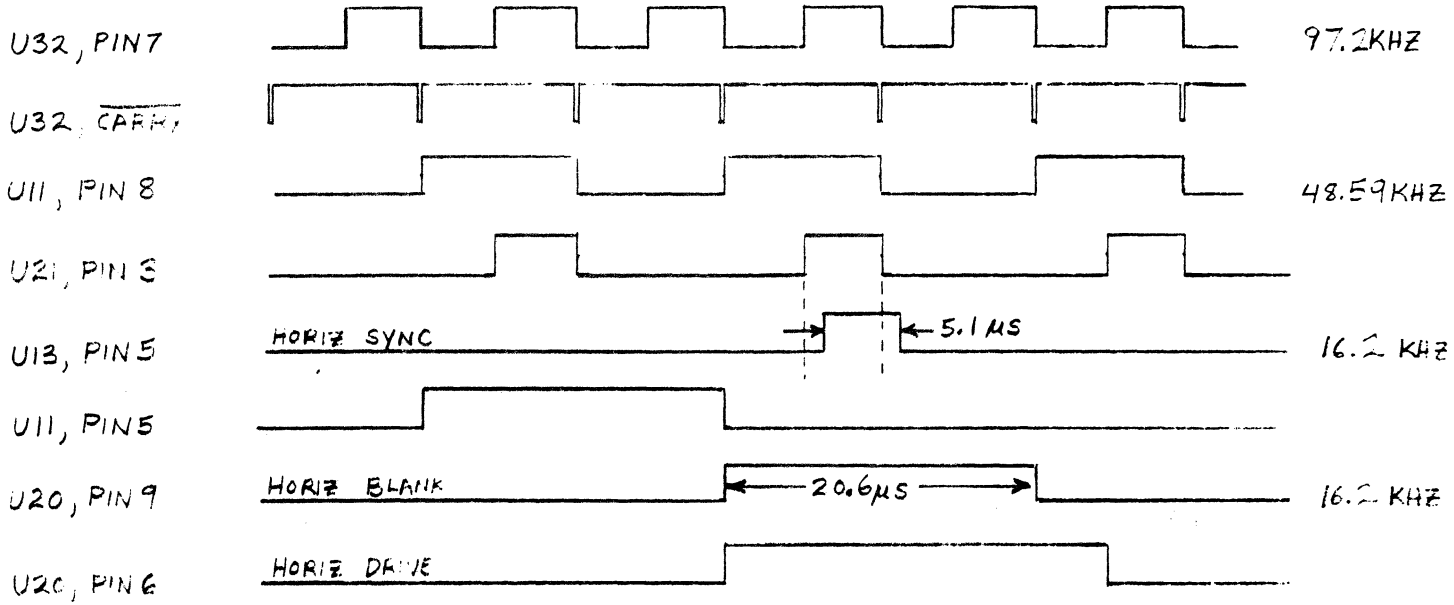


FIGURE 2

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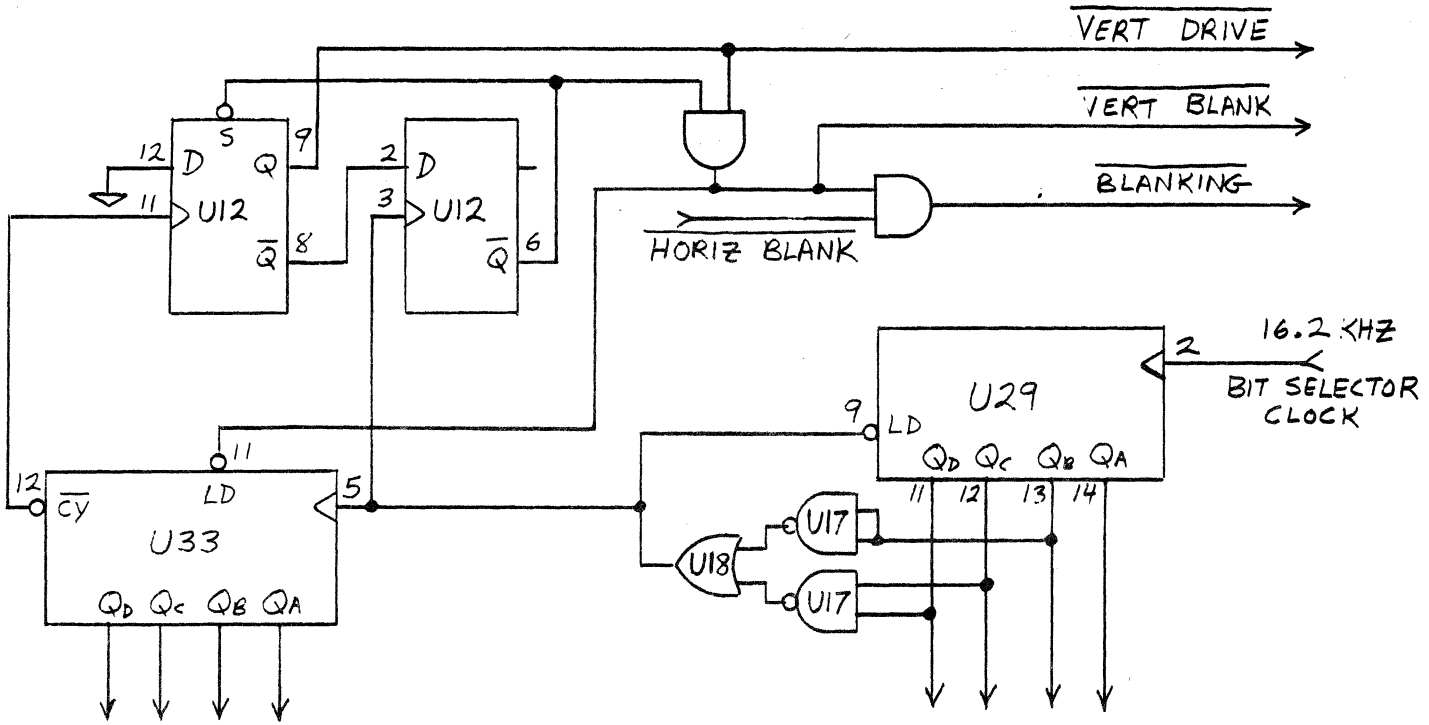
VERT DRIVE
VERT BLANK
BLANKING
HORIZ BLANK
U12
U12
U33
U29
U17
U17
U18
16.2 KHZ
BIT SELECTOR CLOCK
LD
CY
QD QC QB QA

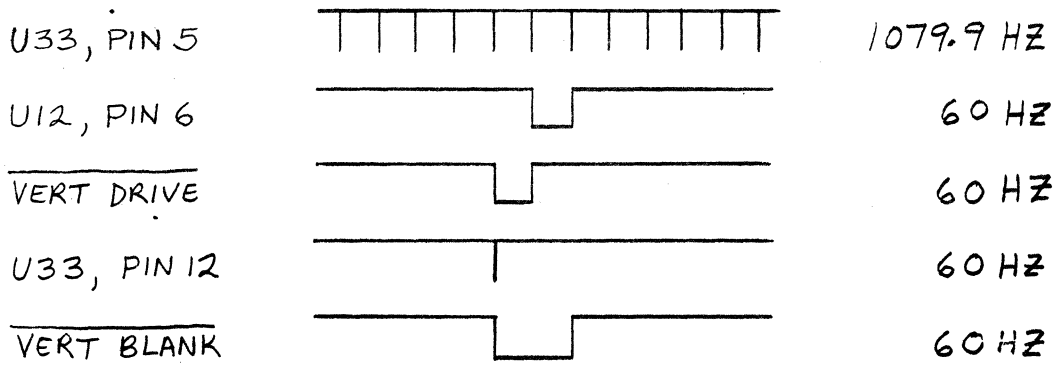
U33, PIN 5
1079.9 HZ
U12, PIN 6
60 HZ
VERT DRIVE
60 HZ
U33, PIN 12
60 HZ
VERT BLANK
60 HZ

FIGURE 3

REVISIONS			
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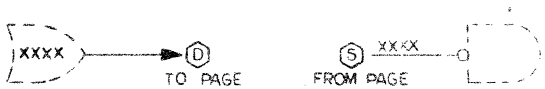
TITLE	PAGE	REV	DATE	BY
	1			
LOGIC DIAGRAM: CENTRAL TIMING, HORIZ.-VERT SIGNAL GENERATORS, MEMORY ADDRESS COUNTER.	2	B	11-29-77	
LOGIC DIAGRAM CARD AND MEMORY ADDRESS BUS	3	B	11-29-77	
LOGIC DIAGRAM: READ/WRITE MEMORY.	4	A	1-3-77	
LOGIC DIAGRAM: INPUT DATA BUS, GRAPHICS GENERATOR.	5	A	1-4-77	
LOGIC DIAGRAM: ROW DOT CHARACTER GENERATOR LOGIC, MONITOR INTERFACE POWER SUPPLIES	6	B	11-29-77	
ASSEMBLY DRAWING: V81, VIDEO BOARD 1	7	B	11-29-77	

PAGE REFERENCE:



SIGNAL ORIGIN

SIGNAL DESTINATION

WHERE, D = TO PAGE
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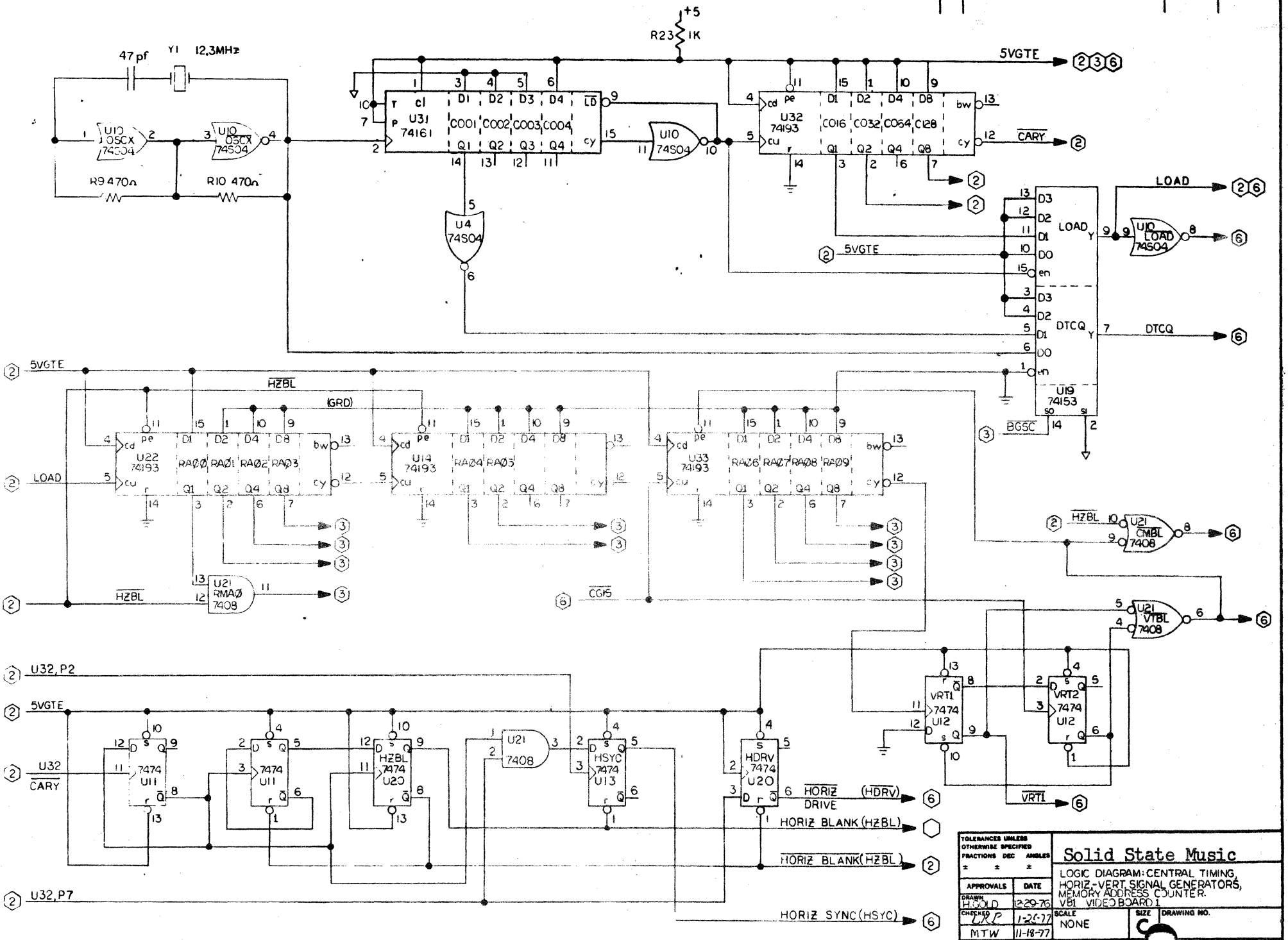

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APPROVALS	DATE
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CHECKED LRP	1-20-77
MTW	11-18-77

Solid State Music

LOGIC DIAGRAM: CENTRAL TIMING, HORIZ-VERT. SIGNAL GENERATORS, MEMORY ADDRESS COUNTER.
VB1 VIDEO BOARD 1

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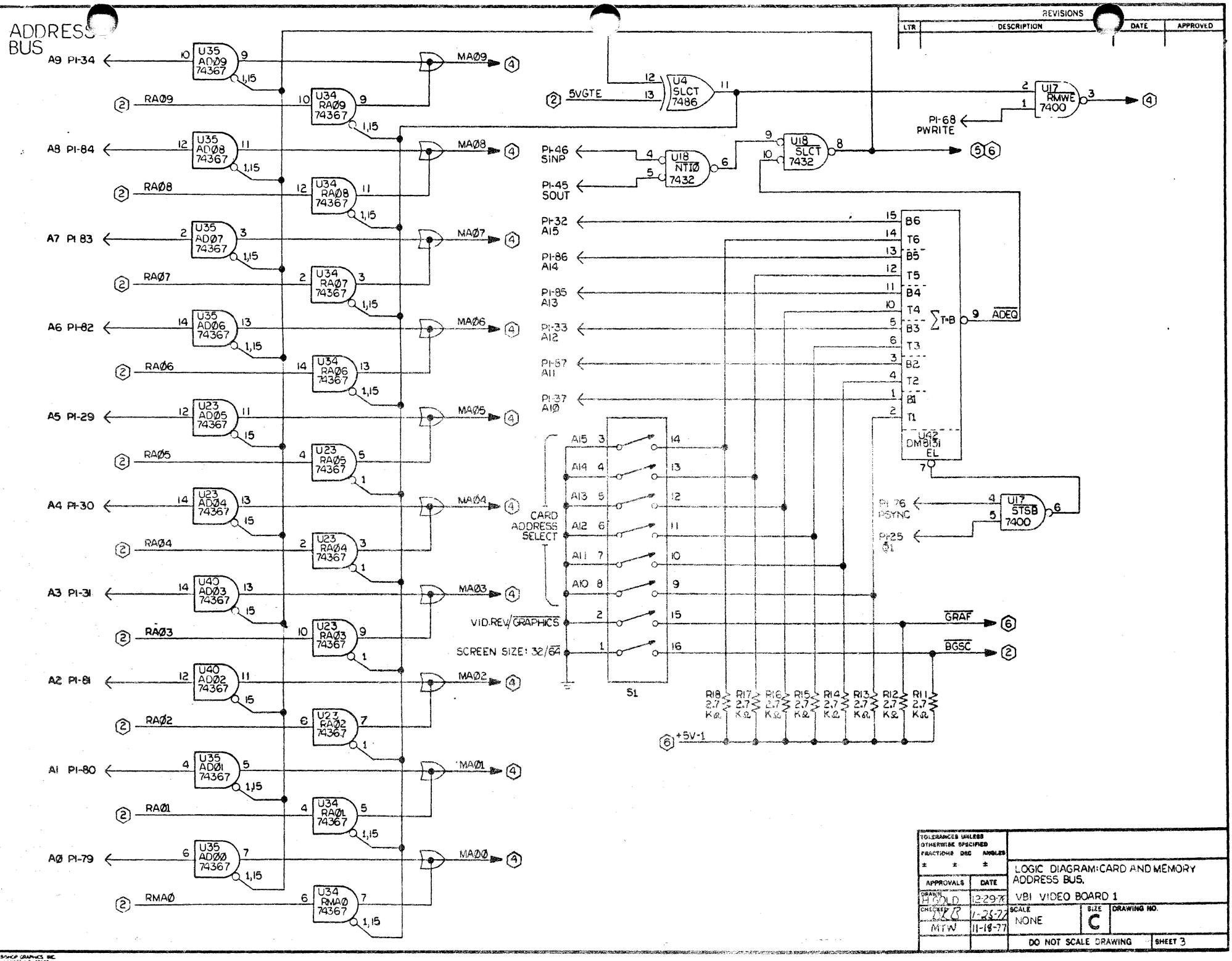

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APPROVALS / DATE	LOGIC DIAGRAM: CARD AND MEMORY ADDRESS BUS.
DRAWN H GOLD 12-29-76	VBI VIDEO BOARD 1
CHECKED DCB 1-26-77 / MTW 11-18-77	SCALE NONE · SIZE C · DRAWING NO.
DO NOT SCALE DRAWING	SHEET 3

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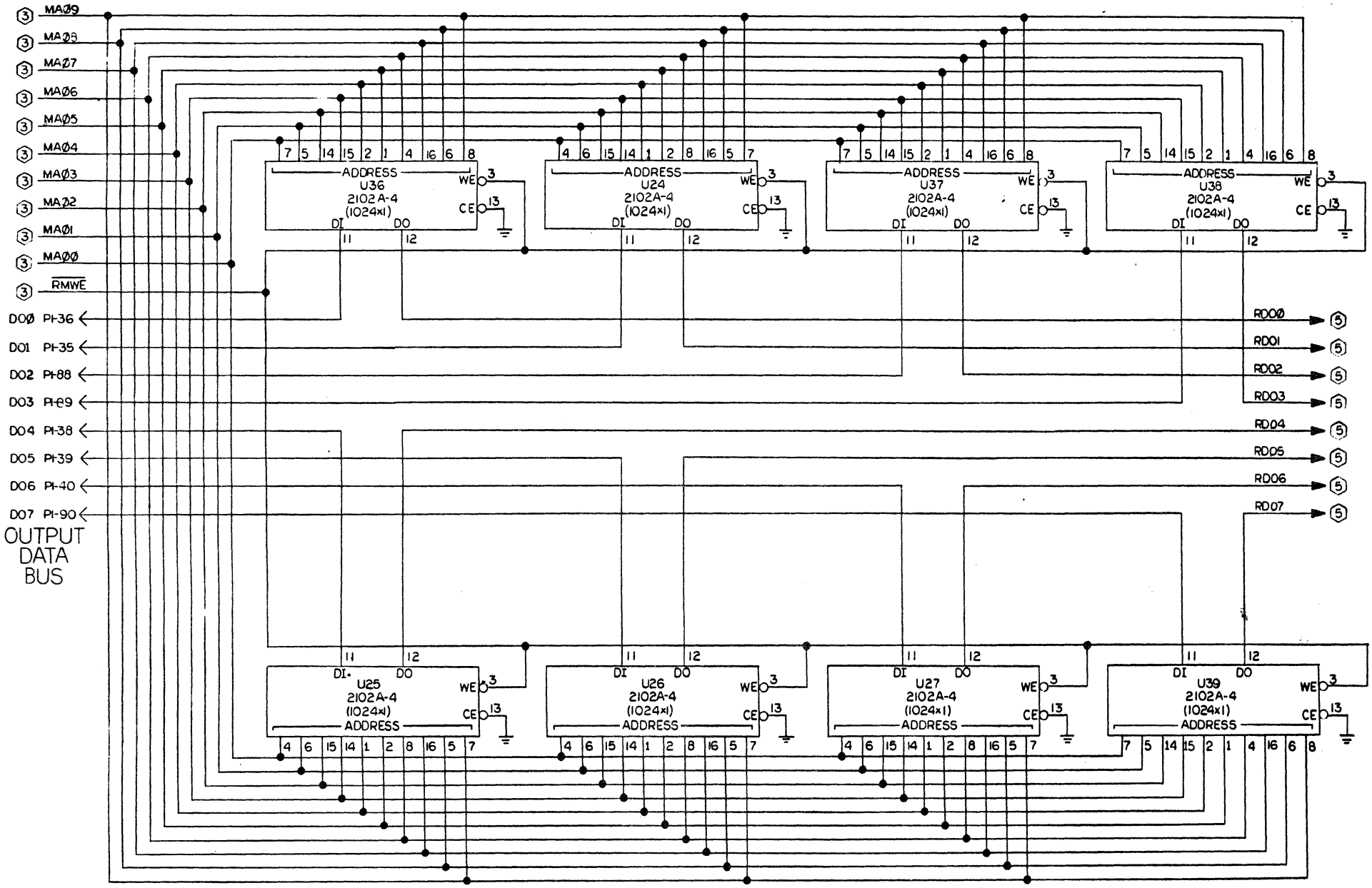

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LOGIC DIAGRAM: READ/WRITE MEMORY

VB1 VIDEO BOARD 1 Rev. 1

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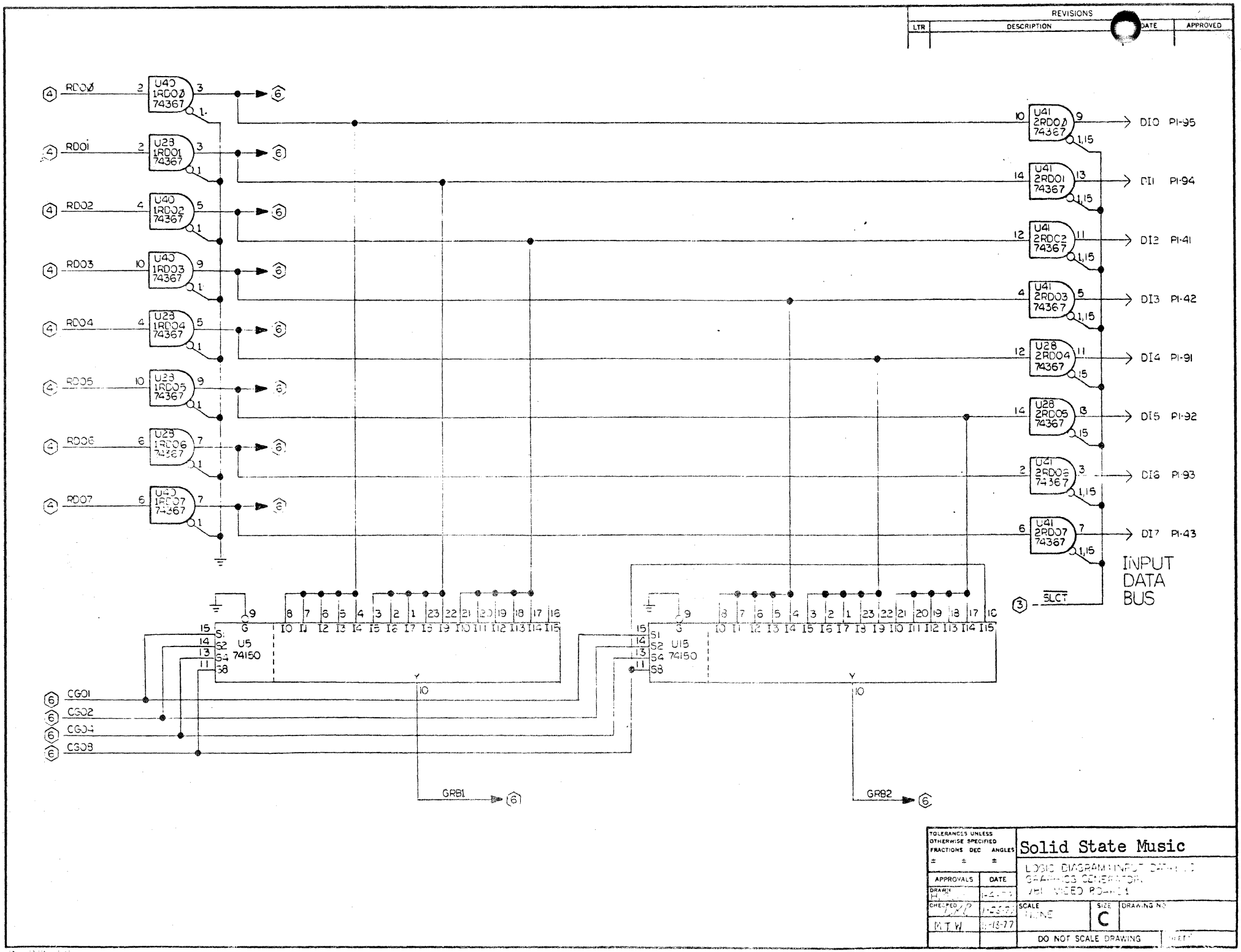
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U40 1RD02 74367
U40 1RD03 74367
U28 1RD04 74367
U28 1RD05 74367
U28 1RD06 74367
U40 1RD07 74367
U41 2RD00 74367
U41 2RD01 74367
U41 2RD02 74367
U41 2RD03 74367
U28 2RD04 74367
U28 2RD05 74367
U41 2RD06 74367
U41 2RD07 74367
DI0 P1-95
DI1 P1-94
DI2 P1-41
DI3 P1-42
DI4 P1-91
DI5 P1-92
DI6 P1-93
DI7 P1-43
INPUT DATA BUS
SLCT
U5 74150
U15 74150
CG01
CG02
CG04
CG08
GRB1
GRB2
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
APPROVALS
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DRAWN
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M T W
Solid State Music
LOGIC DIAGRAM INPUT DATA
GRAPHICS GENERATOR
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SCALE
NONE
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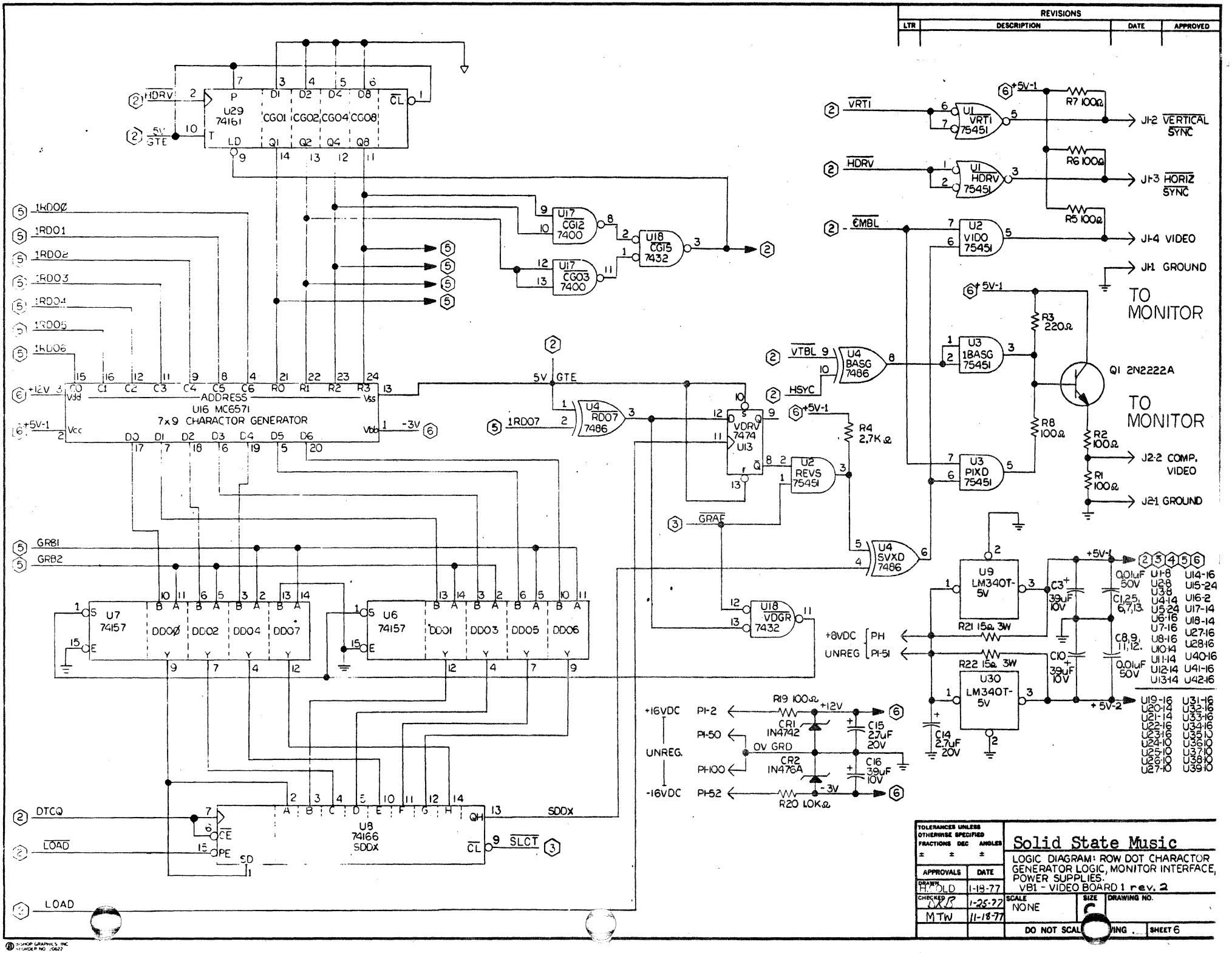
DRAWING NO
DO NOT SCALE DRAWING


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
U29 74161 CG01 CG02 CG04 CG08
HDRV
5V GTE
U17 CG12 7400
U17 CG03 7400
U18 CG15 7432
1RD00
1RD01
1RD02
1RD03
1RD04
1RD05
1RD06
1RD07
+12V
+5V-1
-3V
ADDRESS
U16 MC6571
7x9 CHARACTOR GENERATOR
U4 RD07 7486
U7 74157 DD00 DD02 DD04 DD07
U6 74157 DD01 DD03 DD05 DD06
GRB1
GRB2
U8 74166 SDDX
DTCQ
LOAD
SDDX
SLCT
VRTI
HDRV
CMBL
VTBL
HSYC
U1 VRTI 75451
U1 HDRV 75451
U2 VIDO 75451
U4 BASG 7486
U3 1BASG 75451
U3 PIXD 75451
U2 REVS 75451
U4 SVXD 7486
U18 VDGR 7432
VDRV 7474 U13
GRAF
R7 100Ω
R6 100Ω
R5 100Ω
R4 2.7K Ω
R3 220Ω
R8 100Ω
R2 100Ω
R1 100Ω
Q1 2N2222A
J1-2 VERTICAL SYNC
J1-3 HORIZ SYNC
J1-4 VIDEO
J1-1 GROUND
TO MONITOR
TO MONITOR
J2-2 COMP. VIDEO
J2-1 GROUND
U9 LM340T-5V
U30 LM340T-5V
R21 15Ω 3W
R22 15Ω 3W
C3 39uF 10V
C10 39uF 10V
C14 2.7uF 20V
C15 27uF 20V
C16 39uF 10V
0.01uF 50V
C1,2,5, 6,7,13
C8,9, 11,12,
+8VDC PH
UNREG PI-51
+16VDC PI-2
UNREG.
-16VDC PI-52
PI-50
PI-100
0V GRD
CR1 IN4742
CR2 IN476A
R19 100Ω
R20 10K Ω
+12V
-3V
+5V-2
U1-8 U14-16
U2-8 U15-24
U3-8 U16-2
U4-14 U17-14
U5-24 U18-14
U6-16 U27-16
U7-16 U28-16
U8-16 U40-16
U10-14 U41-16
U11-14 U42-16
U12-14
U13-14
U19-16 U31-16
U20-14 U32-16
U21-14 U33-16
U22-16 U34-16
U23-16 U35-10
U24-10 U36-10
U25-10 U37-10
U26-10 U38-10
U27-10 U39-10
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
APPROVALS DATE
DRAWN H. OLD 1-18-77
CHECKED 1-25-77
MTW 11-18-77
Solid State Music
LOGIC DIAGRAM: ROW DOT CHARACTOR GENERATOR LOGIC, MONITOR INTERFACE, POWER SUPPLIES.
VB1 - VIDEO BOARD 1 rev. 2
SCALE NONE
SIZE C
DRAWING NO.
DO NOT SCALE DRAWING
SHEET 6

Solid State Music

NEW SOFTWARE PACKAGE

The following software package is completely new and consists of 4 programs:

1) A Teletype Simulator program that can easily be patched-in to work with BASIC or other working software.

2) A TTY Simulator Demo program which may be used with the TTY Simulator in order to use the program without other software. The Demo includes cursor movement & video inverse capability using the following characters:

CNTRL U = UP
CNTRL D = DOWN
CNTRL F = FORWARD
CNTRL B = BACK
CNTRL H = HOME
CNTRL L = FORM FEED (blanks screen)
ESC = INVERT VIDEO

3) A Graphics Interface Subroutines program which provides the ability to generate graphics by specifying the coordinates of a particular "dot" and whether it is to be light or dark.

4) A "Doodle" demonstration program that may be used with the Graphics Interface subroutines in order to use them without other user software. "Doodle" enables a user to "paint a picture" by moving the cursor to various locations and setting each location light or dark. These functions are performed thru the use of the following characters:

W = white	D = down
Q = black	F = forward
U = up	B = back

Additionally, up to 10 pictures may be saved by typing an "S" followed by a digit from Ø to 9. The picture may be retrieved by typing a "G" followed by the digit corresponding to the desired picture. This feature does require an additional 10K of memory starting at 1000 hex, however.

PATCHING INTO 3.1 *MITS BASIC

Mits basic has two output routines, one for the main console I/O and one for their "out" command. Only the main console routine needs to be altered. In 3.1 Basic the output routine looks like the following:

ADDRESS	BYTES	MNEMONIC
Ø4 BF	DB,ØØ	Stat: IN Ø; input status
Ø4 C1	E6,8Ø	ANI 8ØH ; check dak flag
Ø4 C3	C2,BF,Ø4	JNZ stat
Ø4 C6	F1	POP PSW; restore data
Ø4 C7	D3,Ø1	OUT 1
Ø4 C9	C9	RET

In 3.2 Basic (without cassette routines), this output routine will be at about Ø4E4 Hex.

Two mnemonics that are boxed-in may be altered if you are using a Altair Rev. Ø interface instead of Rev. 1 as shown. The patch is to replace the routine called STAT with the following:

ADDRESS	BYTES	MNEMONIC
Ø4 BF	F1	PATCH: POP PSW; restore data
Ø4 CØ	B7	ORA A
Ø4 C1	C8	RZ; return if a null
Ø4 C2	C5	PUSH B
Ø4 C3	4F	MOV C, A
Ø4 C4	CD,00,3F	CALL VDTTY (see video
Ø4 C7	C1	POP B driver)
04 C8	C9	RET

Remember, when you put in the VB-1 software, Basic should not be allowed to write over it. This is done by re-assembling the VB-1 software for uncommitted memory or when MITS Basic is initialized and prints out "memory size" then type-in 16120.

* MITS, Inc., Albuquerque, New Mexico 87106

```
                ;       VIDEO BOARD DRIVER


                ;       THIS SUBROUTINE FACILITATES THE USE
                ;       OF THE SOLID STATE MUSIC VBI BOARD
                ;       AND A VIDEO DISPLAY DEVICE AS A
                ;       CONSOLE OUTPUT DEVICE.
                ;       ASCII CHARACTERS PRESENTED TO THE
                ;       SUBROUTINE IN THE C REGISTER  ARE
                ;       DISPLAYED ON THE SCREEN.  CERTAIN
                ;       CHARACTERS, LISTED BELOW , RECEIVE
                ;       SPECIAL TREATMENT.  ALL REGISTERS
                ;       ARE PRESERVED BY THIS SUBROUTINE.

                ;        LOC IS THE BEGINNING ADDRESS OF THE
                ;       SUBROUTINE.  IT MAY BE IN RAM OR ROM.

3F00            LOC     EQU     3F00H

                ;       VID IS THE BEGINNING ADDRESS ASSIGNED
                 ;      TO THE DISPLAY RAM LOCATED ON THE VBI
                ;       BOARD.

EC00            VID     EQU     0EC00H

                ;        THREE BYTES OF RAM ARE REQUIRED FOR
                ;       HOUSEKEEPING.  THESE BYTES MUST BE
                 ;      IN AN AREA UNUSED BY OTHER PROGRAMS.

3FEA            VDPTR   EQU     LAST    ;CURSOR POINTER
3FEC            VDHLD   EQU     VDPTR+2 ;CHARACTER HOLD



                ;       NON-DISPLAYABLE CHARACTERS

000C            FF      EQU     0CH     ;FORM FEED, CONTROL-L
                                        ;CLEAR SCREEN, HOME CURSOR
000A            LF      EQU     0AH     ;LINE FEED
                                        ;DOWN ONE LINE, CLEAR LINE
000D            CR      EQU     0DH     ;CARRIAGE RETURN
                                        ;MOVE CURSOR TO LEFT MARGIN


                ;       OPTIONAL CURSOR CONTROL CHARACTERS

0015            UP      EQU     15H     ;CONTROL-U
0004            DN      EQU     04H     ;CONTROL-D
0006            FW      EQU     06H     ;CONTROL-F
0002            BK      EQU     02H     ;CONTROL-B
0008            HM      EQU     08H     ;CONTROL-H
```

```
                ;       NORMAL ENTRY POINT

3F00                    ORG     LOC

3F00 E5         VDTTY:  PUSH    H       ;SAVE HL
3F01 21EA3F             LXI     H,VDPTR ;ADDR OF CURSOR POINTER

                ;       ALTERNATE ENTRY POINT
                ;       THIS ENTRY POINT MAY BE USED IF
                ;       THE CURSOR POINTER AND CHARACTER
                ;       HOLD ARE AT LOCATIONS OTHER THAN
                ;       THOSE SPECIFIED ON THIS LISTING.
                ;       THE USER MUST SUPPLY SUBROUTINE
                ;       ENTRY CODE AS FOLLOWS:
                ;ENTR:  PUSH    H       ;SAVE HL
                ;       LXI     H,PNTR  ;ADDR OF CURSOR POINTER
                ;       JMP     ALTVD   ;JOIN THIS CODE

3F04 D5         ALTVD:  PUSH    D       ;SAVE DE
3F05 C5                 PUSH    B       ;SAVE BC
3F06 F5                 PUSH    PSW     ;SAVE AF
3F07 5E                 MOV     E,M     ;LPTR
3F08 23                 INX     H       ;
3F09 7E                 MOV     A,M     ;HPTR
3F0A E603               ANI     3       ;CONVERT TO VIDEO
3F0C C6EC               ADI     VID SHR 8 ;RAM ADDRESS
3F0E 57                 MOV     D,A     ;
3F0F 23                 INX     H       ;
3F10 46                 MOV     B,M     ;CHAR UNDER CURSOR
3F11 EB                 XCHG            ;PNTR TO HL
3F12 70                 MOV     M,B     ;RESTORE PREV CHAR

                ;       IDENTIFY INPUT CHAR

3F13 79                 MOV     A,C     ;NEW  CHAR
3F14 FE0C               CPI     FF      ;
3F16 CA763F             JZ      VIDFF   ;FORM FEED
3F19 FE0D               CPI     CR      ;
3F1B CA843F             JZ      VIDCR   ;CARRIAGE RETURN
3F1E FE0A               CPI     LF      ;
3F20 CA8B3F             JZ      VIDLF   ;LINE FEED

                ;       THE FOLLOWING INSTRUCTIONS
                ;       (MARKED YYYY) MAY BE REMOVED
                ;       IF CURSOR CONTROL IS NOT
                ;       REQUIRED.

3F23 FE15               CPI     UP      ;YYYY
3F25 CAD23F             JZ      CRUP    ;YYYY
3F28 FE04               CPI     DN      ;YYYY
3F2A CAD83F             JZ      CRDN    ;YYYY
```

```
3F2D FE06              CPI     FW      ;YYYY
3F2F CA4C3F            JZ      CRRT    ;YYYY
3F32 FE02              CPI     BK      ;YYYY
3F34 CADE3F            JZ      CRLT    ;YYYY
3F37 FE08              CPI     HM      ;YYYY
3F39 CAE43F            JZ      CRHM    ;YYYY

                ;      DISPLAYABLE CHARACTER .

                ;      THE FOLLOWING INSTRUCTIONS
                ;      (MARKED XXXX) MAY BE RE MOVED
                ;      IF SENSE SWITCHES ARE NOT
                ;      TO BE USED.

                ;      CHECK FOR END LINE

3F3C 7D                MOV     A,L     ;XXXX
3F3D E63F              ANI     3FH     ;XXXX
3F3F FE3F              CPI     3FH     ;XXXX
3F41 C24B3F            JNZ     VIDB0   ;XXXX

                ;      IGNORE CHARACTER IF END OF
                ;      LINE AND SENSE SWITCH 2 OFF

3F44 DBFF              IN      0FFH    ;XXXX
3F46 E602              ANI     2       ;XXXX
3F48 CA623F            JZ      VIDRT   ;XXXX
3F4B 71        VIDB0:  MOV     M,C     ;
3F4C 010100    CRRT:   LXI     B,1

                ;      ADJUST CURSOR POINTER

3F4F 09        CRADJ:  DAD     B       ;

                ;      CHECK FOR OVERFLOW

3F50 7C                MOV     A,H     ;
3F51 FEF0              CPI     (VID+1024) SHR 8 ;
3F53 C2623F            JNZ     VIDRT   ;
3F56 26EF              MVI     H,(VID+960) SHR 8 ;
3F58 7D                MOV     A,L     ;
3F59 F6C0              ORI     0C0H    ;
3F5B 6F                MOV     L,A     ;
3F5C CDAA3F            CALL    ROLL0   ;
3F5F C3683F            JMP     VIDR1   ;

                ;      COMMON EXIT CODE
                ;      NORMALIZE CURSOR POINTER

3F62 7C        VIDRT:  MOV     A,H     ;
3F63 E603              ANI     3       ;
3F65 C6EC              ADI     VID SHR 8 ;
```

no overflow

```
3F67 67                 MOV     H,A     ;
3F68 7E         VIDRI:  MOV     A,M     ;CHAR UNDER CURSOR
3F69 367F               MVI     M,7FH   ;CURSOR
3F6B EB                 XCHG            ;PNTR TO DE
3F6C 77                 MOV     M,A     ;CHAR UNDER CURSOR
3F6D 2B                 DCX     H       ;
3F6E 72                 MOV     M,D     ;HPTR
3F6F 2B                 DCX     H       ;
3F70 73                 MOV     M,E     ;LPTR

                ;       RESTORE REGISTERS, EXIT

3F71 F1                 POP     PSW     ;
3F72 C1                 POP     B       ;
3F73 D1                 POP     D       ;
3F74 E1                 POP     H       ;
3F75 C9                 RET             ;

                ;       PROCESS FORM FEED
                ;       FILL SCREEN WITH SPACES,
                ;       MOVE CURSOR TO TOP LEFT

3F76 2100EC     VIDFF:  LXI     H,VID   ;
3F79 E5                 PUSH    H       ;
3F7A 3620       VIDFC:  MVI     M,' '   ;
3F7C 23                 INX     H       ;
3F7D 7C                 MOV     A,H     ;
3F7E FEF0               CPI     (VID+1024) SHR 8 ;
3F80 DA7A3F             JC      VIDFC   ;
3F83 E1                 POP     H       ;

                ;       PROCESS CARRIAGE RETURN
                ;       MOVE CURSOR TO BEGINNING
                ;       OF LINE

3F84 7D         VIDCR:  MOV     A,L     ;
3F85 E6C0               ANI     0C0H    ;
3F87 6F                 MOV     L,A     ;
3F88 C3623F             JMP     VIDRT   ;

                ;       PROCESS LINE FEED
                ;       MOVE CURSOR DOWN ONE LINE,
                ;       FILL NEW LINE WITH SPACES

3F8B D5         VIDLF:  PUSH    D       ;
3F8C 114000             LXI     D,64    ;
3F8F 19                 DAD     D       ;
3F90 7C                 MOV     A,H     ;
3F91 FEF0               CPI     (VID + 1024) SHR 8 ;
3F93 C2C13F             JNZ     VDLF3   ;
```

```
                ;       THE FOLLOWING INSTRUCTION
                ;       (MARKED XXXX) MAY BE REMOVED
                ;       IF SENSE SWITCHES ARE NOT
                ;       TO BE USED.

                ;       WAIT UNTIL SENSE SWITCH 1 IS ON
                ;       BEFORE ROLLING UP ONE LINE.

3F96 DBFF       VDLF2:  IN      0FFH    ;XXXX
3F98 E601               ANI     1       ;XXXX
3F9A CA963F             JZ      VDLF2   ;XXXX


                ;       ROLL THE WHOLE DISPLAY UP ONE
                ;       LINE.

3F9D CDAA3F             CALL    ROLL0   ;
3FA0 7D                 MOV     A,L     ;
3FA1 F6C0               ORI     0C0H    ;
3FA3 6F                 MOV     L,A     ;
3FA4 26EF               MVI     H,(VID+960) SHR 8 ;
3FA6 D1                 POP     D       ;
3FA7 C3623F             JMP     VIDRT   ;

                ;       ROLL SUBROUTINE

3FAA D5         ROLL0:  PUSH    D       ;
3FAB E5                 PUSH    H       ;
3FAC 1100EC             LXI     D,VID   ;
3FAF 2140EC             LXI     H,VID+64 ;
3FB2 7E         ROLL1:  MOV     A,M     ;
3FB3 12                 STAX    D       ;
3FB4 3620               MVI     M,20H   ;
3FB6 13                 INX     D       ;
3FB7 23                 INX     H       ;
3FB8 7C                 MOV     A,H     ;
3FB9 FEF0               CPI     (VID+1024) SHR 8 ;
3FBB C2B23F             JNZ     ROLL1   ;
3FBE E1                 POP     H       ;
3FBF D1                 POP     D       ;
3FC0 C9                 RET             ;
                ;       FILL NEW LINE WITH SPACES

3FC1 E5         VDLF3:  PUSH    H       ;
3FC2 7D                 MOV     A,L     ;
3FC3 E6C0               ANI     0C0H    ;
3FC5 6F                 MOV     L,A     ;
3FC6 3620       VDLF4:  MVI     M,' '   ;
3FC8 23                 INX     H       ;
3FC9 1D                 DCR     E       ;
3FCA C2C63F             JNZ     VDLF4   ;
3FCD E1                 POP     H       ;
```

```
3FCE D1                 POP     D       ;
3FCF C3623F             JMP     VIDRT   ;

                ;       THE FOLLOWING INSTRUCTIONS,
                ;       ALONG WITH THOSE MARKED
                ;       YYYY ABOVE, MAY BE REMOVED
                ;       IF CURSOR CONTROL IS NOT
                ;       REQUIRED.

                ;       CURSOR CONTROL PROCESSING

3FD2 01C0FF     CRUP:   LXI     B,-64   ;YYYY
3FD5 C34F3F             JMP     CRADJ   ;YYYY
3FD8 014000     CRDN:   LXI     B,64    ;YYYY
3FDB C34F3F             JMP     CRADJ   ;YYYY
3FDE 01FFFF     CRLT:   LXI     B,-1    ;YYYY
3FE1 C34F3F             JMP     CRADJ   ;YYYY
3FE4 210000     CRHM:   LXI     H,0     ;YYYY
3FE7 C3623F             JMP     VIDRT   ;YYYY
3FEA 00         LAST:   NOP

0000                    END
```

```
                ;       VDTTY DEMONSTRATION ROUTINE

                ;       LOC IS THE BEGINNING ADDRESS OF THE
                ;       ROUTINE.  IT MUST BE IN RAM.

3E00            LOC     EQU     3E00H

                ;       VID IS THE BEGINNING ADDRESS ASSIGNED
                ;       TO THE DISPLAY RAM LOCATED ON THE VB1
                ;       BOARD.

EC00            VID     EQU     0EC00H

                ;       VDTTY IS THE VIDEO DRIVER
                ;       ROUTINE.

3F00            VDTTY   EQU     3F00H

3E00            STACK   EQU     3E00H

                ;       NON-DISPLAYABLE CHARACTERS

001B            INV     EQU     1BH     ;ESCAAE
000C            FF      EQU     0CH     ;FORM FEED(CONTROL-L)
000A            LF      EQU     0AH     ;LINE FEED
000D            CR      EQU     0DH     ;CARRIAGE RETURN
0015            UP      EQU     15H     ;CONTROL U
0004            DN      EQU     04H     ;CONNROL D
0006            FW      EQU     06H     ;CONTROL F
0002            BK      EQU     02H     ;CONTROL B
0008            HM      EQU     08H     ;CONTROL H


3E00                    ORG     LOC

3E00 31003E     DEMO:   LXI     SP,STACK
3E03 CD4C3E     D1:     CALL    CI
3E06 E67F               ANI     7FH
3E08 4F                 MOV     C,A
3E09 FE0C               CPI     FF
3E0B CA453E             JZ      DISP1
3E0E FE0D               CPI     CR
3E10 CA453E             JZ      DISP1
3E13 FE0A               CPI     LF
3E15 CA453E             JZ      DISP1
3E18 FE15               CPI     UP
3E1A CA453E             JZ      DISP1
3E1D FE04               CPI     DN
3E1F CA453E             JZ      DISP1
3E22 FE06               CPI     FW
3E24 CA453E             JZ      DISP1
3E27 FE02               CPI     BK
3E29 CA453E             JZ      DISP1
3E2C FE08               CPI     HM
3E2E CA453E             JZ      DISP1
3E31 FE1B               CPI     INV
3E33 3A4B3E             LDA     BIT8
```

```
3E36 C2433E            JNZ     DISP
3E39 E680              ANI     80H
3E3B EE80              XRI     80H
3E3D 324B3E            STA     BIT8
3E40 C3033E            JMP     D1
3E43 B1        DISP:   ORA     C
3E44 4F                MOV     C,A
3E45 CD003F    DISP1:  CALL    VDTTY
3E48 C3033E            JMP     D1
3E4B 00        BIT8:   DB      0

               ;       CONSOLE INPUT SUBROUTINE

3E4C DB00      CI:     IN      0
3E4E E601              ANI     1
3E50 C24C3E            JNZ     CI
3E53 DB01              IN      1
3E55 C9                RET


0000                   END
```

```
                        ;       GRAPHICS INTERFACE SUBROUTINES

                        ;       THESE SUBROUTINES FACILITATE THE
                        ;       USE OF THE SOLID STATE MUSIC VB1
                        ;       BOARD AS A VIDEO DISPLAY DEVICE
                        ;       AND A GRAPHICS DISPLAY DEVICE.

                        ;       THESE SUBROUTINES TREAT THE DISPLAY
                        ;       SCREEN AS A MATRIX OF DOTS, 48 DOTS
                        ;       HIGH BY 128 DOTS WIDE.  EACH DOT IS
                        ;       SPECIFIED IN TERMS OF ITS VERTICAL
                        ;       COORDINATE(0-47) AND ITS HORIZONTAL
                        ;       COORDINATE(0-127).  DOT 0,0 IS AT
                        ;       THE LOWER LEFT CORNER OF THE SCREEN.

                        ;       THE SUBROUTINES HAVE SIMILIAR
                        ;       INTERFACES WITH THEIR CALLING
                        ;       PROGRAMS.  REGISTER B IS PRESERVED.
                        ;
                        ;       ENTRY CONDITIONS:
                        ;               H = VERTICAL COORDINATE
                        ;               L = HORIZONTAL COORDINATE
                        ;       EXIT CONDITIONS
                        ;               A = DIFFERS BY SUBROUTINE
                        ;               B = PRESERVED
                        ;               C = BIT MASK FOR SPECIFIED DOT
                        ;               DE= MEMORY ADDRESS OF DOT
                        ;               H = VERTICAL COORDINATE
                        ;               L = HORIZONTAL COORDINATE
                        ;       H AND L ARE CONVERTED(IF NECESSARY)
                        ;       MODULO 48 ANN 128 RESPECTIVELY.

                        ;       LOC IS THE BEGINNING ADDRESS OF
                        ;       THESE SUBROUTINES.  IT MAY BE IN
                        ;       RAM OR ROM.

3E80                    LOC     EQU     3E80H

                        ;       VID IS THE BEGINNING ADDRESS ASSIGNED
                        ;       TO THE DISPLAY RAM LOCATED ON THE VB1
                        ;       BOARD.

EC00                    VID     EQU     0EC00H

3E80                            ORG     LOC


                        ;       THE CHECK SUBROUTINE SETS THE ZERO
                        ;       FLAG TO INDICATE WHETHER THE SPECIFIED
                        ;       DOT IS WHITE OR BLACK.  IF THE DOT
                        ;       IS CURRENTTY WHITE THE ZERO FLAG IS
                        ;       SET ON, IF THE DOT IS BLACK THE FLAG
                        ;       IS SET OFF.  THE A REGISTER CONTAINS
                        ;       ZERO IF THE DOT IS WHITE, THE BIT
                        ;       MASK IF IT IS BLACK.

3E80 CD9A3E     CHECK:  CALL    CNVRT   ;
```

```
3E83 A1              ANA     C       ;
3E84 C9              RET             ;

                ;    THE WHITE SUBROUTINE SETS THE
                ;    SPECIFIED DOT WHITE.  REGISTER
                ;    A CONTAINS THE NEW CONTENTS OF
                ;    THE MEMORY LOCATION.

3E85 CD9A3E  WHITE:  CALL    CNVRT   ;CONVERT
3E88 E6BF            ANI     0BFH    ;CLEAR  NUSED BIT
3E8A F680            ORI     80H     ;SET GRAPHICS BIT
3E8C B1              ORA     C       ;SET THIS DOT
3E8D A9              XRA     C       ;CLEAR THIS DOT
3E8E 12              STAX    D       ;UPDATE BYTE
3E8F C9              RET             ;

                ;    THE BLACK SUBROUTINE SETS THE
                ;    SPECIFIED DOT BLACK.  REGISTER
                ;    A CONTAINS THE NEW CONTENTS OF
                ;    THE MEMORY LOCATION.

3E90 CD9A3E  BLACK:  CALL    CNVRT   ;CONVERT
3E93 E6BF            ANI     0BFH    ;CLEAR UNUSED BIT
3E95 F680            ORI     80H     ;SET GRAPHICS BIT
3E97 B1              ORA     C       ;SET THIS DOT
3E98 12              STAX    D       ;UPDATE BYTE
3E99 C9              RET             ;
                ;    THE CNVRT SUBROUTINE PERFORMS
                ;    THE COORDINATE TO ADDRESS -
                ;    BIT MASK CONVERSION.  REGISTER
                ;    A CONTAINS THE CURRENT CONNENTS
                ;    OF THE MEMORY LOCATION.

3E9A C5      CNVRT:  PUSH    B       ;

                ;    NORMALIZE THE COORDINATES

3E9B 7D              MOV     A,L     ;
3E9C E67F            ANI     7FH     ;
3E9E 6F              MOV     L,A     ;
3E9F 7C              MOV     A,H     ;
3EA0 D630    D1:     SUI     48      ;
3EA2 F2A03E          JP      D1      ;
3EA5 C630    D2:     ADI     48      ;
3EA7 FAA53E          JM      D2      ;
3EAA 67              MOV     H,A     ;
3EAB E5              PUSH    H       ;

                ;    CONVERT COORDINATES TO ADDRESS
                ;    IN DE

3EAC 44              MOV     B,H     ;
3EAD 4D              MOV     C,L     ;
3EAE 5C              MOV     E,H     ;
3EAF 1600            MVI     D,0     ;
3EB1 210100          LXI     H,1     ;
3EB4 19              DAD     D       ;
3EB5 29              DAD     H       ;
```

```
3EB6 29                 DAD     H       ;
3EB7 19                 DAD     D       ;
3EB8 29                 DAD     H       ;
3EB9 29                 DAD     H       ;
3EBA 19                 DAD     D       ;
3EBB 54                 MOV     D,H     ;
3EBC 7D                 MOV     A,L     ;
3EBD E6C0               ANI     0C0H    ;
3EBF 5F                 MOV     E,A     ;
3EC0 19                 DAD     D       ;
3EC1 19                 DAD     D       ;
3EC2 29                 DAD     H       ;
3EC3 29                 DAD     H       ;
3EC4 78                 MOV     A,B     ;
3EC5 94                 SUB     H       ;
3EC6 47                 MOV     B,A     ;
3EC7 3EC0               MVI     A,(VID+960) AND 0FFH
3EC9 93                 SUB     E       ;
3ECA 5F                 MOV     E,A     ;
3ECB 3EEF               MVI     A,(VID+960) SHR 8
3ECD 9A                 SBB     D       ;
3ECE 57                 MOV     D,A     ;
3ECF 79                 MOV     A,C     ;
3ED0 1F                 RAR             ;
3ED1 B3                 ORA     E       ;
3ED2 5F                 MOV     E,A

                ;       GENERATE BIT MASK

3ED3 79                 MOV     A,C     ;
3ED4 1F                 RAR             ;
3ED5 78                 MOV     A,B     ;
3ED6 17                 RAL             ;
3ED7 4F                 MOV     C,A     ;
3ED8 0600               MVI     B,0     ;
3EDA 21E43E             LXI     H,DTAB  ;
3EDD 09                 DAD     B       ;
3EDE 7E                 MOV     A,M

                ;       PREPARE FOR EXIT

3EDF E1                 POP     H       ;
3EE0 C1                 POP     B       ;
3EE1 4F                 MOV     C,A     ;
3EE2 1A                 LDAX    D       ;
3EE3 C9                 RET             ;

3EE4 04         DTAB:   DB      04H
3EE5 20                 DB      20H
3EE6 02                 DB      02H
3EE7 10                 DB      10H
3EE8 01                 DB      01H
3EE9 08                 DB      08H

0000                    END
```

```
                ;       DOODLE (GRAPHICS DEMO)

EC00            VID     EQU     0EC00H
3E00            STACK   EQU     3E00H
3E80            CHECK   EQU     3E80H
3E85            WHITE   EQU     3E85H
3E90            BLACK   EQU     3E90H


3D00            ORG     3D00H

3D00 31003E     DOODL:  LXI     SP,STACK ;
3D03 2100EC             LXI     H,VID    ;
3D06 36BF       D0:     MVI     M,0BFH   ;
3D08 23                 INX     H        ;
3D09 7C                 MOV     A,H      ;
3D0A FEF0               CPI     (VID+1024) SHR 8 ;
3D0C C2063D             JNZ     D0       ;
3D0F C3153D             JMP     D2       ;
3D12 22CD3D     D1:     SHLD    CURS     ;
3D15 2ACD3D     D2:     LHLD    CURS     ;
3D18 CD803E             CALL    CHECK    ;
3D1B 1A                 LDAX    D        ;
3D1C F680               ORI     80H      ;
3D1E 32CF3D     D3:     STA     OLD      ;
3D21 3ACF3D     D4:     LDA     OLD      ;
3D24 A9                 XRA     C        ;
3D25 12                 STAX    D        ;
3D26 0610               MVI     B,10H    ;
3D28 CDBB3D             CALL    WAIT     ;
3D2B C23A3D             JNZ     D5       ;
3D2E 3ACF3D             LDA     OLD      ;
3D31 12                 STAX    D        ;
3D32 0620               MVI     B,20H    ;
3D34 CDBB3D             CALL    WAIT     ;
3D37 CA213D             JZ      D4       ;
3D3A 3ACF3D     D5:     LDA     OLD      ;
3D3D 12                 STAX    D        ;
3D3E CDD03D             CALL    CI       ;
3D41 FE51               CPI     'Q'      ;BLACK
3D43 CA743D             JZ      BLK      ;
3D46 FE57               CPI     'W'      ;WHITE
3D48 CA7A3D             JZ      WHT      ;
3D4B FE53               CPI     'S'      ;SAVE
3D4D CA803D             JZ      SAVE     ;
3D50 FE47               CPI     'G'      ;GET
3D52 CA863D             JZ      GET      ;
3D55 2C                 INR     L        ;
3D56 FE46               CPI     'F'      ;FORWARD
3D58 CA123D             JZ      D1       ;
3D5B 2D                 DCR     L        ;
3D5C 2D                 DCR     L        ;
3D5D FE42               CPI     'B'      ;BACK
3D5F CA123D             JZ      D1       ;
3D62 2C                 INR     L        ;
3D63 24                 INR     H        ;
3D64 FE55               CPI     'U'      ;UP
3D66 CA123D             JZ      D1       ;
3D69 25                 DCR     H        ;
```

```
3D6A 25              DCR     H       ;
3D6B FE44            CPI     'D'     ;DOWN
3D6D CA123D          JZ      D1      ;
3D70 24              INR     H       ;
3D71 C31E3D          JMP     D3      ;

3D74 CD903E  BLK:    CALL    BLACK   ;
3D77 C3153D          JMP     D2      ;

3D7A CD853E  WHT:    CALL    WHITE   ;
3D7D C3153D          JMP     D2      ;

3D80 CD903D  SAVE:   CALL    NUM     ;
3D83 C38A3D          JMP     SG      ;

3D86 CD903D  GET:    CALL    NUM     ;
3D89 EB              XCHG            ;

3D8A CDAA3D  SG:     CALL    MOVE    ;
3D8D C3153D          JMP     D2      ;

3D90 CDD03D  NUM:    CALL    CI      ;
3D93 D630            SUI     '0'     ;
3D95 FA903D          JM      NUM     ;
3D98 FE0A            CPI     10      ;
3D9A F2903D          JP      NUM     ;
3D9D 67              MOV     H,A     ;
3D9E 2E00            MVI     L,0     ;
3DA0 29              DAD     H       ;
3DA1 29              DAD     H       ;
3DA2 110004          LXI     D,STORE ;
3DA5 19              DAD     D       ;
3DA6 1100EC          LXI     D,VID   ;
3DA9 C9              RET

3DAA 0604    MOVE:   MVI     B,4     ;
3DAC 1A      MV1:    LDAX    D       ;
3DAD E6BF            ANI     0BFH    ;
3DAF 77              MOV     M,A     ;
3DB0 13              INX     D       ;
3DB1 2C              INR     L       ;
3DB2 C2AC3D          JNZ     MV1     ;
3DB5 24              INR     H       ;
3DB6 05              DCR     B       ;
3DB7 C2AC3D          JNZ     MV1     ;
3DBA C9              RET             ;

3DBB C5      WAIT:   PUSH    B       ;
3DBC CDDC3D  W1:     CALL    CSTS    ;
3DBF B7              ORA     A       ;
3DC0 C2CB3D          JNZ     W2      ;
3DC3 0D              DCR     C       ;
3DC4 C2BC3D          JNZ     W1      ;
3DC7 05              DCR     B       ;
3DC8 C2BC3D          JNZ     W1      ;
3DCB C1      W2:     POP     B       ;
3DCC C9              RET             ;

3DCD 0000    CURS:   DW      0
```

```
3DCF 00        OLD:    DB      0

               ;       CONSOLE INPUT SUBROUTINE

3DD0 DB00      CI:     IN      0       ;
3DD2 E601              ANI     1       ;
3DD4 C2D03D            JNZ     CI      ;
3DD7 DB01              IN      1       ;
3DD9 E67F              ANI     7FH     ;
3DDB C9                RET             ;

               ;       CONSOLE STATUS SUUOUTINE

3DDC DB00      CSTS:   IN      0       ;
3DDE E601              ANI     1       ;
3DE0 D601              SUI     1       ;
3DE2 9F                SBB     A       ;
3DE3 C9                RET             ;

0400                   ORG     1024

0400           STORE:  DS      10240

0000                   END
```

```
;THIS SIMPLE PROGAM WAS DESIGNED TO DISPLAY
;THE OUTPUT OF THE SOLID STATE MUSIC VB1
;VIDEO INTERFACE BOARD.

;THE UPPER HALF OF THE DISPLAY SHOWS THE 64
;UNIQUE GRAPHIC CHARACTERS WHILE THE LOWER
;HALF DISPLAYS THE ASCII CHARACTER SET.

;              NOTE:TO SELECT GRAPHICS MODE THE
;                   GRAPHICS POSITION OF S1,THE
;                   DIP SWITCH,MUST BE CLOSED
;                   AND DATA BIT D7 SET TO A
;                   ONE.

;  | D0 | D3 |    THE DIFFERENT GRAPHIC CHARACTERS
;  | D1 | D4 |    ARE CREATED BY SETTING DATA BITS
;  | D2 | D5 |    D0-D5.(REFER TO FIG 1)IF THE
;                 DATA BIT IS SET TO A ONE THE COR-
;    FIG.1        RESPONDING SECTION OF THE GRAPHIC
;                 CHARACTER WILL BE BLACK. IF IT IS
;                 SET TO ZERO THAT SECTION WILL BE
;                 WHITE.

EC00            VID     EQU     0EC00H  ;VIDEO  STARTING  ADDRESS

0100                    ORG     100H
0100 2100EC             LXI     H,VID
0103 3EF0               MVI     A,0F0H
0105 06FF               MVI     B,0FFH
0107 BC         LOOP1:  CMP     H
0108 CA1001             JZ      PROG
010B 70                 MOV     M,B
010C 23                 INX     H
010D C30701             JMP     LOOP1
0110 2100EC     PROG:   LXI     H,VID
0113 0E09               MVI     C,09H
0115 3EFF               MVI     A,0FFH
0117 114000     LOOP2:  LXI     D,40H
011A 19                 DAD     D
011B 0D                 DCR     C
011C CA1C01     STUCK:  JZ      STUCK
011F 77         LOOP3:  MOV     M,A
0120 23                 INX     H
0121 23                 INX     H
0122 3D                 DCR     A
0123 1D                 DCR     E
0124 1D                 DCR     E
0125 CA1701             JZ      LOOP2
0128 C31F01             JMP     LOOP3
0000                    END
```

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