Part Number 800-1184-01
Revision 50 of 28 September 1984

Engineering Manual

for the

Sun-2/120 Backplane

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Revision History

Revision	Date	Comments
50	28 September 1984	First release of this Theory of Operation Manual.

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Preface

Purpose and Audience

The purpose of this manual is to enable Sun customers and licensors of the Sun Workstation design to understand how the backplane is used. Licensors of the Sun Workstation design should use this manual to aid them in modifying the backplane.

Summary of Contents

This manual describes the Sun-2/120' and Sun-2/170' backplanes. It details the level of compliance with the IEEE-796 Multibus specification for the P1 bus. This manual also describes the P2 configurations for both the 120 (nine-slot) and 170 (15-slot) models. Also included is a description of the pin assignments on the P1 and P2 connectors.

At the end of this manual, we have supplied a reader comment form. Please use the comment form to list errors and omissions. Your responses will help a great deal in our efforts to keep our documentation up to date.

Notations Used In This Manual

When possible, the schematics were drawn to standard drafting conventions. Signal flow is shown from left to right, and top to bottom. Connected sections of the design are logically grouped together, as much as the available space allows.

Conventions used for hardware signal names in this manual are:

- Both active-high and active-low signals are used. A signal name that is followed by a minus sign (–) indicates that the signal is active LOW (<0.4V). For example, the Column Address Strobe, M.CAS0–, is such a low-active signal.
- A signal that is *not* followed by a minus sign is understood to be a HIGH active signal (>2.0V). An example of such a signal would be the parity error signal, PARERR.
- For signals with multiple meanings or synonyms, the signal names are listed as separated by a slash (/). An example of this would be the on-board, memory expansion select signal, PM.OB–/P2. A high signal is understood to be an assertion of the P2 bus, while a low signal is an assertion of on-board status.
- Bus signals are indicated by a common prefix followed by a number. For example, a 16-bit data bus might be labelled D0, D1, D2, and so on until D15.
- A group of signals that is part of a signal vector is denoted by a common prefix separated from its suffix by a period. For example, all P1 signals start with the prefix "P1.", and P1 bus address signals are P1.A00, P1.A01, etc.

- Connector signals are distinguished by a suffix of "[]" with an optional string enclosed inside the square brackets identifying the connector name.

Components

Components in the schematics are identified by *component name* (this is also referred to as the ''body name'' in the wirelist). Components are named according to their generic or industry standard names. The way the components are drawn reflects their circuit function rather than the manufacturer's definition.

Each component carries a *location label* identifying its component type and approximate location in the schematics. Location labels consist of a letter followed by three digits. For instance, U300 is a DIP positioned on page three of the schematics.

The letter stands for the type of component, and is one of the following:

Letter	Component Type
C	Standard Capacitor
D	Diode
K	Electrolytic Capacitor
L	Inductor
X	Decoupling Capacitor
J	Jumper or Connector
R	Resistor
S	Single-in-Line Component
U	Dual-in-Line Component
P..L..	Programmable Logic Array

Programmable logic components, such as PALs and PROMs, are described in a high-level functional language from which they are translated automatically into the bit patterns for programming. Programmable logic elements are identified by name.

Chapter 1

Backplane

1.1. Overview

This manual describes the Sun 120' and 170' backplanes. The main features of the backplanes are:

- IEEE-796 bus standard compatible
- Arbitration using the *parallel priority* technique
- 20-bit address
- 8- or 16-bit data bus
- 9 slots on the 120 backplane
- 15 slots on the 170 backplane

The reader should have copies of the IEEE-796 bus specification, 120 backplane schematics, and the 170 backplane schematics.

1.2. P1 Section — Levels of Compliance

The P1 section of the Multibus complies to the IEEE-796 specification as follows:

Table 1-1: Multibus Compliance

Data Path	D16	8 or 16-bit data path
Memory Address Path	M20	20-bit memory address path
I/O Address Path	I16	8 or 16-bit I/O address path
Interrupt Attributes	V0	Non-bus-vectored interrupt requests

A parallel priority bus arbitration technique is used on both backplanes. Priorities on the 9-slot backplane are slot C9 highest, and slot C1 lowest. Priorities on the 15-slot backplane are slot C1 highest, and slot C15 lowest.

The following are deviations from the IEEE-796 specification. The first three deviations are due to the CPU in the Sun-2/120 and Sun-2/170.

1) INIT– pulse length during a reset instruction (non-power-up reset) will not meet the five-millisecond minimum. It will be 12.4 microseconds (usec).

2) INT0– through INT7– are reversed in priority as per the 68010. INT0– is not used and INT7– is the highest priority.

3) The LOCK function is not implemented.

4) The pullups on CBRQ– and BUSY– have been reduced to 320 ohms (1K in parallel with 470 ohms) so that these signals will be pulled up within 100 nsec (max bus clock of 10 MHz).

1.3. The P2 Section

The P2 section of the backplane is configured differently for the nine-slot (120) and 15-slot (170) backplanes.

1.3.1. 120 Backplane Configuration

All nine P1 slots are connected together and the P2 slots are connected as shown in Figure 1-1:

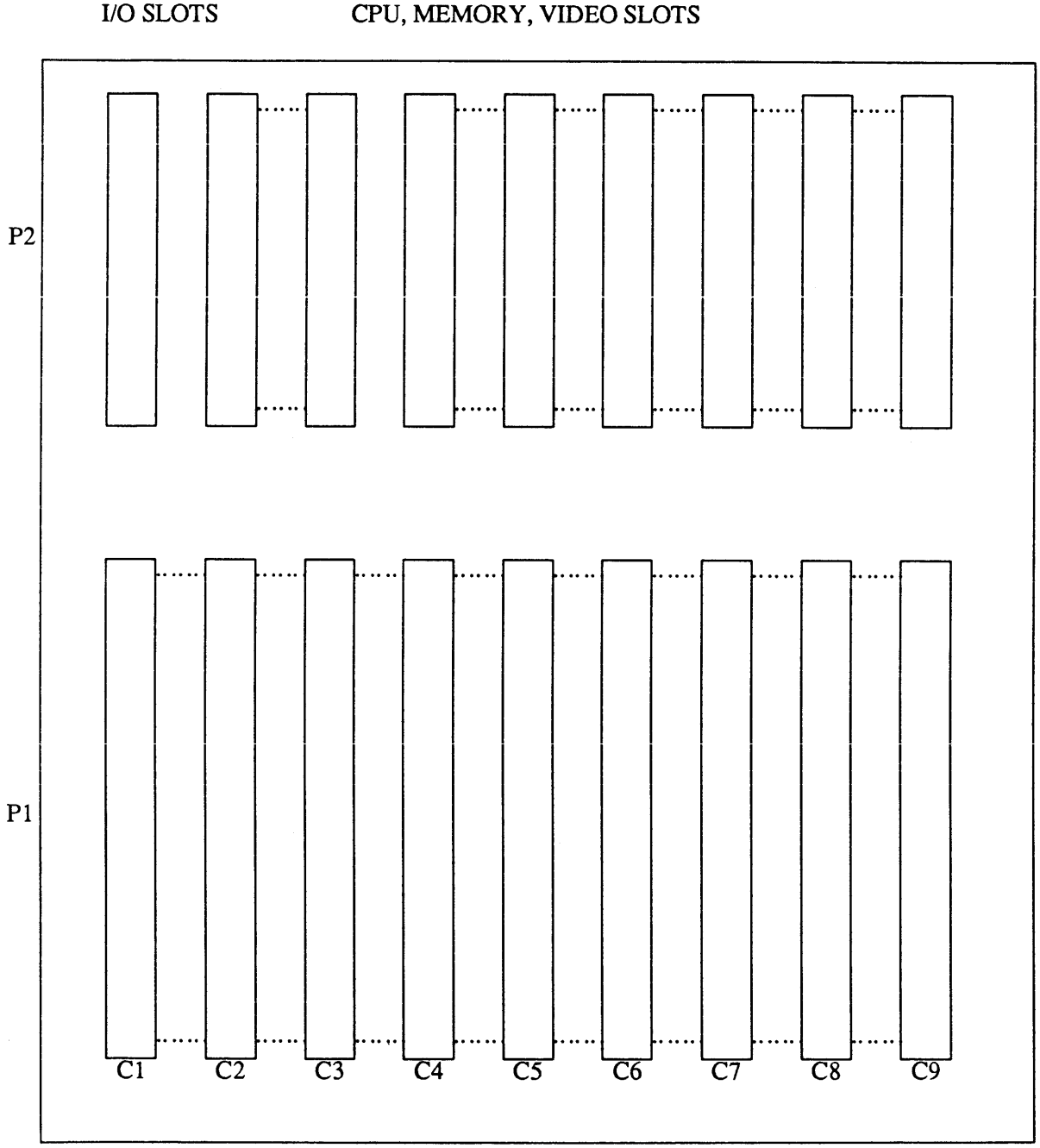


Figure 1-1: 9-Slot Backplane

1.3.2. 170 Backplane Configuration

All fifteen P1 slots are connected together and the P2 slots are connected as shown in Figure 1-2:

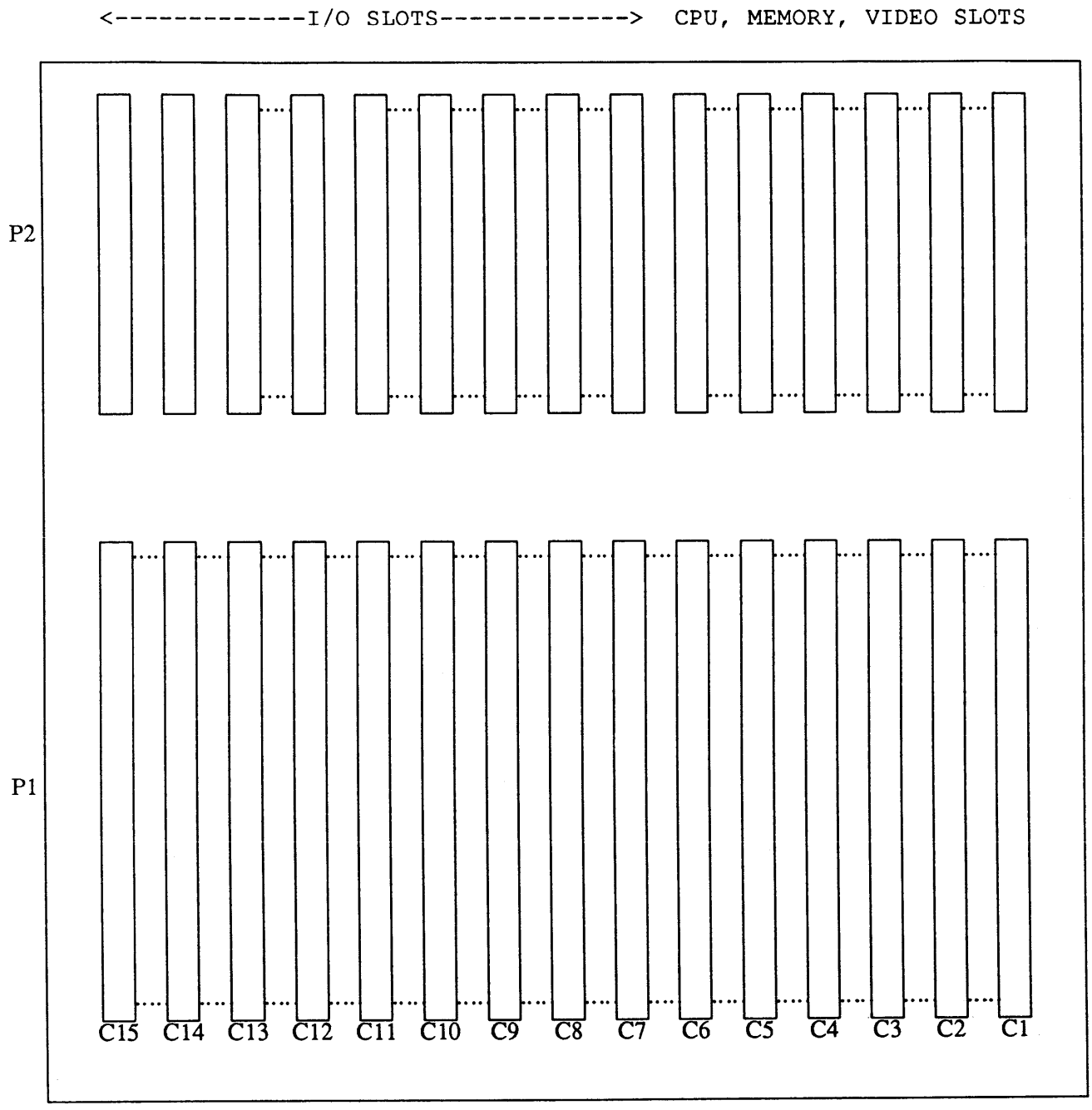


Figure 1-2: 15-Slot Backplane

1.4. P1 and P2 Signal List

The P1 slots (120 and 170) have the following pin assignments:

Table 1-2: Pin Assignments on the P1 Connector

	Pin	*Component Side*		*Pin*	*Circuit Side*	
		Mnemonic	*Description*		*Mnemonic*	*Description*
Power Supplies	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5v	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9	-5V	-5Vdc	10	-5V	-5V dc
	11	GND	Signal GND	12	GND	Signal GND
Bus Controls	13	BCLK–	Bus Clock	14	INIT–	Initialize
	15	BPRN–	Bus Pri. In	16	BPRO–	Bus Pri. Out
	17	BUSY–	Bus Busy	18	BREQ–	Bus Request
	19	MRDC–	Mem Read Cmd	20	MWTC–	Mem Write Cmd
	21	IORC–	I/O Read Cmd	22	IOWC–	I/O Write Cmd
	23	XACK–	XFER Acknowledge	24	INH1–	Inhibit 1 (disable RAM)
Bus Controls and Address	25	LOCK–	Lock	26	INH2–	Inhibit 2 (disable PROM or ROM)
	27	BHEN–	Byte High Enable	28	AD10–	Address
	29	CBRQ–	Common Bus Request	30	AD11–	Bus
	31	CCLK–	Constant Clk	32	AD12–	
	33	INTA–	Intr Acknowledge	34	AD13–	
Interrupts	35	INT6–	Parallel	36	INT7–	Parallel
	37	INT4–	Interrupt	38	INT5–	Interrupt
	39	INT2–	Requests	40	INT3–	Requests
	41	INT0–		42	INT1	
Address	43	ADRE–		44	ADRF–	
	45	ADRC–		46	ADRD–	
	47	ADRA–	Address	48	ADRB–	Address
	49	ADR8–	Bus	50	ADR9–	Bus
	51	ADR6–		52	ADR7–	
	53	ADR4–		54	ADR5–	
	55	ADR2–		56	ADR3–	
	57	ADR0–		58	ADR1–	
Data	59	DATE–		60	DATF–	
	61	DATC–		62	DATD–	
	63	DATA–	Data	64	DATB–	Data
	65	DAT8–	Bus	66	DAT9–	Bus
	67	DAT6–		68	DAT7–	
	69	DAT4–		70	DAT5–	
	71	DAT2–		72	DAT3–	
	73	DAT0–		74	DAT1–	
Power Supplies	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved, bussed	78		Reserved, bussed
	79	-12V	-12Vdc	80	-12V	-12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

The CPU, Memory, and Video board P2 slots (C4:9 for the 120, C1:6 for the 170) have the following pin assignments:

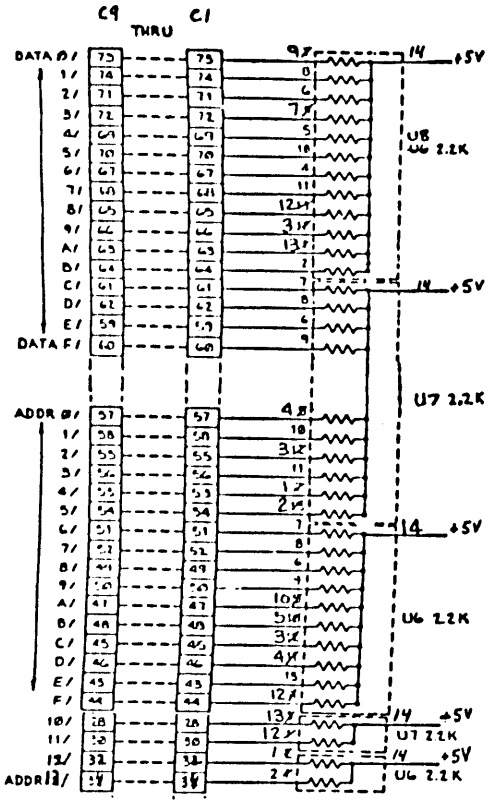
Table 1-3: Pin Assignments on the P2 Connector

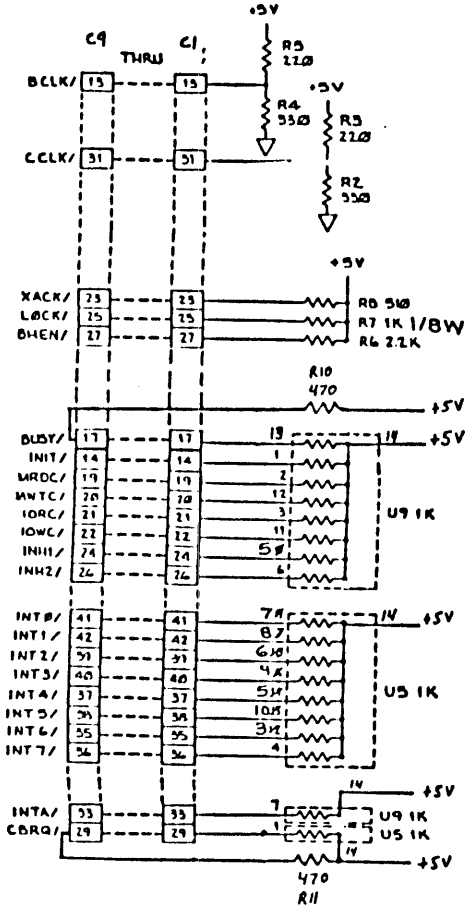
Pin	*Component Side*		*Pin*	*Circuit Side*	
	Mnemonic	*Description*		*Mnemonic*	*Description*
1	A09	Address bit 9	2	A18	Address bit 18
3	A19	Address bit 19	4	A20	Address bit 20
5	CAS–	Column Address Strobe	6	RAS–	Row Address Strobe
7	WAIT–	DTACK WAIT signal	8	WEL–	Write Enable — lower byte
9	DI00	Data In 0	10	DO00	Data Out 0
11	DI01	Data In bit 1	12	DO01	Data Out bit 1
13	A01	Address bit 1	14	A21	Address bit 21
15	DI02	Data In bit 2	16	DO02	Data Out bit 2
17	DI03	Data In bit 3	18	DO03	Data Out bit 3
19	A02	Address bit 2	20	A22	Address bit 22
21	DI04	Data In bit 4	22	DO04	Data Out bit 4
23	DI05	Data In bit 5	24	DO05	Data Out bit 5
25	A03	Address bit 3	26	REFR–	Refresh
27	DI06	Data In bit 6	28	DO06	Data Out bit 6
29	DI07	Data In bit 7	30	DO07	Data Out bit 7
31	A04	Address bit 4	32	GND	Signal GND
33	DIL	Parity In — lower byte	34	DOL	Parity Out — lower byte
35	DIU	Parity In — upper byte	36	DOU	Parity Out — upper byte
37	A05	Address bit 5	38	GND	Signal GND
39	DI08	Data In bit 8	40	DO08	Data Out bit 8
41	DI09	Data In bit 9	42	DO09	Data Out bit 9
43	A06	Address bit 6	44	GND	Signal GND
45	DI10	Data In bit 10	46	DO10	Data Out bit 10
47	DI11	Data In bit 11	48	DO11	Data Out bit 11
49	A07	Address bit 7	50	R/W–	Read — high, Write — low
51	DI12	Data In bit 12	52	DO12	Data Out bit 12
53	DI13	Data In bit 13	54	DO13	Data Out bit 13
55	A08	Address bit 8	56	WEU–	Write Enable — upper byte
57	DI14	Data In bit 14	58	DO14	Data Out bit 14
59	DI15	Data In bit 15	60	DO15	Data Out bit 15

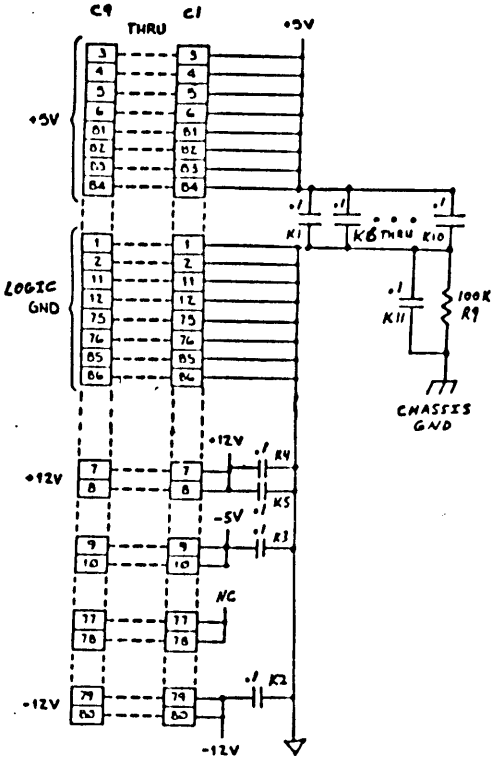
Appendix A

Backplane Schematics

P1 CONNECTIONS







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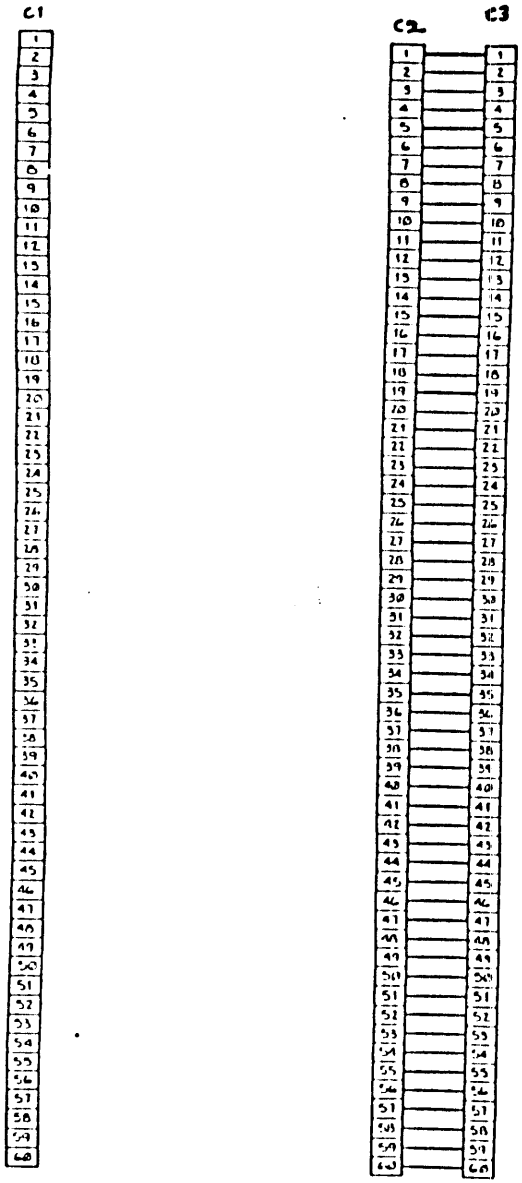
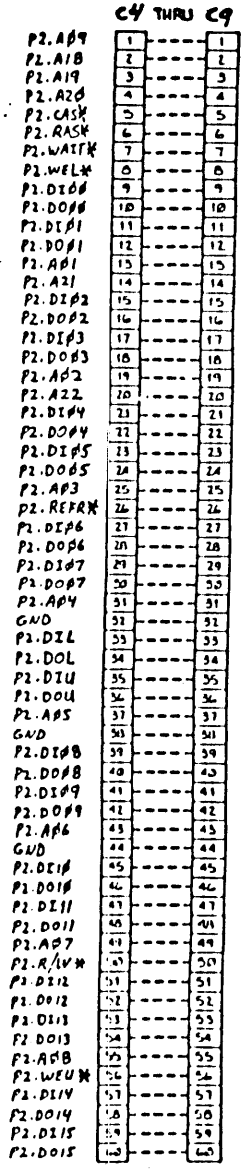
K. BIZSAK	July 11, 1984	P1 1 of 3

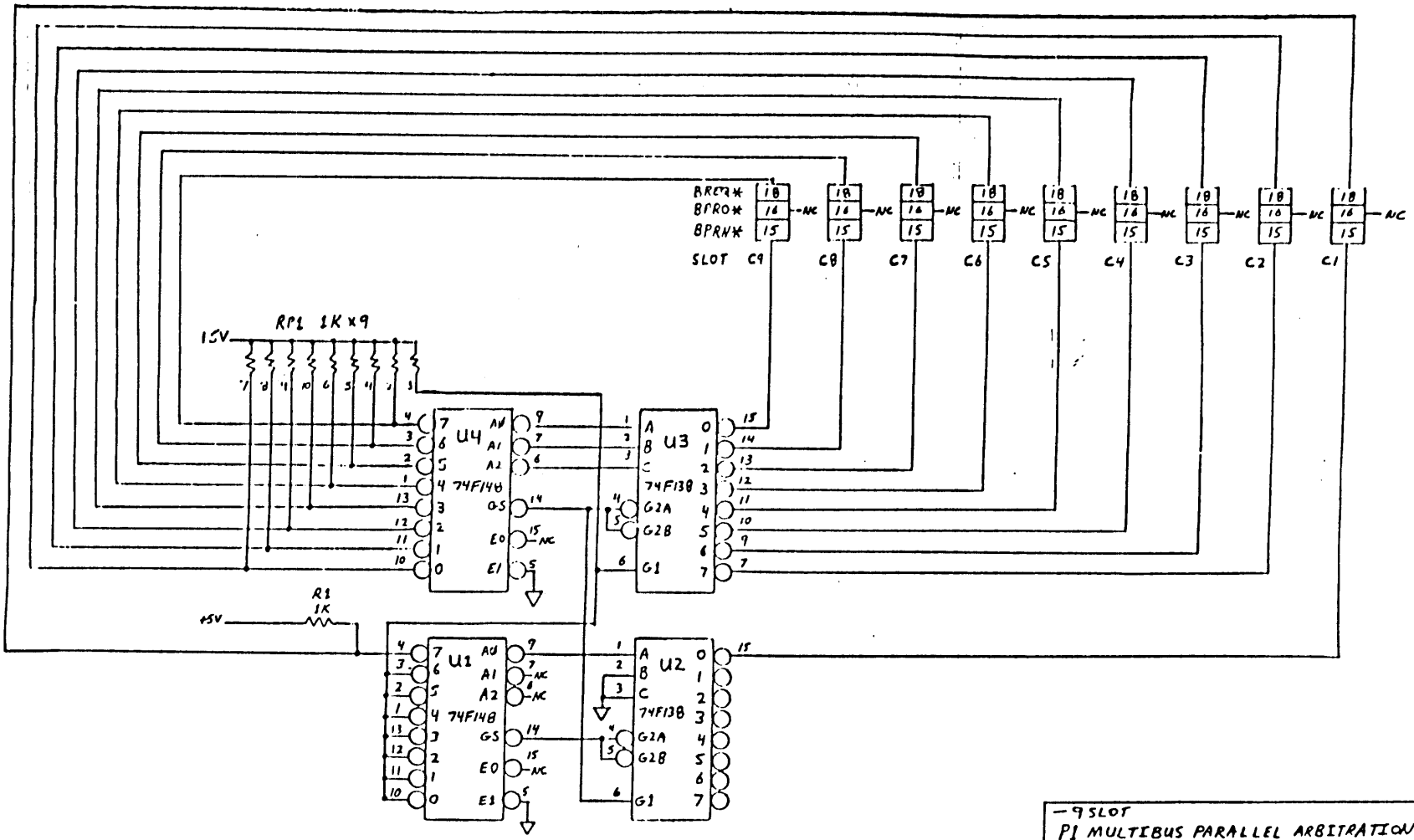


I/O P2 CONNECTOR SLOTS



CPU, MEMORY, VIDEO P2 CONNECTOR SLOTS

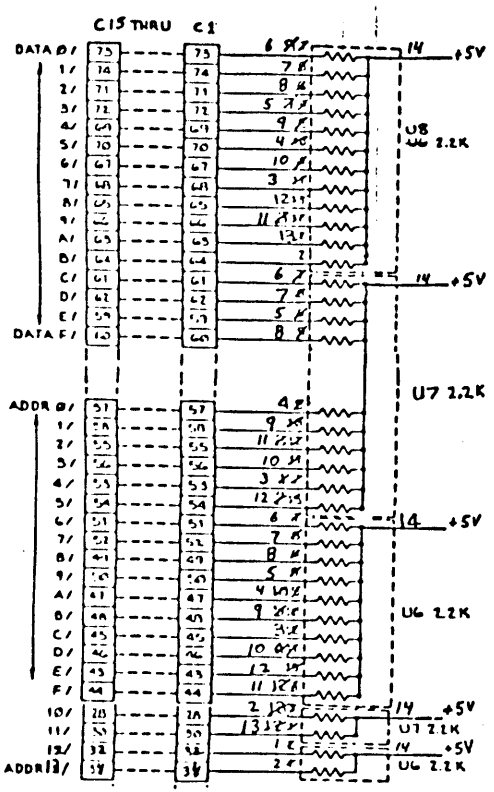
P2 MULTIBUS CONNECTIONS - 95L		
K. BIZIAK	JULY 12, 1980	PG 2 of 3

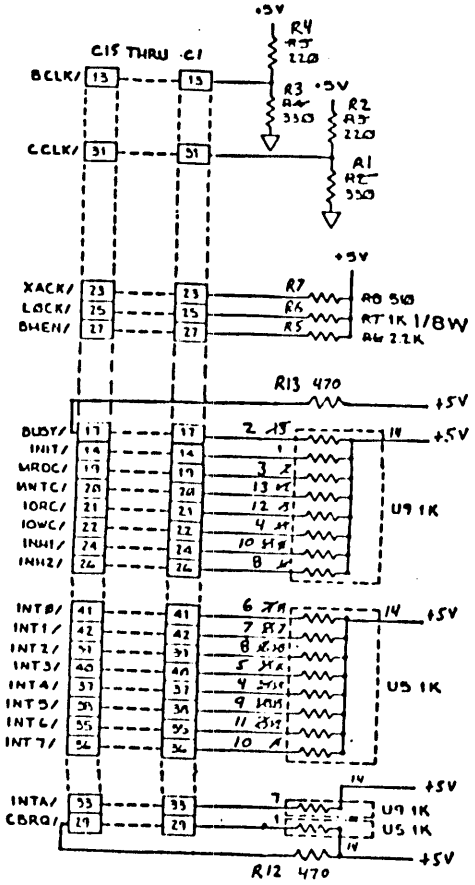


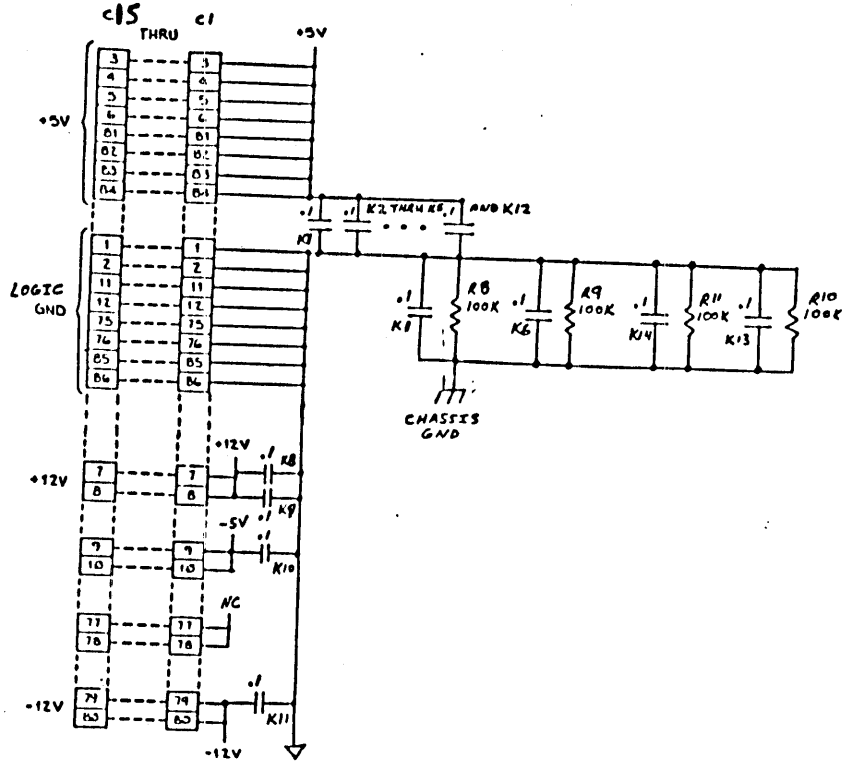
-9 SLOT
PI MULTIBUS PARALLEL ARBITRATION

K. BIZJAK	July 12, 1984	PG 3 of 3

P1 CONNECTIONS







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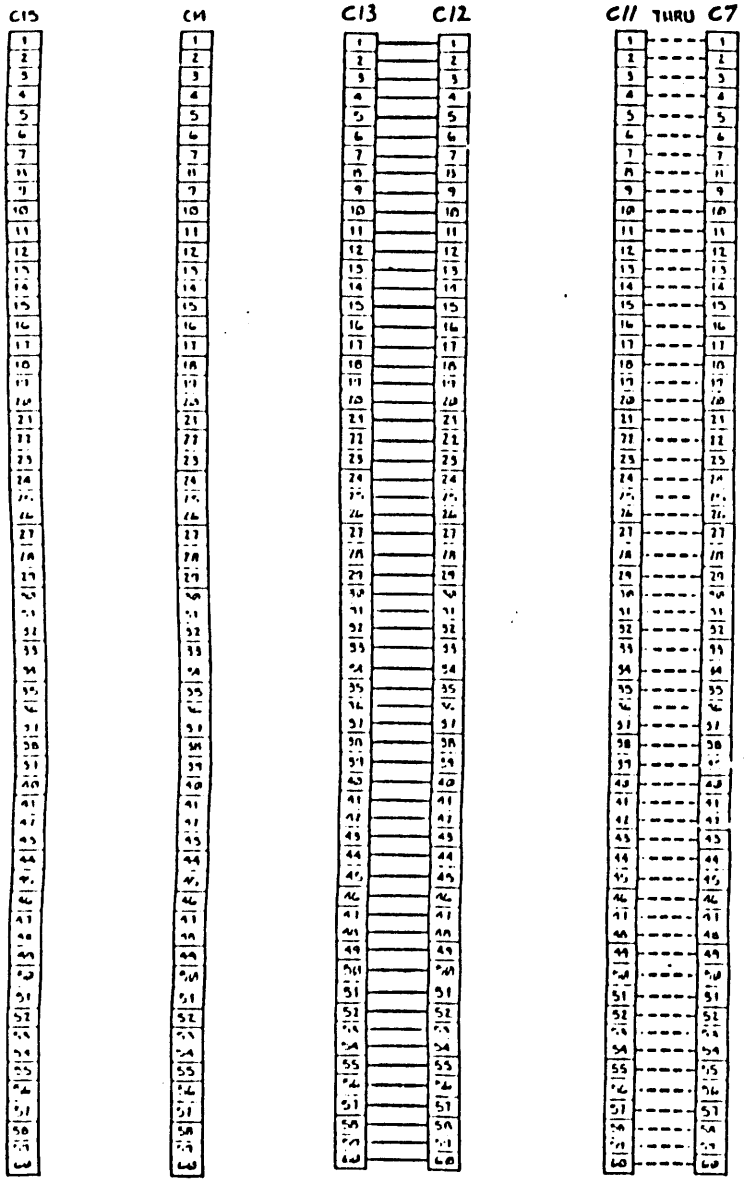
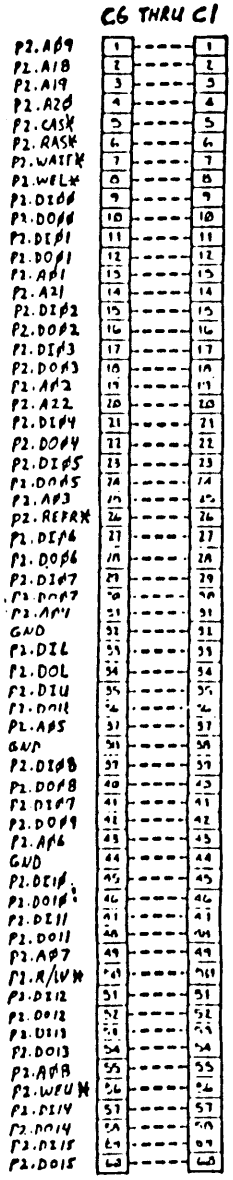
K. BEZSAK	~~Feb 13, 1985~~ 12/4 2:36 PM	16 of 3



I/O P2 CONNECTOR SLOTS



CPU, MEMORY, VIDEO P2 CONNECTOR SLOTS

P2 MULTIBUS CONNECTIONS - 15 SLOT		
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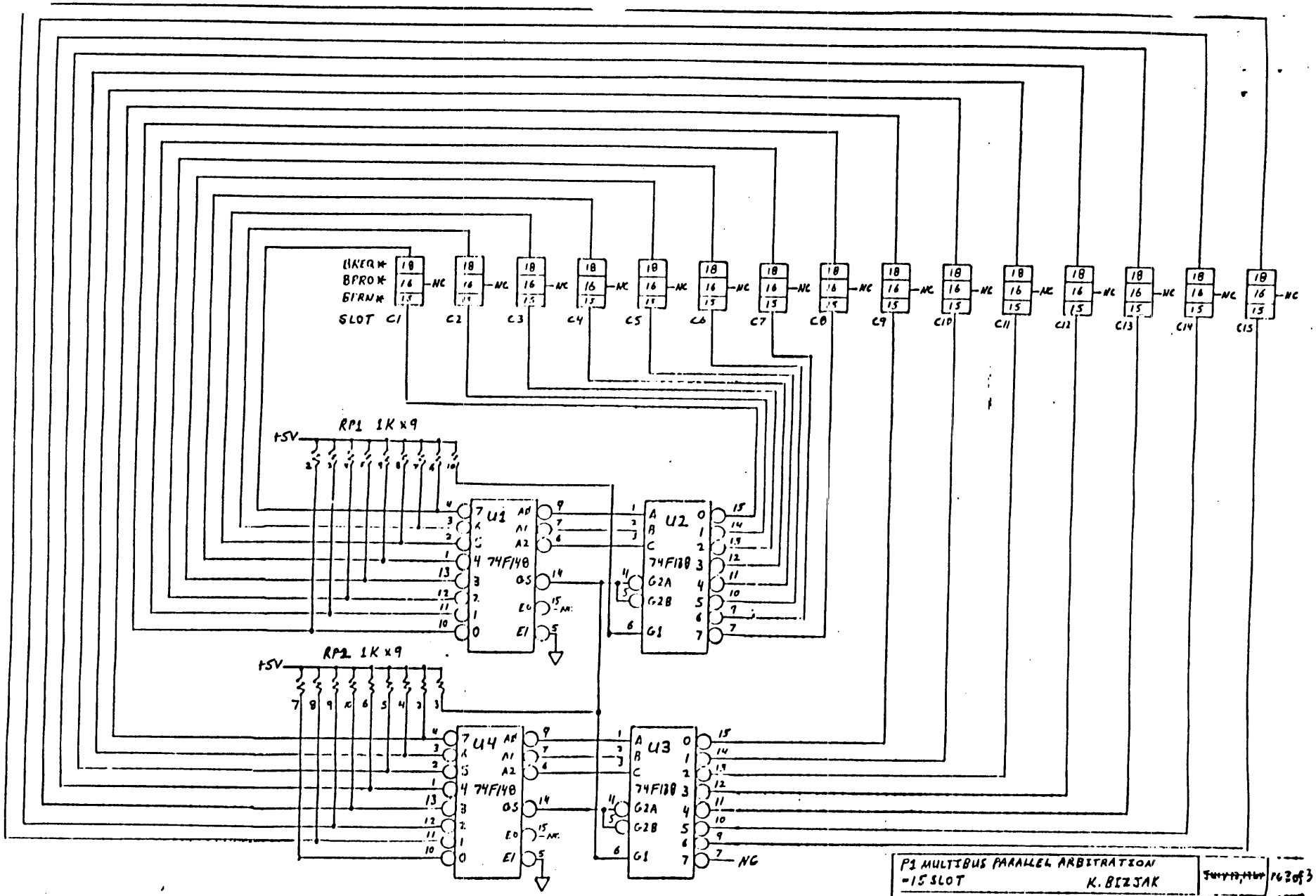

P1 MULTIBUS PARALLEL ARBITRATION
=15 SLOT
K. BIZSAK

~~Sheet 13, 1984~~ 16 of 3

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Content:

Please list errors of fact by page number and actual text of the error.

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