SYM-1 SINGLE BOARD COMPUTER

HARDWARE

THEORY OF OPERATIONS

MANUAL

By Robert A. Peck

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ACKNOWLEDGEMENTS

I wish to thank Synertek Systems Corporation for their support of this project including their permission to include the SYM-1 schematic in this book.

Introduction -

The SYM-1 Microcomputer is a well-organized unit having many unique features. The instruction manuals provided with it are certainly helpful in getting to know how to use the unit, however for the user with homebrew expansion on his mind or the OEM manufacturer adding the SYM to their systems, there seemed to be something missing. That needed item is hopefully provided here. It is intended to be a line-by-line, gate-by-gate theory of operations manual for the SYM-1 single board computer. The primary emphasis is on the digital functions.

It is intended to serve as a trouble shooting reference as well as a basis on which additional features could be added to the SYM. Various items contained herein are also covered in the SYM Reference Manual, but the viewpoint or approach here may differ. From this combination of available information, the user may gain a better nderstanding of the unit and thereby a greater degree of usefulness.

If the user of this manual has any questions about the SYM which have not been covered here, I will attempt to provide an answer. Suggestions for additions or changes to this manual would also be welcomed. If you desire a written response, please send your questions or comments along with a self-addressed stamped envelope to the address below.

For those SYM owners who need introductory software, I also offer the SYM/KIM Appendix. Send a self-addressed stamped envelope for a free reprint of the description printed in the December 1979 issue of MICRO magazine.

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P.S.

The SYM-1 Monitor Theory of Operations Manual is in process and should be ready in March, 1980. It contains a description of the SYM monitor routines supplementing the monitor listings currently in the SYM Reference Manual. It consists of a set of flow narratives for each of the monitor routines to enable the user to understand the way each subroutine is used. From a thorough knowledge of the monitor, one might save time by using more of its routines in other programs. Write for price details.

AN OVERVIEW

Since the power of the SYM-1 is derived not only by the basic hardware features which it employs, but also from the functions provided by the monitor, it seems appropriate to start an indepth analysis of the unit by examining the circuitry which controls the monitor, and how we get there in the first place.

The monitor circuit is contained in a 2332 ROM (4k by 8) located in socket U20 on the board. Further ROM space, for easy expandability, is provided in prewired sockets U21, U22, and U23. Each of these can be configured to accept a 2716, 2316B, 2332 or 2364 ROM at a future date. The address decoding and socket reconfiguration can all be accomplished by removal and repositioning of small wire jumpers strategically placed on the board so that no cutting of circuit board traces would be required to change the system.

Because of the types of ROM sockets already provided on the board, and their possible configurations, one might conceive the possibility of eventually adding four 2364 type ROM's on the board for a total of 32K by 8 of ROM continuously online. This possibility is not too far-fetched at this time considering the current offerings by Synertek Systems Corp. Specifically, the current monitor ROM is a 4K by 8 unit, and an eventual expansion to an 8K by 8 monitor is planned.

In addition to the monitor, also offerred is a Microsoft 8K basic on a pair of 4K ROM's and a resident editor assembler on a single 2364 or a pair of 2332 ROM's occupying another 8K of memory space. So even now we can fill the empty sockets with presently available firmware preconfigured for the unit, bringing it close to its total onboard capacity with ease. (One might decide to resort to some form of piggy-back arrrangement to preserve the very last ROM socket for separate use later, but thats up to the user to decide).

Address decoding for all of the memory comprising the upper 32K block of the memory space is provided by a pair of 74LS145 BCD-Decimal Decoders. These are specified as U10 and U11. The five high order address lines (A15-A11) are decoded here. Each one of the open-collector outputs of the decoders (with exception of outputs 8 and 9) is used as the active-low chip select line, either for the ROM's or for the system-dedicated RAM or I/O devices, all of which will be discussed later.

One additional level of logic is used in the production of the chip select for the ROM sockets, and that is a 7408 Quad-AND gate. The output of each of these gates is dedicated to controlling the chip select lines for each of the 4 ROM's designated U20-23. The reason for this extra logic is to take care of the power-on reset jump into the monitor circuit. This is a separate subject and the following section is dedicated entirely to the power-on reset function.

POWER-ON RESET

The monitor circuit has been written to occupy the memory space from 8000-8FFF (hex) with future versions potentially going from 8000-9FFF. At the time of power-up, the 6502 automatically puts FFFC onto the address bus to retrieve the low order byte of the reset routine address. Then it puts out FFFD onto the address bus to retrieve the high order byte of the reset routine. Next, this routine address is assembled internally and is put out onto the address bus to retrieve the first op code of the reset routine. At this time the reset routine address becomes the contents of the program counter. The address found during the initial reset sequence is 8B4A. Since this is in the monitor circuit, the monitor chip is selected. The reset routine could now proceed normally.

To access this data, since there is no ROM physically located at this address range, (FFFC,FFFD) some means must be used to provide the processor with the start address of the reset routine. This is accomplished by the presence of the active-low $\overline{\text{POR}}$ signal which is gated through U24 to form the chip select for the socket U20 which contains the monitor ROM. This allows us to retrieve the reset vector from actual locations 8FFC and 8FFD instead of FFFC and FFFD. The reset vector obtained is 8B4A, which is one of the addresses in the monitor ROM itself. Since this address in the program counter will cause the continued selection of the monitor ROM (thru pin 10 of U24) there is no further need for the $\overline{\text{POR}}$ signal to be on pin 9 of U24. Output 1 or 2 of U10 will, at this point, maintain the chip select for U20 as it represents an active low 8xxx signal.

Since the $\overline{POR}$ signal is no longer useful, we have to get rid of it. In fact, if it always stays active, we will always be selecting the monitor ROM even though we are trying to access another memory location as well. The $\overline{POR}$ line went active (low) in the first place when the RES pulse was received by 6522 #1. This action caused all of the internal registers to be set to zero. This caused the CA2 line (pin 39) to go high. This signal is combined with the $\overline{AA0}$ signal from U10 in one of the NAND gates of U8 to form $\overline{POR}$ in its active low state. At power-up, memory page A0xx is not selected, so $\overline{AA0}$ will be high.

At monitor location, 8B4A, the sequence of events is first to initialize the stack pointer to a value of FF and then to immediately store a value of CC into memory location A00C. This had two specific actions. One, the presence of A00C on the address lines forces line $\overline{AA0}$ to go low. This, through the U8 NAND gate, forces the $\overline{POR}$ signal to go high. Then when the data storage is completed, since A00C represents the location which controls the CA2 output, the data CC into that location forces the CA2 line to be held low. This in turn, again through U8, maintains $\overline{POR}$ in a disabled (high) state.

At this point, then, the program counter will still contain an address within the monitor circuits, so the program will continue normally in the absence of the $\overline{POR}$ signal.

While we're on the subject of the power-on reset, the $\overline{POR}$ signal serves one more useful purpose. In the SYM monitor the 128 bytes of RAM located within the 6532 device is initialized to hold a copy of the last 128 bytes of the monitor ROM itself. This includes the addresses required by the monitor vectors and such addresses as the reset routine, the $\overline{IRQ}$ routine, $\overline{NMI}$ routine and so forth. These are copied from the monitor ROM during the power-on reset sequence. Because this is a RAM area (A600-A67F), the user may change the monitor to vector to a user-selected address instead of the monitor selected address during the execution of various monitor routines.

After the $\overline{POR}$ has been disabled, access to locations F8xx-FFFF will cause a selection of the monitor RAM circuit. The selection is accomplished when address decoder U11 applies a chip select to 6532, effectively translating address FFFF into A67F, FFFE into A67E and so forth. If we wanted to use a different

$\overline{IRQ}$ routine, we would subsitute our routine address into locations A678 and A679 in place of the monitor $\overline{IRQ}$ routine address which is currently 800F.

During the power-up sequence, we are actually enabling the monitor ROM, and already doing a translation from FFFC to 8FFC for example, we must therefore inhibit the selection of the monitor RAM during the power up sequence. Therefore, the $\overline{POR}$ signal is used as a gating signal into U7 (74LS10) to prevent the F8xx line from becoming active.

Addressing of the Monitor RAM

There may be some desire on the part of the user to avoid having the monitor RAM accessible at the upper addresses of the memory space. Therefore, a jumper has been provided at the intersection of the points U and 22. This may be removed,disabling this function. By removing the jumper, it enables the user to install 2K of RAM in the memory space within the range of F800-FFFF. The chip select for this memory will be derived from the $\overline{F8}$ line of the U11 decoder.

One of the reasons for considering adding the 2K of RAM at this location rather than allowing access of the system RAM here might be the need to squeeze in additional memory space wherever available for larger systems. Specifically the use of the $\overline{F8}$ decode as an alternate access point for the system RAM is an excellent idea for the basic SYM as delivered, however,it uses up the entire upper 2K memory space with only 128 bytes of RAM.

To explain this further, the $\overline{F8}$ decode is taken to mean any address greater than or equal to F800. This allows the monitor RAM to respond with its contents not only at FF80-FFFF, but also at F800-F87F, F880-F8FF and 13 other address ranges in 128 byte increments from F900-FF7F. This multiple address accessibility is caused by the use of only seven address lines (A0-A6) along with the $\overline{F8}$ decode in the selection of this RAM area. This is known as "don't care" addressing, where it doesn't matter whether the unused address bits are high or low, since there is no other memory space utilized in the selected range.

There are other areas where limited address decoding has been used to simplify the construction of the SYM, and these items are shown in a separate table. If one decided to add extra RAM or I/O to the system, this table will indicate where additional address decoding will be required.

Before leaving the subject of the F800-FFFF address area, the use of FFFA thru FFFF must be mentioned. Specifically these addresses contain the $\overline{NMI}$, $\overline{RST}$ and $\overline{IRQ}$ vectors. If we disable the access to the monitor RAM by removing the U to 22 jumper, we lose access to these vectors located at A67A-A67F. Therefore, if we do add the memory as noted above (2K from F800-FFFF), we must also add a routine to our extended monitor to initialize FFFA-FFFF the same as A67A-A67F. This will maintain compatibility with existing SYM software.

Now that we've got the power-on reset sequence down, lets begin the next section taking a look at the functions of each IC in detail. This is done in a tabular fashion for convenience.

I.C. No.	Type	FUNCTION PROVIDED
U1	74LS138	Provides decoding for the lowest 8K of the address space. Decoding is accomplished in 1K increments so that each of the 8 outputs (active low) can serve as a chip select enable line for a pair of 2114 static memory chips. This chip is enabled by the combination of address lines A15, A14, and A13 entering one sement of U3. Only when all three lines A15, A14, and A13 are low is pin 12 of U3 high. Line 12 of U3 is used as the active-high enable input of U1, which defines this chip as a decoder for the lowest 8K of the memory space. Address lines A10, A11, and A12, then, select which 1K of the lowest 8K is being selected. Schematic location: F-7
U2	7404	Hex inverter, provides buffer functions at pin 34 of the 6502 and signal inversion elsewhere. Schematic location: F-7, E-7(2), D-7(2)
U3	74LS27	Triple 3-input NOR One section provides address space segmentation as noted in the section on U1 above. Section two provides the write enable signal for all RAM in the system by combination of the phase 2 and the RW signals. This signal on U3 pin 8 is inverted and buffered by one section of U2. Section three of this IC inverts and converts to TTL levels the output of the Reset one-shot timer U6. Schematic location: F-7(2), E-7
U4	74LS00	Quad 2-input NAND Section 1 is used as an enable input for IC U10. See U10 section for further details. Sections 2, 3, and 4 are used for write protect of the first, second and third 1K of memory beyond the initial 1K. The active high write signal output of U3 pin 8 is combined with the active low write protect signals $\overline{WP1K}$, $\overline{WP2K}$, $\overline{WP3K}$. If both $\overline{WPnK}$ signal and the WRITE signal are high, the output of the respective NAND will be low, forming an active low write-enable for that memory area. $\overline{WP1K}$ refers to the memory 0400-07FF, $\overline{WP2K}$ to 0800-0BFF, and $\overline{WP3K}$ protects 0C00-0FFF. Schematic locations: F-7(3), B-8.

I.C. No.	Type	FUNCTION PROVIDED
U5	6502	The CPU chip, refer to the SYM reference manual for complete data sheets and the SYM Hardware Manual for other details.
U6	555	Programmable timer. Set up as a one-shot multivibrator. Debounces the reset switch. Provides the appropriate rise-time for the reset function on the PCU and peripheral chips thru connection to U3.
U7	74LS10	Triple 3-input NAND Section 1 serves to produce the enable signal for the output of U11. Specifically output pin 12 is connected to the D input of U11. See description of U10 and U11 for further details of the use of this line as an enable. Section 2 combines the line A9, the read-write signal and the write-protect-monitor signal into a write-enable line for U27, which contains the monitor RAM. Section 3 combines the signals DBUG-ON (DBOUT) Not-Monitor ($\overline{RN}$) and SYNC to produce an active low $\overline{NMI}$ request. The combination of those signals forms the basis for the monitor trace routine function. For each op-code fetch, the SYNC line goes high. If the opcode is not being fetched from the monitor circuit, the $\overline{RN}$ line will be high. If the DEBUG function is active, the DBOUT line will be high. This combination forces $\overline{NMI}$ to go low, causing the Nonmaskable Interrupt. Like all interrupts, this one saves the processor status, but also displays the current program counter contents in the left 4 digits of the disply and a '2' in digit 5 which indicates this is a $\overline{NMI}$ interrupt. The reason for having the $\overline{RN}$ (Not-Monitor) signal here is to avoid trying to trace the operation of the processor while it is within the monitor itself. The primary problem is that the monitor must store all of the CPU status and registers, then it must create and maintain the display. If the $\overline{RN}$ signal was not included, then for every opcode fetch, there would be new $\overline{NMI}$ request generated. In other words, we would be in an endless loop and could not perform the intended functions. Schematic locations: D-7, C-5, A-8

I.C. No.	Type	FUNCTION PROVIDED
U8	7400	Quad 2-input NAND Section 1 combines the signals CA2 and AA0 into an active low output on pin 3 known as POR, which is the power-on reset. IF AA0 is high, it means that addresses A000-A7FF are not being selected. Line CA2 is an independently controllable line within the 6522 at U25. See the power-on reset section for further details. Section 2 and 3 of U8 are connected together as a bistable flip-flop and serve as a single-bit memory. The high state is DEBUG-ON, the low state is DEBUG-OFF. See U7 for further details. Section 4 of U8 forms a part of the gating for read-write signal of U25-6522. Schematic locations: D-7(2), B-5, A-6
U9	74LS04	Hex Inverter Provides various inverter/buffer functions Schematic locations: C-8 (A14 invert) B-6 (A10 invert) C-5 (WPM invert) B-5 (A9 invert)
U10,U11	74LS145	BCD to Decimal Decoder Drivers U10 allows for segmenting of the 3rd 16K memory space into 8 - 2K segments (8000-BFFF). U11 allows for segment of the 4th (uppermost) 16K memory space into 8 - 2K segments (C000-FFFF). Both U10 and U11 have 4 lines as inputs and 10 lines as outputs. The input lines are D, C, B, and A in the order of binary sigificance. The 10 output lines are designated 0-9, each of which goes low when active. Only 8 of the output lines of each is used however, specifically, 0-7 of each. This means that the D input is used as an enable for that complete 16K segment of memory in that when D is active, the binary input is 8 or more, none of the lines 0-7 will be active. For U10, the D input is controlled by the combined gating of A15 and A14 into NAND gate U4. When both are active, D goes low, enabling this decoder as noted above, from 8000-BFFF.

I.C. No.	Type	FUNCTION PROVIDED
		For U11, the D input is controlled by the combined gating of A15, A14, and $\overline{POR}$ into 3-input NAND U7. When all 3 are high, D goes low, enabling this decoder as noted above, from C000-FFFF. $\overline{POR}$ is included here because the processor is trying to access locations FFFC and FFFD during power on reset, but we have ($\overline{POR}$) enabled the monitor ROM instead. Since we actually pick up the reset vector from the monitor (8FFC and 8FFD) there must be no simultaneous access to fFFC and FFFD. So we use $\overline{POR}$ to disable this upper 16K decoder at reset. Schematic Locations: U10 - B-7 U11 - A-7
U12-19	2114	1024 by 4 Static RAM's Each of these RAM's has connections to the 10 lowest order address lines A9-A0 (allows for selection of 1024 different locations) U12, 14, 16 and U18 provide data bits D0-D3 U13, 15, 17 and U19 provide data bits D4-D7 U12 and U13 occupy address space 0000-03FF U14 and U15 " " " 0400-07FF U16 and U17 " " " 0800-0BFF U18 and U19 " " " 0C00-0FFF U12 and U13 cannot be write protected. The system stack is located in this area and must be continuously writeable. U14 and U15 derive their write-enable signal from U4 pin 6. U16 and U17 derive their write-enable signal from U4 pin 11. U18 and U19 derive their write-enable signal from U4 pin 8. Schematic locations: F-4 thru F-6
U20	2332 2364 2316B 2716	4K by 8 ROM .... OR 8K by 8 ROM .... OR 2K by 8 ROM .... OR 2K by 8 EPROM (UV Eraseable) U20 normally contains the SYM monitor ROM: it is a 2332.

I.C. No.	Type	FUNCTION PROVIDED
		U20-23 are all directly wired with low order address lines A10-A0. As such, each socket could address 8K of ROM directly. Since U20 is a 4K device, besides the enable line at pin 20, we also need on extra line to distinguish between the upper and lower 2K of the 4K contents of the ROM. Therefore, A11 is brought into pin 18 of U20. This is the point A to point 1 jumper on the SYM board. Pin 21 of U20 is wired to ground. This is to activate CS2 (chip select 2) which is active low on the SYM monitor circuit. When an expanded version of the monitor is issued (8K by 8), it will only be necessary to cut the connection from 3 to E and instead mount a jumper from 4 to E. Also jumper from 7 to 10 and 8 to 9 (the same effect as jumping from 9 to J and 10 to J). Then the expanded SUPERMON will be accessed from 8000-9FFF. U21 is factory wired for a 2716 or 2316B Addressed as C000-C7FF. U22 is factory wired for a 2716 or 2316B Addressed as C800-CFFF. U23 is factory wired for a 2716 or 2316B Addressed as D000-D7FF. Schematic locations: D-4 to D-6
U24	7408	Quad 2-input AND Each of the 4 sections is used to provide the chip select for one of the 4 onboard ROM sockets U20-23. The power-on reset jump may be wired to any one of the 4 sockets by wiring point 19 to N, P, R, or S, with the remaining points (only one to 19) wired to 20. This arranges for the power-on jump into one of the ROM's only, with the others addressed normally. Schematic locations: D-6, D-5(2), D-4
U25	SY6522	Versatile Interface Adaptor Addressed at A000-A3FF (see address decoding charts for more data on addressing). This VIA takes part in the power-on reset sequence, which is explained elsewhere. CA2 (pin 39) is used for this function. It also controls the remote start-stop function for the cassette tape unit thru CB2 (pin 19).

I.C. No.	Type	FUNCTION PROVIDED
		Interpretation of the data from the cassette tape is done by counting and timing the duration of pulses arriving at PB6 (pin 16) from the output of U25, pin 7. Schematic locations: C-6 See SYM reference manual for complete data sheets on this device.
U26	LM311	Comparator. A reference voltage of +2.5 V derived from voltage divider R95-R126 is fed into the plus input of the comparator. The audio input from the output of the tape recorder is fed to the negative input of the 311. When the input level is above 2.5V, the output of the 311 is near +5V; when the output of the tape is below 2.5 V, the output of the 311 is near ground. This circuit converts the tape waveform into square waves for more precise interpretation. Schematic location: A-6
U27	SY6532	System RAM, I/O Combination Address Space A400-A7FF (See address charts for further details) Port A, when used as an output by the monitor routines, controls the onboard display. One bit of output, when high, causes one segment of the display to light. This is a display which is multiplexed, which means that the buffered bit outputs from port A are connected to all 6 digits. (All segment A's connected together, all segment B's connected together, etc). But only one path to +5 V is provided at a time. The digit to light is chosen by Port B bits 0-3, into decoder-driver U37. Port A, when used as an input, looks at the onboard keypad. Port B acts as an output in thise case, and the presence of a key closure is sensed on Port A, then interpreted by the monitor routines. Port B, bits 4 and 7 serve as the CRT terminal output and input respectively. Port B, bits 5 and 6 serve as the TTY output and input respectively. For complete data sheets on this device, see SYM reference manula. Schematic location: B-5

I.C. No.	Type	FUNCTION PROVIDED
U28	SY6522	Versatile Interface Adaptor, user supplied Address space A800-ABFF, (see address chart). Since it is user supplied, all functions of the 6522 are open to the users own applications. Schematic location: F-3
U29	SY6522	VIA, Address space AC00-AFFF (see chart) Port A bits 0, 1, 2, and 3 are dedicated to write-protecting the monitor RAM, areas from 400-7FF, from 800-BFF, and C00-FFF. If any one of these bits is set low, the system will be unable to write into the selected area. This function may be disabled by removal of the appropriate jumpers. Port A bits 4 and 5 enable the software to call for the DEBUG function, rather than always requiring access to the DEBUG keys. If bit 4 is set low and bit 5 is high, DEBUG will be on. If bit 5 is set low and 4 high, the DEBUG function will be disabled. The reason the DEBUG function does not come up "accidentally" during the power-up is that the reset pulse on the 6522 input sets all internal registers to zero which configures this port as an input. Only an intentional setting of port A bit 4 as an output and writing a low level there will cause DEBUG to come on. In addition the reset pulse is applied to the DEBUG flip-flop through one output of U38 to assure that DEBUG will be off as the monitor is initially selected. Output lines CA2 and CB2 are reserved and buffered for use with the scope output. Finally, Port B, bits 4, 5, 6, and are buffered for uses as outputs. Schematic location: D-2
U30	7416	Hex Inverter Dedicated to driving the onboard display. Schematic location: D-2
U31-36	HP5082-7730	Seven segment displays, with decimal point. Schematic location: C-3(3), C-2(3)
U37	74145	BCD to decimal decoder driver. This one is not an "LS" type as is U10 and U11 because it is not connected to any of the chip (U4) address lines. We minimize the address line loading by the use of the "LS" circuits.

I.C. No.	Type	FUNCTION PROVIDED
		Outputs 0-5 of this chip enable digits 1-6 of the display. Output 7 is used to produce the audio outut to the input of the tape recorder. Outputs 8 and 9 are unused and represent the disabled state of the decoder when active. As with U10 and U11, the D input of the device is used as the enable (low) or disable (high) for this decoder. Schematic location: B-3
U38	7416	Hex inverter. Two parts of this chip are dedicated to the operation of the hex display. One section inverts the reset signal to turn off the DEBUG function. The next two parts of the chip are dedicated to the CRT-IN and CRT-OUT circuitry. The last section (terminals 3 and 4) are unused. Schematic locations: C-3(2), A-4(2), D-7

ADDRESS SPACE ALLOCATIONS - SYM-1 (as delivered)

Due to the use of partial address decoding, the following segments of the memory space "repeat" themselves, that is, they are accessible at more than one physical address. In the memory map which follows, these address spaces will be referenced by the letter which is shown opposite each one. This will indicate, therefore, where extra address decoding would be required to expand the use of these repetitive memory segments.

A. A000-A00F (U25) — Chip selected by address lines A0, A1, A2, A3, $\overline{A10}$ and U10 selected line $\overline{AA0}$.
As a result of the limited address decoding, address A000 is also accessible at A010, A020, A030..... A100, A110, and so forth up to A3F0, for a total of 64 different locations. Similarly, any address within the range A000-A3FF is also accessible at any one of 64 different locations.

B. A400-A41F (U27)
C. A600-A67F (U27) — Chip selected by address lines A0, A1, A2, A3, A4, A5, A6, $\overline{A10}$ and A9 along with U10 select line $\overline{AA0}$. Address range A400-A41F also is accessible at

A420-A43F
A440-A45F
etc
A500-A51F
A520-A53F

and so forth for a total of 16 areas of possible access.

Address range A600-A67F also is accessible at A680-A6FF
and A700-A77F
and A780-A7FF
and if jumper U - 22 is installed the monitor RAM is also accessible at:

F800-F87F
F880-F8FF
F900-F97F
etc

for a total of 20 different areas.

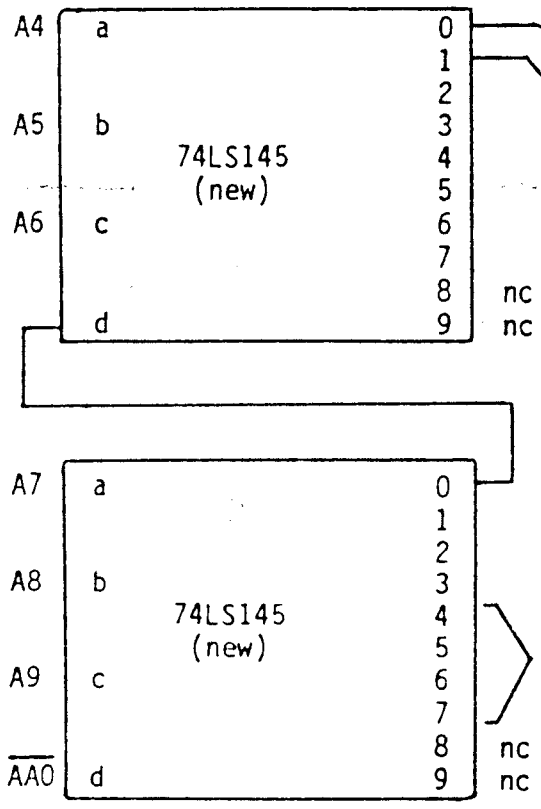
D. A800-A80F (U28) Chip selected by address line A0, A1, A2, A3, $\overline{A10}$ and decoder U10 output line $\overline{AA8}$.
As with range A000-A00F described above, each address in this range is also accessible at 64 different locations.

E. AC00-AC0F (U29) Chip selected by address lines A0, A1, A2, A3, $\overline{A10}$, and decoder U10 output line $\overline{AA8}$.
As with range A000-A00F described above, each address in this range is accessible also at 64 different locations.

SYM-1 MEMORY MAP

	FFFF	
16 REPEATS OF ADDRESS SPACE C		
	FF80	
OPTIONAL RAE (PART 2)		
	E000	
OPTIONAL BASIC (PART 2)		
	D000	
OPTIONAL BASIC (PART 1)		
	C000	
OPTIONAL RAE (PART 1)		
	B000	
64 REPEATS OF ADDRESS SPACE E		
	AC00	SPACE E = AC00-AC0F
64 REPEATS OF ADDRESS SPACE D		
	A800	SPACE D = A800-A80F
4 REPEATS OF ADDRESS SPACE C		
	A600	SPACE C = A600-A67F
16 REPEATS OF ADDRESS SPACE B		
	A400	SPACE B = A400-A41F
64 REPEATS OF ADDRESS SPACE A		
	A000	SPACE A = A000-A00F
FUTURE EXPANSION OF SUPERMON		
	9000	
SUPERMON VER·1·0 OR 1·1		
	8000	
UNUSED		
	2000	
DECODERS FOR 4 BY 1K ONBOARD		
	1000	
WRITE-PROTECTABLE RAM		
	0C00	
WRITE-PROTECTABLE RAM		
	0800	
WRITE-PROTECTABLE RAM		
	0400	
USER RAM		
	0200	
STACK		
	0100	----00FF, 00FE RESERVED FOR SUPERMON USE
USER RAM		

EXAMPLE OF ADDING MORE 6522's IN THE ADDRESS SPACE A000-A3FF



Address lines A0-A3 go directly to the new 6522, data lines and IRQ connections also. Chip enables are changed as noted here.

To Pin 214 of U25 (in place of A10). Now this VIA only accessed at A000-A00F.

To Pin 24 of new VIA. Address space A010-A01F only. Pin 23 of new VIA goes to AA0. Address lines 0, 1, 2, and 3 also go to the new VIA, BUT note that as we attempt to expand the memory space this way, we'll have to add buffers to the address lines such as 74367's (see SYM Reference Manual, Chapter 8).

Outputs 2 thru 7 of the upper 74LS145 may be used to enable additional VIA's in the same manner, each one occupying a 16 byte address space. For example, A020-A02F, A030-A03F, and so forth.

Outputs 0 thru 7 of the lower 74LS145 segments the address space into eight different groups from A000-A0FF, A100-A1FF, and so on to A700-A7FF. The way the SYM is addressed however, with the monitor I/O at A400-A41F and the monitor RAM at A600-A67F, we will not use outputs 4-7 of the lower 74LS145 because these would overlap existing onboard addresses.

APPENDIX 1 -

SYM-1 IC INTERCONNECT REFERENCE LISTING

Notes:

1. In the listing which follows, UX-Y indicates IC number "X", pin number "Y".
2. "E-NN" indicates expansion connector "E" and NN is the pin number.
3. "AA-NN" indicates the "AA" connector, "NN" the pin number.
4. "A-NN" indicates the "A" connector, "NN" the pin number.
5. "AXX" (no hyphen) indicates a connection to an Address line.

SYM•1 IC INTERCONNECT REFERENCE LISTING

IC/PIN#	POINTS TO WHICH IT IS CONNECTED				SIGNAL NAME
U1•01	(U20•23)•19	U9•1	E•M		A10
U1•02	U20•18	U10•15	U11•15	E•N	A11
U1•03	U10•14	U11•14	E•P		A12
U1•04	GND				GND
U1•05	GND				GND
U1•06	U3•12				1/4 8K SEL
U1•07	A•J				1C
U1•08	GND				GND
U1•09	A•K	E•16			18
U1•10	A•H				14
U1•11	A•F				10
U1•12	U18•8	U19•8	A•E		0C
U1•13	U16•8	U17•8	A•D		08
U1•14	U14•8	U15•8	A•C		04
U1•15	U12•8	U13•8	A•B		00
U1•16	+5V				+5V
U2•01	UNUSED				
U2•02	UNUSED				
U2•03	U5•39				PHASE•2
U2•04	U2•5				PHASE•2 NOT
U2•05	U2•4				PHASE•2 NOT
U2•06	E•U				PHASE•2 OUT
U2•07	GND				GND
U2•08	E•V				RW
U2•09	U2•10				RW•NOT
U2•10	U2•9				RW•NOT
U2•11	U5•34				RW
U2•12	U12•10	U13•10	E•Z		WRITE•NOT
U2•13	U3•8	U4•5			WRITE
U2•14	+5V				+5V
U3•01	U3•1	U4•2	U7•1	E•T	A15
U3•02	U9•13	U7•13	E•S		A14
U3•03	U3•4	U3•5	U6•3		RES
U3•04	U3•3	U3•5	U6•3		RES
U3•05	U3•3	U3•4	U6•3		RES
U3•06	U5•40	E•7			RES•NOT
U3•07	GND				GND
U3•08	U4•5	U4•13	U4•10		WRITE
U3•09	E•Y				PHASE•2•NOT
U3•10	U3•11	U2•8	E•V		RW
U3•11	U3•10	U2•8	E•V		RW
U3•12	U1•6				1/4 8K SEL
U3•13	U3•13	U10•13	U11•13	E•R	A13
U3•14	+5V				+5V
U4•01	U9•12				A14•NOT
U4•02	U3•1	U7•1	E•T		A15
U4•03	U10•12				3/4 8K SEL
U4•04	U29•3	R67	AA•W		WPIK•NOT

SYM•1 IC INTERCONNECT REFERENCE LISTING

IC/PIN#	POINTS TO WHICH IT IS CONNECTED							SIGNAL NAME
J4•05	U3•8	U4•10	U4•13					WRITE
J4•06	U14•10	U15•10						WRI•NOT
J4•07	GND							GND
J4•08	U18•10	U19•10						WR3•NOT
J4•09	U29•05	R69	AA•18					WP3K•NOT
J4•10	U3•8	U4•5	U4•13					WRITE
J4•11	U16•10	U17•10						WR2•NOT
J4•12	U29•4	R68	AA•X					WP2K•NOT
J4•13	U3•8	U4•5	U4•10					WRITE
J4•14	+5V							+5V
J5•01	GND							GND
J5•02	R74	E•2						RDY
J5•03	E•3							PHASE•1
J5•04	R73	E•4	U25•21	U28•21	U29•21			IRQ•NOT
J5•05	UNUSED							•
J5•06	U7•8	E•6						NMI•NOT
J5•07	U7•10	E•1						SYNC
J5•08	+5V							+5V
J5•09	(U12•19)•5	(U20•23)•8	(U25,28,29)•38	U27•7	E•A			A0
J5•10	(U12•19)•6	(U20•23)•7	(U25,28,29)•37	U27•6	E•B			A1
J5•11	(U12•19)•7	(U20•23)•6	(U25,28,29)•36	U27•5	E•C			A2
J5•12	(U12•19)•4	(U20•23)•5	(U25,28,29)•35	U27•4	E•D			A3
J5•13	(U12•19)•3	(U20•23)•4	U27•3	E•E				A4
J5•14	(U12•19)•2	(U20•23)•3	U27•2	E•F				A5
J5•15	(U12•19)•1	(U20•23)•2	U27•40	E•H				A6
J5•16	(U12•19)•17	(U20•23)•1	E•J					A7
J5•17	(U12•19)•16	(U20•23)•23	E•K					A8
J5•18	(U12•19)•22	U9•9	E•L					A9
J5•19	U27•38	U9•1	(U20•23)•19	U1•1	E•M			A10
J5•20	U20•18	U10•15	U11•15	U1•2	E•N			A11
J5•21	GND							GND
J5•22	U10•14	U11•14	U1•3	E•P				A12
J5•23	U3•13	U10•13	U11•13	E•R				A13
J5•24	U9•13	U7•13	U3•2	E•S				A14
J5•25	U3•1	U4•2	U7•1	E•T				A15
J5•26	(U13,15,17,19)•11	(U20•23)•17	(U25,27,28,29)•26	E•8				D7
J5•27	(U13,15,17,19)•12	(U20•23)•16	(U25,27,28,29)•27	E•9				D6
J5•28	(U13,15,17,19)•13	(U20•23)•15	(U25,27,28,29)•28	E•10				D5
J5•29	(U13,15,17,19)•14	(U20•23)•14	(U25,27,28,29)•29	E•11				D4
J5•30	(U12,14,16,18)•11	(U20•23)•13	(U25,27,28,29)•30	E•12				D3
J5•31	(U12,14,16,18)•12	(U20•23)•11	(U25,27,28,29)•31	E•13				D2
J5•32	(U12,14,16,18)•13	(U20•23)•10	(U25,27,28,29)•32	E•14				D1
J5•33	(U12,14,16,18)•14	(U20•23)•9	(U25,27,28,29)•33	E•15				D0
J5•34	U2•11							RW
J5•35	UNUSED							
J5•36	UNUSED							
J5•37	Y1	R77	C13	CR26	CR27			XTAL
J5•38	E•5							RO
J5•39	C13	U2•3						PHASE•2
J5•40	U3•6	E•7						RST

SYM•1 IC INTERCONNECT REFERENCE LISTING

IC/PIN#	POINTS TO WHICH IT IS CONNECTED				SIGNAL NAME
U6•01	GND				GND
U6•02	R72	C10	RST•SW		RST
U6•03	U3•3	U3•4	U3•5		TIMER•OU
U6•04	R70				
U6•05	C11				
U6•06	U6•7	R71	C25		
U6•07	U6•6	R71	C25		
U6•08	+5V				+5V
U7•01	U3•1	U4•2	E•T		A15
U7•02	E•18	U24•9	U8•3		POR•NOT
U7•03	E•W				RW•NOT
U7•04	U9•10				WPM
U7•05	(U12•19)•22	U9•9	E•L		A9
U7•06	U8•12				WRITE•MON
U7•07	GND				GND
U7•08	U5•6	E•6			NMI•NOT
U7•09	U8•8	U8•5	E•17		DEBUG•ON
U7•10	U5•7	E•1			SYNC
U7•11	U24•8	U20•20			RN•NOT
U7•12	U11•12				4/4 8K SEL
U7•13	U9•13	U3•2	E•S		A14
U7•14	+5V				+5V
U8•01	U10•5	U25•23	U27•37	R59	AA0•NOT
U8•02	U25•39				CA2•U25
U8•03	U7•2	U24•9	E•18		POR•NOT
U8•04	R76	U29•7	AA•20	U38•8	DBUGOFF
U8•05	U8•8	U7•9	E•17		DBUGON
U8•06	U8•9				DBUGLATCH
U8•07	GND				GND
U8•08	U8•5	U7•9	E•17		DBUGON
U8•09	U8•6				DBUGLATCH
U8•10	R75	U29•6	AA•19		DBUGON
U8•11	U27•35				RW•MON
U8•12	U7•6				WRITE•MON
U8•13	U2•10	U2•9	E•W		RW•NOT
U8•14	+5V				+5V
U9•01	(U20•23)•19	E•M			A10
U9•02	U25•24	U28•24			A10•NOT
U9•03	UNUSED				
U9•04	UNUSED				
U9•05	UNUSED				
U9•06	UNUSED				
U9•07	GND				GND

SYM•1 IC INTERCONNECT REFERENCE LISTING

IC/PIN#	POINTS TO WHICH IT IS CONNECTED	SIGNAL NAME
U9•08	U27•36	A9•NOT
U9•09	(U12•19)•22 E•L	A9
U9•10	U7•4	WPM
U9•11	R83 U29•2 AA•V	WPM•NOT
U9•12	U4•1	A14•NOT
U9•13	U7•13 U3•2 E•S	A14
U9•14	+5V	+5V
U10•01	U24•10 R79	88XX
U10•02	U24•10 R79	88XX
U10•03	UNUSED	90XX
U10•04	UNUSED	98XX
U10•05	U25•23 U27•37 R59	AA0
U10•06	U28•23 U29•23 R60	AA8
U10•07	UNUSED	B0XX
U10•08	GND	GND
U10•09	U27•37 R98	B8XX
U10•10	UNUSED	DISABLE
U10•11	UNUSED	DISABLE
U10•12	U4•3	3/4 8K SEL
U10•13	U3•13 U11•13 E•R	A13
U10•14	U11•14 U1•3 E•P	A12
U10•15	U20•18 U11•15 U1•2 E•N	A11
U10•16	+5V	+5V
U11•01	R80	C0XX
U11•02	R81	C8XX
U11•03	R82	D0XX
U11•04	UNUSED	D8XX
U11•05	UNUSED	E0XX
U11•06	UNUSED	E8XX
U11•07	UNUSED	F0XX
U11•08	GND	GND
U11•09	U27•37 R98	F8XX
U11•10	UNUSED	DISABLE
U11•11	UNUSED	DISABLE
U11•12	U7•12	4/4 8K SEL
U11•13	U3•13 U10•13 E•R	A13
U11•14	U10•14 U1•3 E•P	A12
U11•15	U20•18 U10•15 U1•2 E•N	A11
U11•16	+5V	+5V
(U12•U19)•01	(U20•23)•2 U27•40 E•H	A6
(U12•U19)•02	(U20•23)•3 U27•2 E•F	A5
(U12•U19)•03	(U20•23)•4 U27•3 E•E	A4
(U12•U19)•04	(U20•23)•5 (U25,28,29)•35 U27•4 E•D	A3
(U12•U19)•05	(U20•23)•8 (U25,28,29)•38 U27•7 E•A	A0
(U12•U19)•06	(U20•23)•7 (U25,28,29) 37 U27•6 E•B	A1

SYM•1 IC INTERCONNECT REFERENCE LISTI"G

IC/PIN#	POINTS TO WHICH IT IS CONNECTED	SIGNAL NAME
(U12•U19)•07	(U20•23)•6 (U25,28,29)•36 U27•5 E•C	A2
(U12,U13)•08	U1•15	00
(U14,U15)•08	U1•14	04
(U16,U17)•08	U1•13	08
(U18,U19)•08	U1•12	0C
(U12•U19)•09	GND	GND
(U12,U13)•10	E•Z	RAM•RW
(U14,U15)•10	U4•6	WR1•NOT
(U16,U17)•10	U4•11	WR2•NOT
(U18,U19)•10	U4•8	WR3•NOT
(U12,14,16,18)•11	(U20•23)•13 (U25,27,28,29)•30 E•8	D3
(U12,14,16,18)•12	(U20•23)•12 (U25,27,28,29)•31 E•9	D2
(U12,14,16,18)•13	(U20•23)•11 (U25,27,28,29)•32 E•10	D1
(U12,14,16,18)•14	(U20•23)•10 (U25,27,28,29)•33 E•11	D0
(U13,15,17,19)•11	(U20•23)•17 (U25,27,28,29)•26 E•12	D7
(U13,15,17,19)•12	(U20•23)•16 (U25,27,28,29)•27 E•13	D6
(U13,15,17,19)•13	(U20•23)•15 (U25,27,28,29)•28 E•14	D5
(U13,15,17,19)•14	(U20•23)•14 (U25,27,28,29)•29 E•15	D4
(U12•U19)•15	(U12•19)•22 U9•9 E•L	A9
(U12•U19)•16	(U12•19)•16 (U20•23)•23 E•K	A8
(U12•U19)•17	(U12•19)•17 (U20•23)•1 E•J	A7
(U12•U19)•18	+5V	+5V
(U20•23)•01	(U12•19)•17 E•J	A7
(U20•23)•02	(U12•19)•1 U27•40 E•H	A6
(U20•23)•03	(U12•19)•2 U27•2 E•F	A5
(U20•23)•04	(U12•19)•3 U27•3 E•E	A4
(U20•23)•05	(U12•19)•4 (U25,28,29)•35 U27•4 E•D	A3
(U20•23)•06	(U12•19)•7 (U25,28,29)•36 U27•5 E•C	A2
(U20•23)•07	(U12•19)•6 (U25,28,29)•37 U27•6 E•B	A1
(U20•23)•08	(U12•19)•5 (U25,28,29)•38 U27•7 E•A	A0
(U20•23)•09	(U13,15,17,19)•14 (U25,27,28,29)•33 E•15	D0
(U20•23)•10	(U13,15,17,19)•13 (U25,27,28,29)•32 E•14	D1
(U20•23)•11	(U13,15,17,19)•12 (U25,27,28,29)•31 E•13	D2
(U20•23)•12	GND	GND
(U20•23)•13	(U13,15,17,19)•11 (U25,27,28,29)•30 E•12	D3
(U20•23)•14	(U13,15,17,19)•14 (U25,27,28,29)•29 E•11	D4
(U20•23)•15	(U13,15,17,19)•13 (U25,27,28,29)•28 E•10	D5
(U20•23)•16	(U13,15,17,19)•12 (U25,27,28,29)•27 E•9	D6
(U20•23)•17	(U13,15,17,19)•11 (U25,27,28,29)•26 E•8	D7
U20•18	U10•15 U11•15 U1•2 E•N	A11
U21•18	GND	GND
U22•18	GND	GND
U23•18	GND	GND
U20•21	GND	GND
U21•21	+5V	+5V
U22•21	+5V	+5V
U23•21	+5V	+5V
(U20•23)•22	(U12•19)•22 U9•9 E•L	A9
(U20•23)•23	(U12•19)•16 E•K	A8
(U20•23)•24	+5V	+5V

SYM•1 IC INTERCONNECT REFERENCE LISTING

IC/PIN#	POINTS TO WHICH IT IS CONNECTED						SIGNAL NAME
U24•01	U11•3	R82					U23•SEL
U24•02	R78						
U24•03	U23•20						U23•SEL
U24•04	U11•1	R80					U21•SEL
U24•05	R78						
U24•06	U21•20						U21•SEL
U24•07	GND						GND
U24•08	U7•11	U20•8					RN•NOT
U24•09	U18•3	E•18					POR•NOT
U24•10	U10•1	U10•2					8XXX
U24•11	U22•20						U22•SEL
U24•12	R78						
U24•13	U11•2						U22•SEL
U24•14	+5V						+5V
U25•01	GND						
U25•02	A•14						
U25•03	A•4						
U25•04	A•3						
U25•05	A•2						
U25•06	A•5						
U25•07	A•6						
U25•08	A•7						
U25•09	A•8						
U25•10	A•9						
U25•11	A•10						
U25•12	A•11						
U25•13	A•12						
U25•14	A•13						
U25•16	U26•7						DATA•IN
U25•17	U3•1	U4•2	U7•1	E•T			A15
U25•18	UNUSED						
U25•19	Q27•BASEL						TAPECNTL
U25•20	+5V						+5V
U25•21	U5•4	E•4					IRQ•NOT
U25•22	U2•8	E•V					RW
U25•23	U10•5						AA0•NOT
U25•24	U9•2	U28•24					A10•NOT
U25•25	U2•6	E•U					PHASE•2
U25•26	(U13,15,17,19)•11	(U20•23)•17	(U27,28,29)•26	E•8			D7
U25•27	(U13,15,17,19)•12	(U20•23)•16	(U27,28,29)•27	E•9			D6
U25•28	(U13,15,17,19)•13	(U20•23)•15	(U27,28,29)•28	E•10			D5
U25•29	(U13,15,17,19)•14	(U20•23)•14	(U27,28,29)•29	E•11			D4
U25•30	(U13,15,17,19)•11	(U20•23)•13	(U27,28,29)•30	E•12			D3
U25•31	(U13,15,17,19)•12	(U20•23)•12	(U27,28,29)•31	E•13			D2
U25•32	(U13,15,17,19)•13	(U20•23)•11	(U27,28,29)•32	E•14			D1
U25•33	(U13,15,17,19)•14	(U20•23)•10	(U27,28,29)•33	E•15			D0
U25•34	E•7	U3•6	U5•40				RES•NOT
U25•35	(U12•19)•4	(U20•23)•5	(U28,29)•35	U27•4	E•D		A3
U25•36	(U12•19)•7	(U20•23)•6	(U[illegible]29)•36	U27•5	E•C		A2

SYM•1 IC INTERCONNECT REFERENCE LISTING

IC/PIN#	POINTS TO WHICH IT IS CONNECTED							SIGNAL NAME
U25•37	(U12•19)•6	(U20•23)•7	(U28,29)•37	U27•6	E•B			A1
U25•38	(U12•19)•5	(U20•23)•8	(U28,29)•38	U27•7	E•A			A0
U25•39	U8•2							
U25•40	GND							GND
U26•01	GND							GND
U26•02	CR28	CR29	R93	R95	R126			AUDIOREF
U26•03	CR28	CR29	R93	R95				AUDIOIN
U26•04	GND							GND
U26•05	UNUSED							
U26•06	UNUSED							
U26•07	U25•16							DATA•IN
U26•08	+5V							+5V
U27•01	GND							GND
U27•02	(U12•19)•2	(U20•23)•3	E•F					A5
U27•03	(U12•19)•3	(U20•23)•4	E•E					A4
U27•04	(U12•19)•4	(U20•23)•5	(U25,28,29)•35	E•D				A3
U27•05	(U12•19)•7	(U20•23)•6	(U25,28,29)•36	E•C				A2
U27•06	(U12•19)•6	(U20•23)•7	(U25,28,29)•37	E•B				A1
U27•07	(U12•19)•5	(U20•23)•8	(U25,28,29)•38	E•A				A0
U27•08	U30•13							COLA
U27•09	U30•11							COLB
U27•10	U30•5							COLC
U27•11	U30•3							COLD
U27•12	U30•1							COLE
U27•13	U30•9							COLF
U27•14	U38•11							COLG
U27•15	U38•13							ROW0
U27•16	U38•6							CRTIN
U27•17	Q28							TTYIN
U27•18	RN1							TTYOUT
U27•19	U38•1							CRTOUT
U27•20	+5V							+5V
U27•21	U37•12							DIS•ENA
U27•22	U37•13							ROW3
U27•23	U37•14							ROW2
U27•24	U37•15							ROW1
U27•25	UNUSED							IRQ•NOT
U27•26	(U13,15,17,19)•11	(U20•23)•17	(U25,28,29)•26	E•8				D7
U27•27	(U13,15,17,19)•12	(U20•23)•16	(U25,28,29)•27	E•9				D6
U27•28	(U13,15,17,19)•13	(U20•23)•15	(U25,28,29)•28	E•10				D5
U27•29	(U13,15,17,19)•14	(U20•23)•14	(U25,28,29)•29	E•11				D4
U27•30	(U13,15,17,19)•11	(U20•23)•13	(U25,28,29)•30	E•12				D3
U27•31	(U13,15,17,19)•12	(U20•23)•12	(U25,28,29)•31	E•13				D2
U27•32	(U13,15,17,19)•13	(U20•23)•11	(U25,28,29)•32	E•14				D1
U27•33	(U13,15,17,19)•14	(U20•23)•10	(U25,28,29)•33	E•15				D0
U27•34	E•7	U3•6	U5•40					RES•NOT
U27•35	U8•11							MONRAMRW
U27•36	U9•8							A9•NOT

SYM•1 IC INTERCONNECT REFERENCE LISTING

IC/PIN#	POINTS TO WHICH IT IS CONNECTED	SIGNAL NAME
U27•37	U10•5	AA0•NOT
U27•38	(U20•23)•19 U9•1 E•M	A10
U27•39	U2•6 E•U	PHASE•2
U27•40	(U12•19)•1 (U20•23)•2 E•H	A6
U28•01	GND	GND
U28•02	AA•D	
U28•03	AA•3	
U28•04	AA•C	
U28•05	AA•12	
U28•06	AA•N	
U28•07	AA•11	
U28•08	AA•M	
U28•09	AA•10	
U28•10	AA•L	
U28•11	AA•9	
U28•12	AA•K	
U28•13	AA•8	
U28•14	AA•J	
U28•15	AA•7	
U28•16	AA•H	
U28•17	AA•6	
U28•18	AA•F	
U28•19	AA•5	
U28•20	+5V	+5V
U28•21	E•4 U5•4	IRQ•NOT
U28•22	E•V U2•8 U3•10 U3•11	RW
U28•23	U10•6 R60	AA8•NOT
U28•24	U9•2 U25•24	A10•NOT
U28•25	U2•6 E•U	PHASE•2
U28•26	(U13,15,17,19)•11 (U20•23)•17 (U25,27,29)•26 E•8	D7
U28•27	(U13,15,17,19)•12 (U20•23)•16 (U25,27,29)•27 E•9	D6
U28•28	(U13,15,17,19)•13 (U20•23)•15 (U25,27,29)•28 E•10	D5
U28•29	(U13,15,17,19)•14 (U20•23)•14 (U25,27,29)•29 E•11	D4
U28•30	(U13,15,17,19)•11 (U20•23)•13 (U25,27,29)•30 E•12	D3
U28•31	(U13,15,17,19)•12 (U20•23)•12 (U25,27,29)•31 E•13	D2
U28•32	(U13,15,17,19)•13 (U20•23)•11 (U25,27,29)•32 E•14	D1
U28•33	(U13,15,17,19)•14 (U20•23)•10 (U25,27,29)•33 E•15	D0
U28•34	U3•6 U5•40 E•7	RES•NOT
U28•35	(U12•19)•4 (U20•23)•5 (U25,29)•35 U27•4 E•D	A3
U28•36	(U12•19)•7 (U20•23)•6 (U25,29)•36 U27•5 E•C	A2
U28•37	(U12•19)•6 (U20•23)•7 (U25,29)•37 U27•6 E•B	A1
U28•38	(U12•19)•5 (U20•23)•8 (U25,29)•38 U27•7 E•A	A0
U28•39	AA•4	•
U28•40	AA•E	•
U29•01	GND	GND
U29•02	AA•V	
U29•03	AA•W	
J29•04	AA•X	

SYM•1 IC INTERCONNECT REFERENCE LISTING

IC/PIN#	POINTS TO WHICH IT IS CONNECTED	SIGNAL NAME
U29•05	AA•18	
U29•06	AA•19	
U29•07	AA•20	
U29•08	AA•17	
U29•09	AA•U	
U29•10	AA•16	
U29•11	AA•T	
U29•12	AA•15	
U29•13	AA•S	
U29•14	AA•Y BUFFERED	
U29•15	AA•21 BUFFERED	
U29•16	AA•Z BUFFERED	
U29•17	AA•22 BUFFERED	
U29•18	AA•14	
U29•19	SCOPE•OUT•BUFF	
U29•20	+5V	+5V
U29•21	E•4 U5•4 U25•21 U28•21	IRQ•NOT
U29•22	E•V U2•8 U3•10 U3•11	RW
U29•23	R60 U28•23	AA8•NOT
U29•24	(U20•23)•19 U9•1 E•M	A10
U29•25	E•U U2•6	PHASE•2
U29•26	(U13,15,17,19)•11 (U20•23)•17 (U25,27,28)•26 E•8	D7
U29•27	(U13,15,17,19)•12 (U20•23)•16 (U25,27,28)•27 E•9	D6
U29•28	(U13,15,17,19)•13 (U20•23)•15 (U25,27,28)•28 E•10	D5
U29•29	(U13,15,17,19)•14 (U20•23)•14 (U25,27,28)•29 E•11	D4
U29•30	(U13,15,17,19)•11 (U20•23)•13 (U25,27,28)•30 E•12	D3
U29•31	(U13,15,17,19)•12 (U20•23)•12 (U25,27,28)•31 E•13	D2
U29•32	(U13,15,17,19)•13 (U20•23)•11 (U25,27,28)•32 E•14	D1
U29•33	(U13,15,17,19)•14 (U20•23)•10 (U25,27,28)•33 E•15	D0
U29•34	E•7 U3•6 U5•40	RES•NOT
U29•35	(U12•19)•4 (U20•23)•5 (U25,28)•35 U27•4 E•D	A3
U29•36	(U12•19)•7 (U20•23)•6 (U25,28)•36 U27•5 E•C	A2
U29•37	(U12•19)•6 (U20•23)•7 (U25,28)•37 U27•6 E•B	A1
U29•38	(U12•19)•5 (U20•23)•8 (U25,28)•38 U27•7 E•A	A0
U29•39	SCOPE•OUT•BUFFER	
U29•40	AA•P	

U30•01	U27•12 A•20	
U30•02	RN2•SEG•E	
U30•03	U27•11 A•22	
U30•04	RN2•SEG•D	
U30•05	U27•10 A•Y	
U30•06	RN2•SEG•C	
U30•07	GND	
U30•08	RN2•SEG•F	
U30•09	U27•13 A•18	
U30•10	RN2•SEG•B	
U30•11	U27•9 A•19	
U30•12	RN2•SEG•A	
U30•13	U27•8 A•21	
U30•14	+5V	

SYM•1 IC INTERCONNECT REFERENCE LISTING

IC/PIN#	POINTS TO WHICH IT IS CONNECTED				SIGNAL NAME
J31•U36•01	SEGMENT•A•ALL•WIRED•TOGETHER				
J31•U36•02	SEGMENT•F•ALL•WIRED•TOGETHER				
J31•03	BUFFER•SW•TO•5V•FROM•U37•01				
J32•03	BUFFER•SW•TO•5V•FROM•U37•02				
J33•03	BUFFER•SW•TO•5V•FROM•U37•03				
J34•03	BUFFER•SW•TO•5V•FROM•U37•04				
J35•03	BUFFER•SW•TO•5V•FROM•U37•05				
J36•03	BUFFER•SW•TO•5V•FROM•U37•06				
J31•U36•04	UNUSED				
J31•U36•05	UNUSED				
J31•U36•06	UNUSED				
J31•U36•07	SEGMENT•E•ALL•WIRED•TOGETHER				
J31•U36•08	SEGMENT•D•ALL•WIRED•TOGETHER				
J31•U36•09	DECIMAL•PT•ALL•WIRED•TOGETHER				
J31•U36•10	SEGMENT•C•ALL•WIRED•TOGETHER				
J31•U36•11	SEGMENT•G•ALL•WIRED•TOGETHER				
J31•U36•12	UNUSED				
J31•U36•13	SEGMENT•B•ALL•WIRED•TOGETHER				
J31•U36•14	DIRECT•SHORT•TO•PIN•3•OF•RESPECTIVE•IC				
J37•01	BUFFER•SWITCH•TO•U31•3,U31•14				
J37•02	BUFFER•SWITCH•TO•U32•3,U32•14				
J37•03	BUFFER•SWITCH•TO•U33•3,U33•14				
J37•04	BUFFER•SWITCH•TO•U34•3,U34•14				
J37•05	BUFFER•SWITCH•TO•U35•3,U35•14				
J37•06	BUFFER•SWITCH•TO•U36•3,U36•14				
J37•07	BUFFER•SWITCH•TO•SPEAKER•SP•1				
J37•08	GND				
J37•09	R61	R90			
J37•10	UNUSED				
J37•11	UNUSED				
J37•12	U27•21				DIS•ENA
J37•13	U27•22	A•V			ROW3
J37•14	U27•23	A•X			ROW2
J37•15	U27•24				ROW1
J37•16	+5V				+5V
J38•01	U27•19				
J38•02	RN1				
J38•03	UNUSED				
J38•04	UNUSED				
J38•05	Q29				
J38•06	U27•16				
J38•07	GND				
J38•08	U8•4	R76			
J38•09	U6•3	U3•3	U3•4	U3•5	
J38•10	RN2•SEG•G				
J38•11	U27•14	A•W			

SYM•1 IC INTERCONNECT REFERENCE LISTING

IC/PIN#	POINTS TO WHICH IT IS CONNECTED	SIGNAL NAME
U38•12	RN2•SEG•DP	
U38•13	U27•15 A•17	
U38•14	+5V	

APPENDIX 2 -

SYM-1 SIGNAL NAME CROSS REFERENCE LISTING

Notes: 1. Signal source is shown by a single '*'.

2. Bidirectional (DATA) lines are shown by '**'.

SYM•1 SIGNAL NAME CROSS REFERENCE LISTING

SIG.NAME	WHERE IT OCCURS ON THE BOARD	
+5V	U1•16	
+5V	U2•14	
+5V	U3•14	
+5V	U4•14	
+5V	U5•08	
+5V	U6•08	
+5V	U7•14	
+5V	U8•14	
+5V	U9•14	
+5V	U10•16	
+5V	U11•16	
+5V	(U12•U19)•18	
+5V	(U20•23)•24	
+5V	U21•21	
+5V	U22•21	
+5V	U23•21	
+5V	U24•14	
+5V	U25•20	
+5V	U26•08	
+5V	U27•20	
+5V	U28•20	
+5V	U29•20	
+5V	U37•16	
AA0•NOT	U10•05*	WHEN THIS LINE IS LOW, THE ADDRESSES FROM
AA0•NOT	U8•01	A000•A7FF ARE BEING SELECTED.
AA0•NOT	U25•23	
AA0•NOT	U27•37	
AA8•NOT	U1C•06*	WHEN THIS LINE IS LOW, THE ADDRESSES FROM
AA8•NOT	U28•23	A800•A8FF ARE BEING SELECTED.
AA8•NOT	U29•23	
AUDIOIN	U26•03	
AUDIOREF	U26•02	
A0	U5•09*	THIS IS ADDRESS LINE A0
A0	(U12•U19)•05	
A0	(U20•23)•08	
A0	U25•38	
A0	U27•07	
A0	U28•38	
A0	U29•38	
A1	U5•10*	THIS IS ADDRESS LINE A1
A1	(U12•U19)•06	
A1	(U20•23)•07	
A1	U25•37	
A1	U27•06	
A1	U28•37	
A1	U29•37	
A2	U5•11*	THIS IS ADDRESS LINE A2
A2	(U12•U19)•07	
A2	(U20•23)•06	
A2	U25•36	
A2	U27•05	
A2	U28•36	
A2	U29•36	
A3	U5•12*	THIS IS ADDRESS LINE A3

SYM=1 SIGNAL NAME CROSS REFERENCE LISTING

SIG.NAME	WHERE IT OCCURS ON THE BOARD	
A3	(U12=U19)=04	
A3	(U20=23)=05	
A3	U25=35	
A3	U27=04	
A3	U28=35	
A3	U29=35	
A4	U5=13*	THIS IS ADDRESS LINE A4
A4	(U12=U19)=03	
A4	(U20=23)=04	
A4	U27=03	
A5	U5=14*	THIS IS ADDRESS LINE A5
A5	(U12=U19)=02	
A5	(U20=23)=03	
A5	U27=02	
A6	U5=15*	THIS IS ADDRESS LINE A6
A6	(U12=U19)=01	
A6	(U20=23)=02	
A6	U27=40	
A7	U5=16*	THIS IS ADDRESS LINE A7
A7	(U12=U19)=17	
A7	(U20=23)=01	
A8	U5=17*	THIS IS ADDRESS LINE A8
A8	(U12=U19)=16	
A8	(U20=23)=23	
A9	U5=18*	THIS IS ADDRESS LINE A9
A9	U7=05	
A9	U9=09	
A9	(U12=U19)=15	
A9	(U20=23)=22	
A9=NOT	U9=08*	
A9=NOT	U27=36	
A10	U1=01	THIS IS ADDRESS LINE A10
A10	U5=19*	
A10	U9=01	
A10	U27=38	
A10	U29=24	
A10=NOT	U9=02*	
A10=NOT	U25=24	
A10=NOT	U28=24	
A11	U1=02	THIS IS ADDRESS LINE A11
A11	U5=20*	
A11	U10=15	
A11	U11=15	
A11	U20=18	
A12	U1=03	THIS IS ADDRESS LINE A12
A12	U5=22*	
A12	U10=14	
A12	U11=14	
A13	U3=13	THIS IS ADDRESS LINE A13
A13	U5=23*	
A13	U10=13	
A13	U11=13	
A14	U3=02	THIS IS ADDRESS LINE A14
A14	U5=24*	

SYM•1 SIGNAL NAME CROSS REFERENCE LISTING

SIG.NAME	WHERE IT OCCURS ON THE BOARD	
A14	U7•13	
A14	U9•13	
A14•NOT	U4•01	
A14•NOT	U9•12*	
A15	U3•01	THIS IS ADDRESS LINE A15
A15	U4•02	
A15	U5•25*	
A15	U7•01	
A15	U25•17	
BOXX	U10•07*	WHEN LOW, ADDRESS B000•B7FF ARE SELECTED
B8XX	U10•09*	WHEN LOW, ADDRESS B800•BFFF ARE SELECTED
CA2•U25	U8•02	
COLA	U27•08*	COLUMN A OF ONBOARD KEYPAD OR SEGMENT OF DI
COLB	U27•09*	COLUMN B
COLC	U27•10*	COLUMN C
COLD	U27•11*	COLUMN D
COLE	U27•12*	COLUMN E
COLF	U27•13*	COLUMN F
COLG	U27•14*	COLUMN G
CRTIN	U27•16*	
CRTOUT	U27•19*	
COXX	U11•01*	WHEN LOW, ADDRESSES C000•C7FF ARE SELECTED
C8XX	U11•02*	WHEN LOW, ADDRESSES C800•CFFF ARE SELECTED
DATA•IN	U25•16	
DATA•IN	U26•07*	
DBUGLATCH	U8•06	PART OF THE DEBUG FUNCTION... THE MEMORY
DBUGLATCH	U8•09	
DBUGOFF	U8•04	WHEN BROUGHT LOW, DISABLES DEBUG FUNCTION
DBUGON	U8•05	WHEN BROUGHT LOW, ENABLES DEBUG FUNCTION
DBUGON	U8•08	
DBUGON	U8•10	
DEBUG•ON	U7•09	
DIS•ENA	U27•21*	WHEN LOW, ENABLES THE ONBOARD DISPLAY
DIS•ENA	U37•12	
DISABL•U10	U10•12	WHEN HIGH, DISABLES MEMORY FROM 8000•BFFF
DISABL•U10	U4•3*	
DISABL•U11	U11•12	WHEN HIGH, DISABLES MEMORY FROM C000•FFFF
DO	U5•33**	DATA LINE D0
DO	(U12,14,16,18)•14**	
DO	(U20•23)•09**	
DO	U25•33**	
DO	U27•33**	
DO	U28•33**	
DO	U29•33**	
DOXX	U11•03**	WHEN LOW, ADDRESSES D000•D7FF ARE SELECTED
D1	U5•32**	DATA LINE D1
D1	(U12,14,16,18)•13**	
D1	(U20•23)•10**	
D1	U25•32**	
D1	U27•32**	
D1	U28•32**	
D1	U29•32**	
D2	U5•31**	DATA LINE D2

SYM•1 SIGNAL NAME CROSS REFERENCE LISTING

SIG.NAME	WHERE IT OCCURS ON THE BOARD
D2	(U12,14,16,18)•12**
D2	(U20•23)•11**
D2	U25•31**
D2	U27•31**
D2	U28•31**
D2	U29•31**
D3	U5•30** DATA LINE D3
D3	(U12,14,16,18)•11**
D3	(U20•23)•13**
D3	U25•30**
D3	U27•30**
D3	U28•30**
D3	U29•30**
D4	U5•29** DATA LINE D4
D4	(U13,15,17,19)•14**
D4	(U20•23)•14**
D4	U25•29**
D4	U27•29**
D4	U28•29**
D4	U29•29**
D5	U5•28** DATA LINE D5
D5	(U13,15,17,19)•13**
D5	(U20•23)•15**
D5	U25•28**
D5	U27•28**
D5	U28•28**
D5	U29•28**
D6	U5•27** DATA LINE D6
D6	(U13,15,17,19)•12**
D6	(U20•23)•16**
D6	U25•27**
D6	U27•27**
D6	U28•27**
D6	U29•27**
D7	U5•26** DATA LINE D7
D7	(U13,15,17,19)•11**
D7	(U20•23)•17**
D7	U25•26**
D7	U27•26**
D7	U28•26**
D7	U29•26**
D8XX	U11•04* WHEN LOW, ADDRESSES D800•DFFF ARE SELECTED
E0XX	U11•05* WHEN LOW, ADDRESSES E000•E7FF ARE SELECTED
E8XX	U11•06* WHEN LOW, ADDRESSES E800•EFFF ARE SELECTED
F0XX	U11•07* WHEN LOW, ADDRESSES F000•F7FF ARE SELECTED
F8XX	U11•09* WHEN LOW, ADDRESSES F800•FFFF ARE SELECTED
GND	U1•04
GND	U1•05
GND	U1•08
GND	U2•07
GND	U3•07
GND	U4•07
GND	U5•01
GND	U5•21

SYM•1 SIGNAL NAME CROSS REFERENCE LISTING

SIG.NAME	WHERE IT OCCURS ON THE BOARD	
GND	U6•01	
GND	U7•07	
GND	U8•07	
GND	U9•07	
GND	U10•08	
GND	U11•08	
GND	(U12•U19)•09	
GND	(U20•23)•12	
GND	U21•18	
GND	U22•18	
GND	U23•18	
GND	U20•21	
GND	U24•07	
GND	U25•40	
GND	U26•01	
GND	U26•04	
GND	U27•01	
GND	U28•01	
GND	U29•01	
IRQ•NOT	U5•04	THE INTERRUPT REQUEST LINE, CAUSES AN IRQ
IRQ•NOT	U25•21*	INTERRUPT OF THE PROCESSOR WHEN LOW ONLY
IRQ•NOT	U27•25*	IF THE INTERRUPTS ARE ENABLED AT THE TIME
IRQ•NOT	U28•21*	
IRQ•NOT	U29•21*	
MONRAMRW	U27•35	MONITOR RAM RW LINE, WHEN LOW ALLOWS WRITE
NMI•NOT	U5•06	NONMASKABLE INTERRUPT CAUSED WHEN LOW
NMI•NOT	U7•08*	
PHASE•1	U5•03*	PROCESSOR CLOCK PHASE 1
PHASE•2	U2•03	PROCESSOR CLOCK PHASE 2
PHASE•2	U5•39*	
PHASE•2	U25•25	
PHASE•2	U27•39	
PHASE•2	U28•25	
PHASE•2	U29•25	
PHASE•2 N	U2•04	INVERTED PHASE 2 CLOCK
PHASE•2 N	U2•05	
PHASE•2 O	U2•06	BUFFERED OUTPUT OF PHASE 2 CLOCK
PHASE•2•N	U3•09	
POR•NOT	U7•02	POWER•ON RESET ACTIVE WHEN LOW
POR•NOT	U8•03*	
POR•NOT	U24•09	
RAM•RW	(U12,U13)•10	RAM READ•WRITE
RAM•RW	U2•12*	
RDY	U5•02*	PROCESSOR READY LINE
RES	U6•3*	RESET OUTPUT OF U6, WHEN HIGH INITIALIZES
RES	U3•03	PROCESSOR AND PERIPHERAL PARTS
RES	U3•04	
RES	U3•05	
RES•NOT	U3•06*	
RES•NOT	U25•34	
RES•NOT	U27•34	
RES•NOT	U28•34	
RES•NOT	U29•34	
RN•NOT	U7•11	NOT•MONITOR, IF HIGH, MON. IS NOT SELECTED

SYM•1 SIGNAL NAME CROSS REFERENCE LISTING

SIG.NAME	WHERE IT OCCURS ON THE BOARD.	
RN•NOT	U24•08*	
RO	U5•38*	PROCESSOR RO LINE
ROW0	U27•15*	ROW 0 OF THE ONBOARD KEYPAD
ROW1	U27•24*	ROW 1
ROW1	U37•15	
ROW2	U27•23*	ROW 2
ROW2	U37•14	
ROW3	U27•22*	ROW 3
ROW3	U37•13	
RST	U5•40	ON THE LEADING EDGE OF A HIGH SIGNAL
RST	U6•02*	CAUSES THE PROCESSOR POWER•ON RESET SEQUENCE
RW	U2•08	
RW	U2•11	THE READ•WRITE LINE, READ•HIGH, WRITE•LOW
RW	U3•10	
RW	U3•11	
RW	U5•34*	
RW	U25•22	
RW	U28•22	
RW	U29•22	
RW•MON	U8•11	MONITOR READ•WRITE, READ HIGH,WRITE•LOW
RW•NOT	U2•09	
RW•NOT	U2•10	
RW•NOT	U7•03	
RW•NOT	U8•13	
SYNC	U5•07*	GOES HIGH FOR EACH ACCESS OF AN OPCODE
SYNC	U7•10	
TAPECNTL	U25•19*	
TIMER•OUT	U6•03*	
TTYIN	U27•17*	
TTYOUT	U27•18*	
U21•SEL	U24•06*	WHEN LOW, IC U21 IS SELECTED
U21•SEL	U21•20	
U22•SEL	U24•11*	WHEN LOW, IC U22 IS SELECTED
U22•SEL	U22•20	
U23•SEL	U24•03*	WHEN LOW, IC U23 IS SELECTED
U23•SEL	U23•20	
WPM•NOT	U7•04	WHEN LOW, MONITOR IS WRITE•PROTECTED
WPM•NOT	U29•2*	
WPM•NOT	U9•10	
WPM•NOT	U9•11	
WP1K•NOT	U4•04	WHEN LOW, 0400•07FF ARE WRITE PROTECTED
WP2K•NOT	U4•12	WHEN LOW, 0800•0BFF ARE WRITE PROTECTED
WP3K•NOT	U4•09	WHEN LOW, 0C00•0FFF ARE WRITE PROTECTED
WRITE	U2•13	WRITE LINE, WHEN HIGH, CPU DOING A WRITE
WRITE	U3•08*	
WRITE	U4•05	
WRITE	U4•10	
WRITE	U4•13	
WRITE•MON	U7•06*	THE MONITOR WRITE LINE, WHEN HIGH,
WRITE•MON	U8•12	WRITE INTO THE MONITOR RAM
WRITE•NOT	U2•12	THIS IS THE ACTIVE LOW WRITE PULSE FOR EXTERNAL RAM
WR1•NOT	U4•06*	WRITE CONTROL 0400•07FF, WRITES IF LOW
WR1•NOT	(U14,U15)•10	
WR2•NOT	U4•11*	WRITE CONTROL 0800•0BFF, WRITES IF LOW

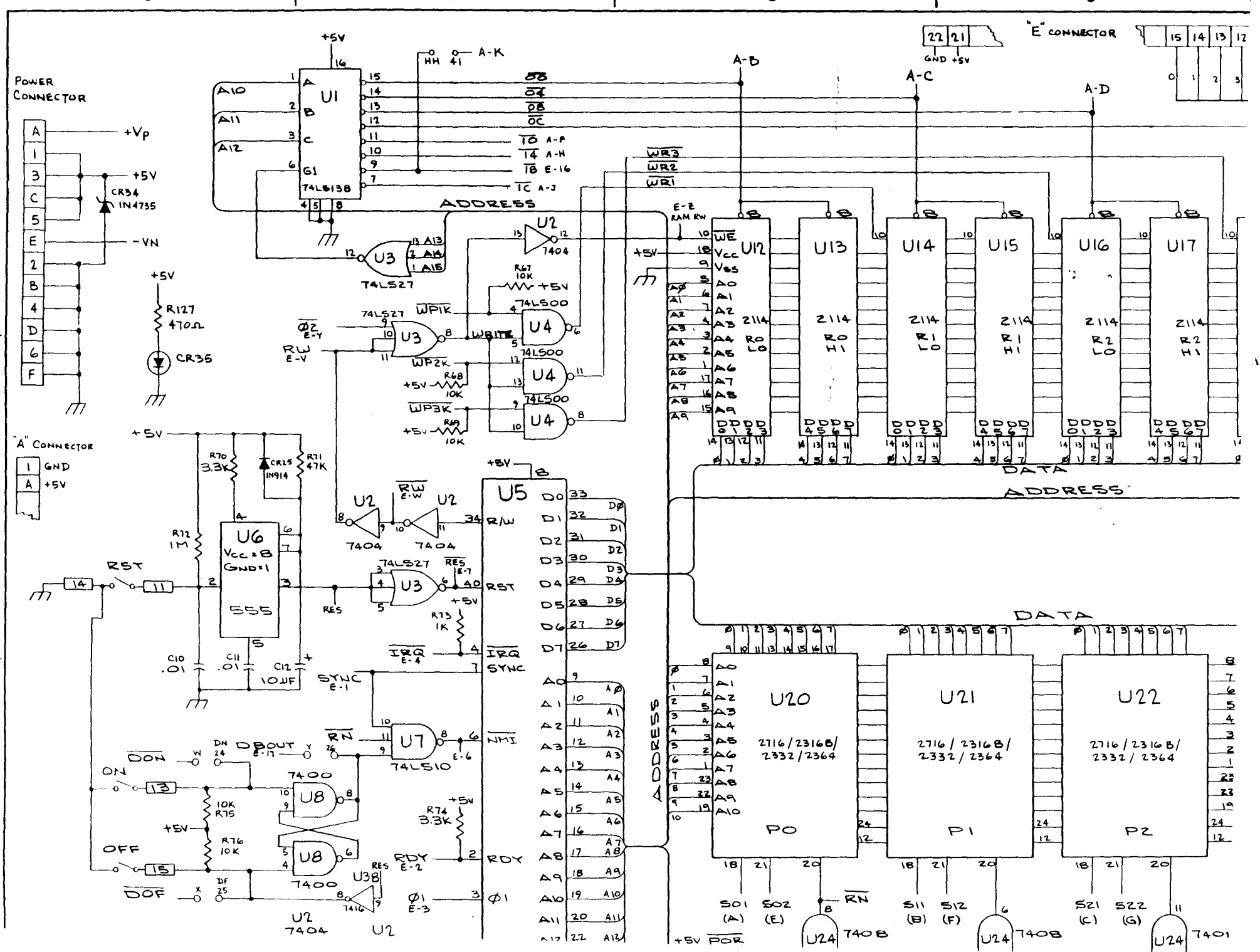
SYM•1 SIGNAL NAME CROSS REFERENCE LISTING

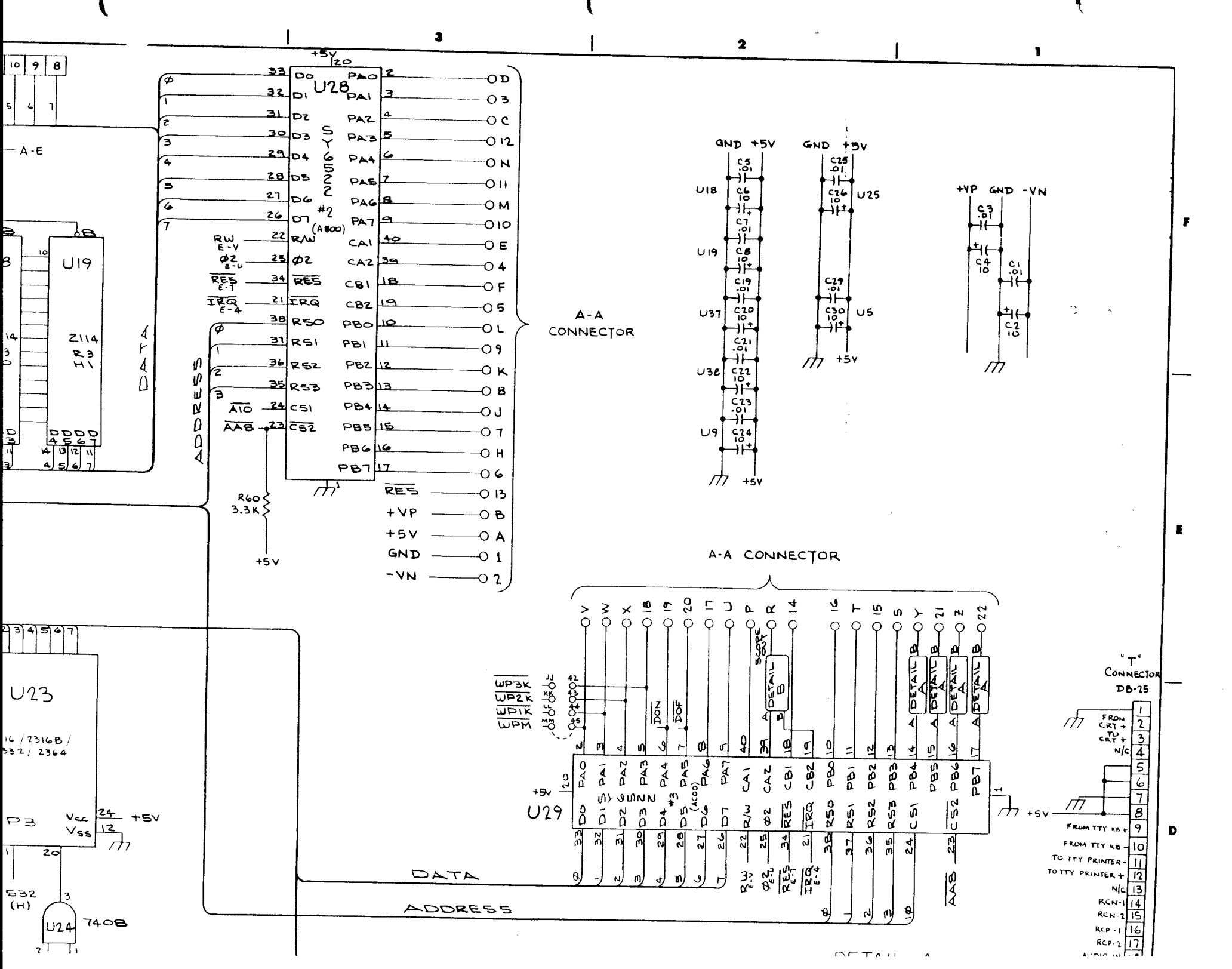
SIG.NAME	WHERE IT OCCURS ON THE BOARD	
WR2•NOT	(U16,U17)•10	
WR3•NOT	U4•08	WRITE CONTROL 0C00•0FFF, WRITES IF LOW
WR3•NOT	(U18,U19)•10	
XTAL	U5•37	TIMING CRYSTAL, HEART OF THE SYSTEM
0C	U1•12*	WHEN LOW, 0C00•0FFF ARE SELECTED
0C	(U18,U19)•08	
00	U1•15	WHEN LOW, 0000•03FF ARE SELECTED
00	(U12,U13)•08	
04	U1•14	WHEN LOW, 0400•07FF ARE SELECTED
04	(U14,U15)•08	
08	U1•13	WHEN LOW, 0800•08FF ARE SELECTED
08	(U16,U17)•08	
1/4 8K SEL	U1•06	WHEN LOW, 0000•3FFF ARE SELECTED
1/4 8K SEL	U3•12*	
1C	U1•07*	WHEN LOW, 1C00•1FFF ARE SELECTED
10	U1•11*	WHEN LOW, 1000•13FF ARE SELECTED
14	U1•10*	WHEN LOW, 1400•17FF ARE SELECTED
18	U1•09*	WHEN LOW, 1800•1BFF ARE SELECTED
3/4 8K SEL	U4•03*	WHEN LOW, 8000•8FFF ARE SELECTED
3/4 8K SEL	U10•1	
4/4 8K SEL	U7•12*	WHEN LOW, C000•FFFF ARE SELECTED
4/4 8K SEL	U11•12	
80XX	U24•10	WHEN LOW, 8000•87FF ARE SELECTED
80XX	U10•01*	
88XX	U10•02*	WHEN LOW, 8300•8FFF ARE SELECTED
90XX	U10•03*	WHEN LOW, 9000•97FF ARE SELECTED
98XX	U10•04*	WHEN LOW, 9800•9FFF ARE SELECTED

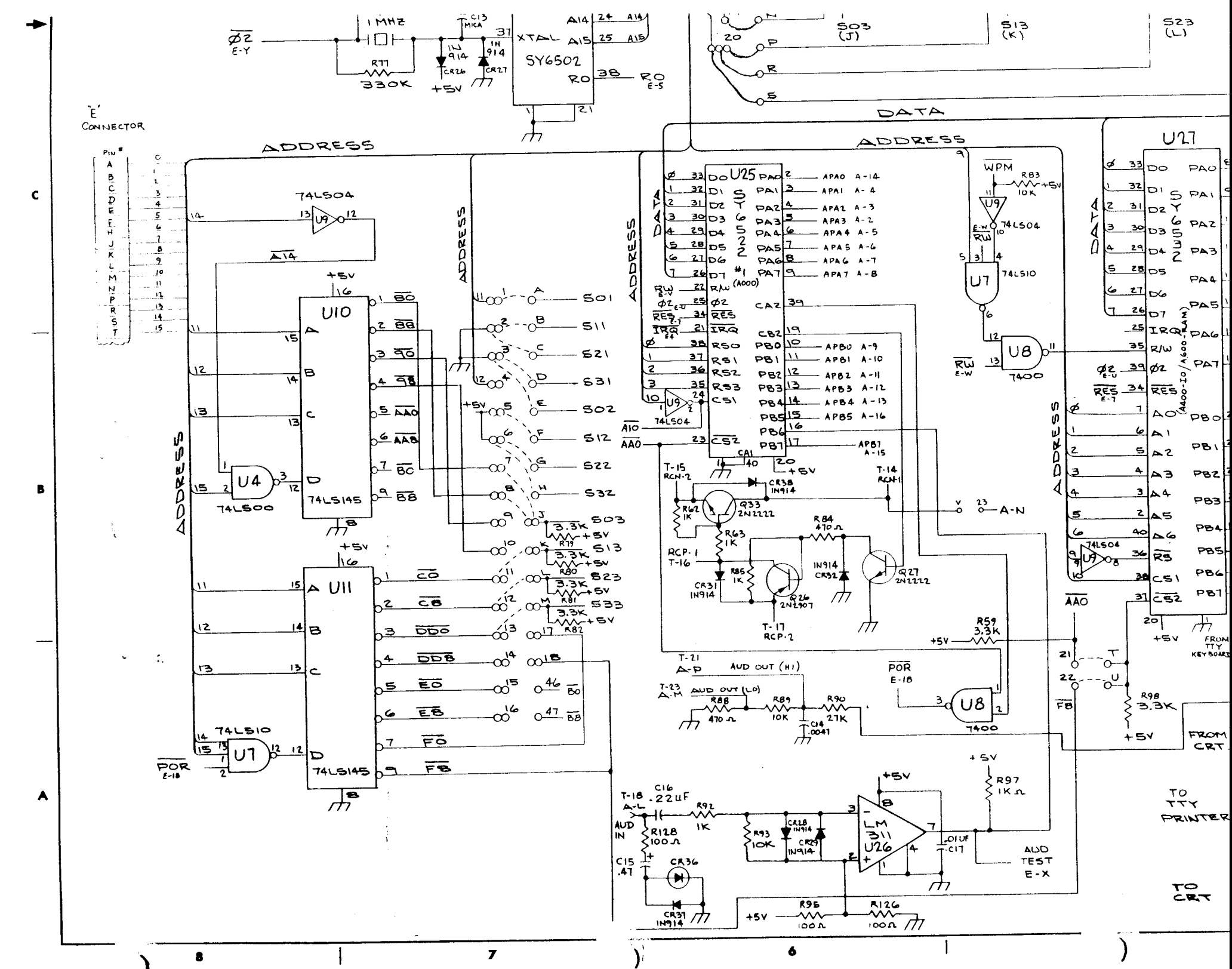
APPENDIX 3 -

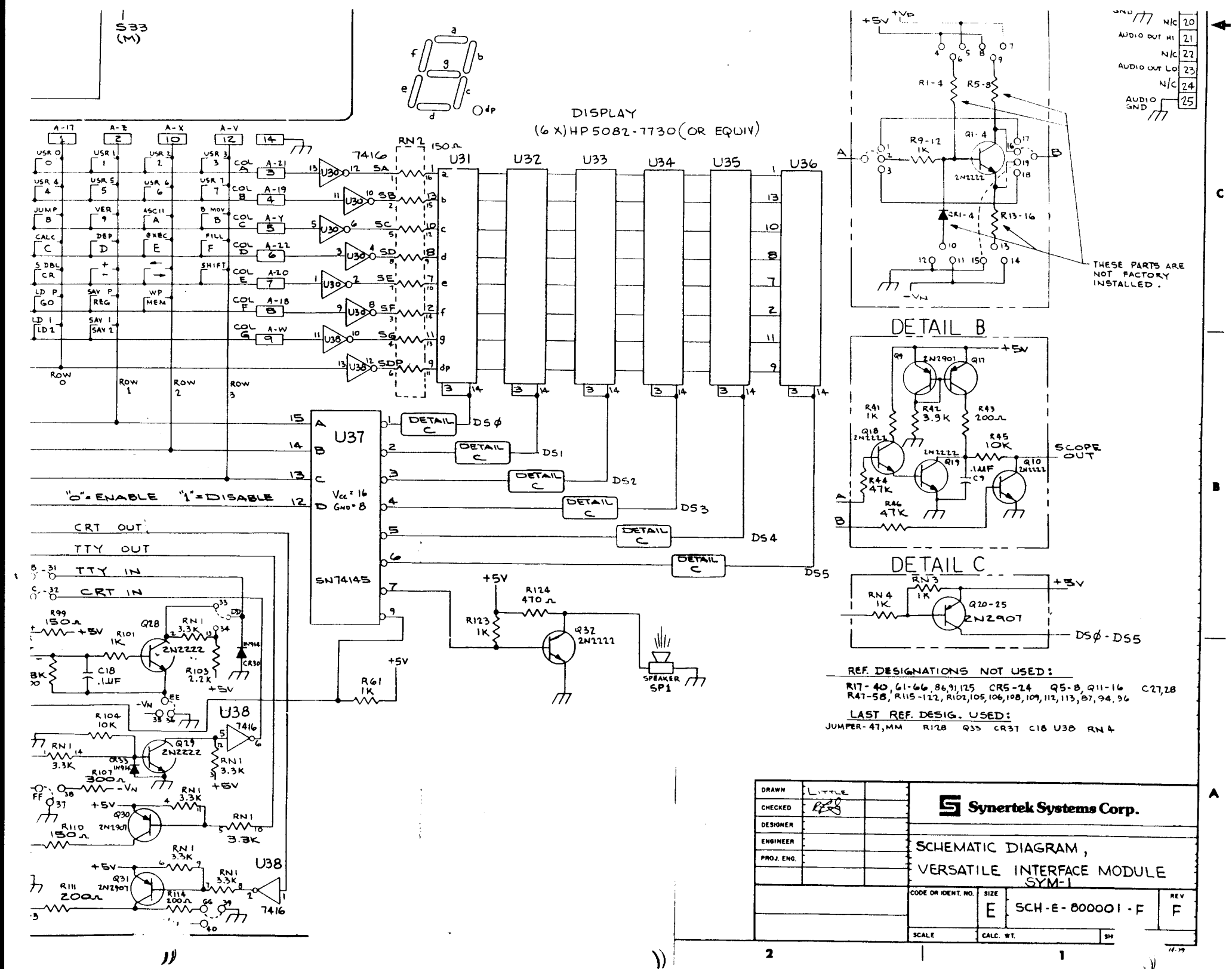
SYM-1 SCHEMATIC DIAGRAM*

*Permission to include in this volume provided courtesy of Synertek Systems Corp.


8
7
6
5
F
E
D
POWER CONNECTOR
+Vp
+5V
CR34 IN4735
-VN
R127 470Ω
CR35
"A" CONNECTOR
GND
+5V
U1
74LS138
A10
A11
A12
A-K
HH 41
ADDRESS
U2
7404
U3
74LS27
R67 10K
74LS00
U4
WP1K
WP2K
WP3K
R68 10K
R69 10K
WRITE
RW E-V
Ø2 E-Y
R70 3.3K
CR25 IN914
R71 47K
R72 1M
U6
Vcc=8
GND=1
555
RST
RES
C10 .01
C11 .01
C12 10µF
U5
R/W
RST
IRQ
SYNC
RDY
Ø1
D0
D1
D2
D3
D4
D5
D6
D7
R73 1K
R74 3.3K
U7
74LS10
NMI
RN
DON
DOF
DBOUT
U8
7400
R75 10K
R76 10K
U38
7416
WR3
WR2
WR1
E-E RAM RW
U12
U13
U14
U15
U16
U17
2114
R0 LO
R0 HI
R1 LO
R1 HI
R2 LO
R2 HI
A-B
A-C
A-D
DATA
ADDRESS
"E" CONNECTOR
GND +5V
U20
U21
U22
2716/2316B/2332/2364
P0
P1
P2
S01 (A)
S02 (E)
S11 (B)
S12 (F)
S21 (C)
S22 (G)
U24 7408
U24 7401
+5V POR


3
2
1
F
E
D
U28
SYSTEM #2 (A800)
U19
2114
U23
U29
U24
7408
U18
U19
U37
U38
U9
U25
U5
GND +5V
+VP GND -VN
A-A CONNECTOR
A-E
DATA
ADDRESS
R60 3.3K
+5V
RW E-V
Φ2 E-U
RES E-T
IRQ E-4
A10
AA8
RES
+VP
+5V
GND
-VN
"T" CONNECTOR DB-25
FROM CRT +
TO CRT +
N/C
FROM TTY KB +
FROM TTY KB -
TO TTY PRINTER -
TO TTY PRINTER +
N/C
RCN-1
RCN-2
RCP-1
RCP-2
DETAIL A
DETAIL B
SCORE ENT
DON
DOF
DATA
ADDRESS


1 MHZ
Ø2 E-Y
R77 330K
C13 MICA
IN 914 CR26
IN 914 CR27
+5V
XTAL
SY6502
A14
A15
RO
RO E-5
S03 (J)
S13 (K)
S23 (L)
DATA
ADDRESS
"E" CONNECTOR
74LS04
U9
U10
U11
74LS145
U4
74LS00
U7
74LS10
POR E-18
U25
SY6522 #1 (A000)
U27
SY6522 (A400-I/O/A600-RAM)
U8
7400
U7
74LS10
WPM
RB3 10K
R/W E-W
Ø2 E-U
RES E-T
IRQ E-F
CA1
CA2
CB1
CB2
CS1
CS2
APA0 A-14
APA1 A-4
APA2 A-3
APA3 A-2
APA4 A-5
APA5 A-6
APA6 A-7
APA7 A-8
APB0 A-9
APB1 A-10
APB2 A-11
APB3 A-12
APB4 A-13
APB5 A-16
APB7 A-15
T-15 RCN-2
T-14 RCN-1
CR38 IN914
Q33 2N2222
R62 1K
R63 1K
R84 470Ω
RCP-1 T-16
CR31 IN914
R85 1K
Q26 2N2907
IN914 CR32
Q27 2N2222
T-17 RCP-2
A-N
R59 3.3K
T-21 A-P
AUD OUT (HI)
T-23 A-M
AUD OUT (LO)
R88 470Ω
R89 10K
R90 27K
C14 .0047
T-18 A-L
C16 .22uF
R92 1K
AUD IN
R128 100Ω
C15 .47
CR36
CR37 IN914
R93 10K
CR28 IN914
CR29 IN914
LM 311 U26
C17 .01UF
AUD TEST E-X
R97 1K Ω
R98 3.3K
R95 100Ω
R126 100Ω
FROM TTY KEYBOARD
FROM CRT
TO TTY PRINTER
TO CRT
R19 3.3K
R80 3.3K
R81 3.3K
R82 3.3K
S01
S11
S21
S31
S02
S12
S22
S32
S03
S13
S23
S33
S0
S1
S2
S3



REF. DESIGNATIONS NOT USED:

R17-40, 61-66, 86, 91, 125 CR5-24 Q5-8, Q11-16 C27,28
R47-58, R115-122, R102, 105, 106, 108, 109, 112, 113, 87, 94, 96

LAST REF. DESIG. USED:

JUMPER-47, MM R128 Q33 CR37 C18 U38 RN4

DRAWN	LITTLE	
CHECKED		
DESIGNER		
ENGINEER		
PROJ. ENG.		

Synertek Systems Corp.

SCHEMATIC DIAGRAM,
VERSATILE INTERFACE MODULE
SYM-1

CODE OR IDENT. NO.	SIZE		REV
	E	SCH-E-800001-F	F
SCALE	CALC. WT.	SH	