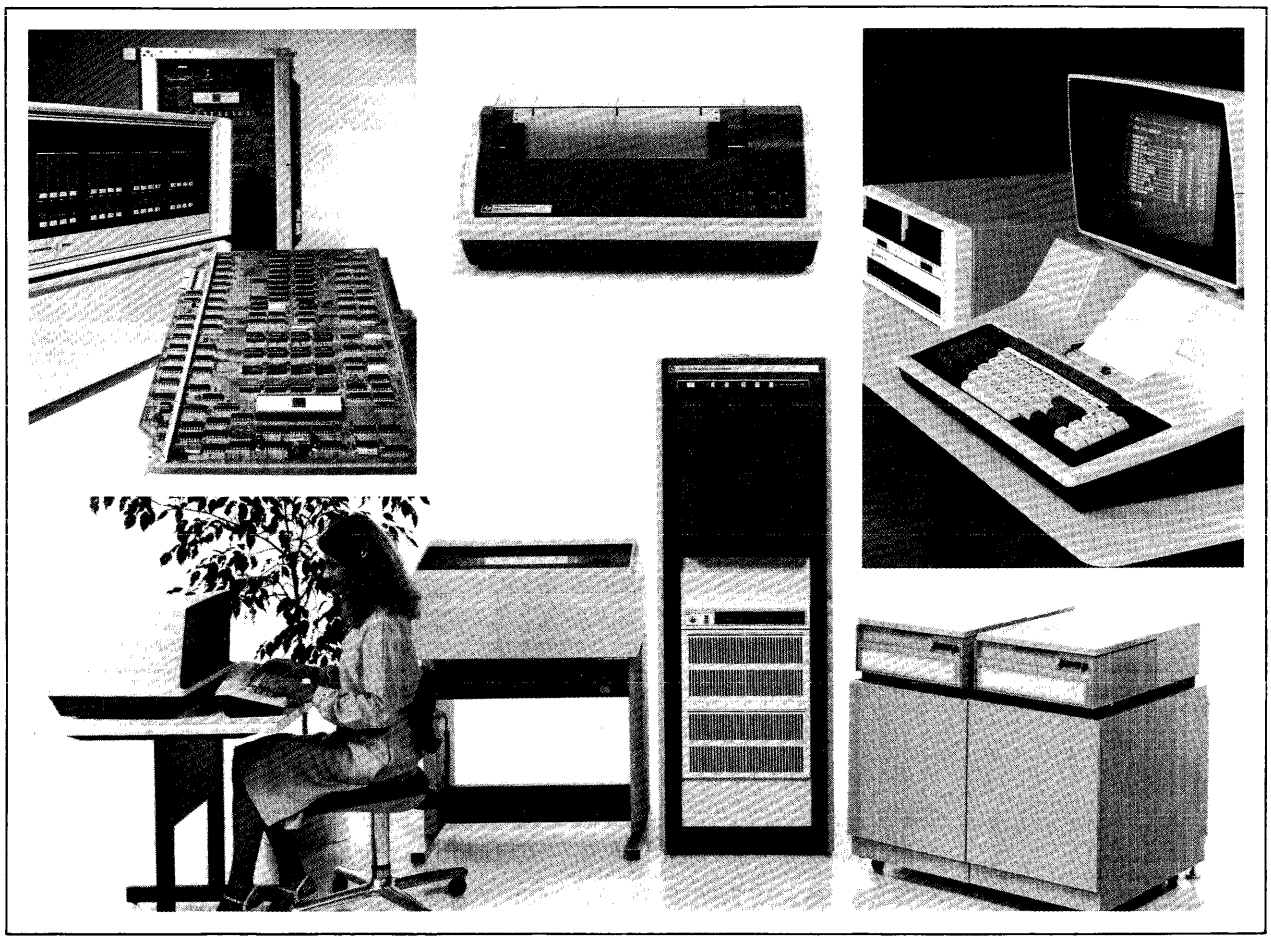
Model 990/10 Computer System
Field Maintenance Manual



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PREFACE

This manual provides field-level operation and maintenance information required to service the Texas Instruments Model 990/10 Minicomputer System. This manual is intended for use by trained Customer Service Engineers or other qualified maintenance personnel assigned to 990/10 field service support.

This manual contains a brief physical and functional description of the 990/10 system and describes all hardware options and system configurations. The manual also contains a description of the Model 990 Maintenance Unit used to load diagnostics and to manually control a system that is down and is not equipped with a programmer panel or operable 733 ASR data terminal. Fault isolation procedures are also provided to permit rapid tracing of system malfunctions down to the replaceable logic board or cable (or replaceable IC level in some cases). Packaging and shipping instructions are also provided to permit safe shipment of the faulty board(s) back to the factory or other authorized depot maintenance facility where board repair is performed.

Field service instructions for the peripheral subsystems in the 990/10 Minicomputer System are covered in a separate manual entitled *Model 990 Computer Peripheral Equipment Field Maintenance Manual*, Part Number 945419-9701.

This manual is organized into six sections and nine appendixes:

I. General Description – Provides an introduction to the Model 990/10 Minicomputer System, describes the physical construction of the system and covers the various hardware options and system configurations which are currently available.

II. Field Service Test Equipment – Describes the 990 Maintenance Unit controls and indicators and provides test setup cabling diagrams for typical system installations. This section also lists the diagnostic tests that are currently available to support field maintenance and provides a list of recommended tools and test equipment.

III. Maintenance – Provides preventive and corrective maintenance procedures for the 990/10 system. This section describes the procedures for installing jumper-wire options and customer ROMs on replacement boards prior to substituting a spare board for a faulty board.

IV. Troubleshooting – Provides a systematic procedure for checking out a system and for tracing system malfunctions down to a replaceable subassembly. After the trouble has been isolated down to a replaceable unit, the unit is replaced in accordance with the instructions in Section III. The system checkout procedures in Section IV are then repeated to ensure that the system is functioning properly.

V. Troubleshooting Diagrams – Contains a collection of system-level diagrams useful in performing field maintenance, fault isolation and repair on the 990/10 system.

VI. Packing and Shipping – Contains instructions for repacking faulty assemblies for shipment back to the factory or other authorized depot maintenance facility.

A. Programming Reference Information – Provides a summary of 990 programming information required for field maintenance of the system.

B. Interrupt Vector Table – Tabular presentation of interrupt level and vector location.

C. Device CRU Formats – List and description of each.

D. Hexadecimal to Decimal Conversion Charts

E. Scoping Loop Programs – Provides a collection of commonly used scoping loops which may be entered into program memory via the programmers panel.

F. CRU Bit Assignments

G. Details of TILINE Operation

H. Detailed Description of CRU

I. ECC 16KB Expansion Board to Add-On Board Interface Signals

RELATED PUBLICATIONS

The following hardware, software and diagnostics publications are available to support programming, operation and maintenance of 990/10 systems:

PROGRAMMING. The following manual provides a detailed description of the instructions, the form and use of assembly language, plus programming conventions.

Title	Part Number
Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide	943441-9701

INSTALLATION AND OPERATION. The following series of manuals provide complete information to install and operate 990 peripheral devices including detailed unpacking, installation, operator controls and programming information.

Title	Part Number
Model 990 Computer Model 913 CRT Display Terminal Installation and Operation	943457-9701
Model 990 Computer Floppy Disc Installation and Operation Guide	945253-9701
Model 990/4 Program Development System Operation Guide	945254-9701
Model 990 Computer Prototyping System Operation Guide	945255-9701
Model 990 Computer PROM Programming Model Installation and Operation	945258-9701
Model 990 Computer 733 ASR/KSR Terminal Installation and Operation	945259-9701

Title	Part Number
Model 990 Computer Line Printer Installation and Operation	945261-9701
Model 990 Computer Card Reader Installation and Operation	945262-9701
Model 990 Computer Communications System Installation and Operation	945409-9701

HARDWARE. This manual presents a technical description of all hardware components in the processing unit. It includes interface descriptions, installation and operating instructions, electrical characteristics, and other essential data concerning the processor and associated chassis.

Title	Part Number
Model 990/10 Computer System Hardware Reference Manual	945417-9701

MAINTENANCE. The following manuals contain troubleshooting procedures for fault isolation to a replaceable assembly for each optional peripheral device. Also included are preventive maintenance requirements, disassembly, repair, and assembly instructions. These manuals are required for maintenance of any peripheral within the system.

Title	Part Number
Model 990 Computer Family Peripheral Equipment Field Maintenance Manual	945419-9701
Model 990 Computer Diagnostic Handbook	945400-9701
Model 990 Computer Family Maintenace Drawings Volume I – Processors	945421-9701*
Model 990 Computer Family Maintenance Drawings Volume II – Peripherals	945421-9702*

*Manual common to both Field and Depot level maintenance

The following manuals are available to enable qualified personnel to repair (at the component level) the major assemblies.

Title	Part Number
Model 990/10 Computer System Depot Maintenance Manual	945404-9701
Model 990 Computer PROM Programming Module Depot Maintenance Manual	945405-9701
Model 990 Computer Model 913 CRT Display Terminal Depot Maintenance Manual	945406-9701
Model 990 Computer 16 Input/Output TTL Data Module Depot Maintenance Manual	945407-9701

Title	Part Number
Model 990 Computer Full Duplex EIA Module Depot Maintenance Manual	945408-9701
Model 990 Computer 16 Input/Output EIA Data Module Depot Maintenance Manual	945415-9701
Model 990 Floppy Disc Depot Maintenance Manual	945418-9701
Model 990 Computer Family Maintenance Drawings Volume I – Processors	945421-9701*
Model 990 Computer Family Maintenance Drawings Volume II – Peripherals	945421-9702*

*Manual common to both Field and Depot level maintenance

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SECTION I

GENERAL DESCRIPTION

1.1 GENERAL

This section provides a brief physical and functional description of the 990/10 Minicomputer System and describes the various system- and board-level options available with the 990/10 equipment.

1.2 990/10 MINICOMPUTER SYSTEM DESCRIPTION

The 990/10 Minicomputer System is a modular data processing system (or general purpose hardware controller in some applications). The CPU is basically a TTL implementation of the microprocessor based on Texas Instruments Model 990/10 minicomputer and includes a wide range of supporting peripherals and controllers.

Typically, a system includes one or more 990/10 minicomputers, one or more (maximum of seven) 990 expansion chassis, and a combination of peripherals and terminals including:

- 913A video display terminals
- 911 video display terminals
- 733 ASR data terminals
- 743 KSR data terminals
- 804 card readers
- FD800 flexible discs(s)
- 306 or 588 line printers
- 979A mag tape transport(s)
- Model DS31 discs
- Model DS 25/50 discs
- Customer-designed controllers
- Communications network

A simplified block diagram of the 990/10 Minicomputer System is shown in figure 1-1. The 990/10 minicomputer and the I/O expansion chassis are described in greater detail in the following paragraphs. For a description of the peripherals and data terminals, refer to the *Model 990 Peripheral Device Field Maintenance Manual.*

1.2.1 990/10 MINICOMPUTER. The 990/10 minicomputer is a general-purpose computer available in two chassis configurations with a wide variety of optional memory boards, power supplies and I/O interface boards. Basically, the minicomputer consists of the following assemblies and subassemblies:

- AU1 board. Contains the ALU (Arithmetic Logic Unit), and ROM microsequencing and program control.
- AU2A (interface) board. Contains logic for interfacing the AU1 board and the rest of the system including the loader ROMs, the CRU interface, the TILINE interface, the front panel interface, the XOP (Extended Operations) interface, the interrupt interface and the clock circuit.

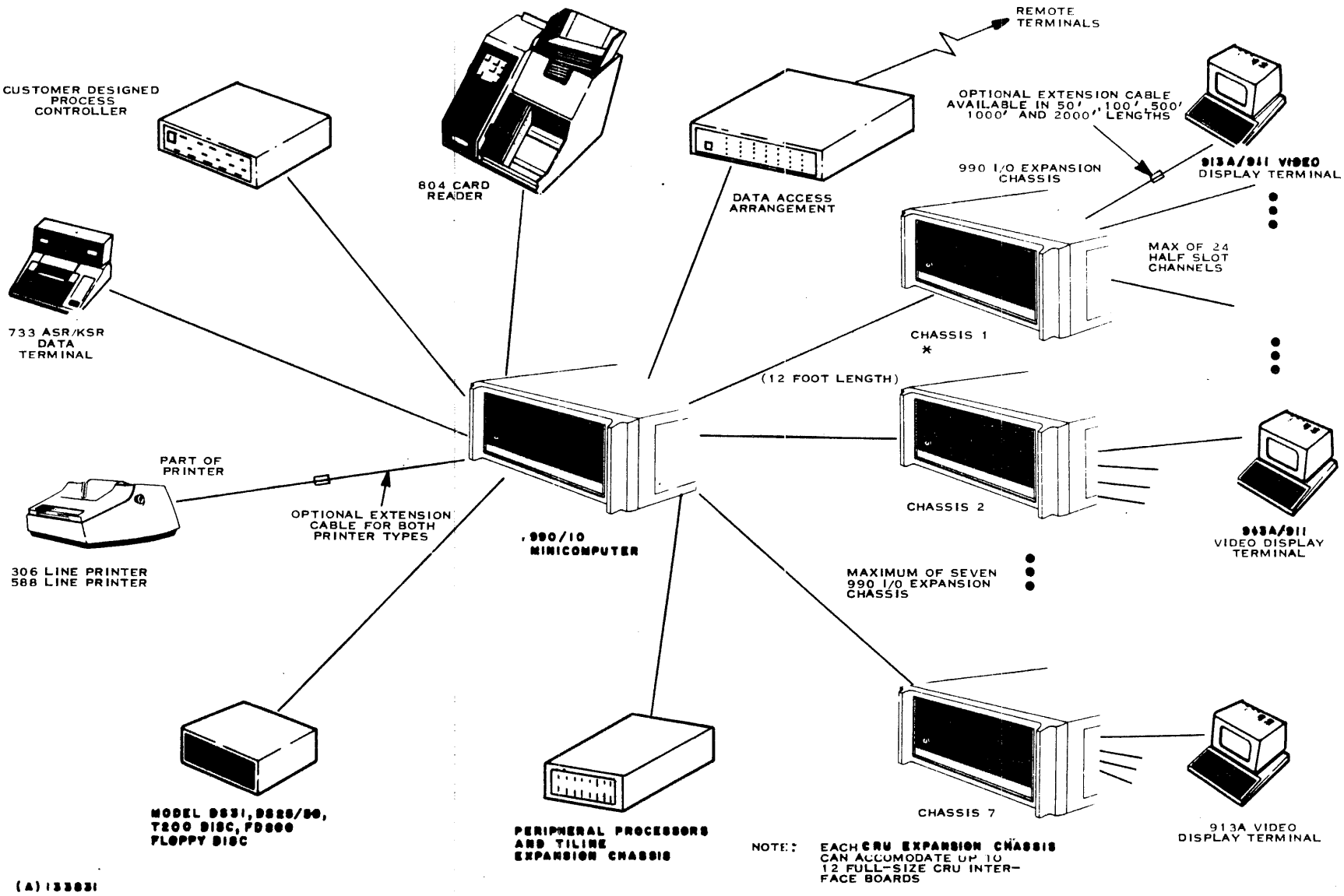

Figure 1-1. Typical 990/10 Minicomputer System

- AU2B (interface) board. Same as AU2A board but also contains mapping logic that permits the addressing of 2 million 8-bit bytes in RAM.

- Memory expansion board. Provides 16K bytes of RAM memory with a self-contained controller. Expandable in 8K-byte increments up to 40KB. Includes parity error detection as an option.

- ECC 16KB expansion board. Provides 16K-bytes of RAM memory with error checking and correction (ECC). On-board controller can control an additional add-on ECC board with up to 48K bytes of RAM.

- Add-On (Array) ECC Memory Board. Provides up to 48K bytes of ECC RAM memory in 16K byte increments. Each Add-on board requires a companion ECC 16K byte expansion board that provides the control function for the pair.

- Memory Controller, 96KB, with ECC, 990/16KR. Provides up to 96K bytes of MOS RAM with ECC in 32K-byte increments. The on-board memory control logic can control up to four additional add-on expansion memory boards, each with 256K bytes of memory with ECC.

- Memory Add-On Module, 256KB, with ECC, 990/16KR. Provides up to 256K bytes of MOS RAM with ECC in 64K-byte increments. Up to four of these add-on modules may be used with the companion Memory Controller, 96KB, with ECC, 990/10 board for a maximum memory size of 1 megabyte.

- Optional EPROM memory board. Contains erasable programmable read only memory (EPROM) in sizes ranging from 2K bytes to 16K bytes in 2K byte increments (field expandable).

- Optional CRU expansion board. Expands the I/O section of the 990/10 minicomputer board to accommodate up to seven additional I/O chassis.

- Optional I/O interface boards. Match the interface requirements of the 990/10 serial I/O section (CRU) with the interface requirements of various peripherals and terminals in the system.

- Chassis. Houses the above described logic boards and contains built-in regulated power supplies, cooling fans and control panel for all configurations.

The 990/10 minicomputer assemblies and subassemblies are shown in figure 1-2. A simplified block diagram showing the board-level organization of the 990/10 minicomputer is shown in figure 1-3. A functional description of each of the major assemblies and subassemblies is provided in the following paragraphs.

1.2.1.1 **990/10 Central Processing Unit.** The 990/10 CPU includes two full-size processor boards, AU1 and AU2. The AU1 board, also referred to as the processor board, contains the ALU and the control logic. The AU2 board, also referred to as the system interface board, contains the ROM Loader and the interface circuits that coordinate the AU1 board operation with the rest of the system. The detailed functions of the boards include the following:

AU1 board:

- Memory Address Register (MA)
- AU Registers (IR, ST, Level, MQ)
- Control ROM (C ROM) and Control Logic
- Register Files (includes WP and PC)
- ALU
- Source Data (SD)

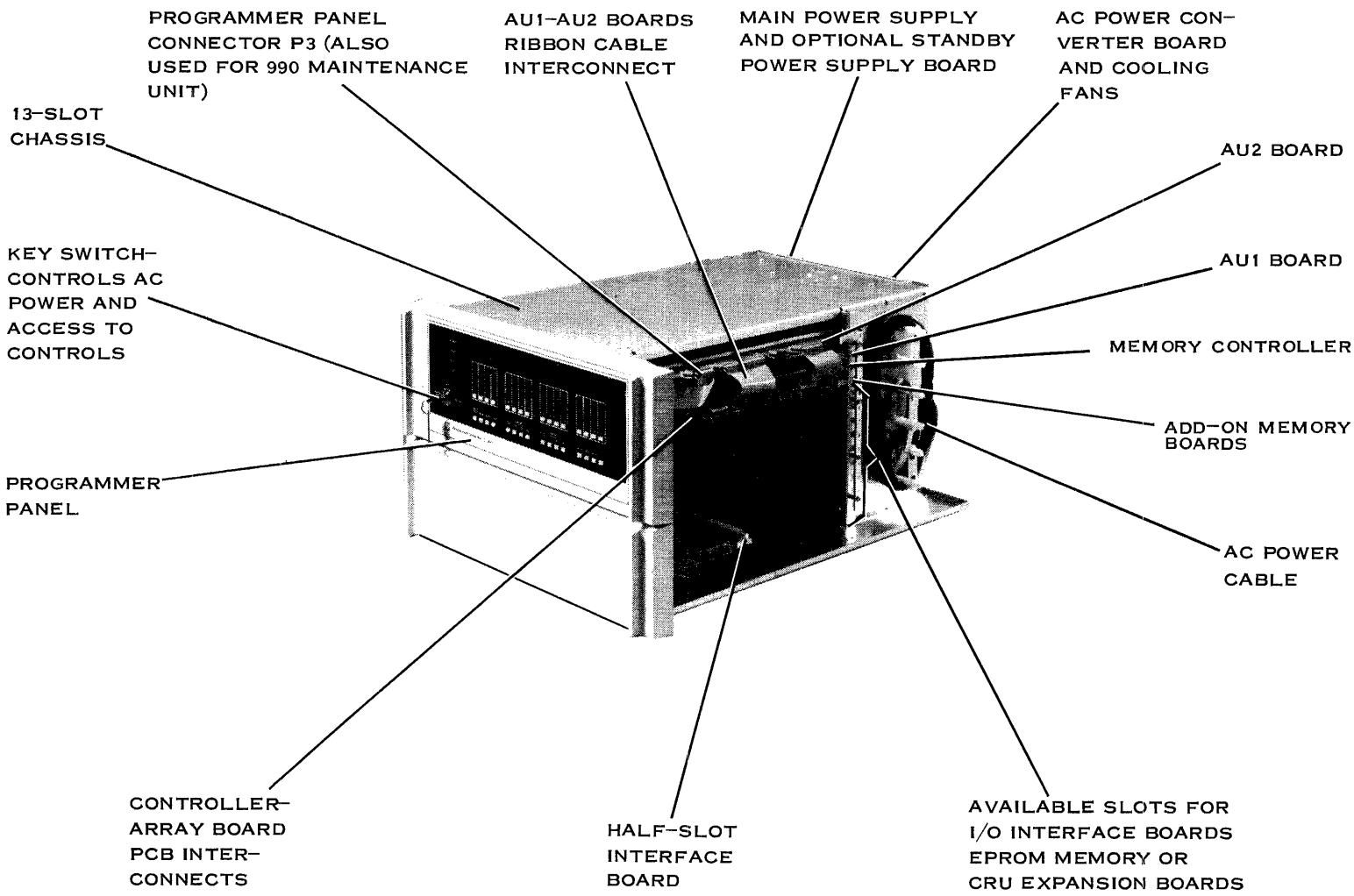

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Figure 1-2. 990/10 Minicomputer Assemblies and Subassemblies

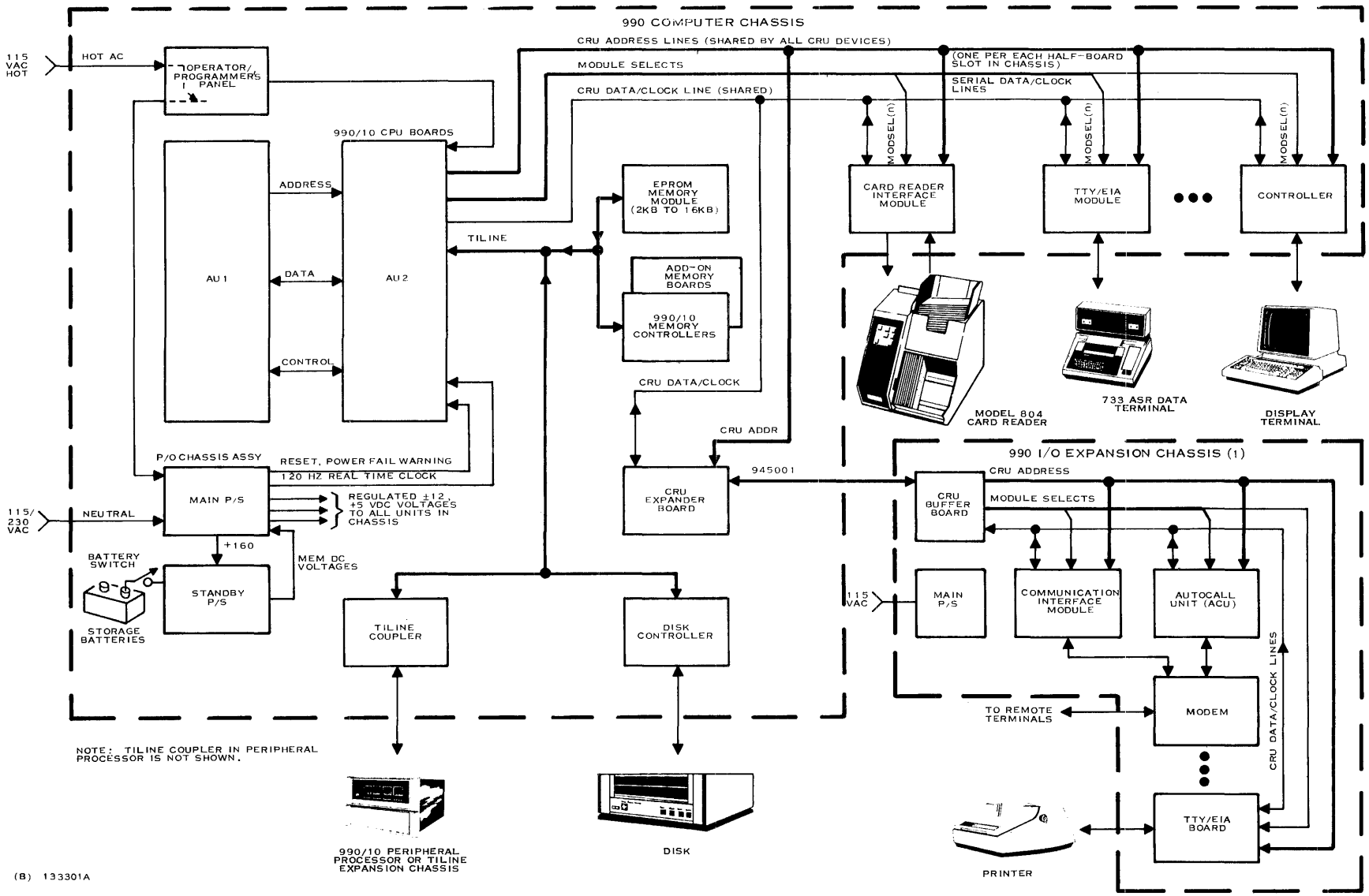


Figure 1-3. 990/10 Board Level Organization

AU2B Board:

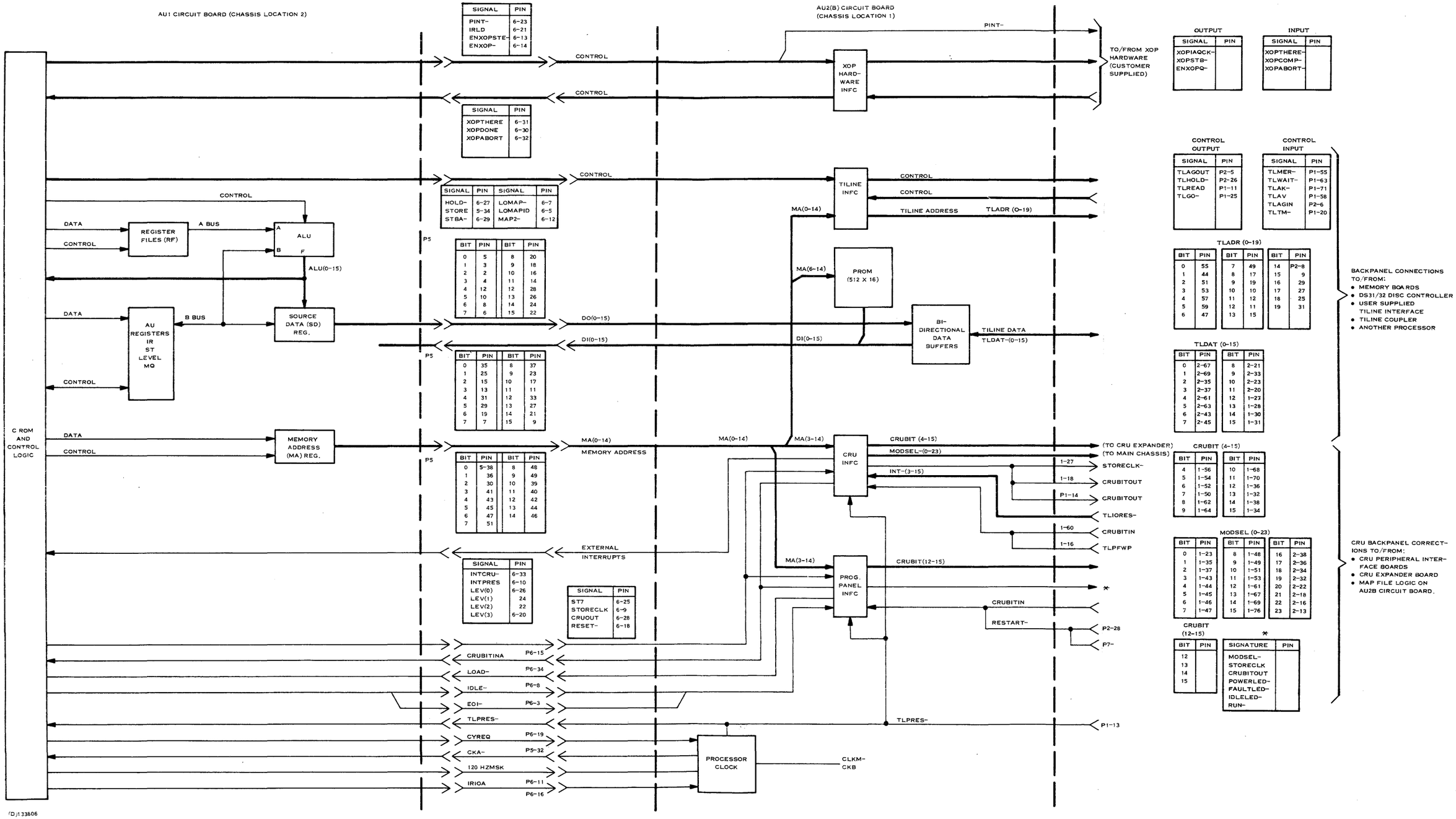
- Processor Clock
- Programmer Panel Interface
- CRU (Communication Register Unit) Interface
- PROM Loader
- TILINE (high-speed) Interface (including Memory Mapping)
- XOP (Extended Operations) Hardware Interface

A functional block diagram of the 990/10 CPU (including both boards) appears in figure 1-4. A brief functional description of the CPU follows.

Overall Operation of CPU. The 990/10 CPU uses a 20-bit address and a 16-bit data bus. The 990 concept features multiple register files (16 registers) that reside in memory. The advanced architecture of the 990/10 CPU permits efficient programming with bit, byte, and word addressing capability and the use of multiple register files allows rapid context switching. Characteristics of the 990/10 CPU are as shown in table 1-1.

The memory data word of the CPU is 16 bits long. Each word is also defined as 2 bytes of 8 bits each. The instruction set of 990/10 permits both word and byte operands. Thus, all memory word locations are on even byte address boundaries. Byte instructions can address either the even or odd byte. The memory space without mapping is 65536 bytes or 32768 words. Word and byte formats are as shown in figure 1-5.

The 990/10 processor employs an advanced memory-to-memory architecture. Blocks of memory designated as workspace replace internal hardware registers as program data registers. The 990/10 memory map is shown in figure 1-6. The first 32 words are used for 16 interrupt trap vectors with the first six words used for internal interrupts and the remaining 26 words used for 13 external equipment interrupts. The next contiguous block of 32 memory words is used by extended operation (XOP) instruction for trap vectors. Those addresses in the range $F800_{16}$ through $FBFE_{16}$ (512 words) are mapped to the TILINE peripheral control space ($FFC00_{16}$ through $FFDFE_{16}$) and the last 512 words (addresses $FC00_{16}$ through $FFFE_{16}$) are preempted to address the TTL P/ROM. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory. Three internal registers are accessible to the user. The program counter register (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically updated. The status register (ST) contains the interrupt mask level and status information pertaining to the instruction operation. Each bit position in the register signifies a particular function or condition that exists in the processor. Figure 1-7 illustrates the bit position assignments. Some instructions use the status register to check for a prerequisite condition, others affect the values of the bits in the register, and others load the entire status register with a new set of parameters. A description of the instruction set contained in the *Model 990 Computer Assembly Language Programmer's Guide* details the effect of each instruction on the status register.



SIGNAL	PIN
PINT-	6-23
IRLD	6-21
ENXOPSTB-	6-13
ENXOP-	6-14

SIGNAL	PIN
XOPTHERE	6-31
XOPDONE	6-30
XOPABORT	6-32

SIGNAL	PIN	SIGNAL	PIN
HOLD-	6-27	LOMAP-	6-7
STORE	5-34	LOMAPID	6-5
STBA-	6-29	MAP2-	6-12

BIT	PIN	BIT	PIN
0	5	8	20
1	3	9	18
2	2	10	16
3	4	11	14
4	12	12	28
5	10	13	26
6	8	14	24
7	6	15	22

BIT	PIN	BIT	PIN
0	35	8	37
1	25	9	23
2	15	10	17
3	13	11	11
4	31	12	33
5	29	13	27
6	19	14	21
7	7	15	9

BIT	PIN	BIT	PIN
0	5-38	8	48
1	36	9	49
2	30	10	39
3	41	11	40
4	43	12	42
5	45	13	44
6	47	14	46
7	51		

SIGNAL	PIN
INTCRU-	6-33
INTPRES	6-10
LEV(0)	6-26
LEV(1)	24
LEV(2)	22
LEV(3)	6-20

SIGNAL	PIN
ST7	6-25
STORECLK	6-9
CRUOUT	6-28
RESET-	6-18

OUTPUT

SIGNAL	PIN
XOPIAQCK-	
XOPSTB-	
ENXOPQ-	

INPUT

SIGNAL	PIN
XOPTHERE-	
XOPCOMP-	
XOPABORT-	

CONTROL OUTPUT

SIGNAL	PIN
TLAGOUT	P2-5
TLHOLD-	P2-26
TLREAD	P1-11
TLGO-	P1-25

CONTROL INPUT

SIGNAL	PIN
TLMER-	P1-55
TLWAIT-	P1-63
TLAK-	P1-71
TLAV	P1-58
TLAGIN	P2-6
TLTM-	P1-20

TLADR (0-19)

BIT	PIN	BIT	PIN	BIT	PIN
0	55	7	49	14	P2-8
1	44	8	17	15	9
2	51	9	19	16	29
3	53	10	10	17	27
4	57	11	12	18	25
5	59	12	11	19	31
6	47	13	15		

TLDAT (0-15)

BIT	PIN	BIT	PIN
0	2-67	8	2-21
1	2-69	9	2-33
2	2-35	10	2-23
3	2-37	11	2-20
4	2-61	12	1-22
5	2-63	13	1-28
6	2-43	14	1-30
7	2-45	15	1-31

CRUBIT (4-15)

BIT	PIN	BIT	PIN
4	1-56	10	1-68
5	1-54	11	1-70
6	1-52	12	1-36
7	1-50	13	1-32
8	1-62	14	1-38
9	1-64	15	1-34

MODSEL (0-23)

BIT	PIN	BIT	PIN	BIT	PIN
0	1-23	8	1-48	16	2-38
1	1-35	9	1-49	17	2-36
2	1-37	10	1-51	18	2-34
3	1-43	11	1-53	19	2-32
4	1-44	12	1-61	20	2-22
5	1-45	13	1-67	21	2-18
6	1-46	14	1-69	22	2-16
7	1-47	15	1-76	23	2-13

CRUBIT (12-15)

BIT	PIN
12	
13	
14	
15	

*

SIGNATURE	PIN
MODSEL-	
STORECLK	
CRUBITOUT	
POWERLED-	
FAULTLED-	
IDLELED-	
RUN-	

Figure 1-4. 990/10 CPU (AU1 and AU2), Functional Block Diagram

Table 1-1. 990/10 CPU Characteristics

Item	Characteristics
Byte Size	8 bits
Maximum memory addressing capability	64K bytes (without mapping). 2M bytes (with mapping)
Clock rate	Approximately 4 MHz
Addressing modes	Immediate Workspace register Workspace register indirect Symbolic memory (direct) Indexed memory Workspace register indirect autoincrement Program counter relative CRU relative
Interrupts	16 interrupts, 13 external
Registers	16
Input/output	Direct (CRU) and Direct Memory Access
Address bus	15 bits (Internal processor), 20 bits (TILINE)
Data bus	16 bits
Power	+12 Vdc, ±5 Vdc (memory and CPU)
Board size	10.8 by 14.25 inches

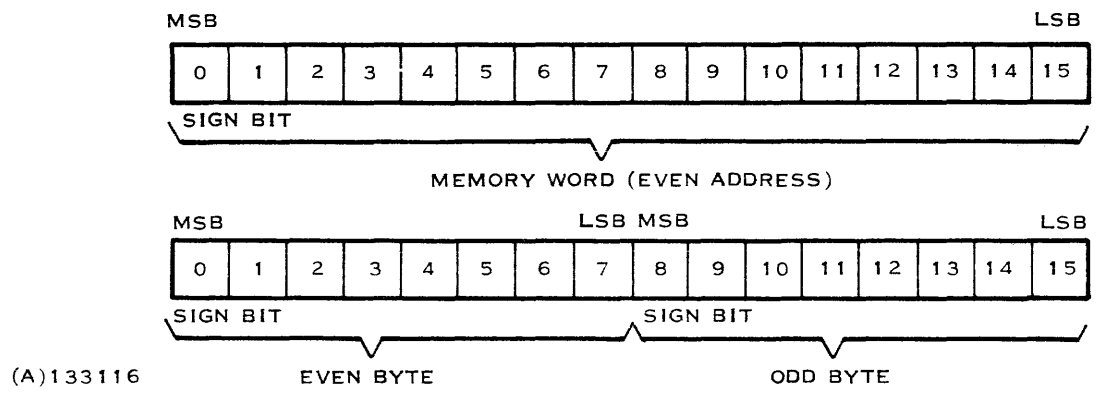


Figure 1-5. Processor Word and Byte Format

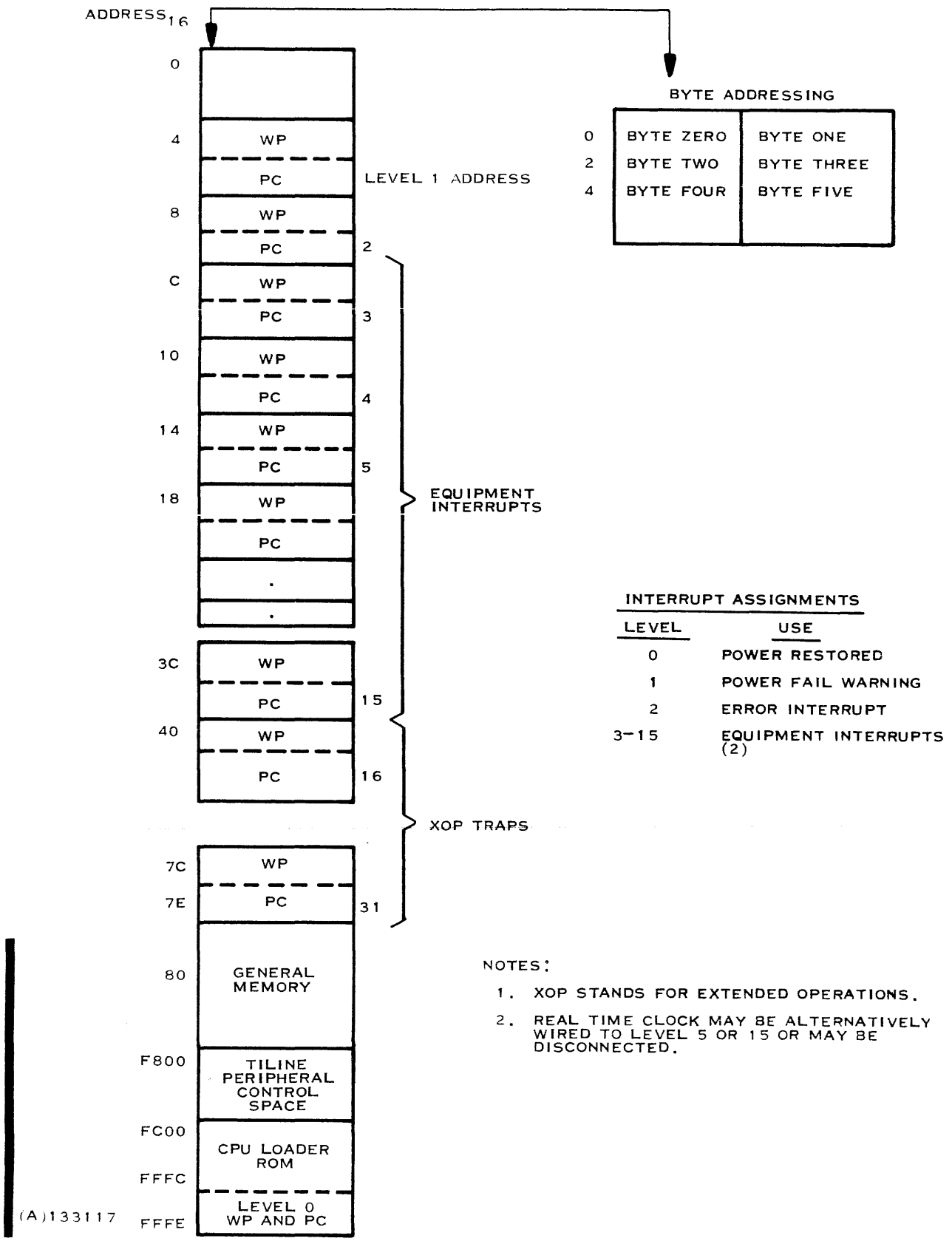


Figure 1-6. 990/10 Processor Memory Map

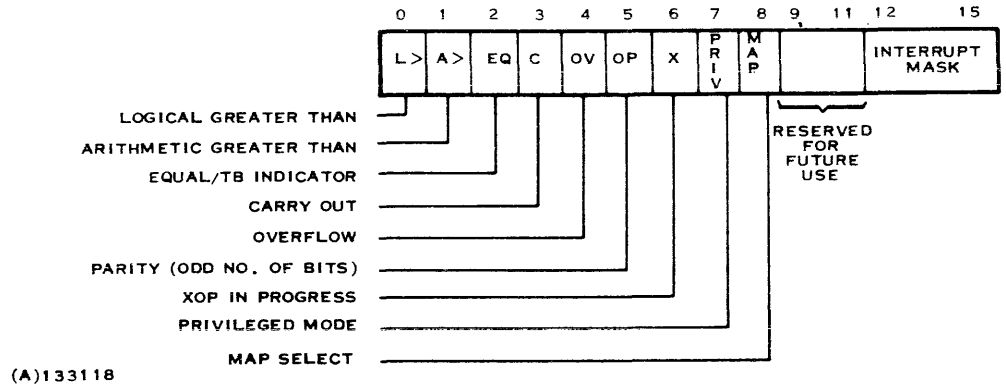


Figure 1-7. Status Register Bit Assignments

The workspace pointer register (WP) contains the address of the first word in currently active set of workspace registers. A workspace register file occupies 16 contiguous memory words in the general memory area (see figure 1-6). Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or index registers. Some workspace registers take on special significance during execution of certain instructions. Table 1-2 lists each of these dedicated workspace registers and the instructions that use them. During instruction execution, the processor addresses any register in the workspace by adding the register number to the contents of the workspace pointer as shown in figure 1-8.

The workspace concept is particularly valuable during operations that require a context switch (a change from one program to another or to a subroutine, as in the case of an interrupt). Such an operation using a conventional multiregister arrangement requires that at least part of the contents of the register file be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the contents of the program counter, status register, and workspace pointer the processor accomplishes a complete context switch with only three store cycles and three fetch cycles. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use in the new routine and the contents of the WP, PC, and ST registers from the previous routine have been saved in new workspace registers 13, 14, and 15, respectively. A corresponding saving in time occurs when the original context is restored. Instructions in the processor that result in a context switch include: Branch and Load Workspace Pointer (BLWP), Return from Subroutine (RTWP), and Extended Operation (XOP).

Device interrupts, TLPRES–, TLPFWP–, and RESTART– also cause a context switch by forcing the processor to trap to a service routine.

Interrupts. Sixteen priority-vectored interrupt levels are implemented in the 990/10 minicomputer. The interrupts generated by extended operation codes (XOPs) are not a part of the priority structure. When an interrupt is recognized by the hardware (interrupt pending at level not masked by status register mask), a BLWP instruction is forced using the words stored at the trap address for the recognized interrupt level for the workspace pointer and program counter. An RTWP instruction is used to exit from an interrupt subroutine and the prior operating environment is completely restored by the RTWP.

Table 1-2. Dedicated Workspace Registers

Register No.	Contents	Used During
0	Shift count (optional) Bits 12-15	Shift instructions (SLA, SRA, SRC and SRL)
11	Return address	Branch and Link Instruction (BL)
	Effective address	Software implemented Extended Operation (XOP)
12	CRU base address	CRU instructions (SBO, SBZ, TB, LDCR and STCR)
13	Saved WP register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD, and RESET)
14	Saved PC register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD, and RESET)
15	Saved ST register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD and RESET)

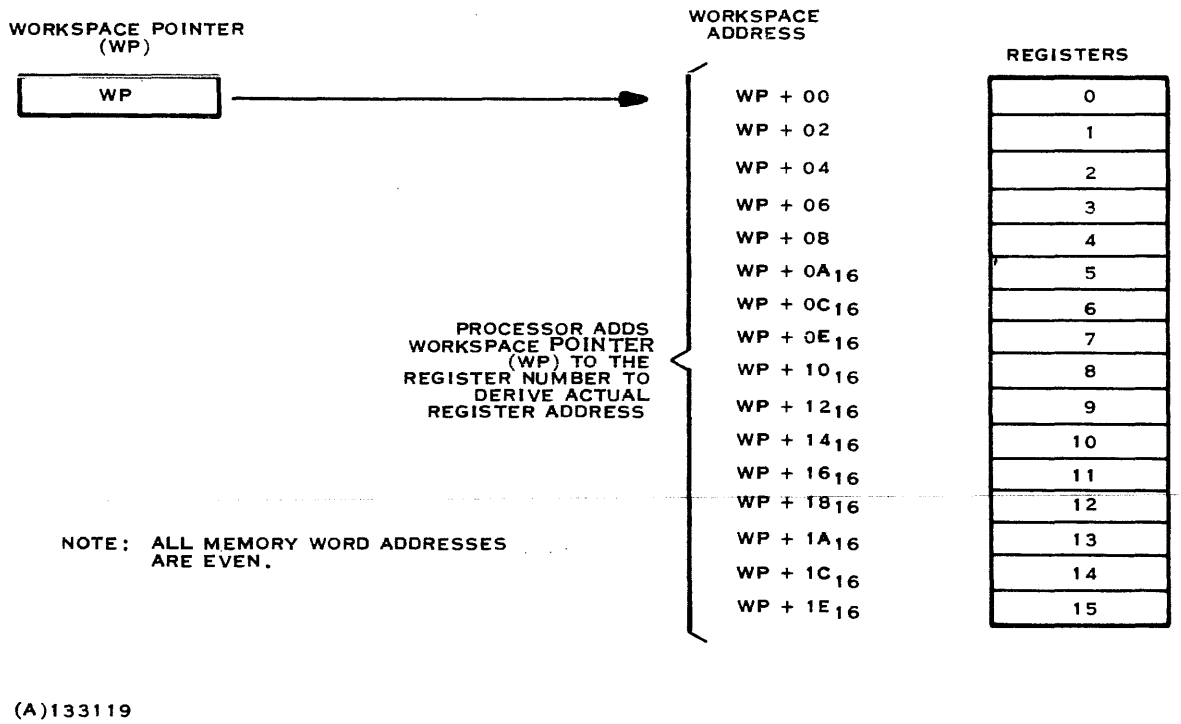


Figure 1-8. Workspace Pointer and Registers

Each of the interrupts has a priority level assigned that ranges from level 0 through level 15. Level 0 has the highest priority and level 15 has the lowest priority. Each priority level has two consecutive memory words with absolute trap addresses reserved for it (see processor memory map, figure 3-3). The first location contains a new workspace pointer and the second location contains a new program counter. Interrupts are enabled at a given level and of higher priority as specified by the four-bit field in the interrupt mask of the status register. Level 0 is the only level that cannot be disabled.

The processor continuously compares the interrupt code (LEV0 through LEV3) with the interrupt mask contained in status register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the processor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. Then, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15 of the new workspace. The processor then forces the interrupt mask to a value that is one less than the level of the interrupt being serviced, except for the level 0 interrupt that loads 0 into the mask. This allows only interrupts of higher priority to interrupt a service routine. The processor also inhibits interrupts until the first instruction of the service routine has been executed so that program linkage is preserved should a higher priority interrupt occur. All interrupt requests remain active until recognized by the processor in the device-service routine. The individual service routines must reset the interrupt requests before the routine is complete. If a higher priority interrupt occurs, a second context switch is made to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower priority interrupt. All interrupt subroutines should terminate with the return instruction to restore original program parameters.

The three highest priority level interrupts are reserved for internal interrupts. The highest of these, level 0, is the power restored interrupt. Any time ac power is restored to the CPU chassis, program execution will begin using the program counter and workspace pointer that were previously stored at the level 0 trap locations. The mask field of the status register is set to 0. This disables all interrupts except level 0. Level 0 interrupt cannot be disabled.

When the 990/10 power supply senses that a loss of ac power is imminent, an interrupt is generated and the processor has 7.0 milliseconds of program time before the system is reset for the power-loss state. This function is wired to the level 1 interrupt. The third internal interrupt is a merging of a number of error conditions. The error conditions are:

- Error (parity/error correcting) from TILINE memory (TLMER)
- Illegal operation (ILLOPSET)
- Privileged instruction fetch (PRIVOPSET) with privileged mode off (status register bit 7 = 1)
- TILINE timeout
- Memory mapping error (if memory mapping option implemented)

The error interrupt function is wired to the level 2 interrupt. Interrupt levels 3 through 15 are reserved for externally requested equipment interrupts. The reserved trap addresses for these levels are as shown in figure 1-6. The interrupt requests from the external devices (or from internal interrupt functions) may be wired to any of the thirteen interrupt request lines (INT3– through INT15–) on the edge connector of the system interface board (AU2). The lines form 13 separate wired-or interrupt buses. A 1-kilohm pull-up resistor is supplied on the board for each line and each interrupt request signal should be an active low signal driven by an open-collector TTL gate. The request signal should remain on the respective interrupt bus until it is reset by software communication. The request signal should be reset at some time before the interrupt service program executes RTWP or the processor will repeat the trap.

TILINE Peripheral Control Space (TPCS). The TILINE peripheral control space (TPCS) consists of those central processor addresses in the range $F800_{16}$ through $FBFE_{16}$ (see memory map, figure 1-6). The addresses ($F800_{16}$ through $FBFE_{16}$) are modified before presentation to the TILINE. Five address bits are appended to the left (most significant bit side) of each address in order to form a 20-bit TILINE word address. In other words, addresses 0000 to $F800_{16}$ are passed through to the TILINE so as to address the first 62K bytes of the 2M bytes of TILINE address space. Addresses $F800_{16}$ through $FBFE_{16}$ are mapped to addresses $FFC00_{16}$ through $FFDFE_{16}$ of the 2M-byte word address space. Memory commands associated with locations $FC00_{16}$ through $FFFE_{16}$ address the TTL PROM loader on the system interface board (AU2).

Input/Output. The 990/10 minicomputer uses a versatile direct command-driven I/O interface designated as the Communications Register Unit (CRU). The CRU provides up to 4096 directly addressable input bits and 4096 directly addressable output bits. Both input and output bits can be addressed individually or in fields of from 1 to 16 bits. The processor employs three dedicated I/O pins (CRUBITIN, CRUBITOUT, and STORECLK–) and 12 bits (CRUBIT4 through CRUBIT15) of the address bus at the interface to the CRU system. The processor instructions that drive the CRU interface can set, reset, or test any bit in the CRU array or move data between memory and CRU data fields.

Because of its extremely flexible data format, the CRU interface can be used effectively for a wide range of control and data transaction operations. These applications can be divided into two broad categories: those involving a single control bit transfer, and those requiring input or output of several data or status bits.

The processor performs three single-bit CRU functions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the processor develops a CRU-bit address and places it on the address bus, CRUBIT4 through CRUBIT15.

For the two output operations (SBO and SBZ), the processor generates a STORECLK– pulse that indicates to the CRU device that the operation is one of output and places bit 7 of the instruction word on the CRUBITOUT line to accomplish the specified operation (bit 7 is a ONE for SBO and a ZERO for SBZ). The test bit instruction is an input operation that transfers the addressed CRU bit from the CRUBITIN input line to bit 2 (equal bit, see figure 1-7) of the status register.

The processor develops a CRU-bit address for the single-bit operations from the CRU base address contained in workspace register 12 (W12) and the signed displacement contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from W12 (in bits 3-14) is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 1-9 illustrates the development of a single-bit CRU address.

The processor performs two multiple-bit CRU operations: store communications register (STCR) and load communications register (LDCR). Both operations perform a data transfer from the CRU-to-memory or from memory-to-CRU as illustrated in figure 1-10. Although the figure shows a full 16-bit transfer operation, any number of bits from 1 to 16 may be involved. The LDCR instruction fetches a word from memory and right-shifts it to serially transfer it to CRU output bits. If the LDCR involves 8 or fewer bits, those bits come from the right-justified field within the addressed byte of the memory word. If the LDCR involves 9 or more bits, those bits come from the right-justified field within the whole memory word. As the bits are transferred to the CRU interface, the CRU address is incremented for each successive bit. This addressing mechanism results in an order reversal of the bit; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressed bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

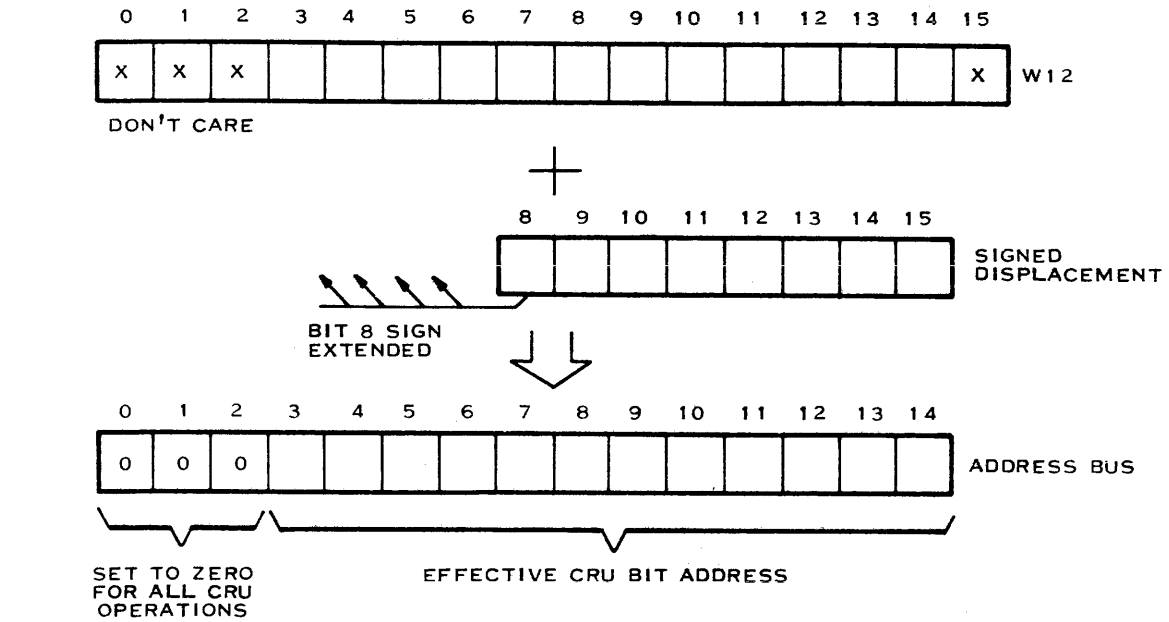


Figure 1-9. 990/10 Single-Bit CRU Address Development

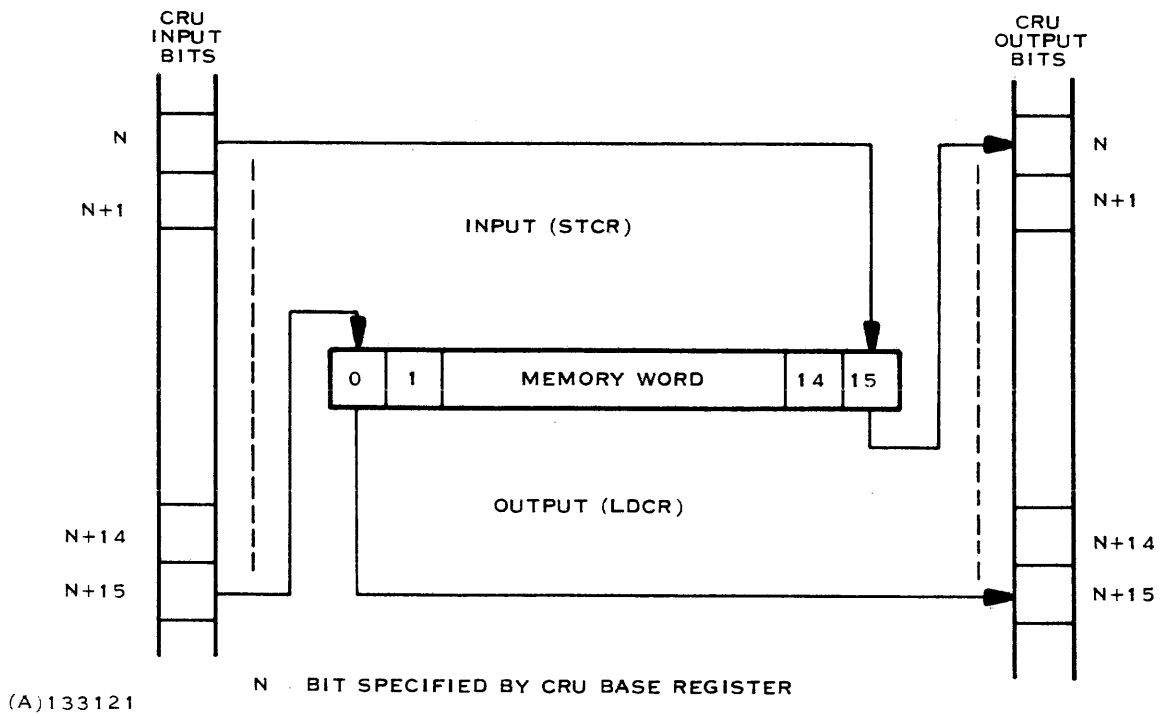


Figure 1-10. 990/10 LDCR/STCR Data Transfers

An STCR instruction transfers data from the CRU to memory. If the operation involves a byte or less transfer, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves 9 to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to zero. When the input from the CRU device is complete, the first bit from the CRU is in the least significant bit position in the memory word or byte.

Load Function. The RESTART– signal permits cold-start ROM loaders and front panel routines to be implemented for the processor. When active, RESTART– causes the processor to initiate a trap immediately following the instruction being executed. RESTART– is an unmaskable interrupt that traps to the TTL PROM loader location $FFFC_{16}$ to obtain the trap vector (WP and PC). The old PC, WP, and ST are loaded into the new workspace and the interrupt mask is set to zero. Then, program execution resumes using the new PC and WP. The RESTART– signal comes into the system interface board either from the backpanel or from the programmer panel connector. The load function can also be initiated by execution of an LREX instruction or through the programmer panel single-instruction (SIE) function.

Privileged Instructions. Certain machine instructions of the 990/10 are treated as privileged instructions and will execute only when the computer is in the privileged mode (bit 7 of the status register equals 0). The attempt to execute a privileged instruction when the computer is not in the privileged mode causes an error condition and a trap through interrupt level 2 (except for instruction RTWP). The privileged instructions are: LIMI, LMF, LDS, LDD, LREX, RSET, CKON, CKOF, IDLE, and RTWP. When any interrupt trap is taken, bit 7 of the status register is cleared to 0 to allow proper interrupt processing. The instruction RTWP executes normally except that during the workspace register 15 to status register transfer, bits 7, 8, and 12 through 15 are not loaded.

Additionally, the addressing of CRU output bits at address $\geq E00_{16}$ (CRU base address $1C00_{16}$) is privileged.

Illegal Operation Codes. When the processor acquires an instruction from memory that cannot be executed, it generates a level 2 error interrupt. A detailed description of error interrupts and illegal operation codes is provided in the *Model 990/10 Computer System Hardware Reference Manual*, Part Number 945417-9701.

Real Time Clock. A line frequency synchronized oscillator on the power supply is an input to the central processor. On every cycle of the oscillator, the real time clock interrupt function is generated. This function may be connected with jumper wires to interrupt level 5 or interrupt level 15 or may be disconnected. The CKON and CKOF instructions are used to enable and disable the real time clock interrupt function independent of the status register mask. This function is normally cleared in the "clock interrupt service routine" with a CKOF-CKON instruction sequence.

XOP Hardware. As a performance enhancement, the 990/10 provides an interface to customer-supplied external hardware modules that execute customer defined instructions while the processor waits for the results. If the external modules are not attached, the processor traps to emulation subroutines instead. A detailed description of the XOP hardware interface logic as implemented on the 990/10 is provided in the *Model 990/10 Computer System Hardware Reference Manual*, Part Number 945417-9701.

Programmer Panel Interface. The 990/10 provides an interface to a programmer panel. The programmer panel is a CRU device that is addressed at CRU base address $1FE0_{16}$. A detailed description of the programmer panel interface is provided in the *Model 990/10 Computer System Hardware Reference Manual*, Part Number 945417-9701. Appendix F provides the CRU bit assignments for base address $1FE0_{16}$. The following programmer panel functions are implemented directly by the 990/10.

- Power LED – Power reset is inverted and supplied to the programmer panel connector through a 180-ohm resistor.
- Fault LED – An SBO instruction to CRU bit 11 causes the FAULT light on both the programmer panel and the system interface board (AU2) to light. The fault indicator flip-flop is buffered to drive both lamps. An I/O reset or an SBZ instruction turns off the fault lamps. A power reset turns the lamps on. The FAULT signal is supplied to the programmer panel through a 180-ohm resistor.
- Run LED – An SBO or SBZ instruction to CRU bit 10 causes the RUN indicator on the programmer panel to illuminate. A power reset also illuminates the RUN indicator. The RUN function is automatically cleared by a RESTART– signal or by setting the single-instruction execute function (programmer panel CRU output bit 14). The RUN signal is supplied to the programmer panel through a 180-ohm resistor.
- Memory error interrupt clear – An SBO or SBZ instruction to CRU bit 12 clears a memory error interrupt.
- Single Instruction Execute (SIE) – An SBO or SBZ instruction to CRU bit 14 causes the load function to be executed after two additional instructions.
- Idle LED – The IDLE– signal from the processor is buffered and provided to the programmer panel connector through a 390-ohm resistor as the IDLELED– signal.

Processor Board to System Interface Board Signals. The interface between the processor board (AU1) and the system interface board (AU2) consists of the following functions:

- Mapping option (on AU2B board only)
- XOP (hardware)
- Data and Address Buses
- CRU interface
- Interrupts
- Clock/clear

The interface is made between the two boards with two short ribbon cables connected to connectors P5 and P6 near the top edge of each board. Pin assignments are the same for both boards. Pin assignments and interface signal functions are described in table 1-3. The input/output (I/O) column of the table is in reference to the AU1 circuit board.

Table 1-3. Processor/System Interface Board Interface Pin Assignments and Functions

Signature	Pin	I/O*	Description
MA0(MSB)	P5-38	OUT	MA0 through MA14 comprise the address bus.
MA1	P5-36	OUT	
MA2	P5-30	OUT	
MA3	P5-41	OUT	
MA4	P5-43	OUT	
MA5	P5-45	OUT	
MA6	P5-47	OUT	
MA7	P5-50	OUT	
MA8	P5-48	OUT	
MA9	P5-49	OUT	
MA10	P5-39	OUT	
MA11	P5-40	OUT	
MA12	P5-42	OUT	
MA13	P5-44	OUT	
MA14(LSB)	P5-46	OUT	
DI0(MSB)	P5-35	IN	DI0 through DI15 comprise the memory read data bus.
DI1	P5-25	IN	
DI2	P5-15	IN	
DI3	P5-13	IN	
DI4	P5-31	IN	
DI5	P5-29	IN	
DI6	P5-19	IN	
DI7	P5-7	IN	
DI8	P5-37	IN	
DI9	P5-23	IN	
DI10	P5-17	IN	
DI11	P5-11	IN	
DI12	P5-33	IN	
DI13	P5-27	IN	
DI14	P5-21	IN	
DI15(LSB)	P5-9	IN	
DO0(MSB)	P5-5	OUT	DO0 through DO15 comprise the memory write data bus.
DO1	P5-3	OUT	
DO2	P5-32	OUT	
DO3	P5-4	OUT	
DO4	P5-12	OUT	
DO5	P5-10	OUT	
DO6	P5-8	OUT	
DO7	P5-6	OUT	
DO8	P5-20	OUT	
DO9	P5-18	OUT	
DO10	P5-16	OUT	
DO11	P5-14	OUT	
DO12	P5-28	OUT	
DO13	P5-26	OUT	
DO14	P5-24	OUT	
DO15(LSB)	P5-22	OUT	

*Input/output is in reference to the processor board.

Table 1-3. Processor/System Interface Board Interface Pin Assignments and Functions (Continued)

Signature	Pin	I/O*	Description
CYREQ	P6-19	OUT	When active (high) indicates that the present clock period is for a memory cycle.
STORE	P5-34	OUT	When high indicates that the memory cycle request is for a write cycle.
HOLD--	P6-27	OUT	A TILINE control signal that suspends control contention during the processing of an ABS instruction so that the effective address can be read, tested, and changed before another master device can have access to memory. This is to assure the validity of global software interlocks in multiprocessor systems.
INTPRES	P6-10	IN	Interrupt present. When active (high) indicates that an interrupt is requested. If INTPRES is active, the processor loads the data on the interrupt-code input lines LEV0 through LEV3 into an interrupt-code storage register. The code is compared to the interrupt bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal to or less than status register bits 12 through 15) the processor interrupt sequence is initiated. If the comparison fails, the processor ignores the request. INTPRES remains active and the processor will continue to sample LEV0 through LEV3 until the program enables a priority low enough to accept the requested interrupt.
LEV0(MSB) LEV1 LEV2 LEV3(LSB)	P6-26 P6-24 P6-22 P6-20	IN IN IN IN	Interrupt codes. LEV0 is the MSB of the interrupt code that is sampled when INTPRES is active. When LEV0 through LEV3 are LLLH, the highest priority interrupt is being requested and when HHHH, the lowest priority interrupt is being requested.
STORECLK	P6-9	OUT	CRU clock enable. When active (high) and ANDed with system clock, develops signal that indicates to addressed CRU device that data on CRUBITOUT should be sampled.
CRUBITINA	P6-15	IN	CRU data in. When the processor executes an STCR or TB instruction, it samples CRUBITINA for the level of the CRU input bit specified by the address bus (MA3 through MA14).
CRUOUT	P6-28	OUT	CRU data out. Serial data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT is sampled by external I/O interface logic at the CRU interface on the positive-going edge of STORECLK–.
INTCRU–	P6-33	IN	When low indicates to processor that CRU address is in the main chassis and that CRU input data can be processed at the 4-MHz rate.
ST8A–	P6-29	OUT	When ST8A– is high (status register bit 8 is low) indicates that MAP0 is to be used during a nonlong distance memory reference.
IRLD	P6-21	OUT	Indicates that the current memory request is an instruction fetch. Signal is used to develop the XOP hardware interface signal XOPIAQCK–.
XOPTHERE	P6-31	IN	Input signal to processor to indicate that a hardware module is available to perform the indicated XOP function.

*Input/output is in reference to the processor board.

Table 1-3. Processor/System Interface Board Interface Pin Assignments and Functions (Continued)

Signature	Pin	I/O*	Description
XOPDONE	P6-30	IN	Input signal to processor developed by either a XOPABORT-- or a XOPCOM-- signal from an XOP hardware module to indicate that an operation was aborted before completion or was successfully completed.
XOPABORT	P6-32	IN	Input signal to processor developed by XOPABORT– signal from an XOP hardware module to signify that the module has terminated an operation before completion.
ENXOPSTB–	P6-13	OUT	Output signal from the processor that develops the XOPSTB– signal to the XOP hardware module to indicate that the effective address has been calculated and is available on the address bus.
ENXOP–	P6-14	OUT	Signal from the processor that develops the ENXOPQ– signal to the hardware module to permit the module to start processing.
CKA–	P5-2	IN	Clock signal generated on AU2 (the system interface board) used to drive AU1 (processor board).
RESET–	P6-18	OUT	Signal generated during the execution of the RSET instruction.
PRIVOPSET–	P6-4	OUT	Signal generated by processor to indicate a privileged instruction fetch attempt when not in privileged mode (status register bit 7 = 1).
ILLOPSET–	P6-6	OUT	Signal generated by processor to indicate that an illegal operation code has been decoded.
PINT–	P6-23	OUT	A low active signal from the processor to indicate to an XOP hardware module the presence of an interrupt.
IR10A	P6-16	OUT	Instruction register bit 10 – high for a CKON instruction to enable the real time clock; set low for a CKOF instruction to disable the real time clock.
ST7	P6-25	OUT	Status register bit 7. Privileged instructions will execute only when register bit 7 is set to 0.
IDLE–	P6-8	OUT	A signal from the processor to the system interface board indicating processor idle mode.
120HZMSK	P6-11	OUT	A signal from the processor that masks the real time clock so that once an interrupt has been generated, a CKOF, CKON instruction sequence is required to generate a second interrupt.
LOAD–	P6-34	IN	A low active signal to the processor indicating that a restart trap has been requested.
LDMAP–	P6-7	OUT	A low active signal from the processor indicating that map-load data is present on internal data lines (applicable to 990/10 with map option).
LDMAPID–	P6-5	OUT	A signal from the processor indicating whether map 0 or map 1 is designated for loading (applicable to 990/10 with map option).
MAP2–	P6-12	OUT	A signal from the processor that indicates when active (low) that ST8A– should be overridden and map 2 be used instead of map 0 or map 1 (applicable to 990/10 with map option).

*Input/output is in reference to the processor board.

Table 1-3. Processor/System Interface Board Interface Pin Assignments and Functions (Continued)

Signature	Pin	I/O*	Description
EOI–	P6-3	OUT	A signal from the processor indicating the last state of an instruction.
HALT–	P6-17	IN	A breakpoint input signal to the processor.

*Input/output is in reference to the processor board.

TILINE. The 990/10 computer uses a high-speed, bidirectional 16-bit data bus called the TILINE that with associated control lines serves to transfer data between all high-speed system elements. These elements include the central processor, the memory, and other rapid data transfer devices such as disc files and magnetic tape transports. The TILINE also serves as a computer-to-computer link and is the backbone of multiprocessor systems.

The TILINE operates asynchronously and the speed of data transfers over the TILINE is governed by distance between and the speed of the devices connected to the TILINE. Consequently, system performance can be tailored to the application by suitable choice of devices and can be upgraded easily as needed.

The devices connected to the TILINE compete for access to the bus through a positional priority system. High-speed peripherals are usually assigned highest priority and the central processor is assigned the lowest priority. In operation, an efficient cycle-stealing action occurs. The overhead time required for switching from central processor access to another device is overlapped with the data transfer. This permits a very high rate of device switching without sacrificing overall data bandwidth. Details of TILINE operation are included in Appendix G.

AU1 Board Component Location. The locations of the major components on the AU1 board are indicated in figure 1-11.

Memory Address Register (MA). As shown in figure 1-4, the MA Register in the AU1 board receives address and control signals from the C ROM and Control Logic. The MA register outputs the memory address to the CRU Interface, the TILINE Interface, the Front Panel and Loader PROM, and the Front Panel Interface on the AU2 board. In the normal sequencing of instructions, the memory address is incremented by 2 to provide the address for the next memory fetch.

AU Registers. The instruction fetched from memory is loaded into the Instruction Register (IR) and is used to drive the C ROM and Control Logic. The AU registers (including the Status Register) also provide B-Bus inputs to the B input of the ALU as indicated in figure 1-4.

Control ROM (C ROM) and Control Logic. The C ROM and Control Logic uses the instruction bits stored in the IR to generate the microinstruction control signals for the CPU. This part of the AU1 board (see figure 1-4) also receives signals from the AU2 board that are used in developing the control signals.

Register Files. Four hardware registers, including the WP and the PC, supply A-Bus inputs to the ALU as indicated in figure 1-4. Source and Destination operand addresses may be stored in the two registers not dedicated to WP and PC.

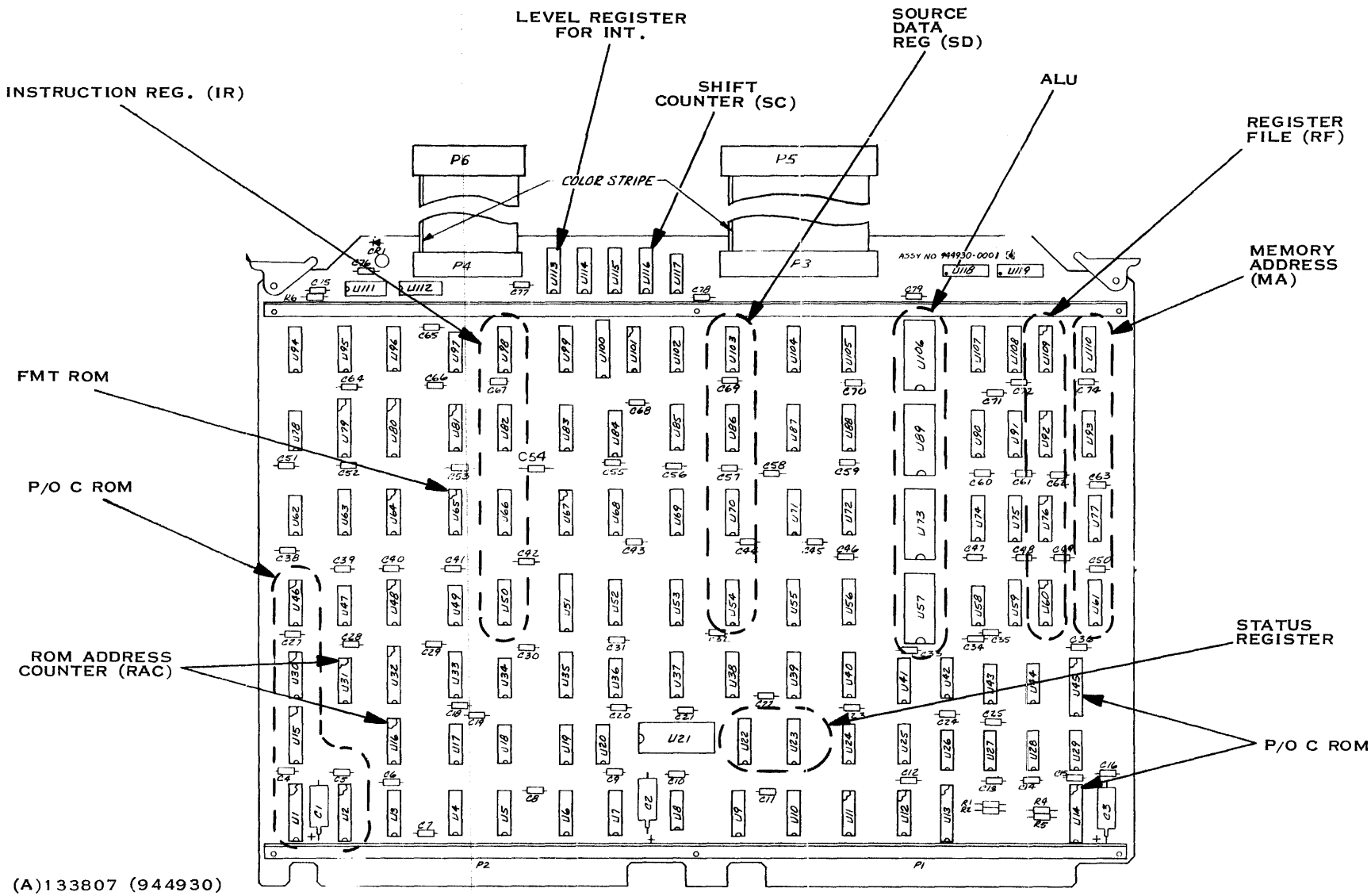


Figure 1-11. AU1 Board Component Location

Arithmetic Logic Unit (ALU). As shown in figure 1-4, the ALU receives A-Bus and B-Bus input signals from one of the register file registers and one of the AU registers, respectively, and responds to an input control signal to provide the desired output. The ALU output drives the Source Data (SD) register as well as the C-Bus multiplexers.

Source Data Register (SD). The SD register supplies the data out signals DO(0-15) that are routed to the buffers in the AU2 board that drive the TILINE. The source data register may also supply signals to the B Bus.

AU2 Boards Component Location. The locations of the major components on the AU2 and AU2B boards and indicated in figures 1-12 and 1-13, respectively.

Processor Clock. The processor clock circuit (figure 1-4) is located on the interface (AU2) board. Timing and control for the processor on the AU1 circuit board, for control and interrupt logic on the system interface board, and timing for the CRU interface and for the TILINE are derived from the system clock that is located on the system interface board.

Programmer Panel Interface. The programmer panel interface circuit on the AU2 board is a CRU device as indicated in figure 1-4. It receives memory address signals, as well as CRU and indicator driving signals, and provides panel control signals to the CPU.

CRU (Communications Register Unit) Interface. Logic for the CRU is mounted on the system interface circuit board. This logic controls the CRU data and control lines. These lines are connected to all main chassis locations except for the two slot locations used by the processor board AU1. Twenty four module select signals are decoded by CRU interface logic and are made available to 11 chassis locations in the 13-slot chassis. Only eight of the module select signals are used for the four available slots used in the 6-slot chassis. Each chassis location (full-sized slot) accommodates one double-connector circuit board or two single-connector circuit boards. Details on the operation of the CRU appear in Appendix H.

PROM Loader. Up to 512 words of TTL programmable read-only memory (PROM) in 256-word increments may be implemented on the system interface board by installing four 256-word by 8-bit PROM devices in the four sockets provided. The TTL PROM may be implemented in one of several loader options with or without a self-test feature. The PROM devices are the Texas Instruments SN74S471s that can be electronically permanently programmed and may be furnished to the user unprogrammed to permit development by the user of a custom loader. A low level signal is required at both of two chip-select pins of the PROM device to enable the device. When not enabled, the high-impedance three-state output of the device permits direct interface with the TILINE data bus.

TILINE Interface. The TILINE interface in the AU2 board consists of the 3-state circuits, send and receive, required for data and address signals on the bus. The AU2B board includes the mapping circuitry in the TILINE interface that makes it possible to address 1024K words of memory. Details on TILINE operation are included in Appendix G.

XOP Hardware Interface. Interface circuitry for the XOP hardware is mounted on the AU2 board interface boards. The XOP hardware itself connects to the small connector at the top of the interface board (see figures 1-12 and 1-13).

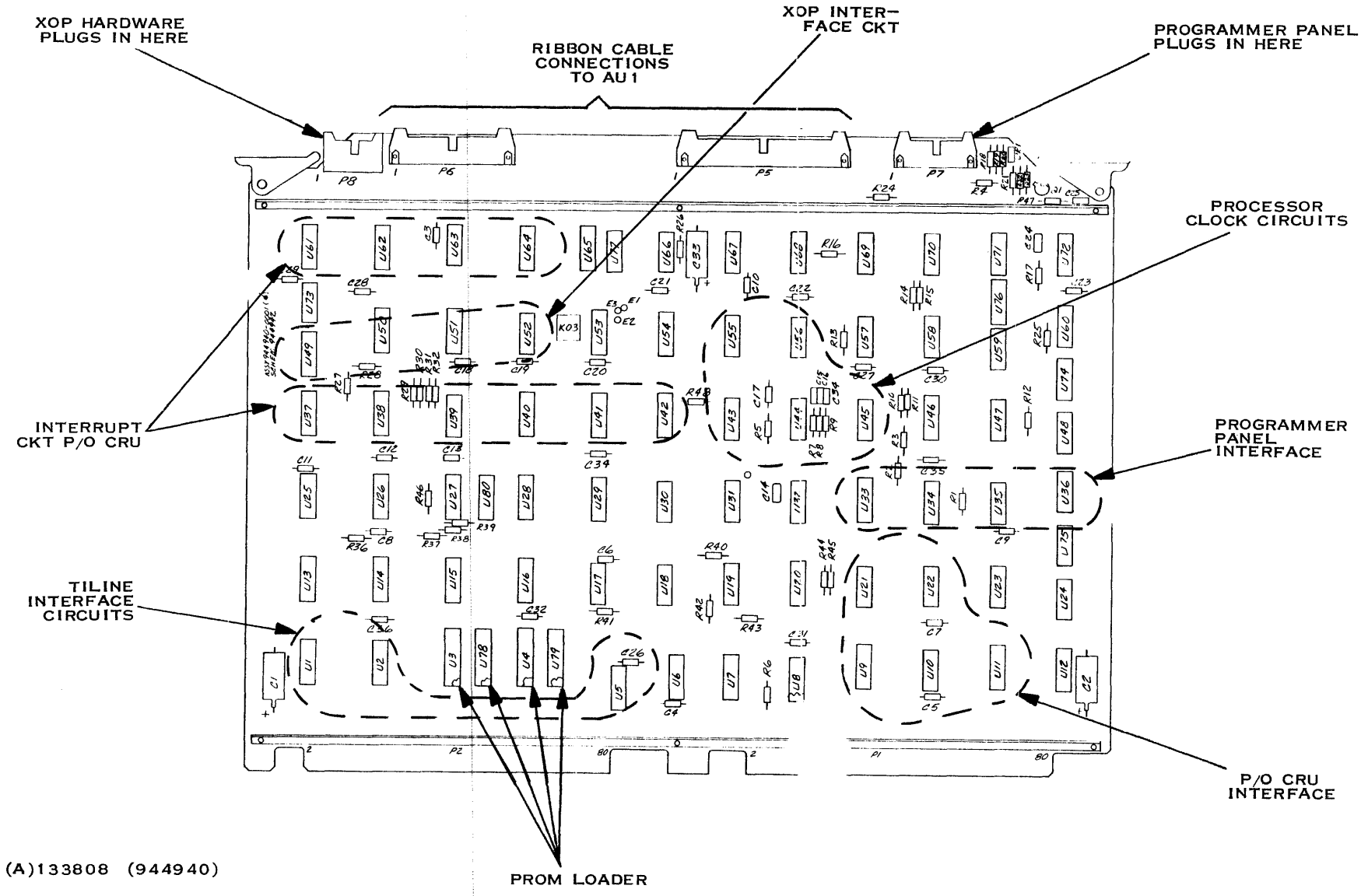


Figure 1-12. AU2 Board Component Location

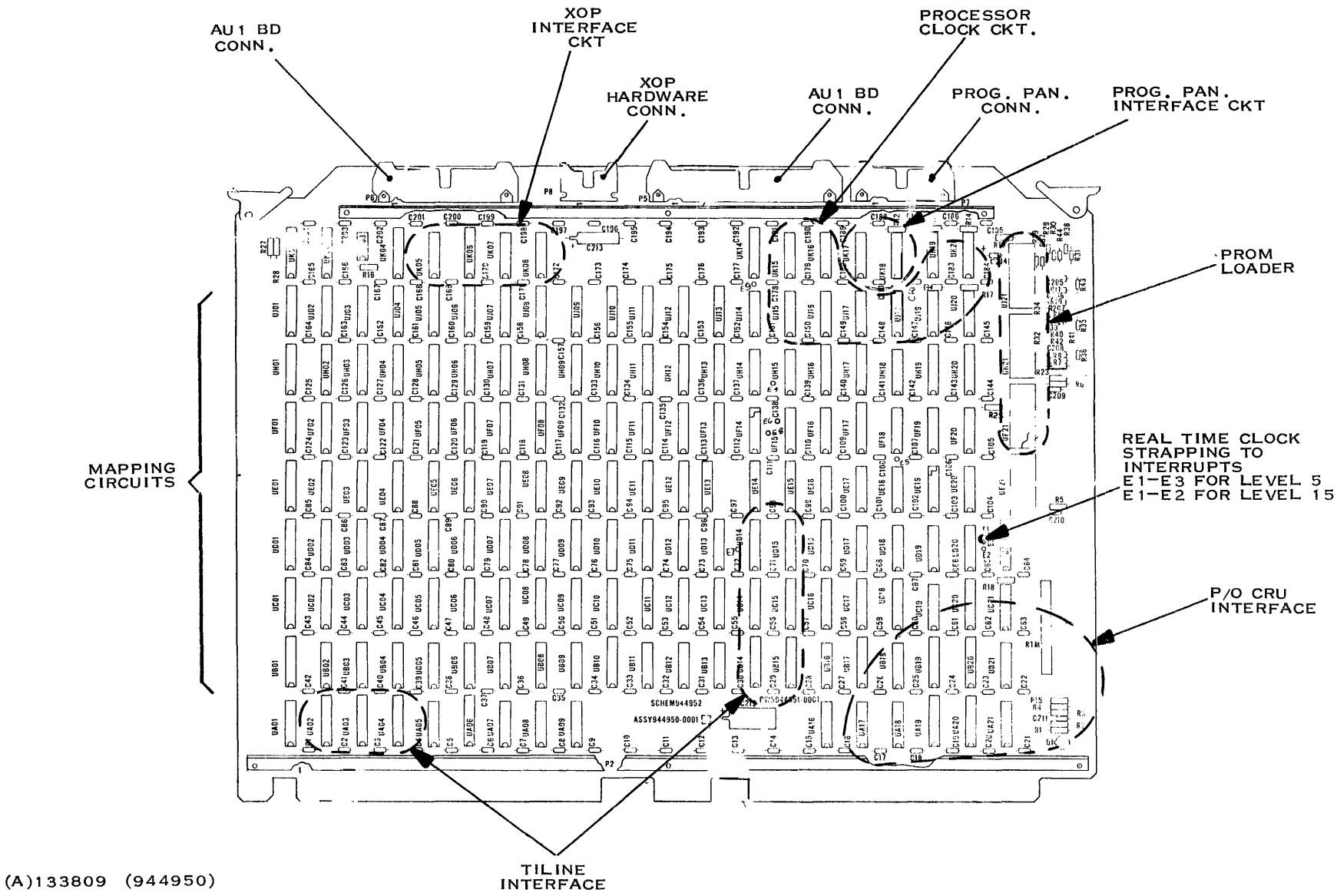


Figure 1-13. AU2B Board Component Location

1.2.1.2 **990/10 RAM Memory Boards.** Five types of RAM memory boards, all based on MOS dynamic RAM devices, are used in the 990/10 computer:

- Memory Expansion Board (without error-correction, parity checking optional).
- **ECC 16KB Expansion Board.**
- Add-On (Array) ECC Memory Board (requires ECC 16KB Expansion Board for control).
- **Memory Controller, 96KB, with ECC, 990/16KR, standard and fine line versions.**
- Memory Add-On Module, 256KB, with ECC, 990/16KR (requires 96KB Memory Board for control).

All RAM memory boards operate as TILINE slave devices. Each type of RAM memory board is described in the following.

Memory Expansion Board. As shown in figure 1-14, the RAM memory on the memory expansion board is organized into banks of 8K bytes of 8 bits each. Each bank uses 16 packages of the TMS 4050NL MOS RAM. Each package implements one bit of the 8192 bytes in its bank. The part number for each amount of memory is as follows:

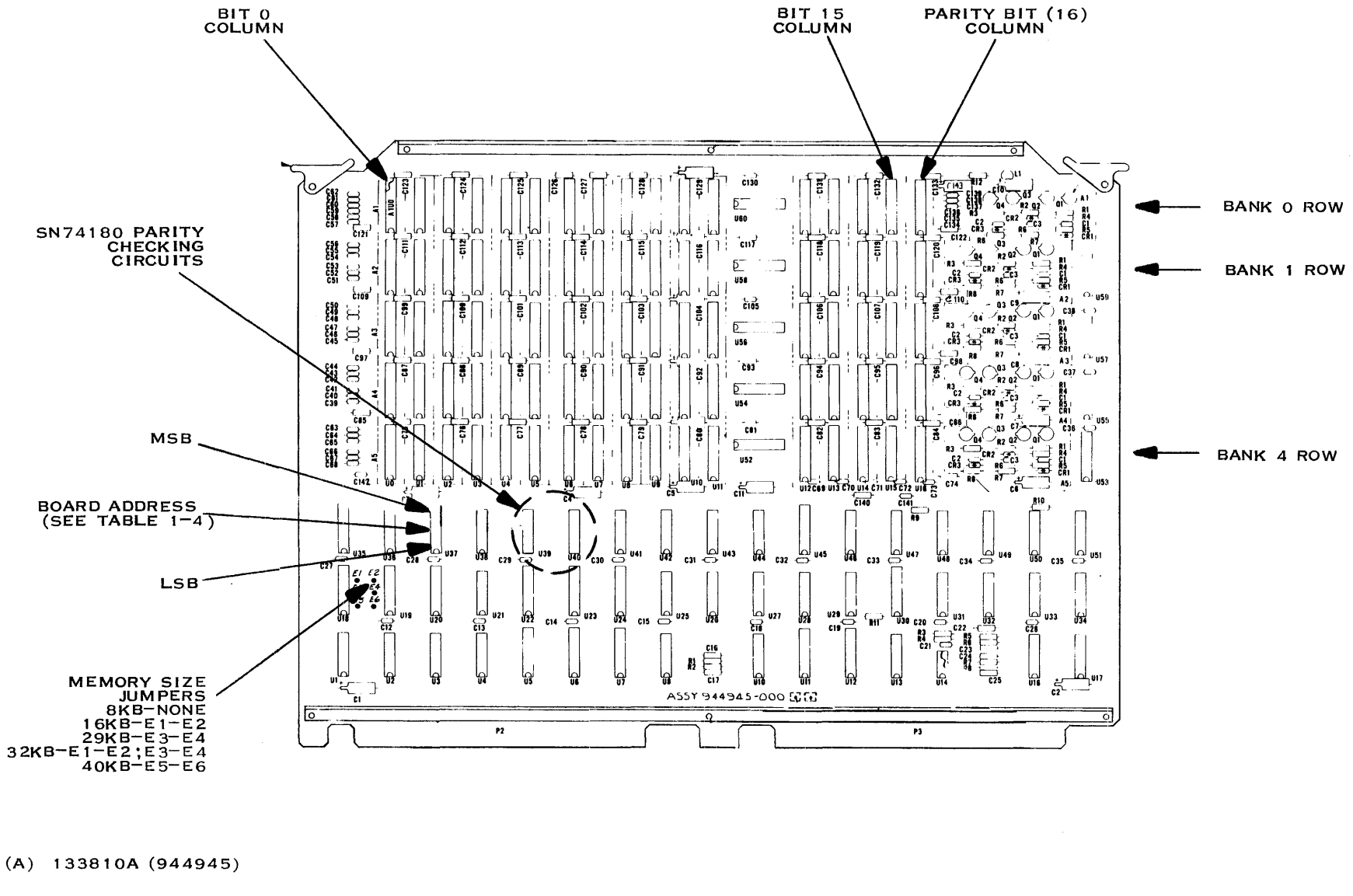
Part Number	Memory Capacity (Words)
944945-0001	8KB
944945-0002	16KB
944945-0003	24KB
944945-0004	32KB
944945-0005	40KB

The strapping schedule for each of the board capacities listed above is indicated in figure 1-14. The required settings for the board (starting) address switches are shown in table 1-4.

Parity error-checking is an optional feature of the memory expansion board. Parity checking is implemented by installing an MOS RAM package in the 16th column (17th bit position) for each bank of memory implemented (see figure 1-14). Two SN74180 type parity checkers (U39 and U40) must also be installed as shown in figure 1-14. An error in a word read from memory is indicated by a lamp (LED) on the board.

ECC Expansion Board. A 16K-byte module with ECC is used as a memory board for the 990/10 minicomputer. The ECC 16KB Expansion Board may actually implement only 8K bytes. The strapping for the two capacities is shown in figure 1-15. The 16K-byte memory board with ECC has a memory controller and may be augmented with an add-on memory board that may contain an additional 16K, 32K, or 48K bytes of ECC memory. The add-on memory board does not have a controller but operates under control of the 16KB memory board with ECC to give a total capacity of 64K bytes of ECC memory per pair of boards. The add-on memory module includes top edge connectors for the interface to the 16KB memory board with ECC. The interface signals are described in detail in Appendix I.

Error-checking and correction ensures accurate storage and retrieval of data. The memory controller generates a 6-bit code during a store operation that is checked during a read operation on the data. The code enables the controller to detect and correct single-bit errors, and to detect two or more errors in each 16-bit word stored in the memory. The 16K-bytes of on-board MOS memory is implemented in two rows of TMS 4060 devices across the top of the board (see figure 1-15). Each row of devices provides for the storage of the 22 bits required for data and error correction. The TMS 4060 device is similar to the TMS 4050 previously described. It has separate I/O terminals provided on a 22-pin dual-in-line package.



(A) 133810A (944945)

Figure 1-14. Memory Expansion Board Component Location

Table 1-4. Memory Expansion Board, Starting Address Switch Settings

Beginning Word* Address On Board ( )16	Address Switch Setting								Number Of Memory Words Below Board
	8	7	6	5	4	3	2	1	
00000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
01000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	4,096
02000	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	8,192
03000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	12,288
04000	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	16,384
05000	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	20,480
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0F000	OFF	OFF	OFF	OFF	ON	ON	ON	ON	61,440
10000	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	65,536
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
40000	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	262,144
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F4000	ON	ON	ON	ON	OFF	ON	OFF	OFF	999,424

* The amount of addressable memory for any particular board is dependent on the configuration of the board, i.e. each dash number has a different size of addressable memory.

As shown in figure 1-15, the Expansion Board includes two LED error indicators and two dual-in-line switch packages for controlling the operation of the board. Two light-emitting diodes, mounted next to the ejector tab on all ECC 16KB Expansion boards indicate errors that may occur during a memory cycle. The Correctable Error indicator lights when the error correcting logic detects and corrects an error in data read from memory. This indicator is not operational if the error correcting logic is disabled. The Noncorrectable Error indicator lights when the error detecting logic senses a data error that cannot be corrected (2 or more bits in error), or a data error that is not corrected because the error correcting logic has been disabled.

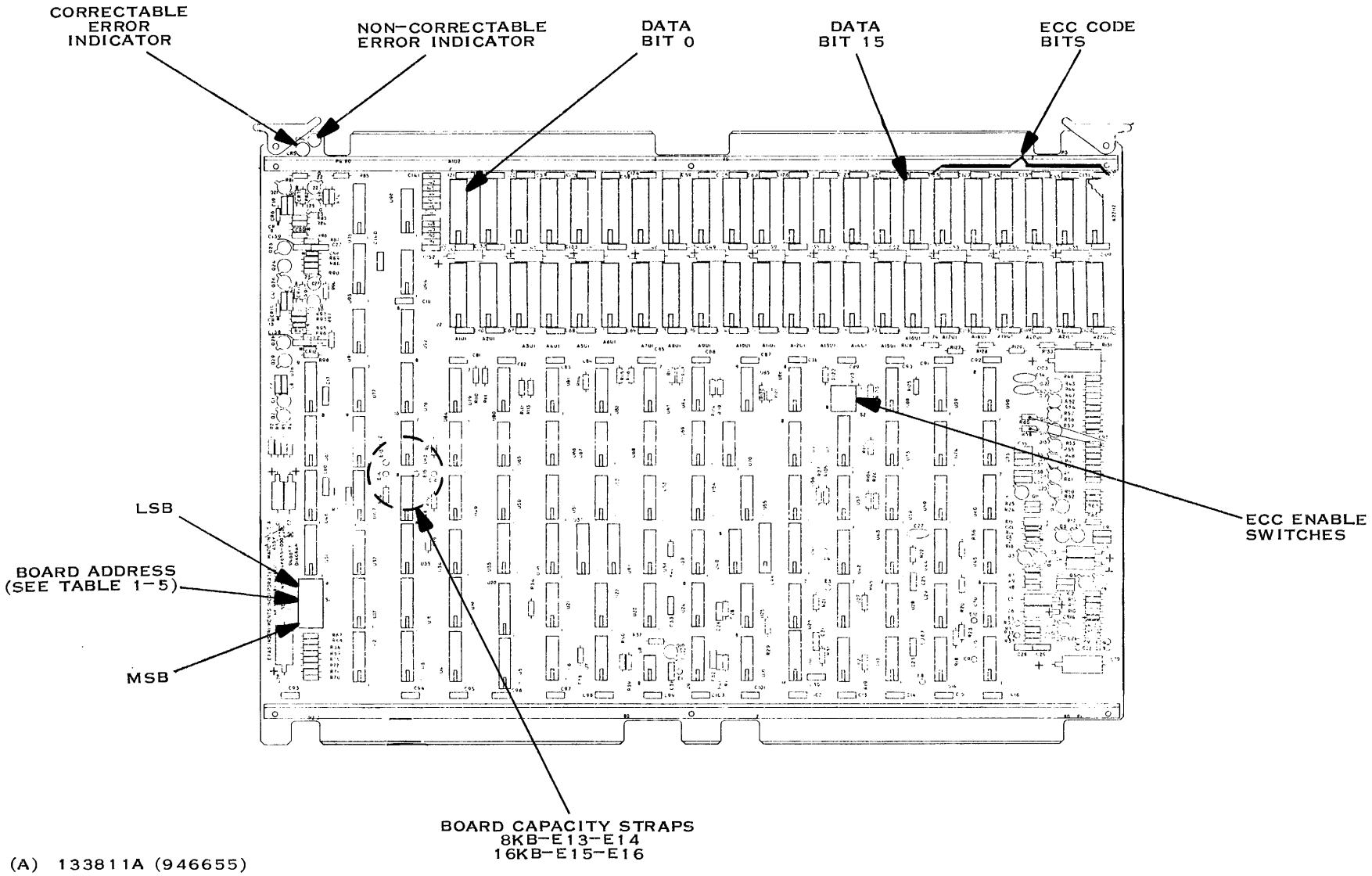


Figure 1-15. 16KB Expansion Board, Component Location

A dual-in-line package (DIP) containing four single-pole, single-throw switches allows the user to select or disable the error correcting logic. Switches 3 and 4 in this package perform no function. Switches 1 and 2 enable the error correcting logic when both switches are set to the ON position. These switches disable the error correcting logic when both switches are set to the OFF position. In no case should one switch be ON while the other switch is OFF, since this condition produces erroneous indications to the memory controller.

Figure 1-15 shows the location of the board (starting) address switches. The required settings for the address switches are shown in table 1-5.

Table 1-5. ECC 16KB Expansion Board and 96KB Memory Controller Board, Starting Address Switch Settings

Beginning Word* Address On Board ( )16	Address Switch Setting								Number Of Memory Words Below Board
	1	2	3	4	5	6	7	8	
00000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
01000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	4,096
02000	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	8,192
03000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	12,288
04000	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	16,384
05000	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	20,480
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0F000	OFF	OFF	OFF	OFF	ON	ON	ON	ON	61,440
10000	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	65,536
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
40000	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	262,144
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F4000	ON	ON	ON	ON	OFF	ON	OFF	OFF	999,424

* The amount of addressable memory for any particular board is dependent on the configuration of the board, i.e. each dash number has a different size of addressable memory.

16KB Expansion Board Memory Size Jumpers. A group of 9 terminals (E1 through E9) are used to encode the amount of memory implemented on the board (1K to 8K). These jumpers are set up as follows:

Memory Size	Jumper Connections
2KB	E1-E2, E4-E5, E7-E8
4KB	E1-E2, E4-E5, E8-E9
6KB	E1-E2, E5-E6, E7-E8
8KB	E1-E2, E5-E6, E8-E9
10KB	E2-E3, E4-E5, E7-E8
12KB	E2-E3, E4-E5, E8-E9
14KB	E2-E3, E5-E6, E7-E8
16KB	E2-E3, E5-E6, E8-E9

Add-On Memory Module W/ECC. The Add-On board provides Error-Checking and Correcting (ECC) memory on a board that is a companion to the 16KB Expansion board since the controller of the latter is required. Up to 48K bytes of ECC memory are provided in 16KB increments as indicated by the following part numbers:

Part Number	Board Capacity in Words
945093-0002	16KB
945093-0004	32KB
945093-0006	48KB

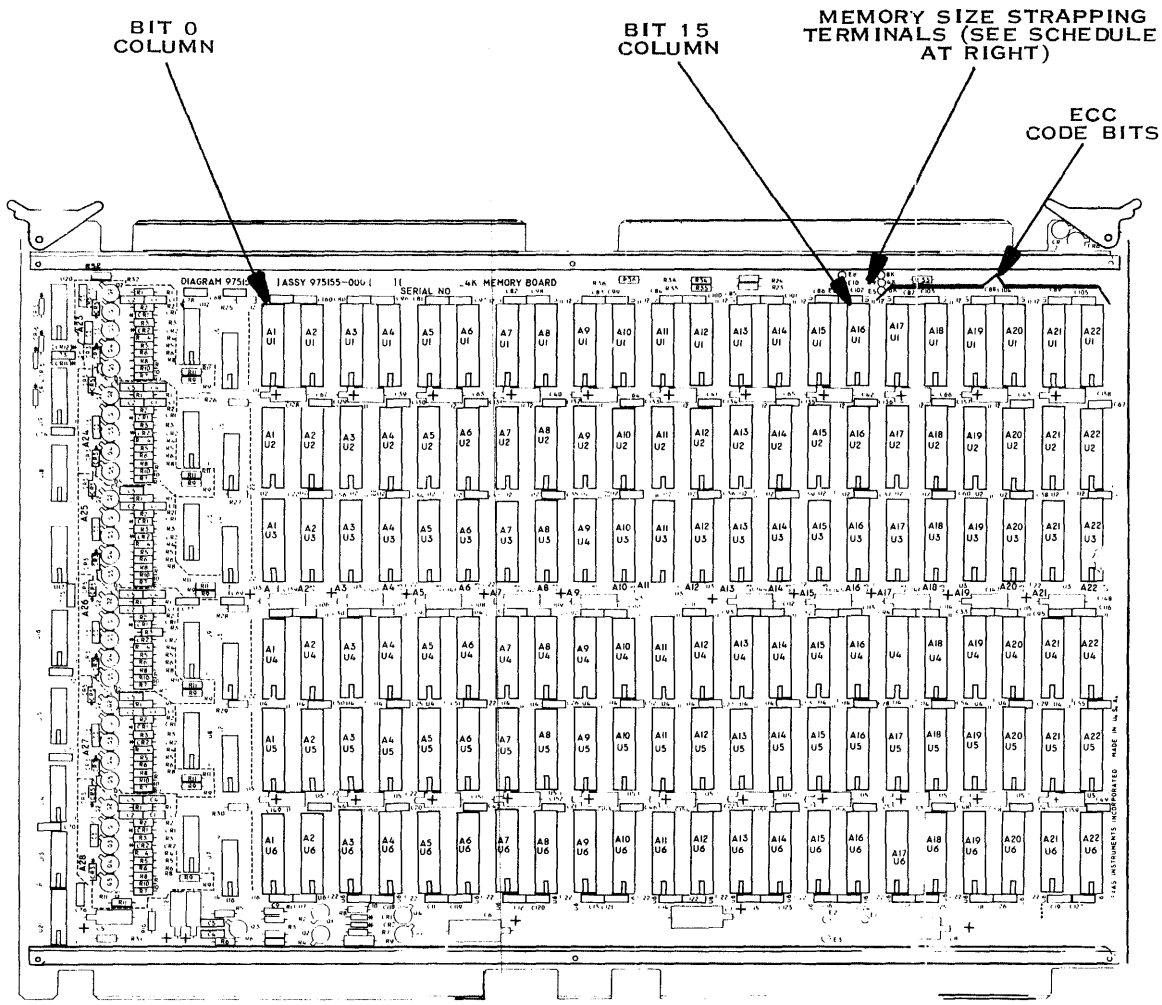
The location of the components are indicated in figure 1-16 which also shows the strapping required to indicate the size of the memory implemented.

Memory Controller, 96KB, with Error Checking and Correcting (ECC), 990/16KR. This memory module, the 96KB memory controller in standard or fine line version, is one of the memory board configurations available for use in the 990/10 minicomputer. The actual memory size of the board may be varied from 0 to 96KB by strapping jumpers J9 and J10. The 96KB memory controller also contains the memory control logic for up to 96K bytes of MOS RAM on the board and the control logic for up to 1 megabytes of additional memory on up to four associated add-on memory expansion boards. The 96KB memory controller board functions as a TILINE slave device and as such generates or accepts data only in response to a TILINE master device. The 96KB memory controller board interface to the TILINE is made through the two 80-pin connectors at the bottom edge of the board that installs in the computer or expansion chassis. Two 50-pin connectors at the top edge of the board are used to interface with expanded memory. The interface signals between the memory controller board and the 256KB add-on memory boards are described in detail in Appendix J. The memory control logic consists of TILINE interface logic, timing and memory refresh control circuits, and error-checking and correction circuits.

The memory array on the memory controller consists of from zero to three banks (rows) of memory chips with 22 memory chips in each bank. Each memory word consists of 16 data bits and six check bits. During normal operation, only the data bits are processed on the TILINE data bus.

The 96KB memory controller board may be placed in a diagnostic mode by addressing the memory controller logic at a specified TILINE Peripheral Control Space (TPCS) address. This address is normally set to $F800_{16}$ (TILINE address $FFE80_{16}$). At this time, the check bits are processed over the data bus in place of the most significant six bits of the data word. Cycle control and refresh control for the add-on memory boards are provided by the 96KB memory controller board, but the add-on memory expansion boards interface directly with the TILINE for address selection. The 96KB memory controller circuitry, including the error-checking and correcting circuits, is implemented in TTL devices on the lower part of the board as shown in figure 1-16A. The 96K bytes of on-board MOS memory consists of three rows of TMS 4116 devices across the top of the board. Each row includes the 22 devices required for the storage of the 22 bits of data and error correction. The TMS 4116 chip is based on N-channel silicon-gate technology and the inputs and outputs are TTL compatible.

In addition to TTL control logic, the 96KB memory controller board includes two light emitting diode (LED) error indicators, eleven LED chip failure indicators, and two dual-in-line switch packages (figures 1-16A and 1-16B). One of these switch packages is used to set the starting address of the on-board memory. The other switch package is used to select a TPCS. The two error-indicating LEDs indicate that a one-bit (correctable) error or a multibit (uncorrectable) error has occurred on this board. The correctable error LED illuminates when the error-correcting logic detects and corrects an error in data read from memory. The memory error LED lights when the error-detecting logic senses a data error that cannot be corrected (two or more bits in error).



MEMORY SIZE	STRAPPING
8K	E7-E8
16K	E5-E6
24K	E5-E6, E7-E8

(A)133812 (975155)

Figure 1-16. Add-On (Array) ECC Memory Board, Component Location

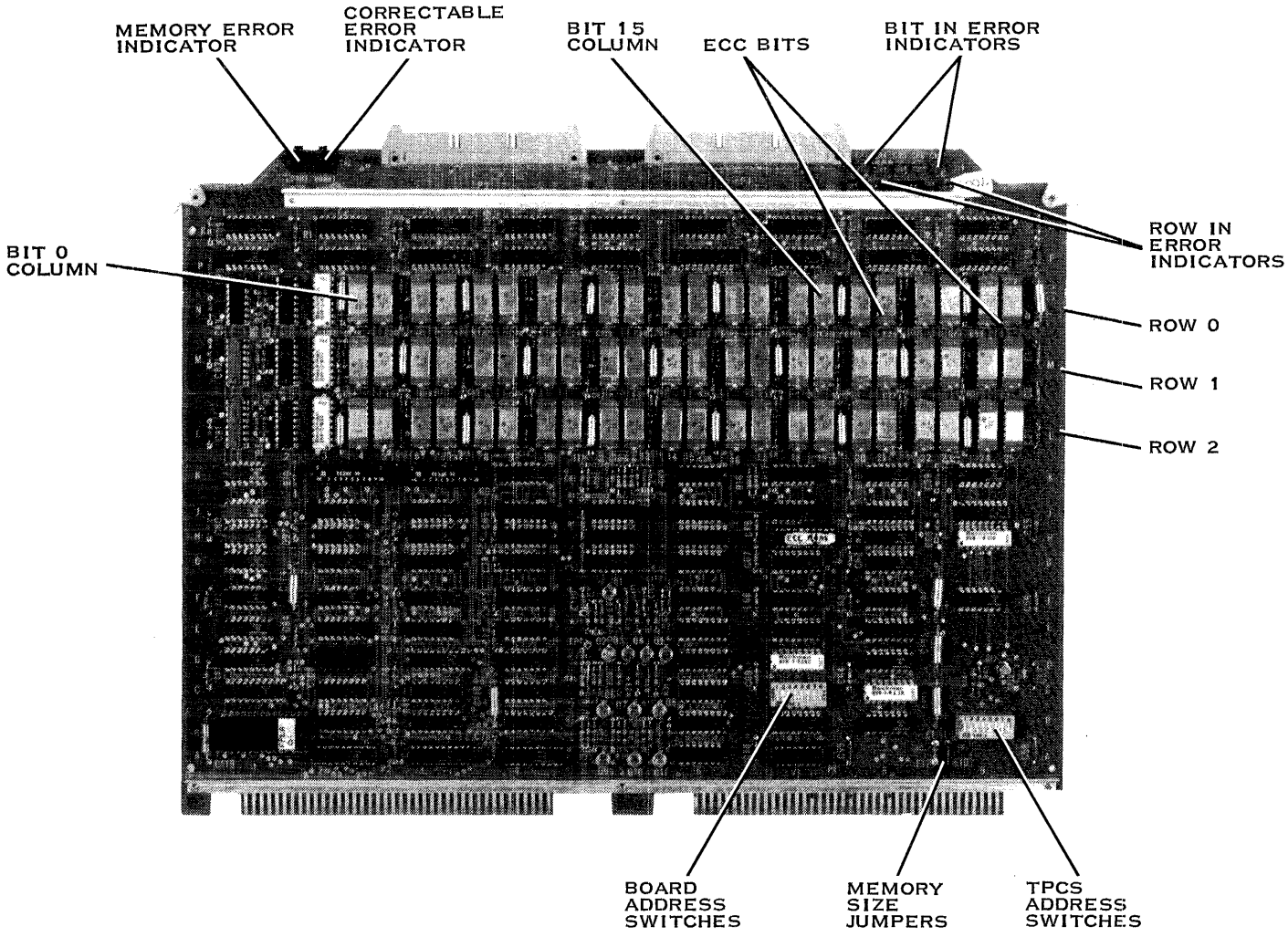


Figure 1-16A. 96KB Memory Controller Board Component Locations, Standard Version

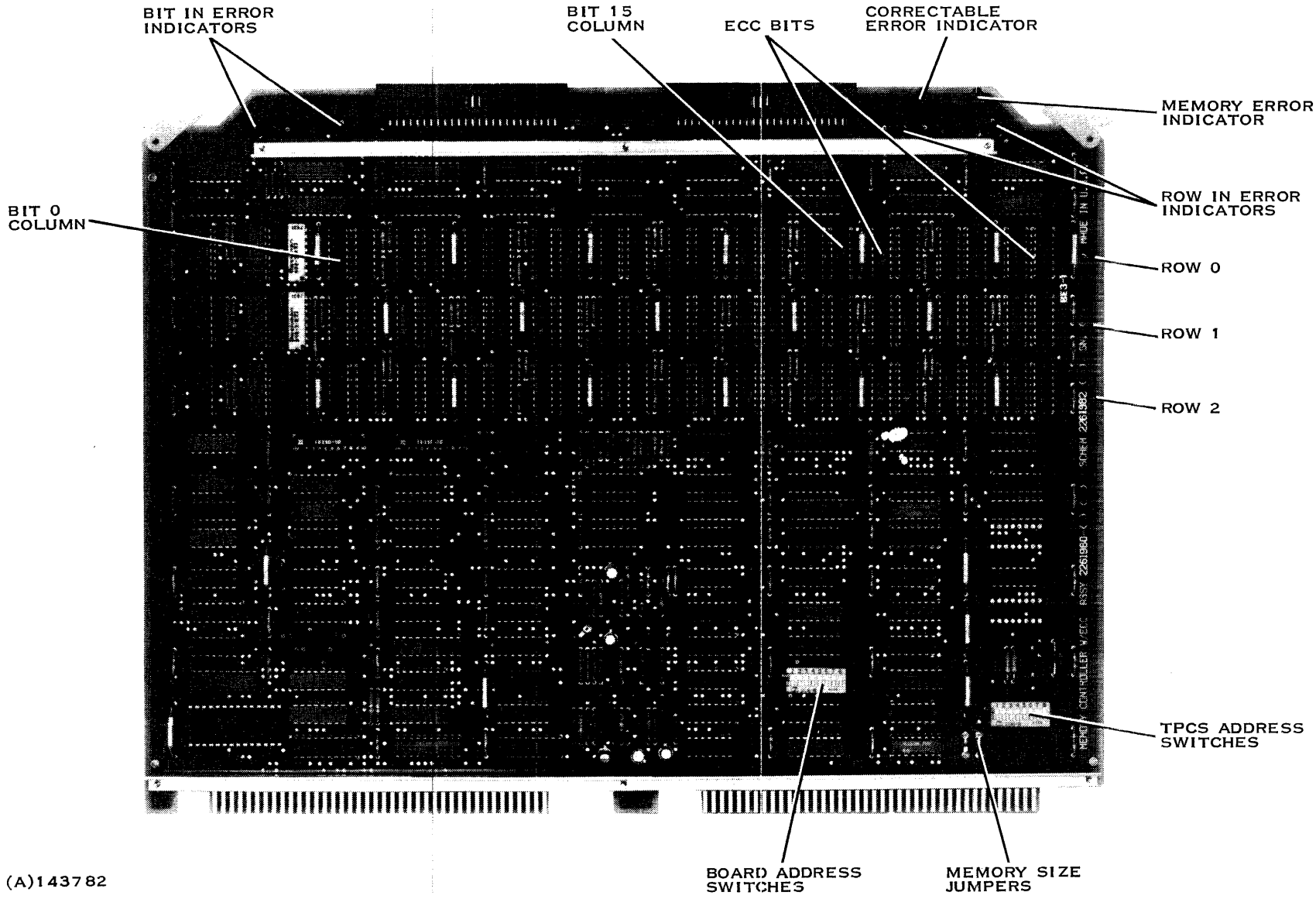
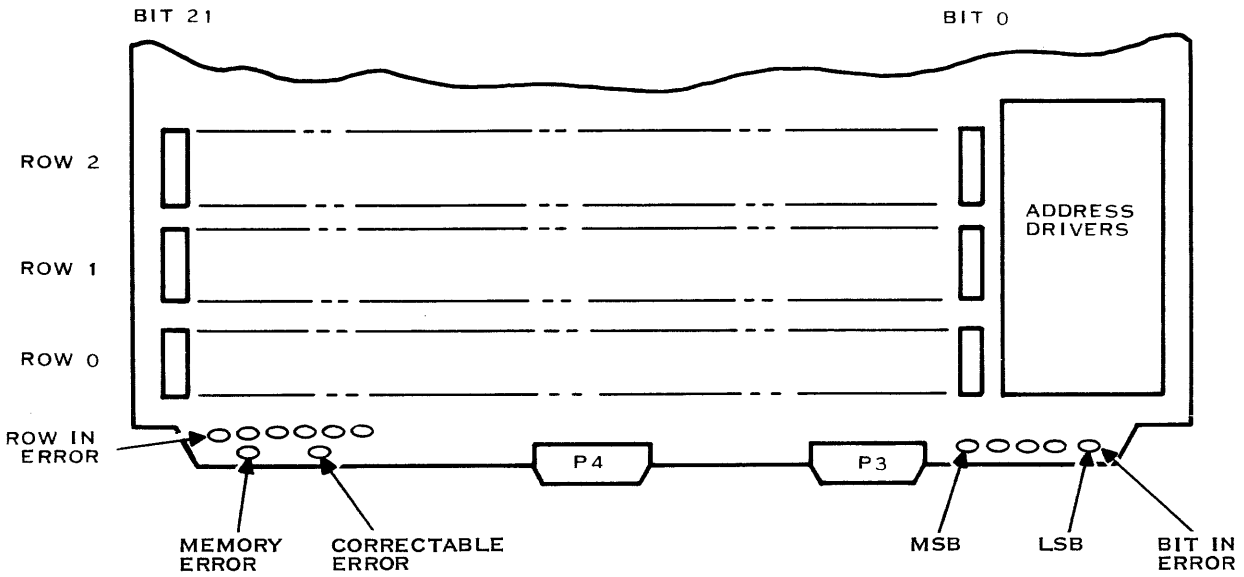


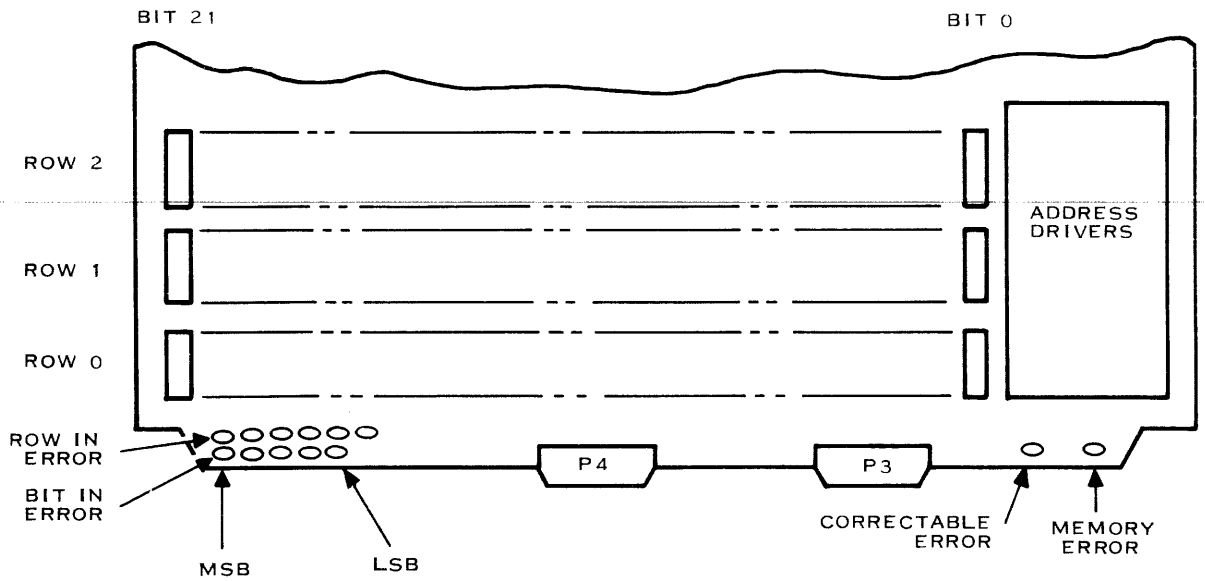
Figure 1-16B. 96KB Memory Controller Board Component Locations, Fine Line Version

These lamps are set on the first occurrence of the respective error stimulant and remain set until the board is powered down or until an I/O reset instruction is issued. The additional eleven chip failures LEDs pinpoint the memory chip that caused the first single-bit error. Additional errors do not affect these indicators but are recorded by the two error indicators located on each add-on memory expansion board. The eleven chip failure indicators are divided into two groups as shown in figure 1-16C. A group of five LEDs form a binary code that identifies the bit that failed. The remaining six LEDs form a binary code that identifies the row that contains the failing chip. Table 1-5A summarizes the error indicators and their functions.

The dual-in-line base address switch consists of eight single-pole, single-throw address switches. The address switches correspond to the eight most significant bits of the 20-bit TILINE address and permit board starting-address selection in 8K-byte increments. Switch 1 is the most significant bit of the address with switch 8 the least significant bit of the address. The required switch settings for the 96KB memory controller are the same as those for the 16KB expansion board and are shown in table 1-5. Addresses other than those shown can be represented in a similar manner using the eight switches to represent the binary number. Since each of the three rows of memory devices represents 32K bytes of memory, the memory capacity available is either 0, 32K, 64K, or 96K bytes. Memory size is set by connecting memory size jumpers as shown in table 1-5B.



FINE LINE VERSION



STANDARD VERSION

(A)143783

Figure 1-16C. 96KB Memory Controller Board Error Indicators

Table 1-5A. Description and Function of 96KB Memory Controller Board Error Indicators

Indicator	Description	Display Convention
Bit In Error	Hexadecimal Code 00 = Bit 0 . . 0F = Bit 15 . . 15 = Bit 21	LED On: Bit = 1
Row In Error	Hexadecimal Code 00 = Row 0 01 = Row 1 02 = Row 2 . . 22 = Row 34	LED On: Bit = 1
Memory Error	Multibit error on this board	LED On: Error
Correctable Error	Single bit error on this board	LED On: Error

Table 1-5B. 96KB Memory Controller Board Memory Size Jumper Schedule

Memory Size (Bytes)	Jumper J9	Jumper J10
0	OFF	OFF
32K	OFF	ON
64K	ON	OFF
96K	ON	ON

TPCS pencil switches correspond to address bits 11 through 18 of the 20-bit TILINE address bus and select the TPCS address that is used to operate the controller in the diagnostic mode. Switch 1 is the most significant bit and switch 8 is the least significant bit of the TPCS address segment. This permits 512 addresses to be selected that fall between hexadecimal F800 and FBFE inclusive in the 15-bit address form, and between hexadecimal FFC00 and FFDFF inclusive in the 20-bit form. Table 1-5C shows some typical TPCS addresses and their corresponding switch settings.

Table 1-5C. TPCS Addresses and Corresponding Pencil Switch Settings

CPU Address	TPCS Address	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
F800-02	FFC00-01	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
F804-06	FFC02-03	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F81C-1E	FFC0E-0F	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
F820-22	FFC10-11	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
F9FC-FE	FFCFE-FF	OFF	ON	ON	ON	ON	ON	ON	ON
FA00-02	FFD00-01	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
FBFC-FE	FFDFE-FF	ON	ON	ON	ON	ON	ON	ON	ON

Memory Add-On Module, 256KB, with Error Checking and Correcting (ECC), 990/16KR. This expansion memory, hereinafter referred to as the 256KB add-on array, contains the storage elements, address decoding logic, and the control and data buffers for up to 256K bytes of MOS RAM on the board. The 256KB add-on array is used in conjunction with the 96KB memory controller and provides high density main memory for the 990/10 central processors. Communication between these boards is done over the TILINE. Up to four of the 256KB add-on boards may be controlled by one 96KB memory controller. The 256KB add-on array board interface to the TILINE consists of the TILINE address lines and power lines and is made through two 80-pin connectors at the bottom edge of the board that installs into the computer or expansion chassis. Two 50-pin connectors at the top edge of the board provide the data path and control signals interface to the 96KB memory controller. Memory on the 256KB add-on array board consists of from one to four banks of memory chips. Each bank consists of two rows of 22 memory chips, one row for even and one row for odd word addresses. Double word read and single word write cycles are implemented for use with a cache type controller.

As shown in figure 1-16D, the 256KB add-on array address decoding logic and the control and data buffers is implemented in TTL devices located on one side of the board.

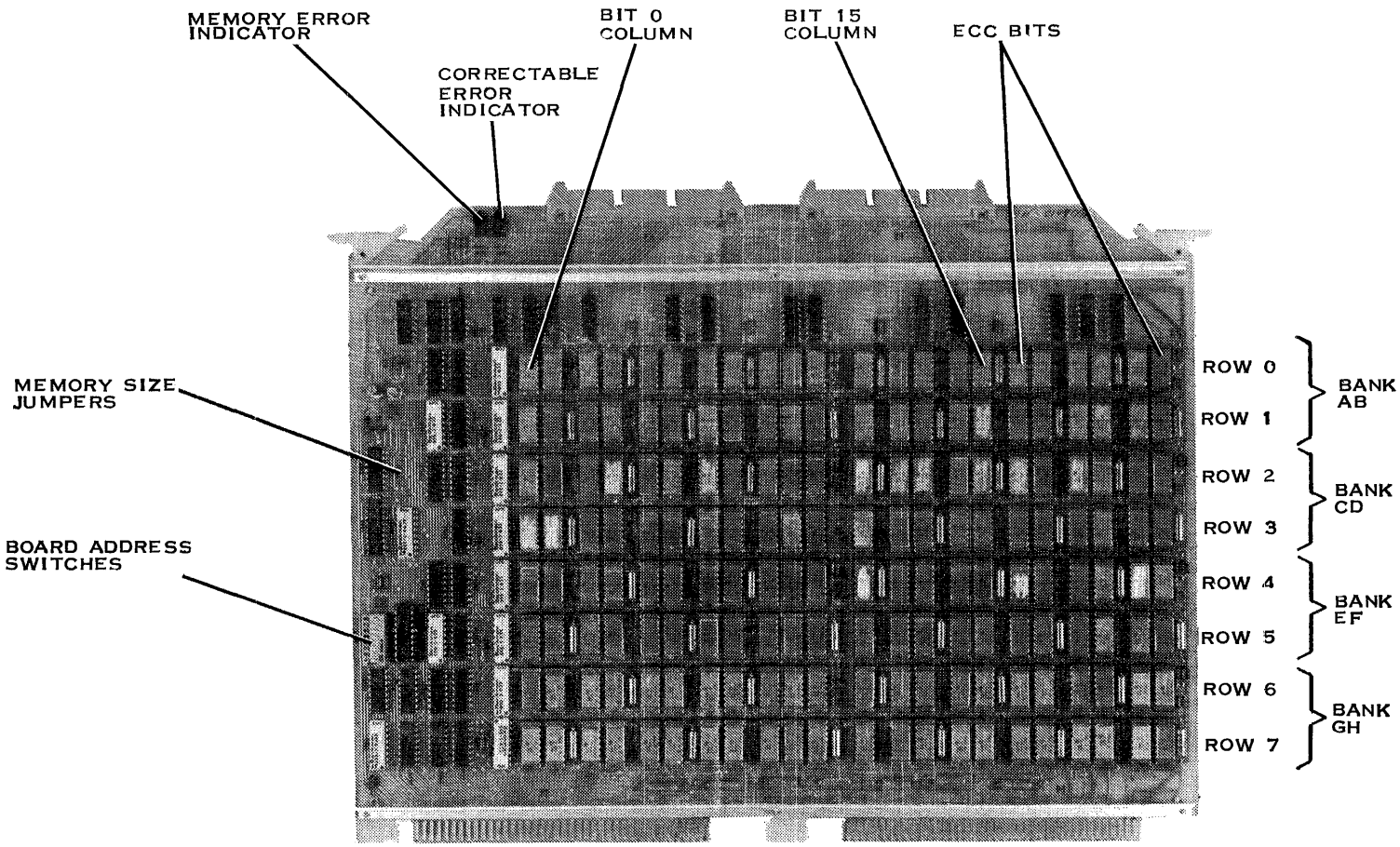


Figure 1-16D. 256KB Add-On Memory Array Board Component Location

The eight rows (or four banks) of the TMS 4116 MOS memory devices extend across the rest of the board with row and bank designations as shown in figure 1-16C. Also on the board are two LED error indicators and the dual in-line switch package used to set the starting address of the board. The two error indicating LEDs reveal that a one-bit (correctable) error or a multibit (uncorrectable) error has occurred on this board. These lamps are set on the first occurrence of the respective error stimulant and remain set until the system is powered down or until an I/O reset instruction is issued. The dual in-line switch consists of eight single-pole, single-throw switches. The address switches correspond to the eight most significant bits of the 20-bit TILINE address and permit board starting address selection in 8K-byte increments. Switch 1 is the most significant bit of the address and switch 8 is the least significant bit of the address. The required switch settings for the 256KB add-on board is the same as that for the 96KB memory controller as found in table 1-5. The memory capacity may be set in increments of from one to four banks of memory. Since each bank of memory represents 64K bytes of memory, the memory capacity available is either 64K, 128K, 192K, or 256K bytes. Memory size is set by connecting jumpers across the terminals of J9 and J10 as shown in table 1-5D.

Table 1-5D. Memory Size Jumpers for 256KB Add-On Memory Array Board

Memory Size	Jumper J9	Jumper J10
64KB	OFF	ON
128KB	ON	OFF
192KB	ON	ON
256KB	OFF	OFF

1.2.1.3 **EPROM Memory Module.** The EPROM memory module is an optional memory board with IC sockets and associated control circuitry to accommodate from 2KB to 16KB of erasable programmable read-only-memory (EPROM). This memory is implemented with 2708 1024 X 8-bit EPROM ICs. Two memory chips are required for each 2KB memory bank. As shown in figure 1-17, a maximum of 8 memory banks may be installed on the board with the leftmost column identified as bank 0 and the rightmost vertical column of two chips being bank 7.

The board jumper options are briefly described in the following subparagraphs.

Computer Type ID Jumper. The 990 EPROM memory module may be used in either a 990/4 or 990/10 computer. For use in a 990/10 chassis, the plug jumper must be installed between terminals E11 and E10 (E12 to E11 designates 990/4 chassis).

Starting Memory Address Bias. The starting address of the EPROM memory module may be placed at any 1K boundary in the 990/10s 1024K address space between 0 and 1023K as controlled by the setting of the five switch positions on DIP switches S1 and S2. Switch bit 1 of S1 is the MSB and switch bit 5 of S2 is the LSB. To select a starting address, the switches are set up in straight binary fashion with a switch in the "on" position designating a logic 1 and a switch in the "off" position designating a logic 0. For example, a starting address at 0 would be set up with all five switches in the off position; a starting address at 1K would have only switch 5 of S2 set to the on position and all others set to the off position; and a starting address of 31K would have all five switch bits of S2 set to the on position.

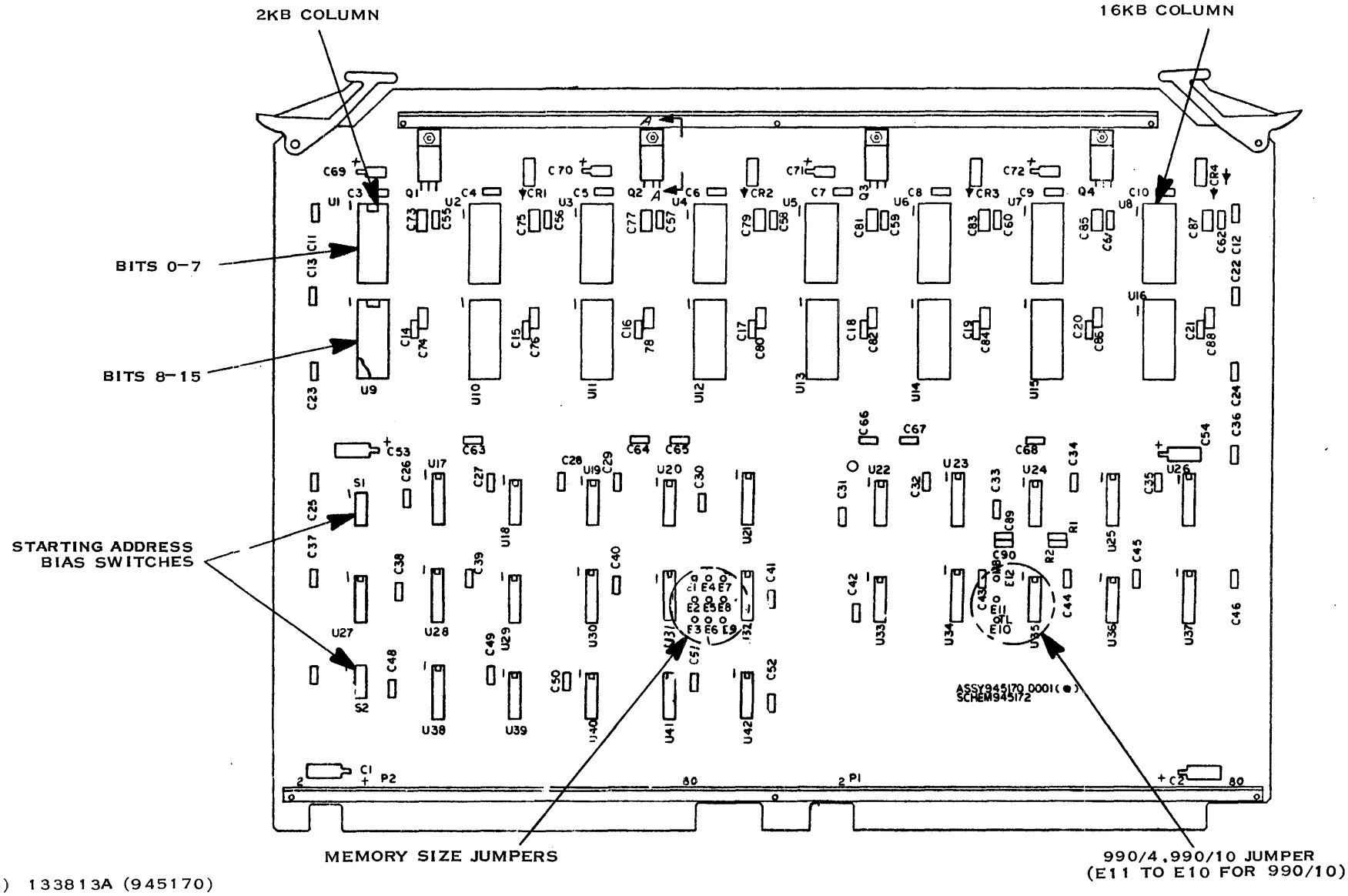


Figure 1-17. EPROM Memory Module Board Layout

1.2.1.4 **990/10 Chassis.** The 990/10 minicomputer may be housed in one of two chassis types including:

- 6-Slot chassis – Contains built-in 20 amp power supply and optional standby supply for semiconductor memory protection during power failure conditions, also contains either programmer or operator panel for system control.
- 13-Slot chassis – Contains 20 or 40 amp main power supply, optional standby power supply and either a programmer or operator panel. This chassis is basically the same as the 6-slot chassis except that it contains provisions for seven additional full-size logic boards.

6- and 13-Slot Chassis Interconnections. All internal connections (with exception of the ac distribution circuits) are accomplished through the backpanel connectors and the backpanel etch wiring.

CPU connections to peripherals and data terminals in the system are accomplished by interface cables that connect to the top edges of the interface boards (see figure 1-18). CPU boards AU2 and AU1 are installed in chassis slots 1 and 2, respectively. The first memory board is installed in slot 3. The 733 ASR interface and various other peripheral interface boards must be installed in accordance with the chassis map shown in figure 1-19. This standard configuration is required to assure software compatibility. However, some boards such as memory expansion, EPROM memory module and CRU expander may be installed in any slot (other than slots 1 and 2) since these devices respond to dedicated CRU addresses (see figure 1-26). Those logic board slots which are marked spare may be used to house any CRU interface board not otherwise identified on the chassis map.

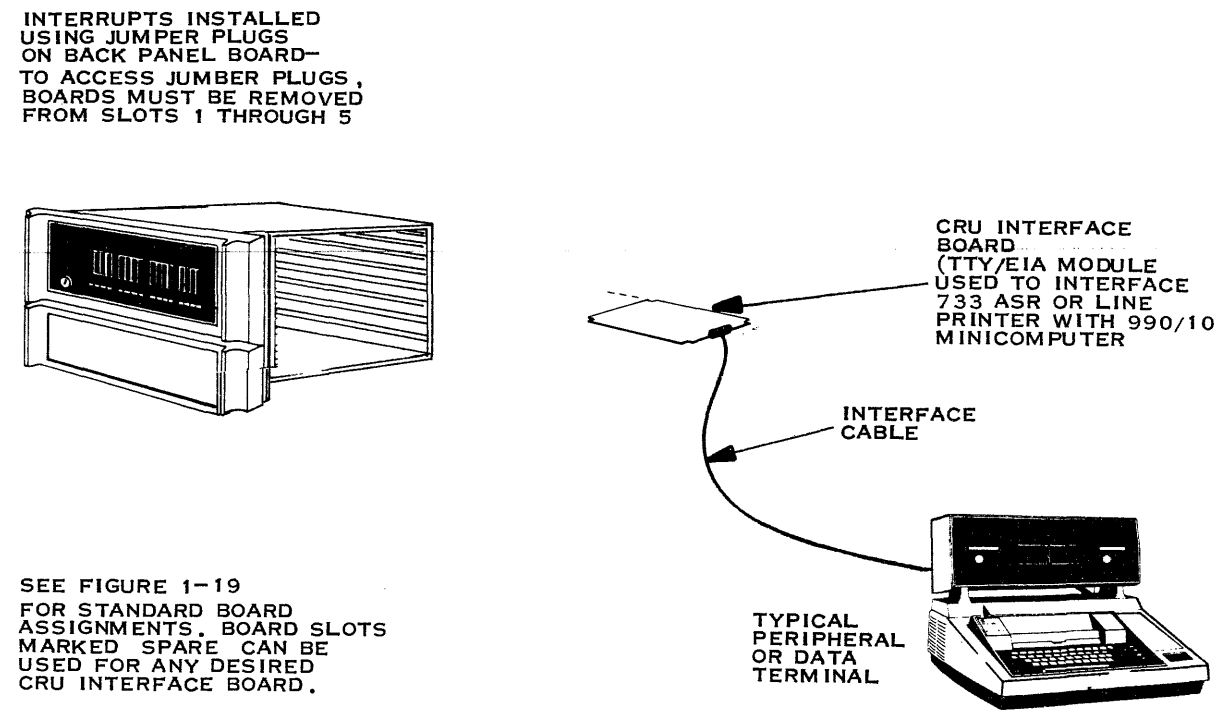


Figure 1-18. System Interconnections, Simplified Diagram

	P1 (FRONT OF CHASSIS)			P2 (REAR OF CHASSIS)		
	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/10 AU2	N/A	N/A	990/10 AU2	N/A
2	0120	990/10 AU1	N/A	0100	990/10 AU1	N/A
3	00E0	MEMORY	N/A	00C0	MEMORY	N/A
4	00A0	FLOPPY DISC CONTROLLER	7	0080	FLOPPY DISC CONTROLLER	7
5	0060	LINE PRINTER	14	0040	CARD READER	4
6	0020	PROM PROGRAMMER	15	0000	733 ASR/KSR	6

NOTE: UNUSED DEVICE INTERFACE LOCATIONS CAN BE USED FOR EXPANSION MEMORY OR OTHER DEVICE INTERFACES (WITH INTERRUPT MODIFICATION).

* INTERRUPT 3 WIRED HERE BUT NOT USED.

(A)133834 (A) 6-SLOT PREWIRED CHASSIS

	P1 (CHASSIS FRONT)			P2 (CHASSIS REAR)		
SLOT NUMBER	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/10 AU2	N/A	N/A	990/10 AU2	N/A
2	02E0	990/10 AU1	N/A	02C0	990/10 AU1	N/A
3	02A0	MEMORY	N/A	0280	MEMORY	N/A
4	0260	MEMORY	N/A	0240	MEMORY	N/A
5	0220	MEMORY	N/A	0200	MEMORY	N/A
6	01E0	MEMORY	N/A	01C0	MEMORY	N/A
7	01A0	DS31/32 DISC CONTROLLER	13	0180	DS31/32 DISC CONTROLLER	13
8	0160	CRT 3	9	0140	CRT 3	9
9	0120	CRT 2 OR CRU EXPANDER	10	0100	CRT 2 OR CRU EXPANDER	10
10	00E0	CRT 1	11	00C0	CRT 1	11
11	00A0	FLOPPY DISC CONTROLLER	7	0080	FLOPPY DISC CONTROLLER	7
12	0060	LINE PRINTER	14	0040	CARD READER	4
13	0020	PROM PROGRAMMER	15 (NOT USED)	0000	733 ASR/KSR	6

(A)133835 (B) 13-SLOT PREWIRED CHASSIS

Figure 1-19. Factory Prewired Chassis Configuration

Interrupt Wiring. Interrupt wiring for the three chassis configurations is accomplished using jumper plugs in jacks 1A1J3 and 1A1J2 on the backpanel board. These jacks may be accessed by removing the logic boards from the first 5 slots.

The interrupt jumper plugs are molded plastic connectors with two rows of square holes for inserting jumper wires. The jumper plug for the 6-slot chassis has 10 holes in each row; the jumper plug for the 13-slot chassis has 24 holes in each row; the jumper plug for the 3-slot chassis has 8 holes in each row. Each hole has a plastic detent that holds the jumper wire in place when it is completely inserted into the hole. Figure 1-20 illustrates the mating of the jumper wire with the plastic jumper plug. Notice that the brass connector on the jumper wire must be oriented properly when inserted into the jumper plug so that the plastic detent can engage the slot in the top of the jumper wire brass connector. The jumper wire can be removed from the jumper plug by lifting up on the plastic detent to free the jumper wire brass connector to slide out the rear of the jumper plug. The spring force of the detent is slight enough that only a fingernail is required to lift it up to release the jumper wire.

Figure 1-21 illustrates the position assignments on the interrupt plugs for both the 6- and the 13-slot chassis. Notice that each interrupt generated by a module has two positions on the plug assigned to it. This configuration allows interrupts that will be recognized on the same level to be daisy-chain linked to each other. A typical daisy-chaining example is provided in figure 1-22.

1.2.1.5 Programmer Panel. The programmer panel provides for manual control of a system and permits data to be entered into selected registers in the 990/10 CPU or memory and displayed from CPU registers and memory locations. A key switch on the programmer panel also controls the application of ac power to the chassis and prevents unauthorized program intervention.

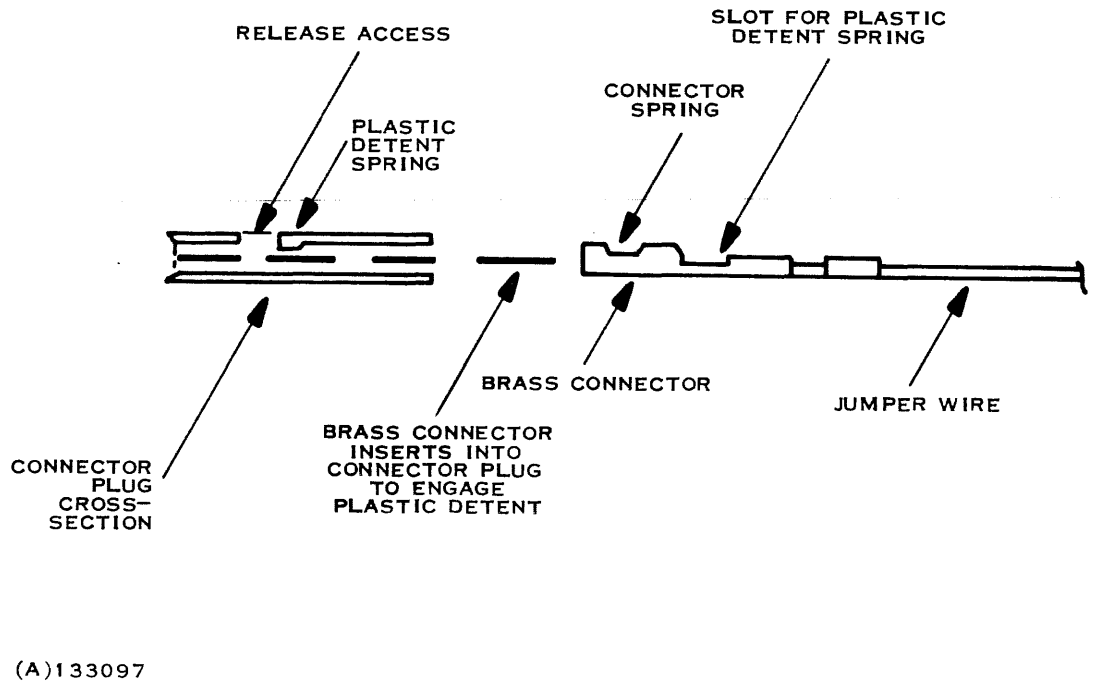


Figure 1-20. Interrupt Jumper Wire Installation

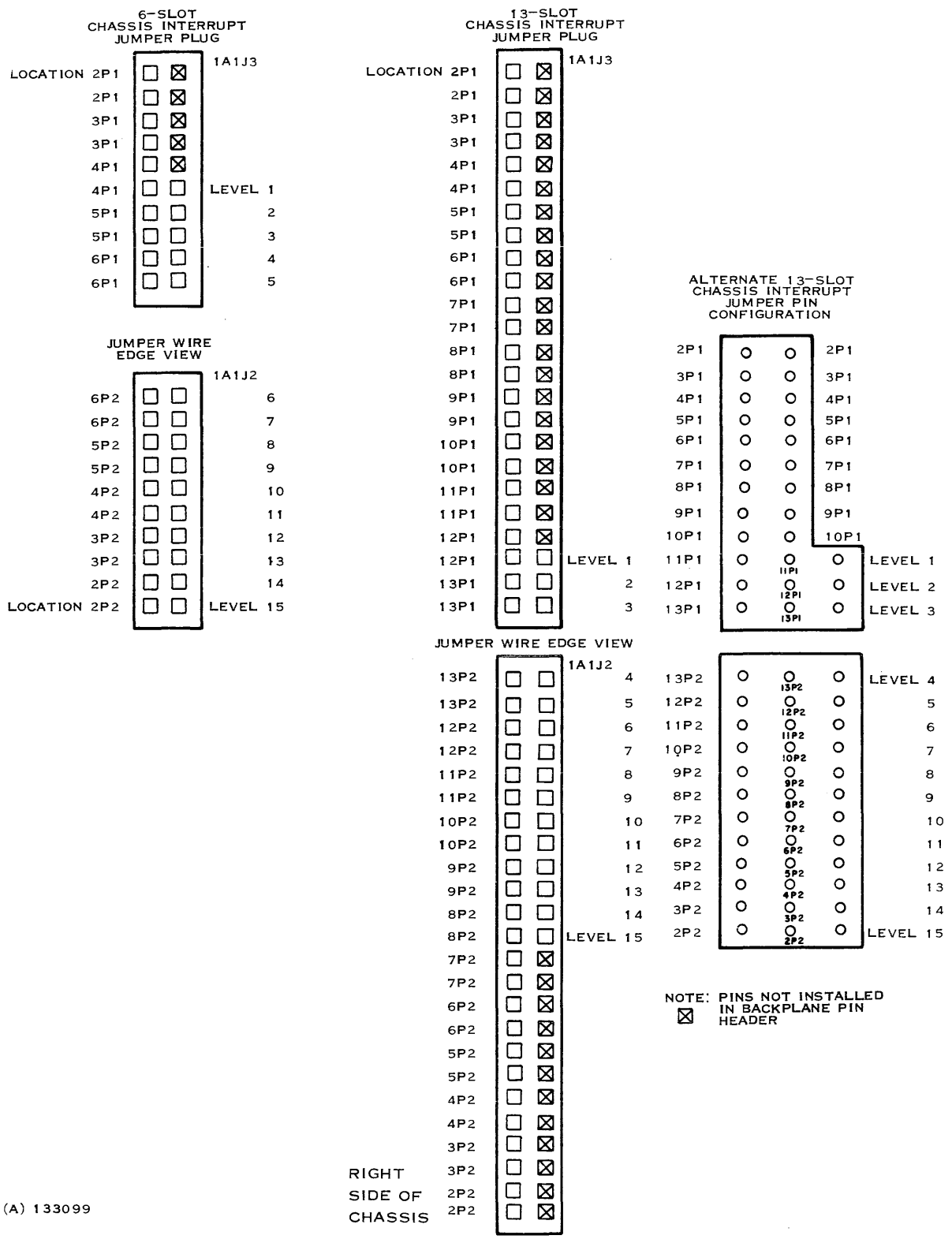


Figure 1-21. 6-Slot and 13-Slot Chassis Interrupt Jumper Plugs

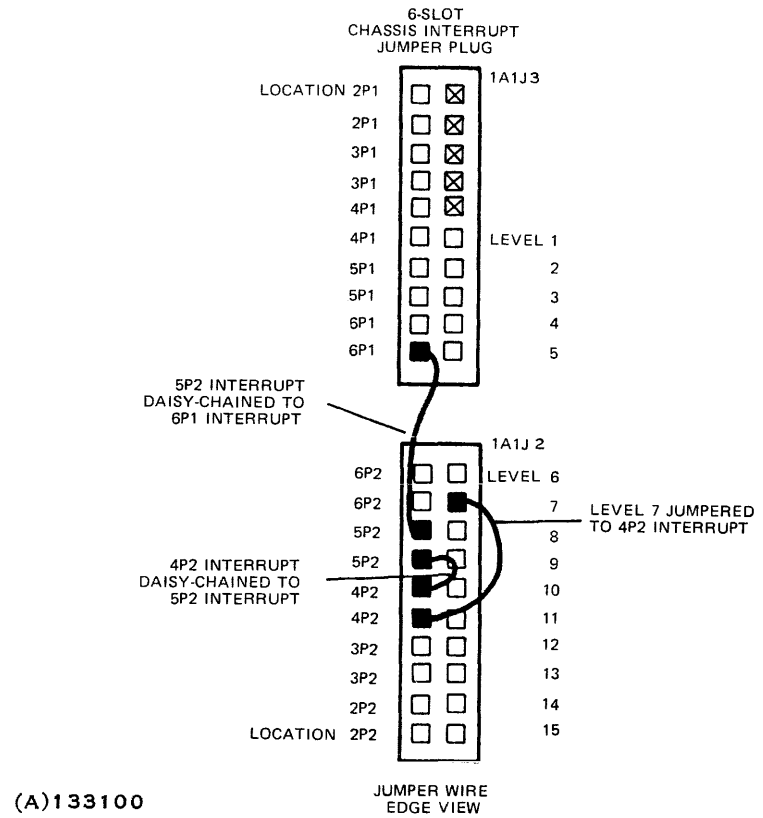


Figure 1-22. Jumper Plug Daisy-Chain Sample Connection

When power is first applied to the chassis, the system comes up in the RUN mode and all programmer panel switches (except the HALT/SIE switch if the key switch is in the UNLOCK position) are locked out. The DATA LEDs are all forced to a logic 1 (all lit). If the processor goes to the idle state, information may be displayed on the panel under software control.

To activate the panel, the key switch must be set to the UNLOCK position and the HALT/SIE switch must be pressed. When these two events occur, a LOAD signal is sent to the CPU that causes it to execute a trap to location $FFFC_{16}$ which contains the workspace pointer value of 80_{16} for the front panel software. The last word in memory (FFFE) contains the program counter value which defines the starting memory address for the panel software. The processor then begins processing the panel utility and constantly monitors the switch outputs via CRU STORE instructions. If any DATA or control switch is pressed, the software activates a debounce timer and then determines when timeout has occurred (approximately 10 milliseconds) by a CRU STORE instruction. The software then reads the switch output and takes the appropriate action. In the case of a DATA switch being pressed, the panel software changes the state of the associated DATA LED (if previously unlit, the LED lights). In case of a control switch entry, the software executes the command.

NOTE

See Section II for a detailed description of the programmer panel controls and indicators.

1.2.1.6 990 Power Supply. Both the 6-slot and 13-slot 990 chassis are equipped with built-in power supplies and cooling fans. The 6-slot chassis contains a 20 amp main power supply and an optional standby power supply which protects the semiconductor memories against accidental loss of data due to temporary power failures.

The 13-slot chassis contains a 20 or 40 amp power supply and optional standby power supply.

Main Power Supply. The main power supply (both 20 and 40 amp versions) consists of the following:

- Ac distribution circuits
- Ac power converter board
- Main power supply board

A schematic diagram of the 990 power supply system is shown in figure 1-23 and the associated parts location diagram is shown in figure 1-24.

The ac distribution circuits route ac power through fuse 1F1 and the key switch on the front panel through a line filter 1FL1 and an optional line transformer (used only in 100, 200 and 230 Vac systems) to a distribution terminal strip 1TB1. Ac power from the terminal strip is routed to the blower fans and the ac power converter board. Protection against a high surge voltage (230 V) is provided by 1C2 which temporarily shorts out and blows the fuse if lightning strikes the power lines.

The ac power converter board performs two functions in the main supply:

- Develops an unregulated +160 Vdc used to drive the main power supply board (both 20 and 40 amp configurations) and the optional standby power supply board.
- Develops a 120 Hz pulse train which is further shaped on the main power supply board and routed to the AU2 board in the CPU to drive the real time clock interrupt circuit.

The main power supply board (1A3) converts the unregulated +160 Vdc from the ac power converter board into the following regulated dc output voltages: +5 Vdc, +12 Vdc and -12 Vdc. If a standby supply is used, the regulated +5, and ±12 Vdc outputs from the standby power supply board are routed through P3 on the main power supply board to P1 which connects to the backpanel board. If the standby supply option is not used, a jumper plug is installed on 1A3J3 which routes the main dc voltages developed on the main power supply board onto the memory dc lines 1A3P1.

The main power supply board also generates a power on reset signal (TLPRES–) when ac power is initially applied to the chassis and generates a power failure warning (TLPFWP–) approximately 8 milliseconds before a power failure occurs. The power failure warning is normally tied into interrupt level 1 on the AU2 board.

The main power supply also provides a pulse shaping and driver function for the 120 Hz real time clock which originates on the ac power converter board. This signal is used to drive the real time clock interrupt logic on the 990/10 AU2 board.

Standby Power Supply. The standby power supply is an optional power system used to provide the regulated dc voltages used by the semiconductor memories in the 990/10 system. The supply consists of a pair of storage batteries, a battery switch, and protective fuse in the rear of the chassis and a standby power supply board which mounts piggy-back on a set of standoffs on top of the main power supply board.

During normal operation, the standby power supply board converts the +160 Vdc (unregulated) output from the ac power converter board into a regulated +5 Vdc and ±12 Vdc. The board also supplies charging current to the two standby batteries. When the batteries discharge to a minimum functional voltage level (after approximately 30 minutes of continuous standby operation), the standby power supply shuts down to protect the batteries. When normal ac power is restored, the standby power supply board develops an equalizing voltage until the charge current drops to a trickle charge level. The supply then switches to a float voltage to maintain the batteries at full charge. The standby power supply also contains provisions for preventing a switch to battery operation (even if the battery switch is in the ON position) unless ac power has first been applied to the system. The standby supply is also equipped with over-voltage sensing circuits which disable the standby supply and blows the battery fuse if any of the memory voltages exceed safe levels.

1.2.1.7 **CRU Interface Boards.** All low-speed interfaces between the CPU and external peripherals and data terminals are provided by CRU interface boards that plug into slots in the main chassis and expansion chassis. These interfaces may be implemented as either half- or full-size boards. Basically, the interface boards provide the address decoding, data buffering and data packing and unpacking required to match the serial CRU interface presented by the CPU with bit, byte or word-oriented peripherals and terminals. Each CRU interface board decodes the address on the CRU address lines when it receives a low-active Module Select signal from the board installed in slot 1 of the chassis (AU2 board in main chassis or CRU buffer board in expansion chassis). If a store clock is present when a valid CRU address is present on the CRU address lines and MODSEL is present, the interface board accepts serial data from the CRUBITOUT line from the CPU. If the clock is not present, a CRU read operation is being performed and serial data from the CRU interface board is sent to the CPU via the CRUBITIN line. All bit selection for CRU board-to-processor transfers is controlled by 990 software which addresses 1 of 16 bits via the 4 LSBs of the CRU address (bits 12-15). Some of the more commonly used CRU interface boards are briefly described in the following paragraphs.

TTY/EIA Terminal Interface Module. The TTY/EIA terminal interface module (Part Number 945075-1) provides an interface between the 990/10 and any terminal device using an EIA standard RS232 interface or 20 milliampere TTY current loop. Some of the 990 peripherals and data terminals that use the TTY/EIA terminal interface module include:

- 733 ASR data terminal
- 733 KSR data terminal
- 743 KSR data terminal
- Model 306 line printer
- Model 588 line printer

The jumper options used to modify the board operation for use with each device type are summarized in figure 1-25.

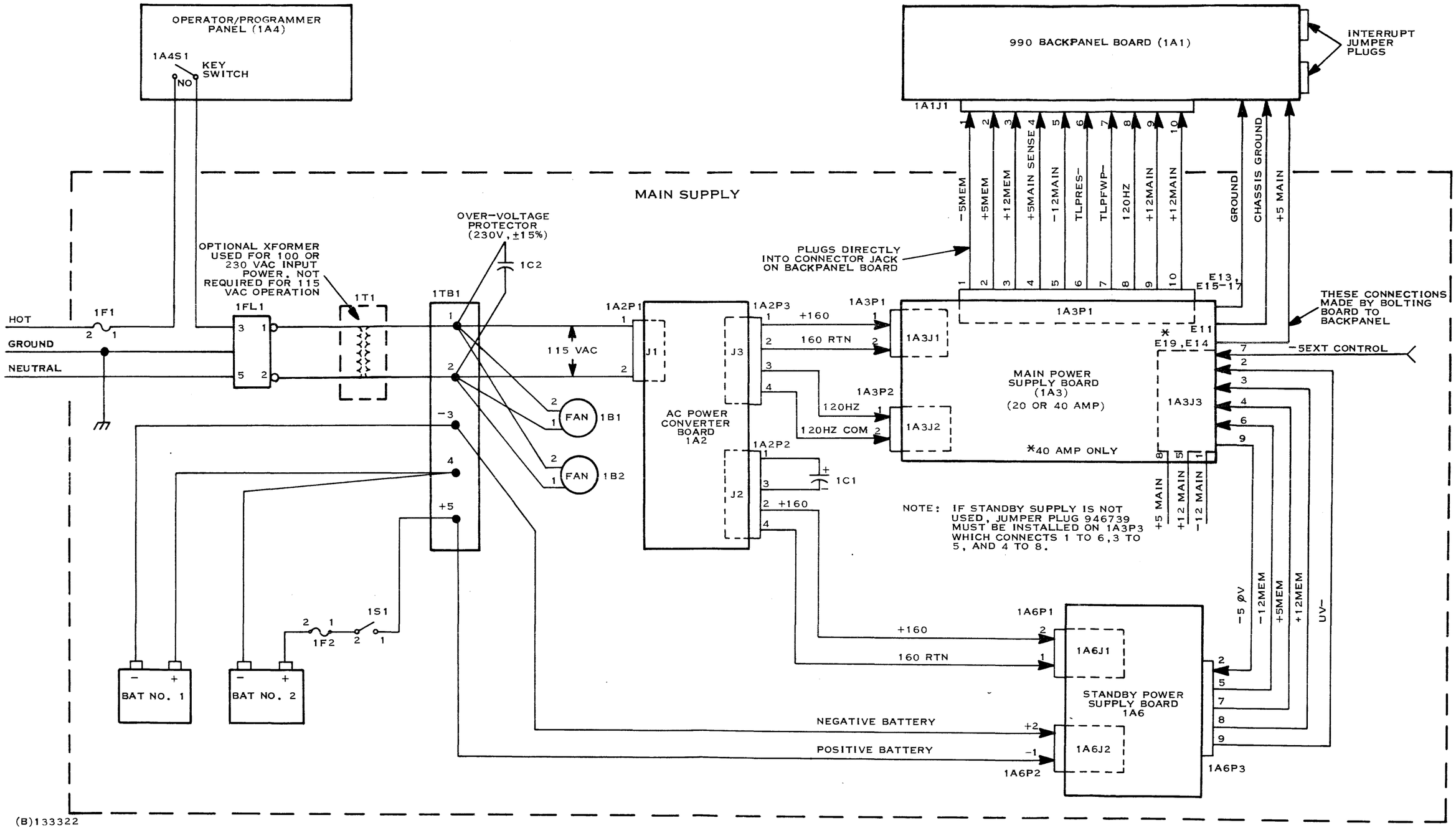
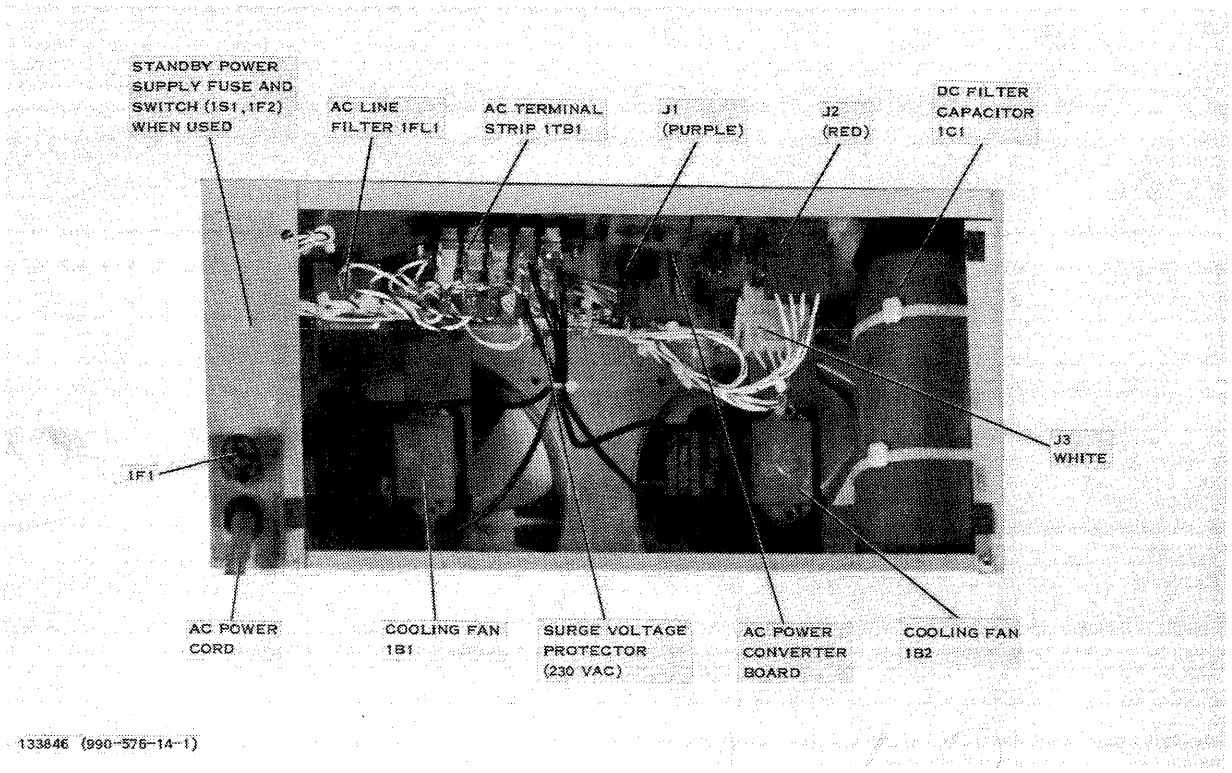


Figure 1-23. 990 Power Supply System



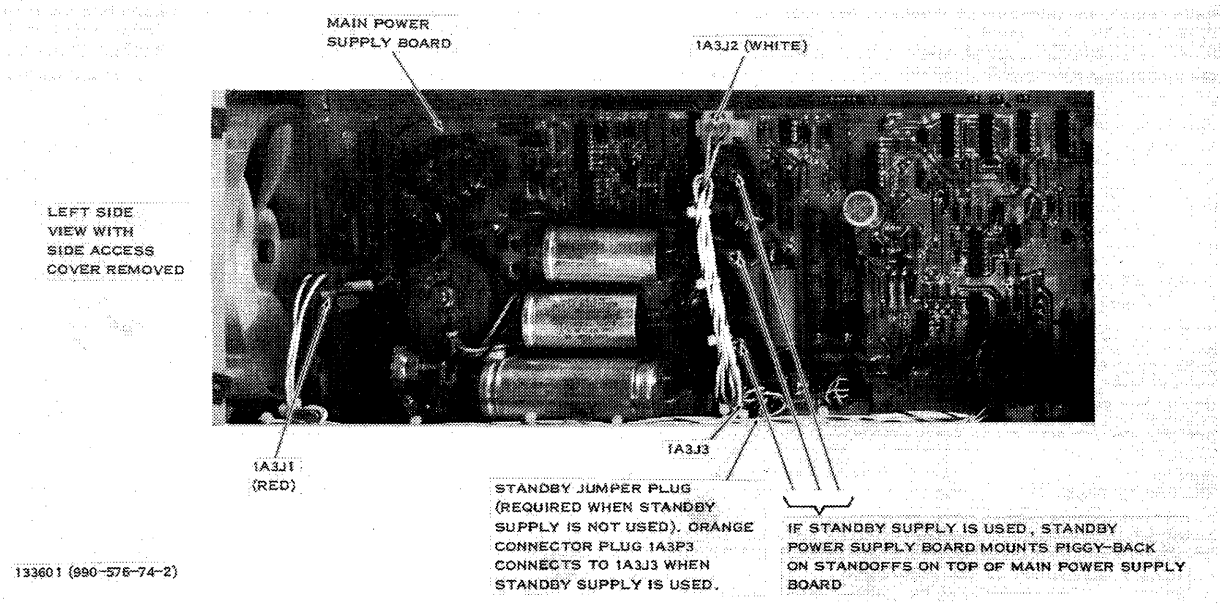
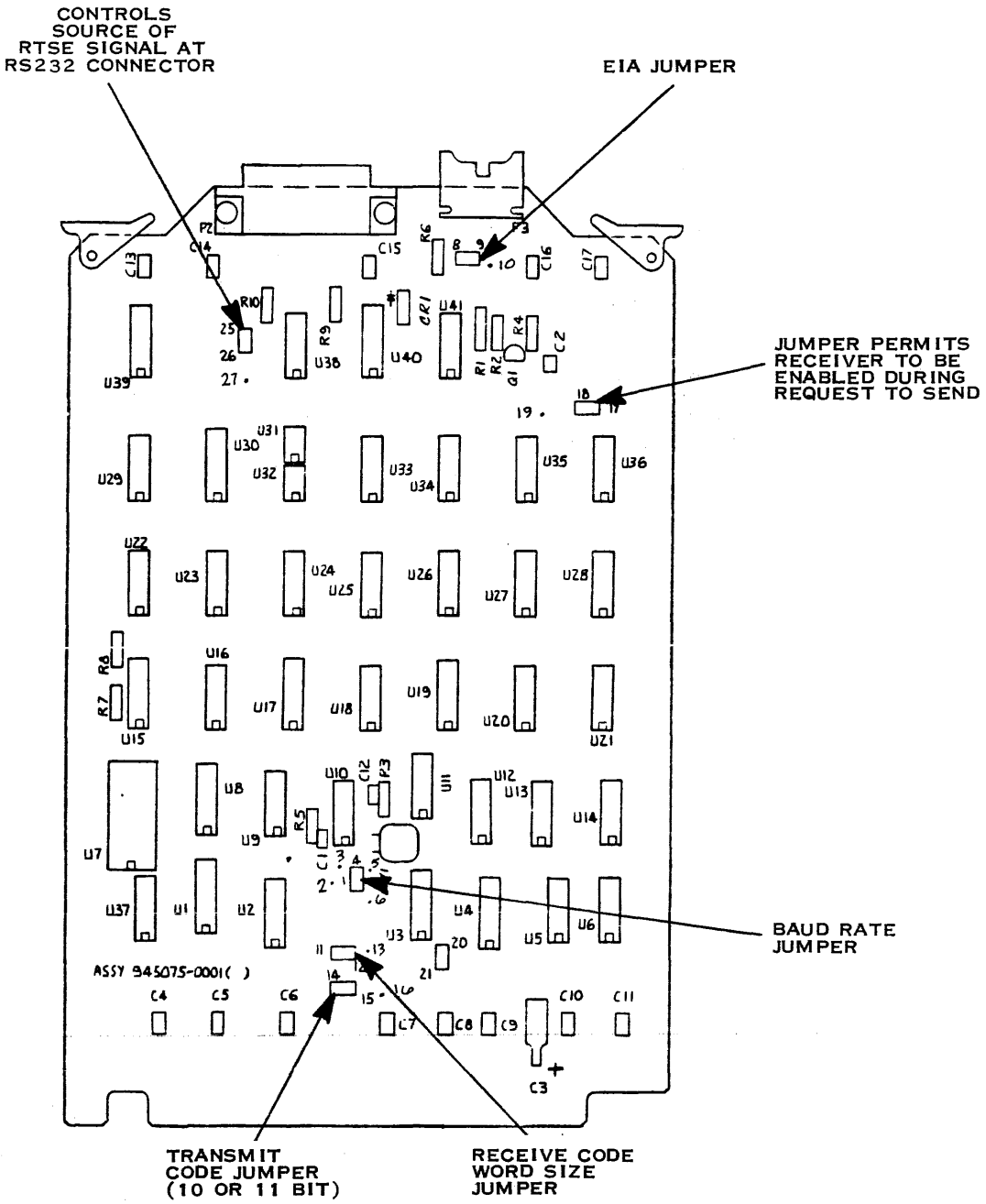


Figure 1-24. Power Supply Assemblies and Subassemblies



SUMMARY OF JUMPER OPTIONS

TERMINAL DEVICE	BAUD RATE	JUMPER CONNECTIONS
733 KSR DATA TERMINAL	300	E1 TO E3, E8 TO E9, E11 TO E12, E14 TO E15, E17 TO E18, E20 TO E21, E25 TO E26
733 ASR DATA TERMINAL	1200	E1 TO E4 (ALL OTHERS SAME AS ABOVE)
588 OR 306 LINE PRINTER	4800	E1 TO E6, E26 TO E27 (ALL OTHERS SAME AS ABOVE)

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Figure 1-25. TTY/EIA Module Options

1.2.1.8 **CRU Expansion Board.** The CRU expansion board primarily expands the CRU interface in the main chassis to drive up to seven additional 990 expansion chassis. The board monitors for interrupts from the seven chassis using two independent interrupt recognition sections (A and B). If an interrupt occurs in chassis 1 through 4, the expansion board generates an INTA– (interrupt A). If the interrupt occurs in chassis 5 through 7, the expander board generates an interrupt B. The expander board then enables the interrupt ID lines from the highest priority chassis (chassis 1 highest priority, chassis 4 lowest priority in interrupt section A). The 990 software may then determine the source of the interrupt by executing an STCR instruction at address $F80_{16}$ (interrupt vector for section A) or $F90_{16}$ (interrupt vector for section B). As a result of the instruction, the CRU expander board serially transfers a 16-bit vector in the format shown in figure 1-26. As indicated in this figure, the interrupt vector identifies the chassis and the unit within the chassis which issued the interrupt. The vector also indicates the on-line status of each expansion chassis which reports to this interrupt monitoring section (chassis 1-4 for section A; chassis 5-7 for section B).

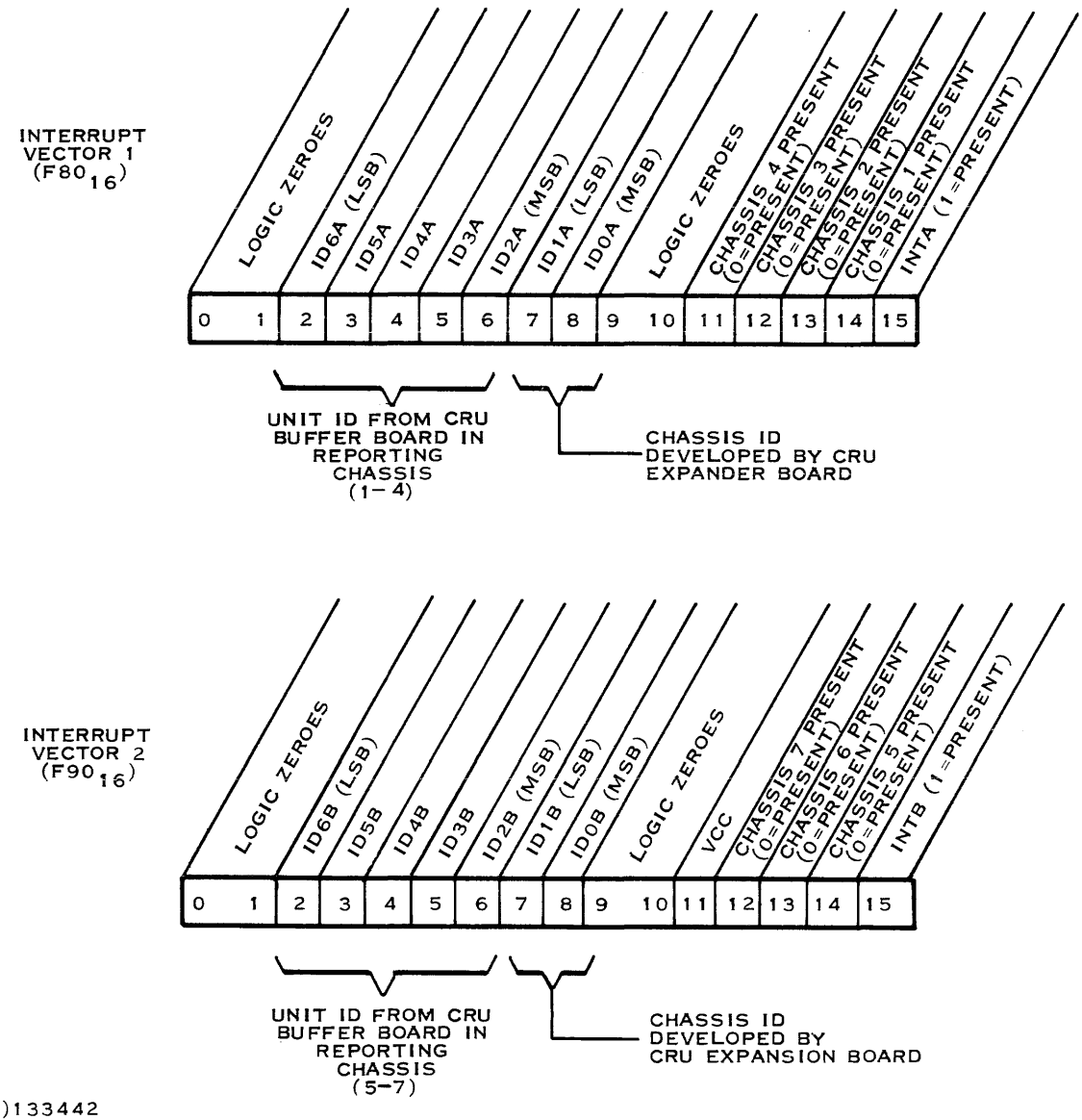


Figure 1-26. Expansion Interrupt Vector Format

The CRU expansion board also contains provisions for fanning-in a direct interrupt (IREQ–) from each of the seven chassis and issuing an INTC– to the CPU if a direct interrupt is received from any chassis. The direct interrupt scheme is used with peripherals requiring faster interrupt service than is available with the interrupt.

The interrupt on the originating board is cleared by the interrupt servicing software via a CRU instruction addressed to the board in the respective expansion chassis.

Interrupt Servicing Jumpers. The two interrupt servicing sections on the CRU expansion board are normally enabled by jumper wires between terminals E5 and E6 (section A) and between terminals E7 and E8 (section B). This option permits disabling the interrupt servicing logic on a CRU expander board when two CRU expander boards are installed in the main chassis (see figure 1-27).

Power On Reset Option. The CRU expander board also contains an option to accept either the power on reset from the power supply board (TLPRES–) via a jumper between terminals E1 and E2 or the reset signal from the CPU (TLIORES–) via a jumper between E3 and E4 (normal configuration). The I/O reset signal from the CPU permits a clear to be generated by either the power supply or by 990 software.

1.2.2 990 I/O EXPANSION CHASSIS. The 990 I/O expansion chassis is added to a system when the main chassis does not contain enough board slots to house all of the CRU interface boards required by the system. The chassis used for the I/O expansion chassis is identical to the main computer chassis except that it contains an operator panel instead of a programmer panel and slot 1 of the expansion chassis houses a CRU buffer board instead of an AU2 board. The interrupt wiring for the expansion chassis is accomplished through jumper plugs on the backpanel board and dc power is supplied by the main power supply in the chassis (identical to the main power supply used in the main chassis).

The operator panel on the expansion chassis contains a key switch which controls ac power to the chassis and a POWER LED which indicates when the power supplies are functioning properly. The interconnection between the operator panel and the CRU buffer board is accomplished through a 26-pin ribbon cable and connector which attaches to connector plug P5 on the top edge of the buffer board. The interface between the main chassis and the expansion chassis is accomplished through a 12-foot ribbon cable (Part Number 945001-1) which attaches to one of the seven ports on the CRU expansion board in the main chassis (P3 through P9 depending on chassis number) and attaches to plug P3 on the top edge of the CRU buffer board in the expansion chassis.

1.2.2.1 Expansion Chassis Interrupt Scheme. A simplified block diagram of the interrupt system associated with a fully expanded 990/10 minicomputer system is shown in figure 1-28. As indicated in this figure, interrupts from each half-board slot in a given expansion chassis is wired to the interrupt jacks J2 and J3 on the backplane board. These interrupt lines are then jumpered to selected interrupt levels 1 through 15 using wire jumpers on the backplane board. The 15 interrupt levels are routed to an interrupt scanner on the CRU buffer board which is located in slot 1 of the expansion chassis. If an interrupt is received on any of the 15 interrupt levels, the CRU buffer board issues an "interrupt present" to the CRU expander board in the main chassis (see figure 1-29). The CRU expander board then responds to the interrupting chassis (having highest priority) with an ID enable signal. This enable is used to gate the five ID bits (which represent the binary value of the interrupt level) back to the CRU expander board. In response to an interrupt request from any of the seven chassis, the CRU expander board issues either an interrupt A (interrupt present in chassis 1 through 4), an interrupt B (interrupt present from chassis 5 through 7) or an interrupt C (direct interrupt present from interrupt chassis 1 through 7).

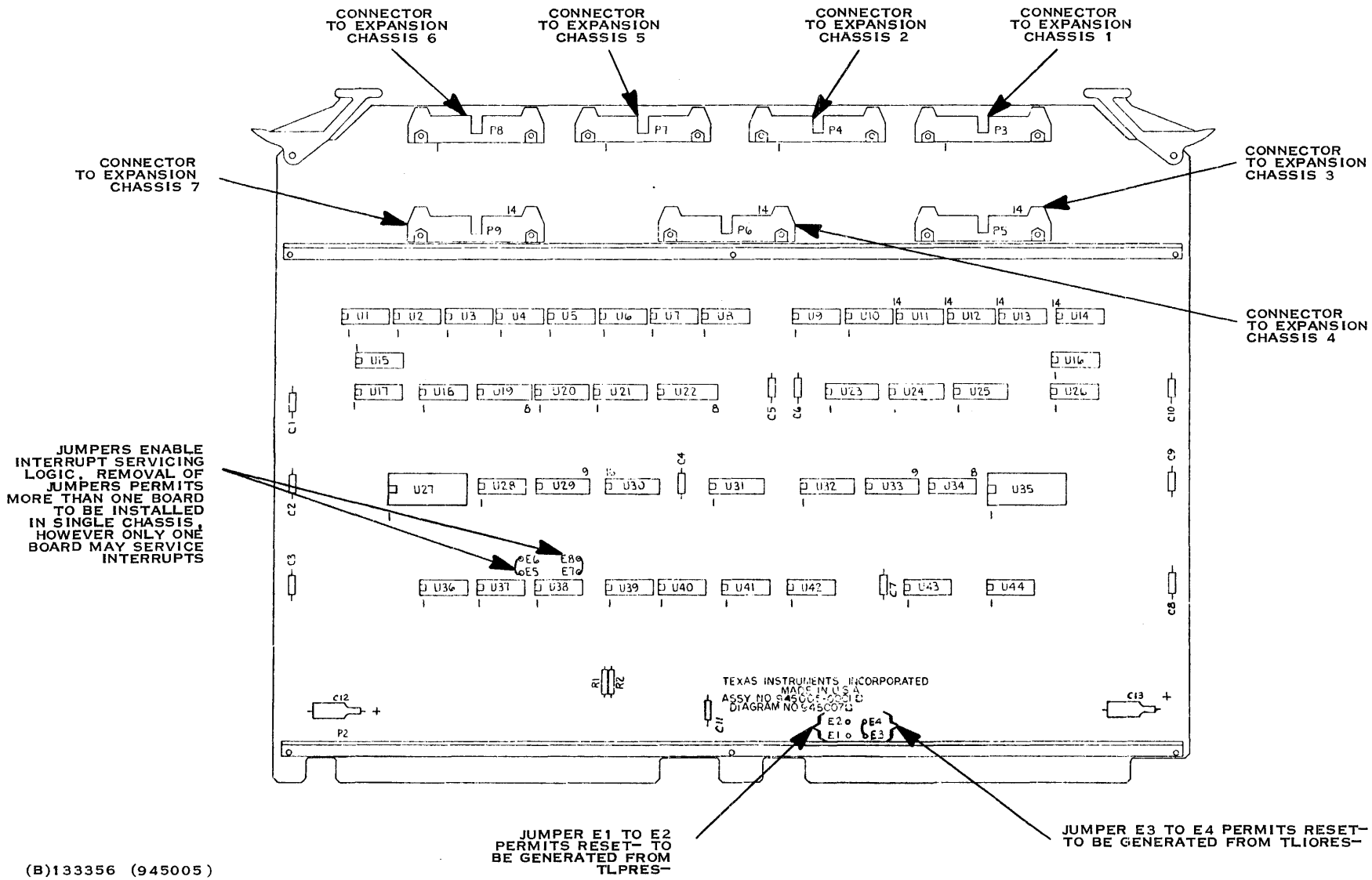


Figure 1-27. CRU Expansion Board Options

Interrupts A and B are used to activate the expander interrupt servicing routine which in turn addresses the appropriate interrupt servicing section (A or B) with a store CRU instruction addressed to either $F80_{16}$ (interrupt A) or $F90_{16}$ (interrupt B). As a result of the store CRU instruction, a 16-bit interrupt vector is sent back to the processor. As shown in figure 1-28, the interrupt vector contains the ID of the originating unit (developed by the CRU buffer board in the interrupting chassis), the ID of the expansion chassis (developed in the CRU expander board) and the status of the expansion chassis associated with the reporting interrupt section (chassis 1-4 associated with interrupt section A and chassis 5-7 associated with section B). The interrupt vector is then used to select the proper interrupt servicing routine associated with the interrupting board.

If a direct interrupt (INT C–) is generated, the interrupt is processed more speedily since the expansion interrupt servicing routine is bypassed and the processor traps directly to the board-level interrupt servicing routine. This interrupt scheme is used when peripherals requiring rapid response to interrupts are located in the expansion system.

1.2.2.2 **CRU Expansion Address Scheme.** A CRU address map for the standard fully expanded 990/10 system is shown in figure 1-30. As indicated in this figure, each chassis is assigned a band of location dependent CRU addresses which are used to address the CRU interface boards implemented within a given chassis. The chassis number (1 through 7) which is assigned to each chassis is determined by an ID plug on the CRU buffer board.

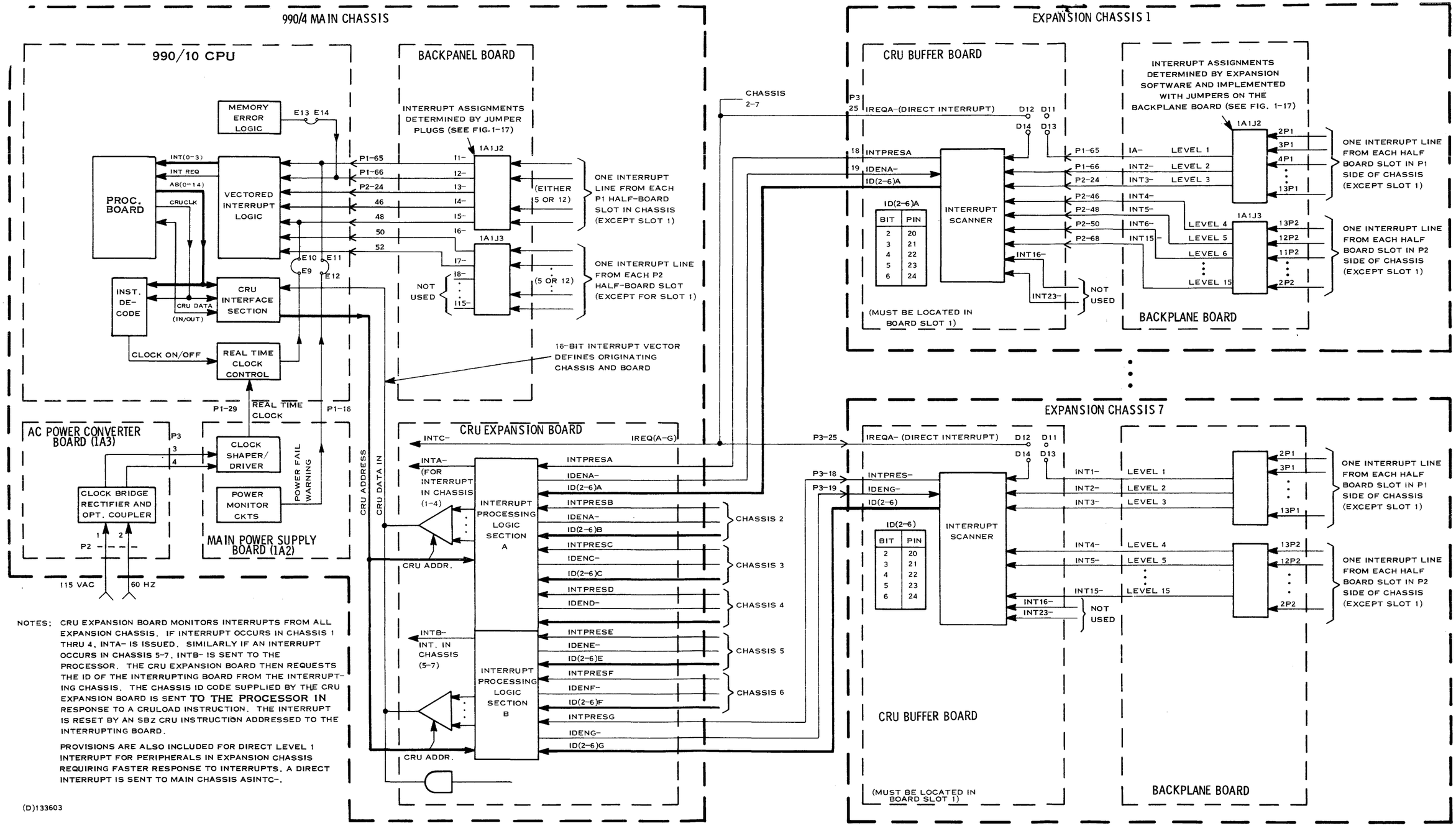
In addition to the location dependent address blocks, several bands of addresses are assigned as dedicated or location independent addresses. In order to implement the dedicated CRU addresses, the boards associated with these address functions contain decoding logic that permits the board to respond to its dedicated address regardless of location. For example, the two interrupt servicing sections on the CRU expansion board are assigned dedicated addresses F80 and F90, respectively. The interrupt servicing logic on the expander board will respond to these CRU addresses regardless of physical placement of the CRU expansion board.

1.2.2.3 **CRU Buffer Board.** The CRU buffer board contains fanout and fanin circuits for the CRU interface signals including CRUBITIN, CRUBITOUT, CRUCLK and CRU address lines. The board also contains an interrupt scanner circuit which monitors the interrupt lines from the various CRU interface boards within the chassis and issues an interrupt to the CRU expander board in the main chassis anytime an interrupt is detected. When the interrupt is acknowledged by means of an ID enable signal, the CRU buffer board sends back the ID code corresponding to the originating interrupt level (1 through 15). The interrupt scanner then halts until software clears the interrupt on the originating board.

The various jumper options on the CRU buffer board are shown in figure 1-31 and briefly described in the following paragraphs.

Chassis Number Select Plug. The jumper plug J2 may be installed into any of seven slots on P4 to assign the chassis addresses to a given expansion chassis. This plug determines which of the seven possible chassis decode lines is routed to the module select decode circuitry on the board.

Direct Interrupt Jumper Option. Interrupt level 1 from the interrupt jumper plug on the backpanel board may be routed through the interrupt scanner and processed by the expansion interrupt routine or wired directly to the interrupt plug on the backpanel board in the main chassis to permit faster interrupt processing. The latter is method is used when a peripheral requiring fast interrupt processing response time is implemented in one of the expansion chassis.



NOTES: CRU EXPANSION BOARD MONITORS INTERRUPTS FROM ALL EXPANSION CHASSIS. IF INTERRUPT OCCURS IN CHASSIS 1 THRU 4, INTA- IS ISSUED. SIMILARLY IF AN INTERRUPT OCCURS IN CHASSIS 5-7, INTB- IS SENT TO THE PROCESSOR. THE CRU EXPANSION BOARD THEN REQUESTS THE ID OF THE INTERRUPTING BOARD FROM THE INTERRUPTING CHASSIS. THE CHASSIS ID CODE SUPPLIED BY THE CRU EXPANSION BOARD IS SENT TO THE PROCESSOR IN RESPONSE TO A CRULOAD INSTRUCTION. THE INTERRUPT IS RESET BY AN SBZ CRU INSTRUCTION ADDRESSED TO THE INTERRUPTING BOARD.

PROVISIONS ARE ALSO INCLUDED FOR DIRECT LEVEL 1 INTERRUPT FOR PERIPHERALS IN EXPANSION CHASSIS REQUIRING FASTER RESPONSE TO INTERRUPTS. A DIRECT INTERRUPT IS SENT TO MAIN CHASSIS ASINTC-.

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Figure 1-28. 990 Interrupt Paths, Simplified Diagram

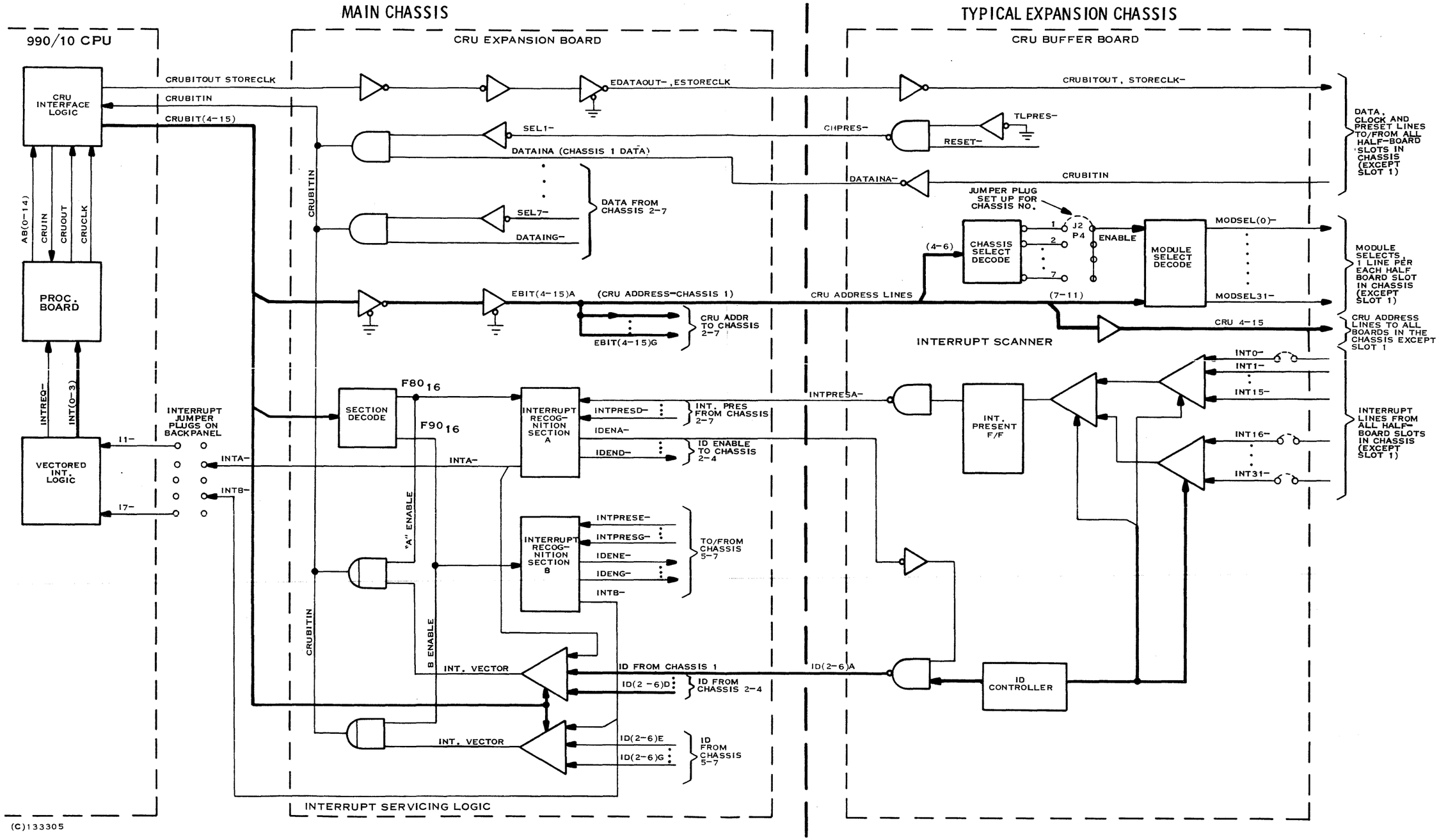


Figure 1-29. CRU Expansion, Simplified Block Diagram

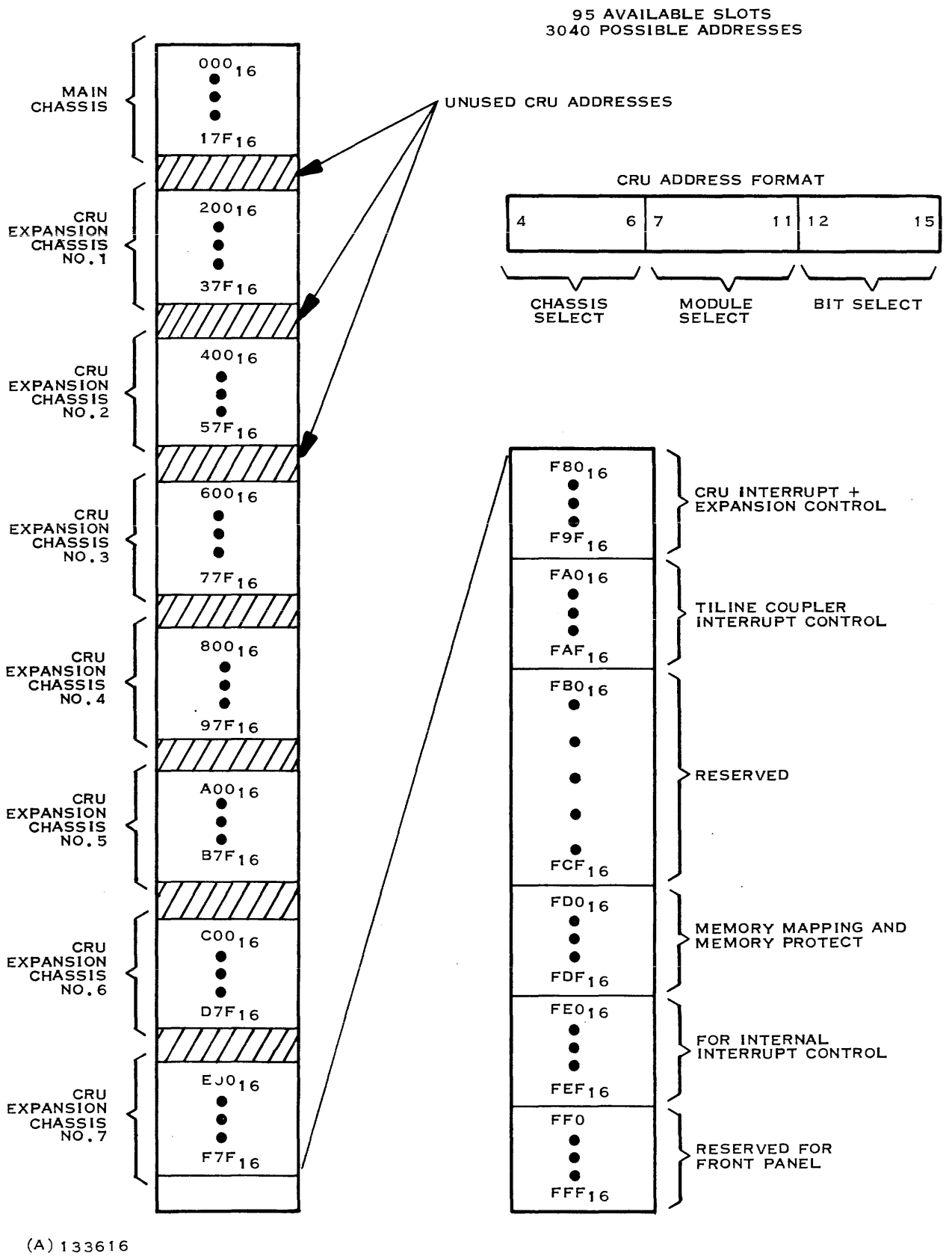


Figure 1-30. CRU Address Map for Standard Expansion Implementation Using 12-inch Chassis

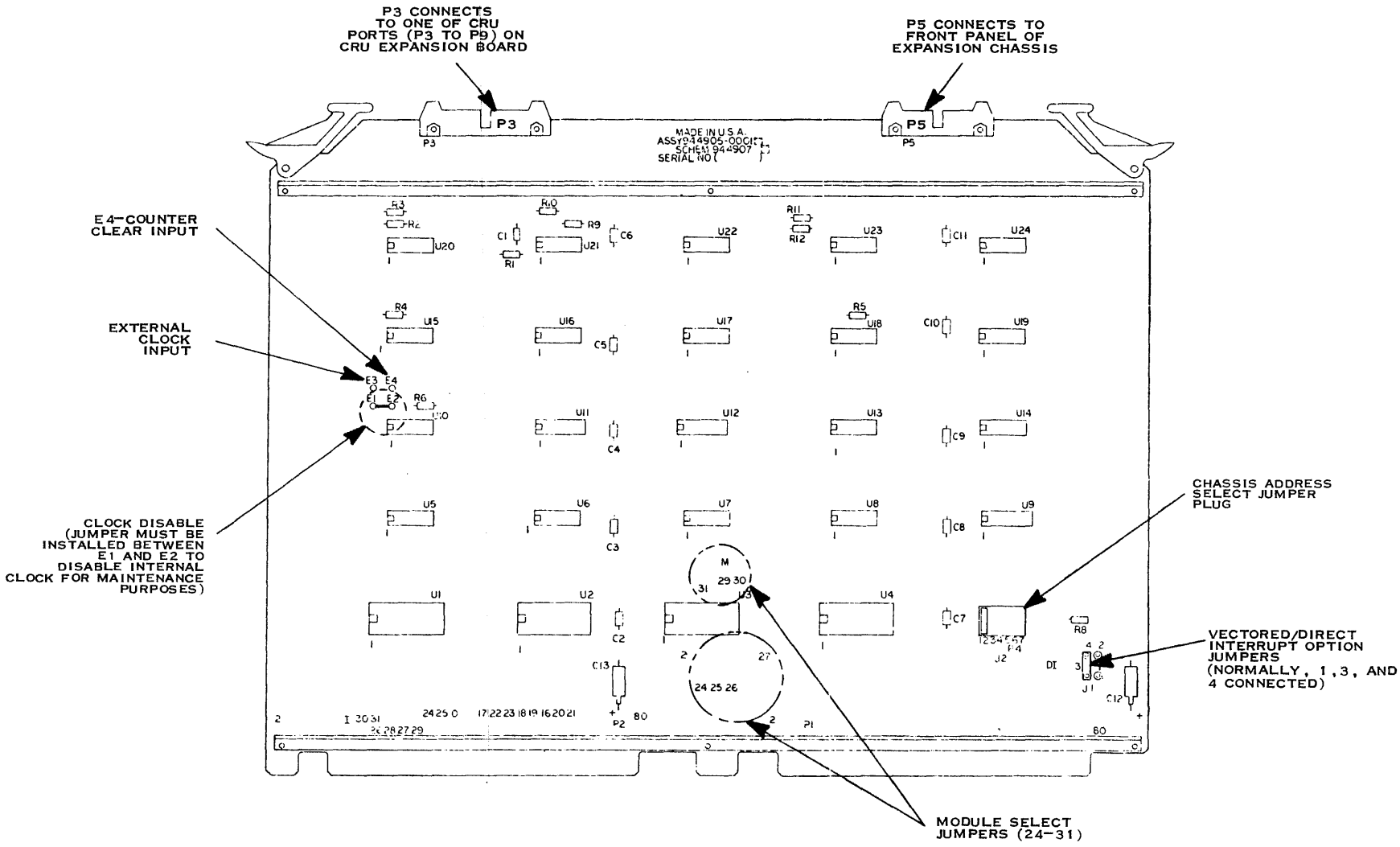


Figure 1-31. CRU Buffer Board Options

For conventional scanner processing of interrupt level 1, a jumper wire is installed between DI3 and DI4. For direct interrupt processing of interrupt level 1, the jumper between DI3 and DI4 is removed and a jumper is installed between DI1 and DI2.

Interrupt Expansion Jumpers. Jumper options are also provided for interrupt levels 0 and 16 through 31.

Interrupt Scanner Maintenance Options. For normal interrupt scanner option, the jumper wire between E1 and E2 is not installed to enable the internal scanner clock. For maintenance operations, a jumper between E1 and E2 may be installed and the interrupt scanner may be driven with an external clock source using terminal E3 as an input point. The scanner may also be cleared by temporarily connecting a ground potential at terminal E4.

SECTION II

FIELD SERVICE TEST EQUIPMENT

2.1 GENERAL

This section describes the 990 Maintenance Unit and other tools, test equipment, diagnostic cassettes and spares required for field-level maintenance of 990/10 Minicomputer Systems.

2.2 TOOLS, TEST EQUIPMENT AND SPARES REQUIRED FOR FIELD MAINTENANCE

A listing of tools, test equipment and replaceable parts required to perform field-level maintenance is provided in tables 2-1 through 2-3, respectively.

2.3 990 MAINTENANCE UNIT

The 990 Maintenance Unit consists of a conventional 990 programmer panel, a 733 ASR cassette transport and a maintenance controller board (containing the cassette read electronics and CRU interfacing logic) all housed in a portable aluminum carrying case as shown in figure 2-1. The maintenance unit permits diagnostics to be loaded into a system not equipped with an operational 733 ASR data terminal and provides for manual control of a computer equipped with an operator panel or inoperative programmer panel. The maintenance unit's carrying case also provides storage space for manuals, CPU ROMs, diagnostic cassettes and interface cables.

Table 2-1. Recommended Tools and Test Equipment for Field-Level Maintenance

Nomenclature	Function	TI Part Number
990 Maintenance Unit (115 Vac Operation)	Used to load diagnostics and display test results in 990/10 systems not equipped with 733 ASR data terminal.	946710-1
990 Maintenance Unit (230 Vac Operation)	Same as above but equipped to operate from 230 Vac input power.	946710-2
14/16 Pin IC inserter/ extractor tool	Used to remove and replace memory ICs.	–
Standard Technician tool kit	Used to assemble/remove assemblies and components and to install new components and assemblies.	–

Table 2-2. 990/10 Diagnostic Tests

Diagnostic Name	Description	TI Part Number
CPU		
AU10	AU Test	945433
HDT10	Hardware Demonstration Test	945456
MEMORY		
RAM10	RAM Test	945439
MAPTST	Map Logic Test	945441
ROMVER	ROM Verifier Test	945443
EROMBT	EROM Memory Board Test	945459
CRU DEVICES		
CRUSOP10	CRU and Hardware XOP Test	945445
LPTEST	Line Printer Diagnostic	945448
CRT913	913 CRT Diagnostic	945450
TST 733	733 ASR KSR Data Terminal Test	945447
FLPSDK	Floppy Disk Test	945435
IO16	16 I/O TTL Module Test	945452
TTYEIA	Full Duplex TTY/EIA Interface Module Test	945453
ROMPG	PROM Programmer Test	945454
CRUEXP	CRU Expansion Chassis Interface Test	945457
CARDRD	Model 804 Card Reader Test	945449
CRCOMM	CRU Synchronous and Asynchronous Comm Interface Test	945437
DAADC	D/A and A/D Converter Test	945438
TILINE DEVICES		
DSKM31	Model 31/32 Disk Test	945451
DSKTRI	Trident Disk Test	945436
TAPTST	979 MT Test	937773

Table 2-3. Field Replaceable Components for 990/10 System

Assembly/Subassembly	TI Part Number
LOGIC BOARDS	
990/10 AU1 board	944930
990/10 AU2 board	944940
990/10 AU2B board (with mapping)	944950
ECC 16KB expansion board	946655-0002
Add-on (array) ECC board	
• with 16KB ECC RAM	945093-0002
• with 32KB ECC RAM	945093-0004
• with 48KB ECC RAM	945093-0006
96KB memory controller, standard version	
• with no memory installed	948960-0001
• with 32KB ECC RAM	948960-0002
• with 64KB ECC RAM	948960-0003
• with 96KB ECC RAM	948960-0004
96KB memory controller, fine line version	
• with no memory installed	2261980-0005
• with 32KB ECC RAM	2261980-0006
• with 64KB ECC RAM	2261980-0007
• with 96KB ECC RAM	2261980-0008
256KB add-on memory array board (used with 96KB memory controller)	
• with 64KB ECC RAM	948955-0001
• with 128KB ECC RAM	948955-0002
• with 192KB ECC RAM	948955-0003
• with 256KB ECC RAM	948955-0004
Memory expansion board	
• with 16KB RAM	944945-0002
• with 24KB RAM	944945-0003
• with 32KB RAM	944945-0004
• with 40KB RAM	944945-0005
Memory parity kit (includes two RAM packages)	945120-0002
TILINE bus expansion kit	945091-0001
990 EPROM memory module	945170-0001
CRU expander board	945005-0001
CRU buffer board	944905-0001
TTY/EIA terminal interface module	945075-0001
990 communications interface module	946104-0001

Table 2-3. Field Replaceable Components for 990/10 System (Continued)

Assembly/Subassembly	TI Part Number[
LOGIC BOARDS (Continued)	
913 video display terminal controller	946695-0001
Card reader interface module	945185-0001
16 I/O EIA data module	945140-0001
800 BPI Mag Tape Controller	947555-0001
16 I/O TTL data module	945145-0001
1600 BPI Mag Tape Controller	948990-0001
Floppy disc controller	945940-0001
Trident disc controller	947525-0001, 0002
Diablo disc controller	974905-0001
CHASSIS AND POWER SUPPLY ASSEMBLIES	
6-slot chassis with operator panel	944960-0002
6-slot chassis with programmer panel	944960-0001
13-slot chassis with operator panel and 20-amp P.S.	945070-0002
13-slot chassis with programmer panel and 20-amp P.S.	945070-0001
13-slot chassis with operator panel and 40-amp P.S.	945050-0002
13-slot chassis with programmer panel and 40-ampere power supply	

Table 2-3. Field Replaceable Components for 990/10 System (Continued)

Assembly/Subassembly	TI Part Number
CHASSIS AND POWER SUPPLY ASSEMBLIES (Continued)	
Ac power converter board	946650-1
20 ampere main power supply board	944970-1
40 ampere main power supply board	944980-14
Standby power supply board	944990-1
Standby power supply kit (with board, batteries, and all hardware)	945128-1
International voltage kit, 100 volt service	945125-1
International voltage kit, 230 volt service	945125-2
Operator panel assembly	945030-1
Programmer panel assembly	945020-1
Interrupt jumper	975321-4
Chassis center card guide kit	945129-1
CABLE ASSEMBLIES	
CRU expansion cable (12 feet)	945001-1
Model 913A VDT extension cable (50 feet)	974998-50
Model 588/306 line printer extension cable (50 feet)	975056-50
LOADER ROMS, MEMORY CHIPS AND REPLACEABLE ICS	
733 ASR/card reader loader ROM	945134-1
733 ASR/card reader loader ROM with self-test	945134-2
990/10 floppy disc loader ROM	945134-6
990/10 floppy disc loader ROM with self-test	945134-7
1024 by 8-bit EPROM IC	996019-1
TMS 4050 4K Dynamic RAM	972659-1
TMS 4060 4K Dynamic RAM	974679-1
TMS 4116 16K Dynamic RAM	996680-1

Table 2-3. Field Replaceable Components for 990/10 System (Continued)

Assembly/Subassembly	TI Part Number
CHASSIS REPLACEABLE COMPONENTS	
Fuse 1F1, 10 amp slo-blo (BUS MDA10.0)	772995-4
Fuseholder	972690-1
Standby replacement plug	946739-1
13-slot chassis air filter	945152-2
6-slot chassis air filter	945152-1
Terminal block 1TB1	975270-5
Surge voltage protector	974805-7
5-inch fan	947512-1
Ac line filter (1FL1)	972838-5
Capacitor (1C1)	972930-69

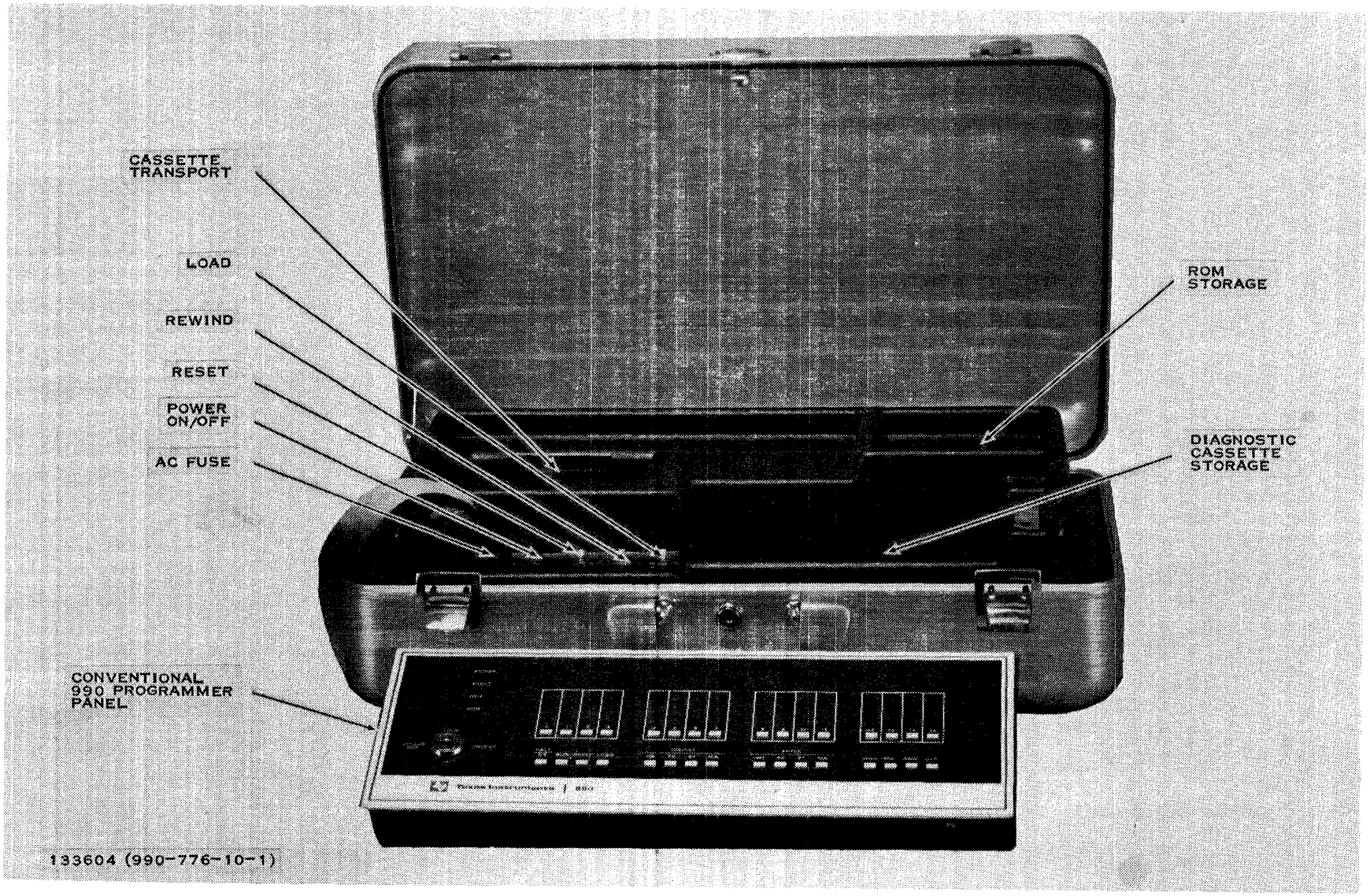


Figure 2-1. TI Model 990 Maintenance Unit

2.3.1 **TEST CONFIGURATIONS.** The maintenance unit accommodates two different test configurations depending on the system under test. In the first configuration (figure 2-2), the maintenance unit ties into the system under test through P7 on the 990/10 interface board (after removal of the existing interface cable from the chassis-mounted operator or programmer panel). In this configuration, diagnostic programs are loaded into program memory from the cassette tape transport on the maintenance unit and the test results are displayed on the DATA LEDs on the programmer panel in the maintenance unit. This configuration is used when the system is not equipped with an operational 733 ASR data terminal.

2.3.1.1 **Standalone Programmer Panel.** The programmer panel may also be detached from the maintenance unit and used as a standalone unit. In this case, the existing interface cable from the chassis-mounted operator or programmer panel is removed from P7 on the interface board and the maintenance unit's programmer panel interface cable is connected to P7 (see figure 2-3). In this configuration, the key switch on the chassis-mounted panel controls the application of ac power to the computer but all other functions are controlled by the standalone programmer panel.

This configuration is used when the system under test is equipped with an operator panel or inoperative programmer panel but contains an operative 733 ASR data terminal. In this case, the diagnostic cassettes are loaded into the system from the 733 ASR and the programmer panel is used to display test data from selected registers in the processor board or from selected memory locations on any of the boards containing memory storage.

2.3.2 **OPERATING CONTROLS AND INDICATORS.** The maintenance unit's operating controls and indicators are shown in figure 2-4 and listed and described in table 2-4. Basically, the maintenance unit contains a POWER ON/OFF switch which controls power to the maintenance unit, a RESET switch which initializes the controller board in the maintenance unit, a REWIND switch which is used to rewind cassette tapes, a LOAD switch which is used to initiate diagnostic load operations plus the conventional controls and indicators found on the 990 programmer panel. However, the function of three of the programmer panel controls and indicators are slightly different when the programmer panel is used as a part of the maintenance unit. These differences include:

- Key switch – Does not affect ac power to the computer or maintenance unit, but otherwise exercises the same key control over program intervention in the computer.
- POWER LED – Indicates the status of the power supply in the maintenance unit rather than the power supply in the computer chassis.
- FAULT LED – May be lit by either the computer (self-test failure) or by the maintenance controller board in the maintenance unit in the event of a faulty tape read operation.

The functions of all other programmer panel controls and indicators are exactly the same as those of a conventional chassis-mounted programmer panel (see figure 2-4 and table 2-4).

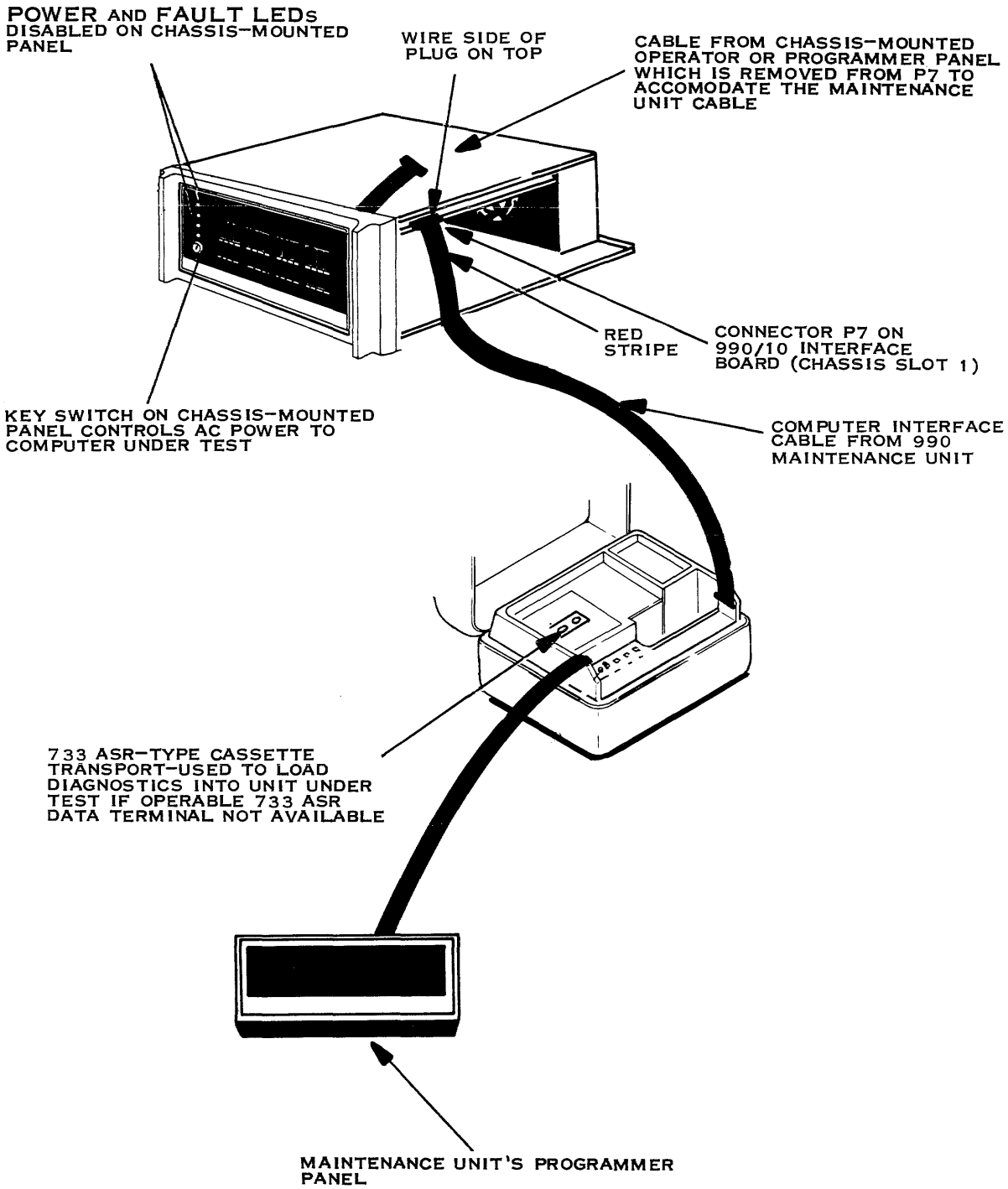


Figure 2-2. Test Setup for System not Containing 733 ASR Data Terminal

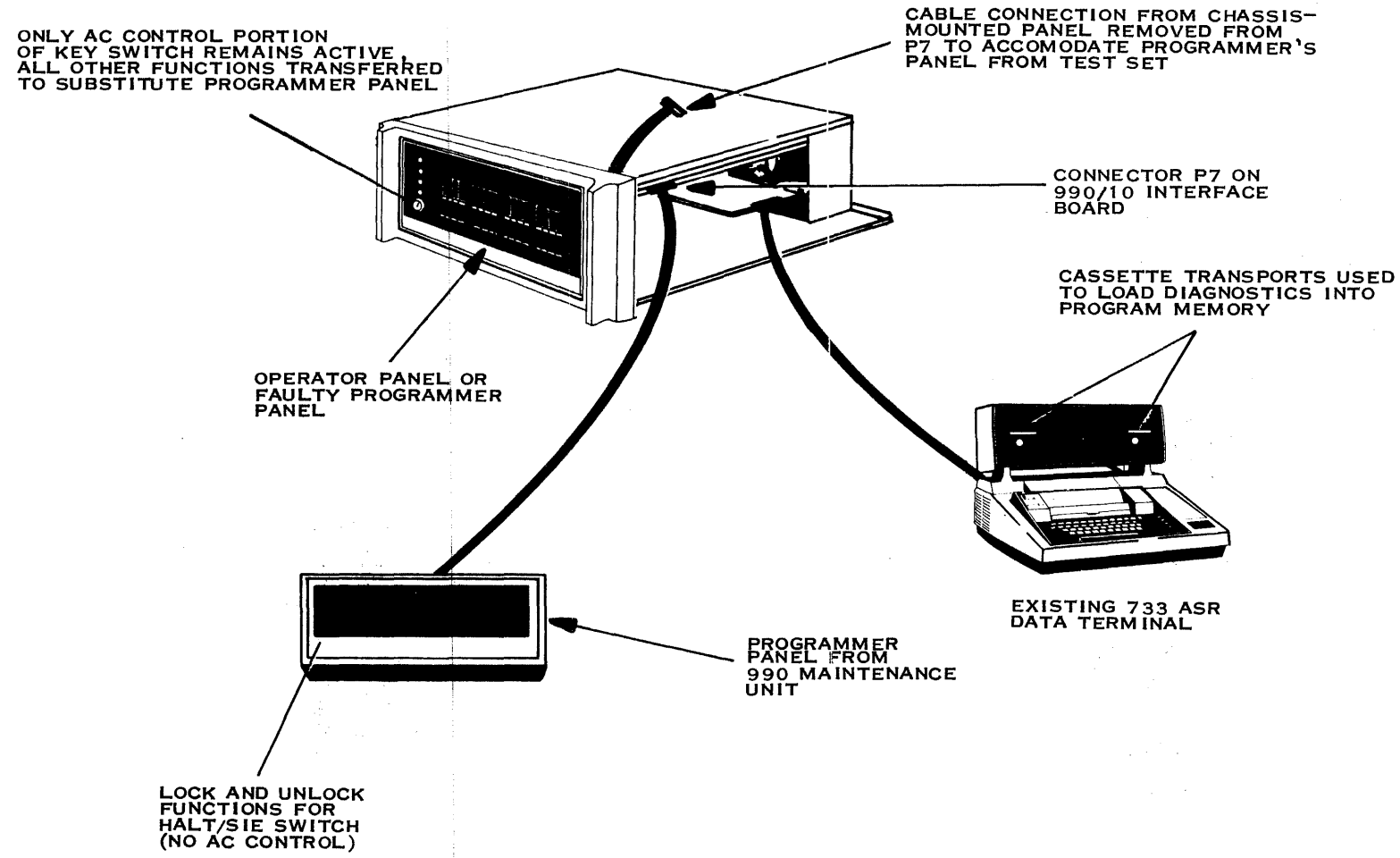


Figure 2-3. Alternate Test Setup Using Programmer Panel Only

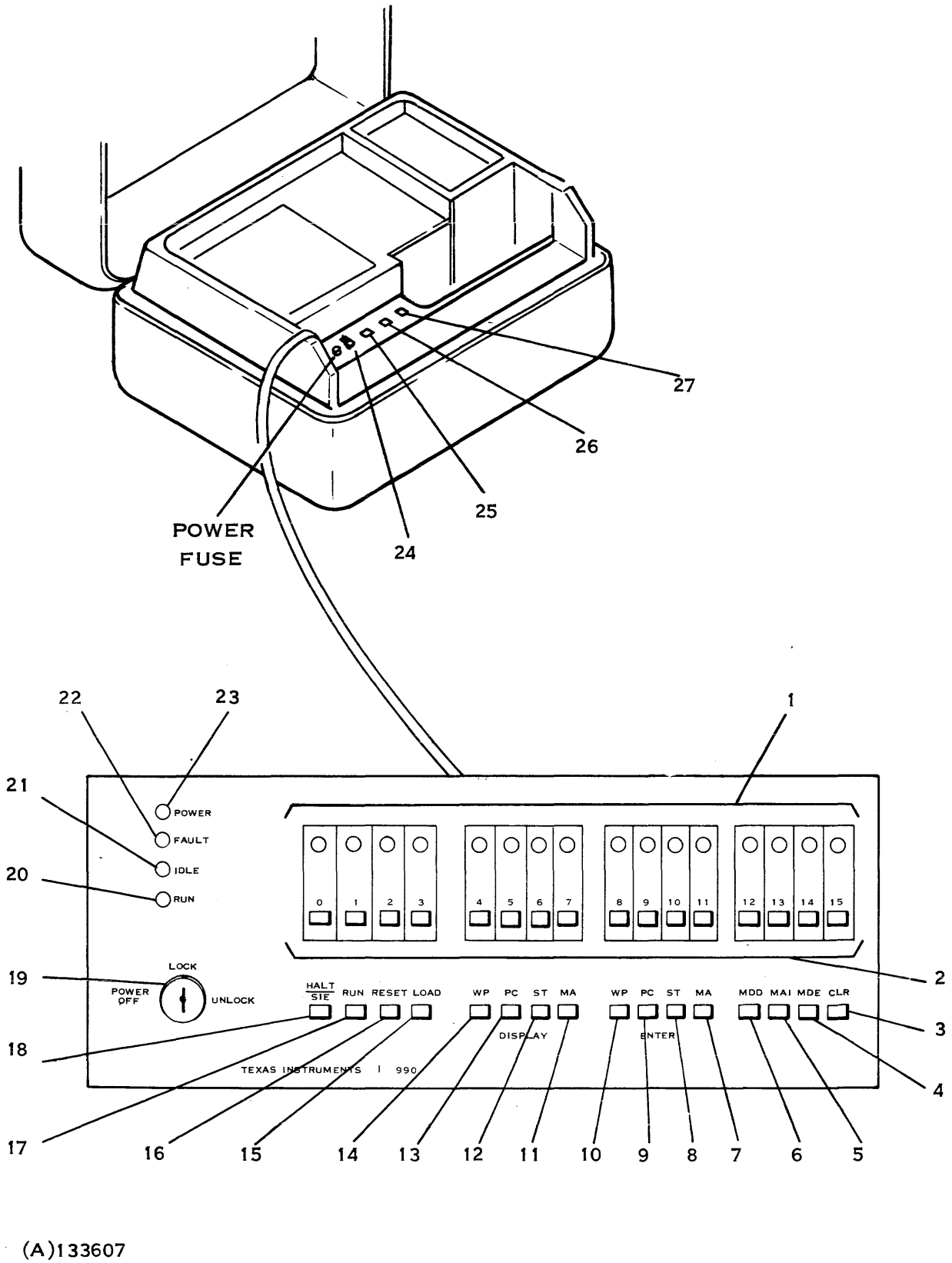


Figure 2-4. Maintenance Unit Controls and Indicators

Table 2-4. Maintenance Unit Controls and Indicators

Ref. No.	Control or Indicator	Function
1	DATA LEDs	The DATA LEDs are used to display data being entered into a CPU register or memory location or data presently stored in a register or memory location. During execution of the diagnostics, error numbers (in hex) are displayed on the right byte and the left byte is forced to all 1's (see error message number descriptions in 990 Computer Diagnostics Handbook). A lit LED denotes a logic 1, an extinguished indicator denotes logic 0. The LSB is displayed on the far right of the LEDs. In the HALT mode, the LEDs display a computer register contents, memory contents or value entered into computer memory via the data entry switches depending on which switches are pressed (see ref. 5, 7, 9, 11, 13, 15).
2	DATA entry switches	Used in conjunction with the ENTRY switches on the panel to enter data and addresses into selected computer registers and memory locations (active only when the panel is in the HALT mode of operation). In the HALT mode, the data LED located immediately above each data entry switch lights as each switch is pressed. The value indicated by the DATA LEDs is then stored in the register or memory address selected by the entry switches.
3	CLR switch	When pressed, this switch clears the DATA LED displays.
4	MDE switch	This switch is pressed to transfer a value displayed on the DATA LEDs to the memory location defined by the contents of the memory address (MA) register in the computer.
5	MAI switch	The memory address increment (MAI) switch is pressed to increment the value stored in the memory address register by a value of 2.
6	MDD switch	When pressed, this switch causes the contents of the memory location defined by the contents of the memory address register to be displayed on the DATA DISPLAY LEDs.
7	ENTER MA switch	When pressed, this switch causes the value displayed by the DATA LEDs to be entered into the computer's memory address register
8	ENTER ST switch	When pressed, the value displayed on the DATA LEDs is entered into the computer's status register.
9	ENTER PC	When pressed, the value displayed on the DATA LEDs is loaded into the computer's program counter.
10	ENTER WP	When pressed, the value displayed on the DATA LEDs is loaded into the computer's workspace pointer register.
11	DISPLAY MA	When pressed, the value stored in the computer's memory address register is displayed on the DATA LEDs.
12	DISPLAY ST	When pressed, the contents of the computer's status register is displayed on the DATA LEDs.
13	DISPLAY PC	When pressed, the contents of the computer's program counter is displayed on the DATA LEDs.

Table 2-4. Maintenance Unit Controls and Indicators (Continued)

Ref. No.	Control or Indicator	Function
14	DISPLAY WP	When pressed, the contents of the computer's workspace pointer register is displayed on the DATA LEDs.
15	LOAD switch	For a programmer panel on the chassis (or PANEL mode of operation for the maintenance unit), pressing the switch causes the computer to trap to the ROM loader.
16	RESET switch	Pressing the RST switch results in an IORESET– pulse being generated which resets all units in the system.
17	RUN switch	When the computer is halted (programmer panel is active), pressing the RUN switch returns the computer to the RUN mode of operation and deactivates the panel.
18	HALT/SIE switch	When the computer is in the RUN mode (RUN LED is lit), pressing the HALT/SIE switch causes the computer to halt and begin processing the front panel software *if* the key switch is set to the UNLOCK position. Pressing the switch when the computer is not in the RUN mode causes the computer to execute a single instruction at the present PC (program counter) address. The contents of the program counter are incremented by two and displayed on the DATA LEDs.
19	Key switch	The key switch (OFF/LOCK/UNLOCK) switch prevents unauthorized computer program intervention. The key must be inserted into the switch and the switch set to the UNLOCK position in order to enable the output of the HALT/SIE switch to the computer. The ac power control function for the 990/4 computer is controlled by the key switch on the chassis-mounted operator or programmer panel.
20	RUN LED	The RUN LED lights when a low-active RUN– signal is generated by the computer indicating the computer is in the RUN mode. When this LED is lit, all switches on the panel except the HALT/SIE switch are disabled and the DATA LEDs are driven under program control. When the RUN LED is extinguished, the panel controls are active.
21	IDLE LED	Lights when the computer is executing an idle instruction (indication of computer inactivity for most interrupt driven software).
22	FAULT LED	The FAULT LED lights when the computer has detected a self-test diagnostic failure or if the maintenance unit has detected a tape data fault.
23	POWER LED	Lights when the POWER ON/OFF switch on the maintenance unit is set to the ON position and the maintenance unit's internal power supply is functioning properly.
24	POWER ON/OFF switch	Controls ac power to the maintenance unit.
25	RESET switch	Initializes the logic on the maintenance unit's maintenance controller board. Has no affect on the system under test.
26	REWIND switch	Causes the cassette tape in the cassette transport to rewind back to the beginning of the tape (tape motion stops when clear leader is sensed).
27	LOAD switch	When the programmer panel is in the HALT mode (RUN LED extinguished), this switch causes the program on cassette tape to be loaded into memory. When the load is complete, program execution begins.

2.3.2.1 **Maintenance Unit Operating Procedures.** Some of the more common operating procedures are briefly described in the following paragraphs. These procedures include:

- Changing panel mode of operation
- Mounting cassette tapes in maintenance unit
- Diagnostic load from cassette transport in maintenance unit
- Entering data into CPU registers or memory locations
- Displaying data from CPU registers or memory locations
- Single instruction execution

Changing Panel Mode of Operation. The programmer panel in the 990 maintenance unit may be operated in one of two modes including RUN and HALT. The computer initially comes up in the RUN mode when ac power is applied to the computer through the key switch on the chassis-mounted front panel. During this time, the RUN LED and all DATA LEDs on the programmer panel in the maintenance unit light and remain lit until the mode of operation changes. If the key switch on the programmer panel in the maintenance unit is set to the LOCK position, all controls on the panel are disabled. To change from the RUN mode of operation to the HALT mode, the key must be inserted in the switch and the key switch must be rotated to the UNLOCK position. At this point, only the HALT/SIE switch on the panel is enabled. When the HALT/SIE switch is pressed, the computer ceases normal program execution and traps to the panel software utility which is located in a ROM in the upper 256 words of address space on the processor board. At this time, the RUN LED on the programmer panel extinguishes and the outputs of the switches on the programmer panel are constantly monitored by software through the programmer panel CRU type interface. At this point, the panel is operating in the HALT mode.

In the HALT mode, a diagnostic tape may be loaded from the maintenance unit or information may be entered into or displayed from selected CPU registers or program memory locations.

In order to switch from the HALT mode of operation to the RUN mode, the RUN switch must be pressed on the programmer panel. This causes the CPU on the processor board to begin program execution at the memory address indicated by its program counter.

Mounting and Removing Tape Cassettes. In order to load a diagnostic tape cassette into the maintenance unit, the cassette transport door must be opened and the cassette inserted with the tape end up. The desired diagnostic title should be facing the operator as shown in figure 2-5. The cassette should then be firmly pressed into the transport such that the capstan and reel motors properly engage the cassette tape and reels. The transport door must then be closed to complete installation of the cassette.

To remove a cassette from the transport, the door should be opened to the first stop and then opened the rest of the way using a quick downward motion. This causes the cassette to eject from the tape transport. When not in use, the transport door should be closed to prevent accumulation of dust or dirt in the tape drive mechanism and read head.

Loading a Diagnostic Into Program Memory. Before initiating a load from a cassette tape, the POWER ON/OFF switch should be set to the ON position and the tape fully rewound by pressing the REWIND switch on the maintenance unit (reference no. 26 in table 2-4). The tape motion will automatically stop when the clear leader at the beginning of the tape is sensed by the maintenance controller board.

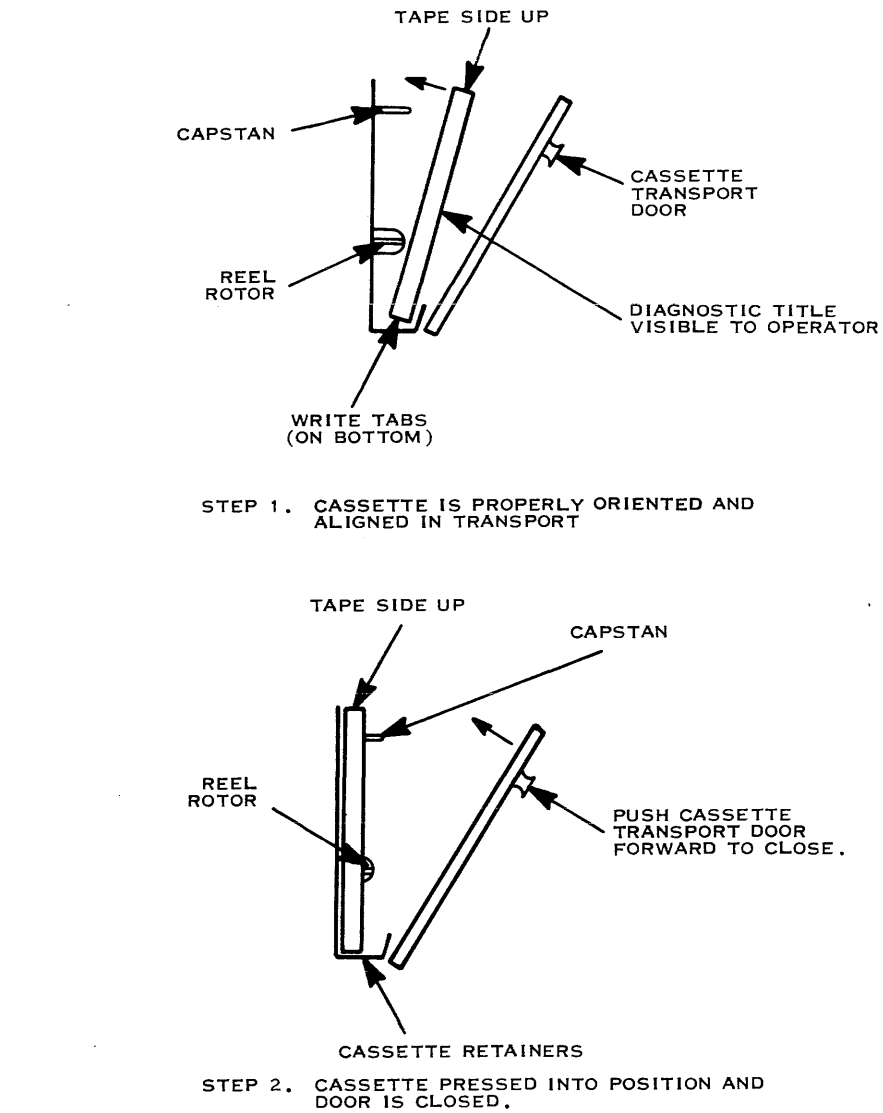


Figure 2-5. Cassette Tape Installation, Simplified Diagram

The Key switch on the 990/10 chassis-mounted operator or programmer panel must be set to one of the ON positions (ON, LOCK, or UNLOCK) to apply ac power to the computer. At this point, the RUN and POWER LEDs should light on the programmer panel in the maintenance unit. The panel's mode of operation must then be changed to the HALT mode by setting the Key switch on the maintenance unit's programmer panel to the UNLOCK position and pressing the HALT/SIE switch. The RUN LED on the panel should extinguish indicating the CPU is now processing the panel software utility. At this point, the panel software begins examining the switch outputs from the programmer panel. The cassette diagnostic load operation may now be initiated by pressing the LOAD switch (reference no. 27 in table 2-4) on the maintenance unit. The panel software recognizes the combination of the Load signal with the Maintenance Unit Present signal as a "Load from maintenance unit cassette" command (refer to the flowchart in figure 2-6). As a result, the panel software branches to the self-test program (if the loader ROM is equipped with self-test). If the self-test fails to execute correctly, the CPU lights the FAULT LED on the programmer panel in the maintenance unit and inhibits the diagnostic load operation.

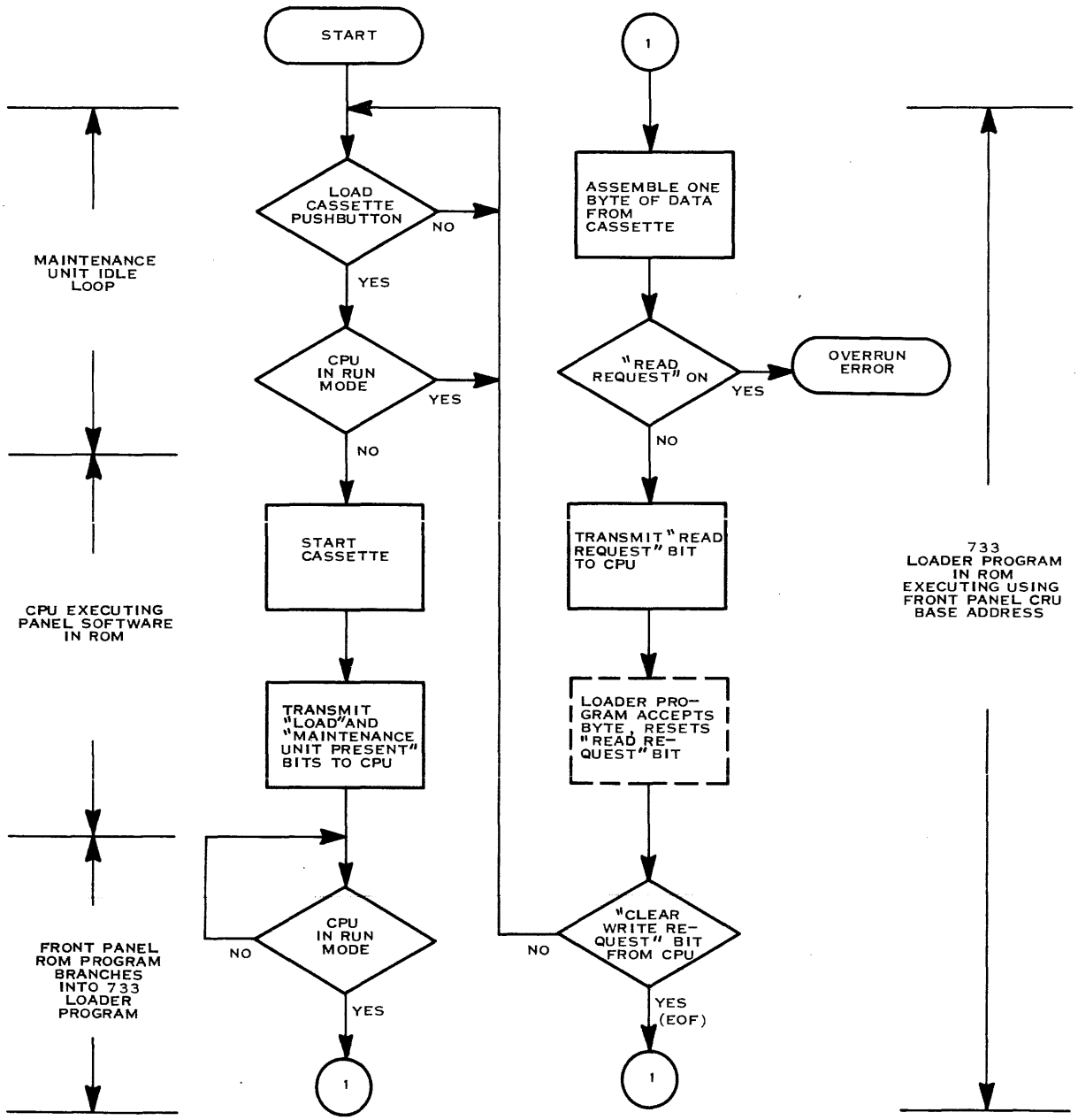


Figure 2-6. Diagnostic Load from Maintenance Unit, Flowchart

However, if the self-test executes satisfactorily (or if self-test is not present), the CPU branches to the ASR loader program which is also stored in ROM on the interface board. Since the load signal occurred with maintenance unit present, the software retains the CRU base address of the front panel.

At this point, the maintenance unit waits for RUN to turn on and then begins transmitting tape read data over the programmer panel CRU interface under control of the 733 loader program. Each time the maintenance controller board in the maintenance unit has a byte of data ready for the computer, it sets CRU bit 12 which is interpreted by software as a Read Request. When the 733 loader recognizes the Read Request, it serially transfers the next byte of data from the maintenance unit and resets CRU bit 12, freeing the maintenance unit to ready the next data byte. If the maintenance unit has another byte of data available before the loader has accepted the previous data byte (CRU bit 12 still set to the computer), the load operation is aborted and the FAULT LED lights on the maintenance unit's programmer panel. When the 733 loader decodes an End of File tag, it sets Clear Write Request via CRU output bit 13 which causes the maintenance unit to stop the cassette transport and return to an idle state.

SECTION III

MAINTENANCE

3.1 GENERAL

This section contains preventive and corrective field-level maintenance procedures for 990/10 minicomputer systems. This section includes assembly and disassembly procedures plus instructions for evaluating each system configuration and incorporating the necessary jumper options on replacement boards before installing the boards in a given system.

3.2 PREVENTIVE MAINTENANCE

Preventive maintenance for the 990/10 minicomputer system is limited to cleaning the washable intake air filter on each computer or expansion chassis in the system on a monthly basis (or more often if required) and periodically executing the diagnostics listed in table 2-2 to ensure that the system is functioning properly. All other preventive maintenance procedures are associated with the system peripherals and are described in the *Model 990 Peripheral Equipment Field Maintenance Manual.*

3.2.1 FILTER REMOVAL/REPLACEMENT. The washable filter used in the 990 chassis snaps into place and is removed by applying finger pressure along the top and bottom edges.

3.3 CORRECTIVE MAINTENANCE

Corrective maintenance at the field-level for the 990/10 is limited to the following:

- Removal and replacement of logic boards in the main chassis or one of the expansion chassis
- Removal and replacement of power supply boards
- Removal and replacement of interconnecting cables
- Removal and replacement of plug-in memory chips, ROM loaders and other 16-pin ICs
- Removal and replacement of the front panel assembly (programmer panel or operator panel) and/or key switch assembly
- Removal and replacement of cooling fans and ac power distribution components

3.3.1 LOGIC BOARD REMOVAL AND REPLACEMENT PROCEDURES. Logic boards are removed from a computer or I/O expansion chassis using the following procedure.

CAUTION

Always turn off power to the chassis before attempting logic board removal. Failure to observe this precaution may result in damage to the board since connector pins are temporarily misaligned during board removal and installation.

1. Set the KEY switch on the front panel of the chassis to the OFF position and remove the key to prevent accidental turn on before the new board has been installed.

2. Remove any top-edge cable connectors which may be mounted on the board.

3. Free the board from the backpanel connectors using the ejector tabs on the top of the board.

4. Remove board from chassis and immediately tag the board with such information as symptom, chassis and slot which the board was removed from and the system location and number (when several systems are installed at the same site).

5. Carefully record the jumper options and any other options (such as parity option, amount of memory, types of ROM loaders and custom ROMs, etc.) which may be installed on the board. These same options must be installed on the replacement board prior to installing the board in the system.

NOTE

Refer to Section I for a summary of board and system options.

6. Install the same options on the replacement board (unless an obvious problem is detected with the original setup of the board).

7. Note the serial number and board options incorporated on the replacement board and transfer this data to the system's configuration chart.

3.3.2 **OPERATOR/PROGRAMMER PANEL REMOVAL AND REPLACEMENT.** The front panel (either operator or programmer panel) may be removed and replaced using the following procedure.

WARNING

Prior to attempting the following removal procedure, disconnect the chassis power cord from ac power. The 115 Vac hot lead is exposed when the panel is removed.

1. Remove the left-side access panel (directly opposite the open side of the chassis) by removing the six holding screws around the perimeter of the panel.

2. Remove two screws from the rear of the panel on each side of the chassis (4 screws total).

3. Remove the two terminal leads from the ac microswitch on the rear of the key switch (the ac microswitch is the leftmost switch as viewed from the rear as shown in figure 3-1).

4. Remove connector plug 1A4P3 from top edge of the AU2 (interface) board and push plug through slot in chassis.

5. Install replacement panel by reversing the above procedure. See figure 3-2 for correct orientation of connector plug.

3.3.3 **POWER SUPPLY REMOVAL AND REPLACEMENT.** The 990 power supply consists of a 20 or 40 amp main power supply board, an ac power converter board and an optional standby power supply board and batteries. Removal and replacement procedures for these assemblies are provided in the following paragraphs.

WARNING

The chassis ac power cord must be removed from ac power before attempting the following power supply board removal procedures. Dangerous ac and dc voltages are exposed if this precaution is not observed.

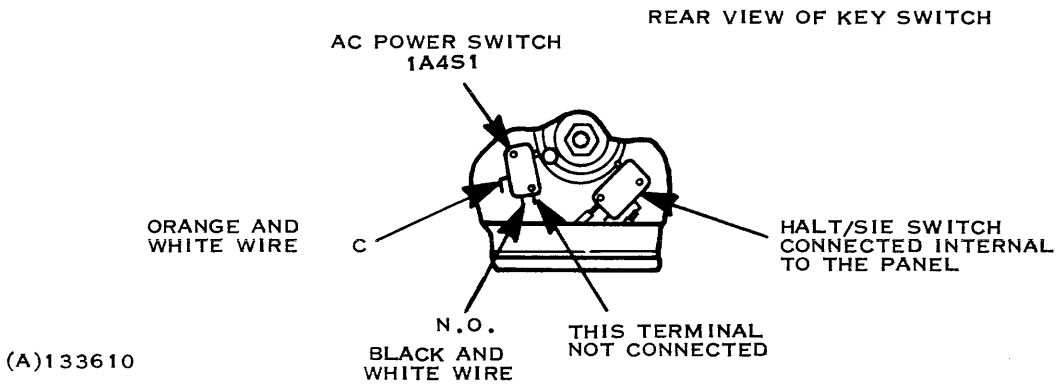


Figure 3-1. 1A4S1 Switch Connections

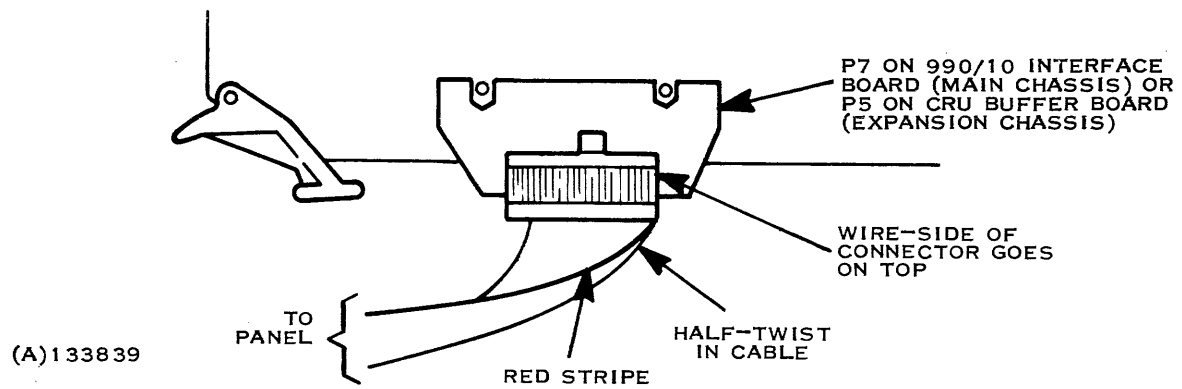


Figure 3-2. Programmer/Operator Panel Cabling Diagram

3.3.3.1 **Main Power Supply Board Removal and Replacement.** The main power supply board is removed and replaced using the following procedure:

1. If standby power supply is installed, this board must be removed first using the procedures provided in paragraph 3.2.3.3.

2. Remove 4 holding screws (2 from each end of board) and three standoffs from center of board.

3. Remove connectors 1A3P1A and 1A3P2 from board. Also, remove 1A3P1B if 40 amp main power supply board is being removed.

4. Carefully pull board straight back to unplug connector 1A3P3 from backpanel board.

5. Install replacement board by aligning board with two board guide pins which protrude from the backpanel board.

6. Carefully exert gentle pressure near the middle of the bottom edge of the replacement board to mate the backpanel and board connectors.

7. Install holding screws and standoffs removed from faulty board.

8. Install connectors 1A3P1A and 1A3P2 (also 1A3P1B if 40 amp supply).

9. Install 1A3P3 on 1A3J3 if standby power supply option is used. If standby option is not used, install standby replacement plug (Part Number 946739-1) on 1A3J3.

3.3.3.2 **Ac Power Converter Board Removal and Replacement.** The ac power converter board is removed and replaced using the following procedures.

WARNING

Remove chassis power plug from ac outlet before attempting the following removal/replacement procedures.

1. Remove the chassis filter by applying finger pressure along the top and bottom edges of the filter.

2. Remove the rear access cover (directly behind the filter unit) by removing the six screws around the perimeter of the cover.

3. Remove three cable connectors (1A2P1, 1A2P2, and 1A2P3) from board.

4. Remove single screw from center of board and remove board from chassis.

5. The replacement procedures are essentially the reverse of the removal procedures described in steps 1 through 4.

3.3.3.3 **Standby Power Supply Board Removal and Replacement.** The standby power supply is removed and replaced using the following procedures.

WARNING

Do not attempt removal of the standby power supply board without first unplugging the chassis power plug from the ac outlet.

1. Remove connector plugs 1A6P1 and 1A6P2 from standby board and remove 1A6P3 from 1A3J3 on main power supply board.

2. Remove five holding screws from board.

3. Installation of a replacement board is the reverse of steps 1 and 2.

3.3.3.4 **Cooling Fan Removal and Replacement.** The cooling fans in the 990 chassis may be removed and replaced using the following procedure.

WARNING

Before removing the rear access cover, remove chassis power plug from ac outlet.

1. Remove chassis filter by applying finger pressure at top and bottom of filter.

2. Remove rear access cover plate by removing six screws around perimeter of cover plate.

3. Remove two plug-on terminal wires from faulty motor.

4. Remove holding screws and lift motor out of chassis.

5. Install new motor by reversing steps 1 through 4.

3.3.4 IC REMOVAL AND REPLACEMENT. All memory ICs used on 990/10 logic boards are plug-in types which are installed in soldered-in IC sockets. These ICs may be removed and replaced using an IC extractor/installer tool. Since the IC leads are slightly flared, a special tool must be used to compress these leads during removal and installation.

NOTE

Failure to use the proper tool can result in bent pins and improperly seated ICs.

Also, correct IC orientation must be observed when installing a new IC. As shown in figure 3-3, the IC index should face the left side of the board for horizontally mounted ICs and face the bottom of the board for vertically oriented sockets.

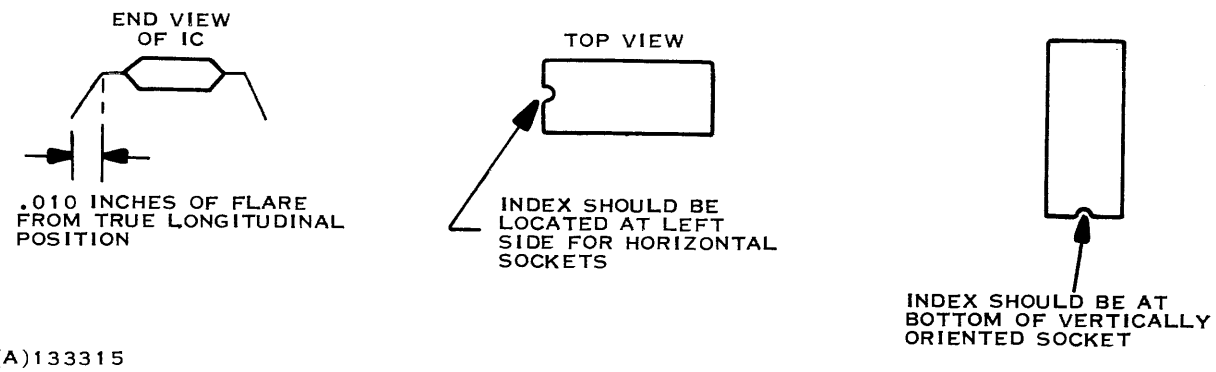


Figure 3-3. IC Installation Diagram

SECTION IV

TROUBLESHOOTING

4.1 GENERAL

This section provides troubleshooting procedures to permit rapid isolation of system failures to a replaceable logic board or cable assembly. Once a suspect subassembly has been identified, the subassembly is removed and replaced in accordance with the corrective maintenance procedures provided in Section III. Additional maintenance information for troubleshooting peripheral equipment is provided in the *Model 990 Computer Family Peripheral Device Field Maintenance Manual.*

4.2 MAINTENANCE PHILOSOPHY

The philosophy for the field maintenance of the 990/10 minicomputer is based on a careful evaluation of the customer-failure report. Troubleshooting makes use of the procedures provided in the system checkout chart in table 4-1 to locate malfunctions and the procedures provided in table 4-2 to isolate the malfunction to the replaceable subassembly (logic card, power supply board, programmer panel/operator panel, cable or plug-in type IC in some cases). Troubleshooting is facilitated by using the field service test equipment described in Section II and the diagrams in Section V.

Once a suspect board is identified, the board is removed in accordance with the procedures provided in Section III and the suspect board is immediately tagged. The replacement board (or other subassembly) is then modified to incorporate the jumper-wire options and any other options originally installed on the faulty board (see instructions in Section III). The replacement board is then installed in the system and the system is retested in accordance with the procedures provided in table 4-1.

4.2.1 DISPOSITION OF FAULTY SUBASSEMBLY. The removed subassembly (less any special-purpose ROMs) should then be packaged for shipment back to the factory using the packing materials removed from the replacement subassembly. In order to avoid damage in shipment, the subassembly should be carefully packed according to the instructions provided in Section VI.

4.3 TROUBLESHOOTING PROCEDURES

A logical approach to troubleshooting a 990/10 minicomputer system is presented in table 4-1. If it is unclear whether the trouble lies in the mainframe or one of the system peripherals, disconnect all peripheral equipment except the ASR 733 and front panel (or the maintenance unit) and check for proper system operation before running the diagnostics in table 4-1. Proper system operation in such a minimum configuration indicates that the trouble lies in one of the peripheral equipments. Once a malfunction is discovered, the fault-isolation procedures in table 4-2 should be used to identify the faulty subassembly.

Table 4-1. 990/10 Minicomputer System Checkout Procedures

Step	Procedure	Normal Indication	If Abnormal
1	Evaluate system problem report and hardware configuration to determine if 990 Maintenance Unit or the unit's programmer panel will be required to troubleshoot the system. If the system is equipped with both an operable 733 ASR data terminal and operable programmer panel, the Maintenance Unit is not required. However, if the system under test does not contain a 733 ASR, the 990 Maintenance Unit is connected to P7 on the system interface board and all programmer panel functions (except ac power control) are transferred to the programmer panel in the maintenance unit (see figure 2-2). If the system contains a 733 ASR but does not contain an operable programmer panel, install the programmer panel from the maintenance unit on P7 of the system interface board as shown in figure 2-3.	–	–
2	If system is off, set key switch on chassis front panel to the LOCK or ON position and observe the POWER LED on the active programmer panel.	POWER LED lights	See step 1 in table 4-2
3	Observe RUN LED on active programmer panel.	RUN LED should light	See step 5 in table 4-2.
4	Set key switch on active programmer panel (either chassis-mounted or panel in the 990 Maintenance Unit) to UNLOCK position.	–	–
5	Press HALT/SIE switch on active programmer panel.	RUN LED extinguishes	See step 4 in table 4-2.
6	If 733 data terminal will be used to load diagnosticts into system, proceed to step 7. If the maintenance unit is hooked to the system, skip to step 8 and continue the procedural steps.	–	–
7	DIAGNOSTIC LOAD PROCEDURE FOR 733 ASR TERMINAL		
	a. Set POWER switch to ON. Install AU10 diagnostic (part no. 945433) into cassette transport (either 1 or 2) and set the PLAYBACK/RECORD switch so that transport containing diagnostic in PLAYBACK mode.	–	–

Table 4-1. 990/10 Minicomputer System Checkout Procedures (Continued)

Step	Procedure	Normal Indication	If Abnormal
	b. Rewind the cassette by momentarily pressing REWIND.	END LED lights and tape motion ceases.	See 733 ASR Operating Manual
	c. Press LOAD/FF to position tape at the beginning.	READY LED lights	–
	d. Setup the terminal's control switches for online operation as follows: • Set ONLINE switch to ONLINE position • Set KEYBOARD, PLAYBACK and PRINTER switches to LINE positions		
	e. Press LOAD switch on active programmer panel.	PLAYBACK ON LED on the 733 lights, cassette tape moves forward in short jerky steps. When load is complete, diagnostic ID is printed out on terminal and program execution begins.	See step 6 in table 4-2
	f. Proceed to step 9 of this table.		
8	DIAGNOSTIC LOAD FROM MAINTENANCE UNIT		
	a. Install AU10 diagnostic cassette (part no. 945433) into cassette transport on maintenance unit.	–	–
	b. Set POWER ON/OFF switch to ON position.	–	–
	c. Press REWIND switch.	Cassette rewinds and halts at clear leader.	See step 6 in table 4-2.
	d. Press LOAD on the maintenance unit.	Tape load begins; tape moves forward continuously until the whole test is loaded. When load is complete, ID is displayed on programmer panel.	

Table 4-1. 990/10 Minicomputer System Checkout Procedures (Continued)

Step	Procedure	Normal Indication	If Abnormal
9	The AU10 diagnostic checks each instruction in the instruction set of the CPU and verifies the real time clock interrupt logic on the interface board. NOTE For a description of the test options available with the AU10 test, refer to the 990 Computer Diagnostic Handbook, P/N 945400-9701.	No error message printout (733) or error number display on programmer panel. (Error message numbers are displayed in the right byte of the DATA LEDs and the left byte is forced to FF_{16} when using programmer panel for error message displays.)	Reference error message descriptions in diagnostics handbook; see steps 7 through 10 in table 4-2.
10	If the system has mapping, repeat step 7 or step 8, as appropriate, using the MAPTST diagnostic program identified in table 2-2. P/N 945441.	Program runs to completion with no error messages printed.	Replace AU2B board.
11	Rewind cassette tape by pressing REWIND on 733 ASR or 990 maintenance unit and repeat diagnostic load procedures for the RAM10 diagnostic test (part no. 945439) which checks each memory location as defined at the beginning of the test. (See diagnostics handbook.)	No errors.	Refer to diagnostics handbook for error message interpretation and see steps 8, 9, 11, 12, and 13.
12	Rewind cassette and install one of the other diagnostic tests identified in table 2-2 as dictated by the problem report. NOTE A collection of loop programs which may be entered from the programmer panel to continuously read or write to/from selected memory locations is provided in Appendix E.	No errors.	See table 4-2.

Table 4-2. 990/10 Minicomputer System Fault Isolation Procedures

Step	Abnormal Indication	Probable Cause	Corrective Action
1	POWER LED does not light and cooling fans inoperative when key switch on front panel is set to LOCK or ON position.	Loss of ac power at the power outlet.	Using multimeter, measure ac voltage at outlet. If voltage is normal (115 Vac, 230 Vac, or 100 Vac as marked on the rear of the chassis next to the power cable outlet), proceed to next substep.
		Blown fuse due to temporary overvoltage condition on ac power line.	Disconnect ac power cord from ac outlet. Remove fuse 1F1 (located at rear of chassis) and perform continuity check using ohmmeter. Replace fuse (if infinite resistance is indicated) and apply power to the system again. If fuse continues to blow, proceed to step 2. If fuse was not blown when first checked, proceed to next substep.
		Open circuit condition in ac distribution system.	UNPLUG AC POWER CORD FROM AC OUTLET. Set key switch on front panel of chassis to LOCK or ON position. Remove rear access cover and perform following resistance checks:
		Faulty power cord.	1. Measure resistance between hot prong of power cord and the black lead of the power cord which connects to pin 2 of the fuse holder 1XF1 (should be 0 ohms). If open, replace power cable. If normal, check resistance between neutral prong of power plug and white lead of power cord which connects to pin 5 of the ac line filter 1FL1. If open circuit is indicated, replace power cord.
		Faulty ac microswitch on rear of operator panel; faulty cam on key switch; loose terminal or broken wire between fuse holder and microswitch or between line filter and ac microswitch.	2. Measure dc resistance between fuse holder (pin 1 or 2) and pin 3 of line filter. If 0 ohms, proceed to next measurement. If infinite or high resistance, remove side access cover (across from logic board side of chassis) and check continuity between the common and normally-open terminals on the ac switch 1A4S4 located directly behind the key switch on the front panel. (The two terminals are the leftmost two terminals on the leftmost switch as viewed from the rear of the panel.) If the switch is open, check the switch cam operation to ensure that the microswitch is being actuated. If not, replace front panel assembly. If the cam is functioning properly, replace 1A4S1. If the switch resistance is normal (0 ohms), use ohmmeter to locate break in wiring between the fuse holder 1XF1 and the N.O. terminal of the switch 1A4S1 or between the common terminal of 1A4S1 and pin 3 of the line filter. If resistance between fuse holder terminal and pin 3 of line filter is normal, perform next check.
		Open circuit in line filter.	3. Measure dc resistance between line filter pins 1 and 3 (0 ohms) and between 2 and 5 (0 ohms). Replace filter if either path is open.
		Loose terminal or break in wiring between line filter and terminal strip.	4. Measure dc resistance between pin 1 of line filter and terminal 1 on terminal strip and between pin 2 of line filter and terminal 2 of terminal strip. If either reading indicates open circuit, repair break in wiring or loose terminal.

Table 4-2. 990/10 Minicomputer System Fault Isolation Procedures (Continued)

Step	Abnormal Indication	Probable Cause	Corrective Action
2	Fuse continues to blow when replaced.	Shorted winding on one of the blower motors or shorted surge voltage protector.	TURN OFF AC POWER TO CHASSIS. Disconnect 1A2P1 (purple plug on the end of the ac power converter board). Install new fuse and retest system. If fuse does not blow, proceed to next substep. If fuse blows, remove the hot lead of each blower motor from terminal 1 on the terminal strip (end terminal on the right), one motor at a time, and measure the dc resistance of the motor (normally between 20 and 30 ohms). Replace any motor with obvious shorted windings. If all motors test good, measure dc resistance between terminals 1 and 2 of terminal block. If less than 5 ohms, replace surge voltage protector 1C2. If all resistance checks are normal, disconnect hot leads of all blower motors and replace one at a time. After each lead is reconnected, turn on ac power to system. Then check fuse. Repeat for each motor until fuse blows. Replace last motor connected when fuse blows.
		Short circuit condition on ac power converter board (1A2).	TURN OFF AC POWER TO THE CHASSIS. Remove all connector plugs from ac power converter board and measure dc resistance between pins 1 and 2 of J1 (purple jack) using R × 1K scale on ohmmeter. Should be approximately 5K ohms in one direction and a minimum of 100K when the leads are reversed. If abnormal, replace ac power converter board. Then proceed to next substep to ensure that a faulty main power supply or standby power supply board did not result in failure of the converter board.
		Short circuit condition on main power supply board (1A3).	Using R × 1K scale on ohmmeter, measure input resistance to main power supply by measuring resistance between pins 1 and 2 of 1A2P3 (white plug removed from ac converter board). Normal resistance is approximately 4.5K in one direction and 11K ohms in the reverse direction. If lower resistance is measured, replace main power supply board. If normal, measure resistance between pins 3 and 4 of the same plug (1A2P3) using the R × 1K scale. Normal values are approximately 2K in one direction and 20K in the reverse direction. If resistance is much lower than normal values, replace main power supply board. If readings are normal, proceed to the next substep.
		Short circuit condition on input side of standby power supply board 1A6 (if used).	Measure dc resistance between pins 2 and 4 of 1A2P2 (red plug removed from ac power converter board) using R × 1K scale on ohmmeter. Normal reading is approximately 4K and 10K (reverse direction). If short circuit is indicated, replace standby power supply board. If standby option is not used, locate and correct short-circuit condition in wiring harness. If resistance is normal (above values if standby supply is used or infinity if supply is not used), proceed to next substep.
		Leaking filter capacitor 1C1.	Measure dc resistance of capacitor 1C1 using RX100 scale by measuring between pins 1 and 3 or connector plug 1A2P2 (red plug removed from ac power converter board). Normal indication is a near-zero initial reading with a gradual movement of the meter pointer toward the infinity side of the scale. If resistance value is low or if capacitor shows signs of leakage, replace capacitor.
			Reconnect the plugs originally removed from ac power converter board. The plugs are keyed such that the plugs will mate in only one way.

Table 4-2. 990/10 Minicomputer System Fault Isolation Procedures (Continued)

Step	Abnormal Indication	Probable Cause	Corrective Action
2	(Continued)	Faulty main power supply board or ac power converter board under full load conditions.	If all static dc resistance tests are normal, swap out main power supply board first. If problem is still present, swap out ac power converter board and ICs if problem continues.
3	POWER LED on front panel fails to light when key switch is set to LOCK or ON position; cooling fans function normally; system inoperative.	Faulty main power supply board 1A3 or low output voltage from ac converter board 1A2.	Remove and replace main power supply board. If problem persists, remove 1A3P1 from main power supply and measure dc voltage between pins 1 and 2 (pin 1 is POSITIVE lead). Set key switch on chassis front panel to OFF position. If less than 130 Vdc, replace ac power converter and/or capacitor 1C1. If problem still persists, proceed to next substep.
		Short circuit on one of the boards in the chassis.	Remove all logic boards from the chassis (as each board is removed, ensure that the board location chart on the top of the computer chassis accurately reflects the boards installed in each slot). Then, install known good 990/4 microcomputer board (or CRU buffer board if problem exists in expansion chassis) in slot 1. If problem is solved, install original boards in remaining slots (one at a time) and retest the system as each board is installed. CAUTION Always turn off power to the chassis when removing and replacing logic boards to avoid damage to the boards due to temporary misalignment of pins. If all original boards are reinstalled (except board in slot 1) and system functions normally, the original board in slot 1 is faulty. If the problem returns as one of the other original boards is installed, the last board installed before reappearance of the power failure is the faulty board and should be replaced. Reinstall all other original boards and retest system.
4	Unable to get programmer panel into halt mode; same symptom appears when programmer panel from 990 Maintenance Unit is substituted for chassis panel. NOTE If symptom appears only with chassis-mounted panel, remove and replace panel.	Custom ROM loader installed on system interface board.	Replace custom ROMs with one of the standard ROM loader configurations (see figures 1-12 and 1-13).
		Faulty ROM memory section or faulty load generation logic on one of CPU boards.	Replace system interface board with known good board (ensure that all jumper options and ROM loaders are properly installed on the replacement board). If trouble persists, replace processor (AU1) board.

Table 4-2. 990/10 Minicomputer System Fault Isolation Procedures

Step	Abnormal Indication	Probable Cause	Corrective Action
5	System fails to come up in RUN mode when power is applied to the chassis.	Loss of power up clear signal from main power supply board or logic stage on system interface board.	Use voltmeter to check that TLPRES– goes high when power is applied (P1-13). If signal goes high, replace system interface (AU2) board; if not, replace main power supply board.
6	Unable to load diagnostics from Maintenance Unit; FAULT LED lights when LOAD is initiated.	Self-test failure due to faulty self-test ROMs, memory or processor error.	Replace the loader ROMs on the system interface (AU2 or AU2B) board (see figures 1-12 and 1-13). If problem persists, replace system interface board (ensure that replacement board is properly configured and that all custom ROMs from faulty board have been transferred to replacement board. If problem persists, proceed to next substep.
		Loss of memory voltage(s)	If standby power supply option is not installed, ensure that standby jumper plug is installed on 1A3J3. Using multimeter, observe the following memory voltages at any connector slot in backplane (use extender board if available): • P2-71: -5 MEM • P2-73: +5 MEM • P2-75: +12 MEM If standby supply option is not used, replace main power supply board if any of these voltages are abnormal. If standby supply is used, replace standby supply if the voltages are abnormal. (-5 MEM may also be due to failure on main power supply board.)
7	Failure of one or more instructions to execute when running the AU10 diagnostic program.	Faulty CPU board.	Replace processor (AU1) board and re-run diagnostic. If trouble persists, replace interface (AU2) board and re-run diagnostic (ensure that all ROMs are installed on the replacement board).
8	RAM10 diagnostic printout indicates single bit error at one or more memory location(s) in 4K RAM or 16K RAM address space on memory board. NOTE See appendix E for loop program which may be entered from the programmer panel to loop on a selected address or band of addresses.	Faulty RAM memory chip	Remove and replace TMS 4050 (TMS 4060 for ECC 8K memory or TMS 4116 for ECC 48K memory) memory chip corresponding to bit position. If problem persists after replacement of memory chip, remove and replace appropriate memory board after carefully implementing all jumper options and address switch settings on the replacement board (see Section I for option descriptions).

Table 4-2. 990/10 Minicomputer System Fault Isolation Procedures (Continued)

Step	Abnormal Indication	Probable Cause	Corrective Action
9	Memory failure on 4K RAM or 16K RAM address space on 990/10 CPU boards. Boards replaced and problems persists.	One of the expansion memory boards is operating with the same starting address due to an improperly selected starting address or faulty address decode on the board.	Check the starting address associated with each memory expansion board or EPROM memory module in the chassis in accordance with the appropriate table in section I. If starting address for each board is properly set up, replace each memory board and repeat diagnostic. Last board replaced when diagnostic board executes properly is the faulty board. Reinstall the other board and repeat the test to ensure that only one problem exists in the system.
10	Real time clock interrupt	Interrupt jumper on interface board not properly connected.	Check jumper connections for desired interrupt levels. If jumper connections are satisfactory, replace the interface board.
		Loss of 120 Hz pulses from power supply.	Remove and replace main power supply board and repeat test. If problem persists, replace ac power converter board. NOTE Faulty subassembly is the last unit replaced before normal test results are obtained. Reinstall other subassembles and repeat test to ensure that only one faulty subassembly exists on the system.
11	Low order memory banks on memory expansion board inoperative, high order banks normal.	Improperly set starting address switches on RAM memory board.	Refer to data in section I for starting address switch positions appropriate for the RAM boards involved.
12	High order memory address space on memory expansion board inoperative, low order banks functioning normally.	Memory size jumpers improperly installed.	Use data in section I to check that the memory size jumpers on the RAM memory boards correspond to the amount of memory implemented on the board. If properly set, replace memory expansion board.
13	Single bit failure in one or more addresses in the memory expansion board address space.	Faulty RAM memory chip	Remove and replace RAM memory chip in memory bank corresponding to faulty address at bit position corresponding to faulty data bit. If problem persists, replace RAM memory ICs in same column in the remaining memory banks. If problem still persists, remove and replace memory expansion board.
14	Memory failure on address space reserved for EPROM memory module.	Jumpers not properly installed on board or starting address for EPROM board not properly set, faulty EPROM board.	Refer to section I data and ensure that all board options are properly installed. If so, replace the board. CAUTION All EPROM chips from the faulty board must be transferred to the exact same socket locations on the replacement board. These chips contain custom software programs which will not function if any of the chips are installed out of their original pattern.

Table 4-2. 990/10 Minicomputer System Fault Isolation Procedures (Continued)

Step	Abnormal Indication	Probable Cause	Corrective Action
15	One peripheral device within main chassis is inoperative; all other peripherals function normally	Peripheral's interface board installed in wrong slot (see figure 1-19 for standard configuration recognized by software).	Move interface board to correct location. If properly located, proceed to next substep.
		Interrupt not wired properly on backpanel board.	Remove first five logic boards in chassis and ensure that jumper is installed correctly (see figure 1-21). If so, replace boards and proceed to next substep.
		Improperly seated interface board or loose cable connector.	Check interface board and associated interface cable connectors for snug fit.
		Faulty interface board or jumper options improperly installed.	If device is 733 ASR, 733 KSR or line printer, see figure 1-25 and verify proper jumper connections.
			At this point, refer to the 990 Computer Peripherals Field Maintenance Manual for additional fault isolation procedures.
16	All peripherals implemented within one expansion chassis are inoperative; peripherals implemented in other expansion chassis function properly.	If POWER LED on chassis is lit and fans are functioning properly, the CRU buffer board is most likely at fault. NOTE If POWER LED and blower motors in expansion chassis are inoperative, see steps 1 and 2 at the beginning of this procedure.	Remove CRU buffer board from chassis and check to see that the jumper plug (P4) on the board is inserted in the slot corresponding to the correct chassis number as follows: CRU EXPANDER PORT / CHASSIS NO. P3 / 1 P4 / 2 P5 / 3 P6 / 4 P7 / 5 P8 / 6 P9 / 7
		Faulty CRU expander board in main chassis or faulty interface cable between CRU expander board in main chassis and CRU buffer board in expansion chassis.	If the jumper plug is properly installed, replace the CRU buffer board and set up the jumper plug (as described above) on the replacement board. If the problem persists, replace the interface cable between the CRU expander board in the main chassis and the CRU board in the expansion chassis and/or CRU expansion board in the main chassis. If problem persists, preceed to next substep.
		Interrupt jumpers not properly installed on expansion chassis backpanel.	Refer to figures 1-20 and 1-21. Check interrupt jumpers in chassis backpanel board to ensure that the interrupt assignments listed on the chassis map (top of chassis) are correctly implemented.
17	One or more function keys on chassis-mounted programmer panel inoperative; programmer panel on Maintenance Unit functions properly.	Defective switch block on programmer panel.	Remove and replace chassis-mounted panel in accordance with the instructions in Section III.

Table 4-2. 990/10 Minicomputer System Fault Isolation Procedures (Continued)

Step	Abnormal Indication	Probable Cause	Corrective Action
18	One or more function keys inoperative on chassis-mounted programmer panel; same problem exists with programmer panel on maintenance unit.	Faulty panel software ROM on system interface board.	Install new ROM loader ICs in accordance with the information provided in figure 1-13. If problem persists, replace system interface board. NOTE Ensure that all jumper options on the replace board match the options installed on the faulty board and that all custom ROMs have been transferred to the replacement board.

SECTION V

TROUBLESHOOTING DIAGRAMS

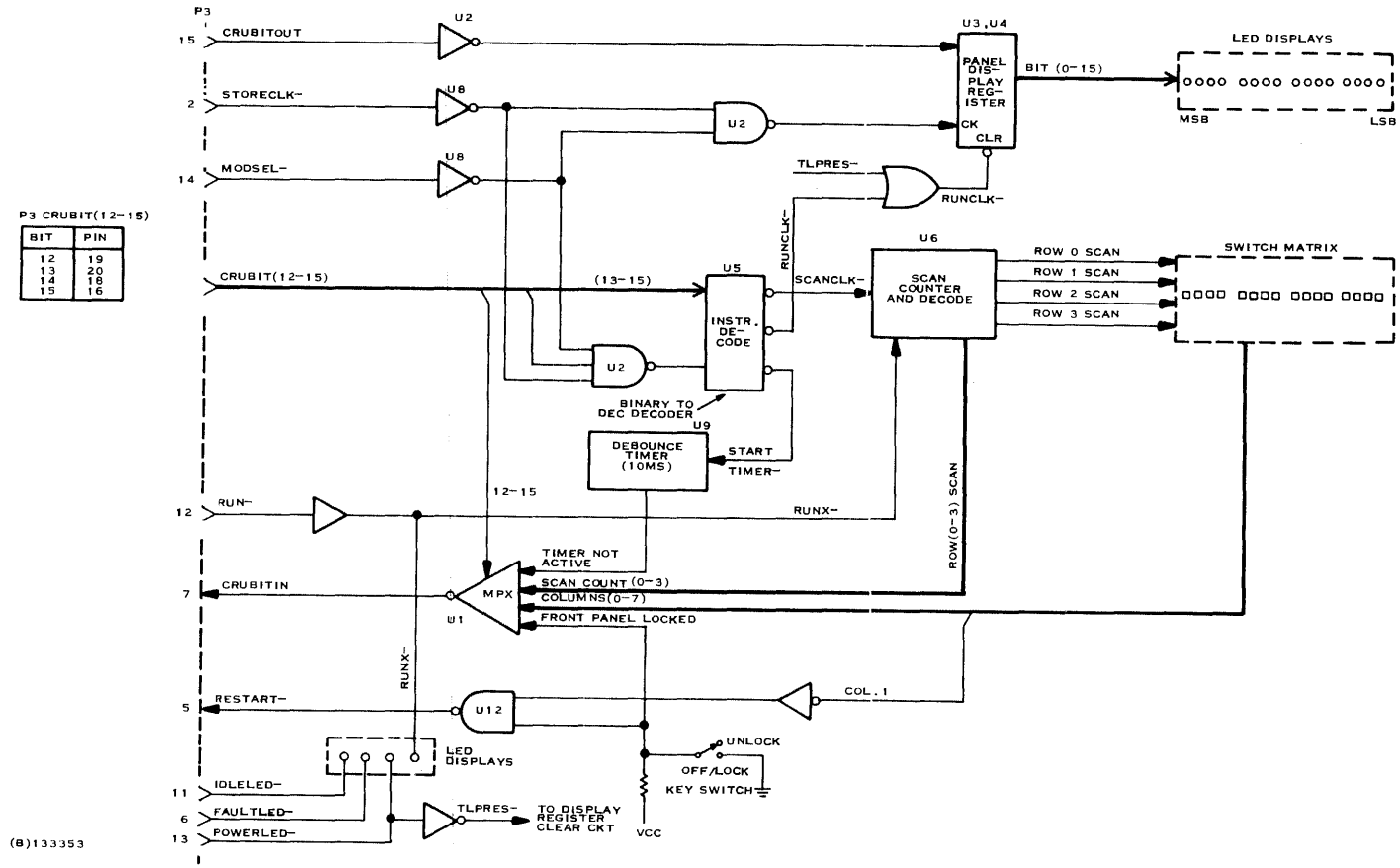
5.1 GENERAL

This section contains a collection of chassis wiring diagrams, backpanel schematics and logic board block diagrams (complete with interface pin assignments) useful in performing field-level maintenance. An index to the drawings in this section is provided in table 5-1.

NOTE

Logic diagrams, IC schematics and power supply schematic diagrams are available in the *990 Computer Family Maintenance Drawings Manual.*

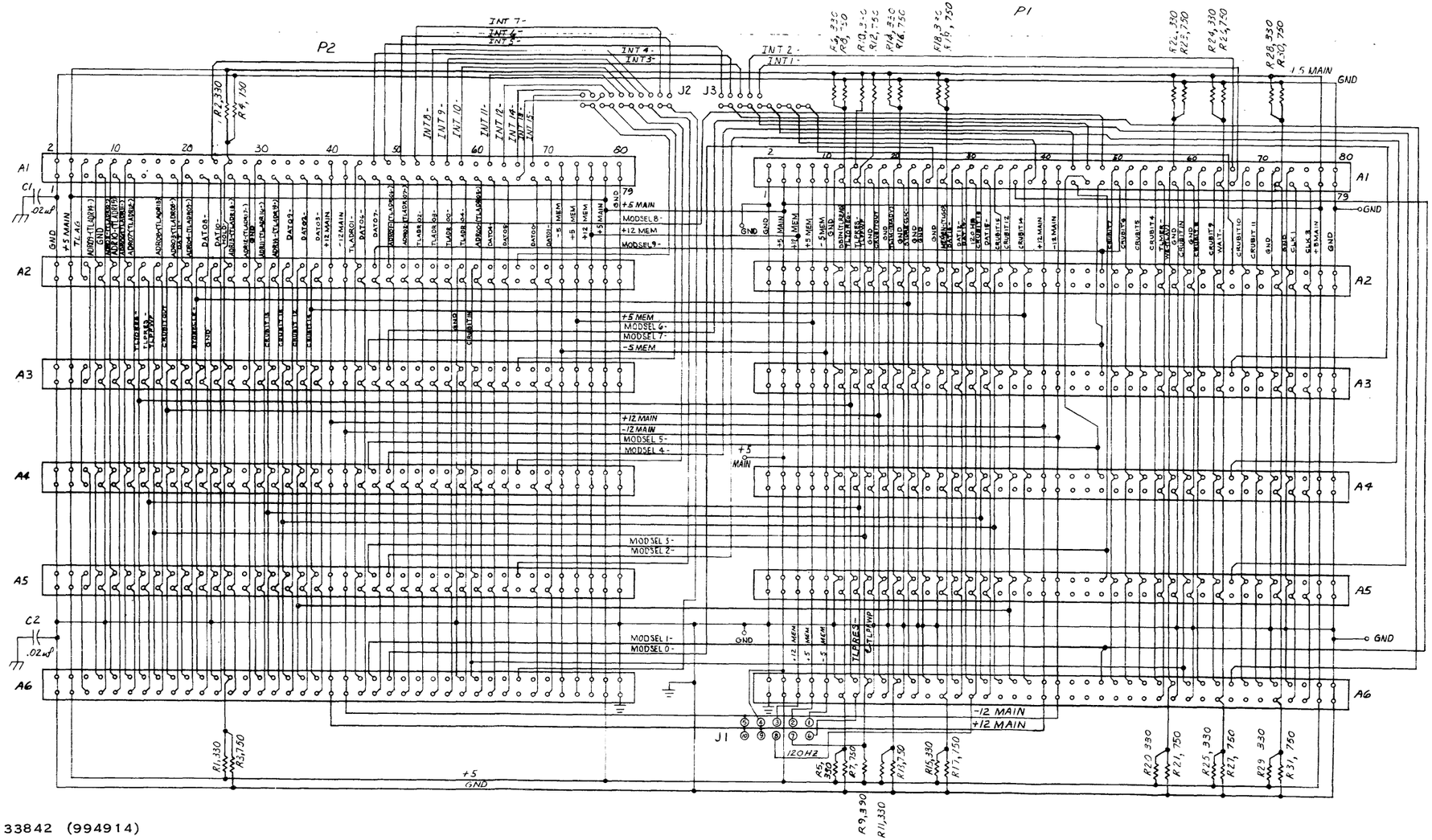
Table 5-1. Diagram Index



P3 CRUBIT(12-15)

BIT	PIN
12	19
13	20
14	18
15	16

Figure 5-1. Programmer Panel Block Diagram



(B)133842 (994914)

Figure 5-2. 6-Slot Chassis Backpanel Schematic

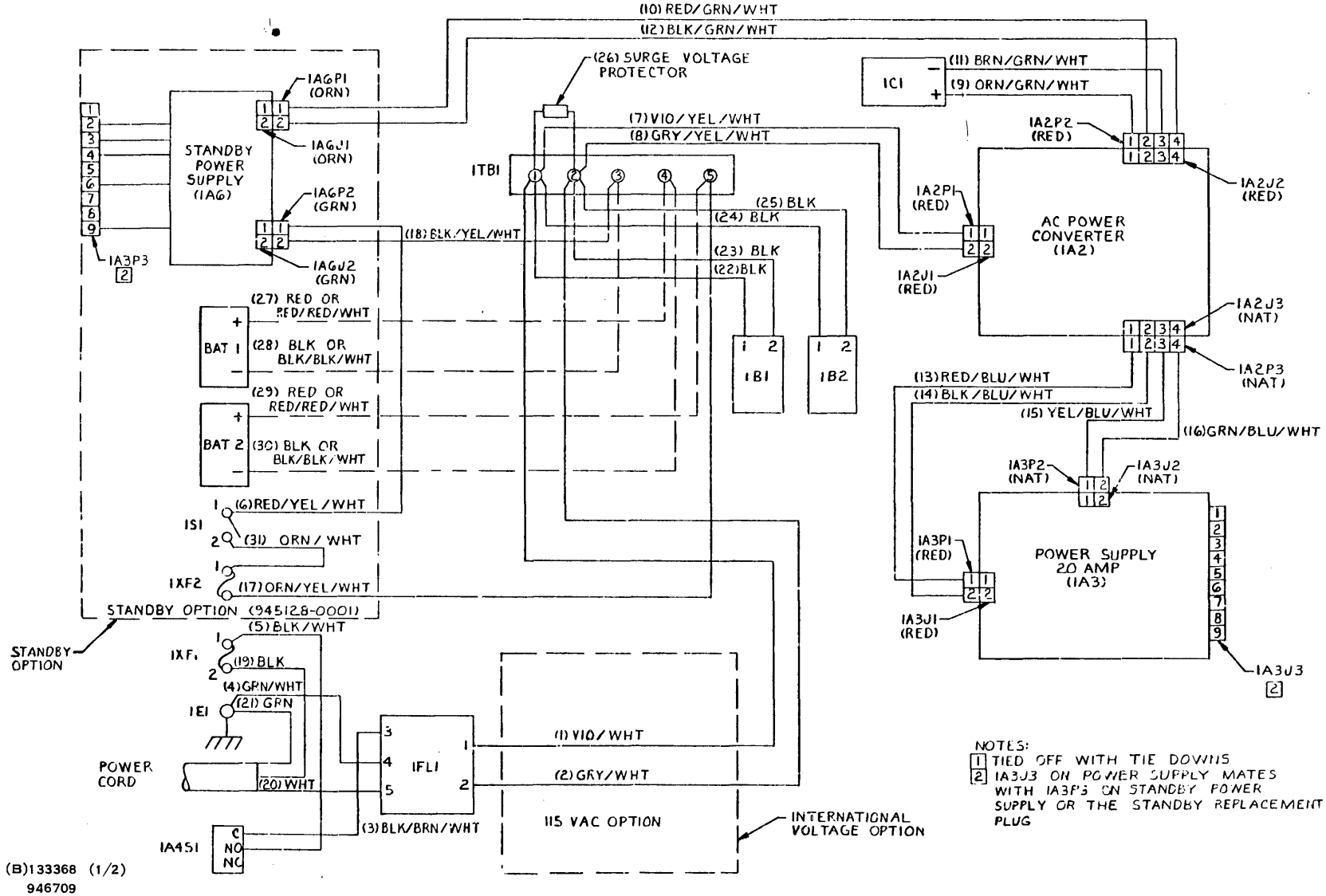
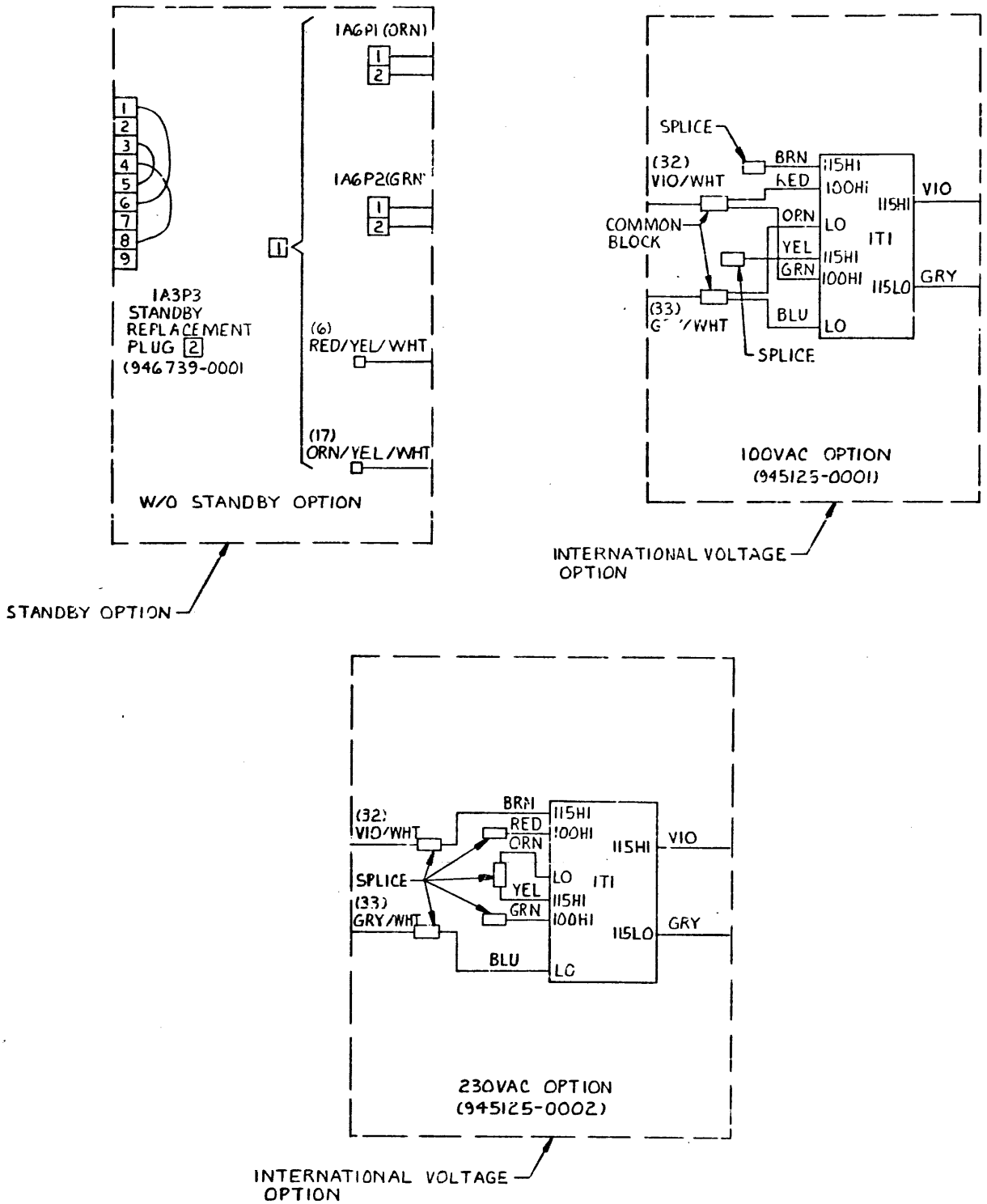
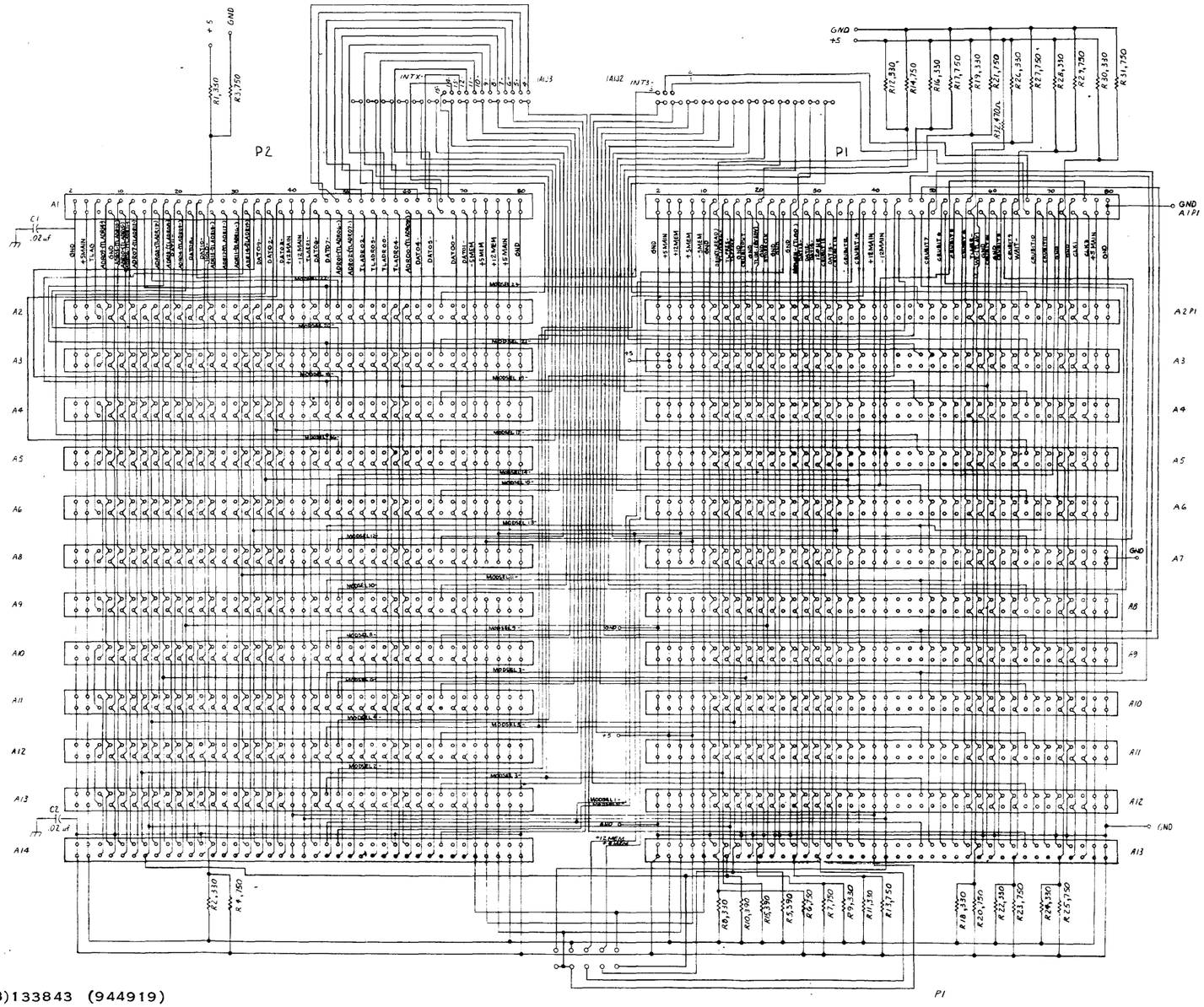


Figure 5-3. 6-Slot Chassis Wiring Diagram (Sheet 1 of 2)



(B)133368 (2/2)
946709

Figure 5-3. 6-Slot Chassis Wiring Diagram (Sheet 2 of 2)



(B)133843 (944919)

Figure 5-4. 13-Slot Chassis Backpanel Schematic

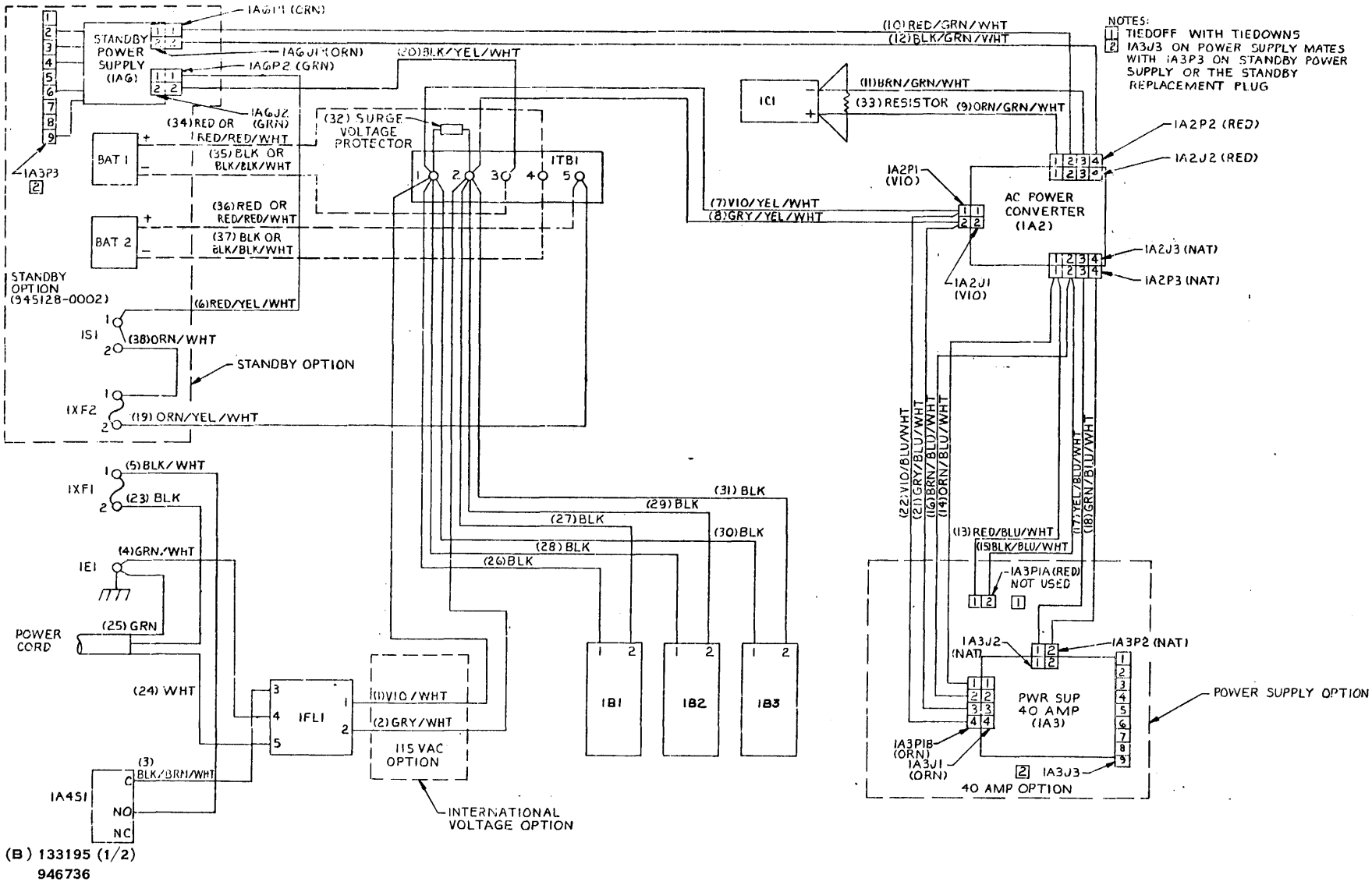
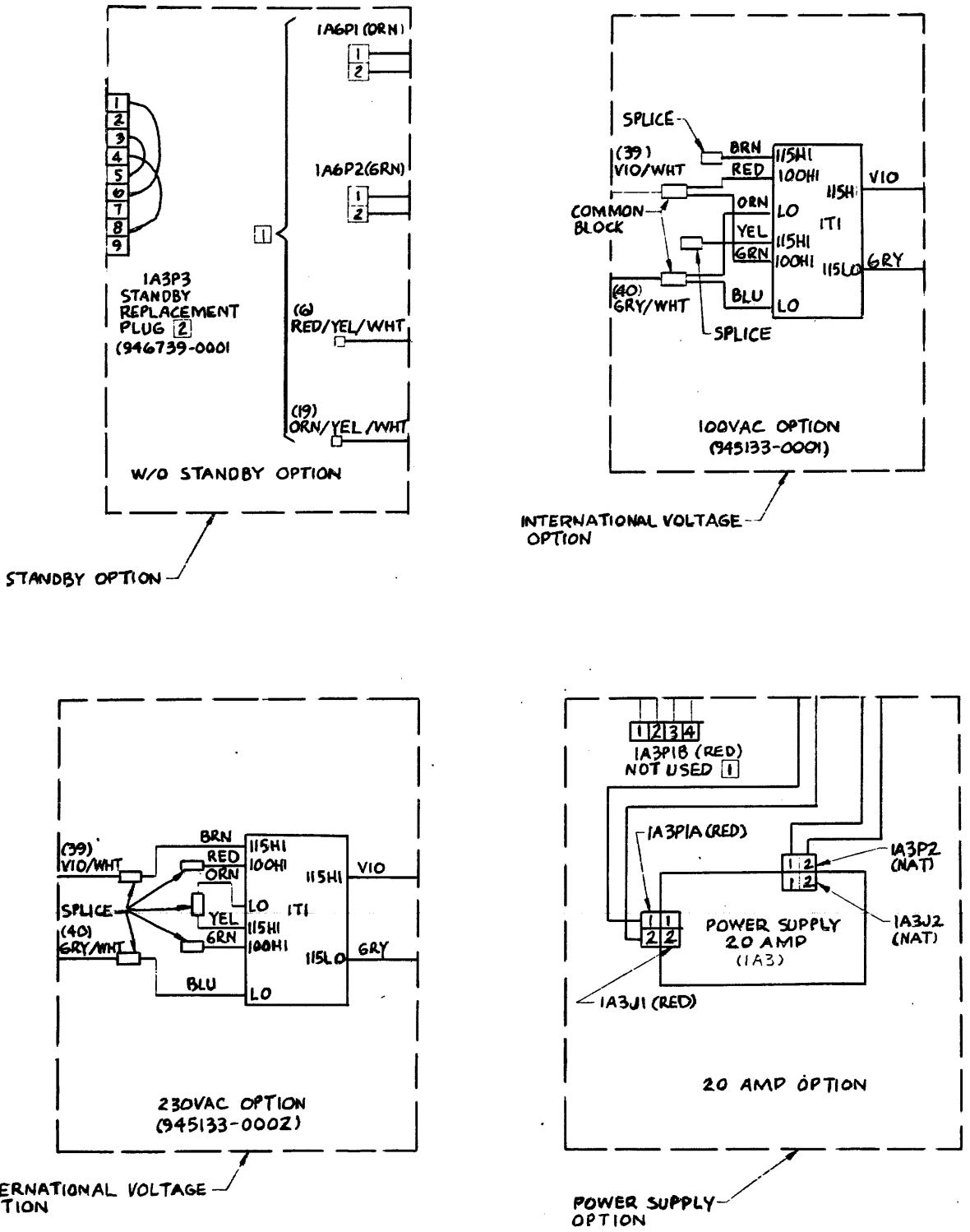


Figure 5-5. 13-Slot Chassis Wiring Diagram (Sheet 1 of 2)



(B) 133195 (2/2)
946736

Figure 5-5. 13-slot Chassis Wiring Diagram (Sheet 2 of 2)

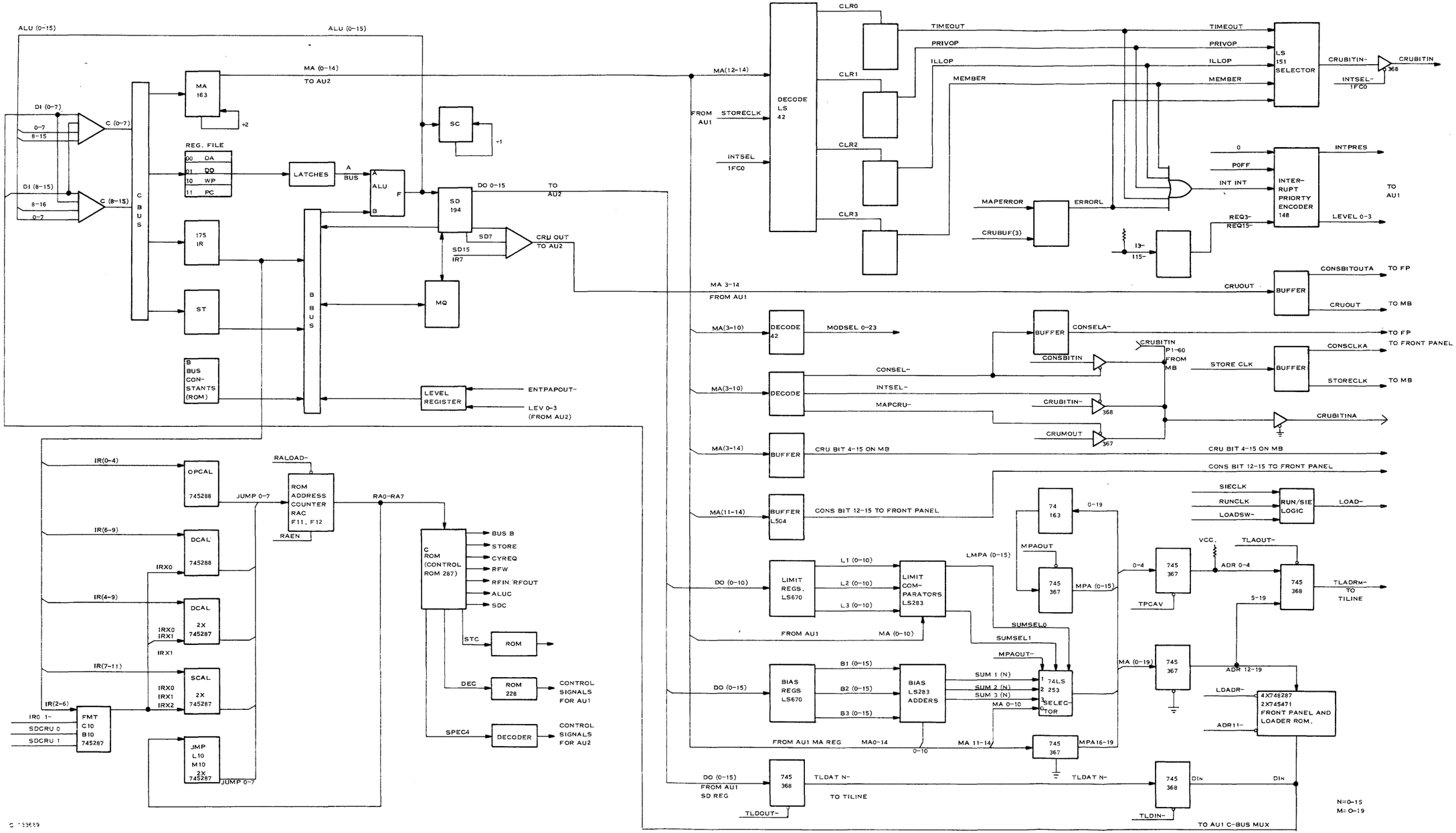


Figure 5-6. 990/10 CPU Board Block Diagram

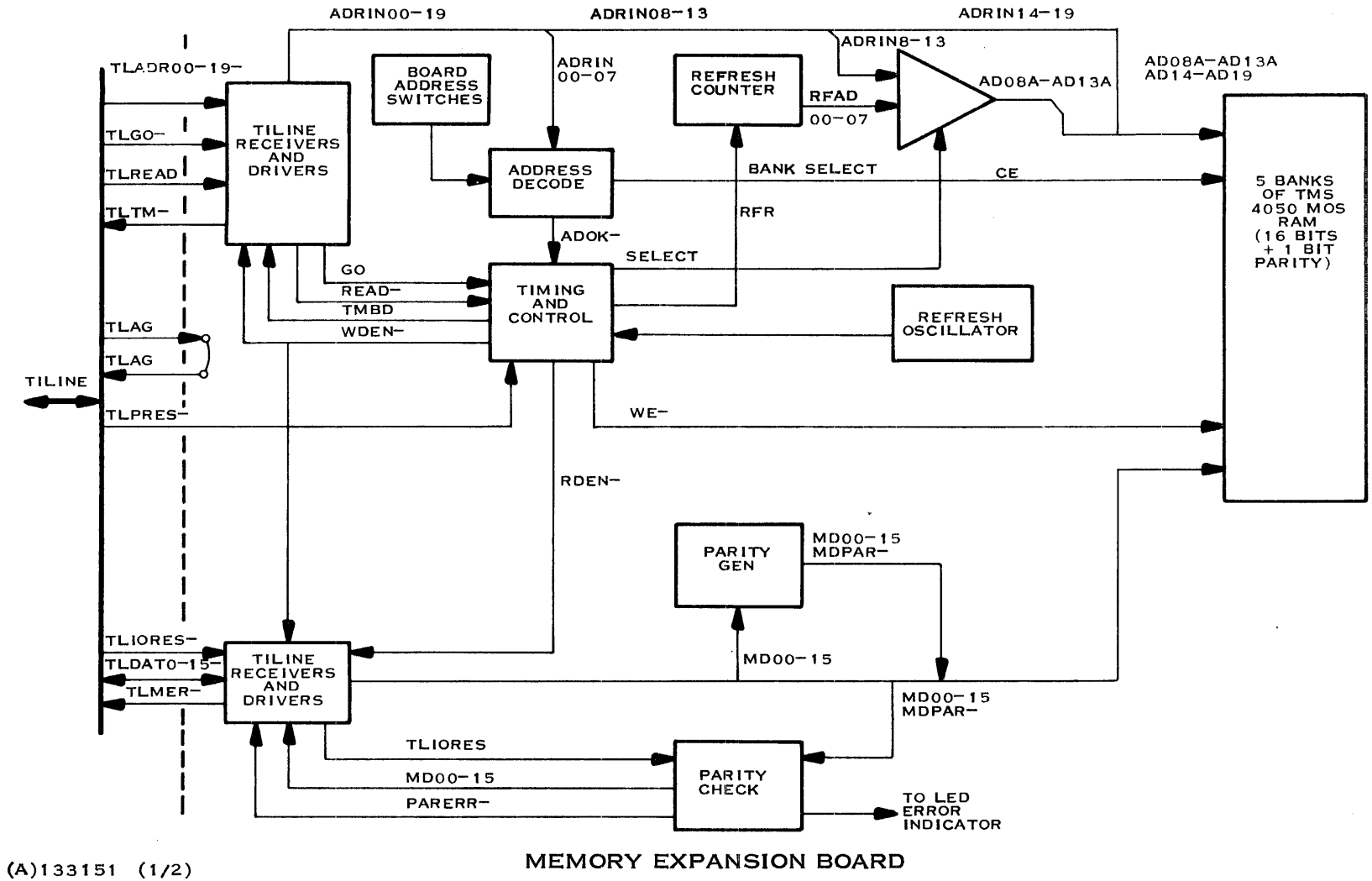


Figure 5-7. ECC 16KB Memory Expansion Board Block Diagram (Sheet 1 of 2)

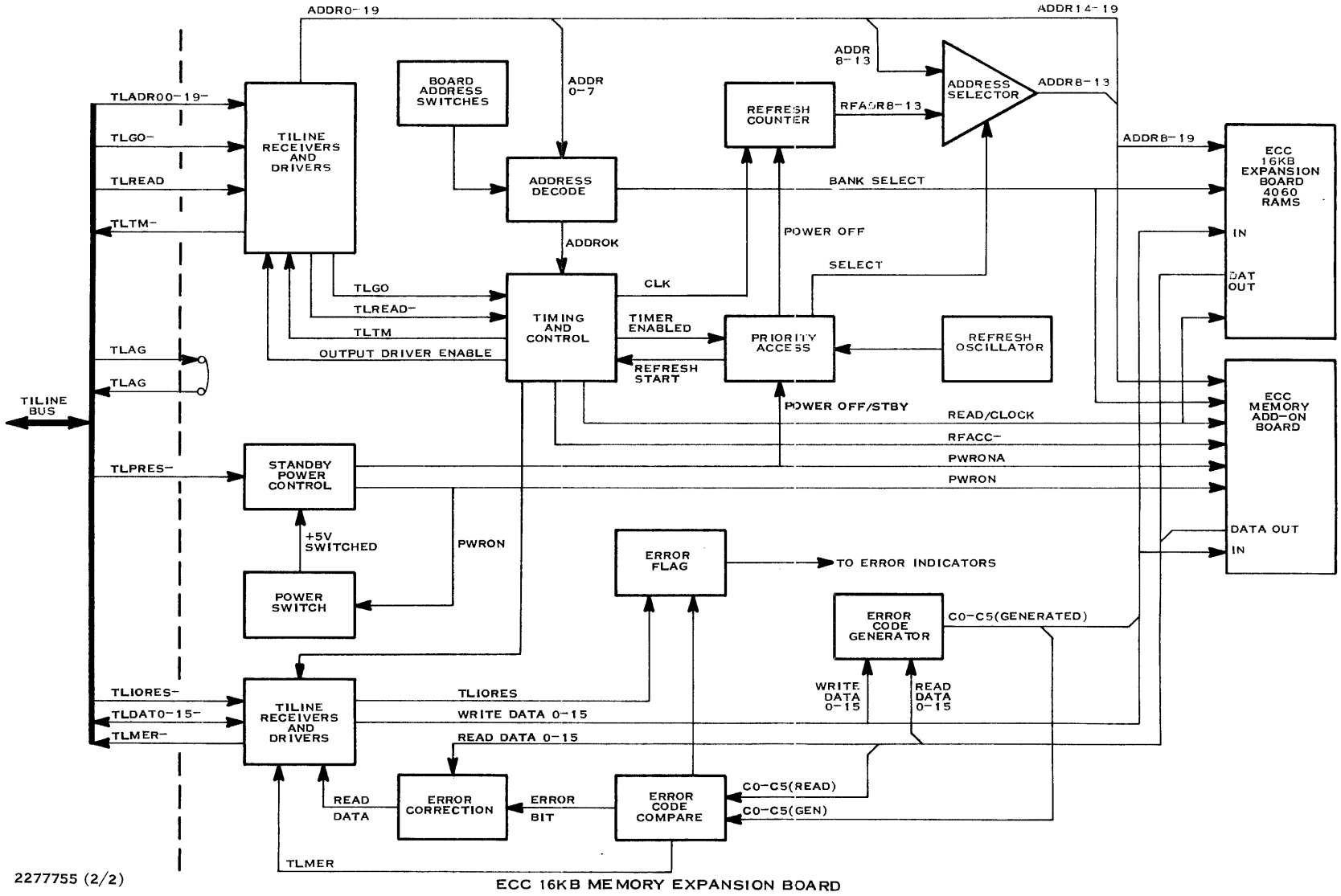


Figure 5-7. ECC 16KB Memory Expansion Board Block Diagram (Sheet 2 of 2)

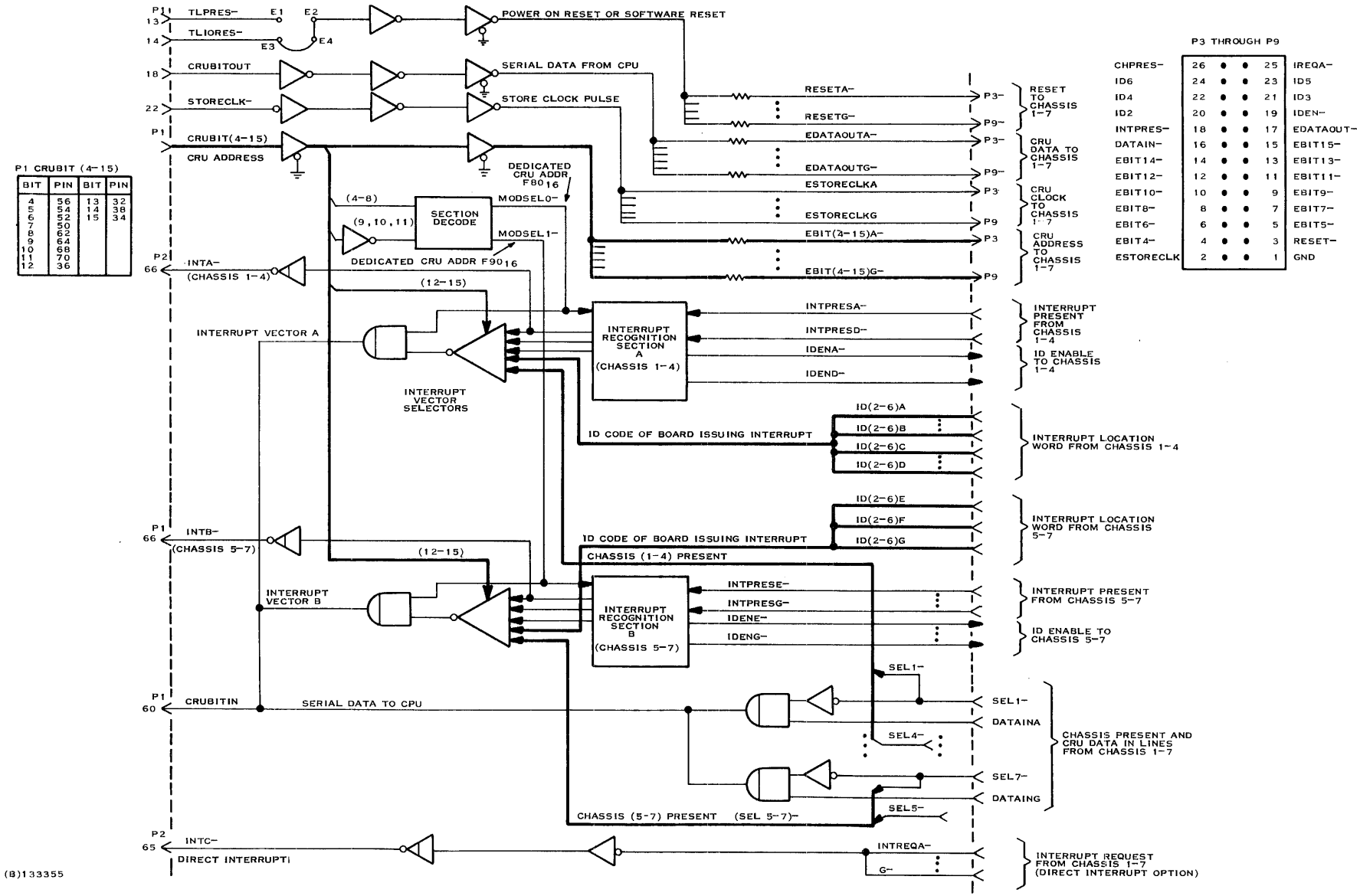
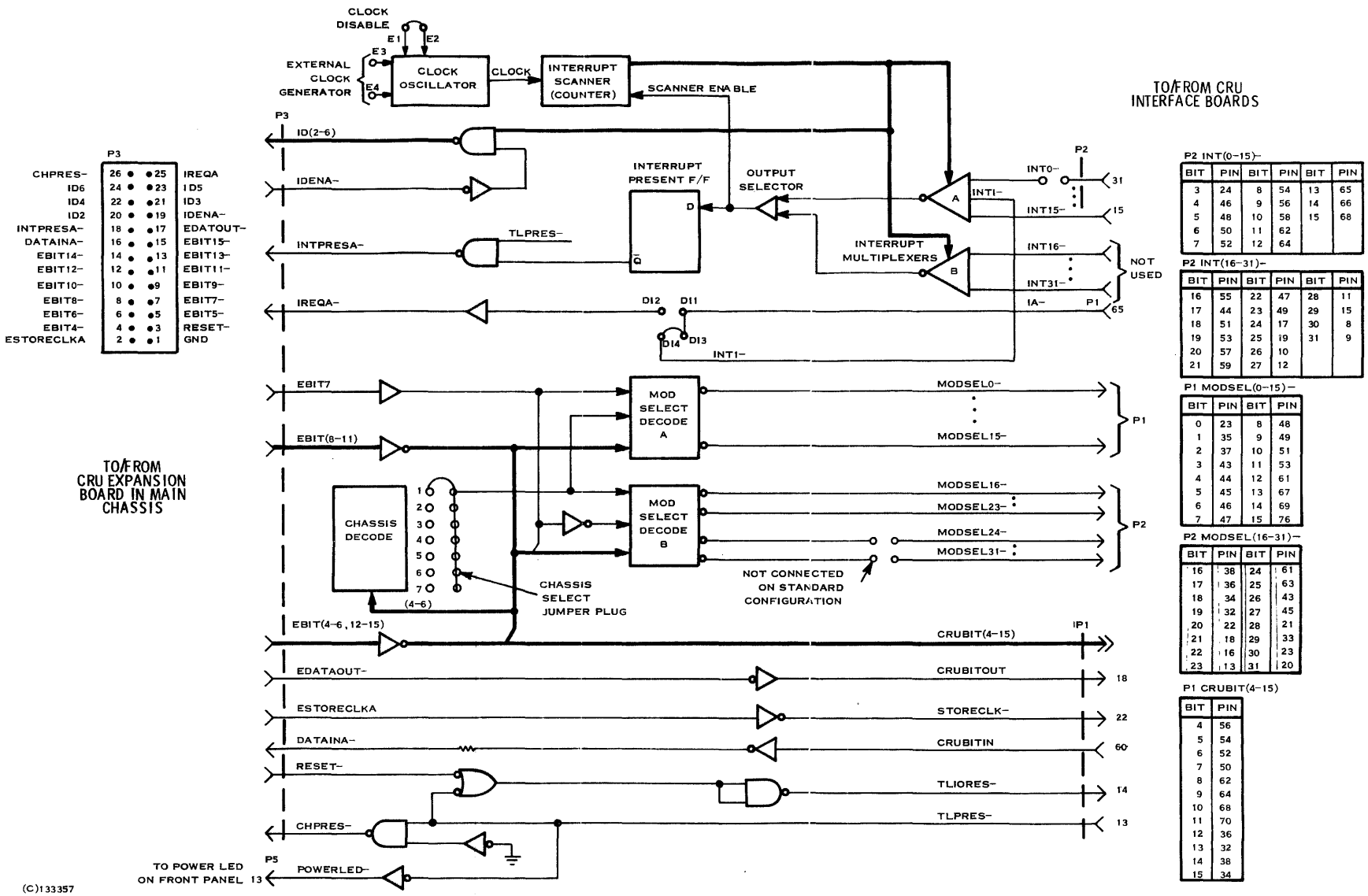


Figure 5-8. CRU Expander Board Block Diagram



P2 INT(0-15)-

BIT	PIN	BIT	PIN	BIT	PIN
3	24	8	54	13	65
4	46	9	56	14	66
5	48	10	58	15	68
6	50	11	62		
7	52	12	64		

P2 INT(16-31)-

BIT	PIN	BIT	PIN	BIT	PIN
16	55	22	47	28	11
17	44	23	49	29	15
18	51	24	17	30	8
19	53	25	19	31	9
20	57	26	10		
21	59	27	12		

P1 MODSEL(0-15)-

BIT	PIN	BIT	PIN
0	23	8	48
1	35	9	49
2	37	10	51
3	43	11	53
4	44	12	61
5	45	13	67
6	46	14	69
7	47	15	76

P2 MODSEL(16-31)-

BIT	PIN	BIT	PIN
16	38	24	61
17	36	25	63
18	34	26	43
19	32	27	45
20	22	28	21
21	18	29	33
22	16	30	23
23	13	31	20

P1 CRUBIT(4-15)

BIT	PIN
4	56
5	54
6	52
7	50
8	62
9	64
10	68
11	70
12	36
13	32
14	38
15	34

Figure 5-9. CRU Buffer Board Block Diagram

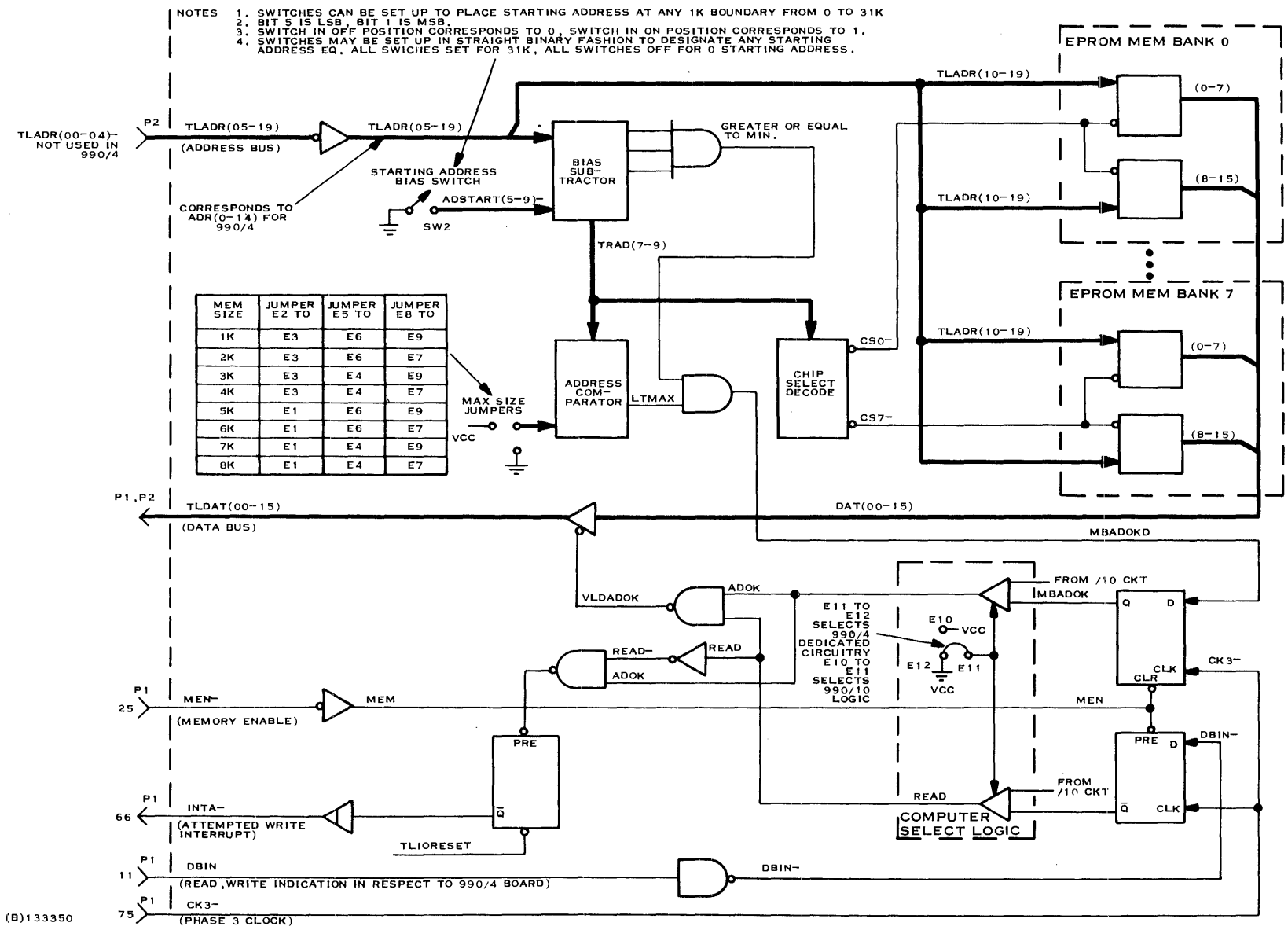


Figure 5-10. EPROM Memory Module Block Diagram

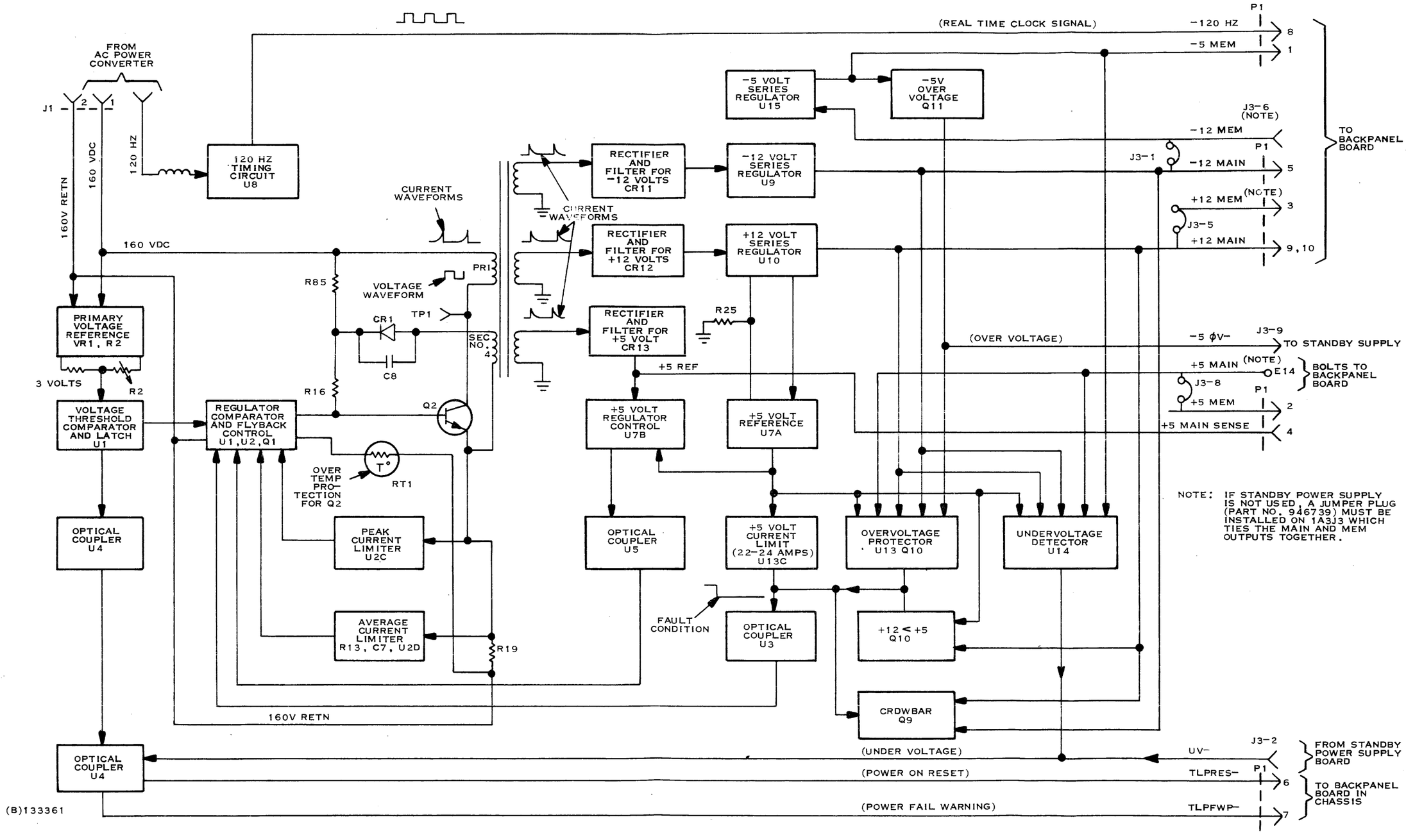


Figure 5-11. Main Power Supply Block Diagram

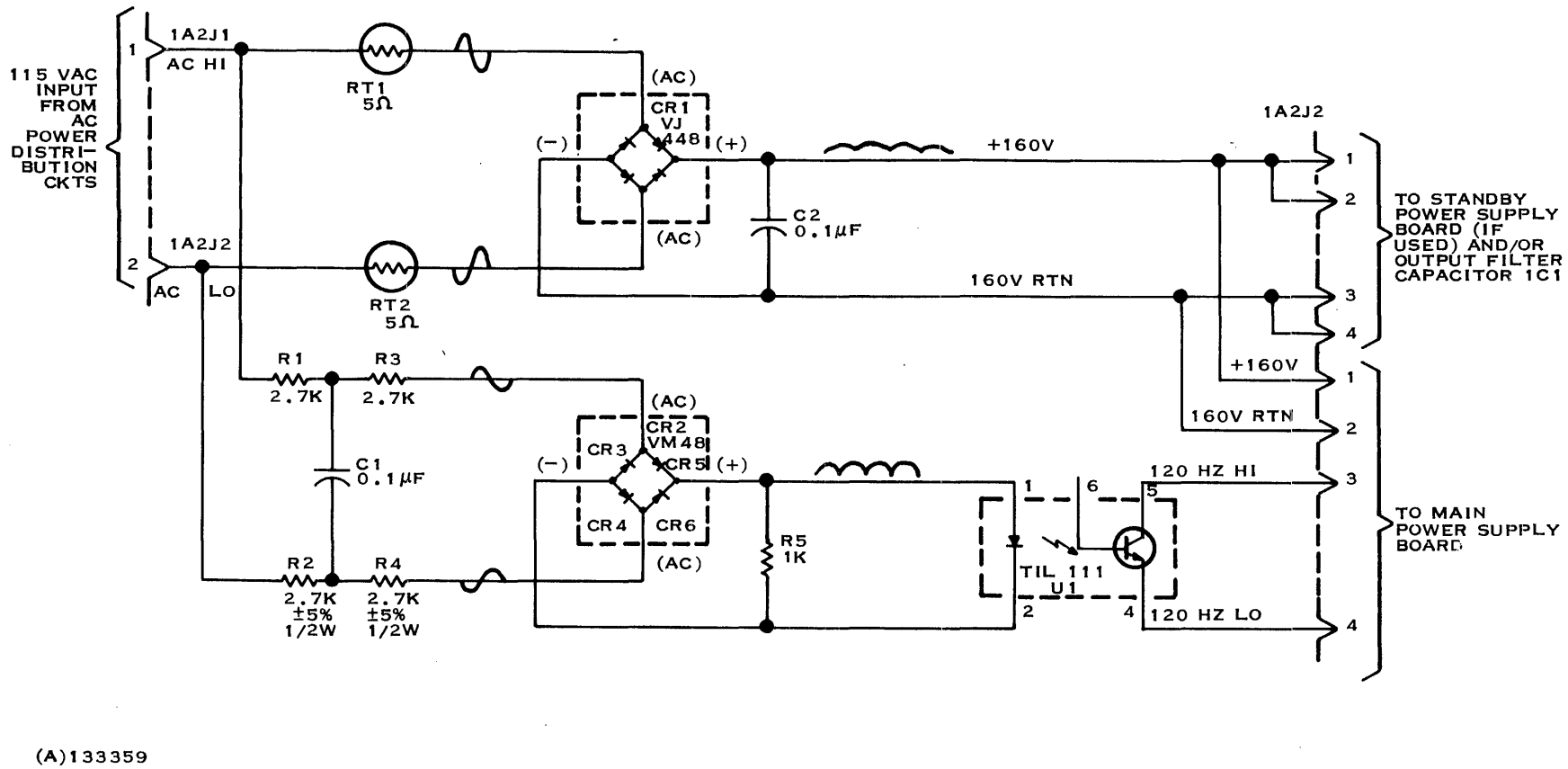


Figure 5-12. Ac Power Converter Board Schematic

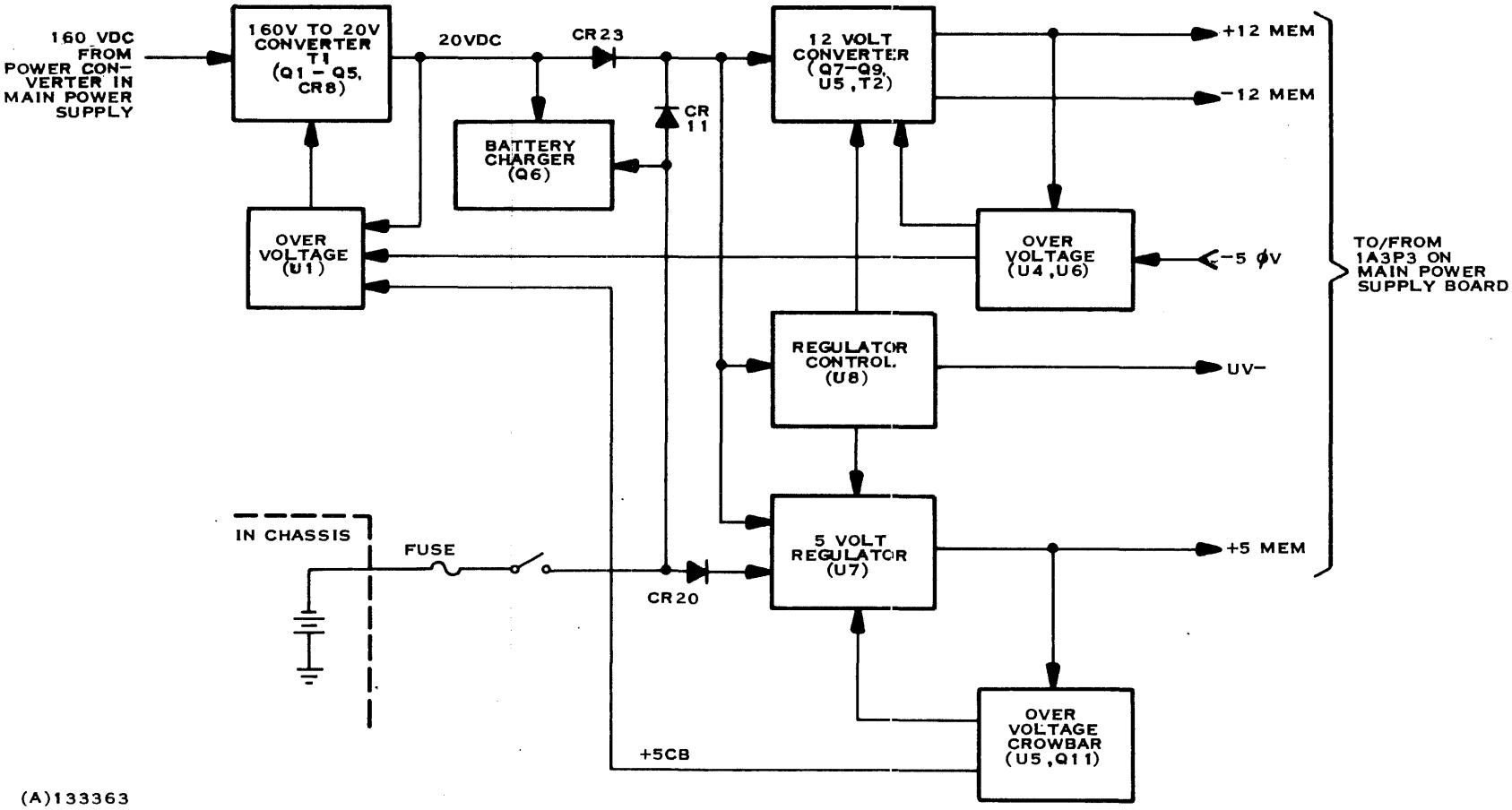


Figure 5-13. Standby Power Supply Board Block Diagram

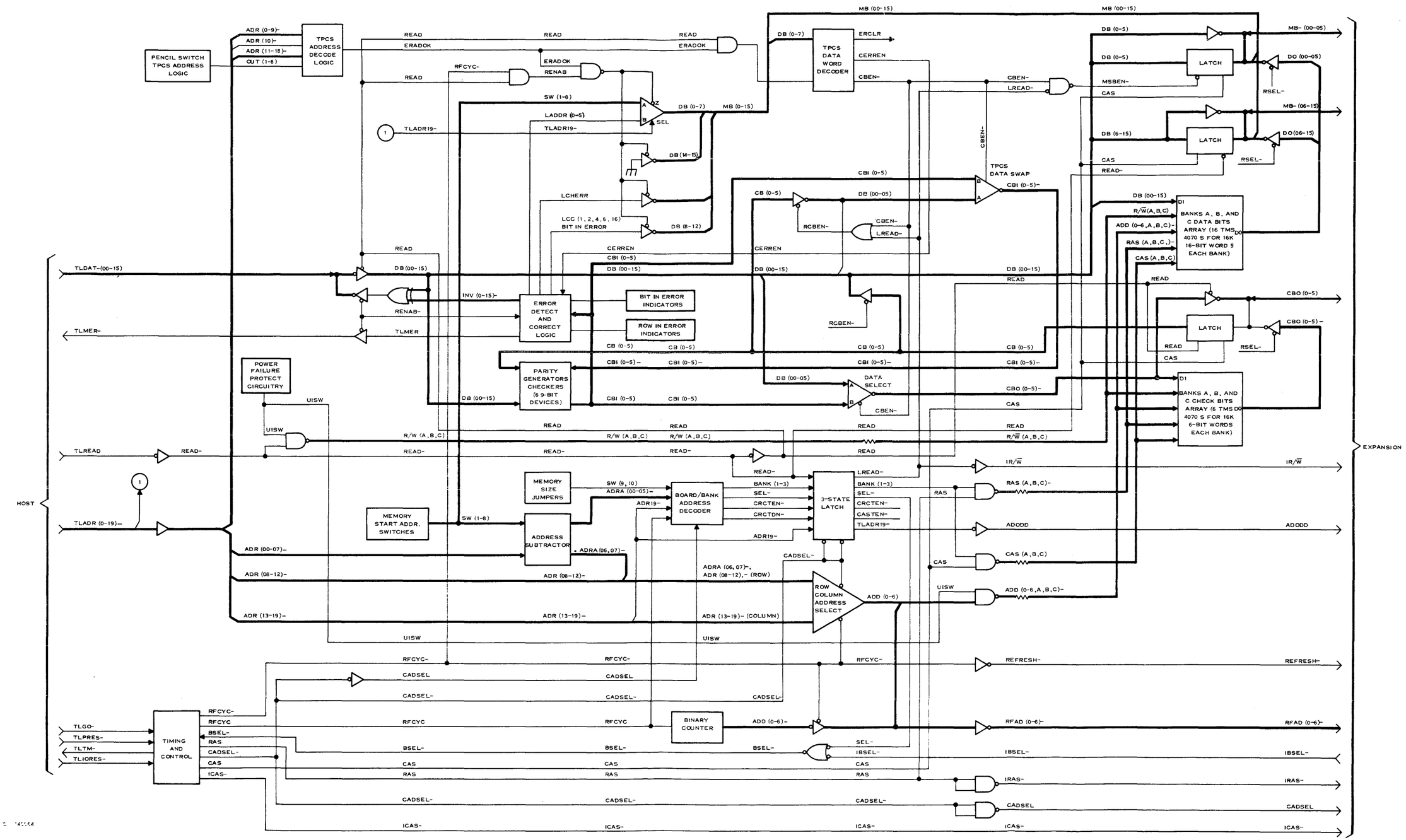


Figure 5-14. ECC 48K Memory Board Block Diagram

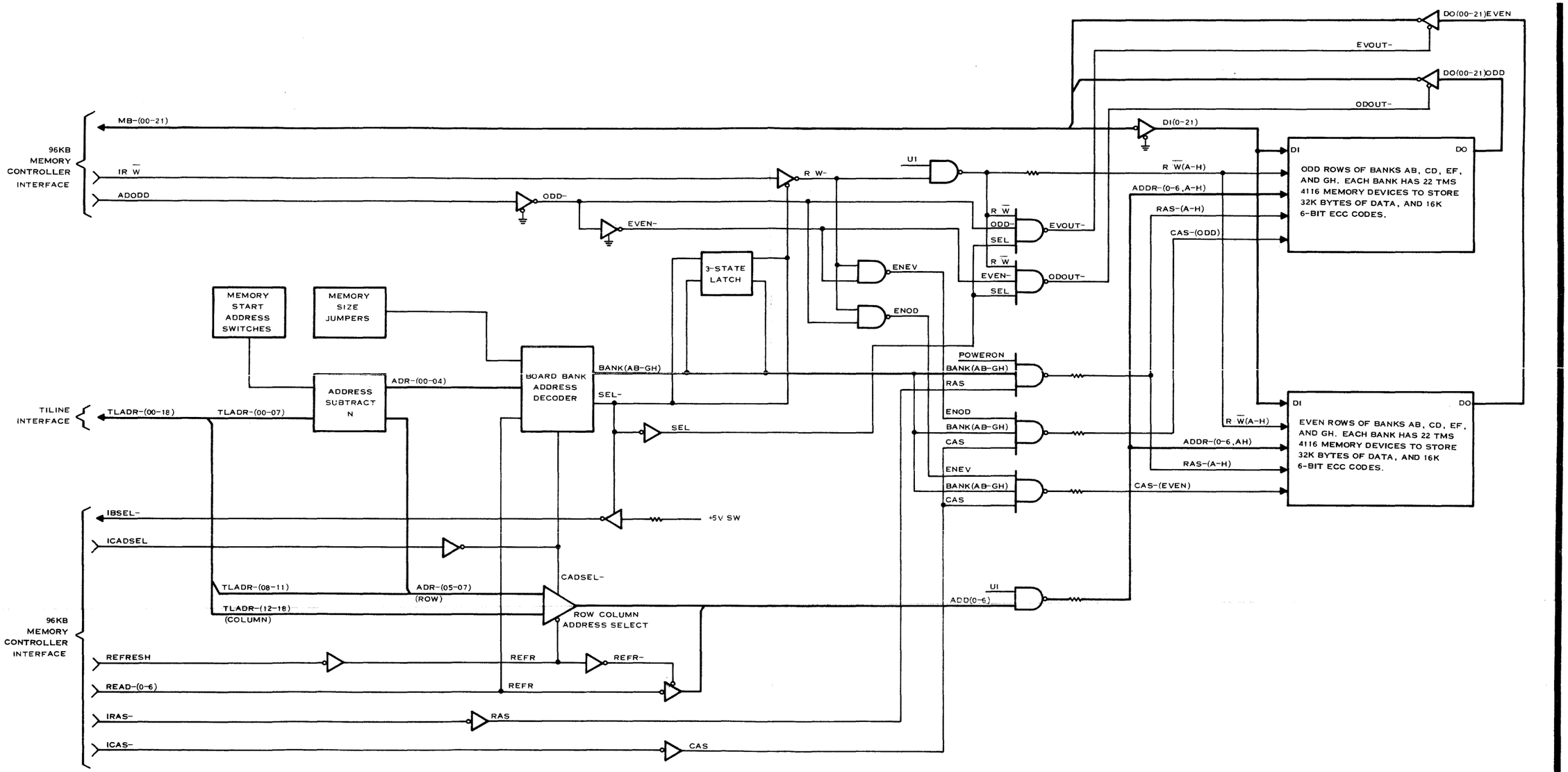


Figure 5-15. 256KB Add-On Array Board Block Diagram

SECTION VI

PACKING AND SHIPPING

6.1 GENERAL

This section provides instructions for unpacking new units and packing faulty assemblies for reshipment to the factory for repair. In most cases, the subassembly will consist of a printed circuit card or cable and will be packed using the packing materials from the replacement subassembly. The procedures for repacking the subassemblies are provided in the following paragraphs.

6.2 UNPACKING/PACKING (6- AND 13-SLOT CHASSIS)

The computer is shipped in a corrugated cardboard container together with the circuit boards and interconnecting cables required to install the system. Upon receipt of the container, inspect to ensure that no signs of physical damage are present. Following preliminary inspection, perform the following steps to remove the computer from its container and ready it for operation. Figure 6-1 illustrates the required steps.

NOTE

Save shipping carton and all packing materials for use in reshipment of the unit.

1. Position container so that the address label is right-side up.

2. Open top of container and remove cushioning material from corners.

NOTE

If the computer has the table top enclosure (6-slot chassis only) no foam block is required to secure circuit boards in chassis.

3. Remove cardboard inner sleeve and foam block (rackmount configurations) from shipping container.

WARNING

Use proper lifting techniques to avoid backstrain when lifting computer chassis.

4. Remove computer and attached shipping pallet from container. When lifting assembly, lift from under the assembly to avoid undue strain on the chassis assembly.

CAUTION

To prevent the mounting screws on the underside of the shipping pallet from scratching table surface, place a shielding material (the packing sleeve removed in step 3 makes an excellent shield) on the table before setting the assembly on the table.

5. Place the removed assembly on a convenient, protected work surface.

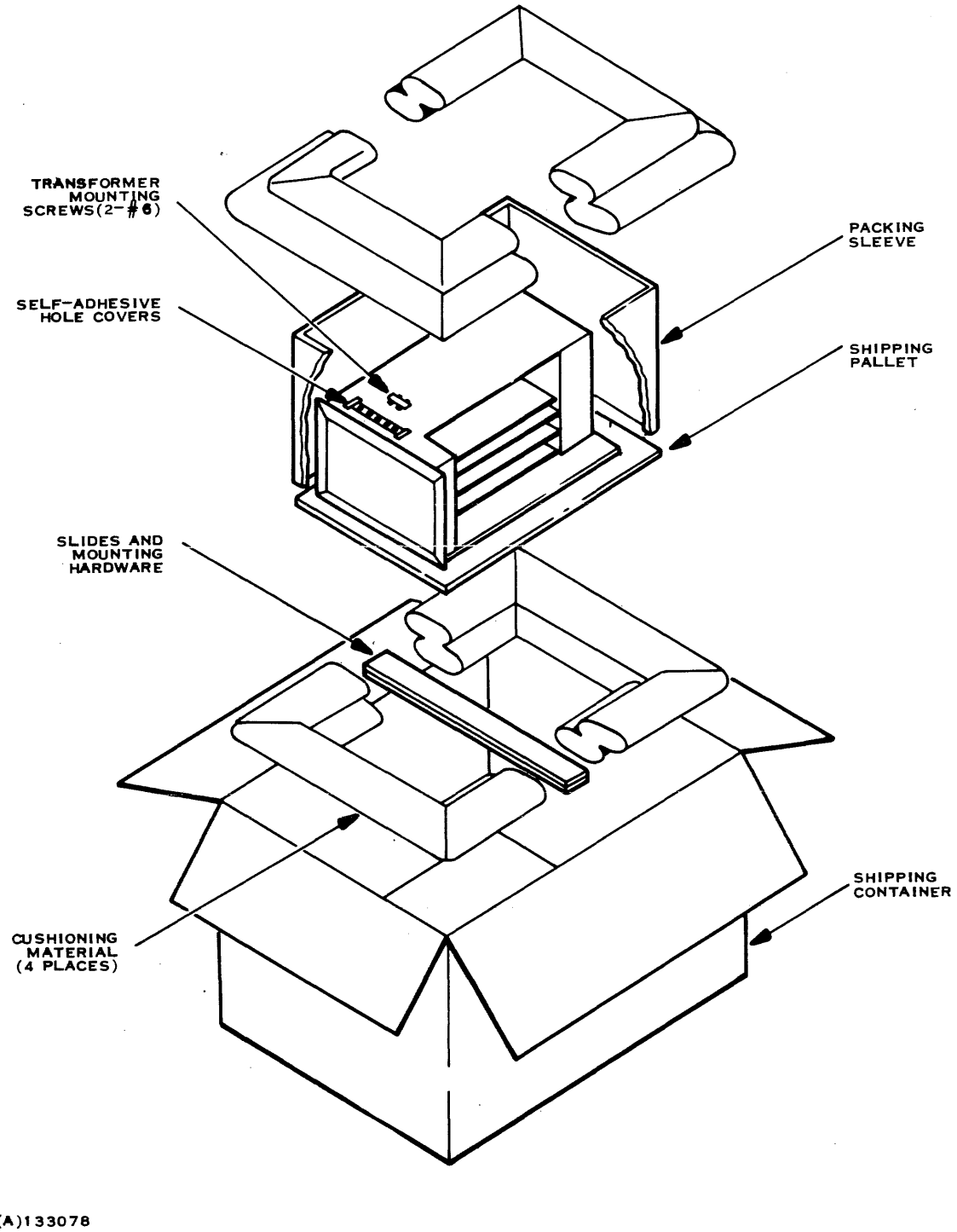


Figure 6-1. Computer Shipping Packaging

NOTE

For rackmount configurations, the slides are packed in the bottom of the shipping container.

6. Remove the rackmount slides (if present) and the interface cables from the bottom of the shipping container.

CAUTION

In the following steps, do not allow the unit to overhang the work surface so far that it will fall off the surface.

7. Position the computer and shipping pallet assembly so that the front edge of the assembly overhangs the edge of the work surface to reveal two (2) #10 mounting screws that secure computer to shipping pallet. See figure 6-2 for location of all mounting screws.

8. Use a straight blade screwdriver to remove the two screws and their associated washers and lock washers. Save the screws and washers for reshipment.

9. Reposition the computer and shipping pallet assembly so that the rear edge of the assembly overhangs the edge of the work surface to reveal three (3) #10 mounting screws that secure computer to shipping pallet.

10. Remove the three screws, washers and lockwashers and save for reshipment.

NOTE

If the computer was ordered for overseas operation, two (2) additional mounting screws are visible on the underside of the shipping pallet. If these screws are not included on the unit being installed, skip step 11.

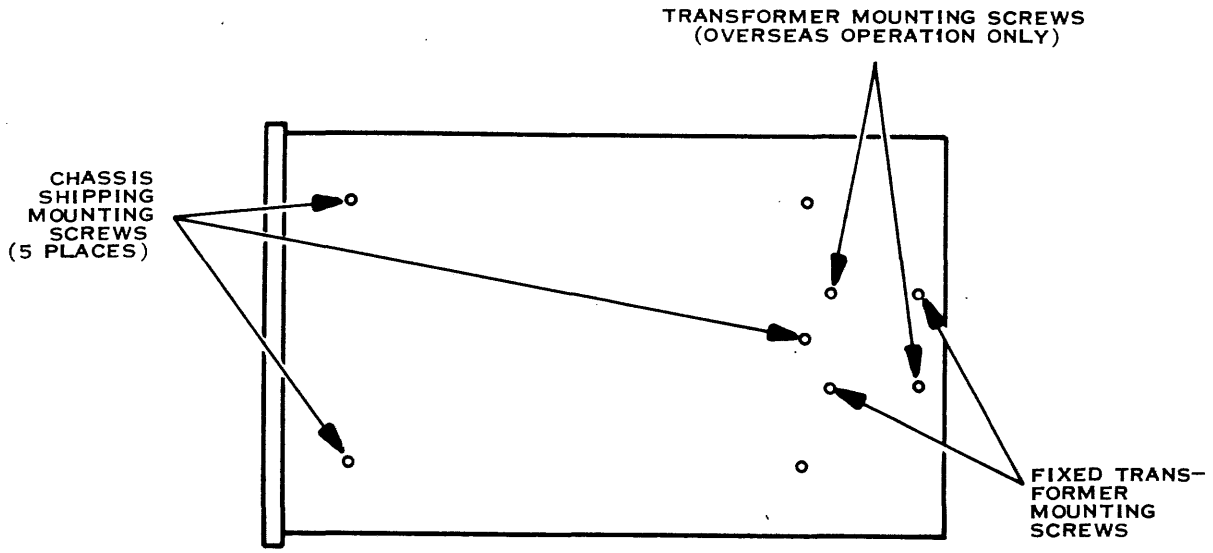
11. Remove two (2) #6 transformer mounting screws and their associated washers and lockwashers and save for reshipment.

12. Lift computer chassis from shipping pallet and place it on the work surface such that the rear of the unit overhangs the work surface to reveal the holes for the removed mounting screws.

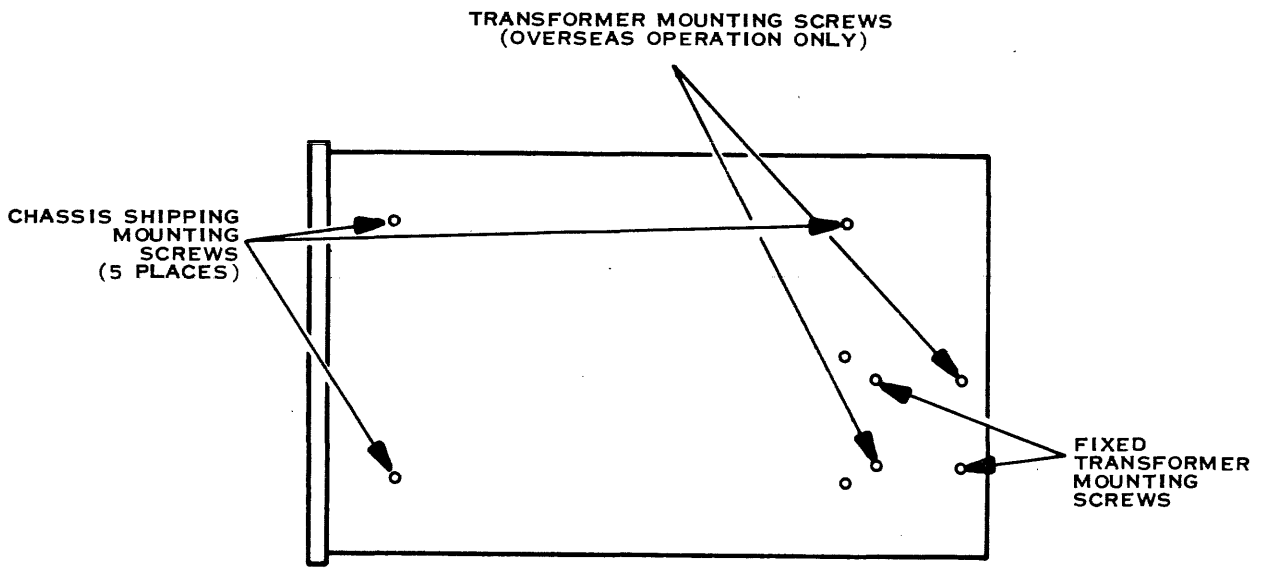
NOTE

If the unit being installed did not have the two #6 mounting screws (see step 11), skip the following step.

13. Remove two (2) #6 screws taped to the top of the computer chassis and insert them in the holes vacated by the two #6 mounting screws moved in step 11. Tighten the two new screws to secure the transformer to the chassis.



(A) 6-SLOT AND TABLE TOP CHASSIS BOTTOM VIEW



(B) 13-SLOT CHASSIS BOTTOM VIEW

(A)133079

Figure 6-2. Location of Chassis Shipping Pallet Mounting Screws

14. Remove the strip of self-adhesive hole covers that are taped to the top of the computer chassis. Use three of the hole covers to cover the three mounting screw holes along the rear of the chassis.

15. Reposition the computer chassis such that the front edge overhangs the work surface to reveal the mounting holes for the front mounting screws.

16. Use the remaining two (2) self-adhesive hole covers to cover the front mounting screw holes.

17. Set the computer chassis in a safe position on the work surface to continue with the remaining portions of the installation procedure.

18. Pack all shipping materials into the original shipping container and store the container for use in reshipment of the unit.

19. Inspect the computer chassis and included components for signs of damage that may have occurred during shipment. If damage has occurred, notify the carrier immediately.

To repack the unit, reverse the above procedure using the original packing material.

6.3 BOARD PACKING/UNPACKING

The logic board assemblies and power supply boards are shipped in bubble-wrap and corrugated cardboard containers. When removing the shipping materials from a spare subassembly, save the bubble wrap and corrugated cardboard for packing faulty boards for reshipment back to the factory.

APPENDIX A

PROGRAMMING REFERENCE DATA

990 INSTRUCTION SET

(ALPHABETICAL ORDER)

Mnemonic Operation Code	Hexadecimal Operation Code	Name	Format
A	A000	Add Words	I
AB	B000	Add Bytes	I
ABS	0740	Absolute Value	VI
AI	0220	Add Immediate	VIII
ANDI	0240	AND Immediate	VIII
B	0440	Branch	VI
BL	0680	Branch and Link	VI
BLWP	0400	Branch and Load Workspace Pointer	VI
C	8000	Compare Words	I
CB	9000	Compare Bytes	I
CI	0280	Compare Immediate	VIII
CKOF (Note 2)	03C0	Clock Off	VII
CKON (Note 2)	03A0	Clock On	VII
CLR	04C0	Clear Operand	VI
COC	2000	Compare Ones Corresponding	III
CZC	2400	Compare Zeros Corresponding	III
DEC	0600	Decrement By One	VI
DECT	0640	Decrement By Two	VI
DIV	3C00	Divide	IX
IDLE (Note 2)	0340	Computer Idle	VII
INC	0580	Increment By One	VI
INCT	05C0	Increment By Two	VI
INV	0540	Invert	VI
JEQ	1300	Jump Equal	II
JGT	1500	Jump Greater Than	II
JH	1B00	Jump High	II
JHE	1400	Jump High Or Equal	II
JL	1A00	Jump Low	II
JLE	1200	Jump Low Or Equal	II
JLT	1100	Jump Less Than	II
JMP	1000	Jump Unconditional	II

Notes 1. 990/10 with mapping only.
2. Does not apply to TMS 9900.

990 INSTRUCTION SET

(ALPHABETICAL ORDER) (Continued)

Mnemonic Operation Code	Hexadecimal Operation Code	Name	Format
JNC	1700	Jump No Carry	II
JNE	1600	Jump Not Equal	II
JNO	1900	Jump No Overflow	II
JOC	1800	Jump On Carry	II
JOP	1C00	Jump Odd Parity	II
LDCR	3000	Load Communication Register	IV
LDD (Note 1)	07C0	Long Distance Destination	VI
LDS (Note 1)	0780	Long Distance Source	VI
LI	0200	Load Immediate	VIII
LIMI	0300	Load Interrupt Mask Immediate	VIII
LMF (Note 1)	0320	Load Memory Map File	X
LREX (Note 2)	03E0	Load or Restart Execution	VII
LWPI	02E0	Load Workspace Pointer Immediate	VIII
MOV	C000	Move Word	I
MOVB	D000	Move Byte	I
MPY	3800	Multiply	IX
NEG	0500	Negate	VI
ORI	0260	OR Immediate	VIII
RSET (Note 2)	0360	Computer Reset	VII
RTWP	0380	Return From Interrupt Subroutine	VII
S	6000	Subtract Word	I
SB	7000	Subtract Byte	I
SBO	1D00	Set Bit To One	II
SBZ	1E00	Set Bit To Zero	II
SETO	0700	Set Ones	VI
SLA	0A00	Shift Left Arithmetic	V
SOC	E000	Set Ones Corresponding, Word	I
SOCB	F000	Set Ones Corresponding, Byte	I

Notes 1. 990/10 with mapping option only.
2. Does not apply to TMS 9900.

990 INSTRUCTION SET

(ALPHABETICAL ORDER) (Continued)

Mnemonic Operation Code	Hexadecimal Operation Code	Name	Format
SRA	0800	Shift Right Arithmetic	V
SRC	0B00	Shift Right Circular	V
SRL	0900	Shift Right Logical	V
STCR	3400	Store Communication Register	IV
STST	02C0	Store Status	VIII
STWP	02A0	Store Workspace Pointer	VIII
SWPB	06C0	Swap Bytes	VI
SZC	4000	Set Zeros Corresponding, Word	I
SZCB	5000	Set Zeros Corresponding, Byte	I
TB	1F00	Test Bit	II
X	0480	Execute	VI
XOP	2C00	Extended Operation	IX
XOR	2800	Exclusive OR	III

990 INSTRUCTION SET

(HEXADECIMAL OP CODE ORDER)

Hexadecimal Operation Code	Mnemonic Operation Code	Name	Format
0200	LI	Load Immediate	VIII
0220	AI	Add Immediate	VIII
0240	ANDI	AND Immediate	VIII
0260	ORI	OR Immediate	VIII
0280	CI	Compare Immediate	VIII
02A0	STWP	Store Workspace Pointer	VIII
02C0	STST	Store Status	VIII
02E0	LWPI	Load Workspace Pointer Immediate	VIII
0300	LIMI	Load Interrupt Mask Immediate	VIII
0320	LMF (Note 1)	Load Memory Map File	X
0340	IDLE (Note 2)	Computer Idle	VII
0360	RSET (Note 2)	Computer Reset	VII
0380	RTWP	Return From Interrupt Subroutine	VII
03A0	CKON (Note 2)	Clock On	VII
03C0	CKOF (Note 2)	Clock Off	VII
03E0	LREX (Note 2)	Load ROM and Execute	VII
0400	BLWP	Branch And Load Workspace Pointer	VI
0440	B	Branch	VI
0480	X	Execute	VI
04C0	CLR	Clear Operand	VI
0500	NEG	Negate	VI
0540	INV	Invert	VI
0580	INC	Increment By One	VI
05C0	INCT	Increment By Two	VI
0600	DEC	Decrement By One	VI
0640	DECT	Decrement By Two	VI
0680	BL	Branch and Link	VI
06C0	SWPB	Swap Bytes	VI
0700	SETO	Set Ones	VI

Notes 1. 990/10 with mapping only.
2. Does not apply to TMS 9900

990 INSTRUCTION SET

(HEXADECIMAL OP CODE ORDER) (Continued)

Hexadecimal Operation Code	Mnemonic Operation Code	Name	Format
0740	ABS	Absolute Value	VI
0780	LDS (Note 1)	Long Distance Source	VI
07C0	LDD (Note 1)	Long Distance Destination	VI
0800	SRA	Shift Right Arithmetic	V
0900	SRL	Shift Right Logical	V
0A00	SLA	Shift Left Arithmetic	V
0B00	SRC	Shift Right Circular	V
1000	JMP	Jump Unconditional	II
1100	JLT	Jump Less Than	II
1200	JLE	Jump Low Or Equal	II
1300	JEQ	Jump Equal	II
1400	JHE	Jump High Or Equal	II
1500	JGT	Jump Greater Than	II
1600	JNE	Jump Not Equal	II
1700	JNC	Jump No Carry	II
1800	JOC	Jump On Carry	II
1900	JNO	Jump No Overflow	II
1A00	JL	Jump Low	II
1B00	JH	Jump High	II
1C00	JOP	Jump Odd Parity	II
1D00	SBO	Set Bit To One	II
1E00	SBZ	Set Bit To Zero	II
1F00	TB	Test Bit	II
2000	COC	Compare Ones Corresponding	III
2400	CZC	Compare Zeros Corresponding	III
2800	XOR	Exclusive OR	III
2C00	XOP	Extended Operation	IX
3000	LDCR	Load Communication Register	IV
3400	STCR	Store Communication Register	IV
3800	MPY	Multiply	IX
3C00	DIV	Divide	IX

Note 1. 990/10 with mapping only.

990 INSTRUCTION SET

(HEXADECIMAL OP CODE ORDER) (Continued)

Hexadecimal Operation Code	Mnemonic Operation Code	Name	Format
4000	SZC	Set Zeros Corresponding, Word	I
5000	SZCB	Set Zeros Corresponding, Byte	I
6000	S	Subtract Word	I
7000	SB	Subtract Byte	I
8000	C	Compare Words	I
9000	CB	Compare Bytes	I
A000	A	Add Words	I
B000	AB	Add Bytes	I
C000	MOV	Move Word	I
D000	MOVB	Move Byte	I
E000	SOC	Set Ones Corresponding, Word	I
F000	SOCB	Set Ones Corresponding, Byte	I

APPENDIX B

INTERRUPT VECTOR TABLE

Table B-1. Interrupt Level Data

Interrupt Level	Vector Location (Trap Address)	Device Assignment	Enabling Mask Values
0	FFFC	Power up	0 through F
1	04	Power failure	1 through F
2	08	Error	2 through F
3	0C	Open	3 through F
4	10	Card reader	4 through F
5	14	Real time clock	5 through F
6	18	733 ASR	6 through F
7	1C	Floppy disc	7 through F
8	20	Open	8 through F
9	24	CRT No. 3	9 through F
10	28	CRT No. 2 or CRU expansion	A through F
11	2C	CRT No. 1	B through F
12	30	Open	C through F
13	34	Diablo disc	D through F
14	38	Line printer	E and F
15	3C	PROM programmer	F only

APPENDIX C

DEVICE CRU FORMATS

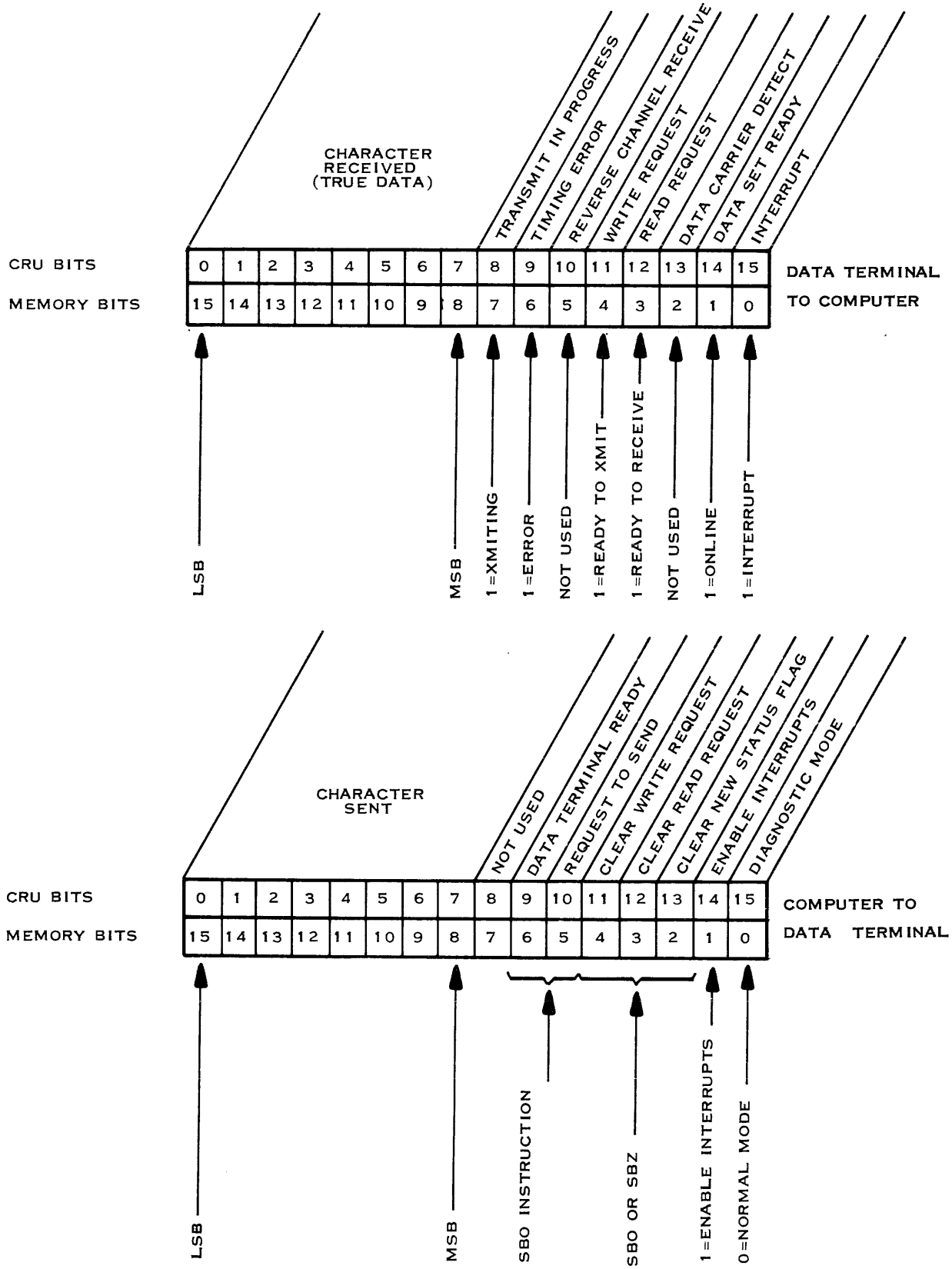


Figure C-1. 733 Data Terminal CRU Formats

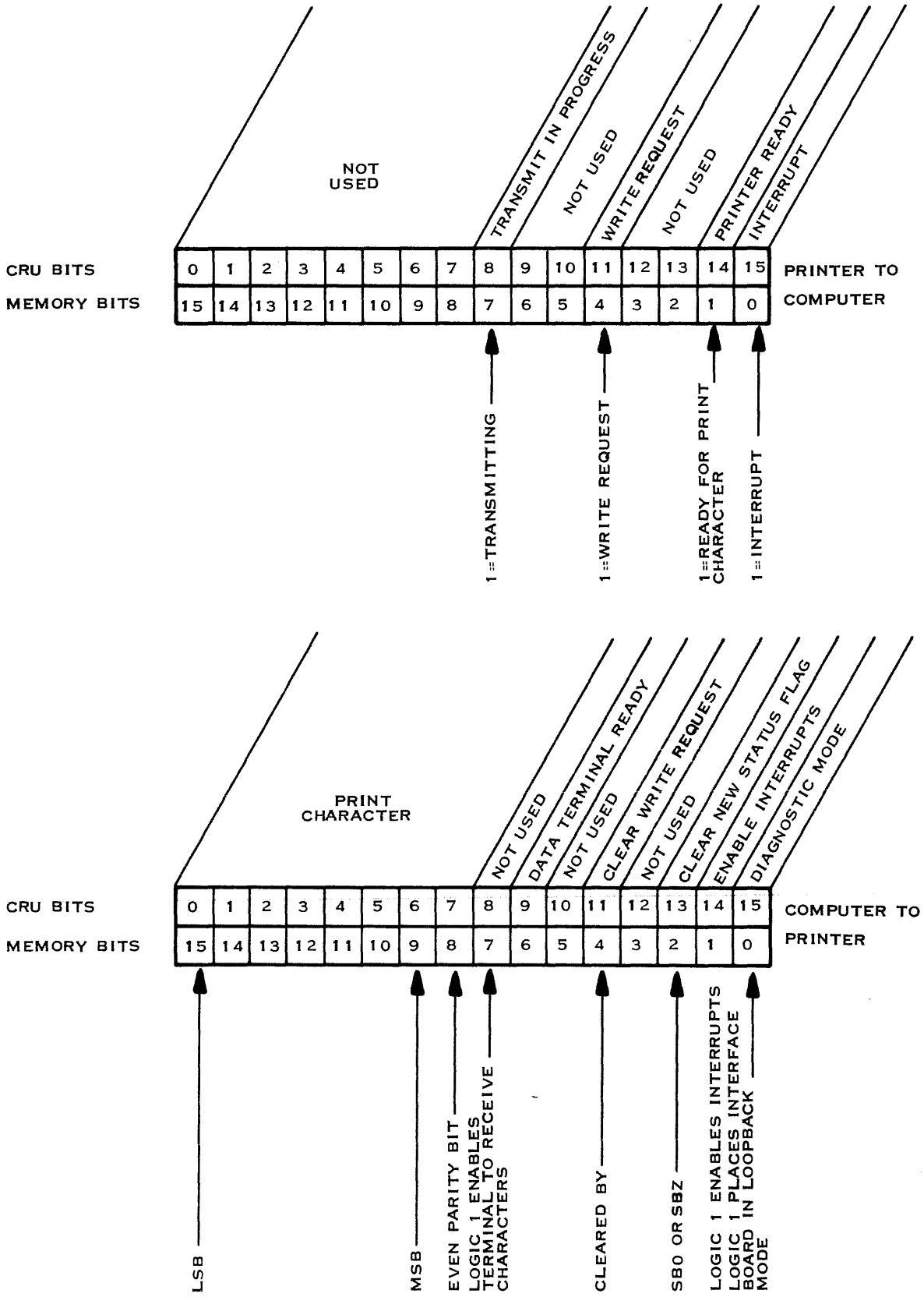


Figure C-2. Model 306/588 Line Printer CRU Formats

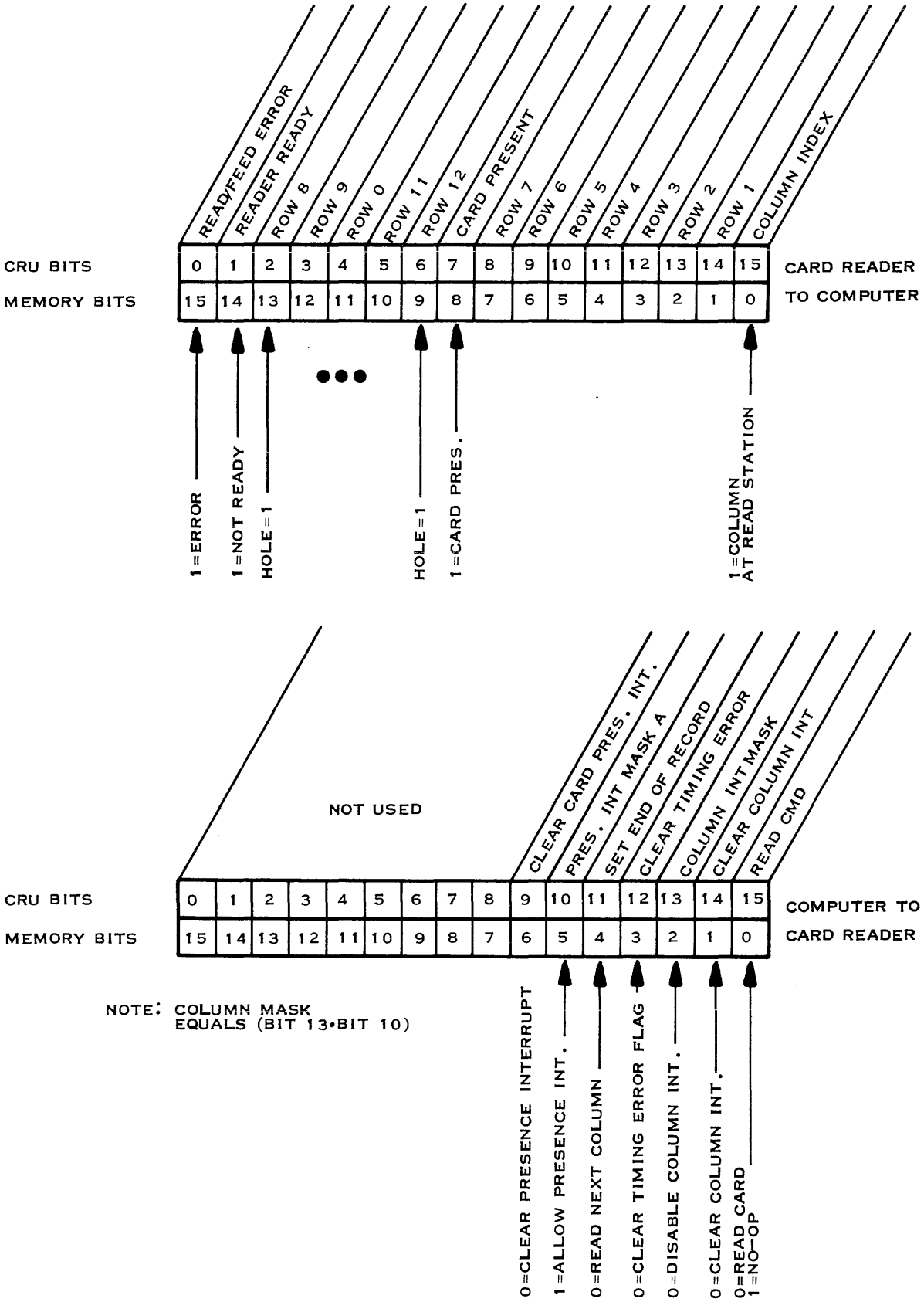


Figure C-3. 804 Card Reader CRU Formats

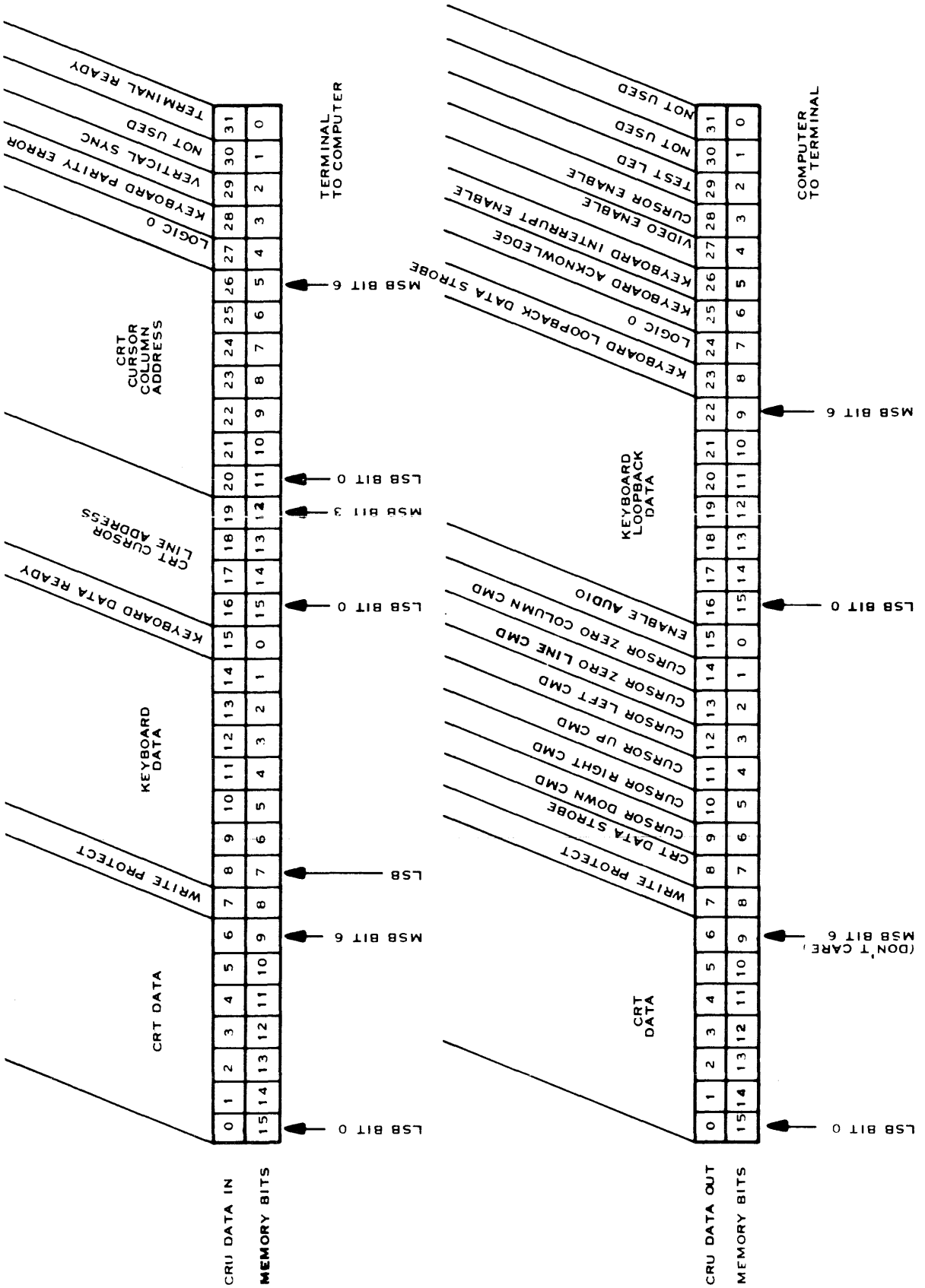


Figure C-4. 913A CRT Display Terminal CRU Formats

APPENDIX D

HEXADECIMAL TO DECIMAL CONVERSION CHARTS

Table D-1. Hexadecimal Arithmetic

ADDITION TABLE

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

MULTIPLICATION TABLE

1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	04	06	08	0A	0C	0E	10	12	14	16	18	1A	1C	1E
3	06	09	0C	0F	12	15	18	1B	1E	21	24	27	2A	2D
4	08	0C	10	14	18	1C	20	24	28	2C	30	34	38	3C
5	0A	0F	14	19	1E	23	28	2D	32	37	3C	41	46	4B
6	0C	12	18	1E	24	2A	30	36	3C	42	48	4E	54	5A
7	0E	15	1C	23	2A	31	38	3F	46	4D	54	5B	62	69
8	10	18	20	28	30	38	40	48	50	58	60	68	70	78
9	12	1B	24	2D	36	3F	48	51	5A	63	6C	75	7E	87
A	14	1E	28	32	3C	46	50	5A	64	6E	78	82	8C	96
B	16	21	2C	37	42	4D	58	63	6E	79	84	8F	9A	A5
C	18	24	30	3C	48	54	60	6C	78	84	90	9C	A8	B4
D	1A	27	34	41	4E	5B	68	75	82	8F	9C	A9	B6	C3
E	1C	2A	38	46	54	62	70	7E	8C	9A	A8	B6	C4	D2
F	1E	2D	3C	4B	5A	69	78	87	96	A5	B4	C3	D2	E1

Table D-2. Table of Powers of 16_{10}

16^n	n	16^{-n}
1	0	0.10000 00000 00000 00000 x 10
16	1	0.62500 00000 00000 00000 x 10^{-1}
256	2	0.39062 50000 00000 00000 x 10^{-2}
4 096	3	0.24414 06250 00000 00000 x 10^{-3}
65 536	4	0.15258 78906 25000 00000 x 10^{-4}
1 048 576	5	0.95367 43164 06250 00000 x 10^{-6}
16 777 216	6	0.59604 64477 53906 25000 x 10^{-7}
268 435 456	7	0.37252 90298 46191 40625 x 10^{-8}
4 294 967 296	8	0.23283 06436 53869 62891 x 10^{-9}
68 719 476 736	9	0.14551 91522 83668 51807 x 10^{-10}
1 099 511 627 776	10	0.90949 47017 72928 23792 x 10^{-12}
17 592 186 044 416	11	0.56843 41886 08080 14870 x 10^{-13}
281 474 976 510 656	12	0.35527 13678 80050 09294 x 10^{-14}
4 503 599 627 370 496	13	0.22204 46049 25031 30808 x 10^{-15}
72 057 594 037 927 936	14	0.13877 78780 78144 56755 x 10^{-16}
1 152 921 504 606 846 976	15	0.86736 17379 88403 54721 x 10^{-18}

Table D-3. Table of Powers of 10_{16}

10^n	n	10^{-n}
1	0	1.0000 0000 0000 0000
A	1	0.1999 9999 9999 999A
64	2	0.28F5 C28F 5C28 F5C3 x 16^{-1}
3E8	3	0.4189 374B C6A7 EF9E x 16^{-2}
2710	4	0.68DB 8BAC 710C B296 x 16^{-3}
86A0	5	0.A7C5 AC47 1B47 8423 x 16^{-4}
4240	6	0.10C6 F7A0 B5ED 8D37 x 16^{-4}
9680	7	0.1AD7 F29A BCAF 4858 x 16^{-5}
E100	8	0.2AF3 1DC4 6118 73BF x 16^{-6}
CA00	9	0.44B8 2FA0 9B5A 52CC x 16^{-7}
E400	10	0.6DF3 7F67 5EF6 EADF x 16^{-8}
E800	11	0.AFEB FF0B CB24 AAFF x 16^{-9}
1000	12	0.1197 9981 2DEA 1119 x 16^{-9}
A000	13	0.1C25 C268 4976 81C2 x 16^{-10}
4000	14	0.2D09 370D 4257 3604 x 16^{-11}
8000	15	0.480E BE7B 9D58 566D x 16^{-12}
0000	16	0.734A CA5F 6226 F0AE x 16^{-13}
0000	17	0.B877 AA32 36A4 B449 x 16^{-14}
0000	18	0.1272 5DD1 D243 ABA1 x 16^{-14}
0000	19	0.1D83 C94F B6D2 AC35 x 16^{-15}

Table D-4. Table of Powers of Two

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5

Table D-5. Hexadecimal–Decimal Integer Conversion Table

The table appearing on the following pages provides a means for direct conversion of decimal integers in the range of 0 to 4095 and for hexadecimal integers in the range of 0 to FFF.

To convert numbers above those ranges, add table values to the figures below:

Hexadecimal	Decimal	Hexadecimal	Decimal
01 000	4 096	20 000	131 072
02 000	8 192	30 000	196 608
03 000	12 288	40 000	262 144
04 000	16 384	50 000	327 680
05 000	20 480	60 000	393 216
06 000	24 576	70 000	458 752
07 000	28 672	80 000	524 288
08 000	32 768	90 000	589 824
09 000	36 864	A0 000	655 360
0A 000	40 960	B0 000	720 896
0B 000	45 056	C0 000	786 432
0C 000	49 152	D0 000	851 968
0D 000	53 248	E0 000	917 504
0E 000	57 344	F0 000	983 040
0F 000	61 440	100 000	1 048 576
10 000	65 536	200 000	2 097 152
11 000	69 632	300 000	3 145 728
12 000	73 728	400 000	4 194 304
13 000	77 824	500 000	5 242 880
14 000	81 920	600 000	6 291 456
15 000	86 016	700 000	7 340 032
16 000	90 112	800 000	8 388 608
17 000	94 208	900 000	9 437 184
18 000	98 304	A00 000	10 485 760
19 000	102 400	B00 000	11 534 336
1A 000	106 496	C00 000	12 582 912
1B 000	110 592	D00 000	13 631 488
1C 000	114 688	E00 000	14 680 064
1D 000	118 784	F00 000	15 728 640
1E 000	122 880	1 000 000	16 777 216
1F 000	126 976	2 000 000	33 554 432

Table D-5. Hexadecimal–Decimal Integer Conversion Table (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
010	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
020	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
030	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
040	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
050	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
060	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
070	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
080	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
090	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
0A0	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
0B0	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
0C0	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
0D0	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
0E0	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
0F0	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255
100	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
110	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
120	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
130	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
140	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
150	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
160	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
170	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
180	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
190	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
1A0	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
1B0	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
1C0	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
1D0	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
1E0	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
1F0	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511
200	0512	0513	0514	0515	0516	0517	0518	0519	0529	0521	0522	0523	0524	0525	0526	0527
210	0528	0529	0530	0531	0532	0533	0534	0535	0536	0537	0538	0539	0540	0541	0542	0543
220	0544	0545	0546	0547	0548	0549	0550	0551	0552	0553	0554	0555	0556	0557	0558	0559
230	0560	0561	0562	0563	0564	0565	0566	0567	0568	0569	0570	0571	0572	0573	0574	0575
240	0576	0577	0578	0579	0580	0581	0582	0583	0584	0585	0586	0587	0588	0589	0590	0591
250	0592	0593	0594	0595	0596	0597	0598	0599	0600	0601	0602	0603	0604	0605	0606	0607
260	0608	0609	0610	0611	0612	0613	0614	0615	0616	0617	0618	0619	0620	0621	0622	0623
270	0624	0625	0626	0627	0628	0629	0630	0631	0632	0633	0634	0635	0636	0637	0638	0639
280	0640	0641	0642	0643	0644	0645	0646	0647	0648	0649	0650	0651	0652	0653	0654	0655
290	0656	0657	0658	0659	0660	0661	0662	0663	0664	0665	0666	0667	0668	0669	0670	0671
2A0	0672	0673	0674	0675	0676	0677	0678	0679	0680	0681	0682	0683	0684	0685	0686	0687
2B0	0688	0689	0690	0691	0692	0693	0694	0695	0696	0697	0698	0699	0700	0701	0702	0703
2C0	0704	0705	0706	0707	0708	0709	0710	0711	0712	0713	0714	0715	0716	0717	0718	0719
2D0	0720	0721	0722	0723	0724	0725	0726	0727	0728	0729	0730	0731	0732	0733	0734	0735
2E0	0736	0737	0738	0739	0740	0741	0742	0743	0744	0745	0746	0747	0748	0749	0750	0751
2F0	0752	0753	0754	0755	0756	0757	0758	0759	0760	0761	0762	0763	0764	0765	0766	0767

Table D-5. Hexadecimal–Decimal Integer Conversion Table (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
300	0768	0769	0770	0771	0772	0773	0774	0775	0776	0777	0778	0779	0780	0781	0782	0783
310	0784	0785	0786	0787	0788	0789	0790	0791	0792	0793	0794	0795	0796	0797	0798	0799
320	0800	0801	0802	0803	0804	0805	0806	0807	0808	0809	0810	0811	0812	0813	0814	0815
330	0816	0817	0818	0819	0820	0821	0822	0823	0824	0825	0826	0827	0828	0829	0830	0831
340	0832	0833	0834	0835	0836	0837	0838	0839	0840	0841	0842	0843	0844	0845	0846	0847
350	0848	0849	0850	0851	0852	0853	0854	0855	0856	0857	0858	0859	0860	0861	0862	0863
360	0864	0865	0866	0867	0868	0869	0870	0871	0872	0873	0874	0875	0876	0877	0878	0879
370	0880	0881	0882	0883	0884	0885	0886	0887	0888	0889	0890	0891	0892	0893	0894	0895
380	0896	0897	0898	0899	0900	0901	0902	0903	0904	0905	0906	0907	0908	0909	0910	0911
390	0912	0913	0914	0915	0916	0917	0918	0919	0920	0921	0922	0923	0924	0925	0926	0927
3A0	0928	0929	0930	0931	0932	0933	0934	0935	0936	0937	0938	0939	0940	0941	0942	0943
3B0	0944	0945	0946	0947	0948	0949	0950	0951	0952	0953	0954	0955	0956	0957	0958	0959
3C0	0960	0961	0962	0963	0964	0965	0966	0967	0968	0969	0970	0971	0972	0973	0974	0975
3D0	0976	0977	0978	0979	0980	0981	0982	0983	0984	0985	0986	0987	0988	0989	0990	0991
3E0	0992	0993	0994	0995	0996	0997	0998	0999	1000	1001	1002	1003	1004	1005	1006	1007
3F0	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023
400	1024	1025	0126	0127	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
410	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
420	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
430	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
440	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
450	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
460	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
470	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
480	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
490	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A0	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B0	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C0	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D0	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E0	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F0	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
500	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1291	1293	1294	1295
510	1296	1297	1298	1299	1399	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
520	1312	1313	1314	1315	1316	1317	1318	1319	1329	1321	1322	1323	1324	1325	1326	1327
530	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
540	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1367	1358	1359
550	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
560	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
570	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
580	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1429	1421	1422	1423
590	1324	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
5A0	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
3B0	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C0	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D0	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E0	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F0	1520	1521	1522	1523	1524	1515	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535

Table D-5. Hexadecimal–Decimal Integer Conversion Table (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
600	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
610	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
620	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
630	1584	1585	1586	1587	1588	1589	1590	1591	1592	1592	1594	1595	1596	1597	1598	1599
640	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
650	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
660	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
670	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
680	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
690	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
6A0	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
6B0	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	17231	1724	1725	1726	1727
6C0	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
6D0	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
6E0	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
6F0	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791
700	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	8102	1803	1804	1805	1806	1807
710	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
720	1824	1825	1826	1827	1818	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
730	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
740	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
750	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
760	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1909	1902	1903
770	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
780	1920	1921	1922	1923	1924	1925	1926	1927	1928	1929	1930	1931	1932	1933	1934	1935
790	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
7A0	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B0	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C0	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D0	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E0	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F0	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047
800	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063
810	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079
820	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
830	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111
840	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127
850	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143
860	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159
870	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175
880	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191
890	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207
8A0	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223
8B0	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239
8C0	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255
8D0	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271
8E0	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287
8F0	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303

Table D-5. Hexadecimal–Decimal Integer Conversion Table (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
900	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319
910	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335
920	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351
930	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367
940	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383
950	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	3496	2397	2398	2399
960	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415
970	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431
980	2432	2433	2434	24351	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447
990	2448	2449	2450	2451	2452	2453	2454	2455	2456	2457	2458	2459	2460	2461	2462	2463
9A0	2464	2465	2466	2467	2468	2469	2479	2471	2472	2473	2474	2475	2476	2477	2478	2479
9B0	2480	2481	2482	2483	2484	2485	2486	2487	2488	2489	2490	2491	2492	2493	2494	2495
9C0	2496	2497	2498	2499	2500	2501	2502	2503	2504	2505	2506	2507	2508	2509	2510	2511
9D0	2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524	2525	2526	2527
9E0	2528	2529	2530	2531	2532	2533	2534	2535	2536	2537	2538	2539	2540	2541	2542	2543
9F0	2544	2545	2546	2547	2548	2549	2550	2551	2552	2553	2554	2555	2556	2557	2558	2559
A00	2560	2561	2562	2563	2564	2565	2566	2567	2568	2569	2570	2571	2572	2573	2574	2575
A10	2576	2577	2578	2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
A20	2592	2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605	2606	2607
A30	2608	2609	2610	2611	2612	2613	2614	2615	2626	2617	2618	2619	2620	2621	2622	2623
A40	2624	2625	2626	2627	2628	2629	2630	2631	2632	2633	2634	2635	2636	2637	2638	2639
A50	2640	2641	2642	2643	2644	2645	2646	2647	2648	2649	2650	2651	2652	2653	2654	2655
A60	2656	2657	2658	2659	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671
A70	2672	2673	2674	2675	2676	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686	2687
A80	2688	2689	2690	2691	2692	2693	2694	2695	2696	2697	2698	2699	2700	2701	2702	2703
A90	2704	2705	2706	2707	2708	2709	2710	2711	2712	2713	2714	2715	2716	2717	2718	2719
AA0	2720	2721	2722	2723	2724	2725	2726	2727	2728	2729	2730	2731	2732	2733	2734	2735
AB0	2736	2737	2738	2739	2740	2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751
AC0	2752	2753	2754	2755	2756	2757	2758	2759	2760	2761	2762	2763	2764	2765	2766	2767
AD0	2768	2769	2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782	2783
AE0	2784	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796	2797	2798	2799
AF0	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815
B00	2816	2817	2818	2819	2820	2821	2822	2823	2824	2825	2826	2827	2828	2829	2830	2831
B10	2832	2833	2834	2835	2836	2837	2838	2839	2840	2841	2842	2843	2844	2845	2846	2847
B20	2848	2849	2850	2851	2852	2853	2854	2855	2856	2857	2858	2859	2860	2861	2862	2863
B30	2864	2865	2866	2867	2868	2869	2870	2871	2872	2873	2874	2875	2876	2877	2878	2879
B40	2880	2881	2882	2883	2884	2885	2886	2887	2888	2889	2890	2891	2892	2893	2894	2895
B50	2896	2897	2898	2899	2900	2901	2902	2903	2904	2905	2906	2907	2908	2909	2910	2911
B60	2912	2913	2914	2915	2916	2917	2918	2919	2920	2921	2922	2923	2924	2925	2926	2927
B70	2928	2929	2930	2931	2932	2933	2934	2935	2936	2937	2938	2939	2940	2941	2942	2943
B80	2944	2945	2946	2947	2948	2949	2950	2951	2952	2953	2954	2955	2956	2957	2958	2959
B90	2960	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2971	2972	2973	2974	2975
BA0	2976	2977	2978	2979	2980	2981	2982	2983	2984	2985	2986	2987	2988	2989	2990	2991
BB0	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC0	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD0	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE0	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF0	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071

Table D-5. Hexadecimal–Decimal Integer Conversion Table (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C00	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C10	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C20	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C30	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C40	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C50	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C60	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C70	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C80	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C90	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA0	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB0	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC0	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD0	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE0	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF0	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327
D00	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D10	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D20	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D30	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D40	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D50	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D60	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D70	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D80	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D90	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA0	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB0	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC0	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD0	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE0	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF0	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583
E00	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E10	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E20	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E30	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E40	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E50	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E60	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E70	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E80	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E90	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA0	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB0	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775

Table D-5. Hexadecimal–Decimal Integer Conversion Table (Cont.)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
EC0	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791
ED0	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807
EE0	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823
EF0	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839
F00	3840	3841	3842	3843	3844	3845	3846	3847	3848	3849	3850	3851	3852	3853	3854	3855
F10	3856	3857	3858	3859	3860	3861	3862	3863	3864	3865	3866	3867	3868	3869	3870	3871
F20	3872	3873	3874	3875	3876	3877	3878	3879	3880	3881	3882	3883	3884	3885	3886	3887
F30	3888	3889	3890	3891	3892	3893	3894	3895	3896	3897	3898	3899	3900	3901	3902	3903
F40	3904	3905	3906	3907	3908	3909	3910	3911	3912	3913	3914	3915	3916	3917	3918	3919
F50	3920	3921	3922	3923	3924	3925	3926	3927	3928	3929	3930	3931	3932	3933	3934	3935
F60	3936	3937	3938	3939	3940	3941	3942	3943	3944	3945	3946	3947	3948	3949	3950	3951
F70	3952	3953	3954	3955	3956	3957	3958	3959	3960	3961	3962	3963	3964	3965	3966	3967
F80	3968	3969	3970	3971	3972	3973	3974	3975	3976	3977	3978	3979	3980	3981	3982	3983
F90	3984	3985	3986	3987	3988	3989	3990	3991	3992	3993	3994	3995	3996	3997	3998	3999
FA0	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012	4013	4014	4015
FB0	4016	4017	4018	4019	4020	4021	4022	4023	4024	4025	4026	4027	4028	4029	4030	4031
FC0	4032	4033	4034	4035	4036	4037	4038	4039	4040	4041	4042	4043	4044	4045	4046	4047
FD0	4048	4049	4050	4051	4052	4053	4054	4055	4056	4057	4058	4059	4060	4061	4062	4063
FE0	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF0	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095

APPENDIX E

SCOPING LOOP PROGRAMS

APPENDIX E

SCOPING LOOP PROGRAMS

E.1 GENERAL

This section contains a collection of loop programs which may be entered into the computer through the programmer panel. The procedure for entering all of these programs is essentially the same as outlined in paragraph E.2.

E.2 READ FOLLOWED BY WRITE AT SAME MEMORY LOCATION

The following program may be used to loop on a single specified address within the 32K address space of the 990/4:

MEM Location	Machine Code	Comments
0900	02E0	LWPI, >100
0902	0100	
0904	0208	LI R8, (location)
0906	2000	Desired memory address (byte address)
0908	0209	LI R9, (data)
090A	0F0F	(or any desired data pattern)
090C	C609	Mov R9, *R8
090E	10FE	JMP $-1

The scoping loop is entered into the computer from the programmer panel using the following procedure:

1. Set the key switch on the programmer panel to the UNLOCK position.

2. If the RUN LED is lit, press the HALT/SIE switch to halt the processor and begin execution of the programmer panel code. When the panel is active, the RUN LED is extinguished.

3. Press the CLR switch to clear the panel's display register.

4. Press the ENTER ST (enter status) switch to clear the status register in the TMS 9900.

5. Set up 0900_{16} on the data display LEDs using the data entry switches. This is the address in memory where the first instruction of the scoping loop is to be stored.

NOTE

When a data display LED is lit, it indicates a "1".

6. Press ENTER MA switch to load the memory address value 0900 into the memory address register of the TMS 9900.

7. Press CLR to clear the displays for the next entry.

8. Set up the instruction code ($02E0_{16}$) on the data LED displays using the data entry switches.

9. Press MDE switch which causes 02E0 to be loaded into memory location 0900.

10. Press MAI which increments the memory address value stored in the memory address register and repeat steps 8-11 to enter the following program values into successive memory locations:

    - 0100
    - 0208
    - Address on which the test will loop (0000 to 1FFFE inclusive)
    - 0209
    - Data to be written into the looped memory location (e.g., $1F1F_{16}$)
    - C609
    - 10FE

11. Press CLR to clear the displays.

12. Enter 0900 into the displays (address of first instruction in the scoping loop).

13. Press ENTER PC to load the value into the program counter.

14. Press RUN to begin execution of the program. The RUN LED should light to indicate proper operation.

NOTE

If the RUN LED fails to light, return to step 1 and repeat the program setup procedure.

E.3 CONTINUOUS READ FROM SELECTED MEMORY LOCATION

The basic scoping loop program described in E.2 may be modified to perform a continuous read at a selected memory address by changing the instruction at memory location 090C in the previous program from C609 to C258 which is a MOV *R8,R9 instruction. This change to the basic program causes data to be read from a selected address and stored in memory location 0112 (workspace register 9). For maintenance purposes, the scoping loop may be interrupted at any time and the value stored in the workspace register may be examined using the following procedure:

1. Halt the processor by pressing HALT/SIE. The RUN LED should extinguish.

2. Press CLR to clear the displays.

3. Enter 0112 into the displays using the data entry switches.

4. Press ENTER MA to load 0112 into the memory address register.

5. Press MDD. The resulting value displayed on the panel LEDs should be the same value stored in memory location 90A of the scoping loop program.

E.4 SCOPING LOOP FOR A BAND OF MEMORY ADDRESSES

The basic scoping loop program may also be modified as follows to permit looping over a band of memory addresses in which the beginning and ending addresses are specified in the program:

Scoping Loop for Reading Band of Memory Addresses

MEM Location	Machine Code	Comments
0900	02E0	LWPI >80
0902	0100	
0904	020A	LI R10, ENDLOC
0906	ENDLOC	Ending address +2
0908	0209	LI R9, DATA
090A	DATA	
090C	0208 ←	LI R8, LOC
090E	LOC	
0910	→ CE09	MOV R9, *R8+
0912	820A	C R10, R8
0914	14FB —	JHE
0916	— 10FC	JMP

The procedures for entering this program into computer memory are essentially the same as described in paragraph E.2.

APPENDIX F

CRU BIT ASSIGNMENTS

Table F-1. Map File CRU Output Bit Assignments

CRU Bit Number	Function
0 (LSB) through 2 (MSB)	Read Register Select Code 2 (LSB) through 0 (MSB): This 3-bit code selects which of the map file registers in the currently selected map will be fanned-in for sampling on the CRU input interface. The code bits are decoded as follows:

Code Bit 0	1	2	Register Selected
0	0	0	Base Register 1
0	0	1	Base Register 2
0	1	0	Base Register 3
0	1	1	Limit Register 1
1	0	0	Limit Register 2
1	0	1	Limit Register 3
1	1	0	Latch Memory Address Register (5-19)
1	1	1	Latch Memory Address Register (0-4)

3	Enable Mapping: When set to a 1, this bit turns on the mapping circuitry; when this bit is cleared, mapping is disabled.
4	Reset Flags: Setting this bit to a 1 clears the error flag and the capture address latch, and prevents them from being set again; clearing this bit enables operation of the two latches.
5	Latch Control 1: When set, this bit instructs the mapping circuits to capture the first address that uses base register 1. The resulting mapped address will be captured in the Latch Memory Address Register.
6	Latch Control 2: When set, this bit instructs the mapping circuits to capture the first address that uses base register 2. The resulting mapped address will be captured in the Latch Memory Address Register.
7	Latch Control 3: When set, this bit instructs the mapping circuits to capture the first address that uses base register 3. The resulting mapped address will be captured in the Latch Memory Address Register.

Table F-2. Programmer Panel CRU Input Bit Assignments

BIT	DESCRIPTION	FUNCTION
0 1 2 3 4 5 6 7	Switch column 7 Switch column 6 Switch column 5 Switch column 4 Switch column 3 Switch column 2 Switch column 1 Switch column 0	CRU input bits 0 through 7 are assigned to switch columns 7 through 0 respectively. An 8-bit Store Communications Register (STCR) instruction from the computer stores the value of a row of eight switches as defined by the scan counter. A switch that has been depressed and has stopped bouncing is stored into memory as a logic ONE.
8	Scan Count 1	A logic ONE on CRU input bit 8 indicates that the scan counter is in the function (row 2 or row 3) group of switches.
9	Scan Count 0	A logic ONE on CRU input bit 9 indicates that the scan counter is in the least significant byte (row 1 or row 3) of either the data or the function group of switches.
10	Timer Active	A logic ONE on CRU input bit 10 indicates that the debounce timer has finished timing out.
11	Front Panel Not Present Or Locked	A logic ONE on CRU input bit 11 indicates that the panel is not connected to the computer or that the programmer panel key switch is in the LOCK position.
12 and 13	Not Used	
14	Maintenance Unit Not Present	A logic ZERO on CRU input bit 14 indicates that the 990 maintenance unit is connected to the computer rather than the standard programmer panel.
15	Not Used	

Table F-3. Programmer Panel CRU Output Bit Assignments

BIT	DESCRIPTION	FUNCTION
0 through 7	Data Display Lamps 0 through 15	A 16-bit word is transferred to the lamps for display by executing two 8-bit Load Communication Register (LDCR) instructions on the word to be displayed in a most significant byte, least significant byte order.
8	Increment scan	A Set Bit to ONE (SBO) or SBZ instruction addressed to CRU output bit 8 increments the scan counter. For example, if the scan counter is at count 11_2 then it will increment to count 00_2 after execution of the SBO. The scan counter is set to 10_2 when the RUN bit is set.
9	Not Used	CRU output bit 9 not used in the programmer panel.
10	Run	An SBO instruction addressed to CRU output bit 10 illuminates the RUN LED, sets the DATA LEDs to log ONEs, sets the scan counter to 10_2, and enables the interrupt. The foregoing actions are effected by programmer panel ROM software when the RUN switch is pressed while in the HALT mode. Following a power-up, the RUN bit is set to a logic ONE.
11	Fault	The FAULT output bit is connected to an LED on both the programmer panel and the computer. A logic ONE to output bit 11 illuminates both LEDs. A zero clears both LEDs.
12	Clear internal interrupts	An SBO or SBZ instruction addressed to CRU output bit 12 clears the error interrupt flag in the computer. This action is performed by the CPU and is not a function of the programmer panel.
13	Start Timer	An SBO or SBZ instruction addressed to CRU output bit 13 starts the debounce timer. CRU input bit 10 monitors the timer output.
14	Single Instruction Execute (SIE)	An SBO or SBZ instruction addressed to CRU output bit 14 enables the computer to execute two more instructions before trapping to the programmer panel ROM. By addressing this bit and following with an RTWP, panel software can perform the SIE function. This action is performed by the CPU and is not a function of the panel.
15	Not Used	CRU output bit 15 not used in the programmer panel.

APPENDIX G

DETAILS OF TILINE OPERATION

APPENDIX G

DETAILS OF TILINE OPERATION

G.1 GENERAL

The TILINE is the high-speed bus that connects the internal RAM, disc, tape, and other processors to the 990/10 CPU via the interface board.

G.1.1 TILINE APPLICATIONS. The TILINE is fully implemented on high capability Model 990 Computers, including the 990/10 minicomputer, where it is utilized as the sole path of data communication between all high-speed system elements. The central processor, the main memory, and all high-speed peripheral devices such as disc files and magnetic tape transports are directly connected to the TILINE. Slower peripheral devices, such as EIA-compatible devices, are connected to the 990/10 minicomputer through the communications register unit (CRU). The interface to the minicomputer system of either a CRU or TILINE device is effected by installing either device into a slot of the chassis backpanel since the CRU and TILINE share the same backpanel but use different pin positions.

G.1.2 MASTER-SLAVE CONCEPT. There are two classes of devices that connect to the TILINE: TILINE MASTER devices that control data transfers, and TILINE SLAVE devices that generate or accept data in response to some MASTER device. Data transfers in either direction always occur between one MASTER and one SLAVE. The central processor is an example of a MASTER device and a memory module is an example of a SLAVE device. All SLAVE devices recognize a specific address and are activated only when addressed. For example, a memory module is activated when some MASTER device performs a read operation from an address within the bounds of its address. The configuration of the system must be such that only one SLAVE device recognizes any particular address. For memory modules, pencil switches on the modules are set to provide the desired starting address and size of the module.

Peripheral controllers are both MASTER and SLAVE devices. Special registers addressed as specific memory addresses near the high end of memory constitute the SLAVE part of the peripheral controller. The registers are loaded by the central processor with memory-to-memory move instructions. The registers specify the parameters of a peripheral data transfer. In the case of a disc, they specify disc address, the number of sectors of data to be transferred, the memory address to which the data is to be transferred and whether the data is to be read or written. One register in each peripheral controller is a status register for that controller. The bits in the register indicate information such as "operation complete", "read error", "rewind complete", and "illegal command". Other bits in the peripheral controller status register are set by the central processor to command the peripheral to start, stop, clear its interrupt, or reset. All of these registers are addressed by the central processor as consecutive words of memory at some specific address. Pencil switches are used to set the address of the registers for each peripheral controller. When a peripheral controller is started by the central processor, it transfers data between memory and the peripheral device by cycle-stealing with the central processor and any other MASTER devices that may be active. When a peripheral controller needs to transfer a word of data over the TILINE, the MASTER device part of the peripheral controller must gain access to the TILINE and then may address a SLAVE (such as a memory module) and read from or write to it.

G.1.3 **TILINE INTERFACE SIGNALS.** There are 48 TILINE interface signals that perform the addressing, data transfer, and control functions of the TILINE. Figure G-1 illustrates and table G-1 defines the TILINE interface signals and gives their assigned connector pin numbers at the chassis packpanel. The signals are functionally grouped and described in the three subparagraphs that follow.

Data Transfer Operations. There are 40 TILINE interface signals that are used exclusively for data transfer operations on the TILINE. As shown in figure G-1, 36 of these signals consist of the 20 address bits and 16 data bits with the remaining 4 signals used primarily for control of the actual data transfer operation. These 4 signals are: TLGO–, TLREAD, TLTM–, and TLMER–. All signals are transmitted and received between a TILINE MASTER device and a TILINE SLAVE device during a transfer of data. A description of both a read and write data transfer are described herein.

Timing for the TILINE MASTER to SLAVE write cycle is as shown in figure G-2 and is referenced in the following discussion. When a TILINE MASTER device has access to the TILINE it may accomplish a memory (SLAVE) write cycle as follows. The MASTER asserts TILINE GO (TLGO–) and at the same time asserts the write command TILINE READ (TLREAD) by setting both signals low. The MASTER at this time also generates valid write data on the data bus (TLDAT–) and a valid 20-bit address (TLADR–) on the address lines. All SLAVE devices on the TILINE receive the TILINE GO transmitted by the MASTER. The SLAVE devices must decode the address to determine which SLAVE is being addressed. The SLAVE generates a delayed GO signal (using a timer circuit) and uses that signal to strobe for a valid address decode. In the case of a memory module, a delayed GO and a valid address decode generate a memory start signal. It is the responsibility of the SLAVE device to delay GO for a time sufficient to accommodate the worst case address decode time and the worst case TILINE skew, with TILINE skew defined as 20 nanoseconds maximum. When the SLAVE device has delayed GO and decoded the address as valid it performs the write cycle and then asserts the TILINE TERMINATE (TLTM–). At the time the SLAVE device asserts TLTM– it must be finished with the TLDAT–, TLADR–, and TLREAD signals from the TILINE. The action just described occurs during "time 1" as shown in figure 3-9. This time is defined as the SLAVE access time and must be less than 1.5 microseconds for all TILINE SLAVES except the TILINE coupler. When the TILINE MASTER receives the asserted TLTM–, it must release TLGO–, TLREAD, TLADR–, and TLDAT– within 120 nanoseconds. This occurs during "time 2" shown in figure 3-9. At this time the MASTER device may relinquish the TILINE to another MASTER device. When the SLAVE receives the release of TLGO–, it must release TLTM– within 120 nanoseconds as shown in "time 3" of figure 3-9. When the MASTER device receives the release of TLTM–, it may begin a new cycle if it has not relinquished the TILINE to another MASTER device. This is shown as "time 4" in figure 3-9.

Timing for the TILINE MASTER to SLAVE read cycle is as shown in figure G-3 and is referenced in the following discussion. When a TILINE MASTER device has access to the TILINE it may accomplish a memory (SLAVE) read cycle as follows. The MASTER asserts TLGO– and at the same time generates a valid address signal (TLADR–) and TLREAD signal. All SLAVE devices on the TILINE receive the TILINE GO transmitted by the MASTER. The SLAVE devices delay the GO signal and decode the address as is done for a write cycle. As in the write cycle, it is the responsiblity of the SLAVE device to delay GO for a time sufficient to accommodate the worst case TILINE skew (defined as 20 nanoseconds maximum) and worst case address decode time. When this has been done and the address is decoded as valid, the SLAVE device begins to generate read data. In the case of a memory module this means starting a read cycle. When read data is valid, the SLAVE device asserts TLTM– and at this time must have finished using TILINE signals TLADR– and TLREAD. If a read error is detected during a read cycle, the READ ERROR (TLMER–) signal is asserted by the SLAVE. This signal must

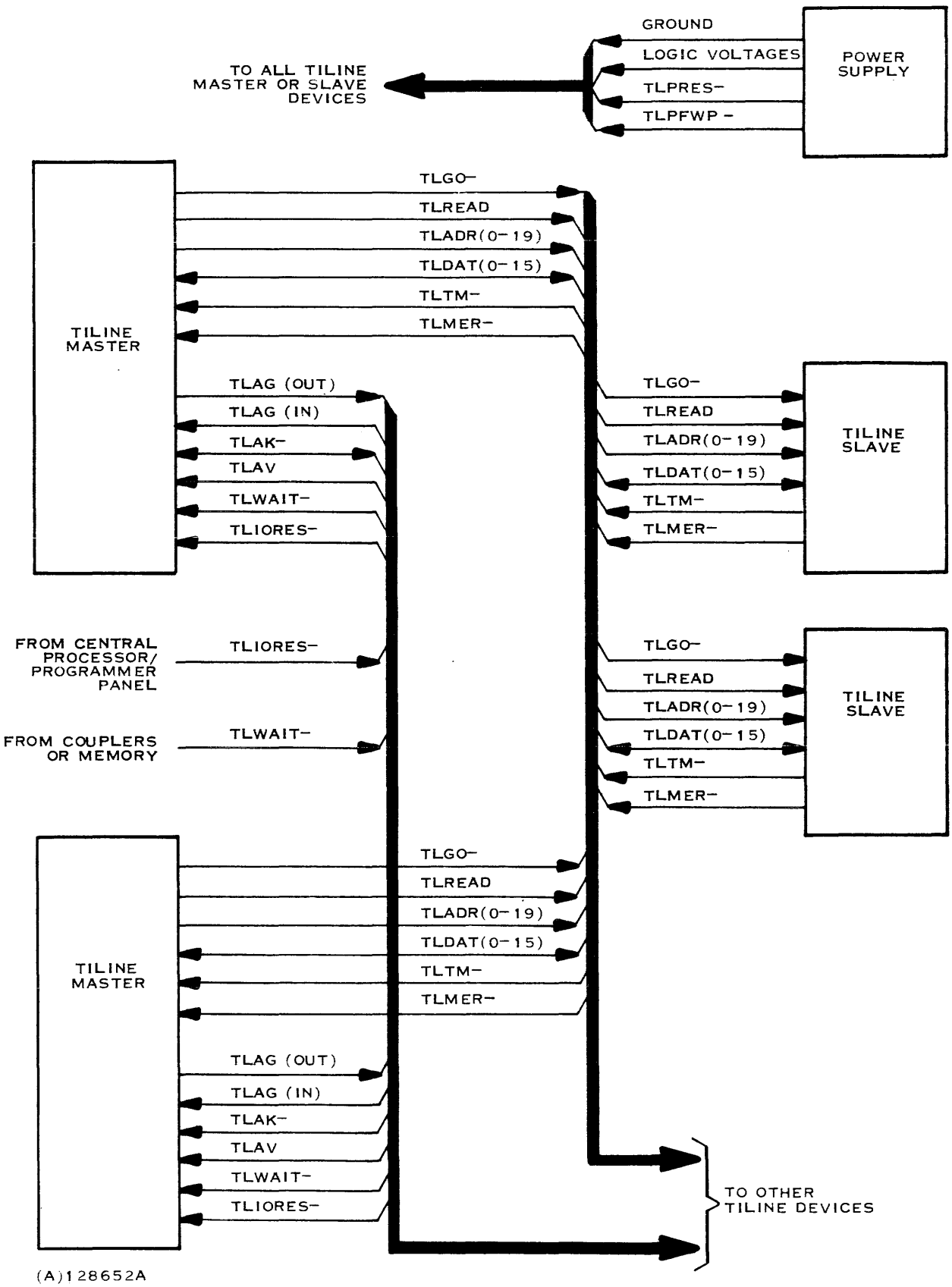


Figure G-1. TILINE Interface Signals

Table G-1. TILINE Signal Definitions

Signature	Pin No.	Definition
TLGO–	P1-25	TILINE Go: Initiates all data transfers when transition from high (3.0V) to low (1.0V) occurs. See note 1.
TLREAD	P1-11	TILINE Read: When high (3.0V) designates a read from SLAVE operation; when low (1.0V) designates a write to SLAVE operation. See note 1.
TLADR00–	P2-55	TILINE Address to define the location of data during a fetch or store operation. When high (≥2.0V) the corresponding address bit is a zero; when low (≤0.8V) the corresponding address bit is a one. See note 2.
01–	P2-44	
02–	P2-51	
03–	P2-53	
04–	P2-57	
05–	P2-59	
06–	P2-47	
07–	P2-49	
08–	P2-17	
09–	P2-19	
10–	P2-10	
11–	P2-12	
12–	P2-11	
13–	P2-15	
14–	P2-8	
15–	P2-9	
16–	P2-29	
17–	P2-27	
18–	P2-25	
TLADR19–	P2-31	
TLDAT00–	P2-67	TILINE Data: Bidirectional data lines that when high (≥2.0V) represent zero data bits, and when low (≤0.8V) represent one data bit. See note 2.
01–	P2-69	
02–	P2-35	
03–	P2-37	
04–	P2-61	
05–	P2-63	
06–	P2-43	
07–	P2-45	
08–	P2-21	
09–	P2-33	
10–	P2-23	
11–	P2-20	
12–	P1-27	
13–	P1-28	
14–	P1-30	
TLDAT15–	P1-31	
TLTM–	P1-20	TILINE Terminate: When low (1.0V) indicates that the SLAVE device has completed the requested operation. See note 1.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.

Table G-1. TILINE Signal Definitions (Continued)

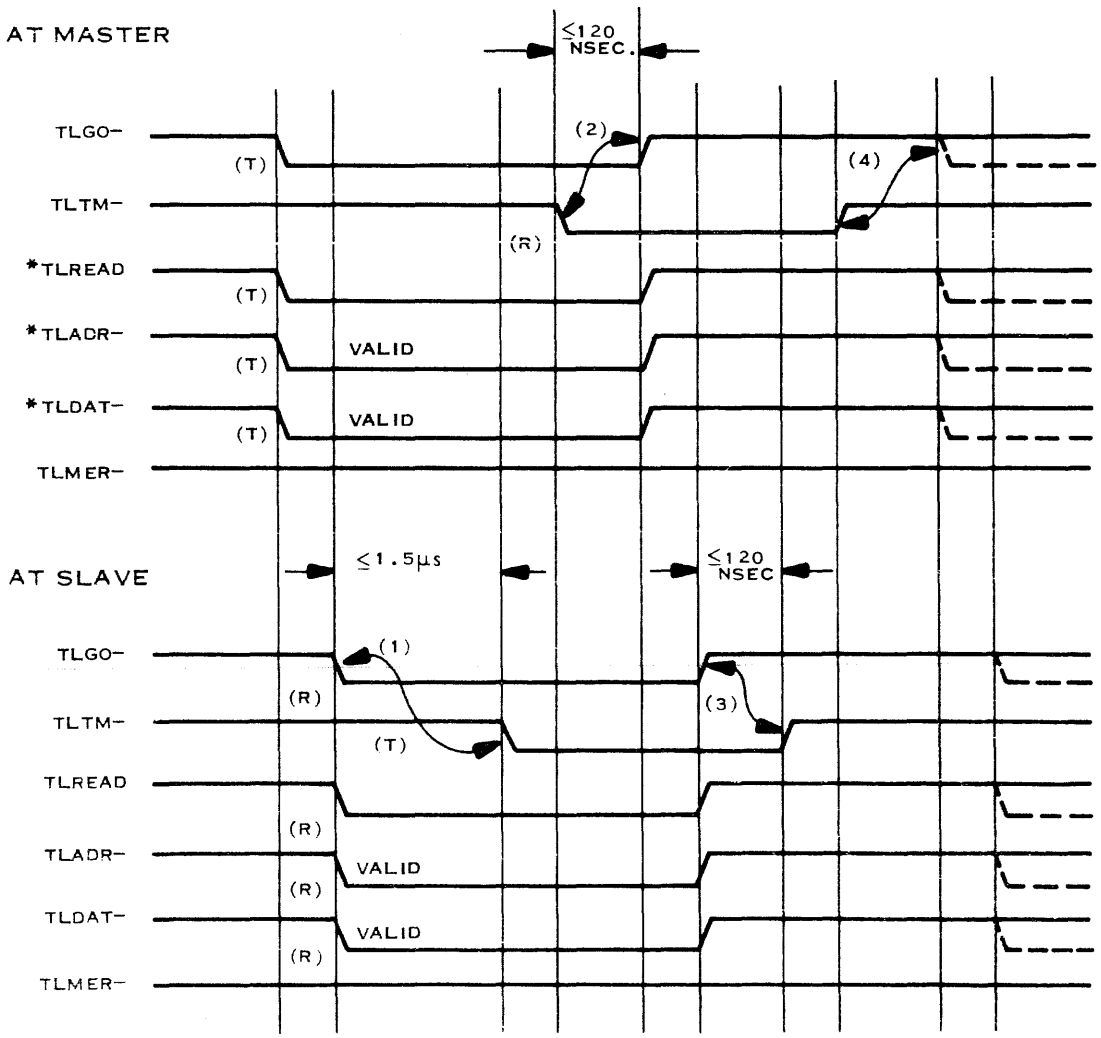
Signature	Pin No.	Definition
TLMER–	P1-55	TILINE Memory Error: When low (≤0.8V) indicates that a nonrecoverable error has occurred during a memory read operation. See note 2.
TLAG (in)	P2-6	TILINE Access Granted: When high (≥2.0V), this signal indicates that no higher priority device has requested use of the TILINE. When low (≤0.8V), this signal prevents the receiving device from gaining access to the TILINE bus.
TLAG (out)	P2-5	TILINE Access Granted: When high (≥2.0V), this signal indicates that neither the sending device nor any higher priority device is requesting use of the TILINE. When low (≤0.8V), this signal indicates that either the sending device or some higher priority device is requesting use of the TILINE bus and prevents all lower priority devices from gaining access to the bus.
TLAK–	P1-71	TILINE Acknowledge: When high (3.0V), this signal indicates that no TILINE device has been recognized as the next device to use the TILINE. When low (1.0V), this signal indicates that some TILINE device has requested access, has been recognized, and is waiting for the bus to become available. See note 1.
TLAV	P1-58	TILINE Available: When high (3.0V), this signal indicates that no TILINE device is using the bus. When low (1.0V), this signal indicates that the TILINE bus is busy. See note 1.
TLWAIT–	P1-63	TILINE Wait: A normally high (3.0V) signal that when low (1.0V), temporarily suspends all TILINE MASTER devices from using the TILINE bus. This signal is generated by bus couplers to allow them to use the bus as the highest priority user. See note 1.
TLIORES–	P1-14 P2-14	TILINE I/O Reset. A normally high (≥2.0V) signal that when low (≥0.8V), halts and resets all TILINE I/O devices. This signal is a 100 to 500 nanosecond pulse generated by the RESET switch on the control console or by the execution of a Reset (RSET) instruction in the AU. Driven by SN7437; Received by 2 (maximum standard SN74- loads per slot).
TLPRES–	P1-13 P2-13	TILINE Power Reset: A normally high (≥2.0V) signal that goes low (≥0.8V) to reset all TILINE devices and inhibit critical lines to external equipment. The signal is generated by the power supply at least 10 microseconds before dc voltages begin to fail during power-down, and until dc voltages are stable during power-up. Driven by 80-milliampere open-collector driver (160 milliamperes with 40-ampere power supply).
TLPFWP–	P1-16 P2-16	TILINE Power Failure Warning Pulse: A 7.0 millisecond pulse preceding TLPRES–. When low (≤0.8V), this signal indicates that a power-down sequence is in progress, allowing the AU to perform its power failure interrupt subroutine. Driven by SN7437; received by two, maximum, standard SN74- loads per card slot.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.

Table G-1. TILINE Signal Definitions (Continued)

Signature	Pin No.	Definition
TLHOLD–	P2-26	TILINE Hold Signal: A normally high (3.0V) signal that goes low (1.0V) to assert that a central processor is executing an ABS instruction. TILINE Hold prevents interference from another processor on the TILINE while the first processor is performing the ABS instruction. This signal is used and propagated by TILINE COUPLERS in multi-processor systems. See note 1.

Note 1: Received by SN75138; driven by 36 milliampere, minimum, open-collector driver.
Note 2: Received by one, maximum, standard SN74- load per card slot; driven by SN74LS367/8.



NOTES: NUMBERS IN PARENTHESES DENOTE TIME PERIODS REFERENCED IN TEXT.
(TILINE DELAY IS EXAGGERATED FOR CLARITY)
(T) = TRANSMITTED
(R) = RECEIVED
*TLREAD, TLADR–, AND TLDAT– MUST BE STABLE AT THE TIME (OR BEFORE) TLGO– IS ASSERTED.

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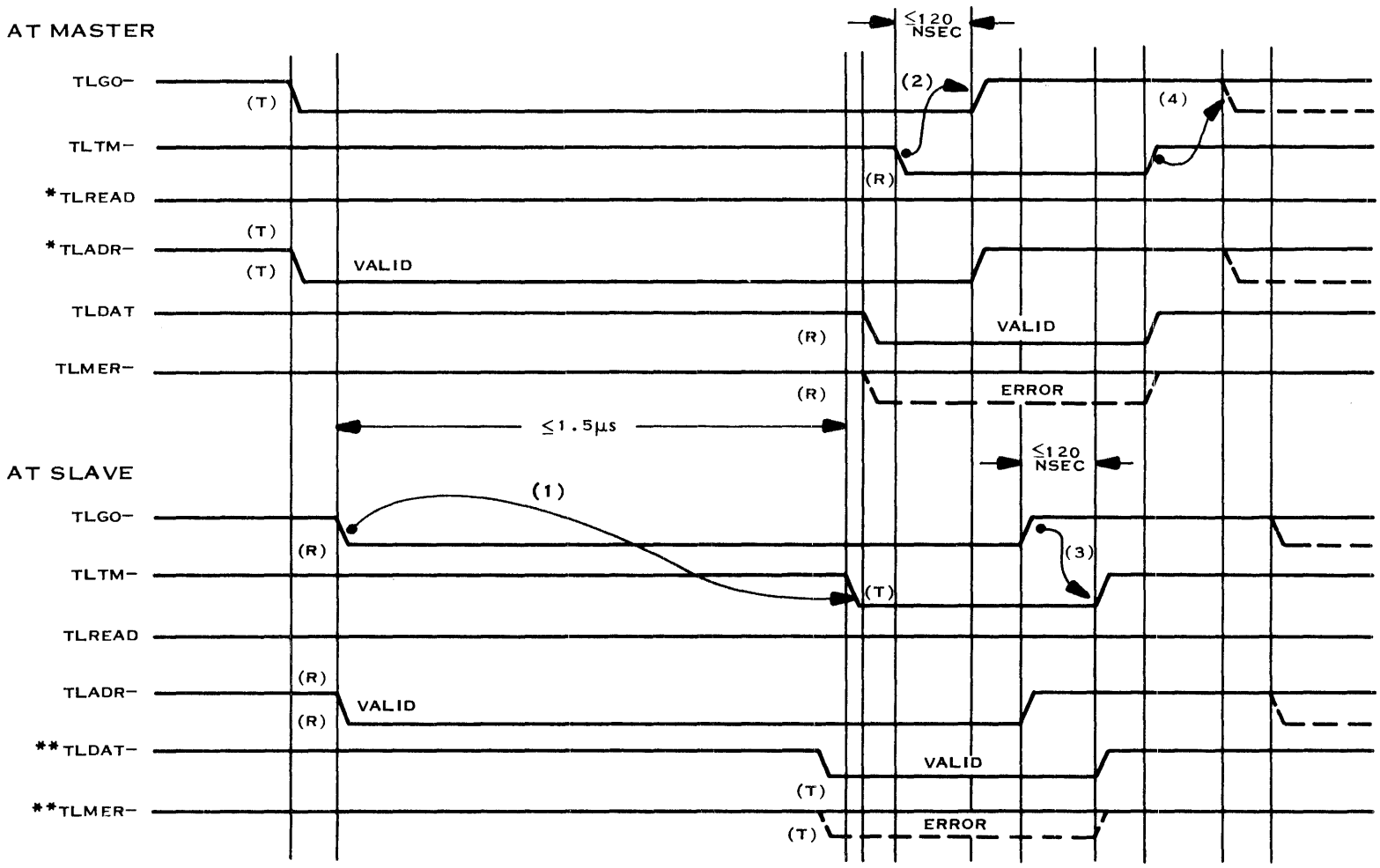
Figure G-2. TILINE MASTER to SLAVE Write Cycle Timing Diagram



NOTES: NUMBERS IN PARENTHESES DENOTE TIME PERIODS REFERENCED IN TEXT. (TILINE DELAY IS EXAGGERATED FOR CLARITY)
(T) = TRANSMITTED (R) = RECEIVED
*TLREAD AND TLADR– MUST BE STABLE AT THE TIME (OR BEFORE) TLGO– IS ASSERTED
**TLDAT– AND TLMER– MUST BE STABLE AT THE TIME (OR BEFORE) TLTM– IS ASSERTED

(A)133123

Figure G-3. TILINE MASTER to SLAVE Read Cycle Timing Diagram

have the same timing that the read data would have had and this action occurs during "time 1" as shown in figure 3-10. "Time 1" is defined as the SLAVE access time and must be less than 1.5 microseconds for all TILINE SLAVES except the TILINE coupler. When the MASTER devices receive the asserted TLTM–, it must delay at least for worst case TILINE skew (20 nanoseconds, maximum) and then release TLGO– and TLADR– signal lines. At the time the MASTER device releases TLGO– it must have finished using the TLDAT– and the TLMER– signals. This action occurs during "time 2" of figure 3-10 and must not require more than 120 nanoseconds. At this time the TILINE MASTER device may relinquish the TILINE to another MASTER device. When the SLAVE device receives the release TLGO–, it must release TLTM– and TLDAT– signals. This action occurs during "time 3" as shown in figure 3-10 and must not be a greater time period than 120 nanoseconds. When the MASTER device receives the released TLTM– it may begin a new cycle if it has not relinquished the TILINE to another MASTER device. This is shown as "time 4" of figure 3-10.

MASTER Device TILINE Acquisition. The three TILINE signals; TILINE Access Granted (TLAG), TILINE Acknowledge (TLAK–), and TILINE Available (TLAV) are used by MASTER devices to schedule the next TILINE MASTER during the last data transfer operation of the present TILINE MASTER. All TILINE MASTER devices are connected to the TILINE in a positional priority system with that TILINE device installed into the highest numbered chassis slot receiving the highest priority. Priority ranking decreases with each chassis slot location toward that chassis slot occupied by the central processor, which has the lowest priority. Figure G-4 illustrates the connections between TILINE MASTER devices that establish the priority system. In the 990/ chassis family backplane etch, TLAGIN is jumpered to TLAGOUT for all TILINE card slots except slot 7 which is, by convention, the slot used for the first TILINE MASTER device controller. Additional TILINE MASTER device controllers may be inserted in other TILINE card slots at higher or lower priority if the etch between pins P2-5 and P2-6 is cut in the slot where the controller is installed.

The access controllers for each of the TILINE MASTER devices are identical. A flowchart of the operation of the access controllers is provided in figure G-5 and is referenced in the following discussion.

When a TILINE MASTER device is inactive or reset, its access controller is in the IDLE state. In this state, TILINE Access Granted (TLAG) is passed on to lower priority MASTER devices and the access controller monitors for a Set Device Access Request signal from the device.

As soon as the device generates a Set Device Access Request signal indicating that it wants to obtain TILINE access the access controller changes from the IDLE state to the DEVICE ACCESS REQUEST (DAR) state.

In the DAR state the access controller monitors TILINE Access Granted (TLAGIN) and TILINE Acknowledge (TLAK–). The access controller also disables TLAGOUT to the lower priority devices. After TLAGIN has been high for at least 100 nanoseconds and after the access controller has been in the DAR state for at least 100 nanoseconds, a high TLAK– causes the access controller to change to the DEVICE ACKNOWLEDGE (DAK) state.

In the DAK state the access controller continues to disable TLAG to lower priority MASTER devices and pulls TILINE Acknowledge (TLAK–) low. In this state the access controller monitors TILINE Available (TLAV) and when TLAV is high the access controller changes to the DEVICE ACCESS (DACC) state.

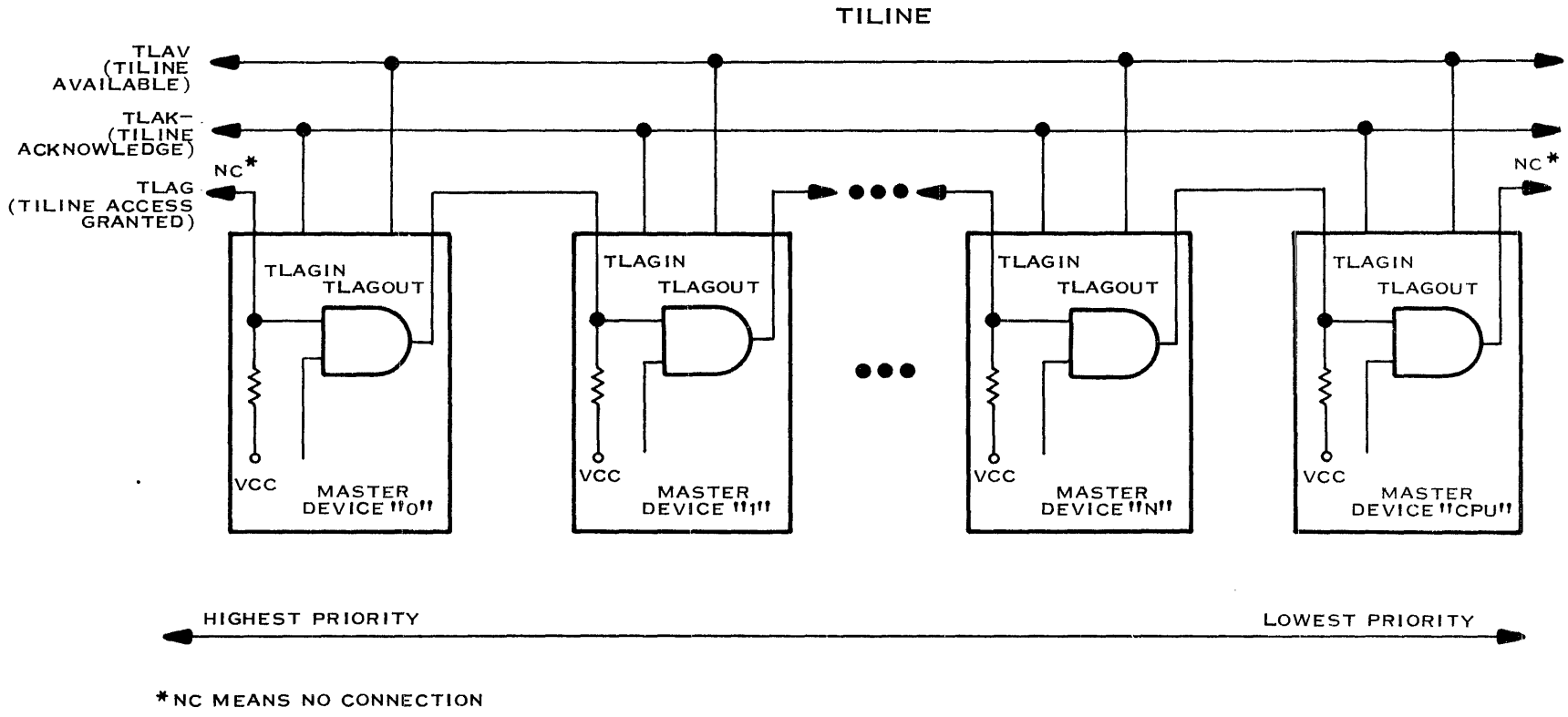


Figure G-4. TILINE MASTER Devices Priority Interconnection

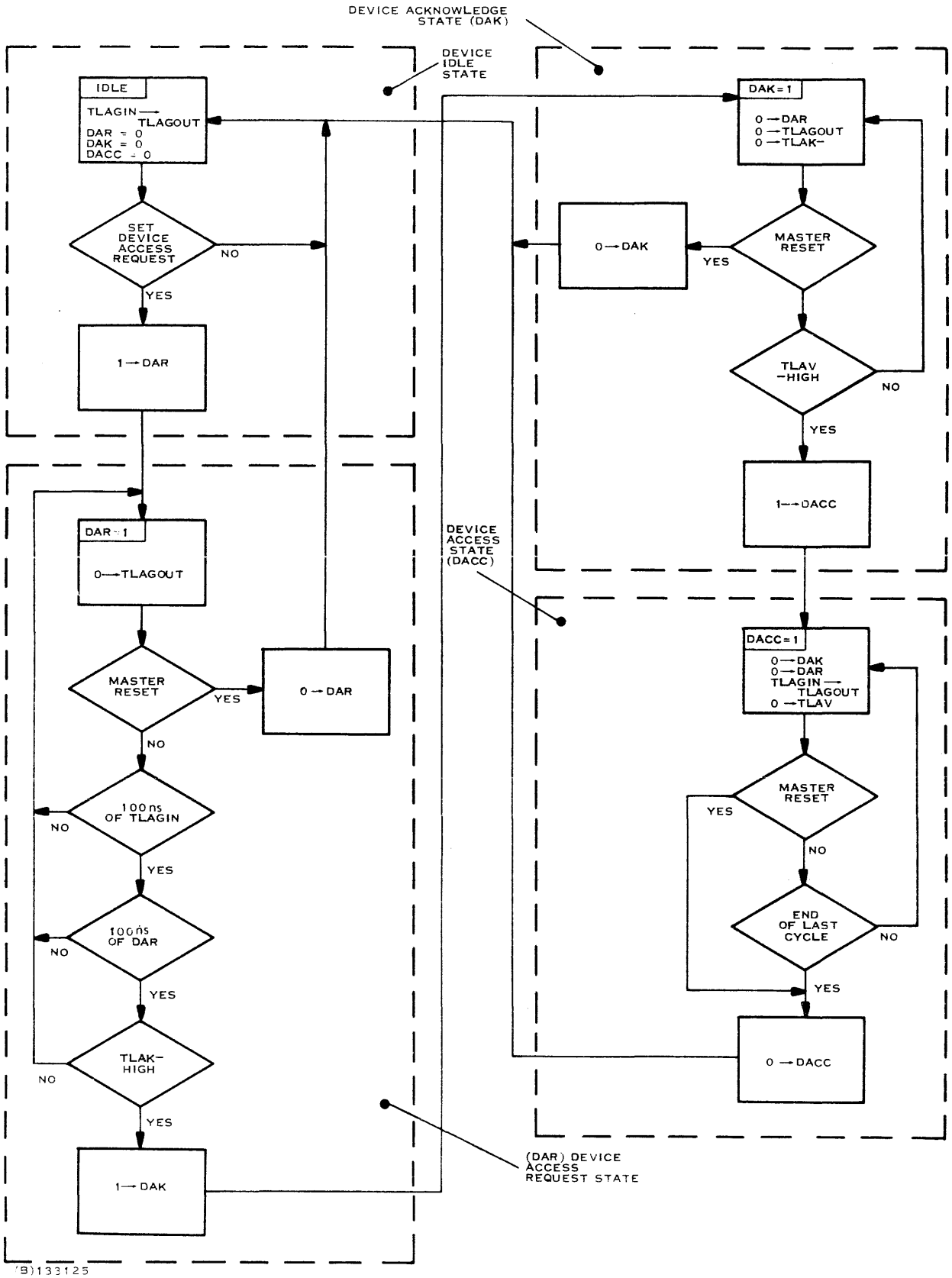


Figure G-5. TILINE MASTER Device Access Controller Flowchart

In the DACC state the TLAG signal is passed on to lower priority MASTER devices and the access controller pulls TLAV low. While in the DACC state the MASTER device has access to the TILINE and may perform data transfers as described previously under data transfers. During the last data transfer the MASTER device performs, it must generate a Last Cycle signal that clears DACC and causes the access controller to return to the IDLE state at the end of the data transfer. Most TILINE device controllers are designed to steal only one TILINE cycle at a time and the Last Cycle control is wired permanently high.

TILINE Special Purpose Functions. In addition to the TILINE signals associated with data transfers and those that establish priority for TILINE access, there are five special function signals. These signals are TILINE I/O Reset (TLIORES–), TILINE Power Failure Warning Pulse (TLPFWP–), TILINE Power Reset (TLPRES–), TILINE Wait (TLWAIT–), and TILINE Hold (TLHOLD–).

The TILINE I/O Reset (TLIORES–) signal is generated by the central processor during execution of its I/O Reset Instruction or in response to the programmer panel RESET switch. TLIORES– is a 100- to 500-nanosecond negative pulse on a normally high line. TLIORES– is also asserted whenever TLPRES– is asserted. TLPRES– is available to all devices connected to the TILINE. TLIORES– functions to halt and reset all TILINE I/O devices. The devices should reset in an orderly fashion in response to TLIORES– and any memory cycle in progress should be completed normally. For example, if a tape write is in progress an end of record sequence should occur. When a device is reset while active it must report abnormal completion status.

The TILINE Power Failure Warning Pulse (TLPFWP–) signal is generated by the power supply to indicate that a power shutdown is imminent. The signal is a low pulse that occurs at least 7.0 milliseconds before TILINE Power Reset (TLPRES–) occurs. The negative-going edge of this pulse causes the central processor to trap to the power failure trap location and the effect of the negative-going edge of TLPFWP– on connected TILINE I/O devices is the same as that of TLIORES–. TLPFWP– remains low until TILINE Power Reset is asserted.

The TILINE Power Reset (TLPRES–) is a normally high signal that goes low at least 10 microseconds before any dc voltage level from the power supply begins to fail due to normal shutdown or because of ac power failure. TLPRES– is generated by the power supply. TLPRES– remains low during and after a power failure. During ac power turn-on, TLPRES– remains at a low level until all dc voltages from the power supply are up and are stable. The purpose of TLPRES– is to reset all device controllers and the central processor during power failure and to directly inhibit all critical lines to external equipment that are powered by a separate power supply. For example, it is TLPRES– that prevents a tape deck from getting a rewind pulse when the central processor is powered up and down. During the power-up sequence, the TLPRES– resets all I/O controllers to their IDLE state and clears any device status information. As TLPRES– goes high indicating that power is up and stable, the central processor performs the power-up interrupt trap.

The TILINE Wait (TLWAIT–) is a normally high signal generated by TILINE Couplers that is used to resolve certain conflicts that can arise in computer-to-computer communication over the TILINE. The purpose of TLWAIT– is to directly disable (inhibit) the following signals from all TILINE MASTER devices (including central processors): TLGO–, TLREAD, TLADR–, and TLDAT–. Note, that these signals are not inhibited in SLAVE devices. The foregoing signals are disabled within 40 nanoseconds of the time that TLWAIT– is asserted and remain disabled as long as TLWAIT– stays low. This action should cause no state change in MASTER devices and except for its TILINE interface drivers, the MASTER device should be unaware that TLWAIT– has been asserted. TLWAIT– inhibits the MASTER device from "seeing" any TILINE Terminate

(TLTM–) or TILINE Memory Error (TLMER–) signals that occur and also holds the MASTER devices TILINE timeout timer reset. TLWAIT– allows TILINE Couplers to exercise a "higher than any" priority on the TILINE.

The TILINE Hold (TLHOLD–) is a normally high signal that is brought low by a central processor prior to the operand fetch of an ABS instruction. TLHOLD– remains low until the operand store cycle is complete or until the processor determines that the operand store is not needed. ABS is intended to be used as a software interlock. ABS reads a memory word, tests it, and then, if it was negative, subtracts it from zero and restores it to memory in its original location. In the use of ABS as a software interlock in multiprocessor systems it is possible for one processor to modify a memory word while another processor is performing an ABS instruction on that word. This interference ruins the usefulness of ABS as a software interlock. The asserted TLHOLD– prevents this interference by holding TILINE access for the processor performing ABS. TLHOLD– is used and propagated by TILINE Couplers in multiprocessor systems.

APPENDIX H

DETAILED DESCRIPTION OF CRU

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DETAILED DESCRIPTION OF CRU

H.1 COMMUNICATIONS REGISTER UNIT (CRU) INTERFACE

The direct command driven input/output interface for the processor is called the CRU. The CRU provides for up to 4096 directly addressable input bits and up to 4096 directly addressable output bits. Input and output operations can address each of the bits individually or in fields of from one to sixteen bits. The processor instructions that drive the CRU can set, reset, or test any bit in the CRU array, or the processor instructions can move data between memory and the CRU data fields.

H.1.1 LOGIC IMPLEMENTATION. Logic for the CRU is mounted on the system interface circuit board and this logic exerts control over the interface data and control lines. These lines are available to all main chassis location except for the two slot locations used by the processor board AU1 and the system interface board itself. Twenty four module select signals are decoded by CRU interface logic and are made available to 11 chassis locations when the 13-slot chassis is used. Only eight of the module select signals are used for the four available chassis locations used in the 6-slot chassis. Each chassis location (full-sized slot) accommodates one double-connector circuit board or two single-connector circuit boards.

H.1.2 MAIN CHASSIS IMPLEMENTATION. The minimum CRU implementation can be effected by installing an AU1 and an AU2 circuit board into a 990 family chassis/power supply assembly. This combination is defined as a main chassis and can be implemented with either a 7-inch chassis that has a maximum of four available full-sized slots or with a 12-inch chassis that has a maximum of 11 available full-sized slots. Each full-sized slot has the capability to implement a maximum of 32 input/output bits using the module select decodes provided. Main chassis CRU addresses begin at 000_{16} and extend to a maximum of $09F_{16}$ for the 7-inch chassis and to a maximum of $17F_{16}$ for the 12-inch chassis. If the main chassis contains a memory circuit board, the number of available full-sized CRU chassis slots is reduced accordingly.

H.1.3 STANDARD CRU EXPANSION IMPLEMENTATION. If a computer system requires more CRU slots than are available in the main chassis, then from one to seven 13-slot CRU expansion chassis can be added. A CRU address map for the standard expansion implementation is shown in figure H-1. The hardware required for the standard CRU expansion implementation is as shown in figure H-2. One 26-conductor ribbon cable is required to connect each expansion chassis. The chassis and backpanels used in the expander chassis are identical to those used for the 12-inch main chassis. The expander board installed in the main chassis contains line drivers and receivers for the expansion cables. The buffer board installed in each expansion chassis decodes module select signals, contains buffers and receivers for the CRU address and data, and additionally generates clock signals for the expander chassis cards. The buffer board also implements an interrupt scanner for up to 32 interrupts per expansion chassis. Software can use the interrupt scanner to construct vectored interrupts for each slot of the expander chassis and eliminate the need to poll devices to determine the source of the interrupt.

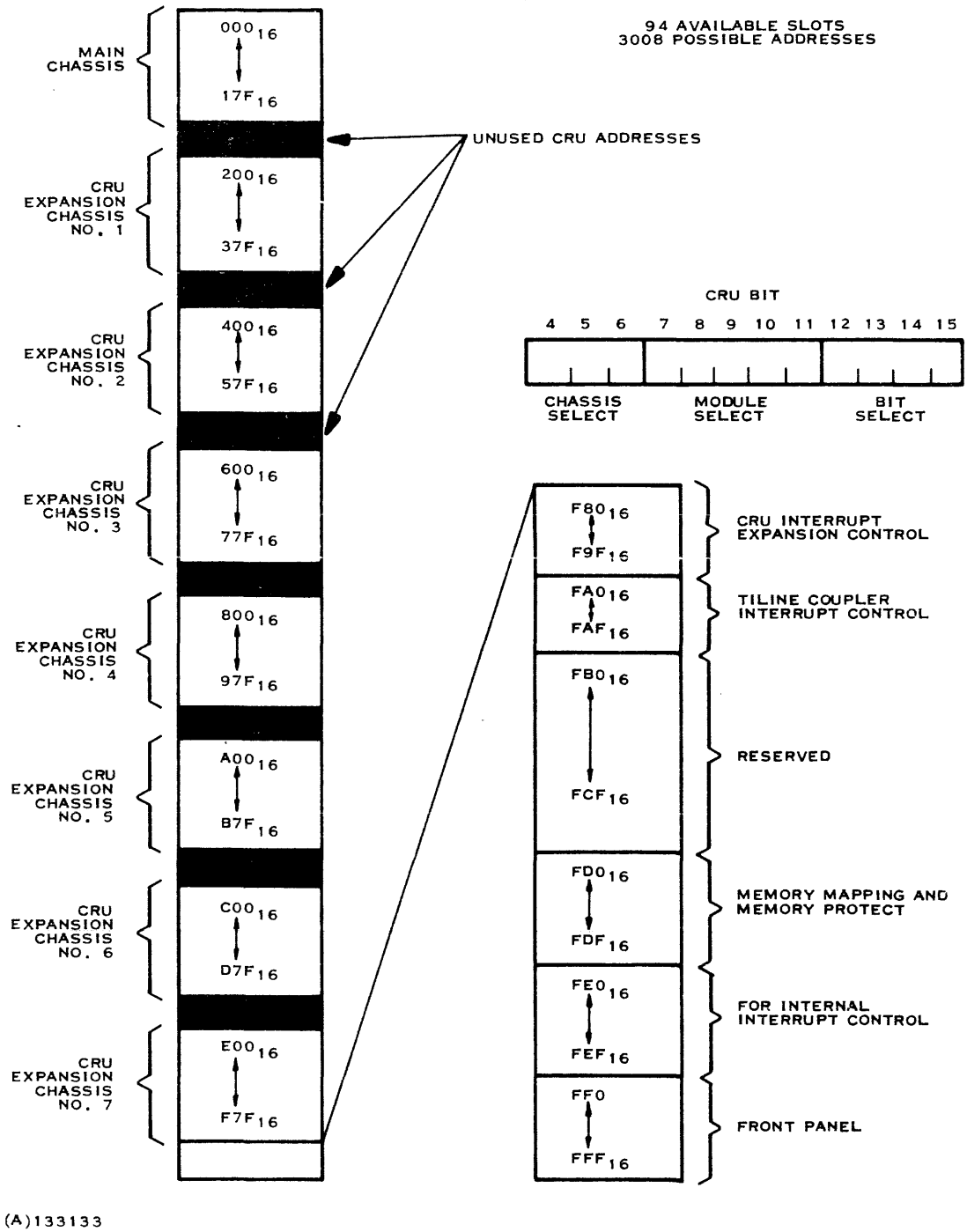

Figure H-1. CRU Address Map for Standard Expansion Implementation Using 13-Slot Chassis

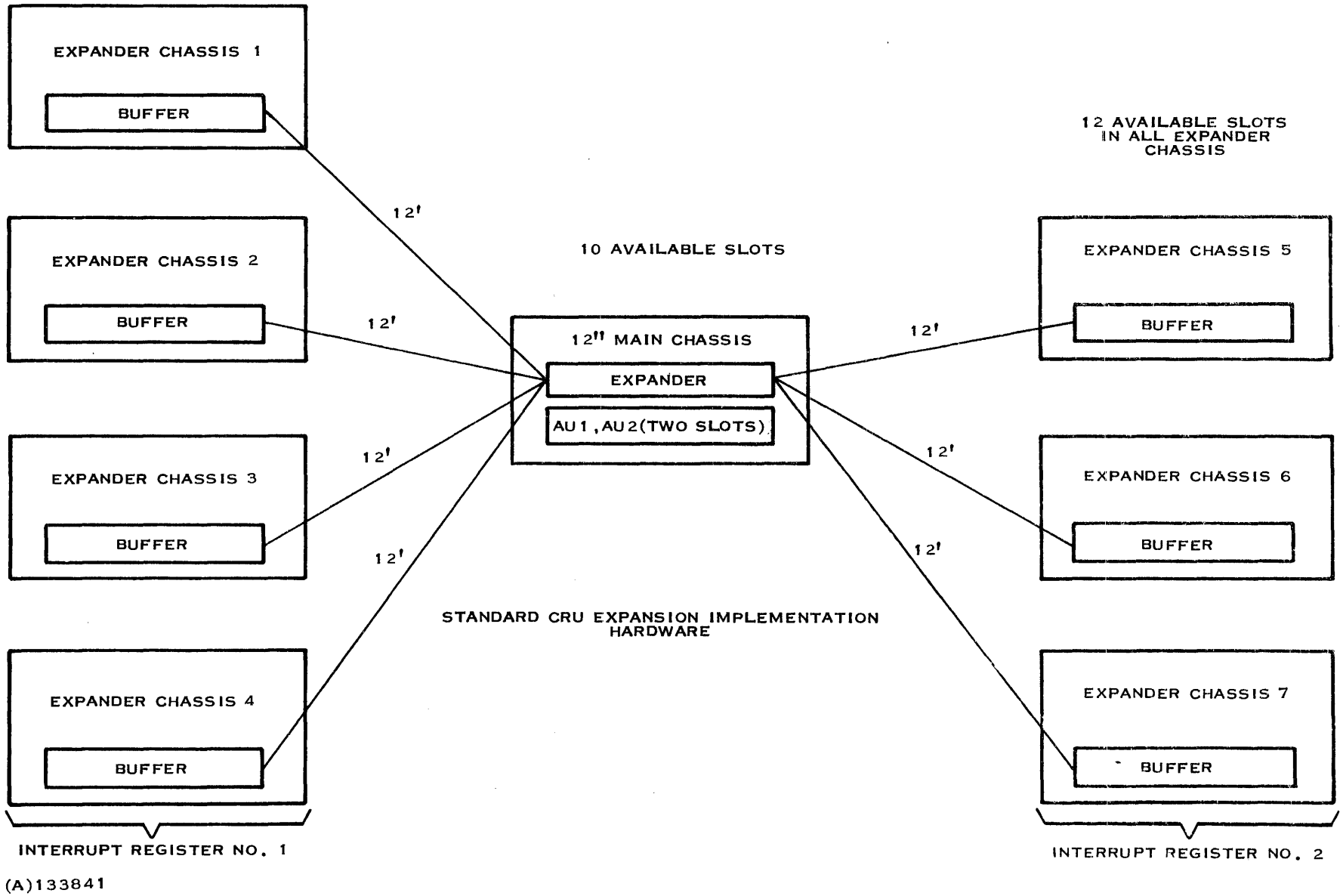

Figure H-2. Standard CRU Expansion Implementation Hardware

H.1.4 CRU APPLICATIONS. Because of its extremely flexible data format, the CRU interface can be used effectively for a wide range of control and data operations. These applications can be divided into two broad categories: those involving a single control bit transfer, and those requiring input or output of a word of several data or status bits.

H.1.4.1 Single-Bit Operations. Single-bit operations typically involve the computer sampling a status bit. When the status bit sets, the computer responds by setting a control bit or by transferring to a different set of instructions. This operation is exemplified by a communications interface unit that generates a single interrupt for one of several reasons such as output complete, input complete, or line status change. An output or input complete requires a transfer to instructions that perform another output or input operation. A line status change might require the setting of a control output or the transfer to instructions that handle the change in other ways.

H.1.4.2 Multiple-Bit Operations. Multiple-bit operations typically involve a data input device such as a keyboard or card reader, or an output device such as a display or card punch. An interrupt from the device causes the processor to perform a store communications register (STCR) instruction to read data from the CRU device and store it into memory. Similarly, to output data to the device the processor executes a load communications register (LDCR) instruction to fetch data from memory and transfer it to the CRU device.

H.2 CRU INTERFACE SIGNALS

Logic on the system interface board impiements a dedicated CRU interface for the programmer panel and also the standard CRU interface for the main chassis. The interface signals to the main chassis are effected at the bottom edge connectors, P1 and P2, of the system interface board. A simplified logic diagram of the CRU interface that shows the interface signals to the main chassis is provided in figure H-3. Table H-1 provides the function of each of the CRU interface signals, the pin numbers of the signals on the system interface board that installs in main chassis slot designated slot 1, and the pin numbers of the signals as they appear on the backpanel chassis slots of either the main chassis or an expansion chassis. These chassis slots are designated slots 2 through 6 for a 6-slot chassis and 2 through 13 for a 13-slot chassis. Both connectors in each chassis slot are furnished with the CRU bit select bits (CRUBIT 12-15) and other CRU interface signals that permit each connector to address 16 bits of the CRU. Connector P1 in a chassis slot receives one module select signal corresponding to one 16-bit register whereas connector P2 receives two module select signals and thus may address up to 32 bits of the CRU. Connector P1 also receives the eight most significant bits of the CRU address thus permitting the chassis slot to be used for a CRU expansion driver or for modules that ignore module select signals to directly decode their own CRU address.

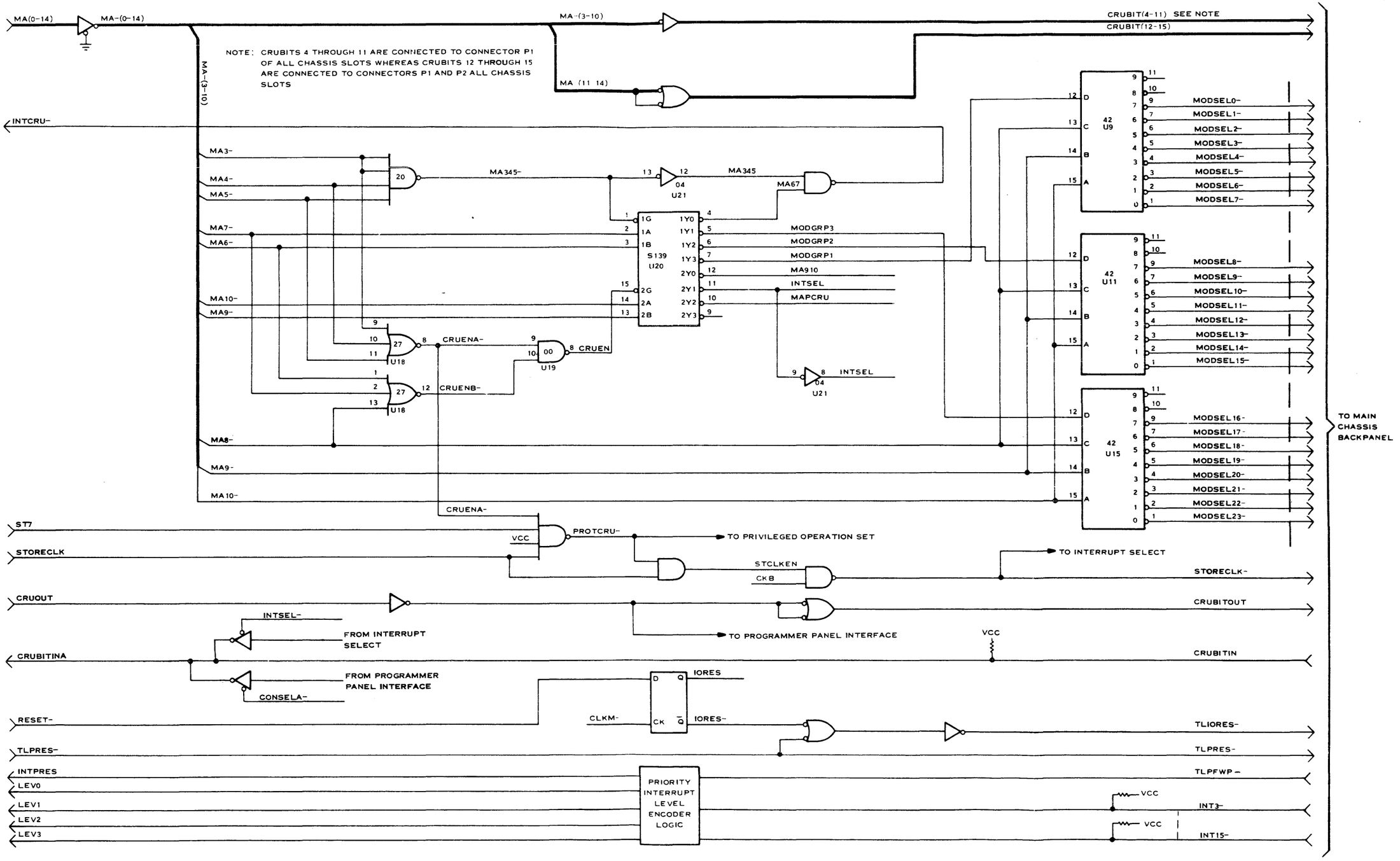

Figure H-3. Simplified Logic Diagram of CRU Interface Implementation

Table H-1. CRU Interface Signals

Signature	990/4 Circuit Board Pin Number	Main or Expansion Chassis Backpanel Pin Number	Function
MODSEL0-	P1-23	Slot 13, P2-48	Module select signals generated by the microprocessor from address bits 7-11 (CRUBITS 8-11) for use within the main or an expansion chassis. Note that P1 in each slot of the backpanel receives one module select signal whereas P2 receives two module select signals. This configuration permits P2 to use 32 bits of the CRU. Note that pin 48 of successive P2 connectors in the chassis slots are connected to even-numbered module select signals and at the CRU circuit board level carries a MODSELA– signature. Pin 46 of successive P2 connectors in the chassis slots are connected to pin 48 of P1 of that slot and then to an odd-numbered module select signal and carries a signature of MODSELB–. Pin P1-48 is not used when a full-sized CRU circuit board is implemented in a chassis slot. MODSEL signal lines will drive 10 TTL loads.
MODSEL1-	P1-35	Slot 13, P1-48 and P2-46	
MODSEL2-	P1-37	Slot 12, P2-48	
MODSEL3-	P1-43	Slot 12, P1-48 and P2-46	
MODSEL4-	P1-44	Slot 11, P2-48	
MODSEL5-	P1-45	Slot 11, P1-48 and P2-46	
MODSEL6-	P1-46	Slot 10, P2-48	
MODSEL7-	P1-47	Slot 10, P1-48 and P2-46	
MODSEL8-	P1-48	Slot 9, P2-48	
MODSEL9-	P1-49	Slot 9, P1-48 and P2-46	
MODSEL10-	P1-51	Slot 8, P2-48	
MODSEL11-	P1-53	Slot 8, P1-48 and P2-46	
MODSEL12-	P1-61	Slot 7, P2-48	
MODSEL13-	P1-67	Slot 7, P1-48 and P2-46	
MODSEL14-	P1-69	Slot 6, P2-48	
MODSEL15-	P1-76	Slot 6, P1-48 and P2-46	
MODSEL16-	P2-38	Slot 5, P2-48	
MODSEL17-	P2-36	Slot 5, P1-48 and P2-46	
MODSEL18-	P2-34	Slot 4, P2-48	
MODSEL19-	P2-32	Slot 4, P1-48 and P2-46	
MODSEL20-	P2-22	Slot 3, P2-48	
MODSEL21-	P2-18	Slot 3, P1-48 and P2-46	
MODSEL22-	P2-16	Slot 2, P2-48	
MODSEL23-	P2-13	Slot 2, P1-48 and P2-46	
CRUBIT4	P1-56	P1-56	Address bit generated by the microprocessor to select a particular chassis (bits 4-6), a 16-bit module within that chassis (bits 7-11), and a particular bit from that module (bits 12-15). CRUBITS 4-11 are capable of driving at least 12 normalized TTL loads, CRUBITS 12-15 are capable of driving 30 normalized TTL loads.
CRUBIT5	P1-54	P1-54	
CRUBIT6	P1-52	P1-52	
CRUBIT7	P1-50	P1-50	
CRUBIT8	P1-62	P1-62	
CRUBIT9	P1-64	P1-64	
CRUBIT10	P1-68	P1-68	
CRUBIT11	P1-70	P1-70	
CRUBIT12	P1-36	P1-36, P2-36	
CURBIT13	P1-32	P1-32, P2-32	

Table H-1. CRU Interface Signals (Continued)

Signature	990/4 Circuit Board Pin Number	Main or Expansion Chassis Backpanel Pin Number	Function
CRUBIT14	P1-38	P1-38, P2-38	
CRUBIT15	P1-34	P1-34, P2-34	
CRUBITOUT	P1-18	P1-18, P2-18	Serial data line for transfer of data from the microprocessor to the addressed CRU bit(s). This line is active only when STORECLK– goes low. (This line will drive 30 normalized TTL loads.)
CRUBITIN	P1-60	P1-60, P2-60	Serial data line for transfer of data from the addressed CRU bit(s) to the microprocessor. This line must be driven by an open collector gate and only when the module is selected. A 470-ohm pull-up resistor is mounted on the 990/4 circuit board for this line.
STORECLK-	P1-22	P1-22, P2-22	An active-when-low pulse that indicates to the selected CRU module that the operation is a write (Set Bit or LDCR) operation. This pulse transfers the data on the CRUBITOUT line into a holding flip-flop that is the CRU bit. (Will drive 30 TTL loads.)
TLIORES-	P1-14	P1-14, P2-14	I/O Reset: A normally high signal that, when low, resets all connected devices. This signal is a minimum 250 nanoseconds pulse that is generated by a RSET instruction in the microprocessor. This signal is also low until dc power is up and stable. (Will drive 30 TTL loads.)
TLPFWP-	P1-16	P1-16, P2-16	Power Failure Warning Pulse: A low signal of at least 7.0 milliseconds duration that indicates that a power failure is imminent. (Will drive 30 TTL loads.)
TLPRES-	P1-13	P1-13, P2-13	Power Reset: A normally high signal that goes low to reset connected devices at least 10 microseconds before dc voltages begin to fail during power down.

APPENDIX I

ECC 16KB EXPANSION BOARD TO ADD-ON BOARD INTERFACE SIGNALS

ECC 16KB Expansion Board to Add-On Board Interface Signals

Signature	Pin No.	Definition
MDO00–	P4-51	Memory read data output from Add-On Board to ECC 16KB Expansion Board
MDO01–	P4-43	
MDO02–	P4-35	
MDO03–	P4-27	
MDO04–	P4-19	
MDO05–	P4-13	
MDO06–	P4-09	
MDO07–	P4-05	
MDO08–	P4-04	
MDO09–	P3-75	
MDO10–	P3-71	
MDO11–	P3-63	
MDO12–	P3-55	
MDO13–	P3-47	
MDO14–	P3-39	
MDO15–	P3-31	
C0OUT–	P3-23	Error correcting code output signals from Add-On Board during Read operation
C1OUT–	P3-17	
C2OUT–	P3-13	
C3OUT–	P3-09	
C4OUT–	P3-05	
C5OUT–	P3-04	
MDI00	P4-53	Memory write data inputs from ECC 16KB Expansion Board to Add-On Board.
MDI01	P4-45	
MDI02	P4-37	
MDI03	P4-29	
MDI04	P4-21	
MDI05	P4-15	
MDI06	P4-11	
MDI07	P4-07	
MDI08	P4-03	
MDI09	P3-77	
MDI10	P3-73	
MDI11	P3-65	
MDI12	P3-57	
MDI13	P3-49	
MDI14	P3-41	
MDI15	P3-33	
C0IN	P3-25	Error correcting code inputs to Add-On Board during write operation.
C1IN	P3-19	
C2IN	P3-15	
C3IN	P3-11	
C4IN	P3-07	
C5IN	P3-03	

Signature	Pin No.	Definition
ADR08 ADR09 ADR10 ADR11 ADR12 ADR13 ADR14 ADR15 ADR16 ADR17 ADR18 ADR19	P4-67 P4-61 P4-69 P4-73 P4-77 P4-75 P4-57 P4-55 P4-59 P4-65 P4-63 P4-71	Least significant 12 bits of address from TILINE bus used as a store or fetch address when accessing a memory location. The most significant 6 bits of this address can also be generated internal to the controller for use during refresh cycles.
DECODEA DECODEB DECODEC	P4-78 P4-76 P4-74	A 3-bit code that indicates which bank (0-7) of memory chips is to be cycled. DECODEA is the least significant and DECODEC is the most significant bit of the code.
XMEM4– XMEM8– XMEM16–	P3-27 P3-29 P3-21	A 3-bit complement code, hardwired in the Add-On Board, that designates to the memory controller the size of the memory contained on the Add-On Board. Valid codes are: XMEM 16- 8- 4- 1 0 1 16KB memory 0 1 1 32KB memory 0 0 1 48KB memory
START	P4-70	Initiates a memory cycle in the Add-On Board
RFACC–	P4-68	When coincident with START, this signal initiates a refresh cycle in the Add-On Board
READ	P4-64	When a logic one, this signal indicates that a read cycle is to be performed from the address on the ADR__ lines. When this line is a logic zero, the Add-On Board performs a write operation.
PWRON	P3-37	When a logic one, this signal applies +5 Vdc to the Add-On Board logic; when a logic zero, this signal removes power from the logic.
PWRONA	P4-66	This signal is a logic zero during power on or off transitions and disables the clock input to the memory chips to prevent voltage spikes from affecting the memory chips. During normal power conditions, this signal is a logic one.
ERROR–	P3-67	A low active signal that indicates a noncorrectable error in data from the Add-On Board and lights an LED on the Add-On Board to indicate that condition.
CERR–	P3-43	A low active signal that indicates a corrected error in data from the Add-On Board. This signal also lights an LED on the Add-On Board to indicate that condition.
DECENB	P4-72	A high active signal that enables the Add-On Board to decode the DECODEA, B,C lines to select a 4K bank of memory on the Add-On Board.

APPENDIX J

96KB MEMORY CONTROLLER BOARD TO 256KB ADD-ON MEMORY ARRAY BOARD INTERFACE SIGNALS

APPENDIX J

96KB MEMORY CONTROLLER BOARD TO 256KB ADD-ON MEMORY ARRAY BOARD INTERFACE SIGNALS

Signature	Pin No.	Definition
MB00–	P4-1	22-bit bi-directional data bus that transfers read and write data between the two boards (includes six check bits MB16– through MB21–).
MB01–	P4-3	
MB02–	P4-5	
MB03–	P4-7	
MB04–	P4-9	
MB05–	P4-11	
MB06–	P4-13	
MB07–	P4-15	
MB08–	P4-17	
MB09–	P4-19	
MB10–	P4-21	
MB11–	P4-23	
MB12–	P4-25	
MB13–	P4-27	
MB14–	P4-29	
MB15–	P4-31	
MB16–	P4-33	
MB17–	P4-35	
MB18–	P4-37	
MB19–	P4-39	
MB20–	P4-41	
MB21–	P4-43	
IBSEL–	P3-19	Board selected signal. The select signal is sent to the 96KB memory controller board controller when the 256KB add-on memory array board decodes a TILINE address that falls in the address space defined by the address switches and memory size jumpers.
IR/W–	P3-21	Read-write control. The read-write control line to the 256KB add-on memory array board specifies either a read or write memory operation.
ADODD	P3-29	Odd word address. The address odd line operates in conjunction with the read-write control line to enable both rows in a selected bank during a read operation or to enable only the required odd or even row during a write operation.
IRAS–	P3-13	Row address strobe. The row address strobe clocks seven row address bits into the memory chips.
ICADSEL	P3-7	Column address select. The column address select line causes the second seven address bits to be applied to the memory chips.

Signature	Pin No.	Definition
ICAS–	P3-15	Column address strobe. Column address strobe clocks the seven column address bits into the memory chips.
RFAD0– RFAD1– RFAD2– RFAD3– RFAD4– RFAD5– RFAD6–	P3-27 P3-33 P3-17 P3-35 P3-25 P3-23 P3-31	Refresh address lines. Refresh address lines provide the row address to the memory chips during a refresh operation.
REFRESH–	P3-5	Refresh cycle in progress. The refresh control line causes the refresh address lines to be applied to the memory chips that are then strobed into the memory chips by the IRAS– pulse.
+5 SWEN–	P3-1	Five volt switch enable. Turns on 5 volts power to 256KB add-on memory array whenever main power is on or during a refresh operation during standby operation.
POWERON–	P3-11	Power on. Power on is true after 5 volts is stable. When false, this signal inhibits extraneous strobes to the memory chips.
IORES–	P3-37	I/O reset. The reset line resets the error indication lamps after initial power-up and in response to a front panel reset or execution of a reset instruction.
IMERR–	P3-3	Memory error, multibit error. Memory error is generated by the control logic of the 96KB memory controller board during a read cycle and sets the error indication lamp on the selected 256KB add-on memory array board.
ICERR–	P3-9	Correctable error, one bit error detected. The correctable error signal is generated by the control logic of the 96KB memory controller board during a read cycle to indicate a one bit error has occurred and sets the error indication lamp on the selected 256KB add-on memory array board.

ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

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The index, table of contents, list of illustrations, and list of tables are used in conjunction to obtain the location of the desired subject. Once the subject or topic has been located in the index, use the appropriate paragraph number, figure number, or table number to obtain the corresponding page number from the table of contents, list of illustrations, or list of tables. The table of contents does not contain four-level paragraph entries. Therefore, for four-level paragraph numbers such as 2.3.1.2, use the three-level number and the corresponding page number. In this case, the three-level number is 2.3.1.

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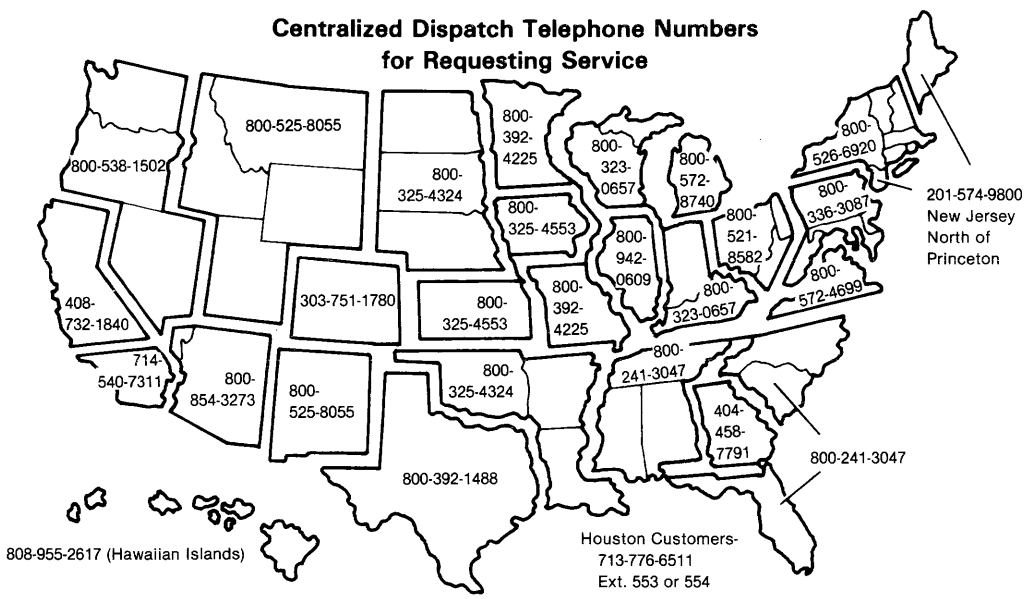

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