SPERRY RAND

UNIVAC

418-III

REAL-TIME SYSTEM

PROCESSOR AND STORAGE

PROGRAMMERS REFERENCE

UP-7627

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1. INTRODUCTION

This document describes the three individual hardware components of the UNIVAC 418-III Real-Time System. These hardware sections and the order of their presentation are as follows:

- Main Storage
- Command/Arithmetic Section
- Input/Output Section

Section 2 of this manual describes main storage and discusses the interfacing between it, the Command/Arithmetic, and the Input/Output sections. In Section 3 the Command/Arithmetic Section is discussed in more detail, and Section 4 describes the Input/Output Section.

2. MAIN STORAGE

Main storage is divided into four banks each consisting of one or two modules. Each module has four bays, each containing 4096 eighteen-bit words of storage. The UNIVAC 418-III main storage is divided into 18-bit addressable words. Up to 131,072 words (4 banks, 2 modules each) may be addressed by the Command/Arithmetic section. Each storage bank has three access paths, one to the Command/Arithmetic (C/A) Section and one to each Input/Output Module (IOM). In this manner, parallel access to storage may be obtained by the C/A and each IOM whenever each references a different storage bank. Regardless of the physical distribution of various modules, addressing is always continuous.

Figure 2-1 illustrates the parallel paths available to each bank. If any bank is being accessed by two or more of the access paths, only one at a time is honored.

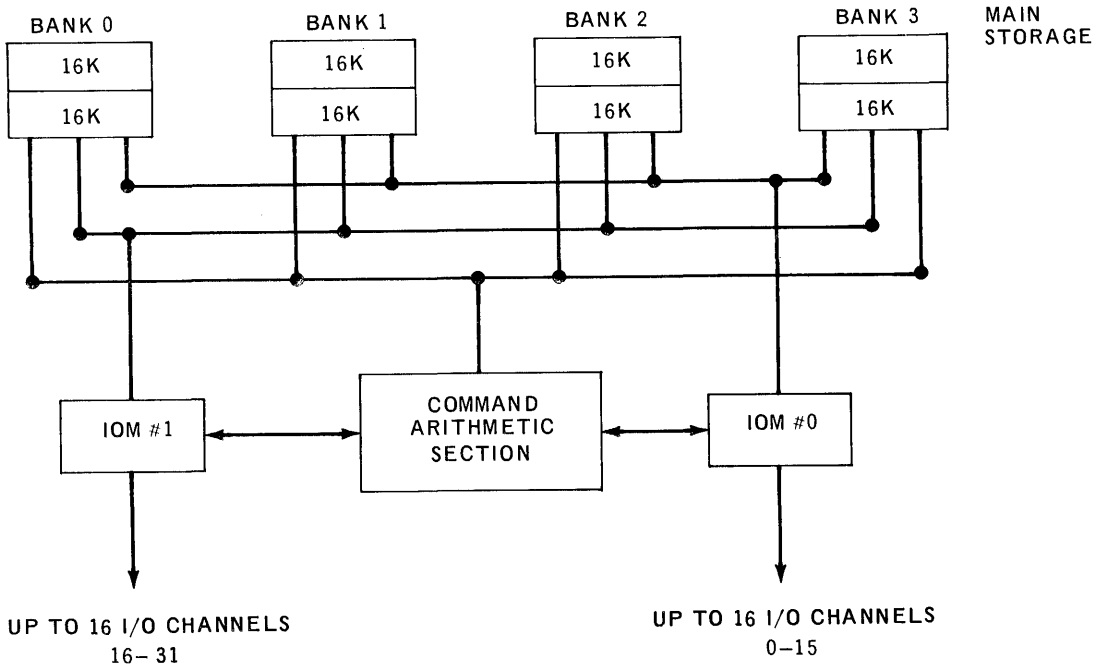


Figure 2-1. Main Storage Allocation

In addition to the ferrite core storage, the UNIVAC 418-III System uses several high speed integrated general registers (IGR) located in the IOM's. Read/restore cycle time for main storage is 750 nanoseconds, and for integrated storage, 186 nanoseconds. These IGR registers are assigned fixed addresses which duplicate the corresponding core storage addresses. Locations 300_8 through 477_8 are the corresponding IGR and core storage locations. The C/A section accesses the IGR storage whenever an address in this range is specified, whereas the I/O sections address the corresponding core storage locations.

3. COMMAND/ARITHMETIC SECTION

3 1. INTRODUCTION

The Command/Arithmetic Section (C/A section) consists of the hardware necessary to enable certain functions to be performed whenever it is given control. These functions are obtained from main storage as are the necessary operands.

In addition to having access to main storage, the C/A section has certain storage registers and designators which allow it to perform its various functions. These are described only to the extent necessary for the programmer to understand how the hardware works.

Appendix D summarizes the instruction repertoire for the UNIVAC 418-III System. For a detailed description of each function, refer to *UNIVAC 418-III Assembler, Programmers Reference Manual, UP-7599* (current version).

3.2. REGISTERS

The following is a brief description of the registers of the C/A section.

- Instruction Address Register

  The Instruction Address Register (IAR) contains the address of the next instruction to be performed. The IAR is not program accessible.

- Arithmetic Accumulators

  There are two arithmetic accumulators, A Upper (AU) and A Lower (AL), which can be operated upon under program control. Each accumulator is 18 bits long: they can be used jointly as one 36-bit accumulator (A register).

- Index Registers

  Eight Index Registers are available for use (only one at a time) as address modifiers. The index registers are program accessible and are storage locations 1_8 through 10_8.

- B Register

  The B Register contains the contents of the active index register and is used by the hardware whenever an indexed instruction is executed. The B Register is not program accessible.

- Index Register Pointer

  The Index Register Pointer contains the main storage address of the currently active index register.

- Special Register

  The Special Register (SR) is used to specify interbay (4K storage segment) addressing. The SR contents are under program control. (See 3.5 for description of SR operation.)

- K0 Register

  The K0 register is used for internal purposes and is not accessible to programmed instructions; it may be inspected from the maintenance panel. During the execution of a shift instruction, K0 contains the shift count.

- Z Register

  The Z register is used for internal purposes and is not accessible to programmed instructions; it may be inspected from the maintenance panel. For most instructions, Z contains the operand address.

- Storage Limits Registers

  Two 9-bit registers, called Storage Limits Upper and Storage Limits Lower, are used to contain the addresses of the upper and lower boundaries of an area which is protected by the Guard Mode. An area so placed under Guard Mode becomes the only area in which the C/A section may cause the contents of any location to be changed. The Storage Limits Registers are loaded as a result of the LGM instruction.

3.3. DESIGNATORS

The following is a description of the designators of the C/A section.

- Compare Designator

  The Compare Designator is a bi-stable, three-stage register whose state is determined by the execution of any of the COMPARE instructions (f = 02, 03, 06, 07). The results of the COMPARE instructions are recorded by the Compare Designator as follows:

  - The COMPARE stage is set upon the execution of any of the COMPARE instructions.

  - The LESS THAN stage is set if a COMPARE instructions finds (AL) less than the contents of the addressed storage location (f = 02, 03), or [(AU) AND (AL)] less than the logical product of (AU) and the contents of the address storage location (f = 06, 07).

  - The EQUALS stage is set if a COMPARE instruction finds (AL) equal to the contents of the addressed storage location (f = 02, 03) or [(AU) AND (AL)] equal to the logical product of (AU) and the contents of the addressed storage location (f = 06, 07).

The COMPARE stage is cleared by the execution of any instruction other than the arithmetic JUMP instructions (f = 60 through 67). Thus, if the results of a COMPARE instruction are to be successfully tested, it must be immediately followed by one or more of the JUMP instructions.

When the COMPARE stage of the Compare Designator is set, or while processing a COMPARE instruction, all interrupts are locked out to avoid the possibility of inadvertently clearing the COMPARE stage. It should be noted that the arithmetic JUMP instructions have significantly different operations if executed when the COMPARE stage is not set.

- Borrow Designator

  The Borrow Designator is a bi-stable, single-stage element whose state is determined by the execution of either a double-length ADD instruction (f = 20, 21), or a double-length SUBTRACT instruction (f = 22, 23). If an end-around borrow would be required during the execution of either of these instructions, it is inhibited and the Borrow Designator is set. The Borrow Designator remains set until the subsequent execution of another double-length ADD or double-length SUBTRACT instruction.

  The condition of the Borrow Designator may be tested by the TEST NO BORROW instruction (f = 5051). When the Borrow Designator is set, interrupts are not locked out.

- Overflow Designator

  The Overflow Designator is a bi-stable, single-stage element which is set when an overflow occurs during the execution of any of the following instructions:

  ADD AL (f = 14, 15)
  SUBTRACT AL (f = 16, 17)
  ADD A (f = 20, 21)
  SUBTRACT A (f = 22, 23)
  DIVIDE A (f = 26, 27)
  ROUND A (f = 5060)
  ADD AL PLUS CONSTANT (f = 71)
  FLOATING POINT DIVIDE (f = 5005)

  The state of the Overflow Designator is tested by either the TEST OVERFLOW instruction (f = 5052) or the TEST NO OVERFLOW instruction (f = 5053). The execution of either instruction automatically clears the Borrow Designator. When the Overflow Designator is set, interrupts are not locked out.

- Guard Mode Designator

  The Guard Mode Designator is a bi-stable, single-stage element set as a result of the LGM (f = 5065) instruction. When the Guard Mode Designator is set by the LGM instruction, any write reference to the storage area outside of the limits set, with the exception of addresses 00_8 through 17_8, will cause a Guard Mode Interrupt. If a privileged instruction is attempted while in Guard Mode, the function will be inhibited and a Guard Mode Interrupt will be generated. The generation of any interrupt will release Guard Mode and clear the Guard Mode Designator.

3.4. INSTRUCTION TYPES AND FORMATS

Instructions for the UNIVAC 418-III System have two parts, the function field and the operand field. The contents of the function field indicates to the C/A section which operation is to be performed; the contents of the operand field supplies the C/A section

with the necessary information to enable it to perform the function. The instruction repertoire is the set of all recognized functions.

The UNIVAC 418-III instructions fall into three distinct types, designated I, II, and III. Type I instructions are identified by function codes 02 through 27, 32, 33, and 40 through 47. Type II instructions are identified by function codes 30, 31, 34 through 37, and 51 through 76. Type III instructions are identified by function codes 5000 through 5077.

- Type I Instructions

  The Type I instruction format is:

  where: f is the six-bit function code

  u is the 12 low-order bits of the operand address.

- Type II Instructions

  The Type II instruction format is:

  where: f is the six-bit function code

  u is the 12 low-order bits of the operand address

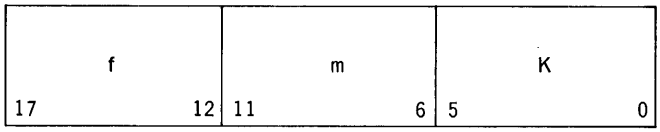
  z is the 12 low-order bits of an 18-bit sign-extended operand.

  When f indicates that the 12 low-order bits are to be interpreted as the actual operand, the 18-bit operand is formed by using z and propagating the contents of bit 11 to the six high-order bits. This is commonly referred to as sign extension.

- Type III Instructions

  The characteristic of a Type III instruction is the use of a major function code of 50 and a minor function code between 00 and 77. Type III instructions may be subdivided into two distinct categories, each with a slightly different format.

Type III-a

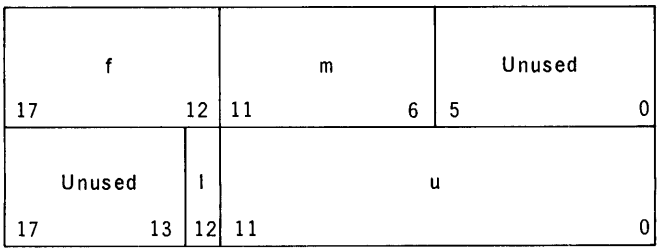


where: f is 50

m is the minor function code

K is zero or a constant less than 64.

Type III-b



where: f is 50

m is the minor function code

I is 0 if indexing is not used

I is 1 if indexing is used

u is the 12 low-order bits of the operand address.

Type III-b instructions are 2-word (36-bit) instructions.

In addition to the foregoing formats there are several Type III-a instructions which use the contents of one or more storage locations following their occurrence for specific data. These are principally the I/O instructions. Control is transferred to the storage location following the data words used by them.

3.5. ADDRESSING

The operand fields of Type I, Type II, and Type III-b instructions contain 12 bits. The UNIVAC 418-III main storage is logically divided into bays, each containing 4096 eighteen-bit words, and may be expanded to a maximum of 32 bays; therefore, each Type I, Type II, or Type III-b instruction provides sufficient space to specify any address within a bay. The bay which contains the desired address is determined by certain rules outlined in the following discussion.

When an instruction is executed which is in the last storage location of a bay, program control passes to the first location of the next bay unless it is a skip or jump type

instruction. If it is a skip type instruction, control passes to the first or second location of the next bay depending on whether or not the skip condition is met. If it is a jump type instruction, control passes to the storage location specified in the next bay. This is tantamount to saying that as long as forward jumps are made, it does not matter where the instruction is located in storage.

In order to enable certain instructions to access any address in storage, the SR (Special Register) may be used to specify which bay is to be used. The Special Register is active or inactive depending on whether bit 4 is set to one or to zero; bit 4 is not a part of the bay identification. Bits 5 and 3 through 0 of SR are the bay bits.

Example:

To set the SR active to bay 25 (31_8), the binary number

5	4	3	2	1	0
1	1	1	0	0	1

(71_8) must be stored in SR because bit 4 (SR active bit) must be set to 1. The desired address is derived by ignoring bit 4 and treating bit 5 as though it were in bit position 4. By doing this, 71_8 becomes 31_8 ($111001_2 \rightarrow 11001_2$).

To set the SR active to bay 5 (5_8), the binary number

5	4	3	2	1	0
0	1	0	1	0	1

(25_8) must be stored in SR.

In order to set the Special Register active to bay 3, the instruction

```
LABEL          OPERATION          OPERAND                    COM
1         10        20        30        40        50
          LSR       023
```

is executed. To set it active to bay 31 (32nd bay), the instruction

```
          LSR       077
```

is executed. To inactivate the Special Register the instruction

```
          LSR       0
```

may be executed.

When the C/A section makes reference to the storage location corresponding to the index register specified in the IRP, the B Register is accessed instead (see 3.2).

When the C/A section makes reference to the addresses 300_8 through 477_8, the contents of the corresponding IGR storage location is accessed instead.

- Type I Instructions

  Type I instructions are SR-sensitive and indexable, meaning that if SR is active, the bay specified by its contents is accessed, and that the contents of the active index register are used to modify the operand address if the function code is odd.

  If SR is not active (bit 4 is zero), the bay to be accessed is that in which the instruction itself resides; the bay bits are taken from the five high order bits of the Instruction Address Register.

If the function code (f) is odd, indexing is specified. This means that the full 18-bit contents of the active index register are arithmetically added to the (positive) 17-bit operand address. Figure 3-1 illustrates the various addressing techniques for Type I instructions.

LABEL	OPERATION	OPERAND	COMMENTS
	LSR	0	. LINE 1
	LL	0100	. LINE 2
	LSR	023	. LINE 3
	LL	0100	. LINE 4
	LSR	0	. LINE 5
	LB	(0300000)	. LINE 6
	LL	*0100	. LINE 7
	LSR	020	. LINE 8
	LL	*0100	. LINE 9
	LSR	023	. LINE 10
	LL	*0100	. LINE 11
	LSR	0	. LINE 12
	LB	(-0100000)	. LINE 13
	LL	*0100	. LINE 14

Figure 3-1. Type I Instruction Addressing Techniques

If line 1 were to be located at address 020000, the following storage references would be made:

LINE NO.	EFFECTIVE U	ADDRESS REFERENCED
2	0100 + 020000	020100
4	0100 + 030000	030100
7	0100 + 020000 + 030000	050100
9	0100 + 000000 + 030000	030100
11	0100 + 030000 + 030000	060100
14	0100 + 020000 – 010000	010100

- Type II Instructions

Type II instructions are never SR sensitive, differing in this respect from Type I instructions. Regardless of the contents of SR, the bay referenced is the one in which the instruction resides.

Some Type II instructions are index sensitive; this allows them to access other bays by using the active index register to modify the address obtained by combining U_{11-0} and IAR_{17-12}.

Three instructions (LBK, LLK, and ALK) do not make a second storage access. The sign-extended value of the operand field is used as the operand.

- Type III instructions

The Type III-a instructions do not require an operand. The Type III-b instructions resemble the Type I instructions: they are SR and index sensitive. When I is set to 1, indexing is used: when it is set to 0, no indexing is used.

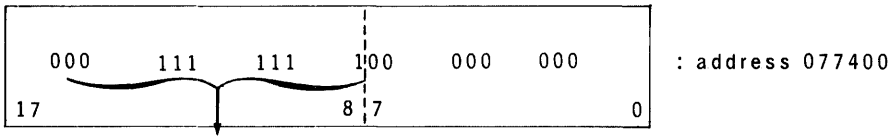
3.6. STORAGE PROTECTION (GUARD MODE LIMITS)

To ensure program protection, a selected area of storage may be placed under Guard Mode Limits through the use of the LGM (f = 5065) instruction. When the Guard Mode is active, any attempt to store into a storage address outside the range set by the LGM instruction causes a Guard Mode Interrupt at address 30_8. Two 9-bit registers, Storage Limits Upper and Storage Limits Lower, may be loaded with the upper and lower bounds of an area of storage to be placed under Guard Mode. For this purpose, storage is divided into 256-word blocks. The LGM is a privileged instruction and may not be used by the programmer.

When the nine high-order bits of a 17-bit storage address are placed in Storage Limits Lower, the first address of that block is the lower bound of the Guard Mode Limits. When the nine high-order bits of a 17-bit storage address are placed in Storage Limits Upper, the last address of that block is the upper bound of the Guard Mode Limits. For example, the instruction

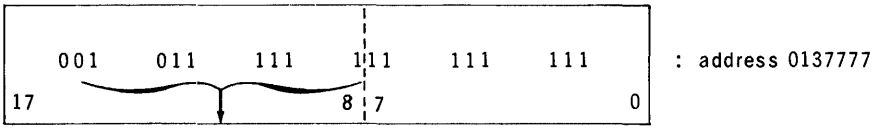
```
LABEL          OPERATION          OPERAND
1         10        20        30        40
          LGM
          +0277177
```

prevents storage outside the range of addresses 077400_8 to 0137777_8; any attempted violation of this restriction causes a Guard Mode Interrupt instead.



: address 077400

0177 = Storage-Limits-Lower Contents



: address 0137777

0277 = Storage-Limits-Upper Contents

Upon the occurrence of any interrupt, the Guard Mode Designator is cleared (disabled), so that all of main storage becomes accessible to subroutines gaining control through the

interrupt locations.

Because locations 0 through 17_8 are never under guard mode protection, it is always possible to use them for storage. The index registers are part of that category and are actually located at addresses 1 through 10_8.

3.7. PRIVILEGED INSTRUCTIONS

Privileged instructions are those which are needed by an operating (controlling) system in order to perform its job; they are considered inappropriate for use in normal (user) programs. The appearance of any of these instructions in any user program would have an unpredictable and probably disastrous effect.

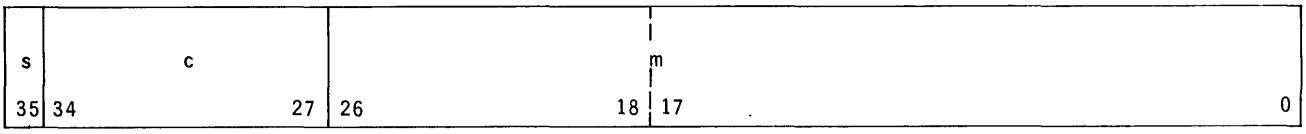
When the Guard Mode Designator is set, through the use of an LGM instruction, any attempt to execute a privileged instruction causes a Guard Mode Interrupt instead. The privileged instruction is not executed or initiated.

The privileged instructions are:

5011 Load Input Channel (LIC)
5012 Load Output Channel (LOC)
5013 Load External Function Channel (LFC)
5015 Stop Input on Channel (STIC)
5016 Stop Output on Channel (STOC)
5021 Test Input Channel (TIC)
5022 Test Output Channel (TOC)
5023 Test Function Channel (TFC)
5024 Wait For Interrupt (WFI)
5025 Wait For Interrupt (WFI)
5056 Stop On Key Setting (SK) - Ignored when in Guard Mode.
5065 Load Guard Mode (LGM)
5066 Set Audible Alarm (SAA)
5067 Enable ESI Interrupts (EEI)

3.8. FLOATING POINT NUMBERS

Floating point numbers are 2-word, 36-bit constants; they consist of a mantissa and a characteristic. The format of a floating point number is:



where:

s is the sign bit
c is the 8 characteristic bits
m is the 27 mantissa bits.

The mantissa (m) contains the 27 significant bits of the floating point number. The magnitude of the mantissa is either zero or between $.4_8$ and $.777777777_8$, normalized so that the most significant bit is a one. The characteristic is the value of c in the expression $2^{c-200_8} * m$. The high-order bit of c (bit 34) is the sign bit of the characteristic. When $c_{34}=1$, the characteristic is positive; when $c_{34}=0$, the characteristic is negative. The sign bit (s) is zero when the floating point number is greater than zero (positive); it is one when the number is less than zero (negative). The magnitude (positive equivalent) of a

negative number is its one's complement.

Take, for example, the number 2.0. It can be rewritten in floating point form as:

$$2.0 * 10^{0}, \text{ or}$$
$$20. * 10^{-1}, \text{ or}$$
$$.20 * 10^{1}, \text{ and many others.}$$

In the above examples, 0, -1, and 1 are the characteristics; 2.0, 20., and .20 are the mantissas. The three expressions represent the same quantities, illustrating that the mantissa and characteristic may be manipulated so that the value of the number remains unchanged. The octal representation of this number is:

$$2.0 * 10^{0} = .2_{8} * 2^{3}$$

To normalize, the mantissa is multiplied by 2, and the characteristic is decreased by one.

The floating point format is:

$$002400000000_{8}$$

Finally, to indicate that the power of the characteristic is positive, the characteristic is biased to obtain 202400000000_{8}. In the same manner, -2.0 is represented as 575377777777_{8}.

3.9. INTERRUPTS

Interrupts are internally generated signals which cause the C/A section to interrupt its normal sequence of instructions (governed by Instruction Address Register contents), and to take the next instruction from a predetermined address in main storage. The contents of the IAR are not changed until the interrupt instruction is executed. An SLJ or SLJI instruction is placed in the interrupt locations, which captures the value of IAR in order to allow normal processing to continue when the interrupt processing coding is completed.

Whenever an interrupt is generated and control passes to the appropriate interrupt location, the Guard Mode designator is cleared, and all subsequent interrupts are held back until the C/A section executes an AAI or EJI instruction.

A summary of all reserved storage locations, including the interrupt locations, is contained in Appendix C.

3.9.1. Parity Fault Interrupts – Locations 21_{8}, 22_{8}, 27_{8}, 31_{8}, 32_{8}, and 40_{8}

Parity errors, whenever they occur during an access of storage by either the C/A or the I/O sections, result in an interrupt. If a parity error occurs when the C/A section accesses main storage, the instruction at location 278 is executed. If a parity error occurs when the C/A section accesses IGR storage, the instruction at location 408 is executed.

If a parity error occurs when the I/O section accesses either main storage (data transfer) or IGR storage (BCW's), the address of the storage location which was being read is placed in locations 22_{8} and 32_{8} for IOM #0 and IOM #1 respectively and s the instruction at location 21_{8} or 31_{8} is executed, depending on whether IOM #0 or IOM

1 was doing the transfer.

Detection of a C/A storage parity error results in execution of the instruction at address 27_8. This may be the result of a fault at either of two possible locations in storage. It could be the address at which the next instruction is located, or it could be the address referenced as a result of the operation being performed. In order to determine the address referenced, the following sequence is used:

(1) If a parity error occurs when reading the contents of the captured IAR address (captured through an SLJ instruction at location 27_8), the error has occurred at the captured IAR address.

(2) If the parity error did not occur at the captured IAR address, a main storage search must be initiated. Instead of reading all of storage to determine which address might possibly have been referenced by some instruction, or instead of trying to find which effective address the interrupted instruction had referenced, a special hardware sequence can be initiated.

An LOC instruction to Channel 0 can be performed with the BCW's set to the range to be tested (between 000000 and 177777_8). Channel 0 scans the first 65K of storage until an error is found.

When an error is detected, IOM #0 stores the address of the error in storage location 22_8 and interrupts the C/A section and causes it to read the instruction from storage address 21_8. Address 21_8 contains a jump to the IOM #0 parity subroutine, which captures and evaluates the address of the parity error.

Channel 0 does not scan beyond the point of error until the subroutine releases the interrupt lockout. The IOM then resumes scanning the remainder of storage starting at the ERROR location + 2 for parity errors; the address following each error is not checked. Channel 0 can scan 65K of storage in approximately 50 milliseconds or more.

If it is desired to scan upper storage (65K - 131K), the monitor interrupt from the foregoing instruction is used to reinitiate the LOC on Channel 0 with the BCW's set to the range to be tested (between 200000_8 and 377777_8).

NOTE: If an error occurs during the read of a jump instruction, the instruction has been executed. If a LOC is used on channel 0, the C/A is locked out during the transfer time, because the IOM now operates at the maximum transfer speed (1.33 million words per second).

3.9.2. Supervisor Call Interrupt - Location 20_8

When an instruction with the function codes 00, 01, 77, 5000, 5001, or 5077 is attempted, the instruction at location 20_8 is executed. If the optional hardware for the convert or floating point instructions is not present, these function codes also cause a Supervisor Call Interrupt whenever they are executed.

3.9.3. Day Clock Interrupt - Locations 23_8 and 24_8

When the Day Clock is attached, location 24_8 is incremented every 6 seconds. Every minute an interrupt at location 23_8 is generated.

3.9.4. Real Time Clock Interrupt - Locations 25_8 and 26_8

The Real-Time Clock (RTC) decrements the contents of location 26_8 every 200 microseconds. When the contents of location 26_8 becomes zero, an interrupt at location 25_8 is generated, and the contents of location 26_8 become 777776_8.

3.9.5. Guard Mode Interrupt - Location 30_8

When the Guard Mode designator is active and an attempt is made by the C/A section to store into a main storage or IGR location which is outside the limits specified by the storage limits registers, the instruction at location 30_8 is executed instead of the attempted store instruction.

When the Guard Mode designator is active and one of the privileged instructions is attempted, the interrupt is generated and the instruction is not executed.

3.9.6. Power Loss Interrupt - Location 33_8

A Power Loss Interrupt results from loss of input power. The Operating System then has at least 0.6 millisecond to store any vital information prior to stopping. When the interrupt is generated, control passes to location 33_8.

3.9.7. Floating Floating Point Underflow Interrupt - Location 34_8

When a floating point instruction is executed and the resulting characteristic has a value of less than zero, a floating point underflow interrupt is generated which causes the instruction at location 34_8 to be executed.

3.9.8. Floating Point Overflow Interrupt - Location 35_8

When a floating point instruction is executed which would cause the resulting characteristic to have a value greater than 377_8, a floating point overflow interrupt is generated which cause the instruction at location 35_8 to be executed.

3.9.9. Interrupt Lockout Timeout Interrupt - Location 41_8

If the C/A section does not release the interrupt lockout within the period of time set by the timeout delay, while in Guard Mode, control is passed to location 41_8, and the instruction previously stored there is executed. The timeout delay is approximately 100 to 200 microseconds.

3.9.10. ISI External Interrupts - Locations 140_8-177_8 and 240_8-277_8

When a peripheral device connected to an ISI channel transmits an External Interrupt (through the EI signal), the data transmitted is placed in location 160_8+CHNO or 260_8+CHNO-16, and the instruction located at address 140_8+CHNO or 240_8+CHNO-16 is executed. CHNO represents the channel number by which the device is attached to either IOM #0 or IOM #1 respectively.

3.9.11. ISI Internal Interrupts - Locations 100_8-137_8 and 200_8-237_8

As a result of the Monitor bit in the BCWT location, each IOM generates an Internal Interrupt whenever the BCW's become equal and the ISI Internal Interrupt locations receive control as a result. There is one interrupt location for each channel of each IOM for both input and output.

3.9.12. ESI Interrupts - Locations 36_8 and 37_8

When an ESI table entry is made, an ESI interrupt is generated whenever the ESI interrupt lockout designator for that IOM is enabled. If interrupts are withheld as a result of any previous interrupt or PAI instruction, the ESI interrupt is delayed until interrupts are again enabled.

If the ESI interrupt lockout designator is set, no ESI interrupt is generated as a result of a new ESI table entry. Depending on which IOM is updating the ESI table, an ESI interrupt causes the instruction at location 36_8 or 37_8 to be executed and the ESI interrupt lockout designator for that IOM to be set.

4. INPUT/OUTPUT SECTION

4.1. INTRODUCTION

This section provides a description of the Input/Output Section of the UNIVAC 418-III Real-Time System. It presents a detailed definition of the data transfer characteristics and of the functional operation of the Input/Output Section. A thorough knowledge of the Input/Output Section is necessary to take full advantage of the operating capabilities of the system.

4.2. GENERAL DESCRIPTION

The Input/Output Section consists of one or two functionally independent Input/Output Modules, IOM #0 and IOM #1. Each IOM is designed to permit I/O data transfers to be independent of the operation of the Command/Arithmetic Section of the UNIVAC 418-III System. See Section 2 for interface with main storage.

Input/Output Module IOM #0 has at least eight I/O channels; this number may be increased to 16 in groups of four. Expansion beyond 16 channels to a maximum of 32 requires the addition of IOM #1. IOM #1 can be added with or without expansion of IOM #0. Except for the following, both Input/Output Modules are functionally identical.

- IOM #0 contains the logic for decrementation of the Real-Time Clock and generation of the Real-Time Clock Interrupt.
- IOM #0, channels 0 and 1, contains the logic for communication with the day clock and the operator's console.
- Channels 16 and 17 of IOM #1 can operate in paired channel mode only.

4.3. FUNCTIONAL OPERATION

All references to input or output are made with respect to an IOM. Input describes a data transfer via an input channel from a subsystem through the IOM to main storage. Output describes a data transfer via an output channel from main storage through the IOM to a subsystem. Any number of subsystems are capable of both input and output data transfers; however, bidirectional transfers do not occur simultaneously. Each IOM contains a set of high speed Integrated General Registers which are used as storage for control words. Each IOM contains from eight to sixteen 18-bit input/output channels. Depending on the peripheral subsystem, these channels can be used singly or in pairs in order to provide a broader data path. Each IOM operates independently of the other, affording two-way simultaneity of input/output and storage with an aggregate capacity of 1.33 million 18-bit word transfers per second per module. Main storage provides separate data paths to and from each IOM.

Each IOM provides the data paths and the control circuitry necessary for direct communication between main storage and the input/output devices. That portion of the circuitry and the data path which is necessary to connect a peripheral subsystem with main storage is called a channel. Each channel allows transfers of data in either direction between main storage and the devices on that channel. Each channel contains 36 data lines, 18 for input and 18 for output.

Most peripheral subsystems utilize both the input and corresponding output lines of the same channel. Data transfers on these subsystems may be made in either direction over a single channel, but not simultaneously. Similarly, data transfers may not occur at the same time through two different channels on the same IOM. If, however, the main storage buffer areas for input/output transfers through channels of different IOM's are located in different main storage banks, these data transfers can occur at the same instant. When two or more subsystems request data transfers at the same time, each IOM performs as a multiplexer with a combined transfer rate of up to 1.33 million 18-bit words per second. If there are two IOM's and separate storage banks, the transfer rate capability is 2.66 million 18-bit words.

Each IOM functions as a small processor. Programmed instructions, executed by the Command/Arithmetic Section, load index values into the Buffer Control Words located in the IOM and also establish desired peripheral subsystem activity. From that point on, the IOM scans the input/output channels automatically, accepting data from and passing data to the subsystem at the normal rate of the subsystem. When a peripheral subsystem requests a data transfer, the contents of the Buffer Control Words for that channel are used as a main storage address, and the transfer occurs. At the same time, the IOM updates the contents of the Buffer Control Word and tests for a terminal condition. This entire operation requires only the time of one memory cycle, 750 nanoseconds. The Buffer Control Words are located in the high speed Integrated General Registers.

The number of data words transferred between a subsystem and main storage, and the address of the locations to or from which they are transferred is controlled by two Buffer Control Words (BCW) which are associated with each data transfer operation. The Initial Buffer Control Word (BCWI) contains the current storage address of the operation. As each data word transfer occurs, the BCWI is incremented or decremented by one, depending upon a bit specified in the Terminal Buffer Control Word (BCWT). The BCWT contains the last (terminal) address of the buffer. The data transfer activity stops and the channel is deactivated when the BCWI and the BCWT are equal.

Each channel operates in one of three states: input, output, or function. The input and output states are used when transferring data to or from main storage. The channel can alternate between the input and the output states on consecutive memory cycles. The function state is the means by which the Command/Arithmetic Section establishes initial communication with a peripheral subsystem and is basically an output state. During this state, the Command/Arithmetic Section causes the IOM to transfer one or more function words to a peripheral subsystem. These function words direct the subsystem to perform the desired operation.

When one or more channels are active, the IOM, independent of program control, scans **the channels in decreasing numerical sequence, in search of input and output data request signals presented by a subsystem. Upon finding a data request signal on an active channel, the IOM controls the transfer of a word between a main storage location and the requesting subsystem. Consecutive transfers of data words to or from a subsystem are performed at a rate governed by the subsystem.**

4.4. CHANNEL OPERATION

A single channel of the Input/Output Section provides 18-bit parallel communication between the IOM and a subsystem. (See Appendix A for a description of normal and compatible channels.)

Logically combining any pair of sequentially numbered even and odd channels (4 and 5, for example, but not 3 and 4, or 5 and 6) into a single 36-bit channel allows 36-bit parallel communication between the IOM and a subsystem.

When operating with paired channels, the control lines associated with the odd numbered channel have control of all data transfers. The most significant half of the 36-bit word is carried by the odd numbered channel; the least significant half is carried by the even numbered channel.

4.5. I/O CHANNEL PRIORITY

Although all I/O channels may be available for communication between the IOM and the subsystems at the same time, only one channel of one IOM is actually transferring data at any given instant. However, since the subsystem handles data more slowly than the main storage and the IOM, it is possible for the IOM to keep all or many of the subsystems operating simultaneously.

The rate of consecutive transfers of data words to or from a subsystem is governed by the subsystem when it is ready to send or receive a data word. When two or more subsystems are currently active, they may also be simultaneously presenting data transfer requests (ODR's, IDR's or both) to the IOM. In order to resolve the conflict of simultaneous requests, a priority control network is used within the IOM.

When an I/O scan is performed and two or more I/O data transfer requests are present, the request from the highest numbered channel is serviced first by the IOM. Any request for I/O data transfer from the same channel is skipped for one I/O scan cycle during the next I/O scan. This allows service for the lower numbered channels of the IOM. The next request serviced is from the highest numbered channel requesting service at the time of the next I/O scan. The scan for a new operation takes place 275 ns before the last pass of the current operation is complete and every 125 ns thereafter.

The following functional priorities are established in each IOM:

(1) Output Data Transfer
(2) Input Data Transfer
(3) Main Memory and IGR Parity Errors
(4) Real-Time Clock Interrupt (IOM #0)
(5) Day Clock Interrupt (IOM #0)
(6) ESI External Interrupt
(7) ISI External Interrupt
(8) External Function Monitor or Output Monitor
(9) Input Monitor
(10) I/O Instructions and arithmetic references to the high speed integrated general register (IGR) in that IOM.

4.6. INPUT/OUTPUT INTERFACE

Each input/output channel between main storage and subsystems is bidirectional; transfers of data and control signals may take place in either direction between main storage and the subsystem on any channel. Each channel has 36 data lines, 18 for input data and 18 for output data, to permit parallel reading or writing of full 18-bit data words on a nonsimultaneous basis. In addition to the data lines, various control lines are used for transmitting control signals between a subsystem and the I/O Section. The lines of an I/O channel are shown in Figure 4-1 and described in Table 4-1.

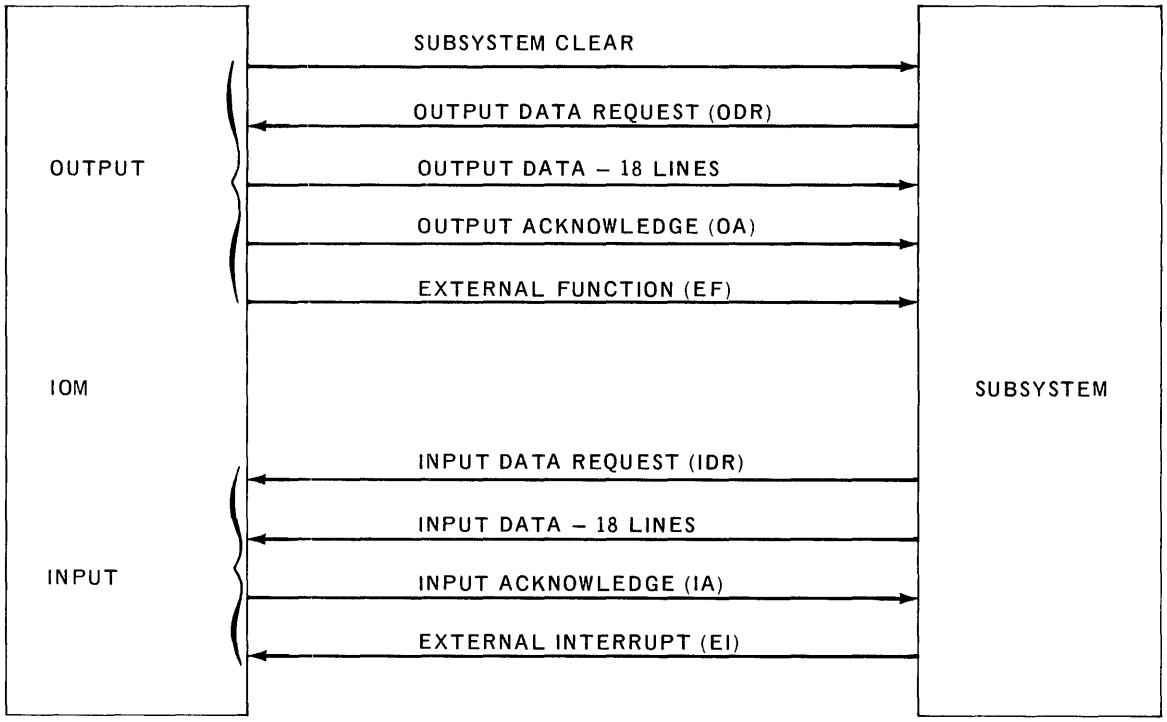


Figure 4–1. One I/O Channel

SIGNAL NAME	ORIGIN	FUNCTION
Subsystem Clear	IOM	Clears subsystem on that I/O channel.
Output Data Request	Subsystem	Indicates to I/O Section that subsystem is ready to receive a data or function word.
Output Acknowledge	IOM	Indicates to subsystem that a data word is on the output data lines.
External Function	IOM	Indicates to subsystem that an External Function Word is on the output data lines.
Input Data Request	Subsystem	Indicates to IOM that a data word is on the input data lines.
Input Acknowledge	IOM	Indicates to subsystem that a data word has been accepted by I/O Section.
External Interrupt	Subsystem	Indicates to IOM that a Status word is on the input data lines.

Table 4-1. I/O Channel Control Signals

4.7. IOM RESPONSE TIME

The interval between a subsystem I/O request and the leading edge of an IOM acknowledge signal is given in Table 4-2.

OPERATION	CHANNEL	
	COMPATIBLE	NORMAL
Internally Specified Index		
18 bit output	1.562 μsec	1.312 μsec
36 bit output	2.312 μsec	2.062 μsec
18 bit input	0.687 μsec	0.687 μsec
36 bit input	1.437 μsec	1.437 μsec
Externally Specified Index		
Output or Input	2.937 μsec	2.937 μsec

Table 4–2. Time Between Subsystem Request and IOM Acknowledge

4.8. OPERATING MODES

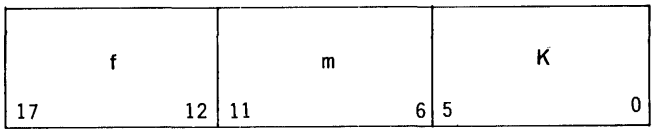
A channel in the I/O Section can operate in either one of the two following modes.

- Internally Specified Indexing (ISI)
- Externally Specified Indexing (ESI)

The formats for the I/O instructions 5011 (LOAD INPUT CHANNEL), 5012 (LOAD OUTPUT CHANNEL), and 5013 (LOAD EXTERNAL FUNCTION CHANNEL) require three memory addresses. The first address is used to store the instruction, the next two succeeding addresses are used to store the buffer limit designators and the modifier and monitor designators. The following illustration shows these details.

18-BIT INSTRUCTION WORD

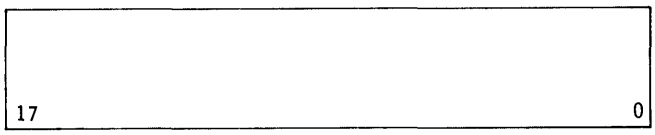
(P) =



f_{17-12} = 6-bit function code (50)
m_{11-6} = 6-bit minor function code (11, 12, 13)
K_{5-0} = 6-bit channel number (00 through 31)

BUFFER CONTROL WORD TERMINAL

(P+1) =



BUFFER CONTROL WORD INITIAL

(P+2) =

(P+3) → P

Execution of the Stop Input on Channel instruction (5015) deactivates the input channel specified by the K field of the instruction. Execution of the Stop Output on Channel instruction (5016) deactivates the output channel specified by the K field of the instruction. Pending monitor interrupts for the terminated channel are cleared.

4.8.1. Internally Specified Indexing (ISI)

All channels, 18 or 36 bit, can operate in an ISI mode. This mode allows input or output on a given channel to one device at a time. All data is sent to or read from one continuous buffer area. Each channel is assigned two pairs of Buffer Control Words (BCW) locations. Any output request on a channel is hardware directed to the location of the first pair of BCW's for that channel. Any input request is directed to the second pair. The BCW's contain the terminal and initial addresses of the main storage locations assigned to the buffer, and certain control bits.

4.8.1.1. Programmed Activation of an I/O Channel - ISI Mode

An input or output channel in ISI Mode is activated when one of the following instructions is executed:

- Load Input Channel (LIC) (5011)
- Load Output Channel (LOC) (5012)

- Load External Function Channel (LFC) (5013)

Execution of the LIC instruction activates the input channel specified by the K field of the instruction and causes the two succeeding addresses to be stored in the input buffer control word addresses for the designated channel.

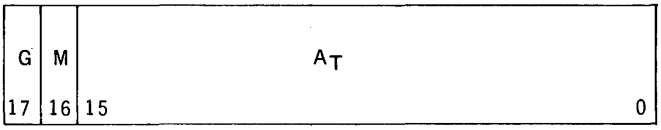
Execution of the LOC or LFC instruction activates the output channel specified by the K field of the instruction and causes the two succeeding addresses to be stored in the output buffer control word addresses for the designated channel. If the instruction is an LFC, an External Function is forced out on the specified channel.

When a channel is activated, data words are transmitted between main storage and a subsystem through the IOM in response to data requests presented by the subsystem on that channel. During the period in which a channel is active, the address of each location in main storage to or from which an I/O data word is transferred is specified by the current contents of the BCWI associated with the channel. As each data word is transferred to or from a location in main storage, the contents of the BCWI is incremented or decremented. When the BCWI equals the BCWT (the least significant 15 bits of each word are compared), the data transfer activity on the related channel is automatically terminated.

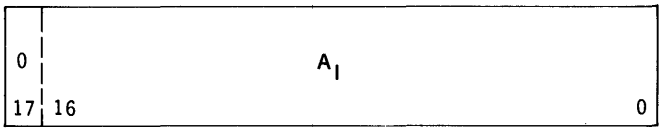
4.8.1.2. ISI Buffer Control Word Formats

All External Function Buffer Control Words and ISI Buffer Control Words are stored in high speed Integrated General Registers (IGR) associated with the I/O channel and consist of a terminal address word and a initial address word in the following formats:

TERMINAL ADDRESS WORD



INITIAL ADDRESS WORD



A_T: The address of the last word in the buffer, less the high order address bit

A_I: The 17-bit address of the first word in the buffer (becomes the present address)

G: A_I modifier
G = 0: A_I is incremented by one for each buffer word transfer.
G = 1: A_I is decremented by one for each buffer word transfer.

NOTE: Each paired channel transfer causes two buffer word transfers.

M: Monitor
M = 0: The channel terminates when the present address equals the terminal address (bits 15 - 0)
M = 1: The channel terminates when the present address equals the terminal address, and a monitor interrupt is generated for the associated channel.

The buffer area may be assigned starting in the lower 65K of main storage and ending in the upper 65K of main storage; the total number of words transferred may not exceed 65K, however. The following shows an example of an incrementing buffer that crosses from lower main storage (banks 0 and 1) to upper main storage (banks 2 and 3).

BUFFER CONTROL WORD TERMINAL

000200_8

BUFFER CONTROL WORD INITIAL

001000_8

CONTENTS OF BCWI WHEN BUFFER TERMINATION IS DETECTED

200200_8

A normal update of BCWI occurs when buffer termination is detected. The final address value stored at the BCWI location for the foregoing example is:

200201_8

If a BCWI specifies an address in the upper 65K (bit 16 set to 1) of main storage, and if the lower address bits (15-0) contain a larger value than contained in the BCWT, the BCWI wraps around zero as shown in the following example of an incrementing buffer. The IOM does not check for this condition.

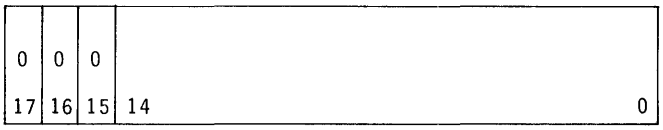
BUFFER CONTROL WORD TERMINAL

000200_8

BUFFER CONTROL WORD INITIAL

201000_8

CONTENTS OF BCWI AT TERMINATION



000200_8

4.8.1.3. ISI Input/Output Activity

Two modes of activity are performed on an output channel. In one mode of output channel activity (Function Mode), data words called External Function words are transferred from main storage through the active output channel to a subsystem. The External Function Word (EF word) is decoded by the subsystem's control section, and the subsystem is consequently conditioned to perform a specific task, or an input or output data transfer operation. Also, in the Function Mode, data words called Identifier (ID) words are transferred through the active output channel after an appropriate function word has been transferred to the subsystem. The ID word is used in the performance of a Search-Read operation in a subsystem; the ID word is an image of a word being searched for in the subsystem. An output channel is activated for operation in the Function Mode by execution of the Load External Function Channel (LFC) instruction.

In the other mode of output channel activity (Output Mode), data words, called output data, are transferred from main storage via the active output channel to the subsystem. If the subsystem is a magnetic tape subsystem, the output data is written on the magnetic tape; if it is a high speed printer subsystem, the output data is printed on paper, etc. An output channel is activated for operation in Output Mode by execution of the Load Output Channel (LOC) instruction.

Similarly, two types of activity are performed on an input channel. In one type of input channel activity (Input Mode), data words, called input data, are transferred from the subsystem through the active input channel to main storage. If the subsystem is a magnetic tape subsystem, the input data is read from the magnetic tape; if it is a card subsystem, the input data is read from cards, etc. An input channel is activated for operation in Input Mode by execution of the Load Input Channel (LIC) instruction.

In the other type of input channel activity (External Interrupt Mode), the subsystem presents a word, called the External Interrupt Status Word to the IOM through the input channel. An external Interrupt Status Word is a coded word which is generated in the subsystem's control section. This word indicates to the program the

successful completion of either a specific task or an input or output operation, or the occurrence of an abnormal condition in the subsystem. It is not necessary to execute a channel activating instruction for the channel to transfer an External Interrupt Status Word to the IOM.

Appendix B is a detailed description of sequence for Input, Output, and Function Mode activity of an IOM.

4.8.1.4. ISI External Interrupt

A subsystem notifies the Command/Arithmetic Section of an abnormal condition or of the normal completion of an operation by placing an External Interrupt Status Word on the input data lines and an External Interrupt (EI) signal on the appropriate line of the input channel. The input channel on which an EI signal is presented is selected to be serviced by the IOM priority network. If more than one channel presents an EI signal, the EI on the highest numbered channel is serviced first, then the next in descending order, and so on. The IOM services the input channel presenting an EI signal as follows:

(1) It transfers the External Interrupt Status Word from the input data lines to a fixed address location in main storage for the channel on which the EI signal is generated.

(2) It places an Input Acknowledge (IA) signal on the appropriate input channel line.

(3) It interrupts the normal sequence of instruction execution in the C/A section thereby causing the C/A section, upon completion of the execution of the current instruction, to load automatically an instruction from the ISI External Interrupt fixed address location.

(4) All ISI interrupts and the ESI tabling notification interrupt are disabled.

The subsystem reacts to the IA signal by returning to its 'at rest' state.

No specific instruction is needed to activate an input channel before an EI signal and an External Interrupt Status Word are presented to the IOM.

4.8.1.5. ISI Monitor Interrupts

When the IOM detects that the BCWT and BCWI are equal and the M flag (bit 16 of BCWT) is set, a monitor interrupt is generated. The monitor interrupts are serviced systematically by the IOM priority network. If more than one channel simultaneously present a monitor interrupt, the one on the highest numbered channel is serviced first. When a monitor interrupt is serviced by the C/A section, the next instruction executed is obtained from the monitor interrupt fixed address locations. Monitor interrupts awaiting service are not cleared by the execution of LOC, LIC, or LFC instructions.

4.8.2. Externally Specified Indexing (ESI)

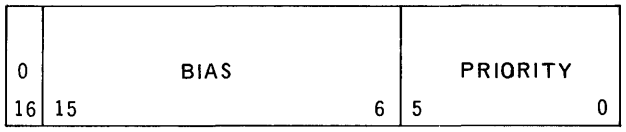
The ESI mode of I/O Channel operation is selected for a paired channel to which a Communication Terminal Module Control Subsystem (CTMC) is connected and to

which in turn up to 16 Communication Terminal Modules (CTM) may be added. Each CTM comprises two or four Communication Line Terminals (CLT).

When a channel is operating in the ESI mode, 18 bits are transmitted, bit-parallel, between main storage and the CTM by way of the IOM and the CTMC Subsystem. Data transmissions to or from a number of CTM's are multiplexed on one I/O channel through the operation of the CTMC subsystem.

Channels operating in ESI must be in paired channel mode. Data and external function words are transmitted on the even numbered channel of the pair. Control signal lines of the odd channel control input and output transfers. External functions are transmitted through the even channel External Function line.

Accompanying each data transfer between the CTMC and the processor is an ESI address identifying which pair of BCW's is to be used to control the data transfer. The ESI address has the following format:



The low order six bits of the ESI address identify the CLT to or from which data is to be transferred. All input CLT's have odd priority codes, and all output lines have even priority codes as indicated by bit 0.

The bias bits are fixed at a specific value at system installation time; they specify the high order portion of the beginning address of the Buffer Control Word (BCW) table.

Since each line requires two successive BCW's it is necessary for the IOM to double the value of the ESI address when referencing the Buffer Control Words.

Figure 4-2 is a schematic representation of the ESI data transmission.

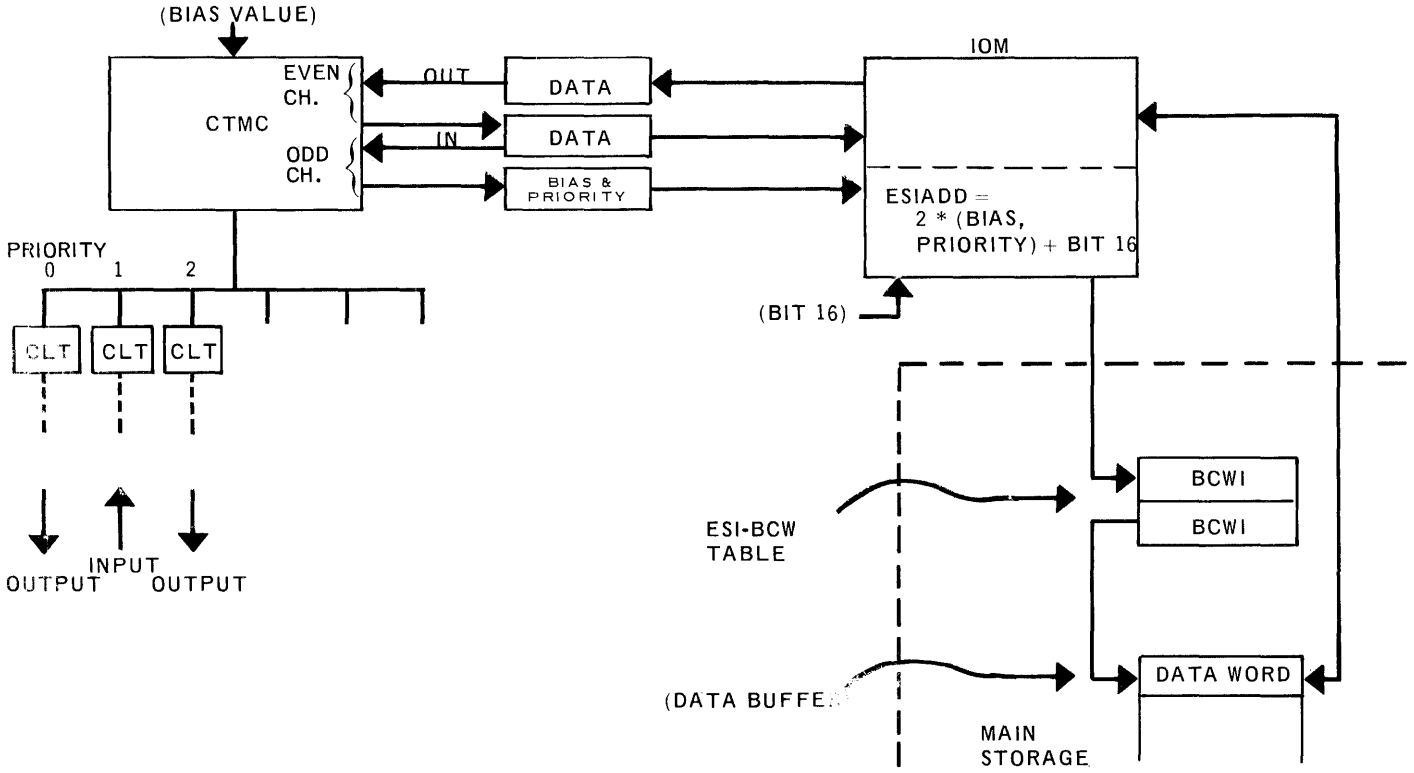


Figure 4-2. ESI Data Transmission

A CTM that is prepared to perform an output operation presents a request to the CTMC when the CTM is ready to receive output data. The CTMC, which continuously scans all CTM's for service requests, locks onto the interface of the CTM requesting service and stays locked until the transfer of one data word to that CTM is complete. If more than one CTM is requesting service at the same time, they are serviced according to priority.

In order to serve a CTM which has requested to output data, the the CTMC presents an ODR to the IOM by way of the appropriate line of the odd output channel. At the same time, the CTMC presents a 15-bit ESI value (bits 14 - 0) to the IOM by way of the odd input channel of the pair.

The ESI value is left shifted (to positions 15 to 1) in the IOM to permit double BCW's. (Address bit 16 is selectable, by connection of a jumper wire in each IOM, to locate BCW's for all ESI devices on the IOM in either of the 65K segments of main storage.) The biased ESI value specifies the absolute address of the location in main storage where the BCWT associated with the particular CTM is stored.

The IOM then obtains the BCWT and BCWI from the locations in main storage specified by the biased ESI value. The IOM then obtains the output data from the location in main storage specified by the contents of the BCWI.

The data is placed on the even channel output data lines and transmitted with an Output Acknowledge (OA) signal via the CTMC to the CTM. Also, the BCWI is tested for the terminal condition, updated, and then restored in the main storage location fromwhich it was obtained. After the CTM receives the output data and OA signal, the CTMC then

seeks another CTM to service.

A CTM that is conditioned to perform an input operation presents a request to the CTMC when it is ready to send input data. The CTMC locks onto the CTM's interface and services multiple requests on a priority basis.

When a particular CTM which is requesting service for an input is serviced, the CTMC presents an IDR to the IOM via the appropriate line of the odd channel. It also presents a 15-bit ESI value on the input lines of the odd channel. The ESI value and fetching of the BCWT and BCWI are handled in the same manner as an output transfer. The IOM then stores the input data in the main storage location specified by the contents of the BCWI and also transmits an IA signal via the appropriate line of the odd input channel. The BCWI is tested for the terminal condition, updated, and then restored in the main storage location from which it was obtained.

4.8.2.1. Programmed Activation of an I/O Channel - ESI Mode

An input or an output channel in ESI Mode is activated when one of the following instructions is executed:

- Load Input Channel (LIC) (5011)
- Load Output Channel (LOC) (5012)

Execution of the LIC instructions activates the input channel specified by the K field (odd channel of the pair must be specified) of the instruction and causes the two succeeding addresses to be skipped.

Execution of the LOC instruction activates the output channel specified by the K field (odd channel of the pair must be specified) of the instruction and causes the two succeeding addresses to be skipped.

Any one or more of the CTM's connected to a CTMC can be caused to perform, or to stop performing, an input or output operation, as a result of programmed execution of the LFC instruction.

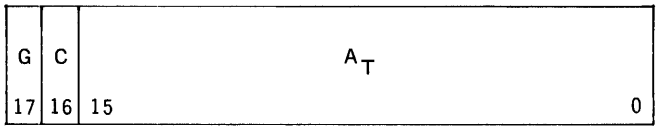
The execution of the LFC for ESI is similar to the operation described for ISI. (See Appendix B.) The LFC word for ESI is composed of three bits of the seven-bit CLT selection code, and a three-bit function code that determines what action the CLT will take.

4.8.2.2. ESI Buffer Control Word Formats

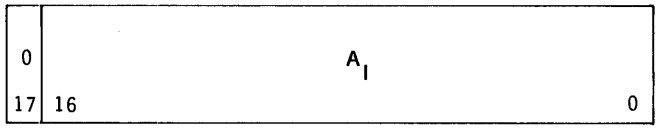
The Buffer Control Word (BCW) used in the ESI Mode of I/O Channel operation may have either of two formats. One of the formats is used with I/O operations on channels in ESI Mode that are wired to transfer one I/O data character per 18-bit main storage address. The other format is used with I/O operations on the channels in ESI Mode that are wired to pack two I/O data characters per 18-bit storage address.

- Fullword ESI Buffer Control Words (18-bit Main Storage Transfers)

BUFFER CONTROL WORD TERMINAL



BUFFER CONTROL WORD INITIAL



A_T: Bits 15 - 0 of the address of the last word in the buffer

A_I: The address of the first word in the buffer (becomes the present address)

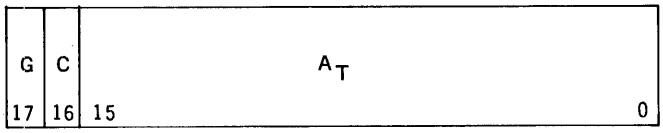
G: A_I modifier
G = 0: A_I is incremented by one for each buffer word transfer.
G = 1: A_I is decremented by one for each buffer word transfer.

C: Chain
C = 0: The buffer is terminated when the present address equals the terminal address.
C = 1: The contents of the address $A_T + 1$ and $A_T + 2$ are stored as new buffer control words for the corresponding device, and buffer termination does not occur. See 4.8.2.5 for an example of ESI data chaining.

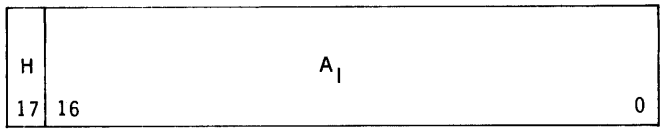
NOTE: If G = 1, $A_T + 1$ and $A_T + 2$ become $A_T - 1$ and $A_T - 2$.

- Halfword ESI Buffer Control Words (9-Bit Main Storage Transfers)

BUFFER CONTROL WORD TERMINAL



BUFFER CONTROL WORD INITIAL



A_T: Bits 15 - 0 of the address of the last word in the buffer

A_I: The address of the first word in the buffer (becomes the present address)

G: A_I modifier
G = 0: A_I is incremented by one for each buffer word transfer
G = 1: A_I is decremented by one for each buffer word transfer
NOTE: Each time G changes, A_I is modified accordingly.

C: Chain
C = 0: The buffer is terminated when the present address equals the terminal address.

C = 1: The contents of the address $A_T + 1$ and $A_T + 2$ are stored as new buffer control words for the corresponding device, and buffer termination does not occur. See 4.8.2.5 for an example of ESI data chaining.

NOTE: If G = 1, $A_T + 1$ and $A_T + 2$ become $A_T - 1$ and $A_T - 2$.

H: Halfword Count

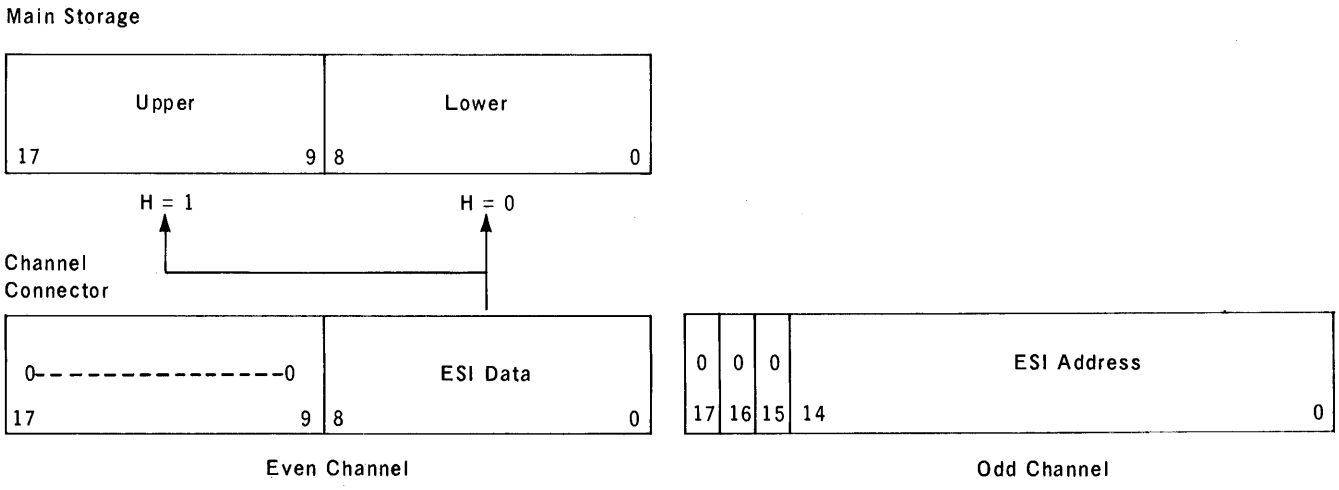
H = 0: On input, the data on the lower 9 bits of the input lines for the even numbered channel is stored in the lower 9 bits of the location specified by the present address.
On output, the contents of the lower 9 bits of the main storage location is sent to the lower 9 bits of both the even and odd numbered channels.

H = 1: On input, the data on the lower 9 bits of the input lines for the even numbered channel is stored in the upper 9 bits of the main storage location.

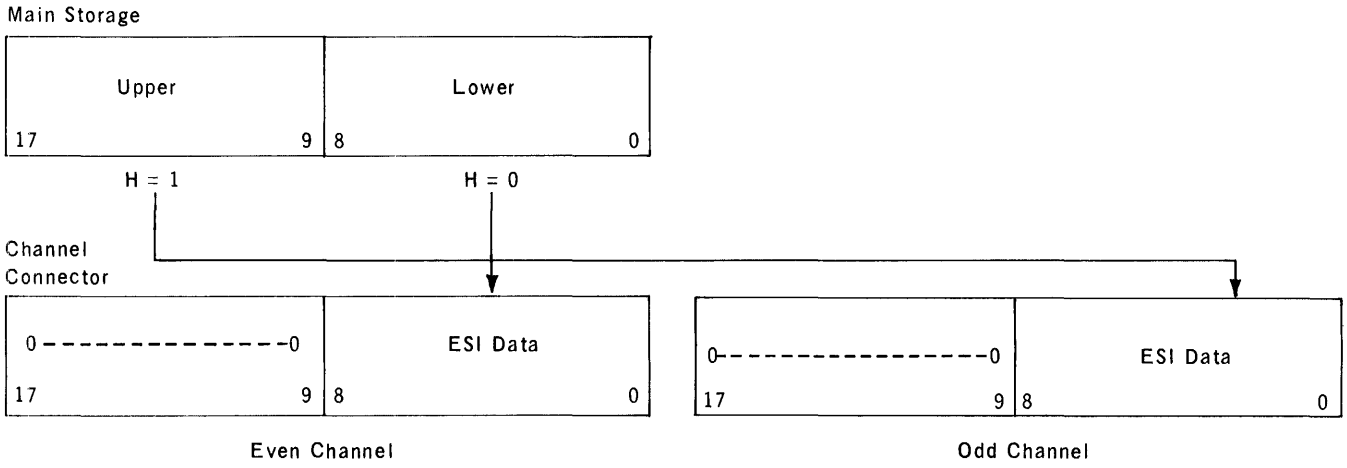
On output, the contents of the upper 9 bits of the main storage location is sent to the lower 9 bits of both the even and odd numbered channels.

NOTE: A data block may start on a halfword boundary but must end on a fullword boundary.

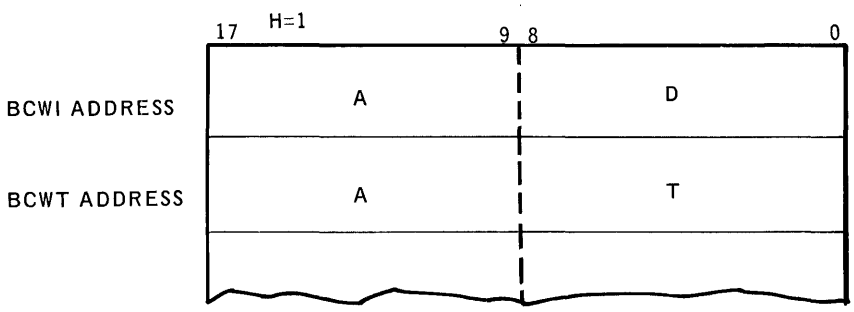
The following shows how 9-bit ESI data is transferred into main storage.



The following shows how 9-bit ESI data is transferred from main storage.



The following shows how characters forming the word 'DATA' appear in storage in ascending order for input or output.



Upon the transfer of each character, the H bit is complemented by the hardware. If the transmission is from 1 to 0, the BCW address is modified as indicated by the G bit in the BCWT. Data transfers may begin on either halfword but must end on a fullword boundary with H = 0.

4.8.2.3. Terminal Buffer Condition Halfword

During each I/O data transfer sequence, the BCWI and the BCWT are compared for a terminal condition. When the IOM is performing an input or output transfer, the terminal condition is indicated when the BCWI and BCWT are equal and the H bit (bit 17 of BCWI) = 1. When a terminal condition is detected and the chain flag (bit 16 of BCWT) is not set, the following sequence of events occurs:

(1) If the operation is an input transfer, the input data is stored in main storage at an address location specified by the BCWI. If the operation is an output transfer, the output data is read from main storage from the address specified by the BCWI and stored in the output buffer register.

(2) The BCWT is restored to a value of +0. This indicates to the IOM that the ESI buffer has been terminated. The contents of the BCWI are not changed.

(3) A buffer termination interrupt is stored in the ESI interrupt table at the location specified by ESI interrupt pointer.

(4) If the operation is an output transfer, an End of Transmission signal is transferred with the data character.

(5) The CTM is acknowledged.

4.8.2.4. Terminal Buffer Condition Fullword

When the IOM is performing an input or output transfer, the terminal condition is indicated by the equality of BCWT and BCWI. When a terminal condition is detected and the chain flag (bit 16 of BCWT) is not set, the following sequence of events occurs:

(1) If the operation is an input transfer, the input data is stored in main storage at an address location specified by the BCWI. If the operation is an output transfer, the output data is read from main storage from the address specified by the BCWI and stored in the output buffer register. The data word specifies an End of Transmission when required.

(2) The BCWT is restored to a value of +0. The contents of the BCWI are not changed.

(3) A buffer termination interrupt is stored in the ESI interrupt table at the location specified by the ESI interrupt pointer.

(4) The CTM is acknowledged.

4.8.2.5. Terminal Condition Fullword or Halfword With Buffer Chaining

When the terminal buffer condition is detected and the chain flag (bit 16 of BCWT) is active, the following sequence of events occurs:

(1) If the operation is an input transfer, the input data is stored in the main storage at an address location specified by the BCWI. If the operation is an output transfer, the output data is read from main storage from an address specified by the BCWI and stored in the output buffer register.

(2) The BCWI is incremented by one if the G flag (bit 17 of BCWT) is not active or decremented by one if the G flag is active.

(3) The BCWT for the new buffer area is read from main storage at the address specified by the updated BCWI and stored in IOM hardware.

(4) The new BCWT is transferred from the IOM to the main storage location specified by the biased ESI value of the CTM and replaces the BCWT which was used on the previous buffer transfer.

(5) The address value contained in the BCWI at this point of the chain sequence is the terminal address ± 1. Step (2) is repeated causing the address value of the BCWI to be updated to the terminal address ± 2.

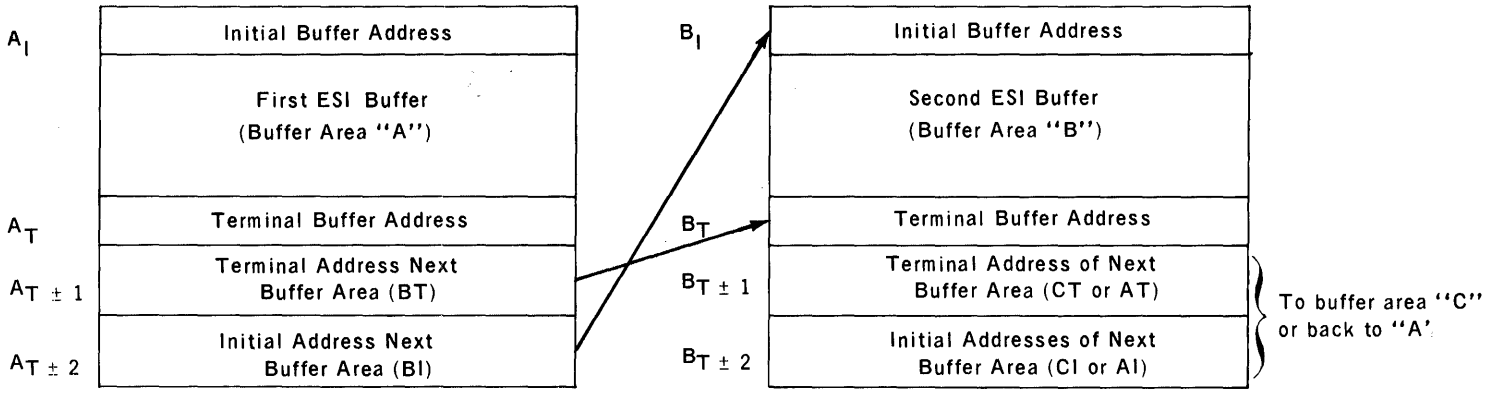
(6) The new BCWI is read from a main storage address specified by the updated BCWI and stored in IOM hardware.

(7) The new BCWI is transferred from the IOM to the main storage location specified by the biased ESI value of the CTM and replaces the old BCWI.

(8) A buffer termination interrupt is stored in the ESI interrupt table at the location specified by the ESI interrupt pointer.

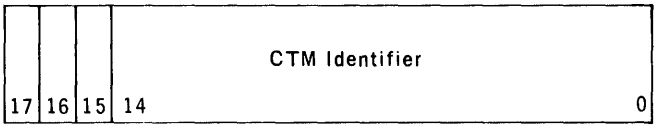
(9) The CTM is acknowledged.

The following shows an example of ESI data chaining.



4.8.2.6. ESI Buffer Termination Interrupt and External Interrupt Tabling

Each IOM is designed to minimize interrupt handling time on ESI channels by hardware tabling of buffer termination and external interrupts. When a buffer termination is detected, an interrupt status word is stored in main storage at an address specified by the ESI interrupt pointer.

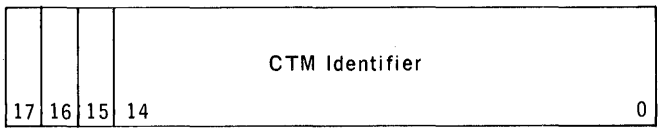


ESI Buffer Termination Status Word

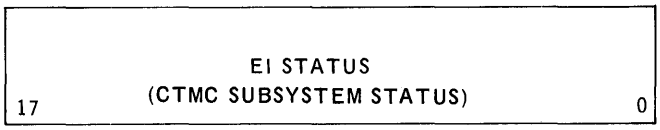
Bits 0-14 contain the CTM identifier presented to the IOM by the CTM. (The ESI value contained in the interrupt status word is not the ESI BCW address).

Bit 15 is a one if the ESI BCW's are stored in the upper 65K of main storage. Bits 16-17 are zero.

When ESI external interrupt (EI) is presented to the IOM, a CTM interrupt word and the EI status word are stored in main storage at addresses specified by the ESI interrupt pointer.



CTM Interrupt Word (odd channel)



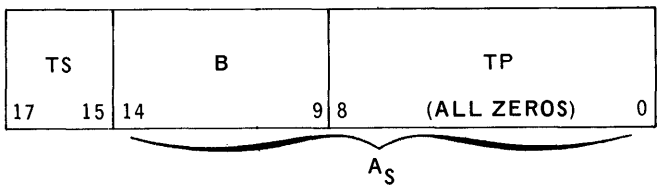
EI Status Word (even channel)

Bits 0-14 of the interrupt word contain the CTM identifier presented to the IOM by the CTM. Bit 15 is a one if the ESI BCW's are stored in the upper 65K of main storage. Bit 16 is a zero.

If the interrupt word resulted from an external interrupt, bit 17 is set to one and the next table location contains the EI status word.

4.8.2.7 ESI Interrupt Table Pointer

The interrupt table pointer provides the storage address and controls the table size ofthe ESI interrupt table. The ESI interrupt pointers are stored in the IGR. IOM #0 pointer is located at address 000340_8, IOM #1 pointer is located at address 000440_8.



ESI Interrupt Pointer

TS: Interrupt Table Size

This field specifies the size of the interrupt table as follows:

TS (Octal)	Table Size in Words (Decimal)
0	64
1	128
2	192
3	256
4	320
5	384
6	448
7	512

B: Address of the interrupt table location (must be located within the first storage bank).

TP: Displacement Table Pointer

A_S: Status Address. A_S = B, TP

This field, bit positions 0 to 14, specifies the main storage location at which to store the interrupt word. Upon receiving or generating an interrupt on an ESI

channel, the interrupt word is stored at main storage location A_S. If the interrupt word resulted from an external interrupt, bit 17 is set to one, and the next table location contains the EI status word. When A_S is equal to the last address of the table, the status is stored and A_S is cleared to its initial address. The ESI interrupt pointers must be loaded into the proper locations following an initial load, and these locations must not be altered again. The contents of the ESI interrupt table may be found by reading the pointer and comparing the pointer address against the address of the last interrupt fetched from the table.

4.8.2.8. ESI Interrupt

Each IOM notifies the C/A section of a table entry by means of an ESI interrupt. The interrupt is generated whenever an ESI Interrupt is stored in the table, as long as the ESI interrupt lockout is cleared. The ESI interrupt lockout is set at the time of generation of the ESI interrupt and can be cleared only by the Enable ESI Interrupt (5067) instruction. Tabling of ESI interrupts by the IOM is not prevented by ESI interrupt lockout but another ESI interrupt does not occur until interrupt lockout is cleared by a 5030 (AAI) or a 54 (EJI) instruction and the ESI interrupt is cleared by 5067 (EEI) instruction to the specified IOM. The IOM does not notify the C/A section of interrupts tabled while the ESI interrupt lockout is set.

4.8.2.9. ESI Parity Error Handling

The following events occur when the IOM detects a BCW parity error during an ESI input data transfer.

(1) The address of the word in error is stored in IOM hardware.

(2) The main storage write control logic is disabled. (The input data word is not stored.)

(3) The address location for the BCWT is stored as all zeros.

(4) The CTM is acknowledged.

(5) The parity error flag is set.

The following events occur when the IOM detects a BCW parity error during an ESI output data transfer.

(1) The address of the word in error is stored in IOM hardware.

(2) The output buffer register is set to all ones.

(3) The address location for the BCWT is stored as all zeros.

(4) The CTM is acknowledged.

(5) The parity error flag is set.

The following events occur when the IOM detects a data parity error during an ESI output transfer or a halfword input transfer.

(1) The address of the word in error is stored in IOM hardware.

(2) The BCWI is updated.

(3) The CTM is acknowledged.

(4) The parity error flag is set.

4.8.2.10. ESI External Interrupt Word Transfers

An external interrupt may be caused by the detection of a single preselected character in the CLT or by the detection of a fault. An external interrupt results in the tabling of two words: the first word is the ESI address with bit 17 set, and the second is the CTMC subsystem status. The IOM tables all External Interrupt status words from ESI channels into main storage. The IOM internally interrupts the Command/Arithmetic Section as it tables the interrupt status word if the ESI interrupt lockout is not set. Further ESI interrupt status words are tabled by the IOM but no more internal interrupts are generated until the Command/Arithmetic Section clears the ESI interrupt lockout with an Enable ESI Interrupts (5067) instruction. Tabling is accomplished using a pointer located at address 000340_8 for IOM #0 and at location 000440_8 for IOM #1. The pointer specifies the address in which to store the interrupt status word and the size of the table. The table wraps around when the last address available in the table is filled, and the next status is stored at the beginning address of the table.

4.9. REAL TIME CLOCK

When the Real Time Clock (RTC) is enabled, the RTC value stored at location 000026_8 of main storage is automatically decremented by one every 200 microseconds. An RTC Interrupt signal is generated when the count is found to be zero at the time an RTC decrement cycle is initiated. An RTC Interrupt signal causes the program control to be switched to execute the instruction at main storage location 000025_8. Location 000026_8 is reset to 777776_8 on the same cycle that the interrupt condition is detected. The program can control the length of time between interrupts by storing a desired value in location 000026_8 and resetting this value upon each interrupt. Interrupt lockout has no effect on RTC decrementation.

4.10. INITIAL LOAD

The system must be master-cleared before starting an Initial Load operation. Initialization of an Initial Load sets up a pair of Input Buffer Control Words for the channel specified by the Initial Load switches on the maintenance panel. The Terminal Address Word has the monitor bit set and contains a terminal address of 010000_8. The Initial Address Word is all zeros. The Initial Load channel is then set in the input mode and an Initial Load Function is sent to the subsystem.

Storage addresses 300_8-477_8 must not be loaded with useful information because this area of main storage cannot be referenced by the Command/Arithmetic Section.

5. OPERATORS CONSOLE

5.1. GENERAL

The operator's console contains the following:

- A 4-bank keyboard with characters and coding as in Table 5-1, with no mechanical connection to the printer.
- A printer to operate at a nominal speed of 10 characters per second with characters and coding as in Table 5-1.
- Indicators and switches for the following functions:

  - Day Clock Decimal Display (optional)
  - Day Clock Fault
  - Abnormal Temperature
  - Stop
  - Run
  - Fault
  - Keyboard On/Off
  - Program Jumps and/or Stops
  - External Interrupt
  - Initial Load
  - Computer Clear
  - IOM #0 and Subsystem Clear
  - IOM #1 and Subsystem Clear

Internal Computer Code (Octal)	Console Printer & Keyboard Symbol	Internal Computer Code (Octal)	Console Printer & Keyboard Symbol
00		40	)
01		41	–
02		42	+
03	(L.F.)	43	<
04	(C.R.)	44	=
05	(space)	45	>
06	A	46	–
07	B	47	$
10	C	50	*
11	D	51	(
12	E	52	”
13	F	53	:
14	G	54	?
15	H	55	!
16	I	56	,
17	J	57	Ⓢ
20	K	60	0
21	L	61	1
22	M	62	2
23	N	63	3
24	O	64	4
25	P	65	5
26	Q	66	6
27	R	67	7
30	S	70	8
31	T	71	9
32	U	72	‘
33	V	73	;
34	W	74	/
35	X	75	.
36	Y	76	□
37	Z	77	↑

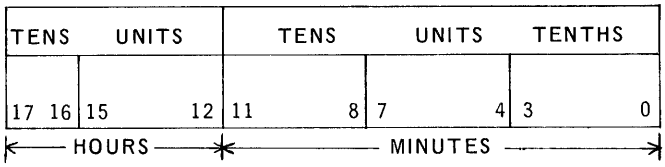
Table 5–1. Console Symbol Code Reference

5.2. DAY CLOCK

The lowest priority channel pair of IOM #0, channels 0 and 1, is intended for communication with the console and the day clock The console uses the ISI Buffer Control Words for channel 1. Storage space for the console data is the lower 6 bits of the memory location specified by the current address word.

The day clock is an optional feature located on the operator's console. The day clock inputs the time to IOM #0 every 6 seconds and stores it in the following format at main storage location 000024_8.

DAY CLOCK FORMAT



The day clock interrupts the computer every minute. When the computer allows the interrupt to be recognized, the program takes the next instruction from storage address 000023_8.

APPENDIX A. NORMAL AND COMPATIBLE CHANNELS

A.1. GENERAL

A patch card located in the logic deck of each IOM enables normal/compatible operation of the IOM. The channels of each IOM are divided into two groups of eight: IOM #0 - (0-7), (8-15); IOM #1 - (16-23), (24-31). Mixing of normal and compatible channels within a group is not permitted. However, normal speed peripherals can operate on compatible channels, possibly at reduced transfer rates.

A.2. NORMAL CHANNELS

A normal channel operates at the highest speed possible consistent with the main storage and logic speeds of the IOM. The maximum data transfer rate that can be achieved on one normal channel under ideal conditons is 570,000 words per second (one word every 1750 nanoseconds). The maximum data transfer rate which can be achieved on a system basis on more than one normal channel under ideal conditions is 1,333,333 words per second (one word every 750 nanoseconds). The actual data transfer rates which could be achieved for a given system are a function of system organization, channel assignments, and choice of peripheral equipment. See Table A-1 for IOM normal-channel data transfer rates.

The UNIVAC 418-III System normal channels are designed to meet the requirements of the IOM/peripheral interface.

CHANNEL REQUESTING TRANSFER	OPERATION	[4] DATA TRANSFER TIME IN μSEC	REPETITION RATE IN MHZ
Internally Specified Index			
[1] Same channel	18-bit output	1.750	0.570
Same channel	36-bit output	2.500	0.400
[2] Same channel group	18-bit output	1.250	0.800
Same channel group	36-bit output	2.000	0.500
[3] Different channel group	18-bit output	0.750	1.333
Different channel group	36-bit output	1.500	0.667
Same channel	18-bit input	1.250	0.800
Same channel	36-bit input	2.000	0.500
Same channel group	18-bit input	0.750	1.333
Same channel group	36-bit input	1.500	0.667
Different channel group	18-bit input	0.750	1.333
Different channel group	36-bit input	1.500	0.667
Externally Specified Index			
Same channel	output or input	3.50	0.285
Same channel group	output or input	3.00	0.333
Different channel group	output or input	3.00	0.333

NOTES

[1] Single channel maximum transfer rates assume that peripheral response does not exceed 400 ns.

[2] Same channel group refers to data transfer requests from two channels that share an output buffer register and acknowledge control logic: 18-bit channel groups (2–4–6), (8–10–12–14), (1–3–5–7), and (9–11–13–15); 36-bit channel groups (3–5–7) and (9–11–13–15).

[3] Different channel group refers to data requests from two channels that do not share an output buffer register or acknowledge control logic.

[4] Times shown are based on 125 ns cycle time and are measured from leading edge to leading edge of the acknowledge signal.

Table A–1. Normal Channel Data Transfer Rates

A.3. COMPATIBLE CHANNELS

The length of time the IOM of the UNIVAC 418-III System holds an output signal (pulse) on a normal channel is shorter than that required for some of the subsystems used with the UNIVAC 418-II System. In order to use these UNIVAC 418-II subsystems with the UNIVAC 418-III System, compatible channel operation is provided to lengthen the time an output signal is held on a channel line.

The maximum data transfer rate over one or more compatible channels is 200,000 words per second (one word every 5 microseconds). See Table A-2 for data transfer rates over IOM compatible channels.

The UNIVAC 418-III System compatible channels are designed to meet the I/O specifications for the UNIVAC 1108 System compatible channels in timing and voltage at the IOM/peripheral interface. Devices which operate on compatible channels are listed in Table A-4.

CHANNEL REQUESTING TRANSFER	OPERATION	DATA TRANSFER† TIME IN μSEC	REPETITION RATE IN MHZ
Internally Specified Index			
Any	18-bit output	5.000	0.200
Any	36-bit output	5.750	0.175
Any	18-bit input	4.500	0.222
Any	36-bit input	5.250	0.190
Externally Specified Index			
Any	Output or Input	7.375	0.135
To calculate Externally Specified Index buffer transfer time, add 750 ns for an unchained buffer and 3 μsec for a chained buffer. This time is added for buffer chaining and interrupt tabling.			

†Times shown are based on 125 ns cycle time and are measured from leading edge to leading edge of the acknowledge signal.

Table A–2. Compatible Channel Data Transfer Rates

APPENDIX B. ISI INPUT, OUTPUT, AND FUNCTION MODE CHANNEL ACTIVITY

B.1. INPUT CHANNEL ACTIVITY

When the LIC instruction is executed, the channel specified by the K field is activated in the Input Mode and the two succeeding storage addresses are transferred to the input buffer control addresses for the specified channel.

The activity performed by the IOM on a channel in the Input Mode is as follows:

(1) When an input channel is active and a subsystem simultaneously presents an input data word and an Input Data Request (IDR) to the IOM over that channel, the IOM services the request as follows:

(a) The IOM transfers the input data word from the input channel into the main storage location specified by the contents of the BCWI.

(b) The IOM tests for a terminal condition by comparing BCWT and BCWI, updates and restores the BCWI to the IGR. If a terminal condition is detected, the channel is deactivated. Steps (a) and (b) are repeated for a 36-bit channel. The most significant 18 bits are transferred to main storage first, over the odd channel of the pair.

(c) The IOM acknowledges its acceptance of the input data word by returning an Input Acknowledge (IA) signal to the subsystem over the same channel.

(2) The subsystem reacts to the IA by removing the IDR and the acknowledged input data word from the input channel. The subsystem then is ready to repeat this foregoing cycle. This process is repeated until the IOM detects a terminal condition when BCWT and BCWI are compared. The channel is then deactivated during the last transfer. If the monitor bit (bit 16 of BCWT) is active when the terminal condition is detected, an input monitor interrupt is generated.

B.2. OUTPUT CHANNEL ACTIVITY

When the LOC instruction is executed, the channel specified by the K field is activated in the Output Mode, and the two succeeding storage addresses are transferred to the output Buffer Control Word addresses for the specified channel. When a channel is active in Output Mode, output data words are transferred from main storage to the subsystem in response to Output Data Requests presented by the subsystem to the IOM.

The initial difference of the BCWT and BCWI should be a value that specifies the number of data words to be transferred to the subsystem.

The activity performed by the IOM on a channel in the Output Mode is as follows:

- When an output channel is active and a subsystem presents an Output Data Request (ODR) to the IOM, the IOM services the ODR as follows:

(1) The BCWT and BCWI are read from the IGR. The difference is tested for a terminal condition and a data word is transferred from a main storage location specified by the BCWI to the output data lines of the channel. If a terminal condition is detected (that is, BCWI and BCWT are equal), the channel is deactivated but the data transfer occurs.

(2) The IOM updates the contents of the BCWI and restores it to the IGR.

(3) The IOM holds the output data word on the output data lines for a limited time, during which the IOM also places on the appropriate output channel line the Output Acknowledge (OA) signal. The subsystem reacts to the OA signal by accepting the output data word and by removing the ODR from the output channel. The subsystem then becomes ready to receive another output data word, and when it is ready, it again presents on ODR on the activated output channel.

If a terminal condition was not detected during the last data transfer and the channel is still active, the previously described sequence of activity is repeated. When the terminal condition is reached, the channel is deactivated. If the monitor bit (bit 16 of the BCWT) is active when the terminal condition is detected, an output monitor interrupt is generated.

B.3. ISI FUNCTION MODE

When the LFC instruction is executed, the channel specified by the K field is activated in the Function Mode and the two succeeding storage addresses are transferred to the output buffer control word addresses for that channel.

When a channel is active in the Function Mode, one or more External Function words may be transferred to the subsystem. The difference between the BCWT and the BCWI controls the number of External Function word transfers that occur. The activity performed by the IOM on a channel activated in the Function Mode is as follows:

(1) When the LFC instruction is executed, a signal called Force External Function (Force EF), which simulates the presence of an Output Data Request (ODR) to the IOM Priority network, is turned on in the IOM. The IOM in turn services the forced request as follows:

(a) The output BCWT and BCWI are read from the IGR. The word count difference is tested, and if the terminal condition is not detected, the channel is activated in the Function Mode. If the channel is 36 bits, the test is not performed until the second half of the Function word is being read. If the terminal condition is not detected, the channel remains active in the Function Mode.

(b) The BCWI is updated and restored to the IGR.

(c) The function word and a control signal called External Function (EF) are placed on the appropriate lines of the activated output channel.

(d) The EF signal is automatically turned off at a particular point in the IOM timing chain cycle which is servicing the forced request. This point occurs after the function word and the EF signal are placed on the output channel line, and after the use of the output BCWT and BCWI for the transfer of the EF word is completed.

(2) The subsystem reacts to the presence of the EF signal on the output channel by clearing data and control logic from the previous operation; it transfers the function word from the output data lines into its control section, and removes the ODR signal, if present, from the output channel. The function word is decoded in the control section of this subsystem, which thenreacts accordingly, and presents to the IOM either an ODR over the output channel or an IDR with an input data word via the input channel.

(3) If the conditioned subsystem presents an ODR to the IOM and the channel is active in the Function Mode, another External Function word is transferred to the subsystem. If the subsystem presents an ODR or IDR and the channel is not active in the Input or Output Mode, the requests are not serviced until the channel is activated by a LOC or LIC instruction.

APPENDIX C. FORMAT OF RESERVED LOCATIONS

000000	RESERVED
000001	INDEX REGISTERS
000010	
000011	RESERVED
000016	
000017	SCALE FACTOR SHIFT COUNT
000020	SUPERVISOR CALL ENTRANCE
000021	PARITY INTERRUPT IOM #0
000022	PARITY ERROR ADDRESS IOM #0
000023	DAY CLOCK INTERRUPT
000024	DAY CLOCK COUNT
000025	REAL-TIME CLOCK INTERRUPT
000026	REAL-TIME CLOCK COUNT
000027	PARITY ERROR MAIN STORE
000030	GUARD MODE INTERRUPT
000031	PARITY ERROR IOM #1
000032	PARITY ERROR ADDRESS IOM #1
000033	POWER LOSS INTERRUPT
000034	FLOATING POINT UNDERFLOW INTERRUPT
000035	FLOATING POINT OVERFLOW INTERRUPT
000036	ESI INTERRUPT IOM #0
000037	ESI INTERRUPT IOM #1
000040	IGR/ARITHMETIC PARITY INTERRUPT
000041	INTERRUPT LOCKOUT TIMEOUT

000100	INTERNAL INTERRUPT INPUT CHANNELS 0–15
000117	
000120	INTERNAL INTERRUPT OUTPUT CHANNELS 0–15
000137	
000140	EXTERNAL INTERRUPT CHANNELS 0–15
000157	
000160	EXTERNAL INTERRUPT STATUS CHANNELS 0–15
000177	
000200	PREVIOUS INTERNAL AND EXTERNAL INTERRUPT ASSIGNMENTS REPEATED FOR CHANNELS 16–31
000277	

000300	RESERVED
000301	
000302	OUTPUT BUFFER CONTROL WORD CHANNELS 1–15
000337	
000340	INTERRUPT TABLE POINTER IOM #0
000341	RESERVED
000342	INPUT BUFFER CONTROL WORDS CHANNELS 1–15
000377	
000400	OUTPUT BUFFER CONTROL WORDS CHANNELS 16–31
000437	
000440	INTERRUPT TABLE POINTER IOM #1
000441	RESERVED
000442	INPUT BUFFER CONTROL WORDS CHANNELS 17–31
000477	

APPENDIX D. INSTRUCTION REPERTOIRE SUMMARY

This appendix contains a complete list of the UNIVAC 418-III Instruction Repertoire. The table consists of the mnemonic operation codes, their octal equivalents, instruction execution time, and a short description.

AU	Upper Accumulator, 18-bit arithmetic register
AL	Lower Accumulator, 18-bit arithmetic register
A	AU and AL linked together to form one 36-bit arithmetic register
I	Indexable
S	SR sensitive
IR	The active Index Register
B	Same as IR
IAR	Instruction Address Register
DC	Compare Designator
M	(y), [y+(B)], [(y) AND (AU)], or [(y+(B)) AND (AU)] of compare instructions
NI	Next instruction
P	Same as IAR
SR	Special Register, 5 bay bits plus one active/inactive bit.
IRP	Index Register Pointer, 3 bits
y	The 17-bit storage address; consists of 12 low-order bits from u in the instruction and 5 high-order bits from IAR 16-12 or SR 5,3-0
K	The low-order 6 bits of the instruction
Z	The low-order 12 bits of the instruction, sign-extended to 18 bits
( )	Contents of an address or register
( )i	Initial contents of an address or register

( )f	Final contents of an address or register
(n)	Contents of the nth bit of a register
(y-1,y)	Contents of two consecutive storage locations linked together to form a 36-bit word. Address y - 1 contains the most significant half of the word; y contains the least significant half of the word.
	Indicates COMPARISON when used in logical expressions
( ) AND ( )	Bit-by-bit or logical product (logical AND) defined by the following table:

	0	1
0	0	0
1	0	1

( ) OR ( )	Logical sum (inclusive OR) defined by the following table:

	0	1
0	0	1
1	1	1

( ) XOR ( )	Logical difference (exclusive OR) defined by the following table:

	0	1
0	0	1
1	1	0

( )'	One's complement of the contents of an address or register
( )•( )	Algebraic product of the contents of two locations
→	Transfer of the quantity stated at the left of the symbol to the address or register stated at the right of the symbol
[ ]	Used to group terms. The brackets do not signify 'the contents of'
*	Optional instruction

Subscripts specify bit positions in the register or quantity subscripted, *n* being each bit position labelled from right to left from 0 to 17.

	MNEMONIC CODE	MACHINE CODE	TYPE: OPERAND TYPE	TYPE: OPERATION TYPE	TIME US	OPERATION	DESCRIPTION
ARITHMETIC	AL	14	Y	I,S	1.5	(AL)+(Y)→ AL	Add to AL
	AA	20	Y	I,S	2.5	(A)+(Y−1,Y)→ A	Add to A
	ALK	71	Z	−−	1.0	(AL)+Z→ AL	Add KONSTANT to AL
	ANL	16	Y	I,S	1.5	(AL)−(Y)→ AL	Add Negatively to AL
	ANA	22	Y	I,S	2.5	(A)−(Y−1,Y)→ A	Add Negatively to A
	M	24	Y	I,S	6.5	(AL)×(Y)→ A	Multiply AL
	D	26	Y	I,S	6.5	(A)÷(Y)→ AL;REM→ AU	Divide A
	RND	5060	−	−	1.75	If (A) positive and (AL_{17}) =1, (AU)+1→ AL; If (A) negative and (AL_{17})=0, (AU)-1→AL; if otherwise, (AU)→ AL	Round A
	*FA	5002	Y	I,S	4.0+ x/8	(A)+(Y−1,Y)→ A	Float Add to A
	*FS	5003	Y	I,S	4.0+ x/8	(A)−(Y−1,Y)→ A	Float Subtract from A
	*FM	5004	Y	I,S	11.0	(A)×(Y−1,Y)→ A	Float Multiply A
	*FD	5005	Y	I,S	11.0	(A)÷(Y−1,Y)→ A	Float Divide A
LOGICAL	AND	52	Y	−−	1.5	(AL) AND (Y)→ AL	AND; Set AL_n=0 for (Y_n=0)
	OR	51	Y	−−	1.5	(AL) OR (Y)→ AL	Inclusive OR; Set AL_n=1 for (Y_n=1)
	XOR	53	Y	−−	1.5	(AL) XOR (Y)→ AL	Exclusive OR; Complement AL_n for (Y_n=1)
	CPL	5061	−−	−−	1.75	−(AL)→ AL	Complement AL
	CPU	5062	−−	−−	1.75	−(AU)→ AU	Complement AU
	CPA	5063	−−	−−	1.75	−(A)→ A	Complement A

	MNEMONIC CODE	MACHINE CODE	TYPE: OPERAND TYPE	TYPE: OPERATION TYPE	TIME US	OPERATION	DESCRIPTION
TRANSFER	LU	10	Y	I,S	1.5	$(Y) \rightarrow AU$	Load AU
	LL	12	Y	I,S	1.5	$(Y) \rightarrow AL$	Load AL
	SU	46	Y	I,S	1.5	$(AU) \rightarrow Y$	Store AU
	SL	44	Y	I,S	1.5	$(AL) \rightarrow Y$	Store AL
	LLK	70	Z	--	1.0	$Z \rightarrow AL$	Load AL with KONSTANT
	MSL	04	Y	I,S	1.5	$(Y_N) \rightarrow AL_N$ for $(AU_N)=1$	Masked Selective Load AL
	SAD	74	Y	--	2.25	$(AL_{11-0}) \rightarrow Y_{11-0}$	Store Address of AL
	LB	32	Y	I,S	1.5	$(Y) \rightarrow IR$	Load the Active B Register
	SB	42	Y	I,S	.75	$(IR) \rightarrow Y$	Store the Active B Register
	LBK	36	Z	I	.75	$Z \rightarrow IR$	Load B with KONSTANT
	LIR	5072	K	--	2.5	$K_{2-0} \rightarrow IRP$	Load Index Res. Pointer
	SIR	72	Y	--	2.25	$IRP \rightarrow Y_{3-0}$; $0 \rightarrow Y_{5,4}$ If $(IRP)=0, Y_3=1$ If $(IRP)\neq 0, Y_3=0$	Store Index Reg. Pointer (IRP points to IR 10_8 when loaded with 0)
	LSR	5073	K	--	1.0	$K_{5-0} \rightarrow SR$	Load Special Register
	LSD	5020			2.50	$((IAR)+1)_{5-0} \rightarrow SR$ $((IAR)+1)_{10} \rightarrow$ Overflow designator $((IAR)+1)_{11} \rightarrow$ Borrow designator	Load Special Designators
	SSR	75	Y	--	2.25	$(SR) \rightarrow Y_{5-0}$; $0 \rightarrow SR_4$	Store Special Register and Inactivate SR
	SSD	5017			2.50	$(SR) \rightarrow [(IAR)+1]_{5-0}$ Overflow designator $\rightarrow [(IAR)+1]_{10}$ Borrow designator $\rightarrow [(IAR)+1]_{11}$	Store Special Designators
	CY	40	Y	I,S	1.5	$0 \rightarrow Y$	Clear Y to Binary Zeros
	*FP	5006	Y	I,S	3.0+ x/8	(A) normalized (mantissa) $\rightarrow A_{35}, A_{26-0}$, If $A_{35}=0$, $(Y_{7-0}) \rightarrow A_{34-27}$ If $A_{35}=1$, $(Y_{7-0})' \rightarrow A_{34-27}$	Floating Point Pack
	*FU	5007	Y	I,S	3.0	If $A_{35}=0$, $(A_{34-27}) \rightarrow Y_{7-0}$, 0's $\rightarrow Y_{17-8}$; If $A_{35}=1$, $(A_{34-27})' \rightarrow Y_{7-0}$, 0's $\rightarrow Y_{17-8}$; (A_{35}, A_{26-0}) sign extended $\rightarrow A$	Floating Point Unpack
	*DB	5074	--	--	9	$(AU_{15-12,\ 9-6,\ 3-0}) \rightarrow AL$	Dec. to Bin. Conversion
	*BD	5075	--	--	9	$(AL) \rightarrow AU_{15-12,\ 9-6,\ 3-0}$	Bin. to Dec. Conversion
	BT	5070	K	--	1+1.5K	$(Y_{AU}) \rightarrow Y_{AL}$; incr.	Block Transfer

	MNEMONIC CODE	MACHINE CODE	TYPE: OPERAND TYPE	TYPE: OPERATION TYPE	TIME US	OPERATION	DESCRIPTION
SHIFT	SRU	5041	K	--	1.25+ K/8	Shift Right AU } K bit positions; end-off	Shift AU Right
	SRL	5042	K	--	1.25+ K/8	Shift Right AL } K bit positions; end-off	Shift AL Right
	SRA	5043	K	--	1.25+ K/8	Shift Right A } K bit positions; end-off	Shift A Right
	SLU	5045	K	--	1.25+ K/8	Shift Left AU } K bit positions; end-around	Shift AU Left
	SLL	5046	K	--	1.25+ K/8	Shift Left AL } K bit positions; end-around	Shift AL Left
	SLA	5047	K	--	1.25+ K/8	Shift Left A } K bit positions; end-around	Shift A Left
	SCA	5044	K	--	2.0+ K/8	Shift Left (End-Around) K Bit Pos. or until normalized; K less actual shift→000017_8	Scale A; Store Scale Factor in absolute Location 17_8
LOOP CONTROL	JBNZ	73	Y	--	1.0	If (IR)≠0, (IR)−1→ IR, Y→ IAR; If (IR)=0, (IAR)+1→ IAR	Jump if B Register Non-Zero
	TB	56	Y	--	2.0	If (IR)=(Y), (IAR)+2→ IAR; If (IR)≠(Y), (IR)+1→ IR, (IAR)+1→ IAR	Test B Register for Equality
	TZ	57	Y	--	2.5	If (Y)=0,(IAR)+2→ IAR; If (Y)≠0,(Y)−1→ Y, (IAR)+1→ IAR	Test location for Zero
COMPARE	CL	02	Y	I,S	1.5	(AL):(Y), Set Comp. Designator accordingly	Compare AL Algebraically
	CLM	06	Y	I,S	1.75	[(AU) AND (AL)]:[(AU) AND (Y)], set Comp. Designator accordingly	Compare AL Masked by AU
CONDITIONAL JUMP CD. SET	JE	60,61	Y	--	.75	If CD. set to=condition) } Y→ IAR	Jump on Equal
	JNE	62,63	Y	--	.75	If CD. set to≠condition } Y→ IAR	Jump on Not Equal
	JLS	66,67	Y	--	.75	If CD. set to<condition } Y→ IAR	Jump on Less
	JNLS	64,65	Y	--	.75	If CD. set to not<condition } Y→ IAR	Jump on Not Less

	MNEMONIC CODE	MACHINE CODE	TYPE: OPERAND TYPE	TYPE: OPERATION TYPE	TIME US	OPERATION	DESCRIPTION
CONDITIONAL JUMP CD. NOT SET	JUZ	60	Y	--	.75	If (AU)=0 → Y→ IAR	Jump on AU Zero
	JUNZ	62	Y	--	.75	If (AU)≠0 → Y→ IAR	Jump on AU Nonzero
	JUP	64	Y	--	.75	If (AU) Is Positive → Y→ IAR	Jump on AU Positive
	JUN	66	Y	--	.75	If (AU) Is Negative → Y→ IAR	Jump on AU Negative
	JLZ	61	Y	--	.75	If (A) = 0 → Y→ IAR	Jump on AL Zero
	JLNZ	63	Y	--	.75	If (AL)≠ 0 → Y→ IAR	Jump on AL Nonzero
	JLP	65	Y	--	.75	If (AL) Is Positive → Y→ IAR	Jump on AL Positive
	JLN	67	Y	--	.75	If (AL) Is Negative → Y→ IAR	Jump on AL Negative
UNCONDITIONAL JUMP	J	34	Y	I	.75	Y→ IAR	Jump
	JI	55	Y	--	1.5	(Y_{16-0})→ IAR	Jump Indirect
	EJI	54	Y	--	1.5	Enable interrupts; (Y_{16-0})→IAR	Enable Interrupts and Jump Indirect
	SLJ	76	Y	--	1.5	(IAR)+1→ Y; Y+1→ IAR	Store Location and Jump
	SLJI	30	Y	I	2.25	(IAR)+1→ (Y); (Y)+1→ IAR	Store Location and Jump Indirect
SKIP	TK	5050	K	--	1.0	If Keys designated by K are set, (IAR)+2→ IAR	Test Keys
	TNB	5051	--	--	1.0	If borrow indicator off → (IAR)+2→IAR	Test No Borrow
	TOF	5052	--	--	1.0	If overflow indicator on → (IAR)+2→IAR	Test Overflow
	TNO	5053	--	--	1.0	If overflow indicator off → (IAR)+2→IAR	Test No Overflow
	TOP	5054	--	--	2.0 Min.	If sum of 1's in (AU) AND (AL) is odd → (IAR)+2→IAR	Test Odd Parity
	TEP	5055	--	--	2.0 Min.	If sum of 1's in (AU) AND (AL) is even → (IAR)+2→IAR	Test Even Parity

	MNEMONIC CODE	MACHINE CODE	TYPE: OPERAND TYPE	TYPE: OPERATION TYPE	TIME US	OPERATION	DESCRIPTION
PRIVILEGED	LGM	5065	--	--	1.75	$((IAR)+1)_{17-9} \rightarrow$ Upper Storage Limit $((IAR)+1)_{8-0} \rightarrow$ Lower Storage Limit, Guard Mode is set, and $(IAR)+2 \rightarrow IAR$.	Load Guard Mode
	LIC	5011	K	--	4.0 Min.	Load I/O channel K from $(IAR)+1$ and $(IAR)+2$, initiate input, $(IAR)+3 \rightarrow IAR$	Load Input Channel
	LOC	5012	K	--	4.0 Min.	Load I/O channel K from $(IAR)+1$ and $(IAR)+2$, initiate output, $(IAR)+3 \rightarrow IAR$	Load Output Channel
	LFC	5013	K	--	4.0 Min.	Load I/O channel K from $(IAR)+1$ and $(IAR)+2$, initiate external function, $(IAR)+3 \rightarrow IAR$	Load External Function Channel
	STIC	5015	K	--	1.75 Min.	Stop input on channel K	Stop Input on Channel
	STOC	5016	K	--	1.75 Min.	Stop output on channel K	Stop Output on Channel
	TIC	5021	K	--	1.0	If input channel K is idle, $(IAR)+2 \rightarrow IAR$	Test Input on Channel
	TOC	5022	K	--	1.0	If output channel K is idle, $(IAR)+2 \rightarrow IAR$	Test Output on Channel
	TFC	5023	K	--	1.0	If external function channel K is idle, $(IAR)+2 \rightarrow IAR$	Test External Function on Channel
	WFI	5024 5025	--	--	1.0	Stop cpu (but not I/O) until interrupt	Wait for interrupt
	EEI	5067	K	--	1.0	Enable ESI interrupt in IOM_1 if K=0, in IOM_2 if $K=020_8$	Enable ESI Interrupts
	SK	5056	K	--	1.0	If in Guard Mode, $(IAR)+1 \rightarrow IAR$, otherwise stop if keys specified by K set	Stop on Key Setting if not in Guard Mode
	SAA	5066	--	--	1.0		Sound Audible Alarm
INTERRUPT CONTROL	PAI	5034 5035	--	--	1.0	Prevent all IOM generated interrupts	Prevent All Interrupts
	AAI	5030 5031	--	--	1.0	Remove lockout on all IOM generated interrupts	Allow All Interrupts
MISC.	RS	5010	Y	I,S	2.5	$(Y) \rightarrow AL$, $1 \rightarrow Y_{17}$	Read and Set
	NOP	5026 5036 5037	Y	--	1.0	$(IAR)+1 \rightarrow IAR$	No Operation

APPENDIX E. MAINTENANCE PANEL

This appendix lists the switches and indicators of the UNIVAC 418-III System Maintenance Panel and gives a brief functional description of each.

Operation and Reset Controls

SWITCH ENABLE Alternate action switch-indicator	Disconnects all neon pushbuttons and the following push switches on the maintenance panel: Rd Next Instr, Storage Parity Intp, Stop on Parity, IOM #0 Test, IOM #1 Test, Arith Test. Indication is unaffected by this switch.
STOP Momentary switch-indicator	Stops C/A-I/O operation and lights the indicator. Normally, it stops at the end of the main timing chain (TO) allowing previously initiated I/O operations to continue.
RUN Momentary switch-indicator	Starts processing and lights the indicator. When in phase, cycle, or instruction rate mode, pushing the run switch issues a clock phase signal, a clock cycle signal, or initiates one sequence arithmetic or I/O.
PROCESSOR RESET Momentary switch	If the processor is stopped, clears section and both IOM's but not the peripherals, to allow starting.
SUBSYSTEM RESET Momentary switch	If the C/A-I/O is stopped, sends a clear signal to each peripheral subsystem.

Disable Controls

The following controls are alternate-action switches. Pressing the switch causes the function listed to occur and lights its indicator. Pressing the switch again reverses or cancels the function and turns the indicator off.

DAY CLOCK	Disables the day-clock, lights its indicator, and lights the DAY CLOCK DISABLE indicator on the operator's panel.
REAL TIME CLOCK	Disables the real-time clock, lights its indicator, and lights the REAL TIME CLOCK DISABLE indicator on the operator's panel.
RD NEXT INSTR	Stops and holds FO, and lights the PROCESSOR DISABLE indicator on the operator's panel.
STORAGE PARITY INTERRUPT	Disables control storage and main storage parity interrupts, lights the indicator, and lights the PROCESSOR DISABLE indicator on the operator's panel.

Selective Stops	
SELECT STOPS 5 switch-indicators and 5 clear switches (0 through 4)	Pushing a switch sets an associated stop flip-flop and lights the indicator. Pressing a clear switch resets the flip-flop and turns the indicator off. Used as a group in conjunction with the stop instruction.
STOPS 6 Indicators (0 through 5)	Indicate that program has stopped as selected. If any of the bits 4-0 in the K-field of the stop (5056) instruction agree with the setting of the five flip-flops, or if bit 5 of the instruction is a 1, the processor stops after completing the instruction. Pushing the RUN switch on the operator's panel restarts the program at the location specified by P. If the K-field does not agree with the flip-flops, or if it is in Guard Mode, the stop is ignored.

Selective Skips	
SELECT SKIPS 5 switch-indicators and 5 clear switches (0 through 4)	Pushing a switch indicator sets an associated flip-flop and lights its indicator. Pushing a clear switch clears the flip-flop and turns the indicator off. Used individually in conjunction with the Stop-on-Keys instruction (SK). If the number in the K-field of the SK instruction is the same as the number of one of the flip-flops that is set, or if K = 40, the program skips to location P+2. If not, the program goes to the next instruction.

Breakpoint Controls	
BREAKPOINT STOP Indicator	Lights when the breakpoint flip-flop is set, stopping the processing at the end of the main timing chain.
SELECT BKPT READ & BKPT WRITE	Controls breakpoint stops. Pushing a switch sets an associated flip-flop and lights the indicator. Pushing CLR clears the flip-flops.

NOTE: These switches may be used, separately or jointly. If BKPT WRITE flip-flop is set the processing halts when the contents of S register are equal to the contents of the BKPT register, and a write is attempted. If the BKPT READ flip-flop is set, the processing halts on any reference other than a write. If both are set, the processing halts on any address compare.

Check Indicators

When a check flip-flop is set, its associated indicator lights and the alarm at the operator's console sounds.

PROCESSOR CHECK	Indicates an air or temperature fault in either the C/A or storage cabinet. Indicates a power failure in either storage cabinet.
PARITY CHECKS Storage A Parity Storage B Parity	Each indicates a parity error in associated main storage module.
IGR 0 Parity IGR 1 Parity	Each indicates a control register parity error in associated IOM.

Check Switches	
AUDIO RESET	Clears any of the above fault indications on the maintenance panel and operator's console if the fault itself has been corrected. Clears the audio alarm if the fault has been corrected. Also resets a programmed audio alarm.

Clock Rate Controls

These four switch-indicators set flip-flops to select the rate of processing operation in various ways. Only one rate can be in effect at a time. Before making a new rate selection the CL button must be pushed to clear the previous selection; normal rate can be cleared only if processing is stopped. If cycle rate or phase rate is in effect, the arithmetic section or either IOM can be disabled or stopped by a toggle switch. Clocking for arithmetic section and both IOM's runs at the rate selected.

NORMAL Switch-indicator	Selects the normal rate of instruction execution. Clock pulses are issued at the normal rate whether stopped or running.
SEQUENCE Switch-indicator	Causes arithmetic section to run at sequence rate; the IOM's continue at rate taye unless switched into test mode. If the IOM's are in test mode, they also run at sequence rate. Sequence rate means passing through a timing chain. This does not necessarily complete a transfer or instruction.
CYCLE Switch-indicator	Selects the clock-cycle of operation. One cycle (4 phases) is completed each time the RUN switch is pressed.
PHASE Switch-indicator	Selects the clock-phase rate of operation. Starting with phase 4, one clock phase is issued each time the RUN switch is pressed. Another rate cannot be selected unless the next phase to be issued is phase 4.
CL Switch	Clears the rate control flip-flops.

Phase Controls (used with clock phase rate of operation)

DISTRIBUTOR 4 Switch-indicators (1 through 4)	Pressing a switch sets the associated phase-step distributor flip-flop and lights the indicator. The distributor is used for clock-phase rate to issue the clock phases in sequence. The next clock phase is issued as indicated.
CLR Manual-clear switch	Clears the four phase-step distributor flip-flops.
PHASE REPEAT One switch-indicator and manual clear switch marked CLR	Sets the phase repeat flip-flop when when in clock-phase rate to prevent the advance of the phase-step distributor. Therefore, the distributor continously issues the clock phase indicated by the phase distributor.

Arithmetic Toggle Switches	
(1) Disable Arithmetic	This switch facilitates manual checkout of the IOM sections by disabling the C/A section.
(2) Disable K = 0	Permits continuous cycling of K-conditioned instructions.

(3) Maintenance Write	Permits continuous cycling of K-conditioned instructions. Permits writing of portions or all of storage depending upon setting of other switches such as RD NEXT INSTR and K = 0. With this switch set, the function is placed in F, the starting address in AL, the data pattern in W; the run switch is then pressed.
(4) Maintenance Read	Cycling is provided in a manner similar to maintenance write. Place address in AU and check for parity errors with *Stop on Parity* set.
(5) Disable Address Increment	Permits maintenance read and write to one storage location.
(6) Disable ADV P	Permits repeated execution of the same instruction from storage.

IOM Disable Toggle Switches

These switches are activated to one or both IOM's by the IOM #0 and/or IOM #1 test switches.

(1) Disable Address Increment	This switch prevents update of any buffer control word and allows the IOM to cycle with peripherals for testing and scoping.
(2) Disable Function Priority	This switch facilitates checkout of arithmetic section (and IOM's) by preventing: (a) Transfers from IOM to arithmetic section (b) Modification of BCW's by arithmetic section.
(3) IOM Stop	This switch causes the stop FF to block IOM scan logic in addition to the arithmetic section timing. It can be used to stop I/O transfers when a breakpoint stop occurs.
(4) Back to Back	This switch prevents setting of EF-active flip-flops and disables compatible lockout. This switch must be active in order to run back-back.

UNIVAC
418-III

PROCESSOR AND STORAGE
UP-7627

UNIVAC SYSTEMS PROGRAMMING LIBRARY SERVICES RELEASE

UNIVAC 418-III Real-Time System Library Memo 3 announces the release and availability of "UNIVAC 418-III Real-Time System Processor and Storage Programmers Reference," UP-7627, covers and 61 pages. This is a Standard Library Item (SLI).

This manual describes the three individual hardware sections of the UNIVAC 418-III Real-Time System. The interfacing between the three sections is discussed and illustrated throughout this manual.

Major headings in the Table of Contents are:

1. MAIN STORAGE
2. COMMAND/ARITHMETIC
3. INPUT/OUTPUT

Distribution of this manual, UP-7627, is being made as indicated below. Additional copies of UP-7627 may be requisitioned from Holyoke, Massachusetts, via a Sales Help Requisition through your local Univac Manager.

The following is a recap of current items for the 418-III System:

UP Number	Title	Release Date
UP-7612	418-III System Binder	June 7, 1968
UDI-723 (Rev. 12-67)	Set - Template and Instruction Booklet	March 29, 1968
UDI-1604	Vocabulary for Information Processing	October 24, 1968
UP-3910.5	Software System Field Report Procedures	May 11, 1964
UP-3910.10	General Software Category Report	March 29, 1968
UP-7503 SERIES	Set of 18 Tabs for COBOL Series	June 16, 1967
UP-7503 Rev. 1	Fundamentals of COBOL - Contents Section	December 23, 1968
UP-7503.1 Rev. 1	Fundamentals of COBOL - Language	December 23, 1968
UP-7503.2 Rev. 1	Fundamentals of COBOL - Table Handling	December 23, 1968
UP-7503.3 Rev. 1	Fundamentals of COBOL - Sorting	December 23, 1968
UP-7513	Binder for COBOL	June 16, 1967
UP-7515	Binder for FORTRAN	January 12, 1968
UP-7536	Fundamentals of FORTRAN (with 10 Index Tabs)	January 12, 1968
UP-3910.11	Update "A" to Fundamentals of FORTRAN, UP-7536	September 20, 1968
UP-3910.12	Update "B" to Fundamentals of FORTRAN, UP-7536	October 14, 1968
UP-7641	Assembler Programming Form	October 4, 1968
UP-7576	System Description	June 4, 1968
UP-7599	Assembler Programmers Reference	June 24, 1968
UP-7659	Programmers Hardware and Software Reference	December 20, 1968
UP-7627	Processor and Storage Programmers Reference	

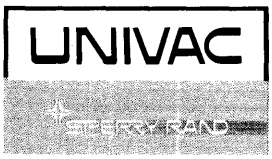
MANAGER
Documentation and Library Services

TO LISTS:

ATTACHMENTS: UP-7627 plus Library Memo 3 to Lists 10U, 217, 630, 692 and S.P.L.S. Lists 57 and 58.

THIS SHEET IS: UNIVAC 418-III Real-Time System Library Memo 3.

DATE: March 28, 1969



UP-7627