

M.A. Breslin
Logical Design

UNIVAC III
Data Interface for I/O

The attached charts indicate the word formats used for communication between the memory and I/O devices. Chart 1 is the read information and Chart 2 is the write information. The read information in CCSC that is^x indicates available only when SCR is read.

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MAB/ne
11/25/60

Rev. A 11/21/60

Chart I

<u>Time</u>	<u>CCSTb</u>			<u>CCSCb</u>				<u>CCSCKb</u>			
	<u>3</u>	<u>2</u>	<u>1</u>	<u>4</u>	<u>3</u>	<u>2</u>	<u>1</u>	<u>4</u>	<u>3</u>	<u>2</u>	<u>1</u>
TP4	25	27	13	24 ^x	23 ^x	22 ^x	21 ^x	19	13	07	01
5	24	26	21					20	14	08	02
6	23	22	20					21	15	09	03
7	06	12	19					22	16	10	04
8	05	11	18	04	03	02	01	23	17	11	05
0	04	10	17	08	07	06	05	24	18	12	06
1	03	9	16	12	11	10	09	25	27	26	26
2	02	8	15	16 ^x	15	14	13				
3	01	7	14	20 ^x	19 ^x	18 ^x	17 ^x				

From CP Register to HST Slave Reg.

From CP Register to

From CP Register to GP Slave Reg.

Chart 2

	<u>HS_bCP</u>			<u>CRB_b</u>				<u>CMWG_b</u>			
	<u>3</u>	<u>2</u>	<u>1</u>	<u>4</u>	<u>3</u>	<u>2</u>	<u>1</u>	<u>4</u>	<u>3</u>	<u>2</u>	<u>1</u>
2	13	07	01					19	13	07	01
3	14	08	02					20	14	08	02
4	15	09	03	04	03	02	01	21	15	09	03
5	16	10	04	08	07	06	05	22	16	10	04
6	17	11	05	12	11	10	09	23	17	11	05
7	18	12	06	16	15	14	13	24	18	12	06
8	19	22	23	20	19	18	17	25	27	26	X
0	20	26	24	24	23	22	21				
1	21	27	25	X	27	26	25				
2											

From HST to Write Register

From AR to Write Register

From GP Channel to Write Register

Univac III Instruction

<u>Binary Code</u>	<u>Octal Code</u>	<u>Description</u>	<u>CVRG</u>	<u>Single word time (usec)</u> **
<u>Bits</u> (20-15)				
Skip console instructions				
000 000	00	Skip	00	9.0
000 001	01	Typewriter → ARi	01	9.0
000 010	02	(m') → Typewriter ARi select character	02	9.0
000 011	03	(m') → Display	03	9.0
Control Instructions				
000 100	04	(MAC) → m'	68	13.5
000 101	05	(TCWR) → m'	05	13.5
000 110	06	m' → CC	49	4.5
000 111	07	m' +1 CC, CC+1 → m'	07,68	13.5
Information Transfer Instructions				
001 000	10	(ARi) → (m')	48	9.0
001 001	11	-(ARi) → (m')	11,48	9.0
001 010	12	(m') → ARi	18,28,59	9.0
001 011	13	-(m') → ARi	13,18,28,59	9.0
Logical Operations				
001 100	14	Extract (m') → (ARi)	14,59	13.5
001 101	15	(ARi) (m') → ARi	15,18,59	9.0
001 110	16	(ARi) (m') → ARi	16,59	
001 111	17			
Arithmetic Instructions				
010 000	20	(m') (ARi) → ARi, Decimal	8,18,59	9.0
010 001	21	-(m')+(ARi) → ARi, Decimal	8,18,29	9.0
010 010	22	(m')+(ARi) → ARj		9.0
		(m') +(AR1,AR2) → AR3,AR4,	8,9,29	13.0
010 011	23	-(m') +(ARi) → ARj		9.0
		-(m') +(AR1,AR2) → AR3, AR4, Decimal	8,9,29	13.5

<u>Binary Code</u>	<u>Octal Code</u>	<u>Description</u>	<u>CVRG</u>	<u>Single word time (usec)</u>
010 100	24	(m')+(ARi) → ARi, Binary	8,18,38	9.0
010 101	25	-(m')+(ARi) → ARi, Binary	8,18,38	9.0
010 110	26	(m')+(ARi) → ARj		9.0
		(m')+(AR1,AR2) → AR3, AR4 Bin.	8,9,38	13.5
010 111	27	-(m')+(ARi) → ARj		9.0
		-(m')+(AR1,AR2) → AR3, AR4, Bin.	8,9,38	13.5
011 000	30	(AR1)(m') → AR2, AR3	30	54-139.5
011 001	31	(AR1,AR2)/(m') → AR1 (Remainder) & AR2 (Quotient).	31	76.5-162
011 010	32	#Double Precision Multiply		
011 011	33	#Double Precision Divide		

Compare Instructions

011 100	34	#Floating Point Add		
011 101	35	#Floating Point Subtract		
011 110	36	#Floating Point Multiply		
011 111	37	#Floating Point Divide		

~~Shift Instructions~~

100 000	40	Right Decimal Shift	40	18*
100 001	41	Left Decimal Shift	41	13.5*
100 010	42	Right Alphabetical Shift	42	21.5*
100 011	43	Left Alphabetical Shift	43	13.5*
100 100	44	Right Binary Circular Shift	44	18-27***
100 101	45			
100 110	46	#Convert Floating to Fixed Decimal		
100 111	47	#Convert Fixed to Floating Decimal		

Index Register Instructions

101 000	50	(IR') → m'	50	13.5
101 001	51	(m') → IR'	51,58	13.5
101 010	52	(m')+(IR') → IR'	52,58	13.5
101 011	53	IR Modifier+(IR') → IR' (IR'): (m') 10-24;	53	18.0
101 100	54	(ARi):(m')	8,39	9.0
101 101	55	1(ARi)1:(m')	8,39,55	9.0
101 110	56	(ARi:ones):(m'zeros)	8	9.0
101 111	57	(ARi ones):(m'ones)	8,57	9.0

Flip-Flop Instructions

110 000	60	Test FF ARi	60	9.0
110 001	61	Reset FF ARi	61	9.0
110 010	62	Set FF ARi	62	9.0
110 011	63			

<u>Binary Code</u>	<u>Octal Code</u>	<u>Description</u>	<u>CVRG</u>	<u>Single word time (usec)</u>
110 100	64	Test FFm	64	9.0
110 101	65	Reset FFm	65	9.0
110 110	66	Alert Keyboard	66	9.0
110 111	67			

Input-Output, Special Data Editing Instructions

111 000	70	Initiate Input-Output	70	13.5
111 001	71	Expand (ARi) → m'		58.8
111 010	72	Compress (m') → ARi		58.8
111 011	73	Zero Suppress (m') → ARi	73	9.0
111 100	74	Translate 90 Column Card Code to machine code (m') → ARi		18.0*
111 101	75	Translate Machine Code to 90 Column Card Code (m') → ARi		18.0*
111 110	76	##Real Time Clock → AR4	76	
111 111	77	Stop and Transfer	49,77	9.0

** Add 4.5 usec for each additional word in operand
Except where marked*:

Time for 2 word shifts: 40 if shift > 6, 18 ; ≤6, 31.5
 41 if shift > 6, 13.5; ≤6, 27
 42 if shift > 4, 22.5; ≤4, 49.5
 43 if shift > 4, 13.5; ≤4, 40.5

*** Shift times for instr. 44 if shift n ≤ 7, 18
 7 < n ≤ 16, 22.5
 16 < n , 27.0

For 90 Col. translates, add 13.5 usec for each additional word.

For recomplement, add 4.5 usec/word.

For indirect addressing, add 4.5 usec/level.

Field selection same time as indirect addressing.

##Reserved for programmed subroutines via "Invalid" Op code interrupt.

Optional

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Function Table Signal List - Univac III Central Processor

<u>FTS.</u>	<u>Polarity</u>	<u>Print</u>	<u>Description</u>
100	+	138	Address I.R. output
101	+	138	Address MAC output
102	+	138	CMMB → CMAS
103	+	138	CCR → CMAM
104	-	143	1111 → CMAM .
105	+	138	CMD → CMAS
106	+	014	Address IR input
107	+	138	Address MAC input
108	+	138	CMMB → CMD
109	+	138	CMAF → CMS
110	+	012	CCR → CAAS
111	+	012	CRB → CAAM
112	+	015	CCR → CAAM
113	+	015	CCR → CAAS
114	+	012	2 x CCR → CAAS
115	+	012	Decimal Correction in CAC
116	+	012	Check CACO
117	-	015	Check Zeros → CAAS
118	-	015	Binary Zeros → CAAM
119	+	013	CRB → CAAS
120	+	012	CACO → CR
121	+	138	10 ⁻¹ CMW → CMW
122	+	009	CCR → CRA
123	+	012	Clear CR ₁
124	+	012	CR ₂
125	+	012	CR ₃
126	+	012	CR ₄
127	+	009	CMR → CRA
128	+	013	Address CRA as input
129	+	013	Address CRA-1 as input
130	+	142	U2BCP → CMW
131	+	142	HS2CP → CMW
132	+	142	CMWG1 → CMW
133	+	142	CMWG2 → CMW
134	+	142	3 → CMW
135	+	142	4 → CMW
136	+	142	5 → CMW
137	+	142	6 → CMW
138	+	142	7 → CMW
139	+	142	8 → CMW
140	+	012	CMR → CCS
141	+	012	CMR → CCR

<u>FTS.</u>	<u>Polarity</u>	<u>Print</u>	<u>Description</u>
142	-	012	Clear CCS'
143	-	014	Clear CCR
144	-	014	Binary Zeros → CCR
145	-	009	Binary Zeros → CCR 25 → 28
146	+	014	10 ⁻¹ CCR → CCR
147	-	015	CRB → CCR 25 - 28
148	+	142	CMWG _n , U ₂ BCP, HS2CP → CMW
149	+	142	CMWG _n → CMW
150	+	009	CMR → CCSFB
151	+	009	Clear CCFSB
152	-	128	Inhibit CMD - CMS
153	-	128	Inhibit CMD → CMS.
154	-	143	-1 → CMAF ₄
155			
156	+	110	CMS → CMMONO1
157	+	110	CMS → CMMONO2
158	+	110	03
159	+	110	04
160	+	110	05
161	+	110	06
162	+	110	07
163	+	110	08
164	+	110	09
165	+	110	10
166	+	110	11
167	+	110	12
168	+	110	13
169	+	110	14
170	+	110	15
171	+	139	Clear IR 01
172	+	139	02
173	+	139	03
174	+	139	04
175	+	139	05
176	+	139	06
177	+	139	07
178	+	139	08
179	+	139	09
180	+	139	10
181	+	139	11
182	+	139	12
183	+	139	13
184	+	139	14
185	+	139	15
186	+	010	Divide - Stage 1 FF
187	+	010	Divide - Stage 2 FF
188	+	012	CMMONO2 → CCFSB
189	+	013	CCFB ₅₋₉ → CCFSB ₀₋₄

<u>FTS.</u>	<u>Polarity</u>	<u>Print</u>	<u>Description</u>
190	+	013	CCFSB+1 → CCFSB
191	+	013	CCFSB-1 → CCFSB
192	+	012	CMM0102 → CCFSB ₀
193	+	011	CCQ → CR12 - 42
194	+	011	CR12 - 42 → CCFSB
195	+	010	1ER _n 1 → IER _n
196	+	010	CRA11-41 → CCQ
197		010	CCQ ±1 → CCQ
198	+	010	IER _n -1 → IEEN
199	+	010	Multiply FF
200	+	139	Clear SCR 1
201	+	139	2
202	+	139	3
203	+	139	4
204	+	110	CMS → CMMATR 1
205	+	110	2
206	+	110	3
207	+	110	4
208	+	143	CCSC → CMMATR 1
209	+	143	CCSC → 2
210	+	143	CCSC → 3
211	+	143	CCSC → 4
212	-	141	+2 → CMA
213	+	141	UA → CMA
214	+	138	-CCR → CMAM
215	+	015	Reset FF AR _m
216	+	015	Test FF AR _m
217	+	015	Set FF AR
218	+	015	Reset FF AR
219	+	015	Test FF AR
220			
221			
222	+	140	CCSC → CMMONO3
223	+	140	04
224	+	140	05
225	+	140	06
226	+	140	07
227	+	140	08
228	+	140	09
229	+	140	10
230	+	140	11
231	+	140	12
232	+	140	13
233	+	140	14
234	+	140	15
235	+	013	Address CRA as Output
236	+	013	Address CRA+1 as Output
237	+	013	Address CRA+2 as Output
238	+	013	Address CRA+3 as Output

<u>FTS.</u>	<u>Polarity</u>	<u>Print</u>	<u>Description</u>
239	+	015	Detect = on IR. comp.
240	-	015	Set = FF
241	+	015	Reset = FF
242	+	015	Set >, < FF
243	+	015	Set >, < FF
244	+	015	CCFSB → CMS
245	+	138	CMS → CMS
246			
247		087	CCS → Display
248	+	013	Address SCR from CRA
249	+	014	2-1 CCR → CCR
250	+	015	Set Standby Unavailable FF AR
251			
252			
253			
254			
255			
256			
257	+	014	CCR ₀₁ → CCR ₂₅
258			
259	+	011	Check CCQ
260	+	009	CCR → CVR
261		015	Inhibit CCR ₀₁₋₀₄ → CCR ₂₅₋₂₈
262	-	011	Clear to Decimal Zeros CCFSB ₆₋₉
263	-	015	CCFSB → CAAS
264	+	015	-(CCR ₂₅) → CR
265	+	015	-(CR ₂₅) → CMW ₂₅
266	+	009	CRA → CMMA
267	+	009	CMR → CMMA
268	-	009	Clear CMMA
269			
270	+	014	CMAF → CMW
271	+	014	CRB → CMW
272	+	014	CCR → Typewriter
273			
274	+	014	Typewriter → CCR
275	+	014	Real Time Clock → CCR
276			
277			
278			
279			
280			
281			
282			
283			
284			
285			
286			
287			

<u>FTS.</u>	<u>Polarity</u>	<u>Print</u>	<u>Description</u>
288			
289			
290			
291	+	013	Binary Zeros = Decimal Zeros.
292			
293			
294			
295	+	010	CACO → CCFSB → CR
296	+	011	CCFSB → CR12-42
297	+	012	CRAK → CMAK.
298	+	014	CMAK → CMS.
299	-	014	Binary Zeros → CMW 20-24

Polarity indicates the voltage level of the signal when the machine is in the General Clear condition. Minus is -3 volts, + is Ground.

Index Register Assignment

<u>IR</u>	<u>Priority</u>	<u>MAC</u>
01	01	CC
02	02	MAR
03	03	U III A
04	04	U III B
05	05	G.P1
06	06	2
07	07	3
08	08	4
09	09	5
10	10	6
11	11	7
12	12	8
13	13	U II
14	14	U III C
15	15	U III D

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Logical Design

Connector Format - UNIVAC III

Univac III has 11 thirty-four (34) pin connectors for logical signals only. These are allotted as follows:

3 for the Memory

8 for the General Purpose Channels.

The format for these connectors is attached. For logical prints refer to DX 144-153.

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Rev. B - 11/21/60

Thirty For Pin Connector

<u>Pin</u>	<u>Title</u>	<u>Description</u>	<u>Polarity</u>
01	CCSG _n 1	Read Character 1	+
02	CCSG _n 2	Read Character 2	+
03	CCSG _n 3	Read Character 3	+
04	CCSG _n 4	Read Character 4	+
05	CSG _n	Memory Granted	+
06	SPAR _e		
07	CFEG _n	Lockout	+
08	CMEG _n	Memory Error	+
09	-CTPG _n	Cycling Unit Start (T3)	-
10	SPAR _e		
11	SPAR _e		
12	SPAR _e		
13	SPAR _e		
14	CMWG _n 1	Write A/N Character 1	+
15	CMWG _n 2	Write A/N Character 2	+
16	CMWG _n 3	Write A/N Character 3	+
17	CMWG _n 4	Write A/N Character 4	+
18	-CMRG _n	Memory Request	-
19	-CMVG _n	Instruction	+
20	-CMMWG _n	Memory Write	+
21	SPAR _e		
22	CFOIGR _n	Set Instruction Interlock FF	-
23	-CFO2G _n	Set Program Interrupt FF	-
24	-CFO3G _n	Set ReRead Error FF	-
25	-CFO4G _n	Set Out of Paper FF	-
26	-CFO5G _n	Set Reissue/Fault FF	-
27	-CR8G _n	80 Column Card Equipment	+
28	-CLTG _n	Printer, Paper Tape or Translate Instruction	+
29	-CR9G _n	90 Column Card Equipment	+
30	-CCR20G _n	20th Call	+
31	-CCROG _n	Rows 9-4	+
32	SPARE		
33	SPARE		
34	SPARE		

Polarity indicates the:

Voltage on output of cable driver when signal is desired.

<u>Pin #</u>	<u>Connector #1</u>	<u>#2</u>	<u>#3</u>
01	CMR01	-CMW01C	-CMS00
02	02	-CMW02C	01
03	03	-CMW03C	02
04	04	-CMW04C	03
05	05	-CMW05C	04
06	06	-CMW06C	05
07	07	-CMW07C	06
08	08	-CMW08C	07
09	09	-CMW09C	08
10	10	-CMW10C	09
11	11	-CMW11C	10
12	12	-CMW12C	11
13	13	-CMW13C	12
14	14	-CMW14C	13
15	15	-CMW15C	CMSW1
16	16	-CMW16C	R1
17	17	-CMW17C	W2
18	18	-CMW18C	R2
19	19	-CMW19C	Spare
20	20	-CMW20C	Spare
21	21	-CMW21C	Spare
22	22	-CMW22C	Spare
23	23	-CMW23C	Spare
24	24	-CMW24C	Spare
25	25	-CMW25C	Spare
26	26	-CMW26C	Spare
27	27	-CMW27C	Spare
28	28	Spare	Spare
29	CMAE1	Spare	Spare
30	2	Spare	Spare
31	CMAE1	Spare	Spare
32	2	Spare	Spare
33	SPAR _e	Spare	Spare
34	SPAR _e	Spare	Spare