WAVE MATE Z80

SUPER BULLET MANUAL

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I INTRODUCTION

The Wave Mate SUPER BULLET is a fast, compact and very powerful single board computer (SBC). The SUPER BULLET provides an 8 megahertz Z80H CPU, 256K bytes of random access memory (RAM), up to 16K bytes of erasable programmable memory (EPROM), 4 RS-232-C serial ports, a Centronics printer interface, a diskette interface (supporting four 8", four 5", and two 3" drives) and SCSI bus interface for Winchester disk controllers. This 8 megahertz Z80H, along with powerful direct memory access controllers (DMA) for data transfer and a greatly enhanced C-BIOS, executes CP/M PLUS at a previously unheard of speed. Video display communication is provided through one of the RS-232-C ports, to which many different serial terminals may be attached. Future I/O expansion is provided through a special bus link. Because the BULLET contains four serial ports and 256K bytes of memory, an efficient and economical multi-user system may be realized.

II DESIGN PHILOSOPHY

The Wave Mate SUPER BULLET has been designed to be the heart of an extremely low cost, high performance microcomputer system. It is ideally suited for high performance single user CP/M and multi-user MP/M small business applications. It is also capable of providing intelligent terminal, distributed processing, and high speed local networking capabilities. Special BULLET hardware features and a greatly enhanced C-BIOS have been implemented in order to overcome limitations of the CP/M operating system encountered in most existing hardware configurations.

Since most small microcomputer systems are I/O bound (rather than compute bound), the BULLET design has addressed this fact by incorporating into its architecture a flexible DMA facility, fully interrupt driven I/O, and a high speed floppy disk controller. The 8MHZ Z-80H CPU was chosen with a full complement of Zilog compatible peripheral chips. This insures a cost effective, simple design; yet unlike most other implementations, the design results in full use of the microprocessor's capabilities.

The SUPER BULLET has been designed with the OEM/systems integrator in mind. Its compact size, low power requirement, and single supply voltage make it easy to incorporate into both existing and new equipment.

III HARDWARE DESCRIPTION

A. Physical Considerations

The SUPER BULLET is packaged on a single printed circuit board measuring 7.875 inches (20 cm) by 10.7 inches (27.2 cm). Mounting holes .156 inches (4 mm) in diameter are provided .250 inches (6.4 mm) from the corners. The maximum height of the board, considering pin lead protrusion through the board on the underside as well as component height, is .625 inches (15.8 mm). Additional height must be provided for the header connectors for the I/O and power. However, all connectors have been placed on the component side of the board. Component and connector identifiers have been silk screened on the board.

B. Electrical Requirements

The SUPER BULLET requires only one regulated 5 volt power supply, which under normal room temperatures need supply only 2 amps. Actual current consumption depends upon use of the optional EPROM and whether the SCSI bus is being used. The plus and minus voltages, required for the RS-232 operation, are generated on the board itself.

For power an AMP connector, part # 350211-1, has been mounted on the board. The mating connector, supplied by the user, must be an AMP part # 1-480424-0 with AMP contacts #60617-4 or equivalent. OEMs that require a low profile power connector should contact Wave Mate regarding an optional connector. If a switching power supply is used, the board and ALL disk drives MUST be shielded from noise.

C. CPU, DMA, and Interrupt System

1. Central Processing Unit (CPU):

The Zilog Z80H CPU device is clocked up to the maximum eight megahertz rate with no memory wait states. Peripheral I/O devices are clocked at a four megahertz rate. Timing differences between slow peripherals and EPROM are resolved by a proprietary circuit.

2. Direct Memory Access (DMA) Facility:

There are two Zilog DMA controllers on the SUPER BULLET, DMA0 and DMA1. These devices provide for data transfer from/to any memory location or I/O device at rates of up to one megabyte per second. External logic is provided which allows transfers from/to any RAM memory bank at the same data rate. It should be noted that only the RAM memory is accessible to the DMA devices, EPROM and ROM memory are not in the DMA map.

External device multiplexing allows several I/O devices to use a

DMA channel and controls transfers between the memory banks.
Device selection and memory control is selected through an
external write only register. I/O port addresses for the DMA
controllers and the external control registers are as follows:

```
1A HEX        DMA channel 0 status/control
14 HEX        DMA channel 0 external control
18 HEX        DMA channel 1 status/control
15 HEX        DMA channel 1 external control
```

DMA I/O device selection and memory control are programmed into
the external control register and are defined in the following
table:

```
BITS 2,1,0        DEVICE

    000           FDC floppy disk controller.
    001           LOGIC 0.
    010           DART serial channel B.
    011           SCSI bi-directional bus.
    100           External device 1.
    101           External device 2.
    110           SIO serial channel A.
    111           SIO serial channel B.
```

RAM memory control of DMA operations is selected according to the
following fields:

```
BITS 5,4          Select source bank.
BITS 7,6          Select destination bank.
```

RAM memory bank selection bit fields are defined as follows:

```
00     BANK 0
01     BANK 1
10     BANK 2
11     BANK 3
```

The remaining bit, bit 3, in this register is unused. Note that
when a transfer is between an I/O port and memory, the memory
control bit fields for both the source and destination must be
programmed the same and must contain the desired memory bank
number for the I/O. A device selection at a known logic state is
provided to facilitate memory to memory moves where it is desired
to move only one byte by using the DMA byte mode and the force
ready command. To use this facility, the DMA must be programmed
for a logic 1 to be ready, and the logic 0 "device" selected.
Then when the force ready command is issued only one byte will
transfer if byte mode has been programmed. If the DMA senses
external ready when it is enabled, the full byte count plus one
will be immediately transferred when the DMA is enabled.

When both DMA devices request the bus at the same time, the bus
request priority is hardwired to give DMA0 the highest priority.

The bus request priority out line of DMA1 is present on the external bus connector as *BAO and additional DMA devices may be added. If additional DMA devices are added, they will be of lower priority and will not have access to the special hardware on the board which allows efficient memory to memory data moves and I/O.

3. Priority Interrupt Structure:

All peripheral devices are connected to the standard Zilog interrupt priority daisy chain. The priority interrupt daisy chain is provided with look ahead logic which terminates on the external bus connector. Thus any devices added to the external bus may use the priority interrupt daisy chain. The priorities are shown in the table below from the highest priority to the lowest:

1. DMA0
2. DMA1
3. SIO
4. DART with FDC on the A level.
5. PIO with Centronics and SCSI.
6. Clock Timer Circuit 0
7. External Devices

When using the interrupt daisy chain the Z80 must be programmed in interrupt mode 2 (IM2). In order to accomodate the slower peripherals, the external timing logic must synchronize to the peripheral clock during the execution of the Z80 RETI instruction. This is required to allow the interrupt daisy chain to stabilize so that the RETI instruction is decoded by the peripheral under service. This synchronization MUST be accomplished by the following three Z80 instructions:

```
OUT   (1FH),A    ; Enable synchronization.
EI               ; Reenable interrupts.
RETI             ; Execute return from interrupt.
```

Failure to execute this code sequence for peripherals which require the RETI instruction will result in a system failure. Once synchronization is started, it is only active for the following two instructions. Interrupts MUST be disabled at the start of this sequence to ensure that it executes uninterrupted.

4. I/O Port Assignments:

The following chart summarizes the I/O port assignments.

PORT	DEVICE
0	DART Channel A Data
1	DART Channel A Status/Control
2	DART Channel B Data
3	DART Channel B Status/Control
4	PIO Port A Data
5	PIO Port B Data
6	PIO Port A Control
7	PIO Port B Control
8	CTC0 Channel 0
9	CTC0 Channel 1
A	CTC0 Channel 2
B	CTC0 Channel 3
C	SIO Channel A Data
D	SIO Channel A Status/Control
E	SIO Channel B Data
F	SIO Channel B Status/Control
10	FDC Command/Status Port
11	FDC Track Register
12	FDC Sector Register
13	FDC Data Register
14	External DMA0 Control Register (Write only)
15	External DMA1 Control Register (Write only)
16	External FDC Register (Hardware Control)
17	Memory Map Select Register (Write only)
18	DMA1 Status/Control
19	SCSI Bi-directional Data Bus.
1A	DMA0 Status/Control
1B	FDC9229 Control (Write only)
1B	Hardware Status Register (Read only)
1C	CTC1 Channel 0
1D	CTC1 Channel 1
1E	CTC1 Channel 2
1F	Return From Interrupt Control (Write only)

D. Memory System

1. Random Access Memory (RAM):

There is 256K bytes of random access memory on the SUPER BULLET.
The memory is physically organized as four 64K banks. External
support logic allows the DMA devices to directly access any
location within this 256K memory system. Although the DMA device
can move data from/to any address within the 256K bytes of RAM on
the SUPER BULLET, the Z80 can only address 64K bytes at any one
time. To provide greater versatility, memory mapping of the CPU
address space is provided through an I/O port. There is a common
memory area which is always in the CPU's context. The common
memory may be mapped into either RAM or the EPROM. The CPU's
common memory may be selected to be either the address space from
0000 HEX to 3FFF HEX, or from C000 HEX to FFFF HEX. This is
equivalent to 16K bytes of address space. The remaining 48K of
CPU address space may be mapped from any one of five logical
banks of 48K which comprise the remainder of the 256K of RAM on
the system. Note that the state of the CPU memory map does not
affect the DMA operations; that is, the memory banks are constant
for the DMA device as it can access the full 256K of RAM memory.
For example, assume two CPU memory maps each contain a program,
and the currently executing program requested the operating
system to read a disk sector. The operating system could
initiate a DMA read sector operation to transfer the data from
the disk to that user space. The operating system could then
switch CPU address banks and start the second program executing
while the DMA operation was being performed without affecting the
transfer of data to the first program.

Selection of the CPU memory map is accomplished by outputting a
map code to the Segment Register at I/O port 17 HEX. The
function of the map code bits is shown in the following table:

SEGMENT REGISTER CONTROL FUNCTIONS:

Bits   Function

4   Select address of common memory area:
        0 = C000-FFFF
        1 = 0000-3FFF
3   Select EPROM to be common:
        0 = RAM is common
        1 = EPROM is common
2,1,0   Select active bank (non-common memory):
        000 = Bank 0 is selected
        001 = Bank 1 is selected
        010 = Bank 2 is selected
        011 = Bank 3 is selected
        100 = Bank 4 is selected

The address mapping function of the Memory Map Register contents is shown in the following table:

	Logical CPU Address			
	0000-3FFF	4000-7FFF	8000-BFFF	C000-FFFF
Segment Register	bank/seg	bank/seg	bank/seg	bank/seg
00000	B0,S0	B0,S1	B0,S2	B0,S3
00001	B1,S0	B1,S1	B1,S2	B0,S3
00010	B2,S0	B2,S1	B2,S2	B0,S3
00011	B3,S0	B3,S1	B3,S2	B0,S3
00100	B1,S3	B2,S3	B3,S3	B0,S3
01000	B0,S0	B0,S1	B0,S2	EPROM
01001	B1,S0	B1,S1	B1,S2	EPROM
01010	B2,S0	B2,S1	B2,S2	EPROM
01011	B3,S0	B3,S1	B3,S2	EPROM
01100	B1,S3	B2,S3	B3,S3	EPROM
10000	B0,S0	B0,S1	B0,S2	B0,S3
10001	B0,S0	B1,S1	B1,S2	B1,S3
10010	B0,S0	B2,S1	B2,S2	B2,S3
10011	B0,S0	B3,S1	B3,S2	B3,S3
10100	B0,S0	B1,S0	B2,S0	B3,S0
11000	EPROM	B0,S1	B0,S2	B0,S3
11001	EPROM	B1,S1	B1,S2	B1,S3
11010	EPROM	B2,S1	B2,S2	B2,S3
11011	EPROM	B3,S1	B3,S2	B3,S3
11100	EPROM	B1,S0	B2,S0	B3,S0

Do not use any undesignated segment register values.

Key to physical "bank/seg" mapping:

B0	Physical Bank 0	S0	Segment 0, 0000-3FFF
B1	Physical Bank 1	S1	Segment 1, 4000-7FFF
B2	Physical Bank 2	S2	Segment 2, 8000-BFFF
B3	Physical Bank 3	S3	Segment 3, C000-FFFF

2. Read Only Memory (ROM):

Initial program loading (the boot process) may be done from a flexible diskette by a 32 byte program in ROM. This function is selected by switch four on SW1. Upon power up or reset, if this switch is OFF, the ROM is mapped into a starting address of zero which is the Z80 starting address after power up reset. In addition, reset enables switch selection of the floppy disk boot parameters. The boot device and mode are determined by the settings of the 8 position DIP switch on the SUPER BULLET. The physical disk unit number is always unit zero regardless of whether it is a 3, 5 or 8 inch drive. The ROM location is read only, a write to its address space will be placed into RAM. The function of the ROM is to read the first sector from track zero into RAM memory starting at address zero. When this is achieved with no disk I/O error, the ROM starts executing the code at location 32 HEX. At any time after a reset, an input or output to the port address 1A HEX (the DMA0 port) will disable the ROM and it will no longer be accessible until another reset occurs.

3. Erasable Programmable Read Only Memory (EPROM):

A location for an optional EPROM is located at U131. This socket is configured as an Intel Universal Memory Site. It accepts either a 24 pin 2732A, or 28 pin 2764, or 28 pin 27128 EPROM. Selection of the type is controlled by jumper option. Refer to the section on switches and jumpers for configuration data. If an EPROM is installed, it may be selected as the reset program by setting SW1 switch four ON. If this option is selected, the program starting at location zero in the EPROM will execute upon reset. At any time after a reset, an input or output to the port address 1A HEX (the DMA0 port) will disable the reset mapping of the EPROM. The EPROM may also be mapped into the CPU memory at any time by appropriate selection of the value placed in the Memory Segment Register. See the memory mapping information under RAM above. The address decoding provides for a 16K EPROM. If an 8K or 4K EPROM is installed the EPROM will appear in multiple images in the CPU memory map. When the CPU is accessing the EPROM the CPU clock is slowed to 4 megahertz. The recommended access time for the EPROM is 250 nano seconds. The SUPER BULLET is shipped without EPROM unless special OEM arrangements have been made.

E. I/O System:

The I/O system is fully decoded on the SUPER BULLET thus all unassigned port addresses from 20 HEX to FF HEX may be used by external hardware. The I/O space from 20 HEX to 2F HEX is set aside for OEM manufactured devices and the space from 30 HEX to 3F HEX is reserved for Wave Mate developed peripherals. The space from 40 HEX to FF HEX is undesignated.

1. Hardware Status Register:

A read only hardware status register at port 1B HEX is provided
to check the state of the following functions:

    BIT   STATUS FUNCTION.

    0   Centronics Busy Bit.
    1   DIP switch 2.
    2   DIP switch 3.
    3   *Floppy disk two sided.
    4   Floppy disk head load status.
    5   *Floppy disk exchange (8 inch only).
    6   FDC interrupt request line.
    7   FDC data request line.

2. Floppy Disk Controller/Formatter (FDC):

This device is a Synertek SY1793-002. It is upward compatible
with the Western Digital FD1793 controller. The following I/O
port addresses are assigned to this device:

    10 HEX   Command/Status register.
    11 HEX   Track register.
    12 HEX   Sector register.
    13 HEX   Data register.

Since this is not a Zilog device and not capable of generating or
responding to the Zilog priority daisy chain interrupt, it is
connected to the DART *RIA (Ring Indicator A) input to provide an
interrupt vector. External logic provides for control of four
8-inch floppy disk drives, four 5-inch floppy disk drives, and
two 3-1/2-inch floppy disk drives. The external logic also
provides for software control of the spindle motors (5 inch and 3
inch drives only), side select, and enabling of write
precompensation. These functions are controlled by write only
registers.

The following table gives the external control port addresses and
bit definitions:

FDC DISK CONTROL REGISTER, PORT 16 HEX:

    BIT 0-3   Bits 0, 1, 2, 3 form a unit select number,
                as follows:
                0, 1, 2, & 3 are the 5 inch drives, 4, 5, 6 & 7
                are the 8 inch drives, and 8 & 9 are the 3 inch.
    BIT 4   Select side 2.
    BIT 5   Disable 3 & 5 inch spindle motors.
    BIT 6   Select 1 or 2 MHZ controller operation.
    BIT 7   Select single or double density operation.

FDC CONTROL PORT 1B HEX:

```
BIT 0        Set FDC9229 P0 mode.
BIT 1        Set FDC9229 P1 mode.
BIT 2        Set FDC9229 P2 mode.
BIT 3        Set SY1793 test pin (fast seek).
BIT 4        Select software control of port 16HEX.
BIT 5        Unused.
BIT 6        Unused.
BIT 7        Set door lock.
```

The FDC device is capable of formatting and reading a wide variety of soft sectored diskettes. With 8 inch drives, it is compatible with the IBM 3740 format and FM recording and the IBM System-34 format and MFM recording. With 5 inch drives, it is compatible with both single density and double density soft sector formats. Data separation for all modes is provided by a digital data separator circuit.

3. Dual Asynchronous Receiver/Transmitter (DART):

This device provides two independent asynchronous serial data channels. Each channel has an independent baud rate which is derived from two channels of the counter timer circuit 0 (described later). The baud rates are determined by the CTC0 and DART programming and can range from 110 baud to 76.8 kilobaud. In addition, the transmit/receive word parameters are fully programmable within the DART. Channel A and B of the DART provide a full implementation of the RS-232-C interface type E, with the exception that there is no circuit CE (ring indicator). Channel A of the DART is normally used for the system console. The channel A ring indicator input is used by the floppy disk controller to request an interrupt vector on the Zilog daisy chain interrupt system. The DART is the fourth device on the interrupt priority daisy chain, following the SIO device.

The DART registers are at the following port addresses:

```
0 HEX        Channel A data.
1 HEX        Channel A status/control.
2 HEX        Channel B data.
3 HEX        Channel B status/control.
```

4. Serial Input/Output (SIO)

This device provides two independent synchronous or asynchronous serial data channels. Each channel has an independent baud rate which is derived from the counter timer circuit 1 (described later). In addition, the transmit and receive baud rates for channel A may be set independently. This allows the user to transmit and receive at different bauds. These baud rates are determined by the CTC1 and SIO programming. For asynchronous operation these bauds can range from 110 baud to 76.8 kilobaud. For synchronous operation, bauds as high as 880K may be programmed. In addition, the transmit/receive word parameters are fully programmable within the SIO. Channel A and B of the

SIO provide a full implementation of the RS-232-C interface type E with the exception that there is no circuit CE (ring indicator). The SIO is the third device on the interrupt priority daisy chain, following the DMA1 device.

The SIO registers are at the following port addresses:

    C HEX   Channel A data.
    D HEX   Channel A status/control.
    E HEX   Channel B data.
    F HEX   Channel B status/control.

5. Counter Timer Circuit (CTC):

Counter Timer Circuit 0 (CTC0):

This device provides four independently programmable counter/timer channels. Channel 0 is used to provide the baud clock for the DART channel A. Channel 1 is used to provide the baud clock for the DART channel B. Channels 2 and 3 are used together to provide a real time clock capability and clock interrupts. This is achieved by using channel 2 as a timer and channel 3 as a counter. Channels 0, 1, and 2 have their inputs connected to a crystal controlled clock which provides a 1.2288 MHZ frequency. The CTC0 device is the sixth device on the interrupt priority daisy chain.

The CTC0 registers are at the following I/O port addresses:

    Channel 0   8 HEX
    Channel 1   9 HEX
    Channel 2   A HEX
    Channel 3   B HEX

Counter Timer Circuit 1 (CTC1):

This device provides additional programmable counter/timer channels. Channel 0 is used to provide the transmit baud clock for the SIO channel A. Channel 1 is used to provide the receive baud clock for the SIO channel A. Channel 2 is used to provide the baud clock for the SIO channel B. Channels 0, 1, and 2 have their inputs connected to a crystal controlled clock which provides a 1.2288 MHZ frequency. The CTC1 device is not on the priority interrupt daisy chain.

The CTC1 registers are at the following I/O port addresses:

    Channel 0   1C HEX
    Channel 1   1D HEX
    Channel 2   1E HEX

Note that channel 3 may not be used. Its port (1F HEX) is used to enable interrupts on the priority daisy chain.

6. Parallel Input/Output Controller (PIO):

This device provides two 8 bit parallel I/O ports. It is used to
implement the Centronics interface and the SCSI bus control
interface. Port B provides the Centronics data and handshake
signals. Port A is used in bit mode to provide status of the
SCSI bus interface. The control signal assignments presented
here are further described under the applicable I/O device.

        PIO Port A, SCSI bus control (bit mode):

        BIT 0: ATN   output
        BIT 1: RST   output
        BIT 2: SEL   output
        BIT 3: BUSY   input
        BIT 4: MSG   input
        BIT 5: C/D   input
        BIT 6: REQ   input
        BIT 7: I/O   input

Note that program control allows these devices to operate in
either interrupt driven or polled mode. The PIO device is the
fifth device on the interrupt priority daisy chain.

The PIO registers are at the following I/O port addresses:

        4 HEX   Port A data.
        5 HEX   Port B data.
        6 HEX   Port A control.
        7 HEX   Port B control.

7. Centronics Printer Port:

The Centronics printer interface has been implemented with the
use of a Zilog PIO device. The PIO port B is programmed in
output mode and provides data output and handshaking to the
interface. The Centronics status is sensed in the hardware
status register. When bit zero is 1 the interface is busy, when
it is zero the interface is not busy. If the interface is not
busy, data may be written to the PIO data port B. An interrupt
may be programmed when the interface accepts the data and
additional data written to port B during the interrupt service
routine.

8. SCSI Bus Interface:

A SCSI bus interface is provided which is capable of controlling
a variety of SCSI compatible devices. It is most commonly used
to communicate with a Winchester disk controller.

The SCSI bus interface is implemented by a bi-directional data
port at 19 HEX. Status and control of the SCSI is implemented
with the PIO Port A programmed in bit mode, and through hardware
handshaking. A read from port 19 HEX accesses the data on the

SCSI data bus. A write to port 19 HEX latches the data which will be read by the external device when it reads the SCSI data bus. Note that a read or write to this port causes the hardware to assert *ACK if enabled by *REQ.

Users wishing to program the SCSI should be familiar with the operation of the SCSI as described in ANSI X3T9.2/82-2.

IV I/O CONNECTORS

1. J1 - 50 pin General Purpose External Bus Connector

A 50 pin male header is used to permit the Z-80A CPU bus and the
DMA bus to be used externally from the SUPER BULLET. The pin-out
of this header is shown below.

PIN	Signal	I/O	Description
1	D0	IO	Data Bit 0
2	D1	IO	Data Bit 1
3	D2	IO	Data Bit 2
4	D3	IO	Data Bit 3
5	D4	IO	Data Bit 4
6	D5	IO	Data Bit 5
7	D6	IO	Data Bit 6
8	D7	IO	Data Bit 7
9	CLOCK	O	4 MHZ Peripheral Clock
10	GND	O	Ground
11	A0	IO	Address Bit 0
12	A1	IO	Address Bit 1
13	A2	IO	Address Bit 2
14	A3	IO	Address Bit 3
15	A4	IO	Address Bit 4
16	A5	IO	Address Bit 5
17	A6	IO	Address Bit 6
18	A7	IO	Address Bit 7
19	A8	IO	Address Bit 8
20	A9	IO	Address Bit 9
21	A10	IO	Address Bit 10
22	A11	IO	Address Bit 11
23	A12	IO	Address Bit 12
24	A13	IO	Address Bit 13
25	A14	IO	Address Bit 14
26	A15	IO	Address Bit 15
27	GND	O	Ground
28	*BAO	O	Bus Acknowledge Out (DMA)
29	*EXRDY1	I	External Device 1 Ready
30	*EXRDY2	I	External Device 2 Ready
31	N/C		Spare
32	*RESET	O	Reset Out
33	*INT	I	Interrupt (CPU)
34	N/C		Spare
35	*BSREQ	I	Bus Request (DMA)
36	*BSACK	O	Bus Acknowledge (CPU)
37	*IORQ	O	I/O Request (CPU)
38	*MREQ	O	Memory Request (CPU)
39	*RD	O	Read (CPU)
40	*WR	O	Write (CPU)
41	*M1	O	Machine Cycle One
42	*RFSH	O	Memory Refresh (CPU)
43	*NMI	I	Non Maskable Interrupt (CPU)
44	*WAIT	I	Wait (CPU)

```
45   *HALT      O    Halt (CPU)
46   *DMEM      I    Disable on board memory
47   *IEOUT     O    External Interrupt Priority
48    N/C            Spare
49    N/C            Spare
50    VCC       O    + 5 VOLTS
```

The female mating connector to J1 is 3M part number 3425-6000 or
equivalent. The output lines are capable of driving a maximum of
4 CMOS loads or 1 TTL load. The maximum cable length to be
attached to J1 cannot exceed 12 inches.

2. J2 - 50 pin SCSI Interface connector

A 50 pin male header is used to connect to a SCSI bus compatible
peripheral. The pin-out of the header is shown below.

```
PIN Signal     I/O   Description
 2  *SD0       IO    Data Bit 0
 4  *SD1       IO    Data Bit 1
 6  *SD2       IO    Data Bit 2
 8  *SD3       IO    Data Bit 3
10  *SD4       IO    Data Bit 4
12  *SD5       IO    Data Bit 5
14  *SD6       IO    Data Bit 6
16  *SD7       IO    Data Bit 7
32  *ATN       O     Attention
34  *SPARE           Spare
36  *BUSY      I     Bus busy
38  *ACK       O     Acknowledge
40  *RST       O     Reset
42  *MSG       I     Message
44  *SEL       O     Select
46  *C/D       I     Command/Data
48  *REQ       I     Request
50  *I/O       I     Input/Output
```

Odd numbered pins 1 through 49 are all connected to ground.

The female mating connector to J2 is 3M part number 3425-6000 or
equivalent. The maximum cable length to be attached to J2 should
not exceed 6 meters.

3. J3 - 10 pin serial port connector

A ten pin male header is used to attach a RS-232-C serial
terminal to the SUPER BULLET using the DART channel A. A ten pin
male header is used to attach a second RS-232-C serial terminal
to the SUPER BULLET.

```
PIN  Signal  I/O  Description
  1  *TXDB    O    Transmit Data
```

```
    2   *RXDB    I   Receive Data
    3   *DTRB    O   Data Terminal Ready
    4   *RTSB    O   Request To Send
    5   *CTSB    I   Clear To Send
    6   *DCDB    I   Data Carrier Detect
    7   RLSDB    O   Receive Line Signal Detect
    8   GND      O   Ground
    9   *CRESET  I   Computer Reset
   10   GND      O   Ground
```

The female mating connector to J4 is 3M part number 3473-6000 or equivalent. The above signals correspond to the Zilog DART definitions. See system set-up for recommended RS-232-C usage.

4. J4 - 10 pin serial port connector

A ten pin male header is used to attach a RS-232-C serial terminal to the SUPER BULLET using the DART channel A. When using the WAVE MATE provided C-BIOS and CP/M, this port is used as the system console. The pin-out of the header is shown below.

```
PIN  Signal  I/O  Description
  1  *TXDA    O   Transmit Data
  2  *RXDA    I   Receive Data
  3  *DTRA    O   Data Terminal Ready
  4  *RTSA    O   Request to Send
  5  *CTSA    I   Clear To Send
  6  *DCDA    I   Data Carrier Detect
  7  RLSDA    O   Receive Line Signal Detect
  8  GND      O   Ground
  9  *CRESET  I   Computer Reset
 10  GND      O   Ground
```

The female mating connector to J3 is 3M part number 3473-6000 or equivalent. The above signals correspond to the Zilog DART definitions. See system set-up for recommended RS-232-C usage.

5. J5 - 34 pin Centronics Printer port connector

A 34 pin male header is used to attach a Centronics type printer to the SUPER BULLET. The pin-out of this header is shown below.

```
PIN   Signal  I/O  Description
  1  *CSTRB    O   Strobe
  3   CDTA1    O   Data Bit 1
  5   CDTA2    O   Data Bit 2
  7   CDTA3    O   Data Bit 3
  9   CDTA4    O   Data Bit 4
 11   CDTA5    O   Data Bit 5
 13   CDTA6    O   Data Bit 6
 15   CDTA7    O   Data Bit 7
 17   CDTA8    O   Data Bit 8
```

```
19   *CACK    I   Acknowledge
21   CBUSY    I   Busy
```

Even pins 2 through 24 and 27, 30, and 31 are all connected to
ground.

The female mating connector to J5 is 3M part number 3414-6000 or
equivalent. The maximum cable length to be attached to J5 should
not exceed 8 feet.

6. J6 - 50 pin 8" floppy disk drive connector

A 50 pin male header is used to attach from one to four 8"
Shugart 800 compatible disk drives to the SUPER BULLET. The
pin-out of this header is shown below.

```
PIN   Signal   I/O   Description
  2   *XTG43    O    Track greater than 43
 10   *FD2S     I    Disk is two sided
 12   *XDCG     I    Disk has been changed (door opened & closed)
 14   *XSIDE    O    Side Select
 16   *DLOCK    O    Door Lock
 18   *XHLD     O    Head Load
 20   *INDEX    I    Index Pulse
 22   *READY    I    Ready
 26   *SEL1     O    Select Drive #1
 28   *SEL2     O    Select Drive #2
 30   *SEL3     O    Select Drive #3
 32   *SEL4     O    Select Drive #4
 34   *XDIR     O    Direction
 36   *XSTEP    O    Step
 38   *XWDAT    O    Write Data
 40   *XWGAT    O    Write Gate
 42   *TR00     I    Track Zero Sensor
 44   *WPROT    I    Write Protect Sensor
 46   *RDATA    I    Read Data
```

All odd numbered pins are connected to ground.

The female mating connector to J6 is 3M part number 3425-6000 or
equivalent. The maximum cable length to be attached to J6 should
not exceed 8 feet.

7. J7 - 34 pin 5-1/4 inch mini floppy disk drive connector

A 34 pin male header is used to attach from one to four 5 1/4
inch Shugart 400 compatible disk drives to the SUPER BULLET. The
pin-out of this header is shown below.

```
PIN   Signal   I/O   Description
  2   *DLOC     O    Door Lock
  4   *MHLD     O    Head Load (jumper option)
```

```
 6    *MSEL4    O    Select Drive #4
 8    *INDEX    I    Index Pulse
10    *MSEL1    O    Select Drive #1
12    *MSEL2    O    Select Drive #2
14    *MSEL3    O    Select Drive #3
16    *MMTR     O    Motor On
18    *MDIR     O    Direction
20    *MSTEP    O    Step
22    *MWDAT    O    Write Data
24    *MWGAT    O    Write Gate
26    *TR00     I    Track Zero Sensor
28    *WPROT    I    Write Protect Sensor
30    *RDATA    I    Read Data
32    *MSIDE    O    Side Select
34    *RDY      I    Ready (jumper option)
```

All odd numbered pins are connected to ground.

The female mating connector to J7 is 3M part number 3414-6000 or equivalent. The maximum length of cable to be attached to J7 should not exceed 8 feet.

8. J8 - 10 pin serial port connector

A ten pin male header is used to attach a RS-232-C serial device to the SUPER BULLET using the SIO channel A.

```
PIN   Signal   I/O   Description
  1   *TXDA     O    Transmit Data
  2   *RXDA     I    Receive Data
  3   *DTRA     O    Data Terminal Ready
  4   *RTSA     O    Request To Send
  5   *CTSA     I    Clear To Send
  6   *DCDA     I    Data Carrier Detect
  7   RLSDA     O    Receive Line Signal Detect
  8   GND       O    Ground
  9   N/C
 10   N/C
```

The female mating connector to J8 is 3M part number 3473-6000 or equivalent. The above signals correspond to the Zilog DART definitions. See system set-up for recommended RS-232-C usage.

9. J9 - 10 pin serial port connector

A ten pin male header is used to attach a RS-232-C serial device to the SUPER BULLET using the SIO channel B.

```
PIN   Signal   I/O   Description
  1   *TXDB     O    Transmit Data
  2   *RXDB     I    Receive Data
  3   *DTRB     O    Data Terminal Ready
```

```
 4  *RTSB    O   Request To Send
 5  *CTSB    I   Clear To Send
 6  *DCDB    I   Data Carrier Detect
 7  RLSDB    O   Receive Line Signal Detect
 8  GND      O   Ground
 9  N/C
10  N/C
```

The female mating connector to J9 is 3M part number 3473-6000 or equivalent. The above signals correspond to the Zilog DART definitions. See system set-up for recommended RS-232-C usage.

10. J10 - 26 pin 3-1/2 inch micro floppy disk drive connector

A 26 pin male header is used to attach one or two 3 1/2 inch Sony compatible disk drives to the SUPER BULLET. The pin-out of this header is shown below.

```
PIN Signal     I/O  Description
  1 *ZMTR       O   Motor On
  2 *ZSEL1      O   Select Drive #1
  3  N/C
  4 *ZSEL2      O   Select Drive #2
  6 *ZDIR       O   Direction
  8 *ZSTEP      O   Step
 10 *ZWDAT      O   Write Data
 12 *ZWGAT      O   Write Gate
 14 *ZHLD       O   Head Load
 16 *ZSIDE      O   Side Select
 18 *INDEX      I   Index Pulse
 20 *TR00       I   Track Zero Sensor
 22 *WPROT      I   Write Protect Sensor
 24 *RDATA      I   Read Data
 26 *RDY        I   Ready
```

Odd numbered pins 5 through 25 are connected to ground.

The female mating connector to J10 is 3M part number 3399-6000 or equivalent. The maximum length of cable to be attached to J10 should not exceed 8 feet.

11. J11 - 4 pin power connector.

```
PIN   Description
  1   Not Connected
  2   Not Connected
  3   Ground (+5V Return)
  4   +5V Plus or Minus 0.25V at 2.0A
```

The female mating connector is AMP part number 1-480424-0 with AMP contacts #60617-4 or equivalent.

V   System Setup

Prior to a cold start boot strap operation, a system serial video
console and floppy disk drive must be connected to the SUPER
BULLET.

        1. System console. For Wave Mate software a serial
terminal console must be connected to J4. Reference should be
made to section IV of this manual for the appropriate connector
pin-outs.

        2. System floppy disk drive. The system can be booted from
either a 5 1/4" mini floppy or an 8" floppy drive, either of them
operating in single or double density recording. The disk drive
choosen for the boot strap operation must be wired as drive 0 and
its characteristics must be reflected by the setting of switches
SW1-5 through SW1-8.

        3. System printer. The system printer may be either a
Centronics parallel or an RS-232 serial model. If a Centronics
printer is selected, then another serial port is free for use in
other ways. i.e. communications port, second printer or terminal.

A.   Switches and Jumpers:

1. Switches

An eight position DIP switch designated as SW1 is located on the
SUPER BULLET.

SW1-1 is used to control power to the SCSI bus termination
resistors. If the SCSI bus interface is not being used this
switch should be off to reduce unnecessary power dissipation. If
the SCSI bus is in use this switch MUST be on.

SW1-2 and SW1-3 are unassigned.

SW1-4 is used to select the BOOT ROM. If this switch is off a
system reset will cause program execution to transfer to the 32
byte ROM on the board. If the switch is on program execution
will transfer to the EPROM device (if provided).

SW1-5 through SW1-8 are used to initialize the floppy disk
controller to be compatible with the type of drive being used in
the boot strapping of the system.

The types of drives and the appropriate switch settings are shown
in the table below:

Floppy type	SW1-5	SW1-6	SW1-7	SW1-8
Double density 3 inch floppy	off	on	on	on
Single density 5 inch floppy	on	on	off	off

Double density 5 inch floppy	on	on	off	on
Single density 8 inch floppy	on	off	on	off
Double density 8 inch floppy	on	off	on	on

2. Jumpers:

Jumper configurations on the SUPER BULLET are set as follows and should seldom need change:

JUMPER   FUNCTION

E1   This jumper is used to select onboard enabling of the ready line when 5 inch disk drives are selected. If the system is connected to 5 inch disk drives which have a drive ready signal on interface pin 34 then this jumper may be left open, otherwise it should be closed. The board is shipped with this jumper closed.

E2   This jumper is used to enable the *WRITE line to U131. If a static RAM is installed instead of EPROM this enables writing to the device when jumpered from 2 to 3. When jumpered from 1 to 2 pin 27 of U131 is tied low. The board is shipped with a jumper from 1 to 2.

E3   This jumper is used to select Address/Power operation to U131 pin 26. U131 is a universal EPROM site and may be used with 2732, 2764, or 27128 EPROM devices. If a 2732 is used pin 26 must be powered. When jumpered from 1 to 2 power is provided. If a 2764 or 27128 is used this must be jumpered from 2 to 3 to provide proper addressing. The board is shipped with a jumper from 1 to 2.

E4   This jumper is used for 5 inch disk drives which require an external head load signal on pin 4 of the interface. When jumpered this signal is active when the 1793 asserts head load. The board is shipped with this jumper open.

B.   Serial Cable Information

The following cable chart is presented to aid in connection of the serial I/O devices to standard RS-232-C terminals. It should be noted that the RS-232-C circuit names define the direction of the signal between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). Computers and modems are defined to be DCE and terminals and printers are DTE. These signal names should not be confused with the signal names assigned by Zilog to the DART. The Zilog names closely follow the usage of the DART/SIO as part of a DTE. In the SUPER BULLET, the RS-232-C

circuits will generally be used as a DCE circuit.

RS-232-C Circuit Name	DB25S Pin	Signal Direction	10 Pin Header	DART Name
BA-Transmitted Data	2	---->	2	RxD
BB-Received Data	3	<----	1	TxD
CA-Request To Send	4	---->	5	CTS
CB-Clear To Send	5	<----	4	RTS
CC-Data Set Ready	6	<----	3	DTR
AB-Signal Ground	7	<--->	8	GND
CF-Received Line Signal Detect	8	<----	7	RLSD
CD-Data Terminal Ready	20	---->	6	DCD

Note: The DB25S pin number above refers to the industry standard D subminature connector with 25 contacts. The 10 pin header refers to J3, J4, J8, and J9 on the SUPER BULLET.

C.   Connecting Floppy Disk Drives

The following disk drive configuration tables are presented to aid in connection of eight inch and five inch floppy disk drives to the SUPER BULLET.   It should be noted that there are few options on the five inch drives and configuration is usually simple.   The eight inch drives sometimes present difficulties due to the number of options and differences in names of the option strapping between drive manufacturers. When optioning eight inch drives the following point should be kept in mind: The stepper motor which positions the heads must be enabled with drive select, not head load.   This is the most common cause of difficulty.   If not set up in this manner, the drive will not move the heads when a restore command without head load is issued.

SHUGART SA400/450/410/460 JUMPER OPTIONS

NAME	OPEN/SHORT
MX	open
DS0	short for unit 0, otherwise open
DS1	short for unit 1, otherwise open
DS2	short for unit 2, otherwise open
DS3	short for unit 3, otherwise open
MS	short
MM	open

SHUGART SA800 JUMPER OPTIONS

NAME	OPEN/SHORT
T3,T4,T5,T6	short
T1	short
T2	short
DS1	short for unit 1, otherwise open
DS2	short for unit 2, otherwise open
DS3	short for unit 3, otherwise open
DS4	short for unit 4, otherwise open
RR	short
RI	short
R,I,S	short
HL	open
DS	short
WP	short
NP	open
D	open
A,B	short
X	open
C	short
Z	short
Y	open
DC	short