Western Digital

WD1005-WAH

USER'S GUIDE
OEM Manual

Design Specification

April 1987

Preliminary

WD1005-WAH
ESDI Winchester
Disk Controller

USER'S GUIDE

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other technical support, please contact
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Description and Document Scope

The WD1005-WAH Winchester Disk Controller is an IBM Personal Computer AT bus compatible module designed to interface one or two disk drives. The WD1005-WAH's drive interface conforms to the ESDI specification. Drives need not be of the same capacity or configuration. All necessary receivers and drivers are included on the board for direct connection to the drives(s).

The ESDI drives used with this controller generally have two modes of operation, soft sector and hard sector. **The WD1005-WAH is designed to operate in the hard sector mode only.** In the hard sector mode, the drive must be configured properly for the mode of operation and the number of desired sectors per track. The WD1005-WAH uses 34 sectors per track.

This document describes installation in the IBM Personal Computer AT. Therefore, all examples in this document use the AT as a "standard." Installation of the WD1005-WAH in AT compatibles may be outside the scope of this document. Refer to your system manuals or contact your dealer for information outside the scope of this document.

Hardware Installation Instructions

This section briefly describes installation of the WD1005-WAH. If the disk drives(s) is (are) being installed internally, it is best to locate the controller in the closest available expansion slot relative to the drive.

CAUTION
Handle the controller board by the ends of the board. Some of the chips are static sensitive and damage may occur if the board is incorrectly handled.

Integrating this controller into a system that does not have floppy support built in requires the use of a stand alone floppy controller such as the WD1002-FOX. It is not acceptable to change the primary/secondary address jumpers on the AT combination card, WD1003-WA2.

Step Instruction

1. Verify controller jumper settings. Only verify the settings. Modification of the standard factory settings on the controller is rarely necessary. Modify the jumpers only under the direction of a qualified individual; i.e., your dealer. Figure 1 illustrates the jumper settings and locations.

2. Verify termination on last drive. Verify proper setting of drive select switches on drive. Do NOT use the drive's radial select option. Refer to the drive owner's manual for information about proper drive termination and select switches.

3. Remove the blank expansion slot bracket. Put the bracket away and save it for possible future use. The screw will be used to hold the controller board in place.

4. Attach the 34-pin control cable connector pin 1 to J4. Keyed connectors prevent reversal of the cables.

5. Connect control cable to drive.

6. Attach drive 0's 20-pin data cable to J2. Data connectors are also keyed.

7. Attach drive 1's 20-pin data cable to J3.

8. Connect the cable(s) to the proper drives(s).

9. Attach the Winchester activity LED connector to J1. J1 is a reversible connector.

10. Install the controller board into the expansion slot. Ensure that the board is seated properly by pressing down on both ends of the board. Secure the board with the bracket screw.

Software Installation Instructions

This section contains instructions for preparing (low level format) the drive to be recognized by the operating system. Formatting the drive uses one of two software programs, the Advanced Diagnostics (or equivalent in AT compatibles) and the WDFMT.EXE or both programs. Use of the programs depends on the controller configuration. Configuring the controller to use the translation feature requires running the Advanced Diagnostics program, Setup, and WDFMT.EXE. Setup defines the drive type for the system and WDFMT.EXE low level formats the drive. Without translation, Advanced Diagnostics can low level format the drive if the system BIOS recognizes the 34 sector ESDI format. Run the DOS programs, FORMAT and FDISK, after performing the low level format, regardless of the controller configuration.

Software Installation Instructions for Translation Mode

Step Instruction

1. Insert the Diagnostics diskette, and turn on the power. After the system test, the program displays the following:

   **The IBM Personal Computer
   ADVANCE DIAGNOSTICS
   Version 1.04
   © Copyright IBM Corp. 1981, 1982, 1983, 1984**

   SELECT AN OPTION

   **0 - SYSTEM CHECKOUT
   1 - FORMAT DISKETTE
   2 - COPY DISKETTE
   3 - PREPARE SYSTEM FOR MOVING
   4 - SETUP
   9 - END DIAGNOSTICS**

   **SELECT THE ACTION DESIRED
   ?**

2. Enter 4 followed by a CARRIAGE RETURN or ENTER. The program displays:

   Use the information on the following screens to set or verify Time, Date, and Options.

   **Press "ENTER" to continue . . .
   ?**

3. Press CARRIAGE RETURN or ENTER. Key in the current date and time, if necessary, at the following displays:

   Current date is:

   If the current date is correct, press "ENTER".

   **If the current date is incorrect, type the new date MM-DD-YYYY. Then, press "ENTER".
   ?**

   Current time is:

   If the current time is correct, press "ENTER".

   If the current time is incorrect, type the new time HH:MM:SS. Then, press "ENTER".

   **24 hour format is required. (Example 1:00 pm is equal to 13:00:00 in 24 hour format.)
   ?**

4. After entering the current date and time, enter "n" at the following display prompt:

Your system may have other options installed.
They are not required for Setup and are not
displayed.

The following options have been set:

Diskette Drive A - High Capacity
Diskette Drive B - Double Sided
Fixed Disk Drive C - Type 4
Fixed Disk Drive D - Not Installed
Base Memory size - 512KB
Expansion memory size - 0KB
Primary display is attached to:
- Monochrome Display Adapter

Are these options correct (Y/N)
?n

Entering "n" at this point allows changing the drive
type. The program continues:

System options information is required to answer
the following questions.

Press "ENTER" continue . . .
?

5. After pressing ENTER, the program requests
information regarding the system diskette drives as
in the following example:

Your diskette drive types are set to the following:

Diskette Drive A - High Capacity
Diskette Drive B - Double Sided

Are diskette drive types correct (Y/N)
?y

6. The next displays define the drive type as follows:

Your fixed disk drive types are set to the following:

Fixed Disk Drive C - Type 4
Fixed Disk Drive D - Not Installed

Is this correct (Y/N)
?n

How many fixed disks are installed?

Enter 0, 1, or 2 for the number of fixed disk drives
installed.
?1

At this point, the drive type must be entered.
When using the translation mode, double the

---

number of physical head's but use the actual
number of cylinders. In the following example, the
drive contained four physical heads and 940
cylinders. Therefore, drive type 4 (8 heads, 940
cylinders) is chosen in this example. Refer to the
appropriate technical manual when determining the
drive types for AT compatibles.

Enter fixed disk type (1-15) for Fixed Disk Drive C.

* * WARNING * *

Entering the wrong drive type causes improper
operation of the fixed disk.
?4

You have set your fixed disk drive types to the
following:

Fixed Disk Drive C - Type 4
Fixed Disk Drive - Not Installed

Is this correct (Y/N)
?y

The primary display comes on when you turn
on the system power switch.

The primary display is attached to the
Monochrome Display adapter.

Is this correct (Y/N)
?y

Base memory is composed of:

- 256KB on the system board or,
- 512KB on the system board or,
- 640KB of Base memory consisting of 512KB
on the system board, and 128KB on the 128KB
Memory Expansion Option.

Base memory size is 512KB

Is this correct (Y/N)
?y

The Expansion Memory size is composed of
additional memory adapters not including the
128KB Memory Expansion option.
Expansion memory size is 0KB

Is this correct (Y/N)
?y

Your system may have other options installed.
They are not required for Setup and are not
displayed.

The following options have been set:

Diskette Drive A - High Capacity
Diskette Drive B - Double Sided
Fixed Disk Drive C - Type 4
Fixed Disk Drive D - Not Installed
Base memory size - 512KB
Expansion memory size - 0KB
Primary display is attached to:
- Monochrome Display Adapter

Are these options correct (Y/N)
?y

Press "ENTER" and stand by while system
resets . . .

7. Insert the DOS Diskette in drive A and boot
the system normally.

CAUTION
EXECUTION OF THE WD FORMAT
PROGRAM IN STEP 8 DESTROYS ALL
DATA ON THE TARGET DRIVE.

8. Remove the DOS diskette and insert the WD
Format diskette into drive A. Type in the following
command line if the drive configuration matches
the default description of 500 physical cylinders,
4 physical heads, 34 sectors/track and 3 to 1
interleave:

A> WDFMT.EXE

If the drive configuration does NOT match the
default values, type in the following command line:

A>WDFMT.EXE ccc hss i

Where:
    ccc is the number of physical cylinders (2048
    physical cylinders, maximum).
    h is the number of physical heads (1 to 16).
    ss is the sectors per track. (Must be 34 since
    the WD1005-WAH only supports hard sectored
    drives.)
    i is the interleave factor.
Separate each command line parameter by a space.

The WD Format program displays the following
menu:

*** Western Digital Corporation ***
Disk Format Utility
Rev. 1.00

Current par
Cylinders: (
    Sectors:

To enter nev
enter a new
    WDFMT -
    <interlea

Warning!!!! ,
destroyed. P
start format

Verifying cy

Separate the
entered. No
cylinder and

9. WD Format
information
block inforn
drive manuf;

You may no'
marked bad

Enter cylind
spaces) at th
ENTER at th

Enter <cylii

After enterin
program disj

Format com

A>

10. Run the FOl

11. Operate the

Software Inst
Non-Translati

Formatting'd
operational n
with a 34 sec

Software Installation Instructions for Translation Mode (Cont'd.)

Current parameters are:

Cylinders: 940	Heads: 4
Sectors: 34	Interleave: 3

To enter new parameters, return to DOS and enter a new command line as follows:

WDFMT <#cvls> < #heads> <#sectors> <interleave>

Warning!!!! All data on drive C will be destroyed. Press ESC to return to DOS, F to start format.

Verifying cylinder: XXX head: y

Separate the new parameters with a space, if entered. Note that the XXX and Y in Verifying cylinder and head line constantly up counts.

9. WD Format program requests bad block information with the following menu. (Bad block information must be supplied from the drive manufacturer.)

You may now enter additional blocks to be marked bad.

Enter cylinder and head info (separated by spaces) at the prompt. To end entry, press ENTER at the prompt.

Enter <cylinder#> <head#>:

After entering the bad blocks, the format program displays the following message:

Format complete . . . Bad block marked

A>

10. Run the FORMAT and FDISK utilities.

11. Operate the system normally.

Software Installation Instructions for Non-Translation Mode

NOTE
Formatting disk media with this operational mode requires a host system with a 34 sector BIOS.

Software Installation Instructions for Non-Translation Mode (Cont'd.)

Step Instruction

1. Boot the system with the Advanced Diagnostics. Define the drive types as described in the previous section, steps 1 through 6, if necessary. After defining the drive types, run System Checkout. Enter 0 after the "Select the action desired" prompt.

2. Select fixed disk option 17.

3. Select the Format Menu from the Fixed Disk Diagnostic Menu.

4. Unconditionally format the drive with the Format Selection Menu.

5. Enter bad blocks in the Defect Entry table.

6. Formatting begins. After formatting the drive, press "ENTER." Boot and operate the system normally.

If you require further information or other technical support, please contact your authorized dealer.

If You Have a Problem...

Listed below are some common problems.

PROBLEM: "Nothing Done Exit" message appears when formatting the drive.

COMMENT: "y" was not pressed. Initiate formatting procedure. Be sure to press "y".

PROBLEM: Drive does not partition.

COMMENT: Check drive types. Note that the drive types for the AT and Compaq machines differ.

PROBLEM: "Error Reading Fixed Disk" appears when booting from hard drive.

COMMENT: DOS partition not active.

PROBLEM: Winchester activity LED continuously lit.

COMMENT: No problem! This is normal operation for ATs.

PROBLEM: For systems with two controllers, both Winchester activity LEDs light at the same time.

COMMENT: Improper drive select or termination. Inspect the drive cables. If the data

Software Installation Instructions for Non-Translation Mode (Cont'd.)

cables are straight, then set both drives' select switches for drive select 2. If the data cables have a twist, set drive C's drive select switches for drive select 1 and drive D's drive select switches for drive select 2. Consult your drive manuals or dealer for drive switch settings. Finally, under no circumstance, use twisted floppy cables for the Winchester drive. Floppy and Winchester drive interface connections differ significantly.

PROBLEM: Error code 1701.

COMMENT: Power supply is overloaded.

PROBLEM: Error code 20.

COMMENT: Controller component malfunction. Controller plugged in incorrectly. Cables reversed. For controller failures, contact your dealer.

PROBLEM: Error code 40.

COMMENT: Wrong drive type. Not enough drive power.

PROBLEM: Error code 80.

COMMENT: Not enough drive power. Bad cables. Improper drive select or termination. Bad drive.

This list is by no means exhaustive. For example, error codes differ for many AT compatibles and their operating systems. If your solution was not listed, then contact your dealer for further information.

For Those of You Who Want to Know More...

Translation

Some versions of MS-DOS are unable to function when the physical number of sectors per track is greater than 17. This becomes a problem when integrating ESDI hard sector encoded drives. The problem can be overcome by letting the controller "translate" the extra sectors per track above 17 into information that the system can recognize. In the case of the WD1005, the controller firmware changes these extra sectors to a "logical" head value that is double the physical heads used. Because of physical limitations of the controller and the system BIOS, this logical value cannot be

Software Installation Instructions for Non-Translation Mode (Cont'd.)

greater than 16, thus limiting the physical head usage to 8. When selecting a drive type during installation, the above limitations must be taken into account. The standard drive tables in most AT type machines limit the usage of most ESDI type drives. The use of software that allows the drive parameters to be changed allows full use of the drive.

In the non-translation mode, the controller uses the actual physical characteristics of the drive. The system BIOS drive tables will not support this feature unless changed to meet the physical requirements of the drive. Software utilities that can change parameter information overcomes this need.

Low-Level Formatting

Regardless of the mode of operation selected, translation or non-translation, the drive must be formatted with 34 sectors per track. A formatting utility called WDFMT, available from Western Digital, allows the drive to be formatted in this manner. Other utilities such as AT Advanced Diagnostics will not function properly because they are designed to work with 17 sectors per track only.

When formatting in the translation mode, the physical number of heads are formatted at 34 sectors per track, not the logical number of heads. For example, if a drive with 4 heads is being used in the translation mode, the logical head will be 8, but the 4 physical heads are formatted at 34 sectors per track.

When using the controller in the non-translation mode, the drive may be formatted to its full physical characteristics, with limits of 16 heads and 2048 cylinders.

DOS Usage/Partitioning

Most ESDI drives will have capacities beyond the DOS 32 megabyte limit. The use of third party software that will allow the drive to be split into multiple partitions can be used to get past the DOS limit. Compaq DOS and its associated FDISK and ENHDISK.SYS programs have the ability to create multiple partitions. New products available from Ontrack Computer Systems and Storage Dimensions have such capabilities. The Disk Manager program from Ontrack and Compaq DOS are the only ones that have been tested at this time. Both work well, providing full usage of the ESDI capacities. Finally, the SpeedStor 286 BIOS contains 34 sectors per track drive parameter tables and supports a 17 sector per track translation mode for extended (more than 16 physical head) drives. SpeedStor also provides a diskette for installation.

J1: WINCHESTER ACTIVITY LED CONNECTOR

W3:
JUMPER 2-3:
PRIMARY ADDRESS RANGE.
STANDARD FACTORY SETTING.

JUMPER 1-2:
SECONDARY ADDRESS RANGE.
SETTING FOR
SECOND CONTROLLER.

NO JUMPER.
STANDARD FACTORY SETTING.

JUMPER 1-2:
SPECIAL TEST SETTING
FOR ORIGINAL EQUIPMENT
MANUFACTURER (O.E.M.).

W1:

J2   J3   J4

1   J1

U6

1 W1

U7

U13

WD5010

1 W2

U14

P2   P3

W3

1

12

W2:
NO JUMPER. ENABLES TRANSLATION. MS-DOS COMPATIBLE SETTING.
STANDARD FACTORY SETTING.
JUMPER 1-2. DISABLES TRANSLATION.

WESTERN DIGITAL
CORPORATION

WD1005-SCS WINCHESTER DISK CONTROLLER

FEATURES

- CONTROLS FOUR SERIAL MODE ESDI COMPATIBLE DRIVES
  - 10 MBITS/SEC
  - SOFT/HARD SECTOR DRIVE
  - AUTO CONFIGURATION FOR EACH DRIVE
- SUPPORTS DRIVES WITH UP TO 16 HEADS, AND 2048 CYLINDERS
- SCSI HOST TRANSFER RATE UP TO 1.67 MBYTE/SEC
- FULL FIRMWARE COMPLIANCE WITH ANSI SCSI X3T9.2 REV. 4A COMMON COMMAND SET
- MULTITHREADED OPERATIONS (MULTIPLE INITIATOR COMMAND QUEUING)
- USER SELECTABLE DEVICE ADDRESS
- LOGICAL UNIT ADDRESSING
- RESERVATIONS SUPPORTED
- PROGRAMMABLE DISCONNECT OPTIONS:
  - IMMEDIATELY UPON RECEIPT OF A COMMAND
  - IMMEDIATELY UPON THE START OF A FORMAT OPERATION
  - SEEKS FOR ONE OR MORE CYLINDERS
  - WHEN A SECTOR OF DATA HAS BEEN TRANSFERRED FROM THE HOST TO THE DATA BUFFER
  - WHEN DATA FROM THE HOST FILLS THE DATA BUFFER
- PROGRAMMABLE RECONNECT OPTIONS:
  - RECONNECTS TIME-OUT
  - THE DISK TRANSFERS ONE SECTOR OF DATA TO THE DATA BUFFER AND THE DATA HAS BEEN VERIFIED

- THE DISK FILLS THE DATA BUFFER (UP TO TWO SECTORS) AND THE DATA IS VERIFIED
- RECONNECT A PROGRAMMABLE NUMBER OF SECTORS PRIOR TO THE START OF DATA TRANSFER FROM THE DISK TO THE DATA BUFFER
- PROGRAMMABLE DEFECT HANDLING OPTIONS:
  - AUTOMATIC DEFECT MAPPING
  - A REASSIGN BLOCK COMMAND FOR POST FORMAT DEFECTS
  - SPARE ALLOCATION ON SECTOR AND/OR TRACK BASIS
  - SPARE SECTORS LOCATED ON SAME CYLINDER
  - PROGRAMMABLE NUMBER OF SPARE SECTORS SPREAD EVENLY OVER THE DISK
  - SUPPORTS A DEFECT LIST IN CYL/HD/SEC, CYL/HD/OFFSET FROM INDEX, OR LOGICAL SECTOR NUMBER FORMAT
- PROGRAMMABLE SECTOR SIZES (128, 256, 512, AND 1024 BYTES PER SECTOR)
- PROGRAMMABLE GAP SIZES
- PROGRAMMABLE INTERLEAVE (INCLUDING 1:1)
- 56-BIT ECC FOR WINCHESTER DATA ERROR DETECTION AND CORRECTION
- EXTENDED SENSE CAPABILITY
- SCSI BUS PARITY OPTION
- SCSI COMPATIBLE BUS HOST INTERFACE
- FULL HARDWARE COMPLIANCE WITH ANSI SCSI X3T9.2 SPECIFICATIONS
- SELF-TEST DIAGNOSTICS

DOCUMENT SCOPE

The intent of this document is to provide the reader with an overview of the WD1005-SCS. Following is a list of documents that will provide the reader with all necessary information:

- WD1005-SCS Winchester Disk Controller   OEM Manual (DOC. 79-000062)
- SCSI Specification ANSI X3T9.2
- SCSI Commond Command Set Specification ANSI X3T9.2/85-82 REV. 4A
- Enhanced Small Device Interface Specification Rev. D July 1, 1984
- WD5010-10 Winchester Controller.....Data Sheet
- WD11C00-14 56-Bit ECC Support Device.....Data Sheet
- WD11C00-19 SCSI Protocol Support Device...Data Sheet
- WD50C20-10 ESDI Adapter Device....Data Sheet

DESCRIPTION

The WD1005-SCS is a single-board Winchester Disk Controller, designed to support up to four Enhanced Small Device Interface (ESDI) compatible disk drives and to interface with the Small Computer System Interface (SCSI) bus. Bus operation is in compliance with the ANSI X3T9.2 SCSI Specification.

Commands directed to the drives are executed by the WD1005-SCS. All communications and data transfers to and from the Host take place via the SCSI bus, in accordance with SCSI protocol.

The WD1005-SCS functions only as a Target device in the SCSI environment. The WD1005-SCS supports disconnect/reconnect operations, allowing for more efficient SCSI bus utilization. SCSI bus arbitration is provided allowing for multiple initiator operation. In addition, the WD1005-SCS Controller board supports one-to-one disk interleave, i.e., fully sustained operations on sequential disk access.

The WD1005-SCS is based on a proprietary chip set, consisting of the WD5010-10, WD11C00-14, WD50C20-10, and WD11C00-19 LSI devices, designed specifically for Winchester/SCSI interface. Extensive error detection and correction, as well as data recovery techniques for disk errors, are incorporated within the controller's design. The 56-Bit error correction circuitry resides in the WD11C00-14. The WD11C00-19 is used to control all communications and data transfer.

ARCHITECTURE

The WD1005-SCS architecture allows an optimum amount of design functions to reside within the board. This is accomplished by creating a unified internal bus structure, whereby all major LSI devices share the same buses.

As illustrated in Figure 1, the WD1005-SCS contains five major VLSI devices:

- 8085 microprocessor
- WD5010-10 Winchester Controller
- WD50C20-10 ESDI Adapter Device
- WD11C00-14 56-Bit ECC Support Device
- WD11C00-19 SCSI Protocol Support Device

Control Processor

The Control Processor is an 8085 microprocessor used for the main board control and is supported by a 27128 (16K X 8) EPROM and a (2K X 8) 2016 static RAM device. The WD1005-SCS Controller's unique architecture facilitates two major functions:

- Support of the SCSI bus application
- 1:1 interleave capability

WD5010-10 Winchester Disk Controller

The primary function of the WD5010-10 is to control data transfer between the disk and the Sector Buffer, after the on-board control processor has positioned the selected head over the desired track. The WD5010-10 receives the parameters and commands from the control processor via the CD0 through CD7 bus.

In addition, the WD11C00-14 assists the WD5010-10 in performing the 56-Bit error detection and correction on all data transfers from the disk.

WD50C20 ESDI Adapter Device

The WD50C20 is an LSI device, implemented in a 3-micron, high-speed CMOS process. It converts the MFM Read and Write Data presented by the WD5010 Interface into NRZ Read and Write Data for use by the ESDI Drive. The WD50C20 also controls communications to serial mode ESDI drives. A serial communication transfer error is reported to the on board 8085 which will make a maximum of 3 attempts to correct the error.

WD11C00-19 SCSI Protocol Support Device

The WD11C00-19 is a 40-pin LSI device designed to provide five major support functions:

- Memory address generation
- Data transfer (read/write) control
- Arbitration
- Parity checker/generator
- SCSI Bus control

All SCSI commands are read, format converted, and then issued to the WD5010-10 for execution.

2

FIGURE 1. BLOCK DIAGRAM
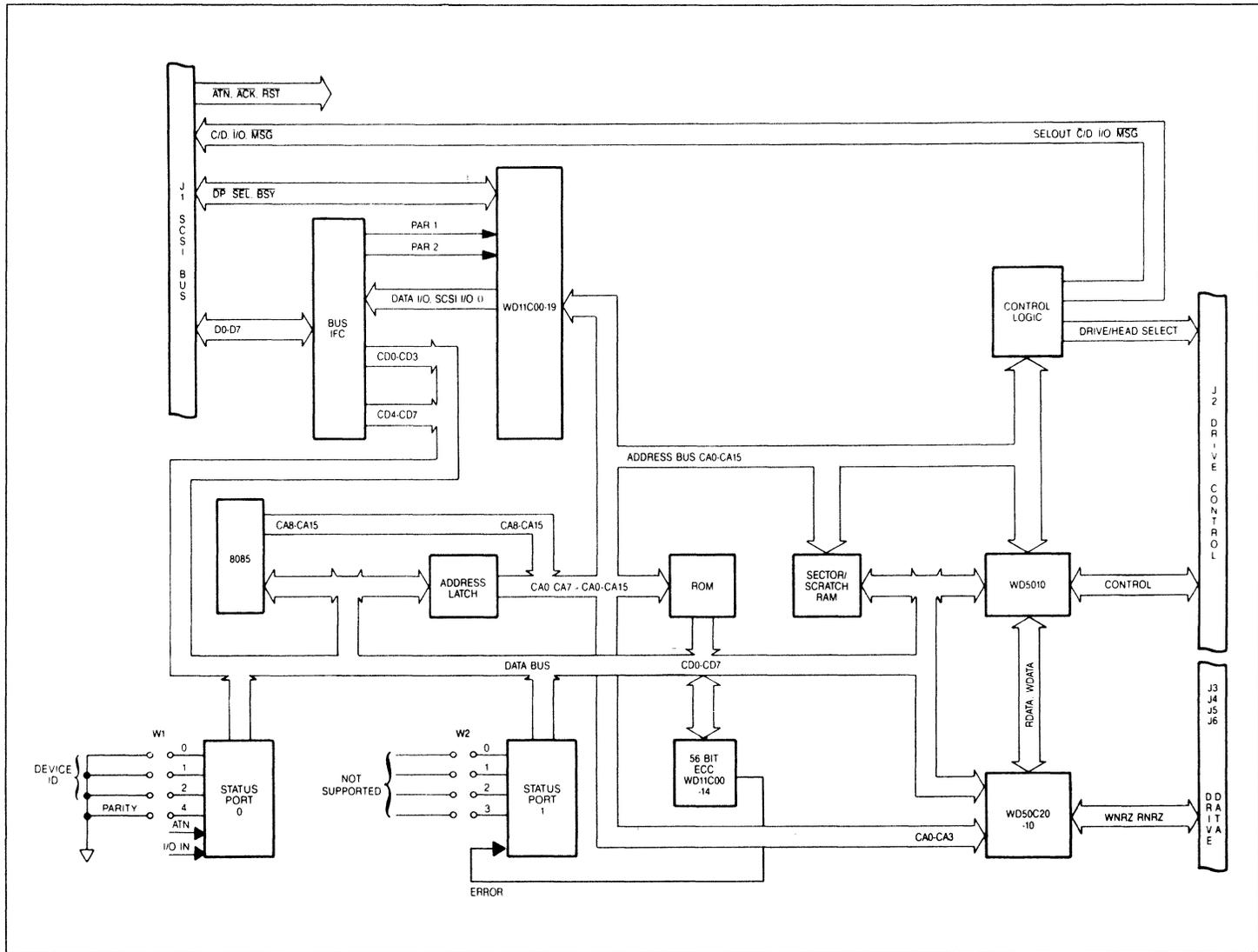
SPECIFICATION

Host Interface

Type	SCSI
Cable length	20 ft (6 m) max.
Termination all signals	Socketed 220/330 ohm resistor pack
	220 ohms to +5 Volts,
	330 ohms to ground
Addressing	Jumper selectable (0 through 7)
	Default = 0

Drive Interface

Cylinders per drive	Programmable up to 2048
Bytes per sector	Programmable (128, 256, 512, 1024)
Sectors per track	Programmable
Heads per cylinder	Programmable up to 16
Drives	4
Data transfer rate	10 Mbps
Sectoring	Soft and hard
CRC polynomial	$X^{16} + X^{12} + X^5 + 1$
ECC polynomial – 56-Bit	$X^{56} + X^{52} + X^{50} + X^{43} + X^{41} + X^{34} + X^{30} + X^{26} + X^{24} + X^8 + X^0$

Cable length:	
Control (daisy-chained)	10 ft (3 m) max.
Data (radially connected)	10 ft (3 m) max.
Termination:	All signals 220 ohms to +5 Volts, 330 ohms to ground
Control	On last drive in chain
Data	On WD1005-SCS

Electrical

Voltage and Current	+5 Vdc ±5% @ 2.0 amps nominal 2.5 amps max

SCSI electrical description

When measured at the SCSI bus device connection, each signal driven by an SCSI device has the following output characteristics:

Signal assertion = 0 to 0.5 Vdc
Minimum driver output capability = 48 mA (sinking) @ 0.5 Vdc

Measured at the connector, each signal has the following input characteristics:

Signal asserted	0 to 0.8 Vdc
Maximum total input load	–0.4 mA @ 0.4 Vdc
Signal de-asserted	2.0 to 5.00 Vdc

Physical Dimensions

Length	8 inches (20.3 cm)
Width	5.75 inches (14.6 cm)
Height (including board, components and leads)	0.75 inches (1.9 cm)

Environment

Temperature:	
Operating range	0°C (32°F) to 55°C (131°F)
Storage range	–40°C (–40°F) to 60°C (140°F)
Relative Humidity:	
Operating range	8% to 80% non-condensing
Storage range	5% to 95% non-condensing
Maximum wet bulb	24°C (75°F)
Altitude:	
Operating range	0 to 10,000 ft (3000 m)
Airflow	150 linear ft/min @ 0.25 inches from component surfaces

INTERFACE ORGANIZATION

The WD1005-SCS is designed to be mounted directly onto a 5.25'' Winchester-type hard disk drive. It contains six vertical-header connectors, a 34-pin edge connector, and one power connector located along the peripheral edges of the board:

- Four Winchester drive data connectors J3, J4, J5, J6

- Two Winchester drive control connectors, one vertical-header and one edge connector. These connectors are mutually exclusive and are both referred to as J2.

- Power connector J7

- Host interface connector J1

The WD1005-SCS accommodates up to four Winchester hard disk drives. The control cable is daisy-chained to each of the four drives; and the drive data cables, which carry differential signals, are radially connected. Table 1 defines the WD1005-SCS connectors and a source for the mating connectors on the associated cables.

TABLE 1. CONNECTOR NUMBERS

CONNECTOR	INTERFACE FUNCTION	EQUIVALENT MATING CONNECTOR
J3, J4 J5, J6	Drive Data (Radially-connected)	Burndy #FRS20BS
J2	Drive Control (Daisy-chained)	Burndy #FRS34BS or #FRE34B
J7	Power	AMP 1-484042-1-0
J1	Host Interface (SCSI Bus)	Burndy #FRS50BS

HOST INTERFACE CONNECTOR

The WD1005-SCS interfaces with the Host via J1, a 50-pin vertical header connector mounted on 0.1 inch centers. The cable used should be a flat ribbon or twisted pair cable of not more than 20 feet in length. Cable termination is via 220/330 ohm resistor packs in position Z1 and Z2. Each signal is terminated to +5 volts, via 220 ohms and 330 ohms to ground. Table 2 provides the connector pin descriptions and its bus signals.

TABLE 2. HOST INTERFACE CONNECTOR (J1) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O *	FUNCTION
1 thru 17	2 thru 18	$\overline{DB0}$ thru $\overline{DB7}$ and $\overline{DBP}$	$\overline{DATA\ BUS\ 0}$ thru $\overline{DATA\ BUS\ 7}$ $\overline{DATA\ BUS\ PARITY}$	I/O	These signals comprise the SCSI tri-state, bi-directional data bus used to transfer commands, status, and data. $\overline{DB0}$ through $\overline{DB7}$ are used for Target device selection and arbitration. $\overline{DBP}$ is odd parity for $\overline{DB0}$ through $\overline{DB7}$ and is not valid during the arbitration process.
19	20	GND	GROUND		
21		GND	GROUND		
	22	NOT CON			
23	24	GND	GROUND		
25		GND	GROUND		
	26	NOT CON			
27	28	GND	GROUND		
29	30	GND	GROUND		

* The I/O column is in relation to the WD1005-SCS and not the Host.

TABLE 2. HOST INTERFACE CONNECTOR (J1) PIN DESCRIPTION (Continued)

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O *	FUNCTION
31	32	ATN	ATTENTION	I	Asserted by the Host to indicate that a message is ready for the WD1005-SCS. This message is read by the WD1005-SCS at its convenience by performing a Message Out Phase.
33	34	GROUND			
35	36	BSY	BUSY	I/O	When asserted as an output, BSY indicates to the Host that the WD1005-SCS is busy executing a command. When asserted as an input, BSY indicates to the WD1005-SCS that the bus is busy with another device and must wait to reselect the Host.
37	38	ACK	ACKNOWLEDGE	I	ACK is the Host's acknowledgment of REQ during a data transfer handshake. It signals the WD1005-SCS that the Host has accepted the data transfer.
39	40	RST	RESET	I	When asserted at least 25 usec, RST places the WD1005-SCS into its initial power-up state.
41	42	MSG	MESSAGE	O	Asserted during the Message Byte Transfer Phase. Used with I/O and C/D to indicate the type of transfer.
43	44	SEL	SELECT	I/O	Used by the Host to select the WD1005-SCS, or by the WD1005-SCS to reselect the Host.
45	46	C/D	CONTROL/DATA	O	C/D along with I/O and MSG Indicates to the Host whether control or data is on the bus. C/D – 0 = Control – 1 = Data Control is defined as command, status, or message.
47	48	REQ	REQUEST	O	A request for a REQ/ACK data transfer handshake. Indicates to the Host that the WD1005-SCS is ready for data transfer.
49	50	I/O	INPUT/OUTPUT	O	Indicates the direction of transfer between the Host and the WD1005-SCS. I/O – 0 = Input to the Host – 1 = Output from the Host

* The I/O column is in relation to the WD1005-SCS and not Host.

WINCHESTER DRIVE CONTROL CONNECTOR

The WD1005-SCS supports the Serial Mode ESDI Drive control protocol. The drive control signals may be connected to either the 34-pin vertical header mounted on a 0.1 inch center, or the 34-pin edge connector. Control signals are common to all drives and are daisy-chained on a single connector J2. The cable used should be a flat ribbon or twisted-pair not more than 10 feet in length.

The control signals are to be terminated at the last drive in the daisy-chain with a 220/330 ohm resistor pack. Each control signal is connected to +5 volts with the 220 ohm resistor and to ground with 330 ohms.

The drive control connector J2 pin description is provided in Table 3.

TABLE 3. DRIVE CONTROL (J2) PIN DESCRIPTION

SIG. GND.	SIG. PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	2	$\overline{HS3}$	$\overline{HEAD}$ $\overline{SELECT}$ 3	O	$\overline{HS3}$ is one of four Head Select signals decoded by the drive to select one of 16 R/W heads.
3	4	$\overline{HS2}$	$\overline{HEAD}$ $\overline{SELECT}$ 2	O	One of four Head Select signals decoded by the drive to select one of 16 R/W heads.
5	6	$\overline{WG}$	$\overline{WRITE\ GATE}$	O	$\overline{WG}$ is asserted when valid data is to be written on the disk. WD1005-SCS de-asserts this signal when a $\overline{ATN}$ is detected.
7	8	$\overline{CSD}$	$\overline{CONFIG\ DATA}$ $\overline{STATUS}$	I	The $\overline{CSD}$ signal represents the 16 bits of Configuration Data or Status plus a Parity bit requested by the WD1005-SCS. The transfer of this data is under control of the $\overline{XREQ}/\overline{XACK}$ handshake.
9	10	$\overline{XACK}$	$\overline{TRANSFER}$ $\overline{ACKNOWLEDGE}$	I	$\overline{XACK}/\overline{XREQ}$ form the transfer handshake for all $\overline{CSD}$ and $\overline{CMD}$ transfers between the drive and the WD1005-SCS.
11	12	$\overline{ATN}$	$\overline{ATTENION}$	I	$\overline{ATN}$ informs the WD1005-SCS of a fault condition.
13	14	$\overline{HS0}$	$\overline{HEAD}$ $\overline{SELECT}$ 0	O	One of four Head Select signals decoded by the drive to select one of 16 R/W heads.
15	16	$\overline{SCT}/\overline{AMF}$	$\overline{SECTOR}/$ $\overline{ADDRESS}$ $\overline{MARK\ FOUND}$	I	For hard sector drives $\overline{SCT}$ is asserted at the start of a sector. For soft sector drives $\overline{AMF}$ is asserted at the end of an Address Mark.
17	18	$\overline{HS1}$	$\overline{HEAD}$ $\overline{SELECT}$ 1	O	One of four Head Select signals decoded by the drive to select one of 16 R/W heads.
19	20	$\overline{INDEX}$	$\overline{INDEX\ PULSE}$	I	Indicates the start of a track and is used both as a synchronization point during formatting and a time-out mechanism for retries. This signal pulses once for each disk revolution.
21	22	$\overline{DRDY}$	$\overline{DRIVE\ READY}$	I	Informs the WD1005-SCS that the drive motor is up to speed.
23	24	$\overline{XREQ}$	$\overline{TRANSFER}$ $\overline{REQUEST}$	O	$\overline{XREQ}/\overline{XACK}$ form the transfer handshake for all $\overline{CSD}$ and $\overline{CMD}$ transfers between the drive and the WD1005-SCS.
25	26	$\overline{DSEL\ 1}$	$\overline{DRIVE}$ $\overline{SELECT}$ 1	O	$\overline{DSEL\ 1}$ is one of three signals encoded for drive selection.
27	28	$\overline{DSEL\ 2}$	$\overline{DRIVE}$ $\overline{SELECT}$ 2	O	$\overline{DSEL\ 2}$ is one of three signals encoded for drive selection.
29	30	$\overline{DSEL\ 3}$	$\overline{DRIVE}$ $\overline{SELECT}$ 3	O	$\overline{DSEL\ 3}$ is one of three signals encoded for drive selection.
31	32	$\overline{RG}$	$\overline{READ\ GATE}$	O	When asserted, $\overline{RG}$ enables data to be read from the disk.
33	34	$\overline{CMD}$	$\overline{COMMAND}$	O	The $\overline{CMD}$ signal transmits the 16 command bits plus a parity bit to the drive. This transfer is controlled by the $\overline{XREQ}/\overline{XACK}$ handshake.

WINCHESTER DRIVE DATA CONNECTOR

The data is differential in nature and must be radially connected to each drive with its own cable, drive 0 to J3 and drive 1 to J4 etc. It should be a flat ribbon cable, or twisted pair, not more than 10 ft. in length. The connector is a 20-pin vertical header on .1 inch center.

TABLE 4. DRIVE DATA CONNECTORS - J3, J4, J5, J6

SIG. GND.	SIG. PIN	I/O	SIGNAL NAME
	1		Drive Selected
2			NC
	3		Command Complete
	4		Address Mark Enable
	5		NC
6			GND
	7		+ Write Clock
	8		− Write Clock
	9		NC
	10		+ Read/Ref. Clock
	11		− Read/Ref. Clock
12			GND
	13	O	+ Write Data
	14	O	− Write Data
15			GND
16			GND
	17	I	+ Read Data
	18	I	− Read Data
19			GND
20			NC

POWER CONNECTOR

A 4-pin connector (J7) is provided for power input to the WD1005-SCS board.

PIN	VOLTAGE
1	NC
2	GND.
3	GND.
4	+5 V

COMMAND DESCRIPTION

The commands are separated into three Groups, group 0 standard commands, group 1 extended commands, and group 7 diagnostic commands. Commands in group 0 and 7 are received from the Host in a six-byte Command Descriptor Block format, while commands in group 1 are received in a 10-byte format.

A list of the commands supported by the WD1005-SCS, along with the two Command Description Block formats, follows. A detailed description of the commands is provided in the OEM Manual.

TABLE 5. COMMAND LIST

COMMAND	OP CODE
TEST DRIVE READY	00
REZERO UNIT	01
REQUEST SENSE	03
FORMAT UNIT	04
REASSIGN BLOCKS	07
READ	08
WRITE	0A
SEEK	0B
INQUIRY	12
MODE SELECT	15
RESERVE UNIT	16
RELEASE UNIT	17
MODE SENSE	1A
RECEIVE DIAGNOSTIC	1C
SEND DIAGNOSTIC	1D
READ CAPACITY	25
READ EXTENDED	28
WRITE EXTENDED	2A
SEEK EXTENDED	2B
VERIFY	2F
READ DEFECT DATA	37
WRITE BUFFER	3B
READ BUFFER	3C
READ LONG	E5
WRITE LONG	E6

GROUP 0 AND 7 COMMAND DESCRIPTION BLOCK

The Command Description Block format used by the Group 0 and 7 commands is provided in Figure 2.

BYTE	BITS							
	7	6	5	4	3	2	1	0
0	OPERATION CODE							
1	LUN			LOGICAL BLOCK ADDRESS (MSB), FORMAT DATA, COMPLETE LIST, DEFECT LIST FORMAT				
2	LOGICAL BLOCK ADDRESS							
3	LOGICAL BLOCK ADDRESS (LSB) OR INTERLEAVE (MSB)							
4	NUMBER OF BLOCKS, NUMBER OF REQUEST SENSE BYTES, NUMBER OF BYTES, INTERLEAVE (LSB), OR PARAMETER LIST LENGTH							
5	ERTY	0	0	0	0	0	0	0

FIGURE 2. GROUP 0 AND 7 COMMAND DESCRIPTION BLOCK

Operation Code — Bits 7-5 designate the command Group, 0 or 7.

Bits 4-0 identify the command function within Group 0 or 7, e.g., Read or Write.

LUN — Specifies the Logical Unit Number of the attached drive. May be any quantity 0 through 3.

Logical Block Address — Specifies the Logical Block Address (LBA) where an operation is to begin.

Format Data, Complete List, Defect List Format — Used in conjunction with the Format Commands:

• Format Data. Bit 4 of byte 1.
• Complete List. Bit 3 of byte 1.
• Defect List. Bits 2, 1, and 0 of byte 1.

Interleave — The interleave factor is used by Format Commands. The disk may be formatted at a 1:1 ratio with the maximum interleave equal to the number of sectors-per-track minus one.

Byte 3 must be zero, byte 4 can be any interleave number from 0 through 128. If an interleave factor of 0 is used, the WD1005-SCS uses a default interleave value of 2.

Number of Blocks — Indicates the number of contiguous logical data blocks to be transferred by an operation. When zero, 256 blocks are transferred. Any other value indicates the number of blocks to be transferred.

Number of Requested Sense Bytes — The number of bytes indicates the length of data allocated by the Host for the returned sense information. The WD1005-SCS only returns sense data in the Extended Sense format.

A requested sense byte count of zero defaults to a data transfer of four bytes. A requested count greater than zero results in a data transfer equal to the request, but never more than eighteen bytes.

Number of Bytes — Used by the Inquiry Command, the Number of Bytes indicates the data length allocated by the Host for the Returned Sense data.

Parameter List Length — The only valid length for proper operation is 30 (decimal). Zero represents a No-Operation condition.

ERTY — Disk error retry bit. When reset, indicates a request for a retry operation. (Used if retries are supported by a specific command.)

GROUP 1 COMMAND DESCRIPTION BLOCK

The Command Description Block format used by the Group 1 commands is provided in Figure 3.

BYTE	BITS							
	7	6	5	4	3	2	1	0
0	OPERATION CODE							
1	LUN			0	0	0	0	0
2	LOGICAL BLOCK ADDRESS (MSB)							
3	LOGICAL BLOCK ADDRESS							
4	LOGICAL BLOCK ADDRESS							
5	LOGICAL BLOCK ADDRESS (LSB)							
6	0	0	0	0	0	0	0	0
7	BUFFER TRANSFER LENGTH, NUMBER OF BLOCKS (MSB)							
8	BUFFER TRANSFER LENGTH, NUMBER OF BLOCKS (LSB) OR PARTIAL MEDIUM INDICATOR							
9	ERTY	0	0	0	0	0	0	0

FIGURE 3. GROUP 1 COMMAND DESCRIPTION BLOCK FORMAT

Operation Code — Bits 7-5 designate command Group 1.

Bits 4-0 identify the function of a command within Group 1, e.g., Read Extended, Write Extended, or Seek Extended to be performed.

LUN — Specifies the Logical Unit Number of the attached drive. May be any quantity 0 through 3.

Logical Block Address — Specifies the Logical Block Address where an operation is to begin.

Buffer Transfer Length — BTL is used by the Read Defect Data, Read Buffer, and Write Buffer Commands. It indicates the number of data bytes to be transferred to or from the Host.

Number of Blocks — Indicates the number of contiguous logical data blocks to be transferred by an operation. When zero, no blocks are transferred. Any other value indicates the number of blocks to be transferred, up to 64K (65535).

PMI — Partial Medium Indicator. Bit 0 of byte 8 used in the Read Capacity Command.

0 = Controller returns address of the last block on the LUN device.
1 = Controller returns the address of the last block, prior to a cylinder boundary following the Block Address given by the Host. For example, Block Address 0 results in the controller returning Block Address 67 on a device with four heads, and is formatted with 17 sectors per track (512 bytes per sector and no Bad Block Mapping).

ERTY — Disk error retry bit. When reset, it requests a retry operation on an error condition. (Used if retries are supported by a specific command.)

TABLE 6. COMMON COMMAND SET ERROR CODES

ERROR CODE (HEX)	ERROR NAME	TYPE OF ERROR	ERROR CODE (HEX)	ERROR NAME	TYPE OF ERROR
00	No Sense		99	Bad Block	Operational
03	Write Fault	Disk Drive	9A	Bad DIF	Operational or Disk Drive Media
04	Drive Not Ready	Disk Drive	9B	Cannot Read Alternate Track Information	
06	Track 0 Not Found	Disk Drive			
10	ID CRC or ECC Error	Disk Drive or Media	9C	Disk Not Formated Correctly	Operational
11	Uncorrectable Data Error	Disk Drive or Media	A0	Bad Command	Command
13	Data Address Mark Not Found	Disk Drive or Media	A1	Illegal Block Address	Operational
18	Correctable Data Error	Media	B0	Bad ROM	Diagnostics
29	Power On or Bus Device Reset	Unit Attention	B2	Bad Winchester	Diagnostics
32	No Defect Spare Location Available	Media	B3	Bad Address Generation	Diagnostics
40	Bad RAM	Diagnostics	B4	Bad Instruction Set	Diagnostics
			B7	Bad Bus	Diagnostics

WESTERN DIGITAL
C O R P O R A T I O N

| 2445 McCABE WAY | |
| IRVINE, CALIFORNIA 92714 | (714) 863-0102, TWX 910-595-1139 |

WD1005-WAH

Features

PC XT height, full slot form factor

AT bus compatible

Controls one or two enhanced small device interface (ESDI) compatible drives with a maximum of 16 heads and 2048 cylinders

MS-DOS mode translates logical tracks to physical tracks; i.e., 17 sectors per track to 34 sectors per track

16-bit data bus for high speed data transfers

8-bit, bi-directional bus for control and status transfers

Multiple sector read/write commands (may cross head and cylinder boundaries)

Read/write, diagnostic, and verify commands

Implied and overlapped seek commands

56-bit ECC for Winchester error detection and correction

Programmable retries/no retries

Hard sectored format (512 bytes/sector, up to 36 sectors/track)

Supports 3:1 interleave

Two 2048 x 8 RAMs for sector data buffer

Design based on a Western Digital chip set consisting of:
    WD1014
    WD1015-23
    WD5010B-10
    WD50C20A-10
    WD1100-14

10.0 MBS data rate

Certifiable as a Class B Computing Device pursuant to Subpart J of Part 15 of F.C.C. Rules

WD1005-WAH BLOCK DIAGRAM

WESTERN DIGITAL
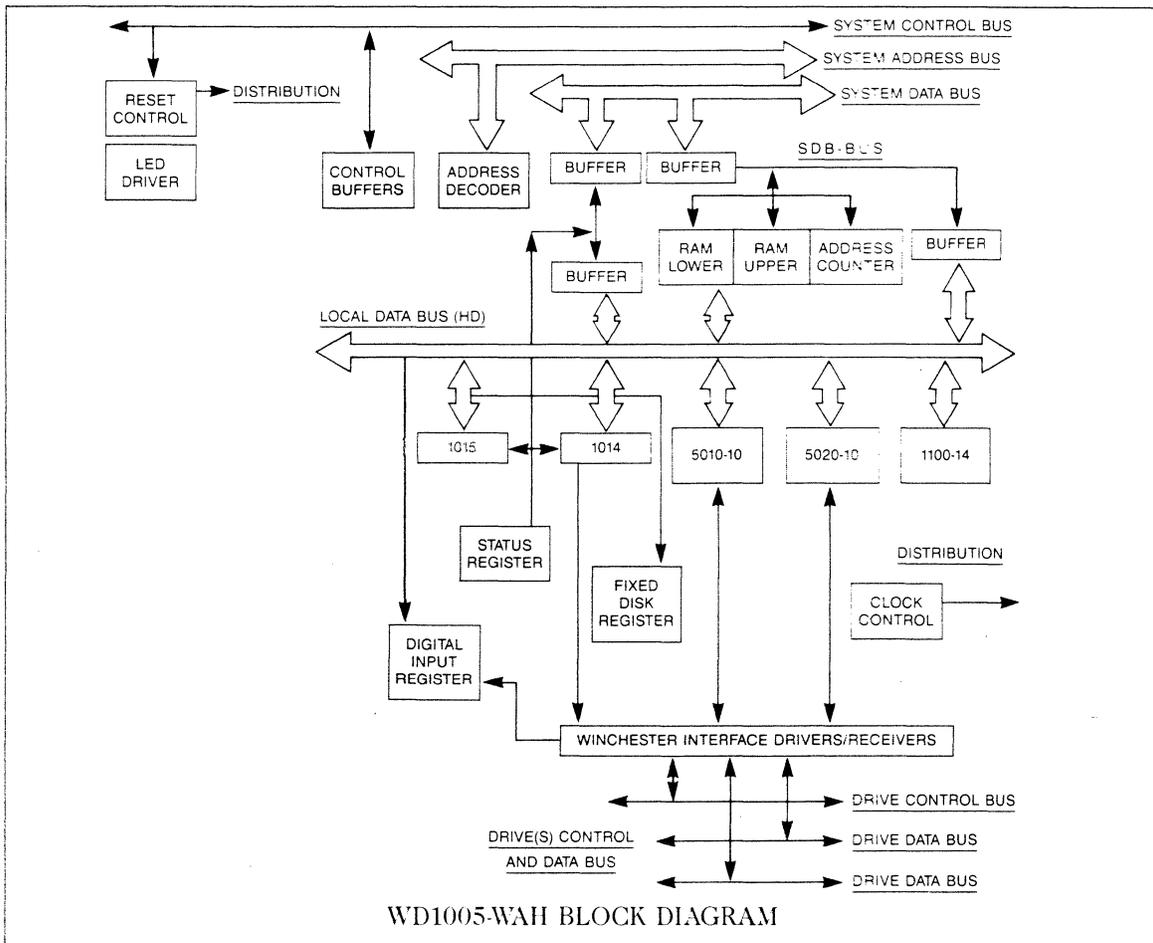
ESDI Winchester Disk Controller

Description

The WD1005-WAH Win-chester Disk Controller is an IBM PC AT bus compatible module designed to interface one or two disk drives. The WD1005-WAH's drive interface conforms to the ESDI speci-fication. Drives need not be of the same capacity or con-figuration. All necessary receivers and drivers are included on the board for direct connection to the drive(s).

Host System Address, Data, and Control Buses interface directly with the WD1005-WAH. Pro-grammed Input/Output (PIO) is the only operational mode for all data, control, and status transfers. All data transfers, except ECC bytes during Read and Write Long operations, are six-teen bits wide. Control and status transfers are 8-bits wide.

Western Digital implements the WD1005-WAH's architec-ture with the WD10C14, WD1015-23, WD5010B-10, WD50C20A-10, and WD1100-14. Extensive error detection and correction, as well as data recovery techni-ques for disk errors, are incorporated within the controller's design.

WD10C14

Module support registers within the WD10C14 include Command/Error, and Sector Size, Drive, Head (SDH) Registers. Only the WD1015-23 directly accesses the WD10C14's Command/Error Register. Either the host or the WD1015-23 may access the SDH Register.

WD1015-23

This device is an 8-bit microprocessor that controls and coordinates the activity of the disk drives, WD5010B-10, WD50C20A-10, and WD1100-14. The WD1015-23 receives and sends command or status information over an internal multiplexed address/data bus. Access to the registers in the WD5010B-10, WD50C20A-10, or WD1100-14 aid the execution of host generated commands as well as error recovery procedures. Additionally, the WD1015-23 performs several module self-tests following a Diagnose Command. Firmware con-trolling these functions resides in the WD1015-23's 2K internal ROM.

WD5010B-10

This advanced design VLSI device controls all data transfers between the Sector Buffer and the drives. The WD5010B-10 performs either single or multiple sector Read/Write commands. The WD5010B-10 also executes programmable format and error recovery algorithms. All commands are executed through the Task Files of the WD5010B-10 after limited intervention by the WD1015-23.

WD50C20A-10

This companion chip to the WD5010B-10 converts the WD5010B-10 data format to the format required by ESDI drives. An 8-bit host interface data bus parallels the WD5010B-10 host interface data bus. Parallel buses transmit WD5010B-10 Task File information into the WD50C20A-10 Task File. A portion of the WD50C20A-10 Task File also stores ESDI information for serial data transfers in addition to device commands and status. The WD50C20A-10 in this applica-tion operates with hard sectored serial mode ESDI disk drives.

WD1100-14

The WD1100-14 ECC polynomial generator/checker with a 12-bit correction span detects a single burst with up to 32 bits in error. Seven check/syndrome bytes (56 bits) are generated and appended to the data field for the error detection and correction process.

WESTERN DIGITAL

NEW PRODUCT BULLETIN

WD1005-SCS

SCSI/ESDI CONTROLLER

FEATURES:

* 5 3/4" x 8" form factor

* SCSI host interface (2.0 MB/s)

* ESDI drive interface (10 Mbits/s)

* Supports up to 4 drives with up to 16 heads

* Soft/hard sector format

* Bus Arbitration including Disconnect/Reconnect

* Standard and Extended commands

* Queued commands

* On-board ping pong buffer

* Supports ESDI Serial Mode Operation with Parity

* Programmable interleave including Read/Write
  continguous sectors (1:1)

* Multiple sectors Reads/Writes with a single command

* Programmable 256/512/1024 Bytes/sector

* 32 bit ECC included in WD2010-10

* Automatic media defect mapping

* On-board diagnostics for drive and controller

* Optional commands on ESDI

* Single +5V supply

DESCRIPTION:

The WD1005-SCS is a single board controller to interface SCSI hosts with up to 7 ESDI drives. Up to 2 MBytes/sec data rates are supported in the host, while up to 10 Mbits/sec are supported on drive interfaces.

The controller performs SCSI bus arbitration with Disconnect/Reconnect operations to permit full utilization of the bus. The protocol conforms to ANSI X3T9.2 specifications. Both standard and extended categories of SCSI commands are supported, including queued commands from the same or multiple hosts.

The WD1005-SCS supports ESDI Serial Mode operation with NRZ data transfers between the controller and drives. Both soft and hard sector formats are supported. The NRZ data is converted to WD2010 format via an adapter chip during FORMAT, READ and WRITE operations. Odd Parity is supported on ESDI command and status information transfers between host and drives.

The controller is capable of reading/writing contiguous sectors on a track with 1:1 interleave. It can also perform multiple sector reads/writes with a single command. The sector size is programmable from 256 B/s to 1024 B/s.

The 32 bit ECC is an integral part of the WD2010 controller chip that performs actual correction in the buffer.

Media defects are handled with Mode Select feature of SCSI where the user is free to determine the desired number of spare sectors on a track, as well as the number of cylinders to be used as spare tracks. While formatting the drives, the WD1005-SCS will automatically relocate bad sectors to spare locations assigned in that track. If the number of spare sectors on a track exceeds the maximum number of spare sectors in the Mode Select, the entire track is automatically relocated to the alternate starting address specified in the Mode Select.

DESIGN SPECIFICATION

ESDI WINCHESTER DISK
CONTROLLER MODULE

WD1005-WAH
SPECIFICATION NO. 96-000371

October 17, 1986

DESIGN SPECIFICATION
TABLE OF CONTENTS

2

1.0 SCOPE

This document describes the functional, electrical and logical
design characteristics of the WD1005-WAH Winchester Controller
(WDC) module. The board is used to interface two Enhanced
Small Disk Interface (ESDI) compatible fixed disk drives
to the PC-AT computer I/O Channel bus structure.

The fixed disk section includes the WD5010 Winchester Disk
Controller, the WD5020 ESDI Adapter Device, the WD1015 Control
Processor, a WD1100-14 ECC Generator/Checker, the WD1014 Logic
Support Device, RAM sector buffer memory and associated control
logic.

Portions of the WD1015 control processor protocol specification
(firmware) are included as a part of this document as is a
description of the module self-test operation. Software which
resides in the PC processor (either test or operational) is not
included as a part of this document.

2.0 APPLICABLE DOCUMENTS

2.1 WD1005-WAH BOARD DOCUMENTS

        61-000158 P/L & Assembly
        60-000123 PWB Fabrication
        65-000146 Artwork, PCB
        96-000370 Test Specification
        68-000159 Schematic Diagram

2.2 COMPONENT DOCUMENTS

        96-000313   WD5010 Winchester Disk Controller
        96-000314   WD5020 ESDI Adapter Device
        75-000181   WD1015-PL23 Control Processor Spec.
        96-000126   WD1100-14 ECC Generator/Checker
        29-000029-0005   WD1014 Logic Support Device
        75-000182   WD1015-PL23 Firmware Listing
        75-000205   PAL Specification, PAL1

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75-000180	PAL Specification, PAL2
75-000208	PAL Specification, PAL3
75-000203	PAL Specification, PAL4
75-000221	PAL Specification, PAL5
75-000204	PAL Specification, PAL6

2.3 REFERENCE DOCUMENTS

IBM PC/AT Technical reference

3.0 DESIGN OVERVIEW

3.1 HARDWARE OVERVIEW

The WD1005-WAH Winchester Disk Controller (WDC) is a PC-AT bus compatible printed-circuit module that interfaces up to two ESDI type fixed disk drives to the system processor. The module fixed disk control section includes the WD5010, WD5020, WD1014 and WD1015 Winchester disk control components, a WD1100-14 ECC Generator/Checker and two 2048x8 RAMS for sector data buffering.

Figure 3-1 is a simplified block diagram of the module fixed section and each major block is briefly described below. The module logic is fully described in the referenced documents or in subsequent sections of this specification.

3.1.1 WD5010 WINCHESTER DISK CONTROLLER

The WD5010 Winchester Disk Controller (WDC) is an advanced design VLSI device that provides the fixed disk drive(s) primary data and control interface and sector data buffer control logic. The major features of the device include:

* Multiple sector read/write commands
* Data transfer rate up to 10 megabits/second
* Programmable format and error recovery algorithms

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3.1.2 WD5020 ESDI ADAPTER DEVICE

The WD5020 is a companion device to the WD5010 that allows control of ESDI compatible drives in either soft-sectored or hard-sectored formats (note: the WDC only supports hard-sectored format). The device converts the WD5010 data and control format to the format required by ESDI drives. The chip also includes the ESDI command and status serial mode interface.

3.1.3 WD1015 BUFFER MANAGER CONTROL PROCESSOR

The WD1015 Control Processor (CP) is an eight-bit microprocessor (type 8049H) that operates with the WD5010, WD5020 and the module support logic to aid in processing the disk commands, to help in error recovery procedures and to perform module diagnostics. The processor chip includes internal data RAM and program ROM memory.

3.1.4 WD1100-14 ECC GENERATOR/CHECKER

Data error detection and correction is provided by the WD1100-14 ECC polynomial generator/checker. The device is designed to generate 7 check/syndrome bytes (56 bits) for the error detection and correction process.

3.1.5 RAM DATA BUFFER

A static RAM on-board memory buffers the sector data and provides the word/byte data format conversion between the drives and the PC-AT system bus. The buffer allows the system processor to access the sector data without timing restrictions.

3.1.6 WD1014 LOGIC SUPPORT DEVICE

Module logic simplification and power reduction is provided by The WD1014 support device which replaces several SSI/MSI components. The internal device logic includes the module command and error registers, the drive and head select registers, address decoding gates and several control functions.

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3.1.7 SYSTEM BUS INTERFACE

The WDC interfaces to the system bus address, data and I/O con-
trol signals. All fixed disk read/write data transfers are 16
bits wide and occur between the bus and the sector data buffer
memory. Control and status transfers are 8 bits wide and use the
lower data byte (SD07-00) only. The WDC module register address
map is fixed (at a primary or secondary range) as are the bus in-
terrupt requests and the DMA channel assignment.

3.1.8 WINCHESTER DRIVE INTERFACE

The WDC interfaces to the fixed disk drives via one 34-pin con-
trol cable and two 20-pin data cables in conformance with stand-
ard ESDI signal definitions.

```
<-----+------------------------------->    SYSTEM ADDRESS BUS
<-----|---------------------------+----->    SYSTEM DATA BUS (15-08)
<-----|-----------------------+---|----->    SYSTEM DATA BUS (07-00)
<-----|-------------------+---|---|----->    SYSTEM CONTROL BUS
      |                 -     |   |   |
+------------+           +------------+           +------------+
|  ADDRESS   |           | BUS BUFFER |           |  SECTOR    |
|  DECODING  |<-+->|     | GATES AND  |<-+->|     |  BUFFER    |
|  GATES     |  |  |     |  WD1014    |  |  |     |  MEMORY    |
+------------+  |  |     +------------+  |  |     +------------+
               |  |           |         |  |          |    LOCAL (HD)
<-----+--------|---------+---------|--------+->  DATA BUS
      |        |         |         |        |
+------------+ |  +------------+ |  +------------+
|            | |  |            | |  |            |
|  WD1015    |<-+->|  WD5010    |<-+->|  WD5020    |
|            | |  |            | |  |            |
+------------+ |  +------------+ |  +------------+
     |    |    |    |       |   |   |
   +-------------+      +-------------+
   |             |      |    ESDI     |
   |  WD1100-14  |      |    DRIVE    |
   |             |      |  INTERFACE  |
   +-------------+      +-------------+
      FIGURE 3-1         <----|---+----> CONTROL BUS
   WDC BLOCK DIAGRAM     <----+--------> DATA BUS (2)
```

7
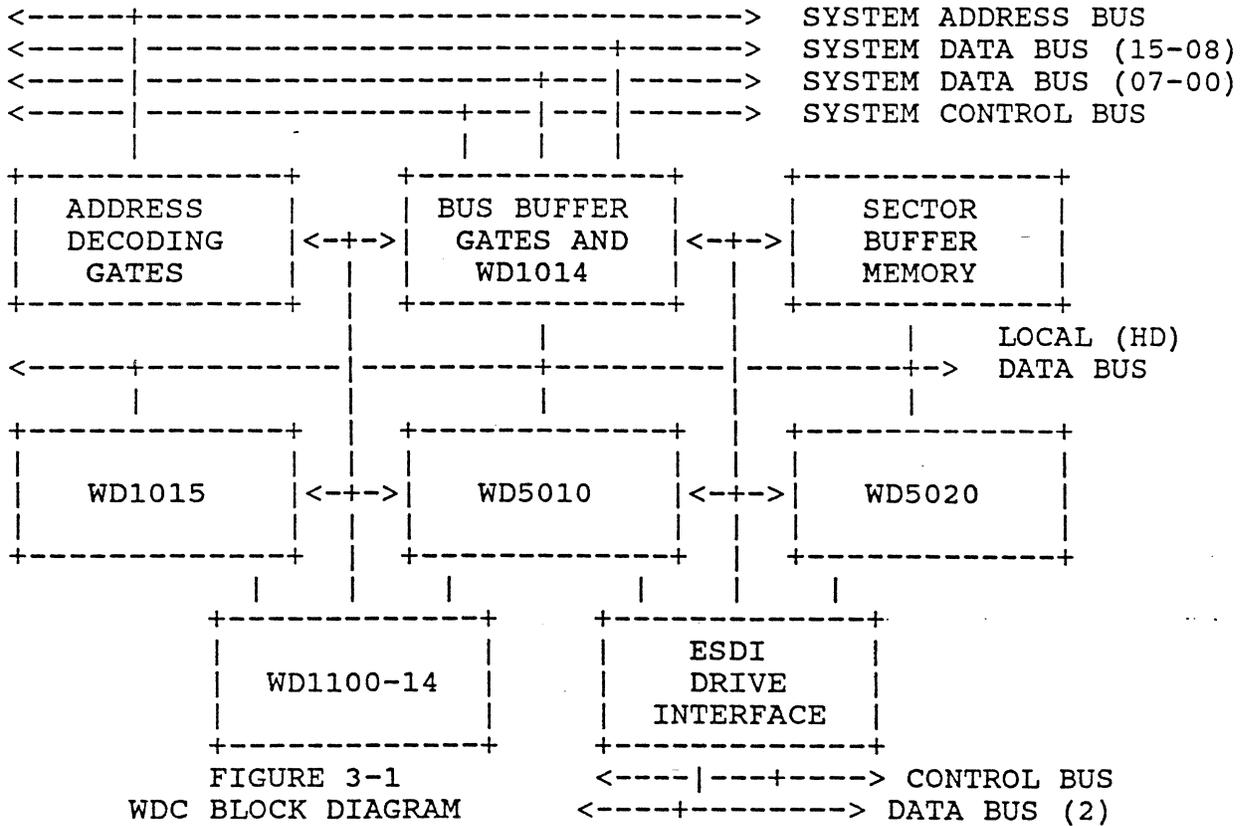
3.2 SOFTWARE OVERVIEW

All control and data transfers between the system processor and
the WDC fixed disk control section use system programmed I/O.
The module address range is fixed (at either of two ranges) as
are the controller priority interrupt levels and the DMA channel
assignment. The module address map and register definitions are
given in Section 5.0 of this document.

3.2.1 FIXED DISK SECTION

3.2.1.1 Command Control Flow

The Winchester controller commands and status descriptors are
well documented in the referenced specifications; however, it is
very important to understand the relation between the system
host, the WD5010/WD5020 devices, the WD1015 and the module sup-
port registers. A typical command sequence is given below to
help illustrate this relationship.

  * In the idle state, the WD5010/20 drive control signals are
    off, the controller status indicates ready, drive status
    is valid, the WDC interrupt is enabled (but not asserted)
    and the WD1015 is in idle, monitoring it's wakeup signal
    input.

  * The system processor outputs the command parameters to the
    WD5010 task file and outputs the operation command (seek,
    read, write) and the command attributes (long mode, retry
    control, etc.). For write operations the system processor
    also outputs the sector or format data.

  * The command output is intercepted by the WD1014 and is
    registered in the device command register (although to the
    system processor it appeared that the command was received
    by the WD5010).

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* A read command output sets the WD1014 wakeup latch which causes the controller status to indicate busy and the WD1015 wakeup signal to be asserted. Write and Format commands set the data request status signal (DRQ) to initiate the host data transfer. Completion of the data transfer (512 or 519 bytes) then sets the WD1015 wakeup signal and busy status.

* The WD1015 then examines the command, verifies command parameters and passes the command to the WD5010/WD5020 for execution.

* The WD5010/20 executes the command providing drive positioning, data transfer control, error monitoring and completion status. Drive read/write data NRZ formatting and clocking is provided by the WD5010/20 devices for commands that require data transfers.

* On command completion, the WD5010 interrupts the WD1015 which again examines the command, status, etc. for any additional command requirements and, if complete, sets the controller status to indicate "not busy" and interrupts the system processor.

* The controller has returned to idle and the host may examine drive and controller status, read input data, etc. as required to complete the operation.

3.2.1.2 Standard Commands

The WD5010 allows execution of the standard commands described in
the WD5010 specification and listed below - refer to Section 5.0
for the WD1005-WAH-WAH command descriptions.

>   Restore, Seek, Read Sector, Write Sector, Scan ID, Write
>   Format, Compute (ECC) Correction and Set (ECC and Drive)
>   Parameters.

Of these, the Scan ID, Compute Correction and Set (ECC/Drive)
Parameters commands are not directly available to the system
processor   (although   they   may   be   executed   by the WD1015
transparently to the host processor).

3.2.1.3 Non-Standard Commands

Fixed disk commands to the WDC are intercepted by the WD1015
(with the aid of the WD1014 logic) and thus commands not
specified in the WD5010 command list may be defined.

>   * SET PARAMETERS - This command transfers the maximum number
>   of sectors per track (HDSCT) and # of heads (HDSDH) to the
>   controller before any multi-sector transfer operations. It
>   is the responsibility of the host not to attempt a multi-
>   sector operation beyond the limits of the file. An inter-
>   rupt is generated at completion of this command and the
>   following information is made available to the host :
>   # heads .... HDSDH register
>   # sectors/track ... HDSCT register
>
>   * Read Verify - This command is very much like the READ com-
>   and except that no data is transferred to the host. This
>   allows the system to verify the data integrity of the
>   file. An interrupt is generated at the completion of the
>   command or if an error occurs.

* Write Verify - Command used the same as the normal write command except that the controller verifies the write data integrity using the ECC check (essentially performing a write followed by a read verify). Multi-sector operation is allowed with the verify function performed on all sectors following the write. Errors encountered during the verify function are reported using the same procedures as a read or read verify command.

* Diagnostic Command - The diagnostic command causes the WD1015 to execute an on-board diagnostic program and to report the test results (at the WD5010 Error Register Address).

* Write Data Stack - Diagnostic command used to allow the host to write data to the sector buffer without executing a actual disk write command.

* Read Data Stack - Diagnostic command used with the above write data stack command allowing the host to read the sector data buffer without executing a disk read operation. Neither the read or write data stack commands generate an interrupt on command completion.

* Initiate ESDI Command - Command used to allow the system processor to directly send instructions to the selected drive by loading the WD5020 transfer data registers (2) and executing the initiate command. The controller serializes the data, adds the required parity bit and transmits the instruction to the drive. The drive completes the instruction and transmits completion status to the controller. The host is interrupted and may read the WD5020 data registers to complete the command. See referenced ESDI documents for drive instructions and completion status responses.

3.2.1.4 Multi-sector Commands

Multiple sector read, write and verify commands of up to 256 sec-
tors are allowed without restriction on track or cylinder
boundaries. Non-recoverable control errors (drive not ready,
write fault, etc.) or non-correctable read data errors will ter-
minate a multi-sector command and the controller expects a new
command to continue operation. Corrected read data errors do not
terminate the commmand and the controller expects a normal data
transfer restart and continuation. The drive parameters are
checked during the execution of this command.

3.2.1.5 Diagnostic Command

The controller on-board diagnostic is executed on command and
verifies the WD1015 firmware and local storage, the sector data
buffer storage and the WD1015 to WD5010, WD5020, WD1014 and
WD1100-14 data paths. Results are encoded and are available to
the system processor via the controller error register - refer to
Section 8.0.

4.0 HARDWARE INTERFACE

This section provides detailed hardware interface information for
the WDC and includes a signal definition of the external signals
used by the module. The signals are also listed in the Appendix
along with their connector pin assignments. Further information
on each signal is provided in the referenced literature.

4.1 SYSTEM BUS INTERFACE

The PC-AT I/O channel signals used by the WDC are noted below
and require both the P1 and P2 system bus connectors.

      SA15-SA00
      System Address bus - Inputs used to select the WDC module
      bus I/O addresses. The module decodes the address input
      terms to select the WD5010/20 task file registers, the
      module control/diagnostic registers, the sector data buffer
      memory and to enable the system bus buffer gates.

SD15-SD00
System Data bus - Bi-directional signals used to transfer
16-bit fixed disk data and 8-bit module control and status
information.

AEN
Address Enable - Input control signal that indicates a valid
I/O address is on the system bus. The address decode logic
uses this term to qualify the I/O address decoding.

BALE
Bus Address Latch Enable - Input control signal used to in-
itiate a system bus data transfer. The WDC module uses this
input to generate the system bus fast I/O transfer control
signal.

-IOCS16
I/O Control Signal 16 - Output signal used to indicate th'
fast 16-bit data transfer mode. The WDC asserts this sig-
nal for all hard disk data transfers.

IRQ14
Interrupt Request Level 14 - Fixed disk control section out
put interrupt level to the processor requesting a data
block transfer or indicating command completion. The
level clears on a subsequent fixed disk command to the
WDC, a system reset, or a read to the HDSTT register.

-IOR
I/O Read - Input read control strobe asserted by the
system processor during bus read transactions.   The WDC
uses the signal (along with the system address bus
decoding) to enable system I/O reads of both data and
status information.

-IOW
I/O Write - Output control strobe asserted by the system
processor during bus write cycles. The WDC uses this
strobe and the decoded bus address to input both data and
command information.

RESET
Reset - Input module reset used to initialize the
WD5010/20, WD1015 and clear the interrupt levels and
to halt drive operation. When reset clears, the WD1015
will automatically execute on-board diagnostic tests and
load the test result status in the fixed disk error
register. No interrupt is issued after the completion
of the diagnostics. The host monitors the BSY bit of the
HDSTT register to check for on-board diagnostic comple-
tion. The BSY bit of the HDSTT   register
will be activated within 1 ms of any RESET pulse. It
will be kept active until the self-test diagnostics are
completed. The active state of the BSY bit will be at
least 1 ms and no more than 1.4 seconds.

4.2 FIXED DISK DRIVE INTERFACE

The Winchester drive control and data (ESDI) interface is in-
cluded here for document completeness.

4.2.1 CONTROL CABLE

DS1-/DS2-
Drive Select - Primary output control signal used to con-
nect a drive interface to the control signals. The
WDC is limited to drive 1 or 2. The signals are negated
by a system master or power-on reset. Drive 1 will be
selected when bit DS1 of the HDSDH register is zero, and
drive 2 will be selected when bit DS1 is a one.

HS3-/0-
Head Select - Binary-coded output head select signals al-
lowing drives with up to sixteen R/W heads to be at-
tached to the controller.

WG-
Write Gate - Write enable output control level to
the selected drive. The signal is negated by a write fault
condition in the drive or by a controller master, power-on
or programmed reset.

RG-
Read Gate - Drive read enable signal to the selected
drive to control the drive VCO and data recovery circuits.

CMD-
Command Data - Sixteen bit serial data (plus parity) to
the selected drive. Data contains instructions for drive
internal execution (recalibrate, seek, request status,
etc.). The data is transferred using a drive/controller
handshake protocol (XREQ- and XACK-).

XREQ-
Transfer Request - Control signal to the selected drive
asserted when each bit of the command data information is
to be transferred to the drive or when the
configuration/status data is to be returned from the
drive. The signal clears when the selected drive asserts
transfer acknowledge (XACK-) to the controller.

XACK-
Transfer   Acknowledge   - The selected drives hand-
shake response to the controller transfer request.   The
drive either   accepts command data or returns
configuration/status information.   Additional signal
descriptions and timing in formation are available in the
referenced documentation.

CSD-
Configuration/Status   Data - Response data from the
selected drive initiated by the controller   command   or
instruction.   The   response   is   16   bits   plus   parity
and indicates the completion status from the command   or
drive   configuration   data   (see   ESDI   drive
documentation).   The information is transferred using the
transfer request/acknowledge protocol.

INDEX-
Index - Positioning signal from the drive that   occurs
once per drive revolution   and   used by the WD5010 and
WD5020 for command timeout and track formatting.

RDY-
Drive Ready - Control signal from the drive   indicating
the drive is ready and that the I/O control signals are
valid.

ATN-
Attention   -   Control signal from the selected drive that
indicates the drive has a fault condition   or   a   change
of status.   The signal is also asserted during drive
power-on when the power up sequence is complete.

SCT-
Sector clock (or   address   mark   found)   from   the
selected drive.   The signal is used in hard sectored for-
mats to signal the beginning of each sector and in soft
sectored formats to flag detection of an address mark.   A
non-gated sector clock signal is also available on the
drive radial cable but is currently not used by the con-
troller.

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4.2.2 DATA (Radial) CABLES

NRZRD0/1(+,-)
NRZ Read Data - Differential read data input from
each drive. The data received from each drive is gated
by the drive select signals and is clocked into the WD5020
for conversion to the WD5010 input.

NRZWD0/1(+,-)
NRZ Write Data - Differential signal to each drive
that defines the data to be written on each track. The
write data is clocked by the drive write clock signal.

RFCLK0/1(+,-)
Read/Reference Clock from the drive used to determine
the drive data transfer rate (10 Mbits/sec.). The read
clock is derived from the drive data recovery circuits and
is supplied during the read data transfer. The drive
reference clock is furnished at all other times.

WTCLK0/1(+,-)
Write Data Clock output to the selected drive and used
to time the write data transitions. The clock is derived
from the reference clock signal.

DSEL0-/1-
Drive Selected - Control signal from (each) drive indicat-
ing that the drive is selected, is present in the sys-
tem and that the drive control and data cables are in-
stalled.

CMDCPL0-/1-
Command Complete - Status signal from each drive that is
asserted when the drive completes any command. The
signal will go false when the first bit of the command
data is received by the drive.

SCLK0-/1-
Sector Clock - Non-gated sector clock and address mark
found signal.

AME0-/1-
Address Mark Enable - Control output to each drive
used to cause address marks to be written (WG- asserted)
or to request drive address mark search (WG- and RG-
inactive).

NOTE: The ESDI 'drive select 3' control line is
not implemented; thus, attached drives must be con-
figured as drive unit 1 or 2 only.

4.3 INDICATORS

LED+/-
LED Indicator(s) - External indicator signals used
to provide visual indication of WDC fixed disk activity.

5.0 SOFTWARE INTERFACE

5.1 REGISTER ADDRESS MAP

The WDC system I/O port address map is summarized in Figure 5-1
and includes the WD5010 and WD5020 task file area and the module
auxiliary support registers. The primary address is listed first
with the secondary address shown within parenthesis (see Section
7.0 for address selection jumper installation).

```
+-------------------------------------------------------------------+
|                            TASK FILES                             |
+-------------------------------------------------------------------+
| ADDRESS (HEX)| REGISTER |              FUNCTION                   |
|--------------|----------|-----------------------------------------|
| 1F0 (170) RW |  HDDTR   | Hard Disk Data Register (16 bits)       |
| 1F1 (171) WO |  HDWPC   | Not used(no effect if written into)     |
| 1F1 (171) RO |  HDERR   | Error Register                          |
| 1F2 (172) RW |  HDSCT   | Sector Count                            |
| 1F3 (173) RW |  HDSSN   | Starting Sector Number                  |
| 1F4 (174) RW |  HDCLL   | Cylinder Number - Low Byte              |
| 1F5 (175) RW |  HDCLH   | Cylinder Number - High Byte             |
| 1F6 (176) RW |  HDSDH   | Sector Size, Drive/Head Select          |
| 1F7 (177) WO |  HDCMD   | Command Register                        |
| 1F7 (177) RO |  HDSTT   | Status Register                         |
| 3F6 (376) WO |  HDFDR   | Fixed Disk (Control) Register           |
| 3F6 (376) RO |  HDASR   | Alternate Status Register               |
| 3F7 (377) RO |  HDDIR   | Digital Input Register                  |
+-------------------------------------------------------------------+
|                        WD5020 REGISTERS                           |
|-------------------------------------------------------------------|
| 1F8 (178) RW |  HDDTL   | HD Command/Status Data - Low Byte       |
| 1F9 (179) RW |  HDDTH   | HD Command/Status Data - High Byte      |
| 1FA (17A) RW |  HDPLO   | PLO Length                              |
| 1FB (17B) RW |  HDGPL   | Gap Length                              |
| 1FE (17E) RW |  HDDRV   | Drive Number (not used)                 |
| 1FF (17F) WO |  ESCMD   | ESDI Adapter Command                    |
| 1FF (17F) RO |  ESSTE   | ESDI Adapter Status/Error               |
+-------------------------------------------------------------------+
```

FIGURE 5-1
REGISTER ADDRESS MAP

5.2 WD5010 WINCHESTER DISK CONTROLLER

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5.2.1 WD5010 TASK FILE REGISTERS

Figure 5-2 summarizes the WD5010 task file registers (addresses 1F1/171 through 1F7/177) and their bit assignments with respect to the system processor lower byte bus terms (SD07-00). Register address 1F0/170 is the 16-bit sector data buffer and all read/write accesses to this fixed address selects the buffer memory. Certain register descriptions shown in Figure 5-2 differ slightly from the standard descriptions contained in the referenced WD5010 documentation. In particular, the HDSDH register forces the ECC option mode and 512 bytes per sector and the HDWPC register is always set to FF Hex by the 1015 to disable write precompensation. Where differences exist, the values shown in Figure 5-2 should take precedence.

REGISTER	7	6	5	4	3	2	1	0
HDWPC	1	1	1	1	1	1	1	1
HDERR	BBD	ECC	0	INF	0	ACD	TK0	DNF
HDSCT	NUMBER OF SECTORS							
HDSSN	STARTING SECTOR NUMBER							
HDCLL	CYLINDER NUMBER LSB							
HDCLH	0	0	0	0	0	CYL NUMBER MSB		
HDSDH	1	0	1	DS1	HS3	HS2	HS1	HS0
HDCMD	COMMAND							
HDSTT	BSY	RDY	WTF	SKC	DRQ	CRD	IDX	ERR

FIGURE 5-2
WD5010 TASK FILE REGISTERS

5.2.2 WD5010 COMMAND DESCRIPTION

The task file command register (HDCMD) accepts the commands and
command attributes as shown in Figure 5-3.   Commands will be ig-
nored when WDC is busy. If the drive is not ready or SEEK COM-
PLETE is false or if a fault condition exists at the drive, then
an aborted command results.   Undefined command codes will ter-
minate with the "aborted command" error.

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	X	X	X	X
SEEK	0	1	1	1	X	X	X	X
RD SECTOR	0	0	1	0	0	0	LNG	RTY
WRT SECTOR	0	0	1	1	0	0	LNG	RTY
FMAT TRACK	0	1	0	1	0	0	0	0
RD VERIFY	0	1	0	0	0	0	0	RTY
WT VERIFY	0	0	1	1	1	1	0	0
INIT ESDI	1	1	1	0	0	0	0	0
DIAGNOSE	1	0	0	1	0	0	0	0
WT STACK	1	1	1	0	1	0	0	0
RD STACK	1	1	1	0	0	1	0	0
SET PARAM	1	0	0	1	0	0	0	1
READ PARAM	1	1	1	0	1	1	0	0

FIGURE 5-3
WD5010 COMMAND SUMMARY

where: LNG = 0 = Normal mode, normal ECC functions are
                    performed.
              = 1 = Long mode, the module is inhibited from gen-
                    erating or checking the seven ECC bytes. The
                    module will append the seven additional bytes
                    supplied by the drive (read) or system
                    processor (write) to the normal data field.
          RTY = 0 = Error retries and ECC correction are enabled.
              = 1 = Retries and ECC correction are disabled.

5.2.2.1 Command Definition

The following provides a brief overview of each command.   Additional information is contained in the WDC firmware description and in the WD5010 specification.

    RESTORE
    The selected ESDI drive is sent a seek to cylinder 0 command via the serial command transfer interface.   The drive heads seek to cylinder 0000 and any track offsets are cleared.   The command will abort with the ERR bit set in the status register and the aborted command (ACD) bit set in the error register if the drive cannot accept the command or if the WD5020 indicates a transfer protocol or transfer parity error.   An interrupt is generated at the end of the command.

    SEEK
    The seek command positions the drive heads over the cylinder specified in the task file cylinder select registers (HDCLH/L) and any track offsets are cleared.   The command will abort under the conditions noted for the restore command above. Bit SKC of the HDSTT register goes true upon the completion of the seek portion of any command involving a seek operation. This includes the SEEK as well as all other related commands. The fixed disk priority interrupt (IRQ14) is generated after a successful ESDI seek command transfer. The host can check for completion of the seek operation by selecting the drive and checking bit SKC of HDSTT.

    READ SECTOR
    A number of sectors (1-256) are read from the selected disk.   If the drive is not positioned at the specified cylinder an implied seek will occur.   Drive furnished ECC check bits will be used if the read long mode is specified. Single burst data errors (up to 12 bits) will be corrected if retries are enabled and the long mode is not selected.   Uncorrectable errors will not inhibit the (error sector) data transfer to the on-card buffer, however multi-sector transfers will be terminated. The WDC interrupt will occur as each sector is ready for system input. No interrupt is generated at the end of this command if successful. During multisector operation, bit BSY of HDSTT is

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on until a sector of data is available for the host to transfer.
At this time, BSY is turned off, IRQ14 occurs, and DRQ is
turned on. After the sector is read by the host, DRQ is turned
off and BSY is turned on for the operation on the following sec-
tor. Sector interleaving of 3:1 is supported under the condition
that the host responds to the interrupt and transfers the sec-
tor data within 500us after IRQ14 occurs.

WRITE SECTOR
     A number of sectors (1-256) are written to the selected disk
with an implied seek occurring if required.   Multiple sector
write (and read) operations may cross track and cylinder
boundaries. System processor supplied ECC bytes will be appended
to the data field in the write long mode.   An interrupt is gen-
erated as the data for each sector is required (except the first
and at the end of the command).   The first data buffer is output
by the system processor after the command has been issued and the
data request status bit is on. During multisector operation, bit
DRQ is turned on, IRQ14 occurs, and the sector data is transfered
by the host. After the transfer, bit DRQ is turned off and bit
BSY is turned on until the data has been transferred to the File.
After the data has been transferred to the File, IRQ14 occurs,
BSY is turned off and DRQ is turned on to initiate the host to
transfer the next sector data to the on-card buffer.

FORMAT TRACK
     The track specified by the task file is formatted with
identification, data and check fields in accordance with the in-
terleave table transferred to the sector buffer. The interleave
table is composed of 2 bytes per sector, with the first byte
being 0 for a good sector or 80h for a bad sector and the second
byte designating the logical sector number. The sectors per track
is specified in the HDSCT Register. Command completion will
leave the data field initialized to zeros. The 7 ECC bytes will
also be appended after the data field. The completion interrupt
is generated as each track is formatted.   The WD1005-WAH
controller forces 512 bytes/sector, and the hard sectored drive
format.

READ VERIFY
     The read verify command functions similar to a normal read
command except that no data is transferred to the Host.   The ECC
bytes are checked for data verification.   Multiple sector opera-
tion is supported. Error retry control is supported.

WRITE VERIFY
     Write verify functions like a normal write operation fol-
lowed by a read verify instruction.   Any unrecoverable error
will terminate the command with the appropriate status. Multiple
sector operation is supported. For multisector operations,   all
sectors are writtern before the read verify operation.   Error
retries cannot be enabled for this command.   Neither verify
command (of course) will allow the long operational mode.

INITIALIZE ESDI

Command used to allow the host to instruct a selected drive by
direct command communication with the WD5020. The host must load
the WD5020 transfer data registers (high and low data bytes)
prior to issuing the the command.   The controller serializes the
data, adds parity and   sends the command to the drive. The
drive executes the command and returns status to the transfer
data registers for host interpretation.

DIAGNOSE

This command instructs the attachment card to perform a self test
and internal device initialization. An interrupt is generated at
completion of the command. The following table shows the error
codes and the order of execution :

05 = WD1015 Device Error
04 = WD1014/1100-14 Device Error
03 = Sector Buffer Error
02 = WD5010/5020 Device Error.
01 = No Error

If any test fails, the remaining tests are NOT performed. All
device tests verify that their internal registers may be accessed
correctly. The WD1100 ECC device test also verifies that the
"preset" and "syndrome" control inputs function correctly. The
Sector buffer test verifies that the address generator, overflow
counter and data retention are functional. The WD1015 test per-
forms a ROM checksum to insure firmware integrity and an internal
RAM data retention test.

No system bus, host interactive or drive diagnostics are
performed. WD1015 is reset (either a power up reset or a
software reset, i.e. a pulse to the RST bit of register HDFDR),
a RECAL command is issued to the file(s) (if the drive(s)
is/are present) to recover from a posssible previous seek
fault condition. No spindle control is implemented by the
WD1015, therefore the drive is assumed to come up to speed at
power on. Refer to Section 8.0 for a test description.

WRITE DATA STACK
Host diagnostic command used to verify the system bus to control-
ler data path and control logic. The data sector buffer must be
filled with 512 data bytes. The data is not examined by the
WD1015 control processor for correct information. The controller
will request data using the normal data request status bit. Com-
mand completion will not generate a completion interrupt. A
fixed disk drive does not need to be present for command
execution.

READ DATA STACK
Host diagnostic command used to transfer the sector data buffer
to system memory. The sector buffer data is not altered (from
any previous read or write operation). A command completion in-
terrupt is not generated nor is any drive activity required.

SET PARAMETERS
When this command is issued, the adapter reads the HDSDH and the
HDSCT registers for drive parameters and uses these parameters
for mutisectors transfer operations(see table below). It is the
responsibility of the host not to attempt a multi-sector opera-
tion beyond the limits of the file. An interrupt is generated at
completion of this command.

```
# heads ........... HDSDH register
# sectors/track ... HDSCT register
```

READ PARAMETERS

MS-DOS assumes that a hard disk has 17 sectors per track (SPT). This reflects the ST-506 type drives. However, the ESDI drives support 34 to 36 SPT. In order to utilize the maximum storage capacity of the ESDI drives, the WD1005-WAH controller translates a PHYSICAL track into 2 LOGICAL tracks.

The WD1005-WAH utilizes the PHYSICAL track in the following manner:

| 0 | sectors 1 - 17 | sectors 18 - 34 | 35 |

Sectors 0 and 35 are optional alternate sectors which are NOT accessed by DOS. Sectors 1-17 represent a logical track, i.e. Logical Head 0, and sectors 18-34 represent another logical track, i.e. Logical Head 1.

As you can see, the Logical drive parameters will show twice the number of actual Physical heads:

PHYSICAL PARAMETERS   LOGICAL PARAMETERS

```
    1024 cylinders                        1024 cylinders
       8 heads                              16 heads
      34 SPT                                17 SPT
```

It is important to note that low-level formats must be accomplished with PHYSICAL parameters, 34-36 SPT. If a format for 17 SPT is attempted, only the data fields will be initialized.

The MS-DOS mode (translation) is invoked by issuing a Set Parameters command (91 hex) with the sector count register set at 17, which is performed by the DOS Bios at "boot" time. This option may be disabled if jumper W2 is installed. Other operating systems may wish to utilize the ESDI drives in a pure PHYSICAL manner.

5.2.3 RETRY ALGORITHM

5.2.3.1 DATA OPERATIONS:

The EDSI drive allows both track and data strobe offsets to
facilitate disk operations in the event of read errors due to
slight head mispositions. This may eliminate the need to invoke
data error correction.

The algorithm for data error correction employed by Western Digi-
tal is to reread up to 8 times and achieve 2 matching sets of
syndromes before any correction attempt.

Combining the two methods yields the following algorithm which is
currently implemented :

Below is a table showing the maximum number of READ retries per-
formed for IDNF errors:

```
                                          F/W  x  5010  =  TOTAL
                                          -----------------------
initially, no offsets ----------------->  8    x   2    =   16
track offsets +1, data strobe offset 0->  8    x   2    =   16
track offsets -1, data strobe offset 0->  8    x   2    =   16
track offsets 0, data strobe offset +1->  8    x   2    =   16
track offsets 0, data strobe offset -1->  8    x   2    =   16
recal, reseek, no offsets------------->   1    x   2    =    2
                                                          -----
                                total IDNF retries -->     82
```

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Below is a table showing the maximum number of READ retries per-
formed for ECC errors:

	F/W	x	5010	=	TOTAL
initially, no offsets ------------------>	8	x	1	=	8
track offsets +1, data strobe offset 0 ->	8	x	1	=	8
track offsets -1, data strobe offset 0 ->	8	x	1	=	8
track offsets 0, data strobe offset +1 ->	8	x	1	=	8
track offsets 0, data strobe offset -1 ->	8	x	1	=	8
reference read to obtain syndromes ----->	1	x	1	=	1
re-read to obtain matching syndromes --->	8	x	1	=	8

                                    total ECC retries --> 49

Below is a table showing the maximum number of WRITE retries per-
formed by the different revision levels for IDNF errors:

REV. 0

	F/W	x	5010	=	TOTAL
initially, no offsets ---------------->	1	x	20	=	20
recal, reseek, no offsets ------------>	1	x	20	=	20

                            total IDNF retries ----> 40

NOTE:
      If any read, at any time, has NO ECC error, then the data is
      assumed to be correct and the operation will continue
      normally.

5.2.3.2 COMMAND TRANSFERS TO FILE:

      Errors in the transfer of data to and from the File during
      ESDI command operations are reported as aborted command er-
      rors after retries are attempted.   The ESDI Informational
      Bulletin - Recommended ESDI Interface Initialization and Er-
      ror Recording Procedures is supported with the exception
      of motor spindle control.

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5.3 WD5020 ESDI ADAPTER DEVICE

5.3.1 WD5020 TASK FILE REGISTERS

Figure 5-4 illustrates the WD5020 task file registers (addresses
1F8/178 through 1FF/17F). For normal controller operation these
registers are accessed only by the WD1015 on-board processor and
are not used by the system processor; however, the controller
design does not prevent system access if the host interface
software/firmware permits (refer to the Initialize ESDI command,
for example).

```
+------------------------------------------------------------------+
| REGISTER |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
|------------------------------------------------------------------|
|  HDDTL   |        COMMAND/STATUS XFER DATA - LOW BYTE            |
|------------------------------------------------------------------|
|  HDDTH   |        COMMAND/STATUS XFER DATA - HIGH BYTE           |
|------------------------------------------------------------------|
|  HDPLO   |  0  |  0  |          PLO LENGTH                       |
|------------------------------------------------------------------|
|  HDGPL   |  0  |  0  |  0  |          GAP LENGTH                 |
|------------------------------------------------------------------|
|  HDDRV   |                    NOT USED                          |
|------------------------------------------------------------------|
|  ESCMD   |                WD5020 COMMAND                        |
|------------------------------------------------------------------|
|  ESSTE   | BSY | ATN | INT | ACK | SCC |MODE | XER | PER |
+------------------------------------------------------------------+
```

FIGURE 5-4
WD5020 TASK FILE REGISTERS

5.3.2 WD5020 COMMAND DESCRIPTION

The WD5020 command register (ESCMD) normally accepts commands
from the WD1015 processor. For normal controller operation these
registers are accessed only by the WD1015 on-board processor and
are not used by the system processor. However, if W1 is jumpered
the host may access these registers. Command execution begins
immediately and subsequent WD5020 register accesses or commands
(except abort) are ignored until the command completes. Figure

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5-5 shows the command byte bit assignments. Figure 5-6 il-
lustrates the drive command confguration (data transfer register
16-bit information) - see referenced drive documentation for a
more detailed description of the command and the response status.
A watchdog timer prevents "Lockups" if the drive fails to respond
within approximately 700 msec.

```
+-----------------------------------------------------------------+
| COMMAND   | 7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|-----------------------------------------------------------------|
| XFER CMD  | 0 |  0 |  0 |  0 |  0 |  0 |  0 |  0 |
|-----------------------------------------------------------------|
| XFER CSD  | 0 |  0 |  1 |  0 |  0 |  0 |  0 |  0 |
|-----------------------------------------------------------------|
| ABORT     | 0 |  1 |  1 |  0 |  0 |  0 |  0 |  0 |
|-----------------------------------------------------------------|
| SET PRAM  | 0 |  1 |  0 |  0 |  0 |  0 |  1 |  0 |
+-----------------------------------------------------------------+
```

FIGURE 5-5 WD5020 COMMAND SUMMARY

```
+-----------------------------------------------------------------+
| COMMAND FUNCTION |    HDDTH    |    HDDTL    |      NOTE         |
|-----------------------------------------------------------------|
| SEEK             | 0000 0CCC | CCCC CCCC | C = CYLINDER     |
|-----------------------------------------------------------------|
| RECALIBRATE      | 0001 0000 | 0000 0000 |                  |
|-----------------------------------------------------------------|
| REQUEST STATUS   | 0010 0000 | 0000 0000 | STD STATUS       |
|-----------------------------------------------------------------|
| REQUEST CONFIG   | 0011 RRRR | 0000 0000 | R = REQUEST #    |
|-----------------------------------------------------------------|
| CONTROL          | 0101 00XX | 0000 0000 |    ATN RST       |
|-----------------------------------------------------------------|
| DATA STB OFFSET  | 0110 0SSS | 0000 0000 | S = STB OFFSET|
|-----------------------------------------------------------------|
| TRACK OFFSET     | 0111 0TTT | 0000 0000 | T = TRK OFFSET|
+-----------------------------------------------------------------|
| DRIVE DIAGNOSTIC | 1000 0000 | 0000 0000 |                  |
+-----------------------------------------------------------------+
```

FIGURE 5-6
ESDI DRIVE INSTRUCTION SUMMARY

5.4 WD1014 CONTROL AND STATUS REGISTERS

5.4.1 HARD DISK ALTERNATE STATUS REGISTER (HDASR) 3F6/376 (RO)

This register provides fixed disk status to the system processor
- refer to Figure 5-7.
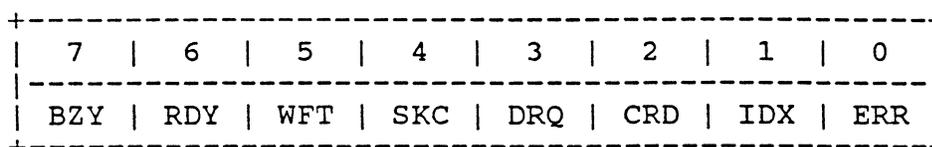
```
+------------------------------------------------------+
|  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
|------------------------------------------------------|
| BZY | RDY | WFT | SKC | DRQ | CRD | IDX | ERR |
+------------------------------------------------------+
```
                          FIGURE 5-7
                 WDC ALTERNATE STATUS REGISTER

   where:
          BZY = Controller Busy Flag
          RDY = Ready from selected drive
          WFT = Write Fault from drive status (via WD1015)
          SKC = Seek Complete from selected drive
          DRQ = Data Transfer Request Flag
          CRD = Corrected Data Flag from WD1015
          IDX = Index Pulse from selected drive
          ERR = Error Flag from WD5010 (via WD1015)

This register reflects the same status as the WD5010 status
register except for bit position 1 where the drive index signal
replaces the command in progress (CIP) flag. It should be remem-
bered that the index bit is not latched and thus follows the
drive control signal (approximately a 2.5 microsecond pulse every
16.7 milliseconds). For multi-sector read operations the
reported sector number (flagged by the corrected data status bit)
will be the 'error sector plus one'. All other error conditions
will report the 'error sector'.

The register may be interrogated by the host processor at any
time without interference with other control functions.

5.4.2 HARD DISK DIAGNOSTIC INPUT REGISTER (HDDIR) 3F7/377 (RO)

The fixed disk diagnostic input register contains the current
state of the fixed disk drive select, head select and drive
write gate signals (complimented form).

```
+-------------------------------------------------------+
|  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
|-------------------------------------------------------|
| N/A | WTG-| HS3-| HS2-| HS1-| HS0-| DS1-| DS0-|
+-------------------------------------------------------+
```
                        FIGURE 5-8
                WDC DIAGNOSTIC INPUT REGISTER
        where:
            WTG- = Write Gate on
            HS3-/0- = Drive Head Select (binary)
            DS1-/0- = Drive Select

5.4.3 HARD DISK AUXILIARY CONTROL REGISTER (HDFDR) 3F6/376 (WO)

The Hard Disk Auxiliary Control Register is used to allow
programable fixed disk reset and to provide enable/disable con-
trol of the fixed disk section interrupt.

```
+-------------------------------------------------------+
|  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
+-------------------------------------------------------+
|  0  |  0  |  0  |  0  |  0  | RST | IEN |  0  |
+-------------------------------------------------------+
```
                        FIGURE 5-9
                  WDC AUX CONTROL REGISTER
        where:
            RST = Program controlled WDC (master)reset
            IEN = WDC Data Transfer Interrupt Enable

NOTE: The software controlled reset bit (RST) will maintain the
fixed disk section logic reset as long as the bit is on. The bit
must be turned on (for a minimum of 10.0 microseconds), then off,
to complete the reset function.

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Additionally, it should be noted that the interrupt enable control bit does not clear the interrupt level in the disabled state. A pending interrupt will occur when the interrupt is again enabled. It should also be noted that a system master reset will clear the interrupt but will leave the interrupt enabled.

5.4.4 FIXED DISK DATA REGISTER

The WDC reserves system I/O address 1F0/170(H) for fixed disk programmed I/O data transfers and all system bus data transactions between the WDC and the system processor at this address use the 16-bit word transfer bus mode. All fixed disk word data is transferred between the system bus and the sector data buffer memory directly; i.e., there are no intervening registers or temporary storage elements. The buffer memory appears to the host as a 'data stack' where the access address is fixed and all transfers must be made as 256 sequentially addressed words - access of single or random addresses is not supported.

For long mode operations, the seven ECC bytes are transferred between the system bus and the WD1100-14 ECC device. All ECC information is always transferred as data bytes - word transfers are used for the sector data only. Refer to Figure 5-10 and 5-11 for a diagram of the read/write data transfer path and fixed disk data format.

```
                                                        SYSTEM
      <-----+--------------------+------>  DATA BUS
            |                    |          SD15-SD00
      +------------+       +------------+
      |   DATA     |       |   DATA     |
      | BFR GATE   |       | BFR GATE   |
      | (15-08)    |       | (07-00)    |
      +------------+       +------------+
              |                    |         BUFFERED
      <-----+----+-----+-----+----+------>  DATA BUS
            |                    |          SDB15-00
      +------------+       +------------+
      |  BUFFER    |       |   DATA     |
      |  MEMORY    |<-+    | BFR GATE   |
      | WORD DATA  |  |    | (07-00)    |
      |------------|  |    +------------+
                      |           |
      +------------+  +--------|   |
      | WD1100-14  |           |
      |   ECC      |<-----------+------>
      | BYTE DATA  |       LOCAL DATA
      +------------+       BUS HD07-00
```
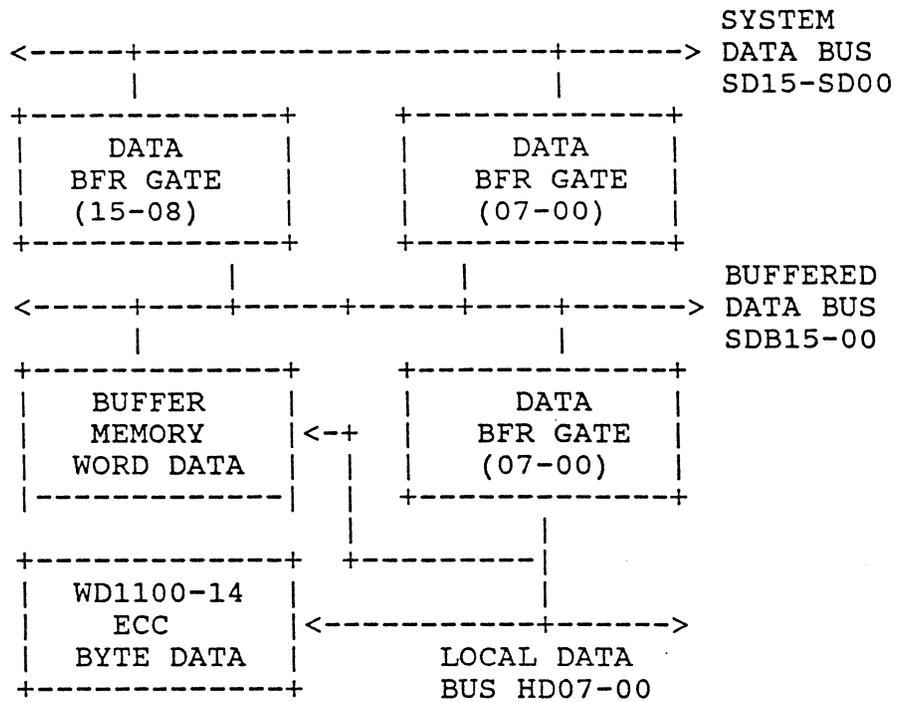
FIGURE 5-10
R/W DATA TRANSFER PATH
FIXED DISK SECTION

```
+------------------------------------------------------------------+
|ID  | WORD 000 | WORD 000 |   | WORD 255 | WORD 255 | CHECK  |
|FLDS|   LSB    |   MSB    |   |   LSB    |   MSB    | FIELDS |
+------------------------------------------------------------------+
```

FIGURE 5-11

5.5 SYSTEM INTERRUPTS

The WDC requests fixed disk read/write (block) data transfers
via a system interrupt (IRQ14). The interrupt level is set by
the WD1015 and will interrupt the system processor when the level
is enabled (bit IEN in auxiliary control register HDFDR reset)
and the WDC is not busy; i.e., not in the disk data transfer
process. The interrupt level clears on any command from the sys-
tem processor, programmed reset, hardware reset or status
register read operation.

5.7 WD1015 COMMANDS

The WD1015 communicates with the WD5010, WD5020, WD1100-14,
WD1014 and the sector data buffer via a set of R/W commands at
pre-set addresses. Commands noted by an asterisk (*) are address
and read or write strobe control only and do not require a data
phase.

ADDRESS	R/W	WD1014 CONTROL COMMANDS
D7	W	Error Register
D7	R	Command Register
D6	W	Set Multiple Mode *
D6	R	Clear Multiple Mode *
D5	W	Set Read Latch *
D4	W	Set Data Request *
D4	R	Set Fixed Disk Interrupt *
D3	R	Clear RAM Address Counter *
D3	W	Reserved
D2	W	Reserved
D2	R	Set 'Sleep' Mode *
D1	R/W	Reserved
D0	R/W	Reserved

ADDRESS	R/W	WD5010 COMMANDS
E7	W	Command Register
E7	R	Status Register
E6	R/W	SDH Register
E5	R/W	Cylinder Number - High Byte
E4	R/W	Cylinder Number - Low Byte
E3	R/W	Sector Number Register
E2	R/W	Sector Count Register
E1	W	Write Pre-compensation Cylinder
E1	R	Error Register

ADDRESS	R/W	WD5020 COMMANDS
EF	W	Command Register
EF	R	Status Error/Register
EE	R/W	Drive Number (not used)
EB	R/W	Gap Length Register
EA	R/W	PLO Length Register
E9	R/W	Data Transfer Register - High
E8	R/W	Data Transfer Register - Low

ADDRESS	R/W	WD1100-14 PPG CHIP SELECT
B0	R/W	Ecc chip select
70	R/W	CS for future use

FIGURE 5-17
CP SUPPORT
COMMANDS

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Read/write address E0 is reserved for WD1015 communication with
the sector data buffer.

5.7 WD1100-14 COMMANDS

The WD1015 control processor accesses the WD1100-14 ECC device
check bytes during the sector data error correction process. The
processor first selects the device ECC control mode by setting
the output port (2) bit position 2 true (high).   The ECC bytes
are then accessed by read or write commands (from 1 to 7) at
address 30. When the bytes have been accessed the control bit is
returned to the false (low) state.

The control processor is also required to initialize (or preset)
the WD1100-14 prior to every ECC generate or check function;
i.e., prior to every sector read or write operation.   Bit posi-
tion 1 of the output port is set, then cleared, to form the
preset control pulse.

6.0 LOGIC DESCRIPTION

This section is intended to augment the descriptions of Sections
4 and 5 with a more detailed description of the WDC logic with
reference to the WD1005-WAH schematic diagrams.   It is assumed
the reader is familiar with standard TTL components and conven-
tional logic symbols. Further, it is necessary for the reader to
be familiar with the referenced VLSI components (WD5010, WD5020,
WD1100-14, WD1015, and WD1014).

6.1 SIGNAL CHARACTERISTICS

6.1.1 Logical Notation

Positive logic notation is used throughout and all signals which
are active in the low state have the negation symbol (SIGNAL-)
and are identified with the low state drawing identifier bubble;
for example:

```
+---------------------------------------------------------------+
| FUNCTION  |                   DEFINITION                      |
|-----------|---------------------------------------------------|
|           | ELECTRICAL |  LOGICAL   |        STATE            |
|           |------------------------------------------------   |
|  SIGNAL   |     H      | 1 TRUE     |  ACTIVE, ASSERTED        |
|           |     L      | 0 FALSE    |                         |
|  SIGNAL-  |     L      | 1 TRUE     |  ACTIVE, ASSERTED        |
|           |     H      | 0 FALSE    |                         |
+---------------------------------------------------------------+
```

NOTE: The system bus signals which are active in the low state
are shown with the negation symbol preceding the term (-SIGNAL).
The WDC logic diagrams follows this convention for system bus
signals only.

6.1.2 Electrical Description

Signals that have the negation symbol have a logical/electrical
relation that is:

```
+------------------------------------------------------------+
| LOGICAL  |  ELECTRICAL    |              |                  |
|  STATE   |    STATE       |   RECEIVER   |    DRIVER        |
|----------------------------------------------------------  |
|    0     | H = TTL HI STATE | 5.25v>H>2.00v | 5.25v>H>2.40v |
|    1     | L = TTL LO STATE | 0.80v>L>0.50v | 0.50v>L>0.00v |
+------------------------------------------------------------+
```

and signals that do not have the negation symbol have a
logical/electrical relation that is:

```
+------------------------------------------------------------+
| LOGICAL  |  ELECTRICAL    |              |                  |
|  STATE   |    STATE       |   RECEIVER   |    DRIVER        |
|----------------------------------------------------------  |
|    0     | L = TTL LO STATE | 0.80v>L>0.00v | 0.50v>L>0.00v |
|    1     | H = TTL HI STATE | 5.25v>H>2.00v | 5.25v>H>2.40v |
+------------------------------------------------------------+
```

6.2 WD5010/WD5020 WDC/ESDI DEVICES

6.2.1 WD5010 WINCHESTER DISK CONTROLLER

The WD5010 Winchester disk controller is shown on sheet 5 of the schematic. It should be noted on the logic diagram that the SDH register latch enable signal (SDHLE-) is not used. The SDH register is contained within the WD1014 support device and the register address decoding and control is included in the WD1014 logic. The SDH register contents are controlled by the control processor firmware.

The WD5010 shares the local bi-directional data bus with the control processor, sector data memory and other VLSI devices. The WD5010 controls the bus when BCS- is asserted.

6.2.2 WD5020 ESDI SUPPORT DEVICE

TBS

6.3 WD1015 BUFFER MANAGER CONTROL PROCESSOR

Primary WDC control is provided by the WD1015 control processor (see sheet 4). The WD1015 can access registers in the WD5010, WD5020, WD1014 and WD1100-14 devices and functions primarily to aid in the execution of host generated commands and in error recovery procedures. The control processor also performs several module self-tests following a 'diagnose' command, master reset or programmed reset (refer to Section 8.0).

The processor input port (port 1) and testable input pins allows firmware testing of the WD5010/20 operation completion signals (INTRQ1/2), the sector buffer RAM address overflow term (SBEF), the WD1100-14 ECC error flag and the drive attention, ready, index, select and command complete status signals. The output port (port 2) is used to provide status (CORRD, ERROR and WF), allow WD1100-14 access and signal the 'long' operational mode (signal LNGMD). The external address control input to the processor (EA) is terminated with a resistor to ground to facilitate production test requirements.

All processor program code and program-related data is stored in
internal WD1015 ROM and RAM.   The module RAM sector data buffer
lower bank is restricted to disk read/ write data; i.e., it is
not used to store WD1015 program variables.   The firmware
descriptions and listings are contained in separate WD1015 and
firmware protocol specifications.

6.4 WD1100-14 ECC GENERATOR/CHECKER

TBS

6.5 WD1014 LOGIC SUPPORT DEVICE

The WD1014 support device logic is shown as a single logic block
on page 7 of this specification.   The primary function of the
units logic is to provide the host command and error registers,
the fixed disk drive and head select register, sector data RAM
control and the WD1015 general control latches (see Figure 6-1).
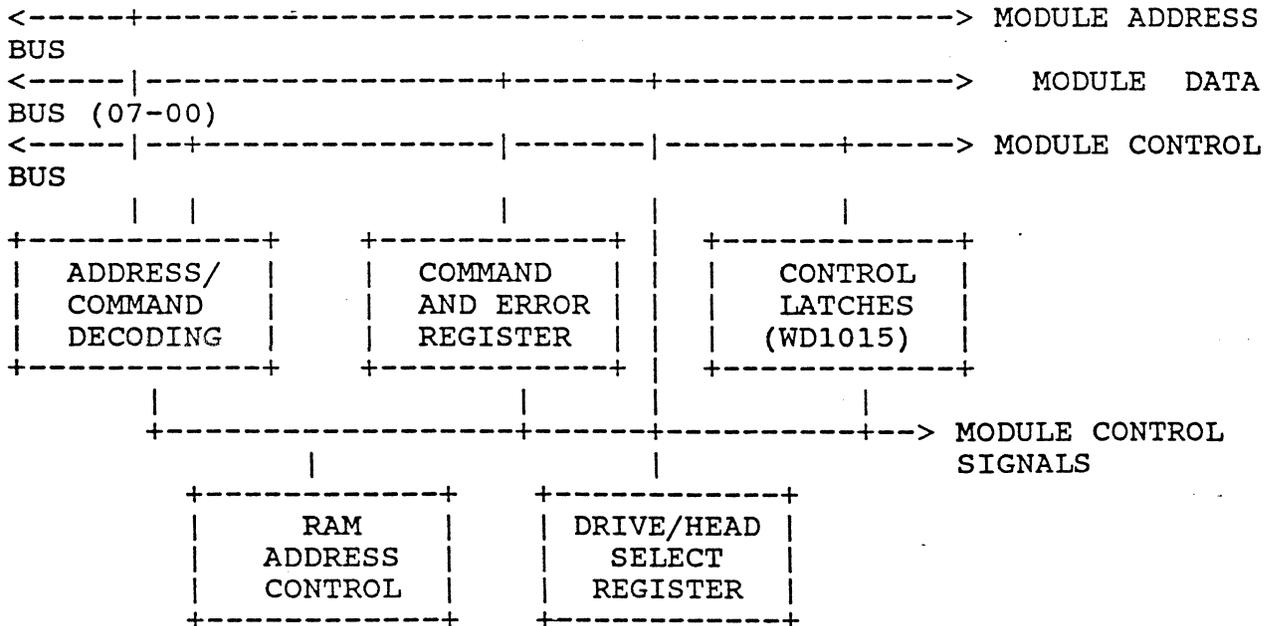
```
<-----+------------------------------------------------> MODULE ADDRESS
BUS
<-----|-------------------+-------+---------------> MODULE  DATA
BUS (07-00)
<-----|--+---------------|-------|---------+-----> MODULE CONTROL
BUS
      |  |               |       |         |
+------------+     +------------+ |    +------------+
| ADDRESS/   |     | COMMAND    | |    | CONTROL    |
| COMMAND    |     | AND ERROR  | |    | LATCHES    |
| DECODING   |     | REGISTER   | |    | (WD1015)   |
+------------+     +------------+ |    +------------+
      |                  |       |         |
      +------------------+-----+---------+--> MODULE CONTROL
            |                  |            SIGNALS
      +------------+     +------------+
      |    RAM     |     | DRIVE/HEAD |
      | ADDRESS    |     | SELECT     |
      | CONTROL    |     | REGISTER   |
      +------------+     +------------+
              FIGURE 6-1
          WD1014 BLOCK DIAGRAM
```

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6.5.1 WD1014 LOGIC DESCRIPTION

The WD1014 address signals (CS1-/0- and A2-0) and read/write con-
trol strobes are driven from the output of either the host or
WD1015 multiplex gates (sheets 3 and 4) depending on whether the
controller is idle or busy (signal WAUP asserted). The decoding
logic controls the WD5010, WD5020, and RAM chip select terms and
the RAM address counter reset and increment signals. The decode
logic also controls the WD1014 (internal) register gating and
general control signals.

The command and error register within the WD1014 is accessed by
the host at the WD5010 command and error register addresses and
allow control processor intervention in the command and error
report functions. The SDH (drive and head select) register is
also provided within the device.

6.6 SYSTEM BUS INTERFACE

Sheets 1 and 3 show the system bus address, data and control in-
terface signals. It is particularly important to note that the
I/O address lines (SA15-00) and the address control signal (AEN)
connect directly to the PAL1 (U34) for adddress decoding. The
data bytes (SD15-00) connect directly to bus transceivers for
connection to the buffered data bus (SDB15-00) and to a bus
buffer gate (U45) for gating to the local fixed disk (HD) data
bus. Figures 6-2, and 6-3 illustrate the I/O read and write
signals and general bus timing characteristics.

```
SA15-01         ----X‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾X----
                    _____

SA00            -----X‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾X----
                     _____
                    _____|Pio16, Pio08|_____
-IOR/-IOW       /                   \            /
                | IOhl16, IOhl08 |
                                              |Tio|
                _____              _____
-IOCS16                         | Tsa00 _____/
                                | Tsa15   |
                                       |T15|_____
READ DATA       ------------------------X‾‾‾‾‾‾‾‾‾‾X-----
                                       |T07|_____

WRITE DATA      ------------------X‾‾‾‾‾‾‾‾‾‾‾‾‾‾X----
                                   |   Tsdw     |
```
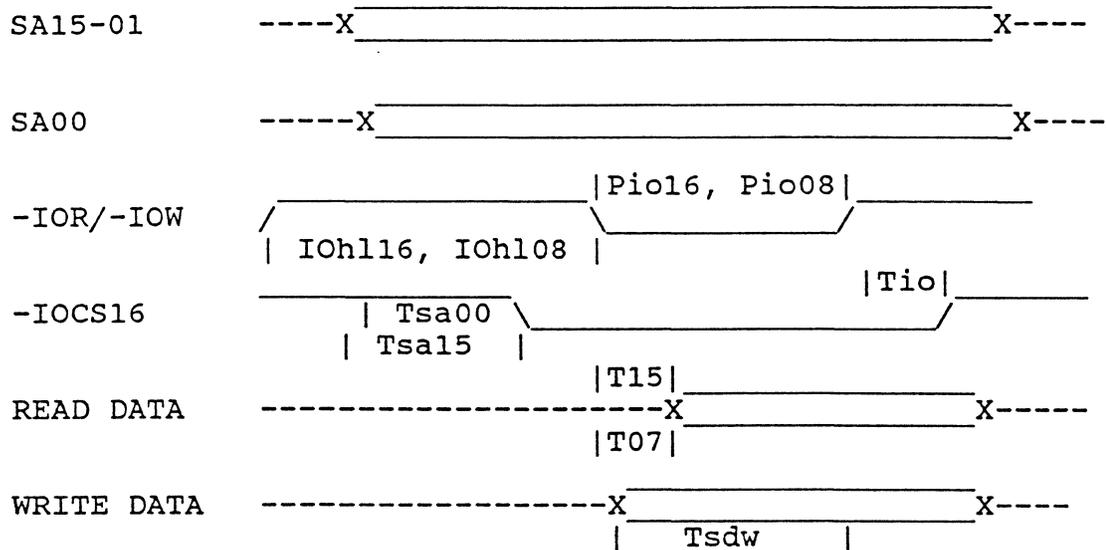
FIGURE 6-2
SYSTEM BUS SIGNALS
PROGRAMMED I/O CONTROL

| SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
Tsa15	-IOCS16 from SA09-01		90	nsec
Tsa00	-IOCS16 from SA00		70	nsec
Tio	+IOCS16 from +IOR/+IOW		90	nsec
T15	SD15-08 from -IOR		130	nsec
T07	SD07-00 from -IOR		110	nsec
	SD15-08 HIZ from +IOR		50	nsec
	SD07-00 HIZ from +IOR		30	nsec
Tsdw	SD15-00 to +IOW	60		nsec
	+IOW to SD15-00 HIZ	50		nsec
Pio16	-IOR/-IOW pulse width (16 bit)	160		nsec
Pio08	-IOR/-IOW pulse width (8 bit)	540		nsec
IOhl16	+IOR/+IOW to -IOR/-IOW (16 bit)	450		nsec
IOhl08	+IOR/+IOW to -IOR/-IOW (8 bit)	375		nsec

FIGURE 6-3
SYSTEM BUS TIMING CHARACTERISTICS

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6.7 FIXED DISK DRIVE INTERFACE

Sheets 1, 6 and 7 illustrate the control and data interface to the disk drives.

6.7.1 Control Interface

The control input signals (sheet 7) are terminated with standard 150 ohm line terminators and buffered by 74LS14 Schmitt Trigger inverters. The (gated) Index, Attention, Transfer Acknowledge, Ready, Configuration/Status Data and Sector Pulse signals connect to the WD5010, WD5010 and WD1015 for control and status information. The non-gated Drive Selected and Command Completion signals also input to the above devices.

All drive control outputs (head select, write gate, etc.) are driven by standard open-collector 7438 drivers. The write gate and head/drive select signals are wrapped back to the Digital Input Register for diagnostic information.

6.7.2 R/W Data Interface

U35 and U30 are the differential data drivers and receivers for each of two drives and connect to separate radial data cables – see referenced documentation for a complete description of the fixed disk read/write data timing and clocking requirements.

6.8 BUFFER MEMORY

The RAM data buffer memory is shown on sheet 8. The RAM address is provided by a 10-bit counter controlled by the WD1014 and an associated logic PAL (PAL2). The RAM chip select (RCS-) is controlled by the WD1014 with the RAM read/write strobes driven by the PAL2 logic – see referenced PAL documentation.

6.9 CLOCK OSCILLATORS

The WD1015, WD5010 and WD5020 clock inputs and drive data clocking is controlled by a 10 MHZ crystal oscillator. The clock generation and default clock control flip-flops are shown on sheet 9. Figure 6-4 illustrates the clock switchover waveforms from drive reference clock to module default clock.

```
SYSCLK _| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |

REFCLK | ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |_

DRVSEL _____|  ̄ ̄ ̄ ̄ ̄ ̄ ̄ ̄ ̄ ̄ ̄ ̄ ̄ ̄ |_____

SYSFF _| ̄ |_| ̄ |_| ̄ |_____| ̄ |_| ̄ |_| ̄ |

DRVFF _____| ̄ |_| ̄ |_____

DTCLK _| ̄ |_| ̄ |_| ̄ |_____| ̄ |_| ̄ |_| ̄ |_| ̄ |_| ̄ |
```
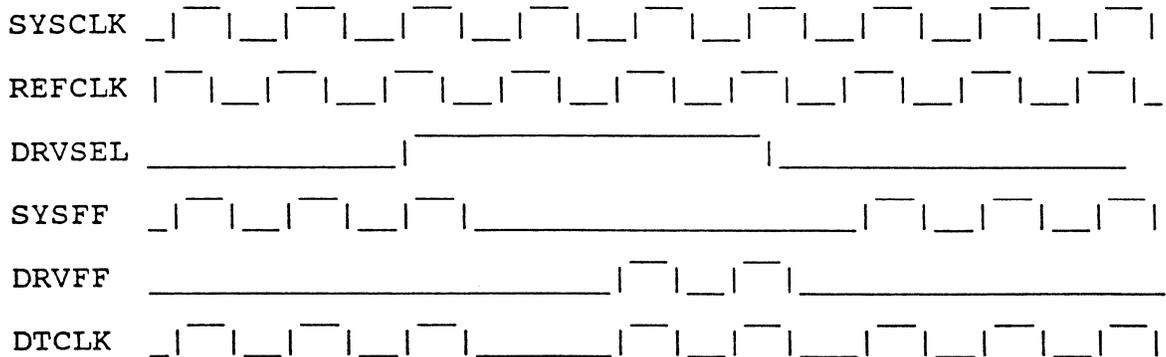
FIGURE 6-4
CLOCK SWITCHOVER WAVEFORMS

6.10 MODULE RESET CIRCUIT

The module power on and low VCC monitor reset control circuitry
is shown on sheet 2. Resistors R1 and R2 set the low VCC trip
point at approximately 4.1 volts. Resistor R4 and capacitor C2
form the power on delay RC and force a reset for 50 to 100 mil-
liseconds after the monitor threshold has been exceeded. Module
reset is also driven by the master reset from the system bus.

6.11 LED DRIVER

The LED (activity) indicator driver and connector are shown on
Sheet 1.   The driver follows the 'wakeup' latch signal (WAUPL).
A current limiting resistor on the WDC limits the indicator cur-
rent to approximately 20 milliamperes.

7.0 INSTALLATION

The WDC module may be installed in any suitable PC slot that
provides both the P1 and P2 connectors.

7.1 MECHANICAL

Figure 7-1 illustrates the general module IC placement and ap-
proximate drive connector locations. The module dimensions are
13.12 by 3.87 inches and a mounting bracket is included.

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```
+--------------------------------------------------------------+
| J1                                                           |
|                                                              |
|                          _       _                           |
|                       |_|    |_|    |___|                    |
|                                                              |
|                        J2     J3     J4                      |
|                                                              |
|                                                              |
|                                                              |
|                                                              |
+-----------------+        P2     +--+          P1      +---+  |
                  +-----------+  +--------------------+
```
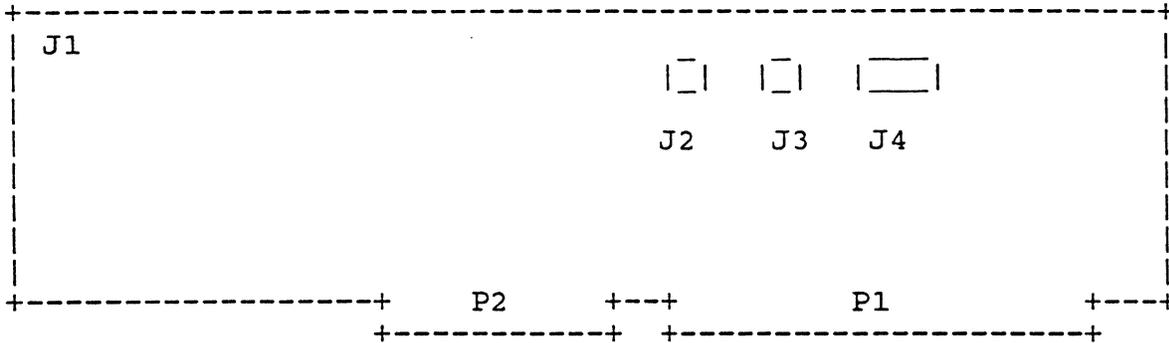
FIGURE 7-1
WDC MODULE LAYOUT

7.2 ADDRESS SELECT JUMPERS

The module primary address range (1F0-1F7 and 3F6-3F7) is
selected by installing the address jumper on pins 2-3 of W3.
The secondary address range is selected by jumper on pins 1-2 of
W2 for addresses 170-177 and 376-377.

8.0 TESTING

8.1 WDC SELF TESTS

The encoded result desriptors for each controller self test are
shown in Figure 8-1. The WDC error register HDERR (hex address
1F1/171) is used to report the test result. The tests are ex-
ecuted following the 'diagnose' command or any reset.
The tests verify the WD1015 firmware checksum, the WD1015 RAM
memory, the sector buffer RAM memory and the WD5010, WD5020,
WD1014 and WD1100-14 data paths. System bus, host interactive or
drive diagnostic tests are not included.

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```
+-----------------------------------------+
| RESULT |          DESCRIPTION           |
|-----------------------------------------|
|   01   | No Errors                      |
|   02   | WD5010/5020 Device Error       |
|   03   | Sector Buffer Error            |
|   04   | WD1014/1100-14 Device Error|
|   05   | WD1015 Device Error            |
+-----------------------------------------+
```

FIGURE 8-1
SELF TEST ERROR CODES

8.2 SYSTEM TESTS

Module software tests designed to operate in the PC-AT other than
the sector data buffer read/write diagnostic commands are not
covered in this document.   These tests would include the WD
"DAD" diagnostic test.

9.0 GENERAL SPECIFICATIONS

9.1 POWER AND ENVIRONMENTAL

9.1.1 Power Requirements

```
        5 VDC         +/- 5.0%  < 2.500 amps
      +12 VDC         +/- 10.0% < 0.020 amps
      -12 VDC         +/- 10.0% < 0.010 amps
      Ripple          100mv p-p(max) all voltages
```

9.1.2 Environmental

```
      Temperature
         Operating          10 to 50 degrees celsius
         Non-operating      -40 to 60 degrees celsius

      Humidity
         Operating          8% to 85% non-condensing
         Non-operating      5% to 95% non-condensing
```

Shock and Vibration
   Shock   35G/20MS square wave maximum
   Vibration   1G/0-600Hz, dwell not to exceed
               30 seconds at (any) resonance
Altitude
   Operating   0 to 3000 meters maximum
   Non-operating   0 to 5000 meters maximum

FCC
   Class   B

MTBF   78,000 POH

9.2 CONTROLLER - FIXED DISK FEATURES

9.2.1 RECORDING SPECIFICATIONS

Encoding Method   NRZ

Data Rate   10.0 MBS

Sector format   512 bytes/sector, 36 sectors/track max
                   hard sectored format only

Drives supported   2 maximum
Heads supported   16 maximum
Tracks supported   32,768 maximum (2048 cylinders)

9.2.2 ERROR CORRECTION SPECIFICATIONS

Method   Polynomial division

Degree   56

Forward polynomial $X^{56} + X^{52} + X^{50} + X^{43} + X^{41} +$
                       $X^{34} + X^{30} + X^{26} + X^{24} + X^{8} + 1$

Reciprocal polynomial $X^{56} + X^{48} + X^{32} + X^{30} + X^{26} +$
                       $X^{22} + X^{15} + X^{13} + X^{6} + X^{4} + 1$

Record length (r) = 519 X 8 bits maximum

Correction span (b) = 12 bits maximum

Single burst detection span = 32   r = 519 X 8 bits

                                     With b = 12 bits
Double burst detection span = 11   r = 519 X 8 bits

                                     With b = 12 bits

Miscorrection probability = 1.47(E-11), r = 519 X 8 bits

9.3 DRIVE INTERFACE

All control and data drivers, receivers and signal terminations
are per the ST-412 interface specification. Drive attachment is
restricted to two units. Drives with up to sixteen heads are
supported.

9.3.1 FIXED DISK DRIVE CONTROL CONNECTOR

WD Part No. 41-000019-000 (Berg type XXXXX-XXX),   Pin 15
polarization

9.3.2 FIXED DISK DATA CONNECTORS

WD Part No. 41-000006-00 (Berg type XXXXX-XXX)

9.3.3 LED Connector

WD Part No. 41-001008-00 (Berg type 65500-104)

9.4 SYSTEM BUS INTERFACE

Programmed I/O is used for all fixed disk control and data
transactions. All data transfers are 16-bits and use the channel
'fast I/O' protocol.   All control transfers are 8-bits wide and
use the lower bus data byte.   The module I/O primary and secon-
dary address range and priority interrupt assignments are fixed.

Bus loading for all WDC input signals will not exceed 2 standard
LSTTL loads in either logic sense.   Module output low state sink
current (Iol) at Vol = 0.4 volts is 12 ma.   on all tri-state out-
puts and 40 ma. on open collector outputs.

APPENDIX

A. SYSTEM BUS CONNECTOR P1

Pins and signals are viewed as looking down at the connector with
the module component side to the right.

```
            B01  GND            A01
            B02  RESET          B01  SD07
            B03  VCC            A03  SD06
            B04                 A04  SD05
            BO5                 AO5  SD04
            B07  -12VDC         A07  SD02
            B08                 A08  SD01
            B09  +12VDC         A09  SD00
            B10  GND            A10
            B11                 A11  AEN
            B12                 A12
            B13  -IOW           A13
            B14  -IOR           A14
            B15                 A15
            B16                 A16  SA15
            B17                 A17  SA14
            B18                 A18  SA13
            B19                 A19  SA12
            B20                 A20  SA11
            B21                 A21  SA10
            B23                 A23  SA08
            B24                 A24  SA07
            B25                 A25  SA06
            B27  T/C            A27  SA04
            B28  BALE           A28  SA03
            B29  VCC            A29  SA02
            B30                 A30  SA01
            B31  GND            A31  SA00
```

B. SYSTEM BUS CONNECTOR P2

Pins and signals viewed as looking down on the connector with the
module component side to the right.

```
D01              C01
D02   -I/OCS16   C02
D03              C03
D04              C04
D05              C05
D06              C06
D07   IRQ14      C07
D08              C08
D09              C09
D10              C10
D11              C11   SD08
D12              C12   SD09
D13              C13   SD10
D14              C14   SD11
D15              C15   SD12
D16   VCC        C16   SD13
D17              C17   SD14
D18   GND        C18   SD15
```

C. FIXED DISK DRIVE CONTROL CONNECTOR J4

Drive control connector viewed as looking at the connector from module component side. (WD connector type LE-8805)

01	GND	02	HS3-
03	GND	04	HS2-
05	GND	06	WG-
07	GND	08	CSD-
09	GND	10	XACK-
11	GND	12	ATN-
13	GND	14	HS0-
15	KEY	16	SCT-
17	GND	18	HS1-
19	GND	20	INDEX-
21	GND	22	RDY-
23	GND	24	XREQ-
25	GND	26	DS0-
27	GND	28	DS1-
29	GND	30	RESERVED
31	GND	32	RG-
33	GND	34	CMD-

D. FIXED DISK DRIVE DATA CONNECTORS J2/J3

The drive data connectors are shown as looking at the connector from the module component side. (WD connector type LE-8804)

01	DSEL0-/1-	02	SCLK0-/1-
03	CMDCPL0-/1-	04	AME0-/1-
05	KEY	06	GND
07	WTCLK0/1(+)	08	WTCLK0/1(-)
09	NU	10	RFCLK0/1(+)
11	RFCCLK0/1(-)	12	GND
13	NRZWD0/1(+)	14	NRZWD0/1(-)
15	GND	16	GND
17	NRZRD0/1(+)	18	NRZRD0/1(-)
19	GND	20	NU

E. EXTERNAL INDICATOR CONNECTOR J1

(WD connector type 41-001008-00)

```
01   LED+
02   LED-
03   LED-
04   LED+
```

F. WD5010 DISK FORMAT WITH 1100-14[EXTERNAL 56 BIT ECC]

WD5010 format with WD1100-14 (56 bit ECC)

GAP1	8*'00'
PLO SYNC	16*'00'
ID SYNC	'A1' 'FE' (Note 1)
ID	Cyl Lo Head (Note 2) Sector
ID CHECK (Note 3)	CRC Hi CRC Lo
PAD	2*'00'
WRITE SPLICE	1 byte
PLO SYNC	12*'00'
DATA SYNC	'A1' 'F8'
DATA	512 bytes
ECC	7 bytes
PAD	2*'33'
INTER-SECTOR GAP	10*'4E'

Note 1:   'FE' for cylinder numbers 0-255.
           'FF' for cylinder numbers 256-511.
           'FC' for cylinder numbers 512-767.
           'FD' for cylinder numbers 768-1023.
           'F6' for cylinder numbers 1024-1279.
           'F7' for cylinder numbers 1280-1535.

'F4' for cylinder numbers 1536-1791.
'F5' for cylinder numbers 1792-12047.

Note :2   bit 7(msb) is bad block flag.
           bit 6 = 0 and bit 5 = 1 for 512 byte sector.
           bit 4 = 0.
           bit 3 - bit 0 are head number.

Note 3:   The 1005-WAH specifies that ID check polynomial is $X16+X12+X5+1$ with CRC register preset to '1's. The ID sync ('A1 FE') is not included in the calculation. The WD5010 uses the same polynomial and presets the same way but the ID sync ('A1 FE') is included in the calculation.