XEROX
BUSINESS SYSTEMS
Systems Development Department

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Subject: **Dandelion Clocks**
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Overview

This memo describes the clock generation and distribution system for the Dandelion processor. It also considers the effects of clock skew caused by component variations and the physical separation of components. Using statistical methods for calculating the propagation delay of the gates in the clock distribution chain, 99.7% of Dandelions will work with off the shelf chips meeting vendor's specifications. Independent of this, however, it is recommended that the ability to measure clock skew on a production basis be developed in the board manufacturing facility. This would assure that all boards are within tolerance and also provide us with valid data on the true distribution of timing parameters in the production environment.

Clocks

The clock circuit on the high speed I/O board provides the following to the rest of the processor. They are all derived synchronously from a 51.04 MHz crystal clock.

137.14 nS processor clock
Click number within the round (3 bits)
Cycle number within the click (3 bits)
Clocks for the memory (RAS, CAS, WPulse)
Display bit clock and Prom counter

Clock Signals on Backplane

The processor, memory, and display clocks are all synchronous to the 51.04 MHz crystal. The largest cycle over which everything repeats is the horizontal line. Each horizontal line contains 14 processor rounds of 5 clicks each (70 clicks total). Each click (411 nS) has 3 cycles (137 nS) making a total of 210 cycles (28.8 uS) per horizontal line. Memory timing repeats once per click.

Following is a list of the clocks provided. In the descriptions below, the signal timing is that seen on the backplane and the low-high transition of Clk is the reference point of 0 nS. This reference point is 25 nS (typ) after the 15 to 9 transition of the main ECL clock counter.

ppClk - This signal repeats every 137 nS, is high for 98 nS and low for 39 nS. On each board, it passes through an inverting clock receiver (74S02) and an inverting clock qualifier (74S00, S04, S10, S20, or others (S51) if not critical) to become a qualified clock (Clk) which is used on that board. This clock will have some amount of skew with respect to the memory clock signals. The magnitude of this skew and associated production considerations are discussed in a later section.

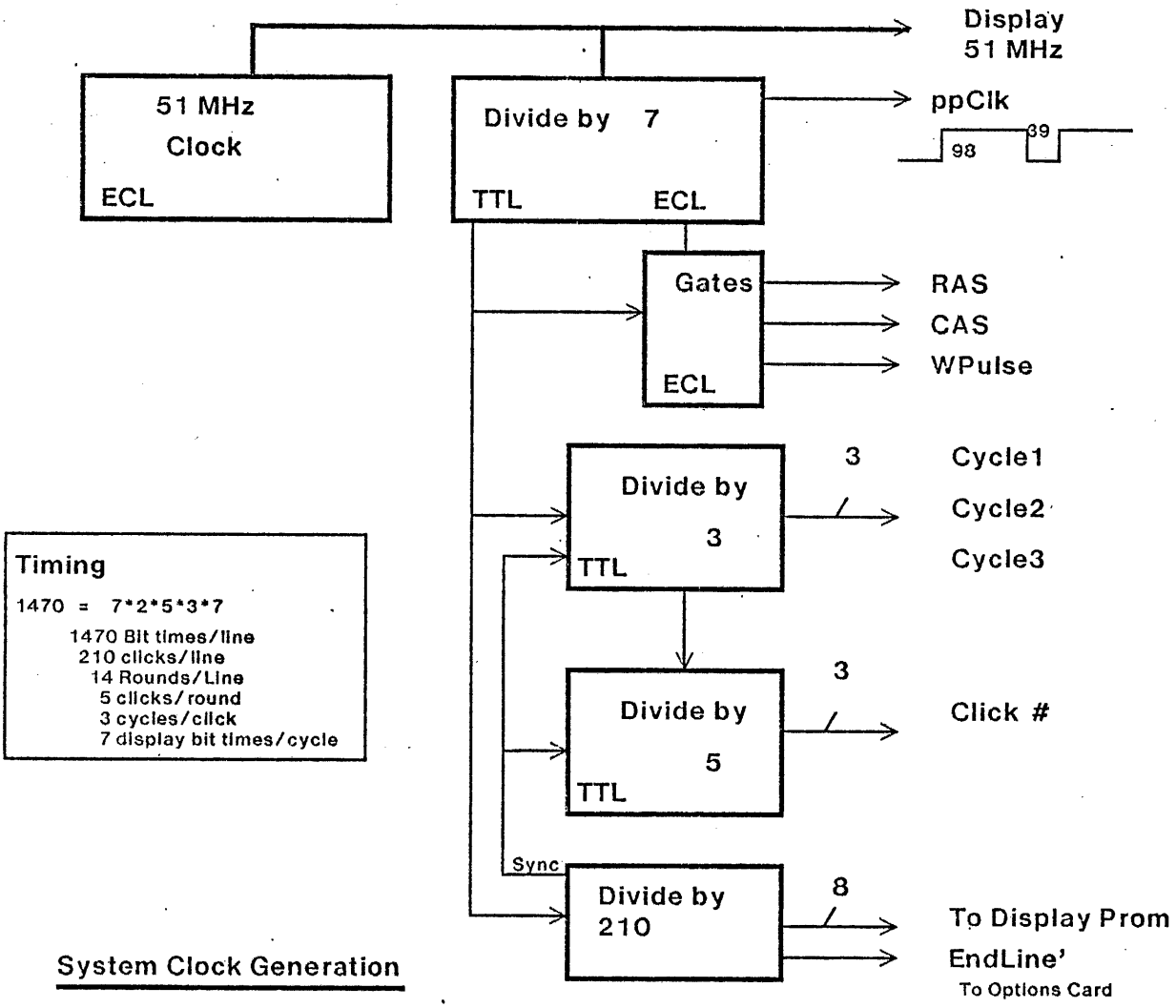
Cycle.1', Cycle.2', Cycle.3' - These signals are the output of a counter clocked by ppClk. Each one goes low in its cycle of a click and is high the rest of the time. While these signals are glitch free, the transitions occur between 5 and 38 nS after Clk. Thus they can be used as clock qualifier signals. If these signals are to be strobed into a register by Clk, they should pass through 1 extra gate delay before the input to the register to assure it meets the hold time requirement of the register.

Click.0, Click.1, Click.2 - These signals are a binary encoding of the click number. Click.0 is the most significant bit and Click.2 is the least significant bit. They also come from a counter clocked by ppClk and have the same timing as Cycle.1' above.

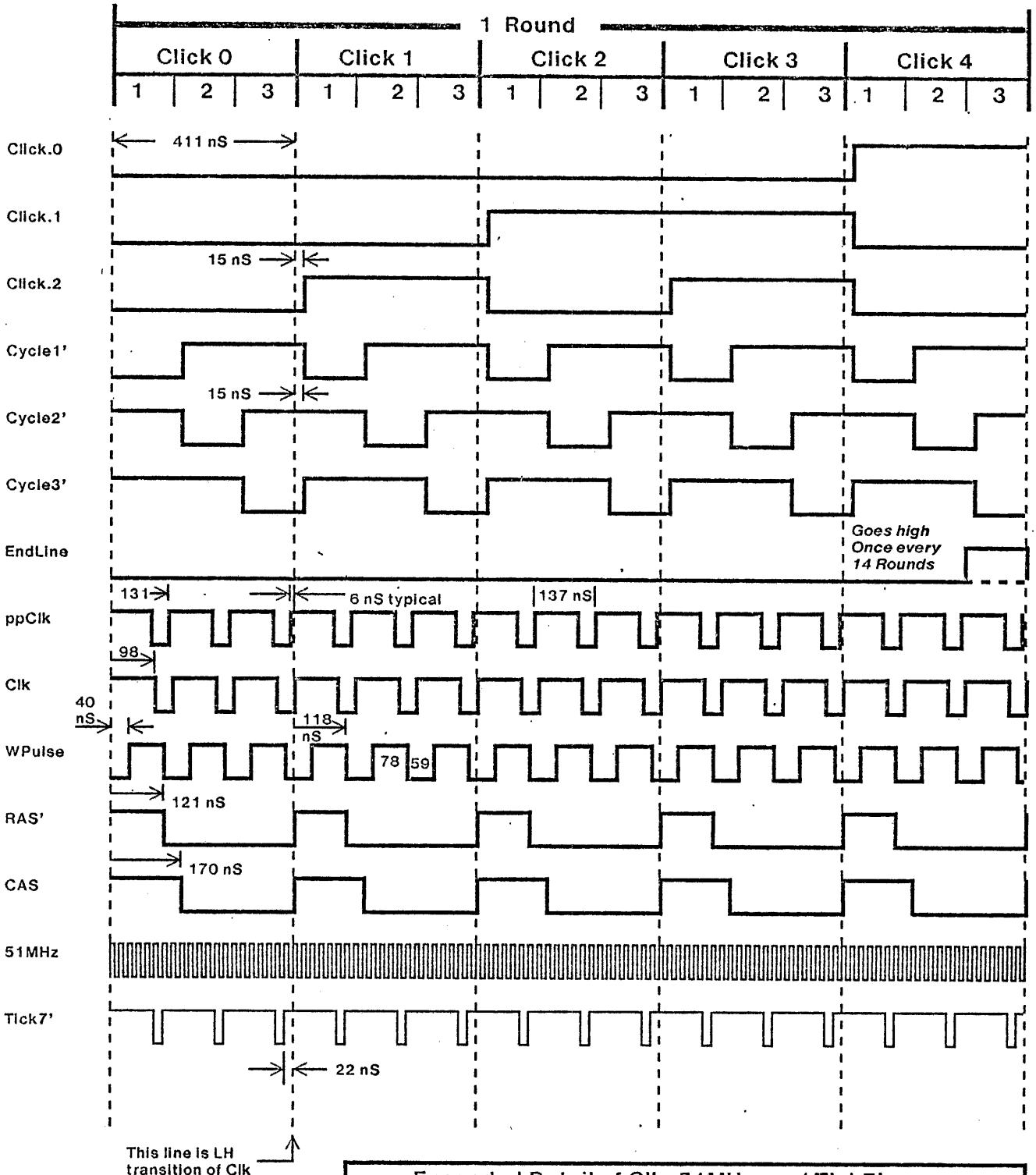
RAS' - This is a memory timing signal used to strobe the high order address bits into the 16K dynamic memory chips with multiplexed address inputs. This signal has a period of one click. It goes low 10 nS before ppClk goes high at the end of cycle 1 and goes high 1-3 nS after ppClk goes high at the end of cycle 3.

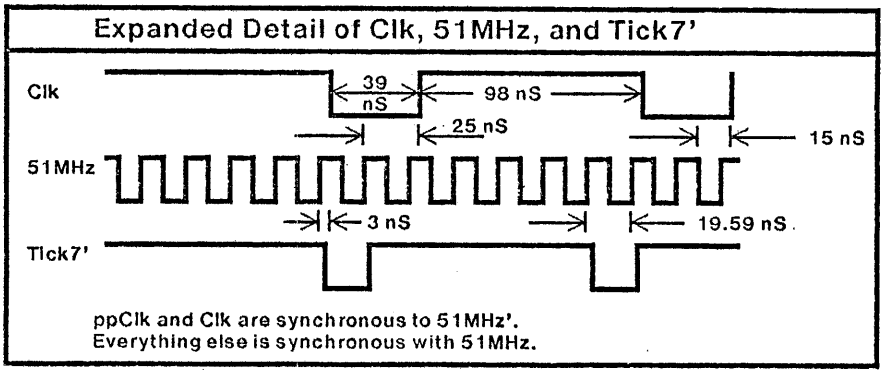
CAS - This is a memory timing signal used to strobe the low order address bits into the 16K dynamic memory chips with multiplexed address inputs. This signal has a period of one click. It goes high 49 nS after RAS' goes low at the end of cycle 1 and goes low 1-3 nS after ppClk goes high at the end of cycle 3 (i.e. the same time RAS' goes high).

WPulse- This signal when qualified in the memory, is used to enable the write inputs of the memory chips at the end of a memory cycle. WPulse goes high in the middle of each cycle and goes low at the end of each cycle, 2-6 nS before ppClk goes high.



System Clock Generation

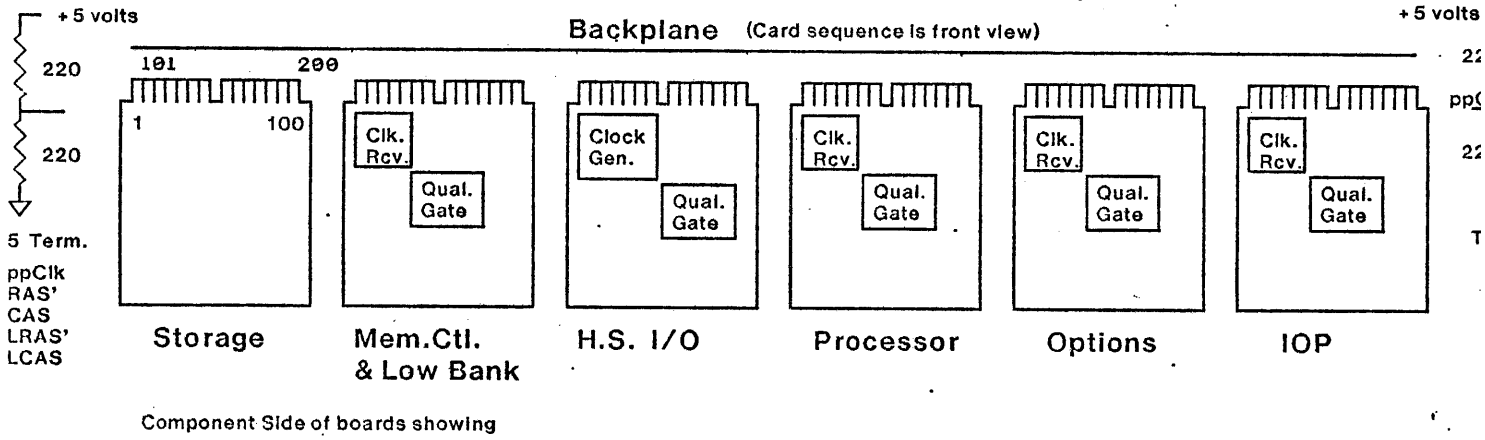




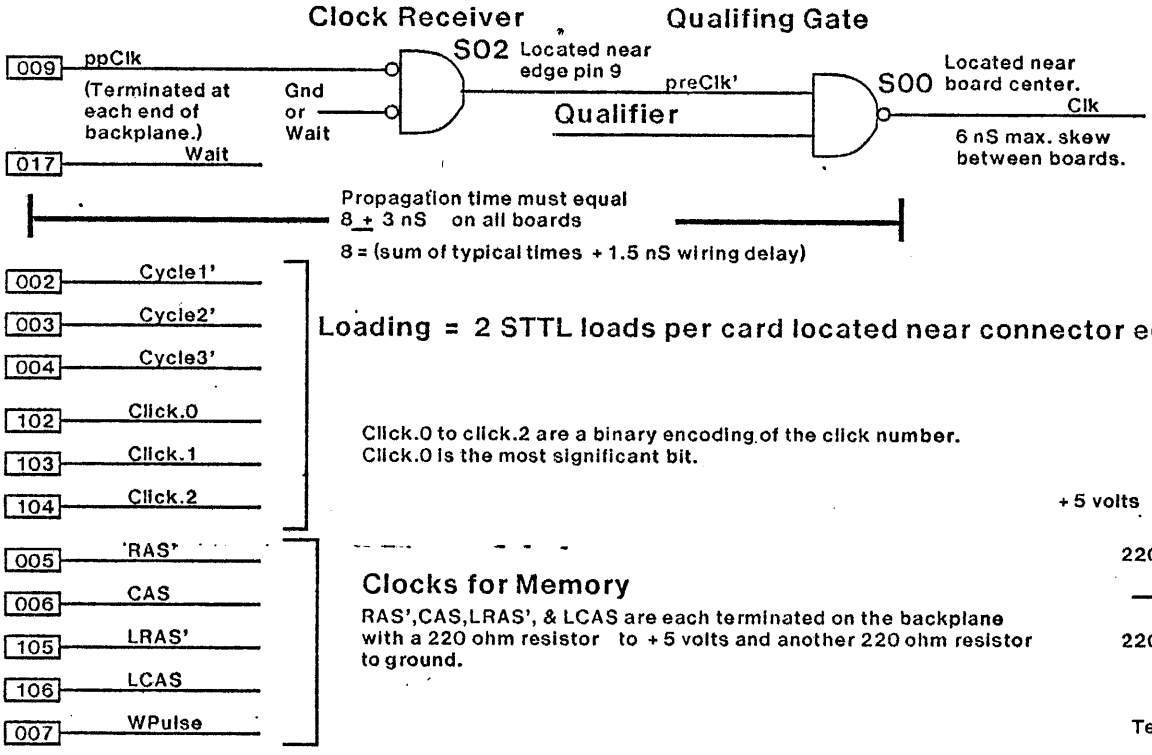
System Clock : Backplane Timing

Clock Distribution

Clock signals are generated on the High Speed I/O Board and distributed on the backplane as shown in the following diagram. Four of the memory timing signals are terminated on the backplane by 220 ohm pullup and 220 ohm pulldown resistors. ppClk is terminated on each end of the backplane in the same manner. Termination of these lines in their characteristic impedance (110 ohms is slightly high) minimizes ringing as well as rise and fall time variations. The next picture shows the details of receiving the clock signal at each of the boards. The receiver is located near the ppClk pin on the board edge and drives a line routed straight to the center of the board where the qualifying gates are located. Two such receivers are permitted per board. The number of qualifying gates tied to each of the clock receivers should be equalized if possible. This minimizes timing skew due to loading variation. The total propagation time should fall into a ± 3 nS range which is determined by the characteristics of typical chips and the production etch propagation time. (defining this tight range centered on typical times makes the chips easier to select)



System Clock Distribution



Clock Receiver Details for each Card

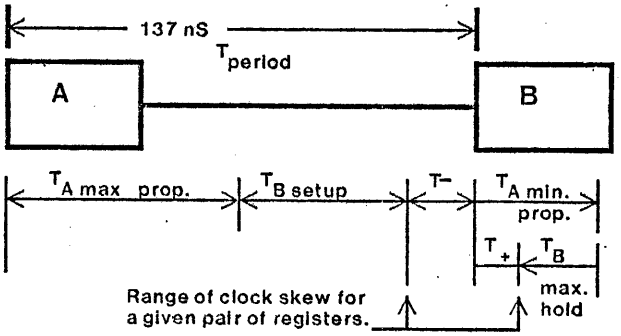
Allowable Skew Determined by Processor Data Paths

When a clock signal is distributed over a large system, it may arrive at the clock inputs of two registers at different times. That difference in time is called *skew*. The purpose of this section is to examine how much skew can be tolerated in the system.

The maximum allowable skew between clocks strobing registers A & B depends on the max. and min. propagation times between the output of register A and the input of register B and the setup and hold time requirements at the input of register B. Following are the limits for positive (T_+) and negative (T_-) skew of clock B referenced to clock A and the nominal clock period (T_{period}).

$T_{A(max.\ prop.)} + T_{B(setup)} + T_- \leq T_{period}$ Long Propagation path limit

$T_{A(min.\ prop.)} - T_{B(hold)} \geq T_+$ Short Propagation path limit



Relationship of Parameters Limiting Clock Skew

Notice that the maximum negative skew T_-, (the amount of time that B shows up early relative to A) is limited to the amount of excess time available between the time when the signal from A becomes valid at the input to B and the setup time of B for the nominal clock period. Put simply, the signal must make it to the register within its setup time, before the register is clocked.

The amount of time that B can show up late with respect to A (positive skew, T_+), must be less than the difference between the minimum propagation time for A and the hold time for B. The signal from A must not change before B is finished looking at it.

An evaluation of the source and sink parameters for the X-Bus, Y-Bus, and YH-Bus results in the following numbers for min. and max. propagation times and setup and hold times. Included are the effects of minimum and maximum enable and disable times for the tri-state drivers.

Parameter	X-Bus	Y-Bus	YH-Bus
Max. Prop.	92 nS	126 (see text)	52
Source	←MD	2901	29701
Max. Setup	40 nS	0 (see text)	70
Sink	2901	MAR	MAR
T_- (Long Path)	5 (>6 with Stat)	1 (>14 with Stat)	15
Min. Prop.	14 nS	24 nS	19
Source	Byte	2901	29701
Max. Hold	6	5	0
Sink	IOOut	SU	MAR
T_+ (Short Path)	8	19	19

T_{period} = 137 nS (Clk-Clk skew = 6 nS Clk-RAS' Skew for MAR← = 14.3 nS)

The allowable Clk-Clk skew is all greater than 6 nS, which is achievable in the clock distributiion system as shown in the following section. The Y-Bus propagation and setup times are limited by the MAR← operation. In this operation, the data must be latched at 127 nS into the cycle. Worst case delay is 126 nS while statistical worst case (3σ) delay is 113 nS, thus allowing 14 nS skew with statistics. The achievable Clk-RAS' skew is 14.3 nS without testing and 10 nS with testing.

Skew Sources and Magnitudes Determined by Clock Distribution Paths

A diagram showing the clock path from the 51 MHz clock to the outputs of the qualifying gates in the system is shown in the next figure. The principal sources of skew are in clock generation, backplane distribution, and board distribution. Each of the above is discussed below along with the proposed handling in production.

It should be noted that the relative skew between the memory system clocks and the processor clock (Clk-RAS') can vary over a wider range than the skew between the appearance of the Clk signal on two separate logic cards (Clk-Clk. This is because all cards use the same ppClk (within a backplane delay) to generate Clk and the only variation is that between the clock receiver and qualifier chips on separate cards. The memory system clocks are delivered to the backplane with some skew with respect to ppClk due to mismatch of components used in the clock generation logic.

Clock Generation

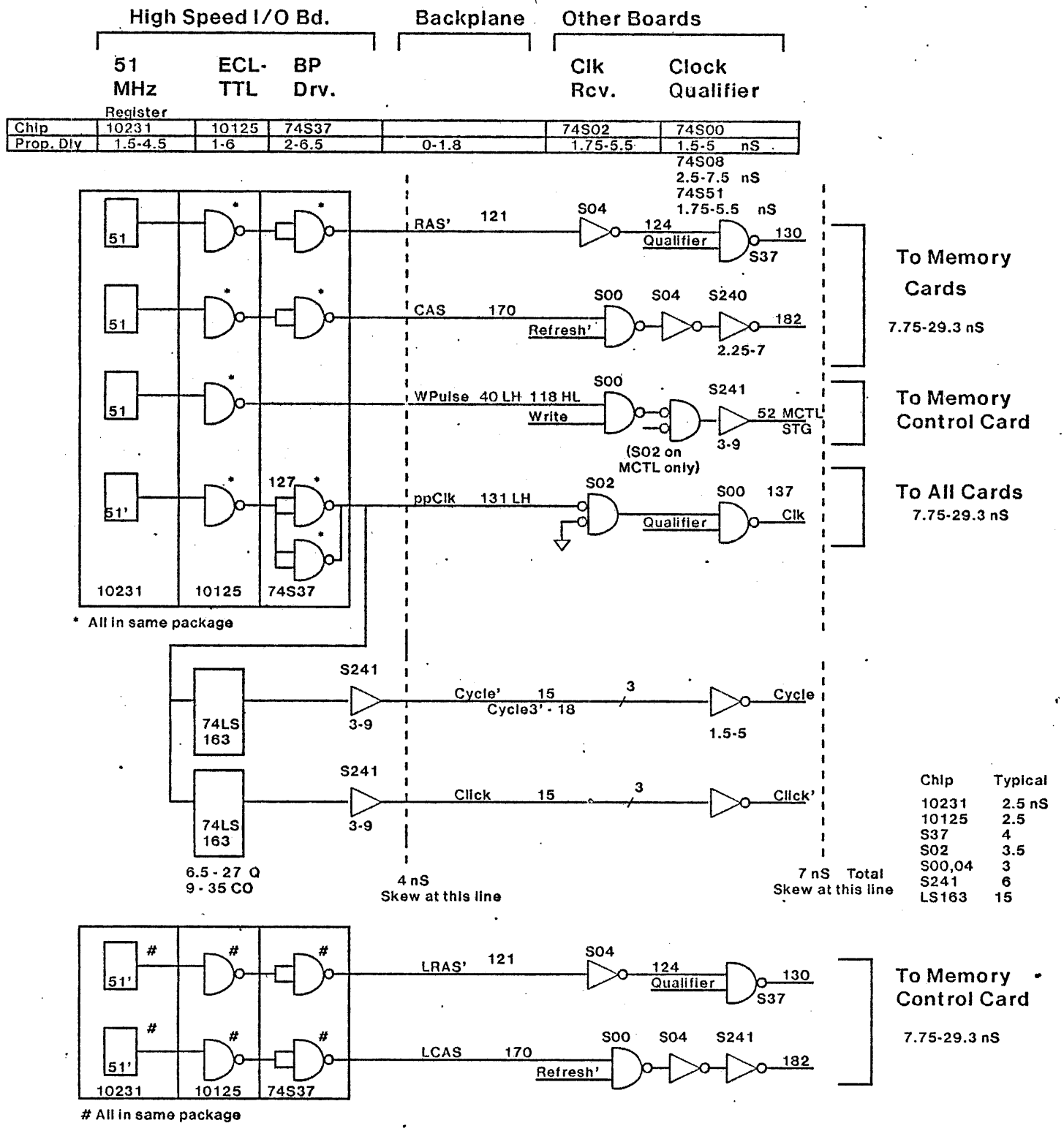
Clock generation is done with ECL logic to allow use of synchronous counters with a 19.59 nS clock cycle. At this point in the system, the only skew that affects system operation is that between ppClk and either RAS' or LRAS'. LRAS' is identical with RAS', except when the display is accessing the low 64K memory bank. ppClk, CAS, and LCAS are clocked from the high-low edge of the 51 MHz clock while everything else is clocked using the low-high edge of the 51 MHz clock. ppClk, LRAS', and RAS' are synchronous, but have rising and falling edges occurring at different times. The nominal (typical) location of each of these transitions is the reference point used in the discussions. The difference in nominal location of clock transitions is subtracted before considering skew.

The amount of skew resulting from use of different edges of the 51 MHz clock depends on the symmetry of the clock source. A 45% - 55% symmetry will result in a 1 nS skew. Variation in component propagation times (10231 D-Register, 10125 ECL-TTL Conv., and 74S37 Buffer - total prop. time = 4.5 to 17 nS) adds another 12.5 nS skew, worst case. The statistical worst case (3 sigma points which include 99.7% of units) is 7.3 nS skew. Adding the clock symmetry gives 8.3 nS skew. This assumes the distribution of propagation delays is a normal distribution with a mean of 2/3 Max. = typical and $+3\sigma$ and -3σ points equal to maximum and minimum propagation delays respectively. (see calculations)

It is proposed that each clock generator be checked in production to guarantee it has a skew of 4 nS or less. This would cause 15% of the boards to be rejected if the chips in the parallel paths on the board had independent characteristics. Since they will probably all come from the same lot, they will likely match and the 4 nS limit will not cause an excessive amount of rework. If a board fails to meet the limit, a well specified probe procedure is used to locate the bad component. (With a bed of nails type tester, this test could be automated such that the offending chip is identified automatically. A circuit which provides a slow TTL interface to the tester and provides 1 nS resolution can be done with about 20 chips and some delay lines.) Component substitution would take place to bring generator within limits. The number of substitutions could be kept low by using selected parts for these functions. Cost of the selected parts could be kept low by specifying that the timing fall within a narrow range centered on the typical time rather than some extreme of the component range.

Backplane Distribution

The skew introduced by the backplane is a fixed function of the physical separation of the boards. The magnitude of the skew ranges from 0 to 1.8 nS depending on backplane position. This number is not included in skew calculations, because a large (10 nS) delay has already been included for backplane in processor numbers.



Note:

1. TTL minimum propagation times above are equal to .5 the typical delay listed in data book.
2. In production, the clock drivers (on HSIO board) will be checked for equal delays, i.e. LRAS = RAS and LCAS = CAS. It is reasonable to assume that gates in the same package have the same delay, but this should also be verified on early boards.
3. Propagation delay from backplane clock bus, through qualifiers, to qualified clock outputs should be __nS +-__1 nS for all boards. This should also be production checked.
4. Numbers above are propagation times in nanoseconds. Single numbers are typical numbers indicated in data sheets. Two numbers indicate a range. Minimum = sum of minimums. Maximum = sum of maximums. (Based on data book 25 deg. C & 5 volt)
5. 10231 ECL flip-flops are clocked by a 51 MHz clock (51) and its complement (51').

Clocks
Clock gen
Distribution
Skew
Allowable Skew
Prop. & hold times

Board Distribution

On each board, ppClk travels from the backplane pin, to a nearby receiver, through about 7 inches of etch, to the qualifier gates located in the center of each card, and finally to the register to be clocked. The worst case skew in this path is 7 nS and the statistical worst case (3σ points) 6 nS. The path from the edge pin to any register communicating off board should be 8 nS ±3 nS. .3 % of the boards will need rework with this limit.

In production, the only variation will be due to IC chip variation since the etch pattern will be fixed. This path should be checked on early units to monitor the distribution of delay times as well as correct out of spec units. Assuming that all gates in an IC package have the same delay, only enough paths would need to be checked to verify at least one pair of gates in each receiver-qualifier package pair.

Appendix

This appendix contains the method of doing the statistical delay calculations as well as the data used to calculate the allowable skew in the system.

Statistical Calculation of Propagation Delay of Clock Distribution Chain

1. It is assumed that the propagation delays of the gates have a normal distribution whose mean is the typical gate delay and 3 times the standard deviation is the limit for max and min prop. times. The approximate rule used by the ED memory group is that min. = 1/3 Max. Typ. = 2/3 Max. This assumption should be checked with the components group.

2. For a normally distributed random variable, the following percentages of all samples fall within the limits indicated

Limits	Percentage
Typ. ± 1 sigma	68%
Typ ± 2 sigma	95.4%
Typ ± 3 sigma	99.7%

sigma - standard deviation

$(\text{sigma})^2$ = variance

3. The statistical sum is the sum of the typical times plus or minus the square root of the sum of the variances.

Clk vs. Clk
on separate logic cards
Skew = 6 nS

S02	S00
3.6 ± 1.8	3.3 ± 1.7

Worst Case 3.5 to 10.4 → 6.9 nS skew

Statistical $3.6 + 3.3 \pm \sqrt{3.24 + 2.89} = 6.9 \pm 2.47$ → 5.94 nS skew

ppClk vs. RAS'
in clock generator
Skew = 8.3 nS

Clock * Symm.	10231	10125	74S37
0 ± .5	3 ± 1.5	3.5 ± 2.5	4.2 ± 2.2

Worst Case 5 to 17.4 → 13.4 nS skew

Statistical $3 + 3.5 + 4.2 \pm \sqrt{2.25 + 6.25 + 4.84} \pm .5 = 10.7 \pm 4.15$ → 8.3 nS skew

* Clock symmetry is added directly because it preceeds the logic chains.

CasLatch vs Clk
In memory system for MAR←
Skew = 14.3 nS

Clock Symm.	10231	10125	74S37
0 ± .5	3 ± 1.5	3.5 ± 2.5	4.2 ± 2.2

Clock generator skew from HSIO board 8.3 nS

S02	S00/S04
3.6 ± 1.8	3.3 ± 1.7

Receiver skew on processor & memory cards. 6 nS

Worst Case 8 to 28.3 → 20.3 nS skew

Statistical Can only take sum of two boxes above since they are separate assemblies which are tested separately. 8.3 + 6 → 14.3 nS skew

Data for Calculation of Allowable Skew

X-Bus Sources	Data Path		EnablePath		Min. Prop. Time	Max. Prop. Time	Min. Enable / Disable
SU	25S09	93422	S374		38	62	28
RH	S374	Am29701 S241	S374	S138	20	61	19
StackP	25S09	S240	S374	S138	38	65	19
IB	LS374	S374 S138 S257	S374	S20	22	42	16.5
YBus	25S10		S374	S20	5+Y-Bus	22+Y-Bus	16
"Zero"	S241		S374	S10 S00	NA	9	20
Byte(fY)	S374	S374 S138 S257	S374	S00	14	32	16.5
Nibble(fZ)	S374	S241	S374	S00	14	26	17
ErrIntStatus	S374	S240	S374	S138	12.5 NA	24	19
←MD		S241	LS163	+S240	50 (Cy3)	92 (Cy3)	15
IOIN	S374		S374	S138 +BP	8 NA	17	18 + BP
Y-Bus Sources							
2901	S374	2901A-1	(Always enabled)		24	91	
YH-Bus Sources							
2901	S374	Am29701	(Always enabled)		20	52	

X-Bus Sinks			Setup Time	Hold Time
2901	2901A-1		40	0
IOOUT	S374		5	2
IOOUT	S373		0	6
IB	S373	LS374	36	0
RH	29701		21	0
XDisp	S151	S00 S64 S374	26	0
IOOut	LS374		20	0
Y-Bus Sinks				
MAR	S373		70, 45	0
X-Bus	S374		5	2
LRot	25S10		12+worst X-Bus	0
SU	93422		45	5
IOOut	S373	clk early	3	7
StackP	25S09		5.5	3
AltUAddr	S257	25S09	20	0
YH-Bus Sinks				
MAR	S374		70	0

Chip Data

Chip	Prop. from DataIn or Clock Min.	Typ.	Max	Enable/Disable Min	Typ	Max	Setup	Hold
S00,10,20		3 nS	5 nS					
S74		6	9				3 nS	2 nS
S138 Dat&Sel		5	12					
S175		8	17				5	3
S240		4.5	7		6 nS	15 nS		
S241		6	9		6	15		
S257 Dat&Sel		5	15		5.5	19.5		
LS283		11	24					
S373		5	13		6	18	0	10
S374		8	17		5	18	5	2
LS374		19	34		10	36	20	0
LS399		21	32				20	0
25S09		8	17				5.5	3
25S10		5	12		5	21		
93422 Addr.Access		30	45		20	30		
Am29701 IDM2901A-1			60+carry					