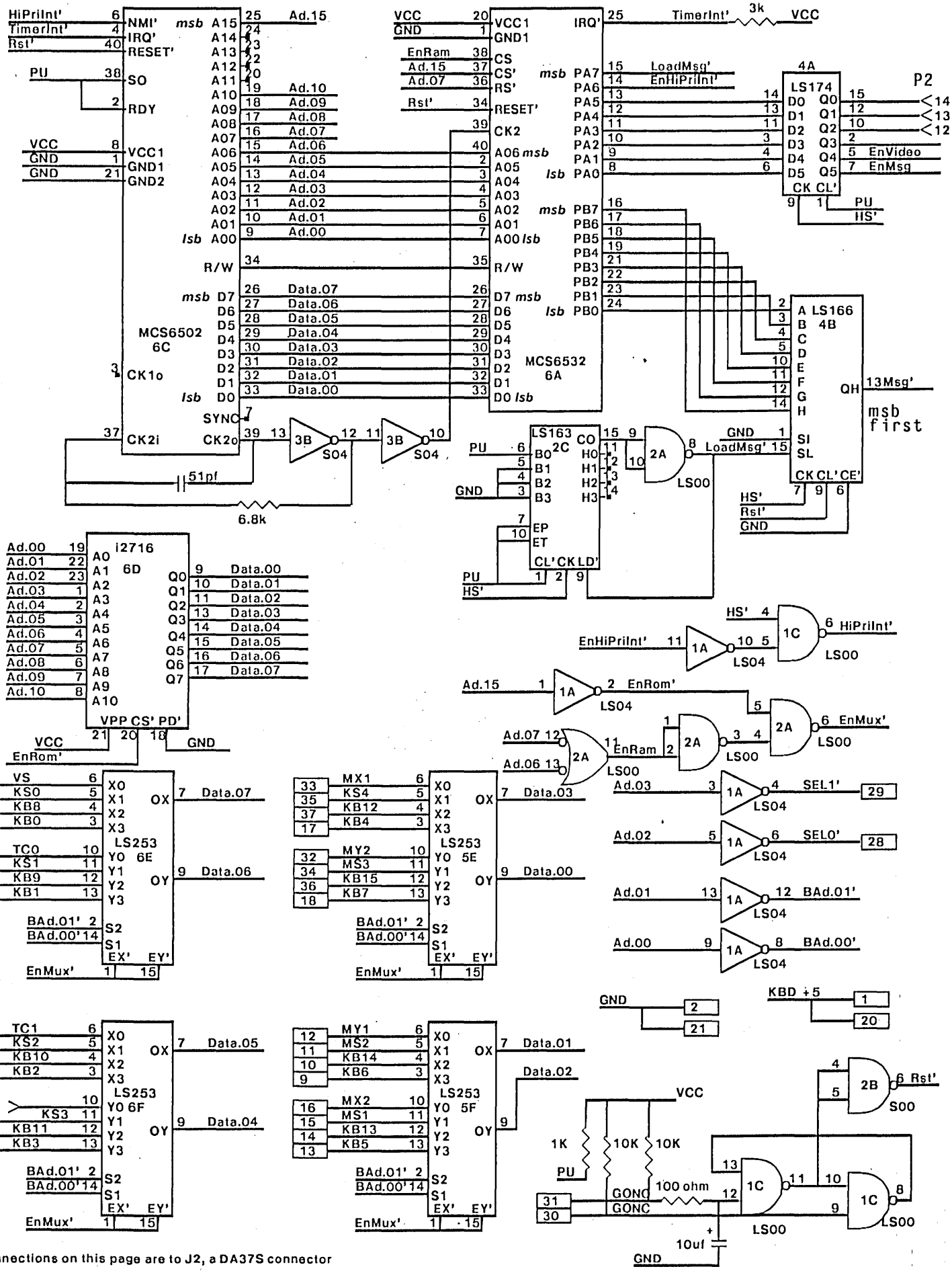
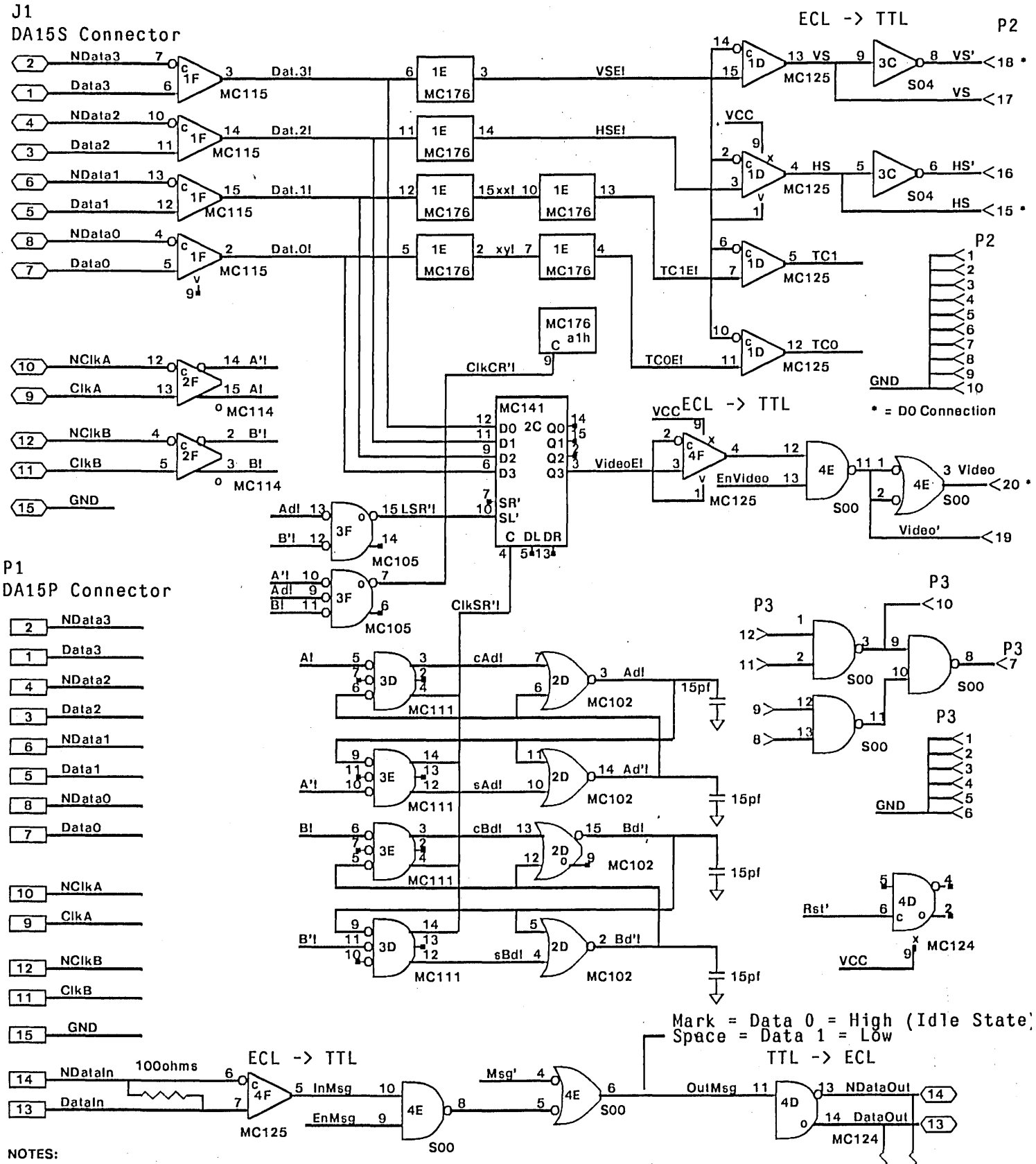


XEROX PARC	Project D0	7-Wire Terminal Interface Backchannel	File Terminal01.sil	Designer Thacker	Rev Gb	Date 12/26/79	Page 1

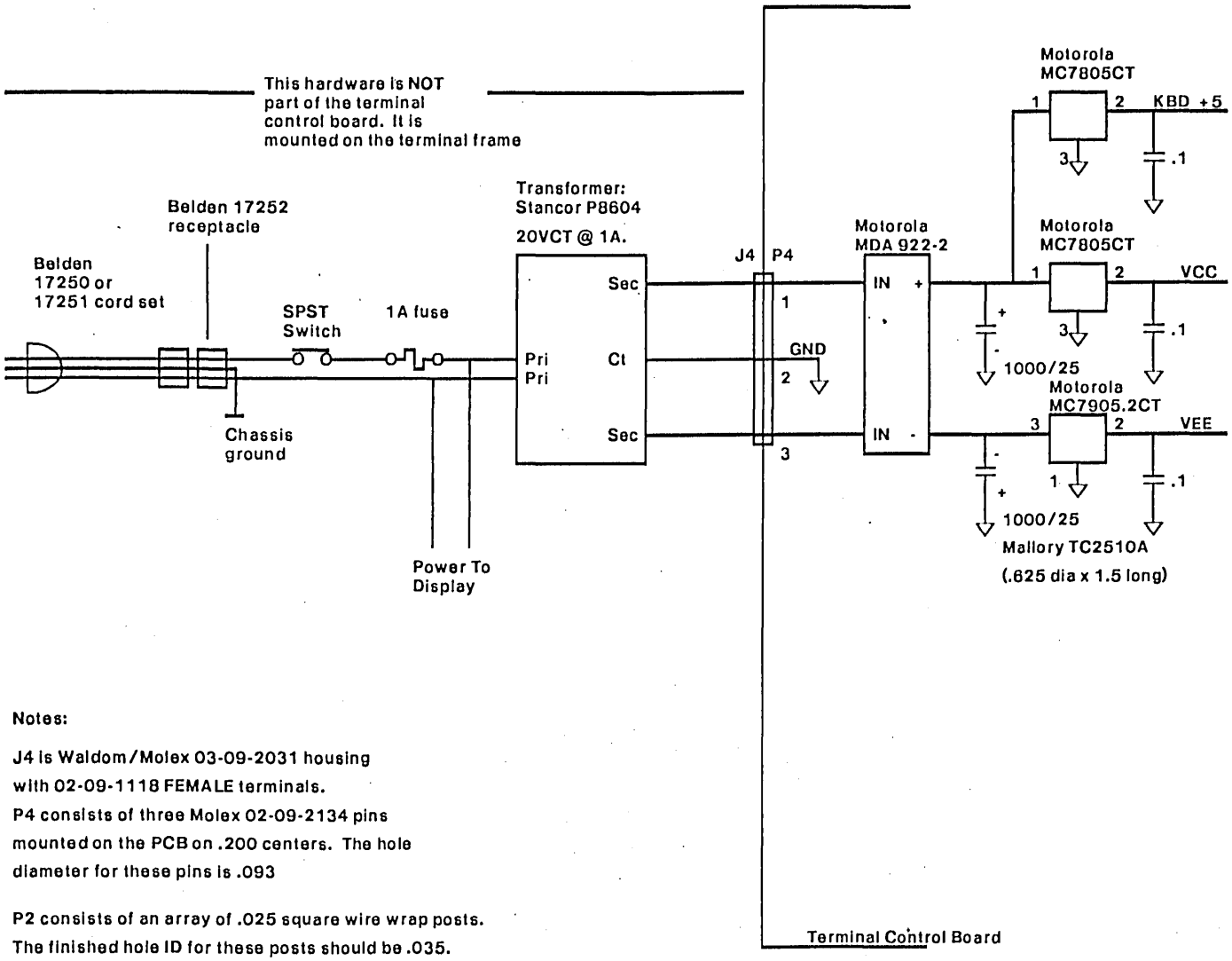


NOTES:

1) All signals with names of the form xxxl have 510ohm pulldown resistors to VEE (-5.2) (26 places)
2) P2 consists of wire-wrap posts on .100 centers
3) Ground, VCC, and VEE pins for ECL chips are as shown:

	GND	VEE	VCC
MC102, MC105, MC114, MC115 MC141	1,16	8	-
MC111	1,15,16	8	-
MC124, MC125	16	8	9
MC173, 176	16	8	-

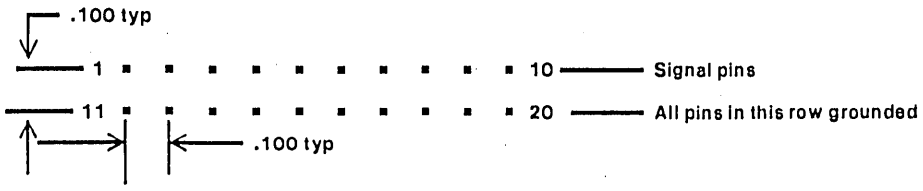
XEROX PARC	Project D0	7-Wire Terminal Interface Video Interface	File Terminal02.sil	Designer Thacker	Rev Gb	Date 12/26/79	Page 2



Notes:

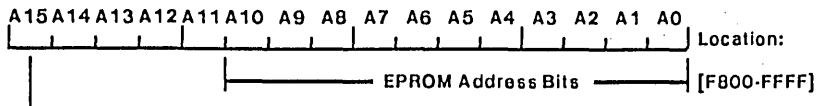
1) J4 is Waldom/Molex 03-09-2031 housing with 02-09-1118 FEMALE terminals. P4 consists of three Molex 02-09-2134 pins mounted on the PCB on .200 centers. The hole diameter for these pins is .093

2) P2 consists of an array of .025 square wire wrap posts. The finished hole ID for these posts should be .035. There should be two rows of pins. Only one row is shown on the logic diagrams; all pins in the other row are connected to ground:



3) VCC and VEE have one .01uf bypass capacitor per IC package.

XEROX PARC	Project D0	7-Wire Terminal Interface Power Supply	File Terminal03.sil	Designer Thacker	Rev GA	Date 4/14/79	Page 3



	RS'	A6	A5	A4	A3	A2	A1	A0		6532 Address Lines
0 X X X X X X X	0	A	A	A	A	A	A	A	[00-7F]	Ram Address (R/W)
	1	0	X	X	X	0	0	0	[80]	Output Register A (R/W)
	1	0	X	X	X	0	0	1	[81]	DDRA (R/W)
	1	0	X	X	X	0	1	0	[82]	Output Register B (R/W)
	1	0	X	X	X	0	1	1	[83]	DDRB
	1	0	X	X	IE	1	X	0	[84,8C]	Read Timer
	1	0	X	X	X	1	X	1	[85]	Read Interrupt Flag
	1	0	X	0	X	1	ED0	ED1	[84-87]	Write Edge Detect Control . (Data not used)
	1	0	X	1	IE	1	TP0	TP1	[94-97,9C-9F]	Write Timer
	1	1	X	X	SEL 0	SEL 1	M0	M1	[C0-CF]	Read Multiplexer Inputs

IE = Disable (0)/Enable (1) timer interrupt
TP = Timer Period: 0 = T, 1 = 8T, 2 = 64T, 3 = 1024T

ED = Edge Detect: 0,2 => Disabled
1 => Interrupt on PA7 negative edge
3 => Interrupt on PA7 positive edge

SEL0, SEL1 determine the keyboard word transmitted to the multiplexers

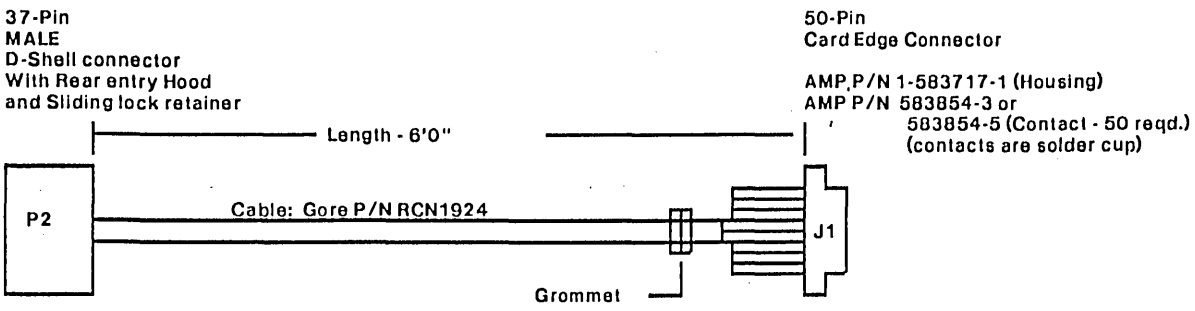
For the AltoII Microswitch keyboard, the bits are as follows:

Address: (BIT:)	7	6	5	4	3	2	1	0	
C3	VS	TC0	TC1	0	MX1	MX2	MY1	MY2	
C2	KS0	KS1	KS2	KS3	KS4	MS1	MS2	MS3	
C1	zero	K	-	P	/	\	lf	bs	(KB8-KB15)
C0	5	4	6	E	7	D	U	V	(KB0-KB7)
C9	Z	lshift	.	;	ret	←	del	none	(KB8-KB15)
C8	1	esc	tab	F	ctrl	C	J	B	(KB0-KB7)
C5	X	O	L	,	'	]	spare mid	spare top	(KB8-KB15)
C4	3	2	W	Q	S	A	9	I	(KB0-KB7)
CD	lock	space	[	=	rshift	spare bot	none	none	(KB8-KB15)
CC	R	T	G	Y	H	8	N	M	(KB0-KB7)

0's correspond to depressed keys

These bits end up in Alto memory as follows:

Address: (BIT:)	0	1	2	3	4	5	6	7	8	9	0	11	12	13	14	15
177034	5	4	6	E	7	D	U	V	zero	K	-	P	/	\	lf	bs
177035	3	2	W	Q	S	A	9	I	X	O	L	,	'	]	spare mid	spare top
177036	1	esc	tab	F	ctrl	C	J	B	Z	lshift	.	;	ret	←	del	none
177037	R	T	G	Y	H	8	N	M	lock	space	[	=	rshift	spare bot	none	none
177030									KS0	KS1	KS2	KS3	KS4	MS1	MS2	MS3



KEYBOARD J1	7-WIRE INTERFACE P1
1	27 BLU
2	9 Y
3	26 Y/BR
4	13 Y/R
5	14 Y/VIO
6	36 Y/GRY
7	24 Y/BLU
8	5 O
9	28 GRY
13	35 O/VIO
14	7 O/BLK
15	22 O/BLU
16	8 O/BRN
17	31 BLU/BLK
23	12 W/GRN
24	33 W/YEL
25	11 W/BRN
A	4 Y/BLK
B	3 VIO
C	17 GRN
D	18 Y/O
E	37 BRN
F	10 BLK (26 GAUGE-SMALL WIRE)
H	25 R
J	6 Y/GRN
K	29 W (26 GAUGE-SMALL WIRE)
N	2 BLK (20 GAUGE-LARGE WIRE)
P	21 W/VIO
S	23 O/R
T	30 BLU/BRN
U	1 W (20 GAUGE-LARGE WIRE)
V	20 O/GRN
W	32 W/BLU
X	16 W/O
Y	34 W/R
Z	15 W/BLK

KEYBOARD J1	7-WIRE INTERFACE P1
U	1 W (20 GAUGE-LARGE WIRE)
N	2 BLK (20 GAUGE-LARGE WIRE)
B	3 VIO
A	4 Y/BLK
8	5 O
J	6 Y/GRN
14	7 O/BLK
16	8 O/BRN
2	9 Y
F	10 BLK (26 GAUGE-SMALL WIRE)
25	11 W/BRN
23	12 W/GRN
4	13 Y/R
5	14 Y/VIO
Z	15 W/BLK
X	16 W/O
C	17 GRN
D	18 Y/O
V	20 O/GRN
P	21 W/VIO
15	22 O/BLU
S	23 O/R
7	24 Y/BLU
H	25 R
3	26 Y/BR
1	27 BLU
9	28 GRY
K	29 W (26 GAUGE-SMALL WIRE)
T	30 BLU/BRN
17	31 BLU/BLK
W	32 W/BLU
24	33 W/YEL
Y	34 W/R
13	35 O/VIO
6	36 Y/GRY
E	37 BRN

NOTES:

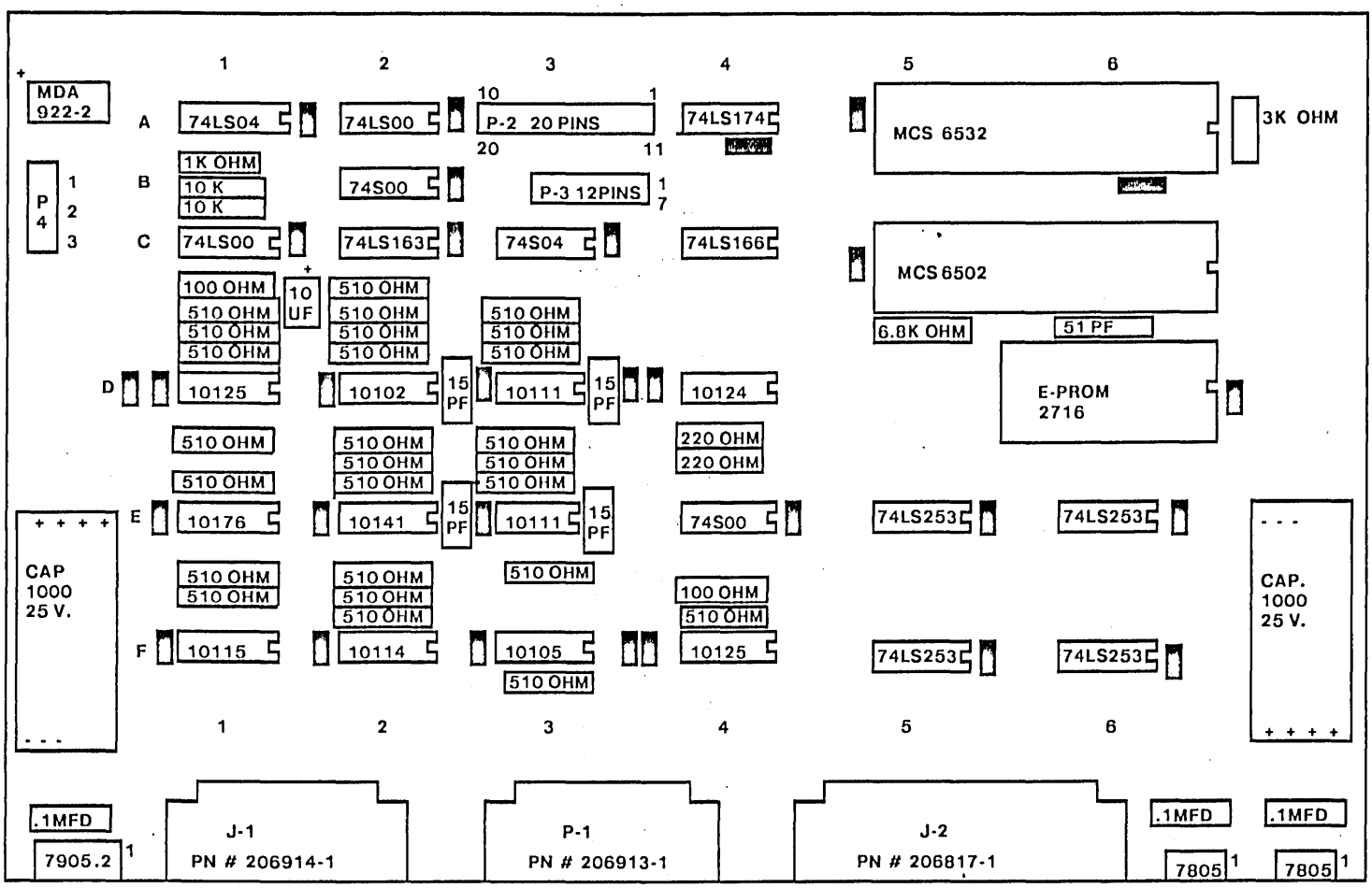
1. CABLE IS 6 FT. LONG +/- 4IN
2. W/GRY WIRE IS CUT OFF
3. O/GRY WIRE IS CUT OFF
4. CABLE IS (GORE PN # RCN1924)

XEROX PARC	Project D0	7-Wire Terminal Interface Keyboard-Terminal Int. Cable	File Terminalcable.sil	Designer Thacker/vest	Rev Gb	Date 12/26/79	Page 1

Changes to generate revision Gb (8/22/79 by CPT).

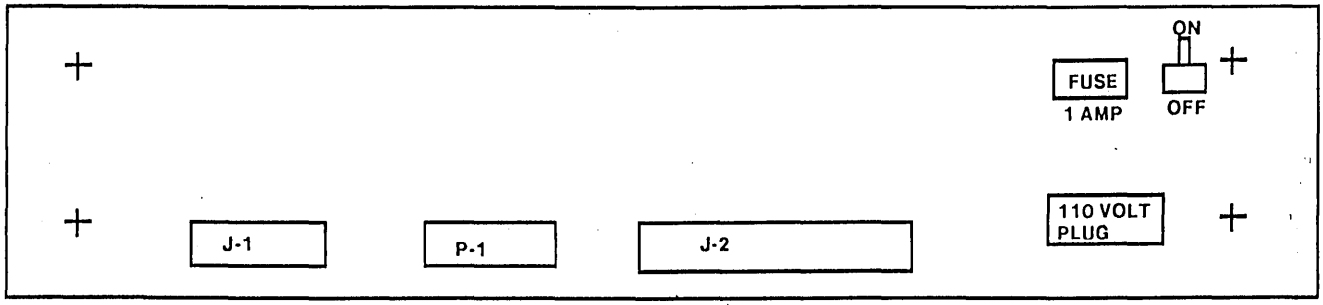
1) 6c.21 ← Vcc, 6c.18 ← Gnd (EPROM select signals).
2) 2b.3,4,5 ← Gnd, rather than Vcc.
3) 4c.6 ← Rst', rather than PU.
4) 4b.9 ← Rst', rather than PU.
5) Added an additional S00 connected to 6 additional pins of P2.
   This chip provides various flavors of sync via jumpers on P2.
6) Changed the way in which Rst' is generated (added power-up reset).
   Changed 2 1K resistors to 10K, added 100 ohm resistor and 10uf capacitor, added
   extra S00 section to generate Rst'.

NOTE: Changes 1-4 will be done to revision A boards via wiring, but 5 and 6 will not be done.
All changes will be incorporated into the revision B artwork.

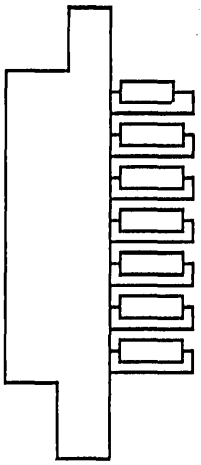


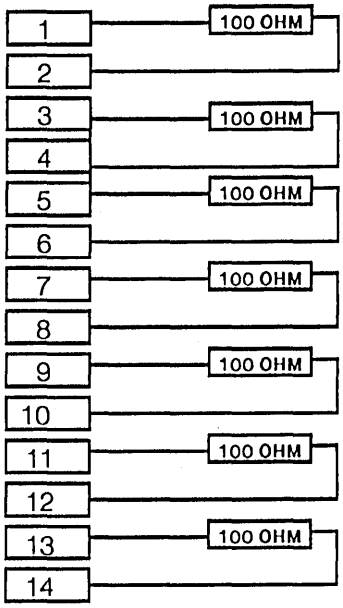
NOTES
1. ▬ IS A .01 UF CAP.
2. ▯ IS A .01 UF CAP.

BACKPANEL



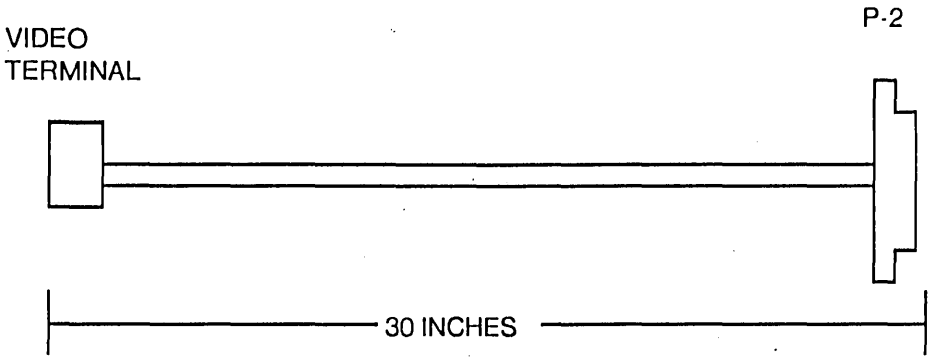
XEROX PARC	Project D0	7-Wire Terminal Interface	File Terminallayout.sil	Designer Thacker	Rev Gb	Date 12/26/79	Page 1





NOTES
RESISTORS ARE 100 OHM 1/4 WATT
TERMINATOR CONNECTOR IS DA 15S

XEROX PARC	Project D0	7-Wire Terminal Interface Terminator	File TerminalTerminator.sil	Designe Vest	Rev Gb	Date 12/26/79	Page 1



VIDEO CABLE D0

VIDEO TERMINAL		P-2 7- WIRE INTERFACE
8	YELLOW	20
10	BLACK	10
9	GREEN	18
10	BLACK	8
6	ORANGE	15
10	BLACK	6

VIDEO CABLE DORADO

VIDEO TERMINAL		P-2 7- WIRE INTERFACE
8	GREEN	20
10	BLACK	10
9	RED	18
10	BLACK	8
6	WHITE	15
10	BLACK	6

NOTES:
1. WIRE IS 26 AWG TWISTED PAIR
2. TEMINAL CONNECTOR IS AMPHENOL P/N 225-21031-101
3. P-2 CONNECTOR IS AMP 1-87456-6

5. COVER CABLE WITH SHRINK TUBING
6. ADD 100 OHM 1/4 WATT RESISTOR FROM PIN # 9 TO PIN # 1 ON THE TERMINAL END OF THE CABLE
7. ADD 100 OHM 1/4 WATT RESISTOR FROM PIN # 8 TO PIN # 1 ON THE TERMINAL END OF THE CABLE
8. ADD 100 OHM 1/4 WATT RESISTOR FROM PIN # 6 TO PIN # 1 ON THE TERMINAL END OF THE CABLE

XEROX PARC	Project D0	7-Wire Terminal Interface gTerminal cable	File Terminalvideocable.sil	Designer VEST	Rev Gb	Date 12/26/79	Page 1