SPECIFICATIONS

ABEL VERSION 3.0

GENERAL DESCRIPTION

ABEL™ is the industry-standard design software that lets you easily describe and implement logic designs in PLDs and PROMs. ABEL combines a natural, high-level design language with a language processor that converts logic descriptions to programmer load files. Programmer load files contain the information necessary to program and test programmable logic devices.

The ABEL design language lets you choose the type of description that is best suited to the logic being described, or the type of description you feel most comfortable with: high-level equations incorporating boolean operators, truth tables, state diagrams, or any combination of these. Meaningful names can be assigned to signals, signals can be grouped into sets, and macros can be used to simplify logic descriptions — all making your logic design easy to read and understand.

The ABEL language processor features powerful logic reduction, extensive syntax and logic error checking, and simulation of designs before a device is ever programmed. ABEL supports not only the most powerful and innovative complex PLDs just introduced on the market, but also many that haven't yet been released. This allows users to evaluate pre-released devices.

FEATURES

- 100% PLD manufacturer support, including more than 200 different PLD architectures
- Support for mainstream as well as advanced PLD architectures, including the Cypress 7C330, Lattice 39V18, ATMEL V750, AMD 29M16, Altera 1800, and TI PSG507
- Full documentation, including 600+ pages of User's Guide, Language Reference, Applications Guide, Systems Specific Information, and User Notes
- 75 design examples provided on disk or tape; 20 design examples provided in the Applications Guide
- Logic Diagram Package showing more than 180 PLD architectures, as well as fuse, pin, and node numbering
- Included with MS-DOS product package:
  - Personal Silicon Foundry™ (PSF™) integrated menu system
  - Terminal emulator utility to file transfer to and from mainframe computers, Data I/O® programmers, and other personal computers via the RS232 COM1 port (full or half duplex)
  - Powerful text editor, PC-Write® by Quicksoft
- PALASM (version 1 only) to ABEL conversion utility
- JEDEC file to ABEL source file decompiler; produces macrocell map (type of flip/flop, type of input, number of input terms, feedback path, reset and preset inputs)

- Boolean equations
- State machine diagram entry, using IF-THEN-ELSE, CASE, GOTO, and WITH-ENDWITH statements
- Truth tables to specify input to output relationships for both combinatorial and registered outputs
- High-level equation entry, incorporating the boolean operators used in most logic designs `(!,&,#,$,!$)`, arithmetic operators `(-,+,*,/,%,<<,>>)`, relational operators `(==,!=,<,<=,>,>=)`, and assignment operators `(=,:=)`
- Absolute fuse patching (i.e. you control the state of any fuse)
- Text librarian, allowing source statements to be stored, reducing execution of commonly used functions
- Four levels of logic reduction algorithms
- Powerful functional simulation, with six trace levels
- Standard JEDEC 3A format programmer load file for data transfer to logic programmers
- Automatic design documentation showing device utilization/listing, device pins available for input and output, the number of product terms used, and product terms still available for use
- Enhanced fusemap generator, handling new macrocells with configurable register types and feedback types
- Dot extensions, to permit greater flexibility for designing more complex devices, such as specifying register type with devices with dynamic register control
- "EZSIM," to shorten the simulation iteration loop, bypassing reduction and fusemap generator

DATA I/O

DATA I/O PRODUCT COMPATIBILITY

The Personal Silicon Foundry integrated menu system allows other powerful Data I/O programs to be integrated with ABEL:

- GATES,™ an interactive PLD design tool for complex designs. GATES includes partitioning and factoring capabilities for multiple and high-end PLD designs
- PLDtest,® used to fault grade PLD vectors, and automatically generate vectors for preloadable PAL®s
- PLD-CADAT,™ a program for integrating PLDs into a CADAT logic simulation. CADAT can then simulate the PLD as if it were a standard off-the-shelf part
- DASH-ABEL,™ a schematic capture interface that converts FutureNet® DASH™ schematic designs into ABEL source files; this allows PLDs to be designed using structural (schematics) as well as behavioral (equations) design entry
- PROMlink,™ a program that permits control of and communication with Data I/O programmers by means of a personal computer
- Logic Programmers: ABEL produces output for Data I/O's logic programmers, supporting the following data transfer formats:

JEDEC 3A ┐
├ PLDs

Motorola Exorcisor
Intel Intellec 8/MDS
Motorola Exormax
Intel MCS-86
├ PROMs

HARDWARE SPECIFICATIONS

Required Hardware Configuration

IBM® Personal System/2,™ IBM PC/XT/AT, Compaq Deskpro 386 or Tandy 3000 *

- DOS 3.1 or higher
- Minimum 384K RAM
- Single 5.25" or 3.5" double-sided, double-density disk drive (two disk drives or hard drive recommended)
- Includes PC-Write by Quicksoft
- Copy protected

VAX-VMS

- VMS 4.6 or higher operating system
- Distributed on ANSI-format, 1600 BPI magnetic tape

VAX-Unix®

- Unix Berkeley 4.3 based operating system
- Distributed on TAR-format, 1600 BPI magnetic tape

Sun-2 or Sun-3™

- Operating system 3.4 or higher
- Distributed on TAR-format, ¼" cartridge tape

Apollo

- Aegis 9.5 or higher
- Distributed on WBAK format, ¼" cartridge tape

* MS-DOS versions only use 640K of memory. This may restrict large truth tables in PROMs or state machine designs.

PROGRAMMABLE LOGIC DEVICE MANUFACTURERS SUPPORTED

Altera
Advanced Micro Devices/MMI
ATMEL
Cypress Semiconductor
EXEL Microelectronics
Fairchild Semiconductor
Gould
Harris
Intel
International CMOS Technology
Lattice Semiconductor
National Semiconductor
PLX
Ricoh
Samsung Semiconductor
SEEQ Technology
SGS-Thomson Microelectronics
Signetics
Sprague Solid State
Texas Instruments
VLSI Technology

PROM MANUFACTURERS SUPPORTED

ABEL supports all of the PROM, EPROM, and EEPROM manufacturer's devices up to 32K bits.

Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046, Redmond, WA 98073-9746, U.S.A. (206) 881-6444/Telex 15-2167
Data I/O Canada 6725 Airport Road, Suite 302, Mississauga, Ontario L4V 1V2 (416) 678-0761/Telex 06968133
Data I/O Europe World Trade Center, Strawinskylaan 633, 1077 XX Amsterdam, The Netherlands +31 (0)20-6622866/Telex 16616 DATIO NL
Data I/O Japan Sumitomoseimei Higashishinbashi Bldg., 8F, 2-1-7, Higashi-Shinbashi, Minato-ku, Tokyo 105, Japan (03) 432-6991/Telex 2522685 DATAIO J

DATA I/O