PLDtest

AUTOMATIC FAULT GRADING AND TEST VECTOR GENERATION FOR DEVICE VERIFICATION.

DATA I/O

THE PRACTICAL ROUTE TO TESTABILITY.

In the era of VLSI design, a single programmable logic device (PLD) can replace the dozens of gates that once covered an entire board. The designer, however, can no longer physically probe gates inside the device to find failures. Instead, the device's internal faults must be apparent through output pins. A comprehensive set of test vectors is therefore required to fully test a PLD's function before it's loaded onto the board.

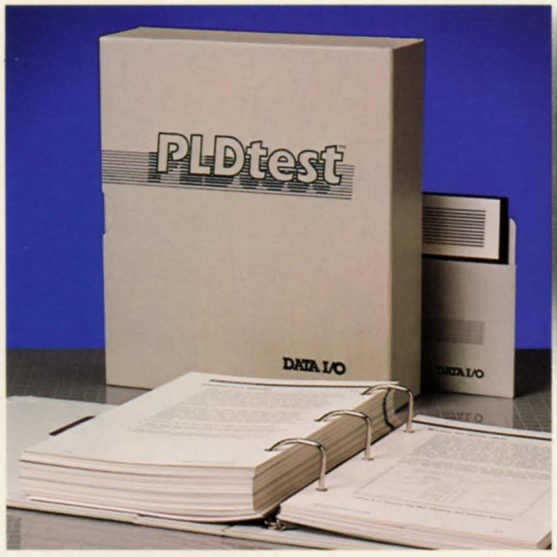
The case for designing testable PLDs is strong: Each device can be fully tested when programming on the production line, reducing board failures and lowering production costs. Yet, manually generating and analyzing test vectors has become nearly impossible, particularly with very large PLDs.

Data I/O's PLDtest™ gives design and test engineers the tools they need to analyze designs and to test the programmed devices. It can also automatically generate test vectors for combinatorial or registered devices with preload. For the design engineer, PLDtest measures the testability of a circuit design, locates untestable portions for design debugging, and produces appropriate documentation. For the test engineer, creating fully-testable devices results in improved circuit reliability. With Data I/O's PLDtest, designing PLDs with a complete set of test vectors has become a practical reality.

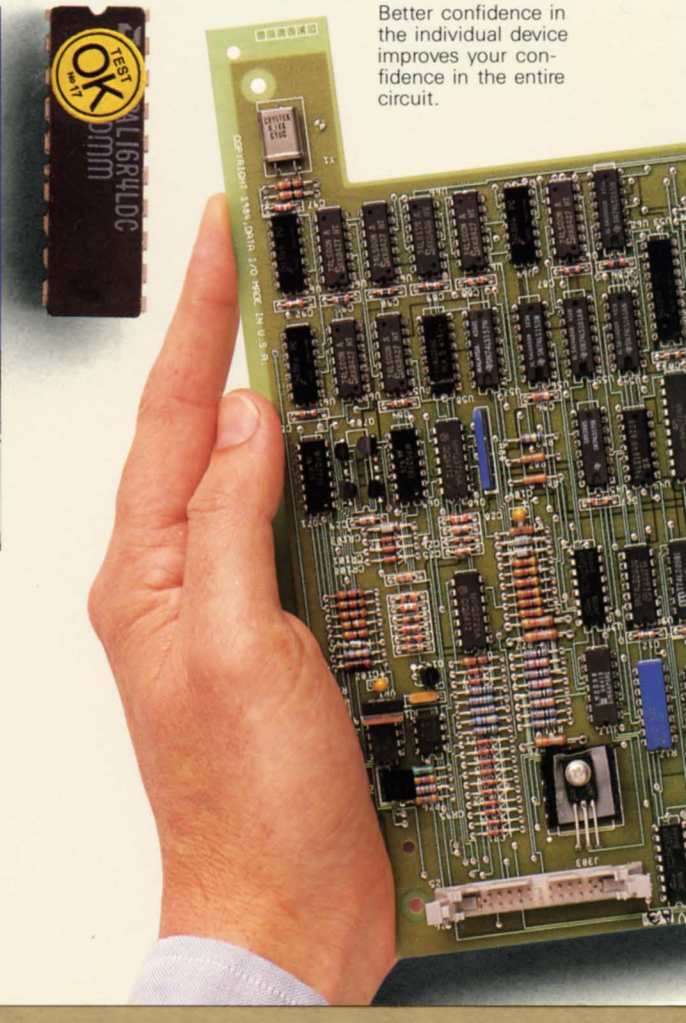
A TRIO OF SOPHISTICATED CAPABILITIES. PLDtest performs fault grading, test vector generation and testability analysis. Fault grading determines the percentage of coverage provided by the test vectors you have created during the design process. PLDtest then automatically generates supplemental or completely new vectors to cover the physical elements of combinatorial devices and registered devices with preload. Finally, summary reports help you analyze the testability of your device by indicating how much is testable and by pinpointing untestable areas.

GRADING YOUR DESIGN'S TESTABILITY. During the development phase, logic designers write test vectors which test the logical function of their design. PLDtest's fault grading function examines these engineer-created test vectors, in conjunction with device information, to determine how many potential faults in the device these vectors will test. You can use this information to write more extensive design vectors covering more faults.

To perform fault grading, PLDtest actually simulates operation of the design. It applies the inputs in each test vector to the design and records the internal device states. It then traces a path backward from each output pin to determine if potential faults can be detected with that pin.



Data I/O's PLDtest dramatically decreases test vector generation time—from days to just minutes.



Better confidence in the individual device improves your confidence in the entire circuit.

GENERATING TEST VECTORS AUTOMATICALLY. PLDtest dramatically decreases test vector generation time — from days to just minutes. Human errors associated with manual methods are eliminated as well.

PLDtest can create new test vectors or supplement engineer-supplied design vectors by automatically generating new test patterns. These cover the operation of the device's physical elements such as AND gates, OR gates, fuses and registers.

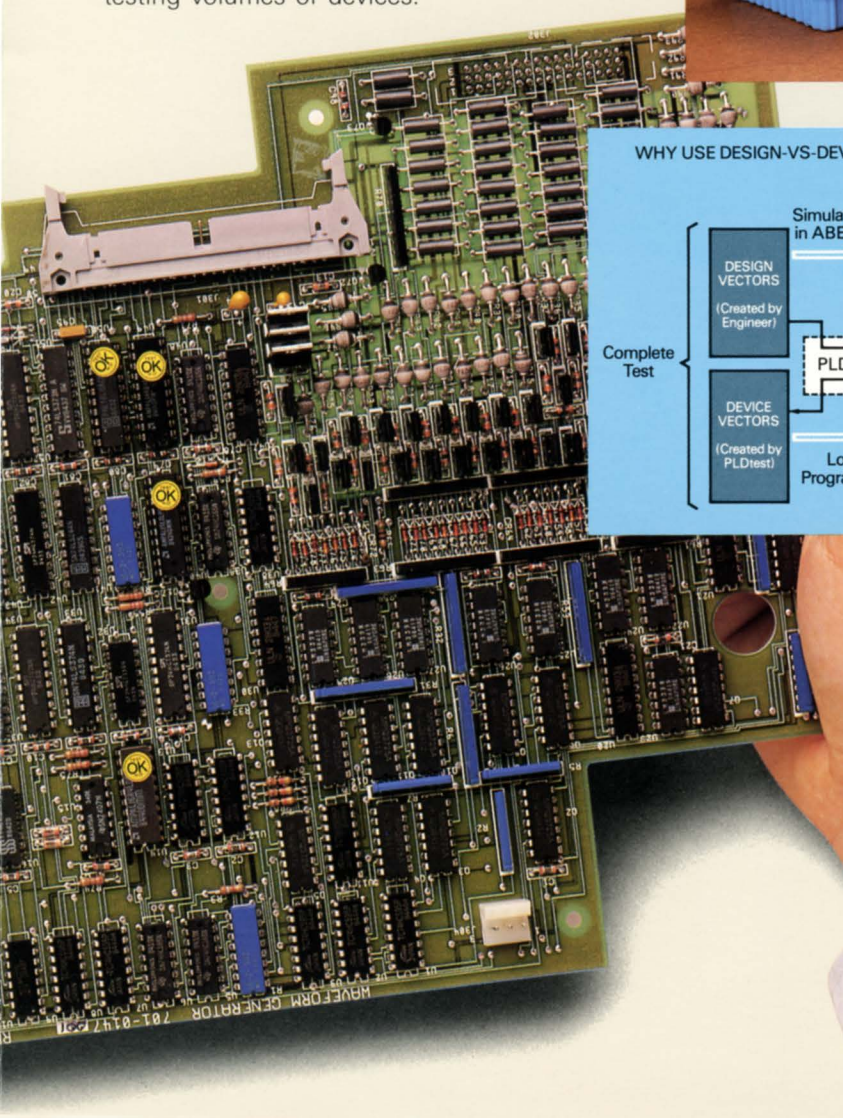
The capability to automatically generate device test vectors turns a time-consuming manual chore into a simple, accurate process.

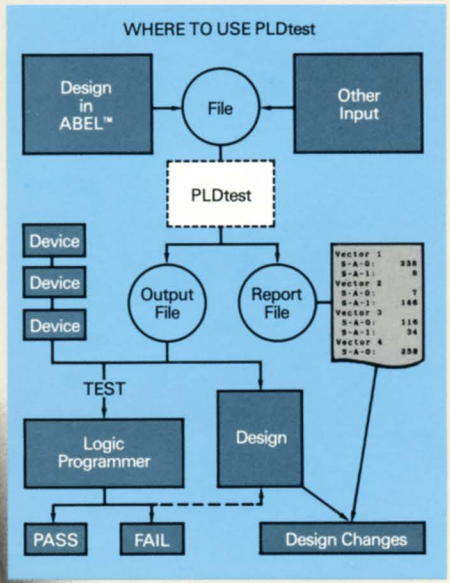
A REPORT FILE SUMS UP DEVICE TESTABILITY. PLDtest generates a report file which contains various performance statistics and a summary of fault coverage. In addition, this report indicates all the faults each vector detects.

Designers can use this list of faults covered and summary of detected and undetected faults as essential feedback during the design phase. Within the production environment, test vectors created by PLDtest are used directly in the logic programmer for programming and testing volumes of devices.

THOROUGH TESTING FOR HIGHER CONFIDENCE IN PRODUCTION. With the combination of your design vectors and those automatically generated by PLDtest, you can thoroughly test each programmable logic component before it is loaded on the board. Comprehensive testing ensures that each copy of your original device is fully functional. And better confidence in the individual device improves your confidence in the entire circuit.

For programming and testing volumes of devices, test vectors created by PLDtest can be used directly in Data I/O's 60H Production Logic Programmer, which is compatible with most handlers.





Chances are that PLDtest is compatible with your current computer. PLDtest runs on MS-DOS-compatible personal computers such as the IBM® PC. It also runs on the DEC® VAX, and other versions are coming.

Because one of the available PLDtest output formats conforms to JEDEC Standard 3, it can be downloaded to compatible logic programmers, such as Data I/O's models 60A, 60H or 29B with LogicPak™.

SOFTWARE UPDATE SERVICE. Joining Data I/O's Software Update Services assures you of prompt software updates for new devices and enhancements.

Data I/O has sales and sales representative offices worldwide to answer your questions or problems.

GENERAL SPECIFICATIONS

COMPATIBLE COMPUTERS: Personal computer (distributed on double-sided, double-density 5-1/4" floppies).
MS™-DOS or PC-DOS operating systems.
256k with two disk drives, recommended minimum.
DEC VAX (distributed on 1600 bpi magnetic tape).
VMS™ operating system.
UNIX™ operating system.

INPUT FORMATS: Choice of JEDEC Standard 3 programmer load file or an ABEL output file.

OUTPUT FORMATS: Choice of a JEDEC Standard 3, ABEL "include" file, or a generic file that can be adapted to any test equipment.

DEVICES SUPPORTED: Most 20-, 24-, and 40-pin PAL®s. Automatic test vector generation for registered devices requires preload capability.

PROMlink: With Data I/O's PROMlink software driver, you can operate Data I/O's programmers from an IBM PC. This software package delivers the simplicity of a menu-driven operation and data file management.

ABEL: ABEL compiles logic designs for virtually all PLDs, including PALs, PROMs, FPLAs, FPLSs and PLEs. It also lets you express your design in any combination of truth tables, state diagrams or Boolean equations. ABEL is also available for VAX, VALID™, SUN™ and Apollo™ systems.

DASH-ABEL INTERFACE: The DASH-ABEL Interface allows FutureNet's Dash 1 or 2 to act as schematic entry for Data I/O's ABEL programmable logic design tool.

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