DR11-C
general device
interface manual

DEC-11-HDRCA-C-D

DR11-C
general device
interface manual

digital equipment corporation · maynard, massachusetts

CONTENTS

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The DR11-C is a general-purpose interface between the PDP-11 Unibus and a user's peripheral (Figure 1-1). The DR11-C provides the logic and buffer register necessary for program-controlled parallel transfers of 16-bit data between a PDP-11 System and an external device. The interface also includes status and control bits that may be controlled by either the program or the external device for command, monitoring, and interrupt functions. The DR11-C is software compatible with the DR11-A.

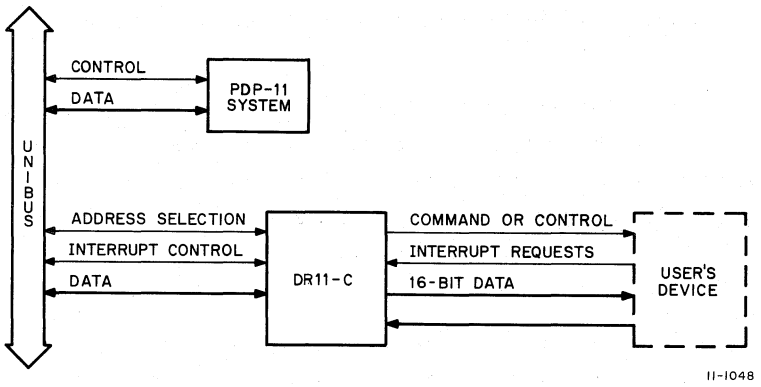


Figure 1-1 System Block Diagram

1.2 GENERAL DESCRIPTION

The DR11-C interface consists of three functional sections: address selection logic, interrupt control logic, and device interface logic.

The address selection logic determines if the interface has been selected for use, which register is to be used, if a word or byte operation is to be performed, and what type of transfer (input or output) is to be performed.

The interrupt control logic permits the interface to gain bus control and perform program interrupts to specific vector addresses. The interrupt enable bits are under program control; the interrupt bits are under control of the user's device.

The DR11-C interface logic consists of three registers: control and status, input buffer, and output buffer. Operation is initialized under program control by addressing the DR11-C to specify the register and the type of operation to be performed.

The following accessories are available for interfacing and may be ordered separately:

a. BC08R (Berg-to-Berg) flat cable. Available in lengths of 1, 6, 8, 10, 12, 20, and 25 feet. When ordering, the dash number indicates the desired cable length; e.g., BC08R-1 or BC08R-25.

b. M971 connector board. A single-height by 8-1/2 in. board that brings the signals from one Berg connector to the module fingers.

c. BC11K-25 cable. Consists of a 20 twisted-pair cable with a Berg connector on one end only. Available in 25 ft lengths.

d. H856 Berg connector. Includes an H856 Berg connector and 40 pins. Crimping tools are available from: Berg Electronics, Inc., New Cumberland, Pa. 17070.

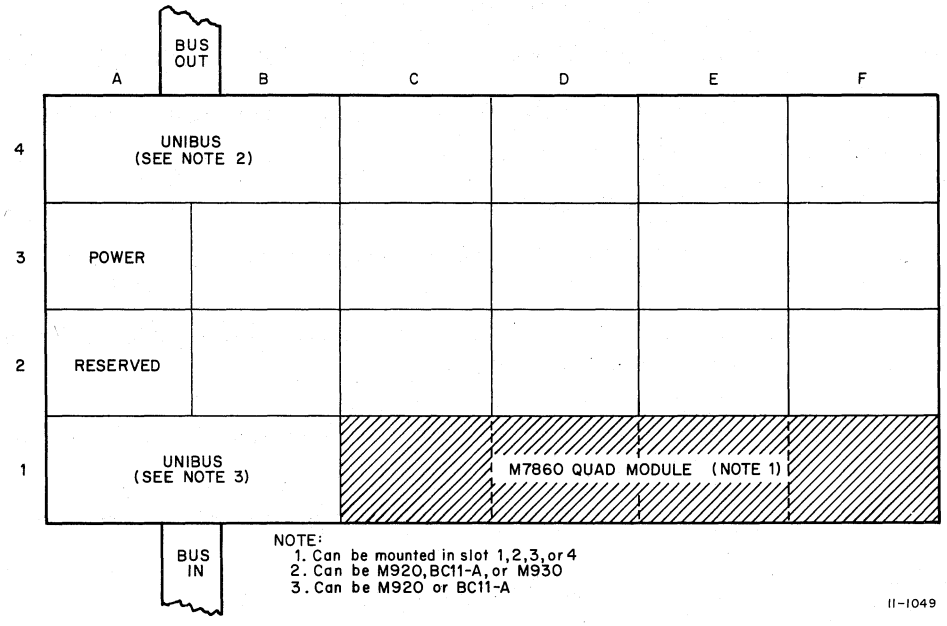


Figure 1-2 Typical M7860 Quad Module Mounting

CHAPTER 2
SOFTWARE INTERFACE

2.1 SCOPE

This chapter presents a detailed description of the three DR11-C registers (Figure 2-1). These registers are assigned bus addresses and can be read or loaded (with the exceptions noted) using any instruction that refers to their addresses. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following: issuing a programmed RESET instruction; depressing the START switch on the processor console; or the occurrence of a power-up or power-down condition of a system power supply.

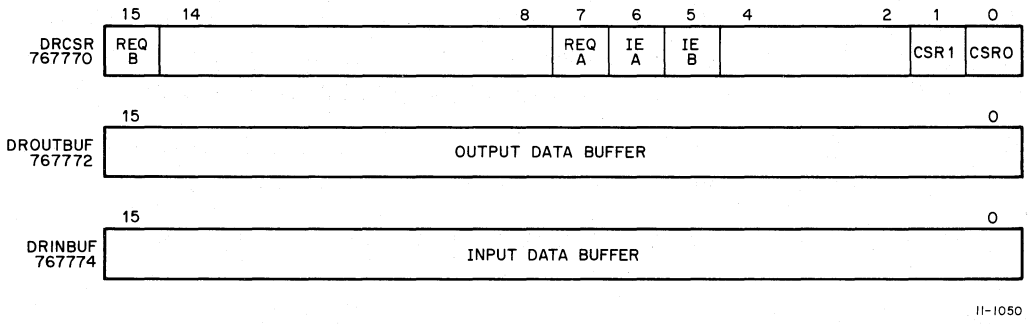


Figure 2-1 DR11-C Register Assignments

The device registers and associated addresses are listed in Table 2-1. Note that these addresses can be changed by altering the jumpers on the address selection logic. However, any programs or other software referring to these addresses must also be modified accordingly if the jumpers are changed. Paragraph 2.5 discusses priority levels and the addressing scheme when more than one DR11-C is used.

Table 2-1
Standard DR11-C Register Assignments

Register	Mnemonic*	Address
Control and Status Register	DRCSR	767770
Output Buffer	DROUTBUF	767772
Input Buffer	DRINBUF	767774

* First two letters of mnemonic (DR) refer to DR11-C interface; the remaining letters represent the mnemonic of a specific register.

Table 2-2
DRCSR Bit Assignments

Bit	Name	Meaning and Operation
15	REQUEST B	This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program. When used as an interrupt request, it is set by the external device and initiates an interrupt provided the INT ENB B bit (bit 05) is also set. When used as a flag, this bit can be read by the program to monitor external device status. When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 01). This permits checking interface operation by loading a 0 or 1 into CSR1 and then verifying that REQUEST B is the same value. Read-only bit. Cleared by INIT.
14–08	Unused	Not Applicable
07	REQUEST A	Performs the same function as REQUEST B (bit 15) except that an interrupt is generated only if INT ENB A (bit 06) is also set. When the maintenance cable is used, the state of REQUEST A is identical to that of CSR0 (bit 00). Read-only bit. Cleared by INIT.
06	INT ENB A	Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST A (bit 07) becomes set. Can be loaded or read by the program (read/write bit). Cleared by INIT.
05	INT ENB B	Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST B (bit 15) becomes set. Can be loaded or read by the program (read/write bit). Cleared by INIT.
04–02	Unused	Not Applicable
01	CSR1	This bit can be loaded or read (under program control) from the Unibus and can be used for a user-defined command to the device (appears only on Connector No. 1). When the maintenance cable is used, setting or clearing this bit causes an identical state in bit 15 (REQUEST B). This permits checking operation of bit 15 which cannot be loaded by the program. Read/write bit (can be loaded or read by the program). Cleared by INIT.
00	CSR0	Performs the same function as CSR1 (bit 01) but appears only on Connector No. 2. When the maintenance cable is used, the state of this bit controls the state of bit 07 (REQUEST A). Read/write bit. Cleared by INIT.

CHAPTER 3
USER INPUT/OUTPUT SIGNALS

3.1 SIGNAL LIST

Tables 3-1 and 3-2 list the signals available to the user's device. Input loading refers to the number of TTL unit loads the input signal must drive. A unit load is defined as:

$2.4V \leqslant$ Input high voltage $\leqslant 5.0V$ @ 40 μA
$0.0V \leqslant$ Input low voltage $\leqslant 0.4V$ @ -1.6 mA

where current flow is defined as positive into the driven gate. All inputs are one standard TTL unit load and have diode protection clamps to ground and +5V.

Table 3-1
User Input Signals

Name	No. of Signals	Loading	Description
IN00 through IN15	16	1 each	Data input from user device. The levels presented on these lines can be examined by reading the input buffer register (DRINBUF) with an instruction such as MOV DRINBUF, R0. This data is transferred to the Unibus when the DR11-C responds to a DATI bus cycle. Because the input buffer register consists of gating logic, the device must hold the IN lines asserted until read onto the Unibus. This is indicated by the trailing edge of the DATA TRANSMITTED pulse. Logic levels are: +3V = 1; 0V = 0.
REQUEST A, B	2	1 each	Two request lines that can be asserted (+3V) by the external device to initiate an interrupt sequence or to generate a flag that can be tested by the program. These request lines must be levels that are held asserted for the entire interrupt sequence and would normally be cleared by NEW DATA READY or DATA TRANSMITTED. Although the external device controls these request lines, an interrupt sequence can only be started by the program because of the associated interrupt enable (IE) bits under program control. Methods of generating these request levels in the user's device are described in Chapter 6. Logic levels are: +3V = 1; 0V = 0.

All outputs are TTL levels capable of driving eight unit loads with the following exceptions:

NEW DATA READY – 30 unit loads
DATA TRANSMITTED – 30 unit loads
INIT – a common signal on both connectors which is driven by one 30-unit load driver

The NEW DATA READY and DATA TRANSMITTED signals are described more fully in Paragraph 3.2.

3.2 VARIABLE SIGNALS

The NEW DATA READY signal is a positive pulse which loads the output buffer register on the leading edge of the pulse. The DATA TRANSMITTED signal is also a positive pulse and is generated when the input buffer register is read by a DATI sequence.

Both of these signals are approximately 400 ns in duration. However, this duration can be changed by adding an external capacitor between back panel pin EB1 and ground. Some typical capacitor values and resultant pulse widths are listed in Table 3-3. The effect of the additional capacitance results in lengthening the bus cycle. This is, therefore, a factor in NPR latency considerations.

Table 3-3
External Capacitor Values

External Capacitor	NEW DATA READY	DATA TRANSMITTED
none	350 ns	450 ns
470 pF	500 ns	600 ns
820 pF	600 ns	750 ns

3.3 CONNECTORS

Figure 3-1 illustrates the layout for the M7860 module, the Berg connectors, and the M971 connector modules referenced in Tables 3-4 and 3-5.

The input and output signals are listed in Table 3-4 and indicate the Berg pin on the M7860 module. Table 3-5 lists all pin connections (in pin number order) for the Berg header on the M7860 module, the Berg header on the M971, and the M971 board pins. Figure 3-2 illustrates the physical location of the pins on the Berg connector.

Table 3-6 shows connections with a BC11K-25.

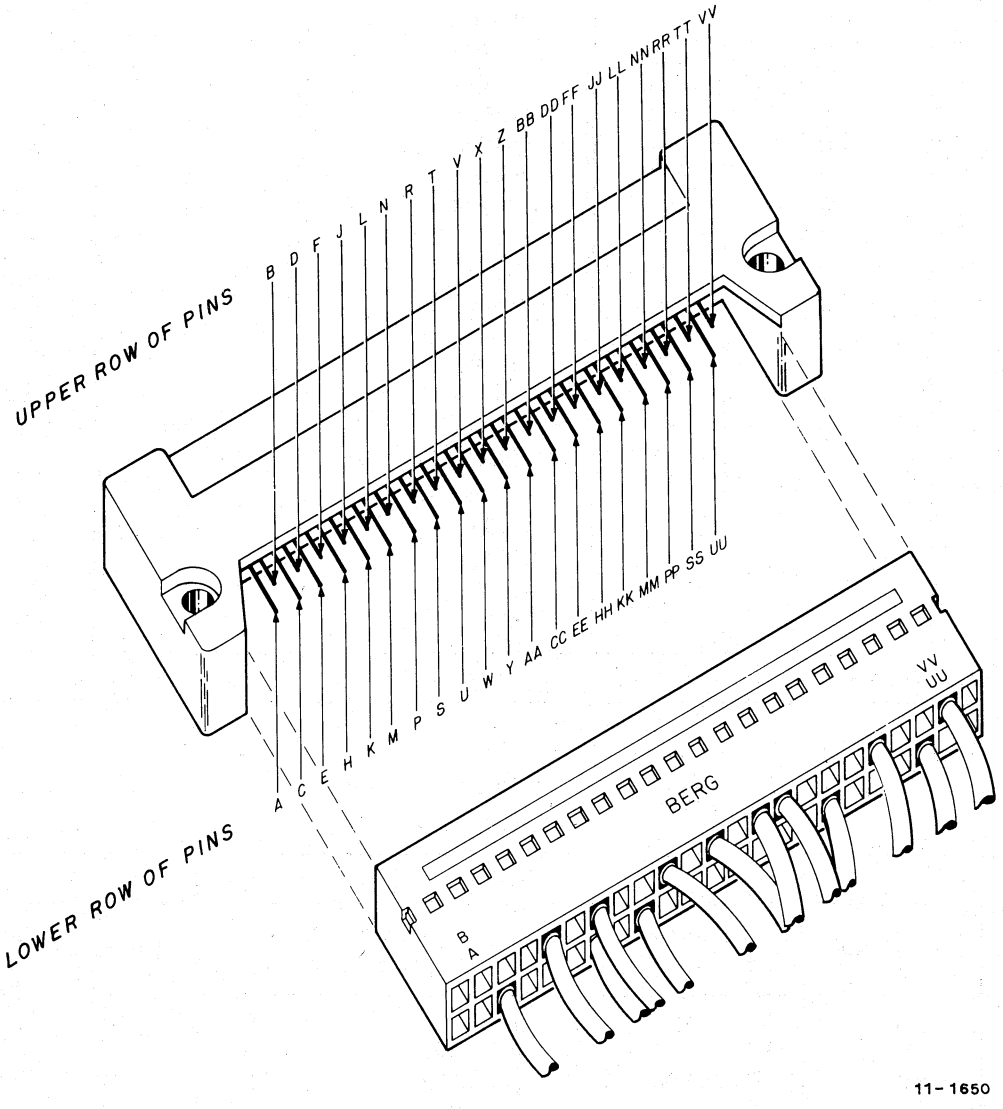


Figure 3-2 Berg Connector

Table 3-5 (Cont)
Pin Connections

M971		M7860				M971	
Board	Berg Header	Connector No. 2 Pin	Name	Name	Connector No. 1 Pin	Berg Header	Board
P1	R	EE	IN06	OUT06	R	EE	F2
N2	S	DD	GND	GND	S	DD	H1
N1	T	CC	IN07	OUT07	T	CC	H2
M2	U	BB	IN03	OUT03	U	BB	J1
M1	V	AA	GND	GND	V	AA	J2
L2	W	Z	IN08	OUT08	W	Z	K1
L1	X	Y	IN09	OUT09	X	Y	K2
K2	Y	X	GND	GND	Y	X	L1
K1	Z	W	IN10	OUT10	Z	W	L2
J2	AA	V	IN11	OUT11	AA	V	M1
J1	BB	U	IN12	OUT12	BB	U	M2
H2	CC	T	GND	GND	CC	T	N1
H1	DD	S	REQ B	CSR1	DD	S	N2
F2	EE	R	GND	GND	EE	R	P1
F1	FF	P	IN13	OUT13	FF	P	P2
E2	HH	N	IN14	OUT14	HH	N	R1
E1	JJ	M	IN15	OUT15	JJ	M	R2
D2	KK	L	GND	GND	KK	L	S1
D1	LL	K	CSR0	REQ A	LL	K	S2
C2	MM	J	GND	GND	MM	J	T1
C1	NN	H	IN02	OUT02	NN	H	T2
B2	PP	F	OPEN	GND	PP	F	T1
B1	RR	E	IN02	OUT02	RR	E	T2
A2	SS	D	OPEN	GND	SS	D	V1
A1	TT	C	DATA TRANS.	OPEN	TT	C	V2
A2	UU	B	OPEN	GND	UU	B	U1
A1	VV	A	OPEN	NEW DATA RDY	VV	A	U2

Table 3-6
BC11K-25 Connections

Twisted Pair	Color	Pin	Connector No. 1	Connector No. 2
black/white-orange	black	A	OPEN	OPEN
	wh-org	B	OPEN	OPEN
black/white-yellow	black	C	OUT00	DATA TRANS.
	wh-yel	D	OPEN	OPEN
black/white-grey	black	E	OPEN	IN02
	wh-gry	F	OPEN	OPEN
black/white-red	black	H	OPEN	IN02
	wh-red	J	GND	GND
black/white-green	black	K	OUT01	CSR0
	wh-grn	L	OUT04	GND

(continued on next page)

CHAPTER 4
THEORY OF OPERATION

4.1 INTRODUCTION

This chapter provides a detailed description of the DR11-C interface. The interface may be divided into five major functional areas: selection logic, interrupt logic, status register, input buffer register, and output buffer register. A block diagram of the DR11-C is shown in Figure 4-1. Each of the functional areas is covered separately in subsequent paragraphs. The basic purpose of each of these areas is as follows:

Selection Logic	Determines if the DR11-C interface has been selected for use, which register is to be used, if a byte or word operation is required, and what type of transfer (DATI or DATO) is to be performed.
Interrupt Logic	Permits the DR11-C to gain bus control and perform a program interrupt. Priority level of bus request (BR) line may be changed by the user.
Status Register	A 16-bit register used to provide user-defined command and monitoring functions; includes interrupt enable bits. Four bits are under program control, two are under device control. Some of the bits in this register can be used for communication if the DR11-C is part of an interprocessor buffer.
Input Buffer Register	A 16-bit read-only buffer that receives data from the user's device for transmission to the Unibus.
Output Buffer Register	A 16-bit read/write register that can be loaded or read from the Unibus. Once the buffer has been loaded, the data is available for transfer to the user's device.

4.2 ADDRESS SELECTION

The address selection logic (drawing DR-4) decodes the incoming address information from the bus and provides four select line (three used) and three gating signals that determine which register has been selected and whether it is to perform an input or output function. Jumpers on the logic are arranged so that the module responds only to standard device register addresses 767770, 767772, 767774, and 767776 (jumper in bit position 12). Although these addresses have been selected by DEC as the standard assignments for the DR11-C interface, the user may change the jumpers to any address desired. However, any MainDEC program (or other software) that references the DR11-C standard address assignments must also be modified if other than the standard assignments are used.

The first five octal digits of the address (76777) indicate that the DR11-C has been selected as the device to be used. The final octal digit, consisting of address lines A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. The two mode control lines, C1 and C0, determine whether the selected register is to perform an input or output function.

Address lines A02 and A01 are decoded to produce one of four select line signals (Table 4-1) which select the register to be used. The two mode control lines produce IN and OUT gating signals (Table 4-1) which determine whether the bus cycle is a DATI or DATO. Note that an IN gating signal is provided for all three registers because all three can be read from the bus. However, an OUT gating signal is not provided for the input buffer register because it cannot be loaded from the bus.

Table 4-1
Gating and Select Line Signals

Select Line	Gating Signal	Function Selected	Reg.	Bus Cycle
0	IN	status to bus	DRCSR	DATI
2	IN	output buffer to bus	DROUTBUF	DATI
4	IN	input buffer to bus	DRINBUF	DATI
0	OUT LOW	bus to status	DRCSR	DATOB
0*	OUT HIGH	unused	–	DATOB
2	OUT LOW, OUT HIGH	bus to output buffer	DROUTBUF	DATO or DATOB
4*	OUT LOW, OUT HIGH	unused	–	DATO or DATOB
6*	IN or OUT	unused	–	DATI, DATO, or DATOB

* Executing any of the above operations referred to as unused does not result in an error trap or any other bus indication. The function is simply not performed.

There are two OUT signals, OUT LOW and OUT HIGH, that refer to the low and high byte of a register, respectively. Both OUT LOW and OUT HIGH are provided for the output buffer register which can be loaded with a full word from the bus. Only OUT LOW, however, is provided for the status register because the high byte contains no bits which can be written into.

The basic functions of the IN and OUT signals are:

a. IN – DR11-C responds by placing data from the selected register onto the bus.
b. OUT LOW – DR11-C loads low byte of selected register.
c. OUT HIGH – DR11-C loads high byte of selected register.

Note that both OUT LOW and OUT HIGH are active when a full 16-bit word is being loaded into a register.

4.2.1 Inputs

A simplified block diagram of the address selection logic is shown in Figure 4-2. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the DR11-C interface is used, an OUT transfer is a transfer of data out of the master (usually the processor) and into the device. Similarly, an IN transfer is the operation of the interface furnishing data to the Unibus.

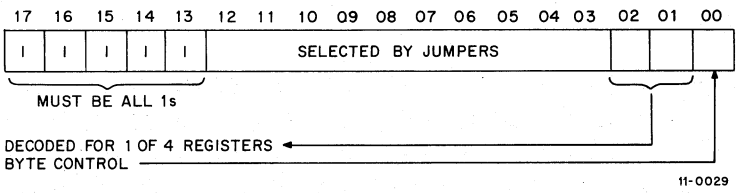


Figure 4-3 Interface Select Address Format

4.2.2 Outputs

The address selection logic output signals are used to permit selection of three 16-bit registers and provide three signals used for gating information into and out of the master device. All of these output signals are listed in Table 4-1. Note that the logic diagram (drawing DR-4) shows an additional select line signal, SELECT 6. This particular signal is not used by the DR11-C interface but the interface can respond to that address.

Tables 4-2 and 4-3 indicate the input signals that select the control output line states.

Table 4-2
Select Lines

Input Lines A⟨02:01⟩	Select Lines True (+3V)
00	0
01	2
10	4
11	6 (not used)

NOTES: 1. Lines A⟨17:13⟩ must be all 1s (0V on Unibus).

2. Lines A⟨12:03⟩ are selected by jumpers.

Table 4-3
Gating Control Signals

Mode Control C⟨1:0⟩	Byte Control A00	Gating Control Signals True (+3V)	Bus Sequence
00	0	IN	DATI
00	1	IN	DATI
01	0	IN	DATIP
01	1	IN	DATIP
10	0	OUT LOW OUT HIGH	DATO
10	1	OUT LOW OUT HIGH	DATO
11	0	OUT LOW	DATOB
11	1	OUT HIGH	DATOB

NOTE: Gating control signals may become true although select lines are not.

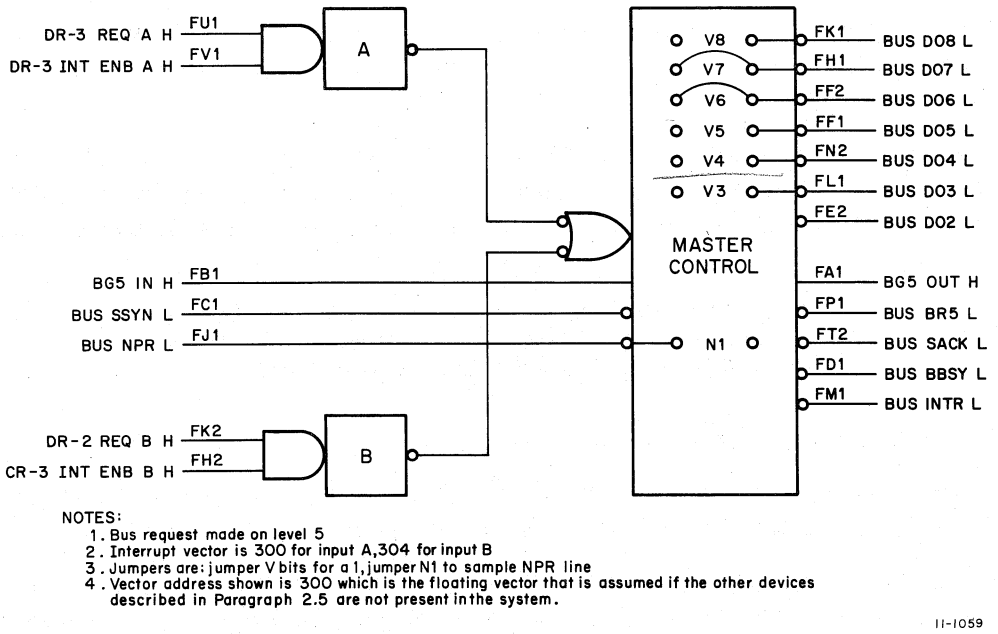


Figure 4-4 Interrupt Control Logic, Simplified Block Diagram

The B input interrupt logic operates in a similar manner to that of the A input logic. In this case, the two input signals that must be high are: REQUEST B and INT ENB B. The logic for INT ENB B is shown on drawing DR-3. When a 1 is loaded into bit 05 of the status register (DRCSR), it sets the interrupt flip-flop to produce INT ENB B H which is applied to the interrupt logic as an enabling signal.

The second signal that must be present is REQUEST B H. As shown on drawing DR-2, this signal must also be produced in the user's device as described in Chapter 6 of this manual.

The B input interrupt logic functions in an identical manner to the A input logic except that it generates a different vector address. Although both REQUEST A and REQUEST B are at a BR5 level, REQUEST A has a slightly higher priority.

Once the DR11-C interface has gained bus control by means of a BR request, an interrupt is generated. The interrupt vector address is selected by jumpers on the logic as shown in Figure 4-4. Because the vector is a 2-word (4-byte) block, it is not necessary to assert the state of bits 0 and 1.

The six selectable (jumpered) lines determine the two most significant octal digits of the vector address. The least significant octal digit is controlled by bit 02 so that all vector addresses end in either 0 or 4. The input to bit 02 is tied to the V2 flip-flop logic. Whenever an interrupt occurs on input A, bus line D02 is *not* asserted, and the interrupt causes a vector at location 300. When a B input interrupt occurs, bus line D02 is asserted, and the interrupt causes a vector at location 304. Note that the first two octal digits can be changed by jumpers but the last octal digit is always 0 or 4.

The BG IN signal is allowed to pass through the logic to BUS BG OUT when the interface is not issuing a request. To request bus use, the AND condition of REQUEST and INT ENB must be satisfied. These levels must be true until the interrupt service routine clears REQUEST or INT ENB. Once bus control has been attained, it is released when the processor responds with BUS SSYN after it has strobed in the interrupt vector. After releasing bus control, the logic inhibits further bus requests from that input (A or B) even if REQUEST and INT ENB

The outputs of the bit 05 and 06 flip-flops (INT ENB A, B) are applied as an enabling level to the interrupt control logic described in Paragraph 4.3.

The outputs of the bit 00 and 01 flip-flops (CSR0 and CSR1) are available to the user and, if desired, can be used as commands to initiate operations within the external device.

It should be noted that all of the read/write status register bits are located in the low-order byte. Therefore, byte addressing can be used for access to these bits. When reading, word addressing must be used if it is desired to read all six bits. However, in the case of loading the register, only DATOB bus cycles are required because any bit that can be loaded from the bus is in the low-order byte of the register.

The remaining two status register bits (07 and 15) are read-only bits which are generated by the external device as described in Chapter 6 of this manual. The logic for these bits (REQUEST A, B) is shown on drawings DR-3 and DR-2, respectively. A simplified version of the logic is shown in Figure 4-6 and described below.

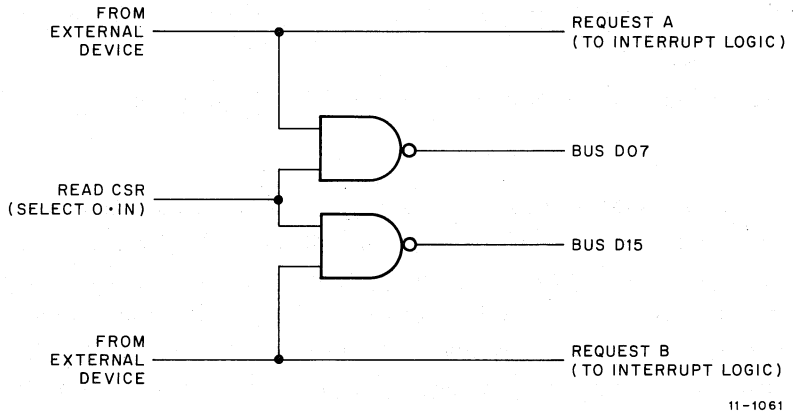


Figure 4-6 DRCSR Read-Only Bits (REQUEST A and B)

When the external device generates a REQUEST level, it is applied directly to the interrupt control logic to initiate an interrupt sequence, provided the associated INT ENB bit has been set. If it is desired to use the REQUEST level as a flag rather than for an interrupt request, then the INT ENB bit is not set by the program and the REQUEST line is read by the program. During this read operation, READ CSR is true and gates the REQUEST level to the appropriate bus data line for reading.

The CSR0 and CSR1 bits and the two REQUEST bits can be used for communication between interfaces when two DR11-C units are being used as an interprocessor buffer. For example, the CSR0 bit in one interface is connected to the REQUEST A input line of the second interface. If the program then sets CSR0 in the first interface, REQUEST A is true in the second interface which then initiates an interrupt sequence. A discussion of the DR11-C used as an interprocessor buffer is covered in Chapter 6 of this manual.

4.5 OUTPUT BUFFER REGISTER (DROUTBUF)

The output buffer is a 16-bit read/write register that can be read or loaded from the Unibus. This register consists of four 8271 IC chips and associated input/output gating. The register logic is shown on drawings DR-2 and DR-3. A simplified version of the DROUTBUF logic is shown in Figure 4-7 and described below. This figure illustrates a single register bit (bit 03). All other bits function in an identical manner.

CHAPTER 5
MAINTENANCE

5.1 INTERFACE TESTING

Checkout and testing of the DR11-C is accomplished by using the MAINT cable supplied with the interface. Rather than using the two M971 connector modules to cable user signals to and from the external device, the maintenance cable plugs into the two connectors on the M7860 module and jumpers the DR11-C output lines to the input lines as shown in Figure 5-1.

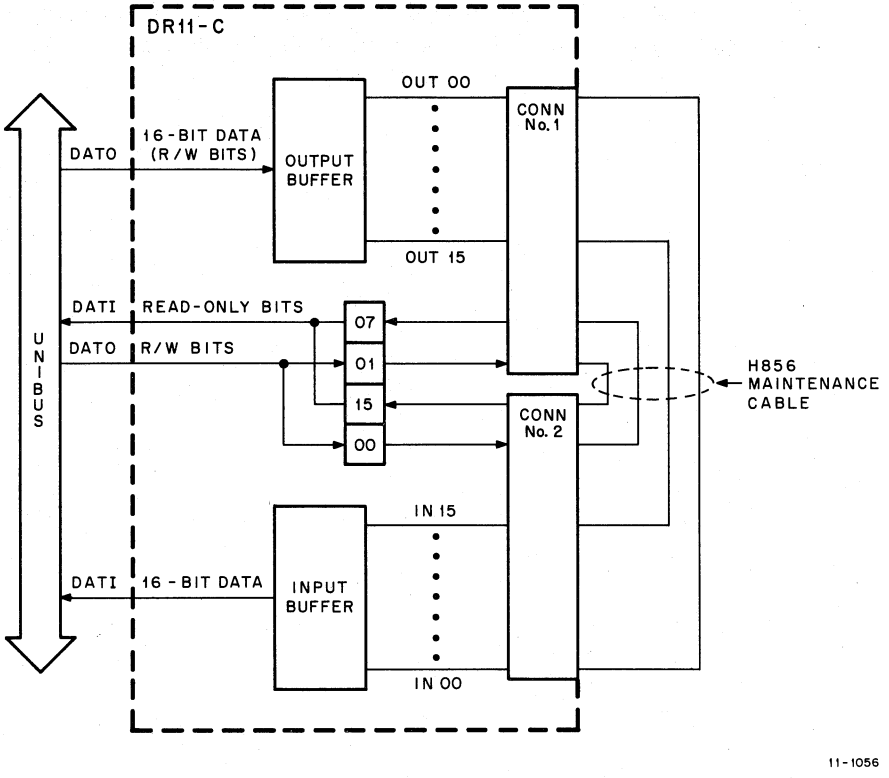


Figure 5-1 DR11-C Bits Jumpered by Maintenance Cable

As can be seen in the figure, any 16-bit word loaded from the bus into the output buffer is fed back into the input buffer for reading from the bus. In this case, if the word that is read is identical to the word that had been loaded, it indicates that the input buffer, output buffer, and associated circuits are all functioning properly.

CHAPTER 6
EXAMPLES

6.1 BASIC INTERFACE

Figure 6-1 illustrates a typical user's device interface, consisting of a basic control section and a data assembly register.

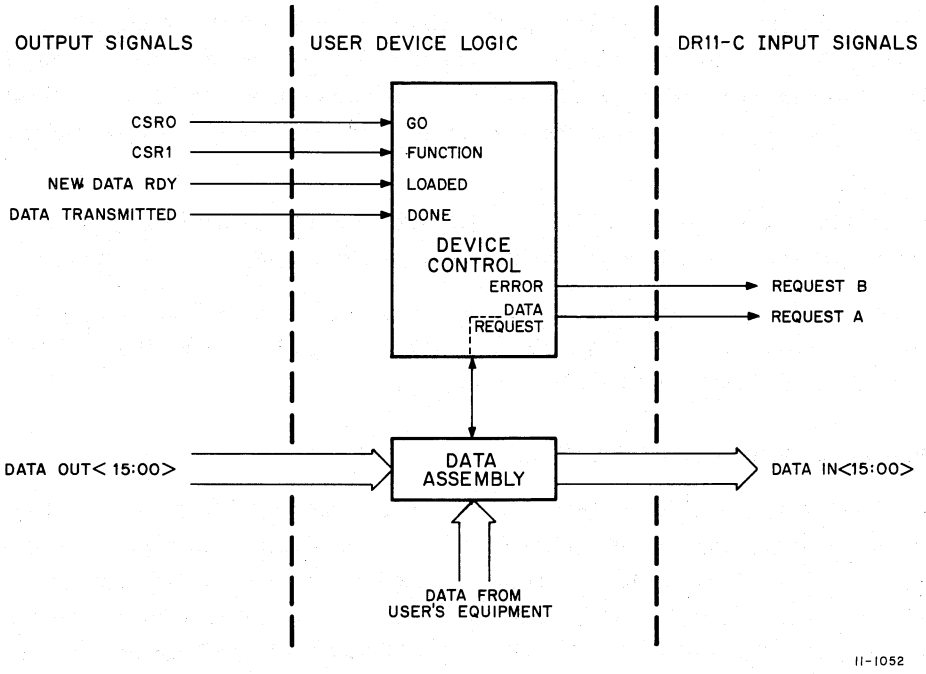


Figure 6-1 Basic Interface

Operation of the interface is initiated by the GO level. The FUNCTION bit informs the device whether it is to perform a read or write operation. When data is ready for transfer to the Unibus or data is required from the Unibus, a low-to-high transition on DATA REQUEST activates the REQUEST A line. The REQUEST A line initiates an interrupt sequence provided the INT ENB A bit in the DR11-C status register has been set. If the desired function is to load data into the user device, a LOADED (NEW DATA READY) pulse informs the device control when the data is ready for transfer. If a write function has been selected, a DONE (DATA TRANSMITTED) pulse informs the device control when the DR11-C has completed strobing of the data. The ERROR

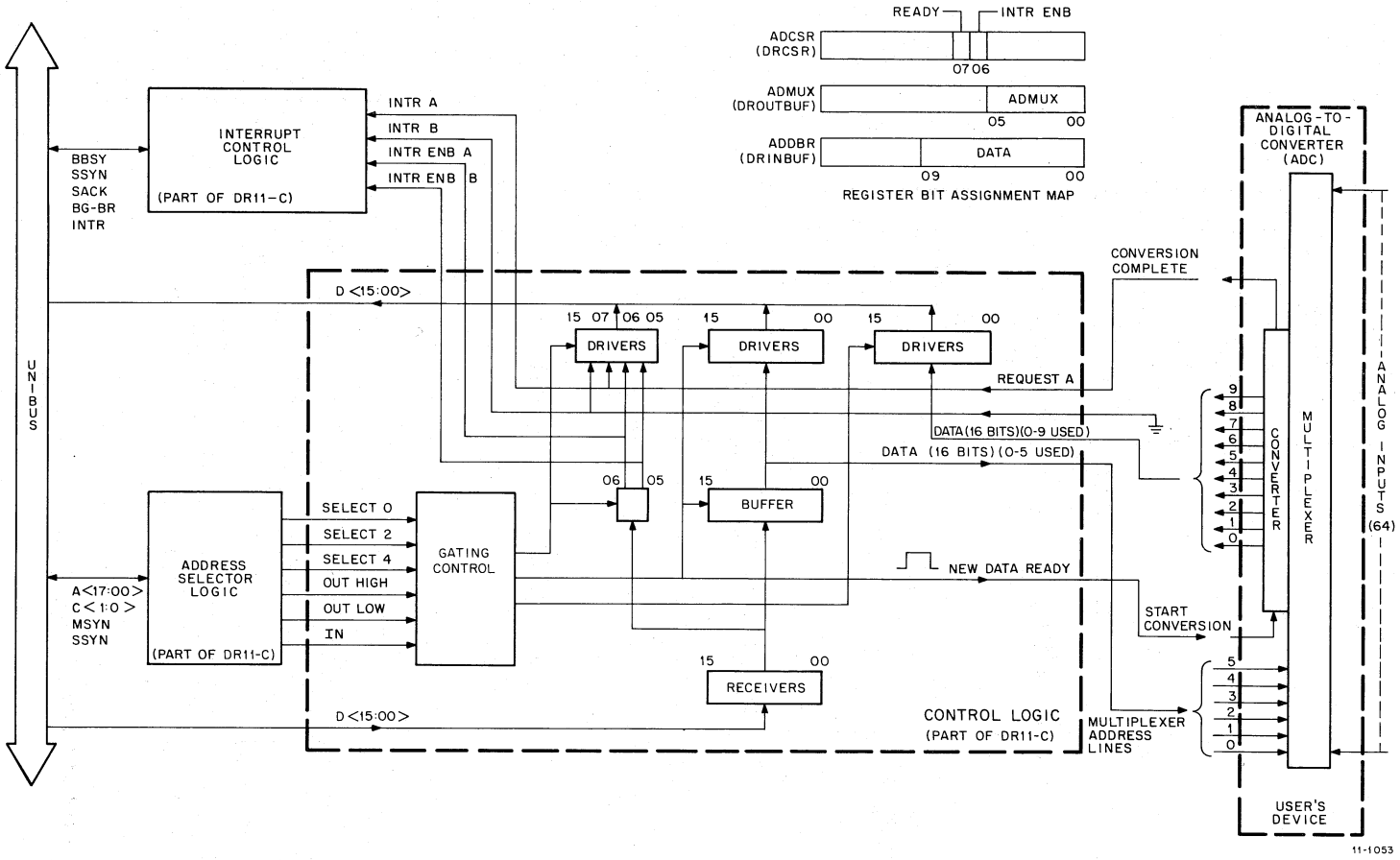


Figure 6-2 Interrupt Serviced Interface

The Connector No. 1 of the first DR11-C is connected to Connector No. 2 of the second DR11-C This causes all of the output lines (OUT00 – OUT15) of the first interface to be connected to the corresponding input lines (IN00 – IN15) of the second interface (refer to pin connections given in Table 3-5). The CSR0 and CSR1 lines of the first unit are connected to the REQ A and B lines, respectively, of the second unit.

Connector No. 2 of the first unit is connected to Connector No. 1 of the second unit. This connects the IN lines and REQ lines of the first unit to the OUT lines and CSR lines of the second unit.

With the two PDP-11 buses interfaced in this manner, setting a CSR bit in one interface activates the REQ line in the other interface to initiate an interrupt sequence. Data can then be loaded from the bus into the DROUTBUF of the first unit for transfer to the DRINBUF of the second unit.

CHAPTER 7
ENGINEERING DRAWING SET

A complete set of engineering drawings is provided with each DR11-C interface. These drawings are bound in a separate volume entitled, *DR11-C General Device Interface,* Engineering Drawings. The general logic symbols used on these drawings are described in the *DEC Logic Handbook,* 1972. Specific symbols and conventions are also included in the *PDP-11 Conventions Manual,* DEC-11-HR6B-D and in certain PDP-11 System manuals. The following paragraphs describe the signal nomenclature conventions used on the drawing set.

Signal names in the DR11-C print set are in the following basic form:

SOURCE	SIGNAL NAME	POLARITY

SOURCE indicates the drawing number of the print where the signal originates. The drawing number of a print is located in the lower right-hand corner of the print title block (DR-2, DR-3, or DR-4).

SIGNAL NAME is the proper name of the signal. The names used on the print set are also used in this manual for correlation between the two.

POLARITY is either H or L to indicate the voltage level of the signal: H means +3V; L means ground.

As an example, the signal:

DR-3 INT ENB A H

originates on sheet 3 of the M7860 module drawing and is read, "When INT ENB A is true, this signal is at +3V."

Unibus signal lines do not carry a SOURCE indicator. These signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal exist. Each Unibus signal name is prefixed with the word BUS.

Interface signals that are fed to the external device are preceded by the pin number in parentheses:

(1VV) NEW DATA READY H

Interface signals received from the external device are followed by the pin number in parentheses:

IN 6 (2PP)

In both of the above cases, the initial number in parentheses is the connector number (1 or 2), and the letter, or letters, are the pin number of that connector.

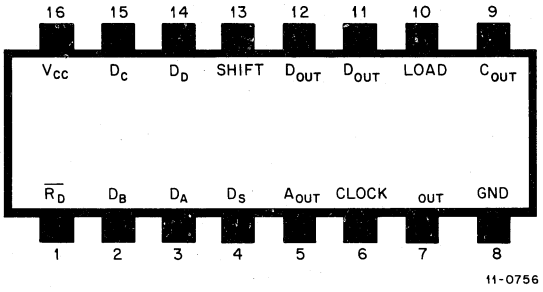
APPENDIX A
INTEGRATED CIRCUIT

There are five 8271 IC chips used in the DR11-C interface. Although this chip is designed as a 4-bit shift register, the shift input is disabled and each chip functions as four individual flip-flops. Four 8271 ICs are used for the 16-bit DROUTBUF register and the remaining IC is used for the four read/write bits in the DRCSR register.

Figure A-1 provides a circuit schematic, packaging diagram, and truth table for the 8271 IC.

Truth Table

Control State	Load	Shift
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1



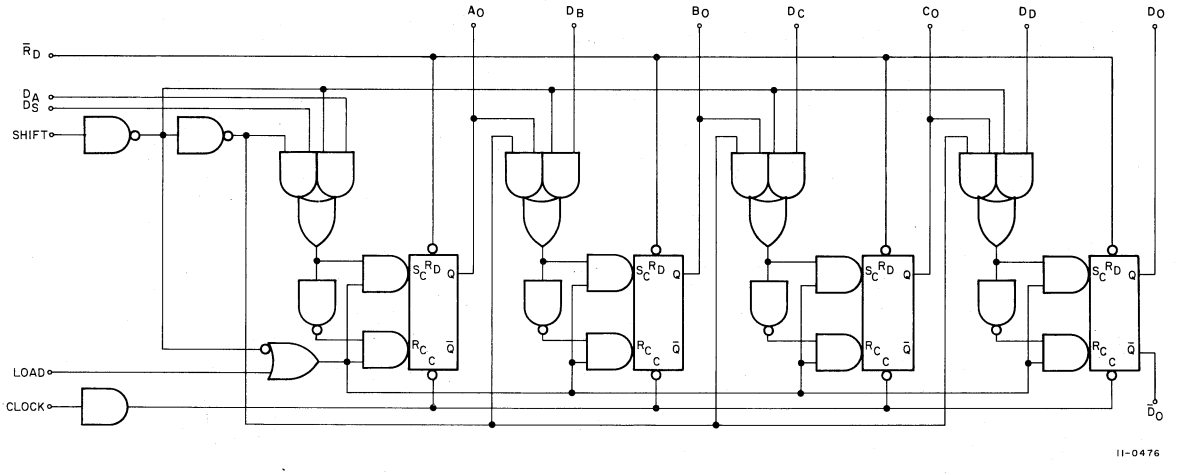


Figure A-1 8271 IC Circuit Schematic

APPENDIX B
USE OF BB11

The BB11 Blank Mounting Panel is a prewired system unit designed for general interfacing. Figure B-1 illustrates the method of mounting a DR11-C interface into a BB11 system unit, assuming that the BB11 has slot 1 wired as a DD11-A or equivalent.

The first step is to mount the DR11-C in one of the four slots. Two of the remaining slots are used for the two M971 Cable Connector modules. This leaves 12 double-height slots available for mounting user interface logic.

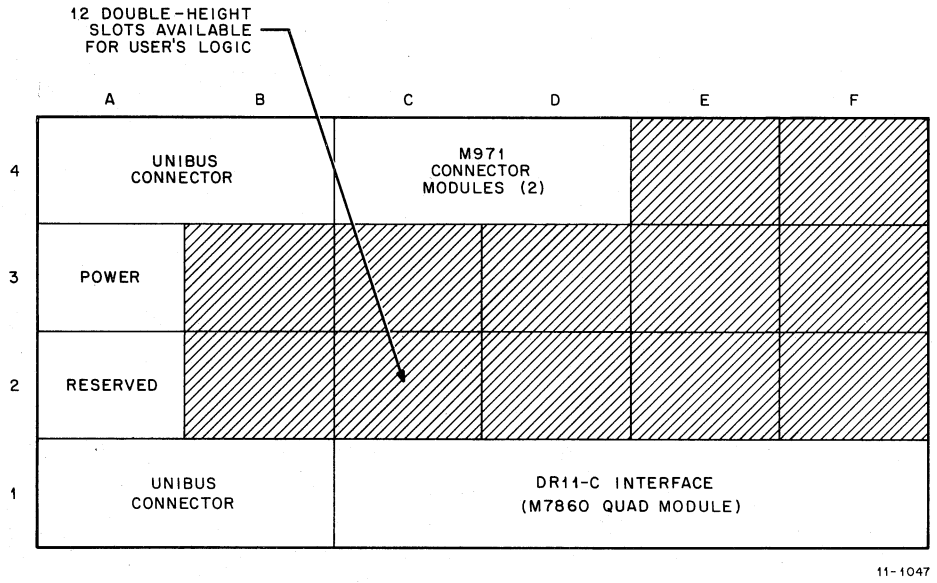


Figure B-1 DR11-C Mounted in BB11 System Unit

DR11-C GENERAL DEVICE INTERFACE MANUAL DEC-11-HDRCA-C-D

READER'S COMMENTS

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgement is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults do you find with the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____
Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

Would you please indicate any factual errors you have found. _____

_____

_____

_____

_____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

— — — — — — — — — — — — Fold Here — — — — — — — — — — — —

— — — — — — — — — Do Not Tear - Fold Here and Staple — — — — — — — — —

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

Postage will be paid by:

Digital Equipment Corporation
Technical Documentation Department
146 Main Street
Maynard, Massachusetts 01754

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS 01754