DEC-11-HMSTS-A-D

PDP-11/45, 11/50 MOS MEMORY TROUBLESHOOTING GUIDE

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to: Ron Moorhead

digital INTEROFFICE MEMORANDUM

TO: All Field Service Personnel

DATE: 13 December 1974

FROM: Conray Wharff

DEPT: 11 Product Support

EXT: 2561 LOC: Pk3/S17

SUBJ:

Enclosed you will find a copy of the MOS Memory Trouble Shooting Guide. It is intended as a trouble shooting aid for MOS systems and should be considered COMPANY CONFIDENTIAL, that is take it on site but do not let the customer read it.

Table Six concerns noise problems in MOS. Noise problems are easy to identify but can not be repaired in the field. Set the CPU up to run a Branch dot as per table six. Scope E105 pin 10 and 11, any noise spike below 11 volts on pin 10 will mean the matrix should be replaced. Please do not send these to the Depot for repair!'. Instead send them to me with all the necessary paper work. I will make sure the branch will receive credit for returning the module.

This cover letter should not be kept with the guide, any errors, suggestions, or submissions should be reported to Conray Wharff, Pk3/S17, extension 3344.

CW/amc

CONTENTS

INTRODUCTION

This troubleshooting guide is intended to assist the service person in the repair of PDP-11/45, 11/50 MOS Memory Systems. This document is for Field Service use only and is to be treated as a Tech Tip.

The guide consists of an annotated flowchart and nine tables that contain reference material relating to the procedures outlined by the flowchart. The flowchart refers to these tables at the appropriate points.

The contents of this guide are a compilation of the experience of several field engineers who have worked extensively with the MOS memory system, which consists of the M8110 Controller and the G401 and G401YA Matrices.

28 June 1974

Table 1
MOS Memory Jumpers

G401 JUMPERS

Table 1a contains the required jumper configuration for the assignment of the 4K block of MOS memory addresses. If, for example, a G401 MOS Memory Matrix has jumpers C and B installed, then that matrix contains memory locations XX 4096 through XX 8191. The Xs preceding the number denote that the memory addresses can be selected anywhere in the range from 0 to 128K. Any address from 4096 to 8191 is recognized and responded to by the matrix.

Table 1a
G401 MOS Memory Matrix Selected Address Configuration (4 of 16K)

MAD 14	MAD 13	Required Jumpers (MAD 14)	Required Jumpers (MAD 13)	MOS Matrix Memory Address Assignment
0	0	C	A	0–4095
0	1	C	B	4096–8191
1	0	D	A	8192–12,287
1	1	D	B	12,288–16,383

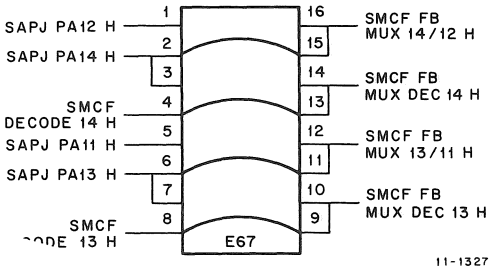
M8110 JUMPERS

The jumper connections on the M8110 SMC module are designated by E numbers. Jumpers are located on E67, E75, E78, E86, and E87 (described in the following paragraphs). E86 jumpers exist on the B etch only. All jumpers are prewired on the controller module; for a specific address configuration, jumper wires must be cut. If the configuration is changed, it is necessary to reinstall some jumpers previously cut. Refer to the *MS11 Semiconductor Memory Systems Maintenance Manual* and related engineering drawing set for detailed information pertaining to the various jumper connections. M8110 jumper locations are shown in Table 1e.

E67 and E68 Jumpers

The jumpers at E67 and E78 allow the M8110 to be configured for MOS or bipolar memory.

Fastbus Interface – The figure below shows the jumper connections at E67 that interface the Fastbus to the controller for MOS memory. Note that bits 13 and 14 are designated for MOS and bits 11 and 12 for bipolar. Note also that SMCF DECODE 14 and SMCF DECODE 13 are connected for MOS memory.



Unibus Interface – The figure below shows the jumper connections at E78 that interface the Unibus to the controller for MOS memory. Note that bits 13 and 14 are associated with MOS and bits 11 and 12 are associated with bipolar. Also note that SMCF DECODE 14 and SMCF DECODE 13 are connected for MOS

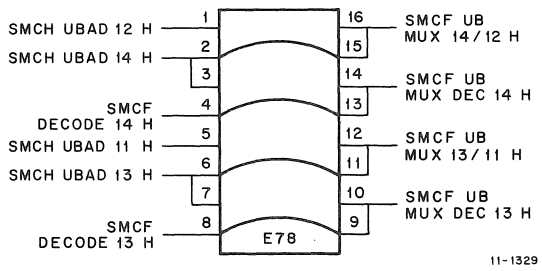


Table 1 (Cont)
MOS Memory Jumpers

M8110 JUMPERS (Cont)
E87 Jumpers

E87 Jumpers – Jumpers C, D, E, F, and H are used to assign a block of MOS or bipolar addresses to a controller from the total available address area from 0 to 12K (Table 1d). For example, to have the controller respond to MOS memory addresses from 96K to 112K, jumpers C and D must be cut. Jumpers C, D, and E allow assignment of 16K words within the total address space.

For MOS memory, jumper A is cut. If this jumper is not cut, the controller is configured for bipolar memory and refresh is inhibited. If the parity option is installed, jumper B is cut to enable the Parity Control register. If jumper T is cut, Parity register address bit 1 will be a 1; if jumper T is not cut, this bit will be a 0. See Drawing D-CS-M8110-0-1, sheet SMCF.

Jumpers F and H are never cut for MOS memory.

Table 1d
Fastbus/Unibus Memory Address (Assign and Decode)

Fastbus/Unibus Address Decoder Bits			MOS Memory Address Assignment	M8110 Jumpers (E87) ("X" denotes jumper to be cut.)		
17	16	15		C	D	E
0	0	0	0–16K			
0	0	1	16–32K			X
0	1	0	32–48K		X	
0	1	1	48–64K		X	X
1	0	0	64–80K	X		
1	0	1	80–96K	X		X
1	1	0	96–112K	X	X	
1	1	1	112–128K	X	X	X

Table 1e gives the location of the E87 jumpers, which varies depending on the module etch revision.

Table 1e
Location of E87 Jumpers

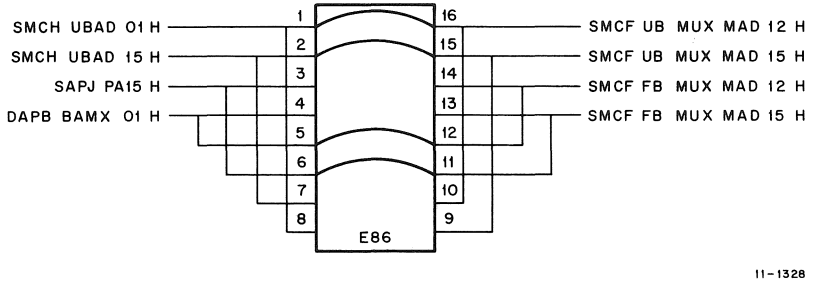
Jumper	Location	
	B Etch	C & D Etches
A	E8705	E8705
B	E8701	E8701
C	E8703	E8704
D	E8704	E8706
E	E8706	E8707
F	E8702	E8703
H	E8708	E8708
T	See Note	E8702

NOTE: Jumper T is located below E85 on the B etch modules.

Table 1 (Cont)
MOS Memory Jumpers

M8110 JUMPERS (Cont)
E86 Jumpers

E86 Jumpers – E86 jumpers, which are used for interleaving, exist on the B etch only. The SMCF FB MUX MAD 15 H input to NOR gate E89 of the Fastbus address decoder is from another jumper-wired multiplexer, E86, on the M8110 module. The figure below shows the jumper configuration required to route Fastbus/Unibus address bit 15 to the address decoder.



INSTALLATION OF MOS ONLY MEMORY

From 4K to 32K of MOS memory, in increments of 4K, can be installed in the PDP-11/45, 11/50 system. The MS11-BC memory option controls 16K of MOS memory. If more than 16K of MOS memory capacity is desired, an additional MS11-BD Memory Control is required. The procedure for installing MOS memory is described below.

1. Turn off circuit breakers on both the H742 Power Supplies. Install the H744 +5 V Regulator (part of the MS11-BC) in slot J of the lower H742 Power Supply.

2. Install the H746 MOS Regulator in slot H of the lower H742 Power Supply.

3. Install the M8110 SMC module in slot 16 of the CPU backplane assembly and install the G401 MOS Memory Matrix modules in the CPU backplane assembly in slots 17–20 (maximum of four G401 modules per M8110).

NOTE
If MS11-BP (memory parity) option is selected, the MOS Memory Matrix modules are designated G401YA.

4. If more than 16K of memory is required, install the second M8110 SMC module that comprises the MS11-BD Memory Control in slot 21 of the CPU backplane assembly. Install the additional G401 MOS Memory Matrix modules, starting at slot 22 of the CPU backplane assembly.

5. Turn on circuit breakers and measure the voltage from A16A2 of the CPU backplane to ground for +5 Vdc.

6. Measure the following voltages at the points indicated below:

Voltage	CPU Backplane Point of Measurement
+23.2 Vdc	Pin A17V2 and ground
+19.7 Vdc	Pin A17U2 and ground
-5 Vdc	Pin F17C1 and ground

7. Readjust as required.

CAUTION
Do not cut any jumpers on the power harness when installing MOS memory.

8. Refer to the MS11 engineering print set for appropriate timing adjustments.

Table 1 (Cont)
MOS Memory Jumpers

INSTALLATION OF MOS AND BIPOLAR MEMORY

Up to 16K of MOS memory (in 4K increments) and up to 4K of bipolar memory (in 1K increments) can be installed in combination in the CPU cabinet. The MS11-CC Memory Control handles 4K of bipolar memory. The installation for combined MOS and bipolar memory is described below.

1. Turn off H742 Power Supply circuit breakers.
2. Cut the jumper between P5-3 and -4 on the power harness.
3. Install the H746 MOS Regulator in slot H of the lower H742 Power Supply.
4. Install one H744 +5 V Regulator in slot J of the lower H742 Power Supply.
5. Install second H744 +5 V Regulator in slot K of the lower H742 Power Supply.
6. If more than 2K of bipolar memory is installed, install third H744 +5 V Regulator in slot L of the lower H742 Power Supply. Cut the jumper between P6-7 and -8 on the power distribution cable harness.
7. Install the M8110 SMC module supplied as part of the MS11-BC MOS Memory Control option in slot 16 of the CPU backplane assembly.
8. Install the G401 MOS Memory Matrices (G401YA if memory parity is selected), starting at slot 17 of the CPU backplane assembly. Up to four modules can be installed.
9. Install the M8110 SMC module supplied as part of the MS11-CC Bipolar Memory Control in slot 21 of the CPU backplane assembly.
10. Install the M8111 Bipolar Memory Matrix modules in the CPU backplane assembly (M8111YA with memory parity), starting at slot 22 of the CPU backplane assembly.
11. Turn on power supply circuit breakers.
12. Measure the following voltages between the points indicated.

Voltage	CPU Backplane
+5 Vdc	Between A16A2 and ground
+23.2 Vdc	Between A17V2 and ground
+19.7 Vdc	Between A17U2 and ground
-5 Vdc	Between F17C1 and ground
+5 Vdc	Between A21A2 and ground
+5 Vdc	Between A24A2 and ground

13. Adjust voltages if required.

NOTE

All M8110 SMC module adjustments have been made at the factory. If further adjustment is required, use the latest SMC module circuit schematic for the proper adjustment procedure.

Table 2
M8110 Controller Timing

Check timing on M8110 controller while running a branch self at a location in the MOS memory to be checked. Adjust if needed. Use probe 1 to trigger the trace on the scope. All measurements are made at a 1.5 V level and at low-going edges of the pulses.

M8110 B Etch Timing

Check	Probe 1	Probe 2	For	Adjust
Address setup	E17 Pin 8	E24 Pin 8	95 ns	R42
CENABLE	E24 Pin 8	E24 Pin 6	70 ns	R7
PRECHARGE	E24 Pin 8*	–	90 ns	R9
Access time	E24 Pin 8	E55 Pin 6	240/210 ns†	R11

M8110 C Etch Timing

Check	Probe 1	Probe 2	For	Adjust
Address setup	E18 Pin 8	E25 Pin 8	95 ns	R42
CENABLE	E25 Pin 8	E25 Pin 6	70 ns	R7
PRECHARGE	E25 Pin 8*	–	90 ns	R9
Access time	E25 Pin 8	E27 Pin 13‡	230 ns	R11
MEM SYNC	E25 Pin 8	E55 Pin 6	240/210 ns†	R1
WRITE PULSE L (loop on DATO)	E27 Pin 8*	–	60 ns	R13

*This is a pulse width.

†M8109 Etch Rev C – If jumpers have been installed on the previously unused half (pins 11, 12, etc.) of the flip-flop at E8 of the M109, R1 (R11) of the M8110 should be adjusted to 210 ns. If the flip-flop is unused, adjust R1 (R11) to 240 ns.

M8109 Etch Rev F – Observe jumpers W6 and W5 on the M8109. If W6 is in and W5 is out, adjust R1 (R11) of the M8110 to 240 ns. If W6 is out and W5 is in, adjust R1 (R11) to 210 ns.

‡‡Measured at positive transition of pulse.

Table 3
PDP-11/45, 11/50 ECO List

This table contains a compiled history per module, console, and backpanel for the PDP-11/45 and 11/50 as of 28 June 1974. It also shows a Shippable Module Revision List.

NOTES

1. The first three ECOs to the backpanel were issued under 7008871 numbers; following ECOs used a mixture of KB11 and KB11-A numbers. It was later decided to use KB11-A. To compensate, the following resulted:

   a. KB11-A-ECO 00003 refers to part number 7008871-00002 (backpanel ECO 2).

   b. KB11-A-ECO 00004 refers to part number 7008871-00003 (backpanel ECO 3).

   c. There is no KB11-A number referring to part number 7008871-00001 (backpanel ECO 1).

   d. Six ECOs exist under KB11.

2. Parity ECOs

   a. Parity ECOs required by the PDP-11/45 CPU are:

Module	ECO No.	Backpanel ECO No.
M8100	00003	KB11-A-00015
M8103	00005	
M8105	00005	
M8106	00007, 00008, 00012, 00012A	

   b. The parity ECOs required by MOS and bipolar memories is:

Module	ECO No.
M8110 (C etch)	00008

3. Speed-up ECO Chart

Module Status	Backpanel Status		
	Old Backpanel ECO KB11-A-00011 and below	With ECO KB11-A-00012A	With ECO KB11-A-00013
M8106 (UBC) CS Rev A-3	OK	Will not work	Will not work
M8106 (UBC) CS Rev F and above (M8106-5 installed)	Will not work	OK (no speed increase)	OK
M8104 (PDR) Etch Rev B	OK	OK	Will not work
M8104 (PDR) Etch Rev C and above	Will not work	OK (no speed increase)	OK (full speed-up modification installed)

4. M8110 Etch Rev C must be used in conjunction with M8106 CS Rev M or higher.

Table 3 (Cont)
PDP-11/45, 11/50 ECO List

Assembly Number	ECO Number	CS Rev	Etch Rev	Code	Date	Comments
M8100	00001	A	A	03	4-18-72	Corrects range of START VECTOR and print errors.
	00001A	A	A	03	4-28-72	Corrects error on ECO 00001.
	00002	B	B	02	6-9-72	Relayout etch.
	00002A	B	B	03	6-20-72	Changes disposition code of ECO 00002. Also lets CMP.B and BIT.B instructions work. (Requires ECO-KB11-A-00006.)
	00003	C	C	02	1-18-73	Parity (Note 2).
	00003A	C	C	03*	3-27-73	Changes disposition code of ECO 00003.
M8101	00001	B	B	06	3-8-72	Selection of 74194 IC.
	00002	C	B	06	6-13-72	Print errors.
	00003	D	B	03	12-6-72	Replacement of selected 74194 by 74S194.
M8102	00001	B	C	03	2-22-72	Corrects etch errors produced by digitizing on a relayout of etch.
	00002	C	C	06	6-13-72	Print errors.
M8103	00001	B	C	02	5-30-72	Relayout and correction of print errors.
	00002	C	C	02	6-29-72	Changes ROM pattern from C40A2 to C47A2.
	00003	D	C	02	1-3-73	Replaces selected 74S153-1 and 74S64-1 to plain 74S153 and 74S64. (Only true if the 74194s on the M8101 are 74S194 in earlier serial number 11/45s.)
	00004	E	C	03	1-18-73	Fix for bad T3 pulses.
	00005	F	C	03*	3-1-73	Parity (Note 2).
	00005A	F	C	03*	3-27-73	Changes FIELD SERVICE EFFECTED BLOCK.
	00006	H	C	03*	10-17-73	Processor could hang in T2 and pause. (Requires ECO M8105-00007.)

Table 3 (Cont)
PDP-11/45, 11/50 ECO List

Assembly Number	ECO Number	CS Rev	Etch Rev	Code	Date	Comments
M8104	00001	B	B	03	4-10-72	Etch errors. FP ROM ADD BIT tied to output of DISPLAY MUX.
	00002	C	C	02*	12-12-72	Speed-up (Note 3).
M8105	00001	B	C†	02	3-7-72	Corrects etch errors and relayout of etch.
	00001A	B	C†	03	4-13-72	Changes DISPOSITION CODE of ECO 00001 and corrects POWER FAIL in Red Zone CLEARS, PDNF.
	00002	C	D†	03	5-19-72	Corrects FP TRAPS to location 4 where BRs below 7 occur at the same time.
	00003	D	E	03	8-16-72	PIRQ level 1 request locks out "T" bit if PSW priority is at level 1.
	00004	E	E	02	12-8-72	The 74S74-45 in location E37 is not necessary; use plain 74S74.
	00005	F	E	02	2-26-73	Parity (Note 2).
	00006	H	E	03*	6-25-73	References to internal registers cause unnecessary data to be put on the Unibus.
	00007	J	E	03*	10-17-73	Processor could hang in T2 and pause. (Requires ECO M8103-00006.)
	00008	K	F	02	11-16-73	Relayout of etch.
M8106	00001	B	B	03	3-27-72	Changes CLEAR on UBCE PUP (1) to UBCB ABORT ACKN L.
	00002	C	C‡	02	4-27-72	Adds timing diagrams and relayout etch.
	00002A	C	C‡	03	5-22-72	Timing of POWER FAIL and STACK YELLOW in bipolar is too tight.
	00003	D	D‡	02	8-23-72	Adds disable jumper for UNIBUS PARITY.

† C and D etch never released to production.
‡ Etch Revs were never built.

Table 3 (Cont)
PDP-11/45, 11/50 ECO List

Assembly Number	ECO Number	CS Rev	Etch Rev	Code	Date	Comments
M8106 (Cont)	00004	E	D‡	02	12-8-72	The 74S74-45 in location E75 is not necessary; use plain 74S74.
	00005	F	E‡	03	12-2-72	CLR MSYN with T1.
	00005A	F	E‡	06	1-5-73	Corrects rework procedure on ECO 00005.
	00006	H	E‡	06	1-31-73	Adds timing diagrams and corrects print errors.
	00007	J	E‡	03*	3-6-73	Parity (Note 2).
	00008	K	E‡	03*	3-14-73	Parity (Note 2).
	00009					
	00009A					Cancelled.
	00010					
	00010A					
	00011	L	E‡	03	5-31-73	Asserts RIP + FP SYNC sooner.
	00012	M	E‡	03*	6-6-73	Parity (Note 2).
	00012A	M	E‡	03*	6-6-73	Corrects rework procedure on ECO 00012.
	00013	N	F	02	8-10-73	Relayout of etch.
	00014	M1	B	03*	2-22-74	Processor could possibly hang during a BR sequence on CS Rev M boards due to missing +3 V signal.
	00015	P	B,F	03*	6-14-74	Power fail not working in console lock mode.
M8107	00001	A	B	02	5-11-72	Corrects etch errors and a relayout of etch.
	00001A	A	B	03	6-9-72	Corrects break-in effectivity.

‡ Etch Revs were never built.

Table 3 (Cont)
PDP-11/45, 11/50 ECO List

Assembly Number	ECO Number	CS Rev	Etch Rev	Code	Date	Comments
M8108	00001	A	A	03	4-4-72	Race condition at 1.2 μs/ROM cycle and corrects print errors.
	00002	B	A	03	4-14-72	Execute only mode.
	00003	C	A	03	4-18-72	Execute only mode and address error on internal REG EXAM after ABORT. (Requires backpanel 7008871 ECO 00002.)
	00004	D	B	02	4-27-72	Etch corrected to bring it to CS Rev C level and relayout.
	00004A	D	B	03	6-9-72	Rework A Etch Rev to bring to D level CS.
	00005					Cancelled
	00005A					
	00006	E	B	06	3-10-73	Documentation change.
	00007	F	B	03*	4-6-73	Failed to ABORT on INT. REG. reference. (Requires ECO KB11-A-00017A.)
M8109	00001	C	C	03	4-24-72	Synchronizer for T1 will not work when T1 SYNC FF output used for logic gating.
	00002	D	C	02	5-31-72	Changes physical size of 0.22 uF capacitor.
	00003	E	C	03	6-5-72	Adjustment of 150 ns range is difficult; change R162.
	00004	F	C	03	6-15-72	ROM and UP B logic change.
	00005	H	D	02	6-19-72	Relayout.
	00006	J	D	03	6-27-72	SSR DLY logic change.
	00007					Cancelled
	00007A					
	00008	K	E	03	9-7-72	PAUSE, STOP 3 logic change. (Requires ECO KB11-A-00009.)

Table 3 (Cont)
PDP-11/45, 11/50 ECO List

Assembly Number	ECO Number	CS Rev	Etch Rev	Code	Date	Comments
M8109 (Cont)	00009	L	E	02	10-5-72	Documentation change and bypass capacitor C60 not connected to ground.
	00010	M	E	02	12-20-72	The 74S74-45 is not necessary in location E08 and E24; use plain 74S74.
	00011	N	F	02	1-2-73	Relayout etch and adds circuit for symmetry problem.
	00012	M1	C	02	2-13-73	Changes E15 from a 74S74-45 to a 74S74-50.
	00013	M2	C	03*	12-20-73	ECOs out the use of 74S74-50; use 74S74-45 as a double synchronizer.
	00014	P	F	03*	2-18-74	Etch error. TIGB SSR MAT H grounded.
	00015	R M3	F C	03* 03*	4-10-74	CPU fails to halt on selected ROM state when micro program break mode is set on maintenance card. Detected when running a test sequence not containing a pause, i.e., 150 ns cycle time.
M8110	00001	B	B	03	5-15-72	Corrects etch errors.
	00002	C	B	03	5-17-72	Violating memory chip (1103-1) spec during refresh cycle and also 4 V spikes on the -15 V line.
	00003	D	B	03	7-28-72	Parity check during refresh cycle and documentation errors.
	00004	E	B	03	8-25-72	Race condition in BEND CYCLE.
	00005	F	C	02	9-7-72	Relayout.
	0005A	F	C	02	10-2-72	Adding and deleting parts to the new layout.
	0005B	F	C	02	3-23-73	
	0005C	F	C	02	4-29-73	
	00006	E1	B	02	4-2-73	Adds new jumper socket.
	00007 00007A					Cancelled

Table 3 (Cont)
PDP-11/45, 11/50 ECO List

Assembly Number	ECO Number	CS Rev	Etch Rev	Code	Date	Comments
M8110 (Cont)	00008	H	C	03*	6-7-73	Parity (Note 2).
	00009	E2	B	03*	6-21-73	Changes setup time on access time spec (capacitor change). Also corrects documentation errors.
	00010	J	D	02*	12-3-73	Corrects documentation errors and relayout of etch board.
	00011	E3	B	06	12-18-73	Rev B Etch M8110 is not documented to allow MOS operation with double synchronizer M8109.
M8111	00001	C	D	02	6-16-72	Relayout etch from nonstandard inner layers to standard inner layers.
	00001A	C	D	06	2-28-73	Cancels relayout and also corrects documentation errors.
M8112	00001	B	B	03	3-24-72	Allows use of 74175-1. Corrects documentation errors and adds ROM map.
	00002	C	B	03	5-11-72	Extra FP SYNC issued during Negate and Absolute with zero exponent; FP REQ is not dropped during a micro trap. Corrects documentation errors.
	00003	D	C	03	6-2-72	FPS and MBRK register may be incorrectly loaded during ABORT sequence; also relays out etch.
	00004	E	D	03	10-12-72	Extra FP SYNC is issued during STCF.
	00005	F	D	02	10-26-72	Corrects print errors and allows use of 74S175 in place of 74175-1.

Table 3 (Cont)
PDP-11/45, 11/50 ECO List

Assembly Number	ECO Number	CS Rev	Etch Rev	Code	Date	Comments
M8113	00001	C	D	03	3-24-72	Corrects etch and documentation errors. Also calls out a relayout of etch.
	00001A	C	C	03	3-29-72	Cancels relayout part of ECO 00001.
	00002	D	C	06	6-8-72	Corrects print errors.
	00003	E	C	03*	8-6-73	Replaces Range ROM from 23C17A2 to 23C48A2.
M8114	00001	B	B	03	3-14-72	Corrects etch errors and documentation.
	00002	C	B	03	5-17-72	Race condition at 20 MHz clock speed; FP ATTN WAIT has glitch during change of ROM state; corrects print errors.
	00002A	C	C	03	5-22-72	Relayout of etch.
M8115	00001	B	B	03	3-13-72	Corrects etch errors.
	00002	C	B	06	7-2-73	Corrects print errors.
M8116	00001	A	B	02	3-3-72	Hand taped artwork prohibits reliable manufacturing of etch; ECO calls for digitizing artwork.
	00002	B	C	03	10-13-72	Corrects digitizing error and relayout of etch.
M8120	–	*	C	–		Used as a M8111 Controller. Released to production at C etch.
	00001	A	D	06		Documentation change.
G401 & G401-YA	00001	C	C	06	3-14-72	Creates a YA variation of the G401.
	00002	D	C	06	5-12-72	Documentation.
	00003	E	D	02	6-1-72	Digitizes etch and calls out special module handle.
	00004	D1	C	03	1-9-73	Adds capacitor on +3 V line to ground and bypass capacitor from ground to 23.2 V plane.
	00005	D2	C	03	2-22-73	Reduces the precharge voltage level into the 1103-1 by adding resistor network.

Table 3 (Cont)
PDP-11/45, 11/50 ECO List

Assembly Number	ECO Number	CS Rev	Etch Rev	Code	Date	Comments
G401 & G401-YA (Cont)	00006	F	D	02	4-3-73	Adds new jumper socket on Rev D etch.
	00006A	F	D	02	5-14-73	Adds resistors to reduce the precharge voltage of ECO 00005 to the parts list.
	00007	H	D	06	7-2-73	Documentation (parts list).
	00008	J	D	03	2-6-74	Noise on two clock lines, Chip Enable and Write Pulse, causes intermittent loss of memory data. Affects D Etch Rev only.
54-09684 (console)	00001	B	B	03	4-3-72	Driver noise on +15 V line; LOCK-ON-OFF switch does not have a shaft feedthrough hole and Z holes on S29 and S31 are too small for switch contact leads.
	00002	C	C	02	4-12-72	Noise on function switch ground return and ground; decoupling needed for +5 V; corrects pad size for Berg connector and a relayout of etch.
	00003	D	C	03*	7-19-72	S30 mounting kep nuts touch etch on side 2; etch near top mounting area touching bracket; halt switch activates in wrong direction and select switch causes noise on function switch ground return.
	00004	E	D	02	2-1-73	Relayout etch.
54-09910	00001	B	B	02	4-13-72	Lack of ground pins for termination of twisted pair ground wires.
	00001A	–	C	–	5-22-73	Adds 5009909 to be updated to C etch.
	00002	C	D	02	1-3-73	Increases width of etch lines on +5 V to increase current carrying capacity.

Table 3 (Cont)
PDP-11/45, 11/50 ECO List

Part	ECO Number	WL Rev	Code	Date	Comments
7008871	00001	A	03	4-25-72	Corrects errors in 11/45 backpanel wire list.
7008871	00002	B	03	5-5-72	BRCA IR 07 (0) H signal required by KT11-C; this ECO adds a wire to Rev A backpanel. (Requires ECO 00003 to the M8108.)
7008871	00003	C	03	5-9-73	Corrects wiring on small peripheral slots.
KB11	00001	–	03	5-5-72	Reworks backpanels with 24 AWG wire in parallel with +5 V etch.
KB11	00001A	–	03	5-18-72	Corrects break-in effectivity of ECO 00001.
KB11	00002	–	03	5-9-72	ECO to power distribution card 5409903 to add Mate-N-Lok connector.
KB11	00003	–	02/06	6-2-72	ECO to the protection sheet 5009936 (mechanical).
KB11	00004	–	02	8-11-72	Adds knock-outs to the 7409215.
KB11	00005	–	02	8-18-72	Reduces cost.
KB11	00005A	–	06	9-14-72	Removes lower fan protection plate (not needed).
KB11	00006	–	02	12-23-72	Mechanical changes to BA11F Mounting Box to provide cost reduction and easier assembly.
KB11-A	00001	–	03	5-9-72	Documentation errors on the MD 7409676-0-0.
KB11-A	00002	–	02	5-9-72	Card guide; affects the MD 7409450-0-0.
KB11-A	00003	–	–	–	Same as 7008871 ECO 00002 (Note 1).
KB11-A	00004	–	–	–	Same as 7008871 ECO 00003 (Note 1).
KB11-A	00005	–	03	6-9-72	Mechanical (scratching of decal on fan housing).
KB11-A	00006	D	03	6-26-72	COMP.B and BIT.B instructions. (Requires ECO 00002A to the M8100.)
KB11-A	00007	–	06	8-8-72	Documentation.
KB11-A	00008	E	03	9-8-72	Signal missing in small peripheral controller slots in KB11-A (slots 26–28).

Table 3 (Cont)
PDP-11/45, 11/50 ECO List

Part	ECO Number	WL Rev	Code	Date	Comments
KB11-A	00009	F	03	9-20-72	Brings ROM 40 BL signal from RACB to TIGA. (Requires ECO 00008 to the M8109.)
KB11-A	00010	–	03	9-27-72	Mechanical (ac wiring being pinched by top of fan housing).
KB11-A	00011	H	06	11-8-72	Corrects wire list prefixes.
KB11-A	00012	J	03	12-28-72	Speed-up (do not install; refer to ECO 00012A).
KB11-A	00012A	J	03	12-28-73	Speed-up (Note 3).
KB11-A	00013	K	02	1-25-73	Speed-up (Note 3).
KB11-A	00014	–	06	1-30-73	Corrects print errors in flow diagram.
KB11-A	00015	L	03*	3-2-73	Parity (Note 2).
KB11-A	00016	M	06	5-11-73	Corrects documentation of wire list.
KB11-A	00017	N	03*	5-21-73	KT11-C fails to ABORT on internal reference. (Do not use this Add and Delete Sheet; refer to ECO KB11-A-00017A.)
KB11-A	00017A	N	03*	6-12-73	All KT11-Cs installed and with the M8108 having ECO 00007 installed must have this change.
KB11-A	00018	–	06	8-2-73	Documentation change. Deletes SMCE MEM D 14 H and SMCE MEM D 15 H from the Wired Assembly (7008871).
KB11-A	00019	–	06	12-14-73	Adds special CS revisions of the M8109 (M1, 2, 3 etc.) to the KB11-A print set.

Table 4
MOS Memory Diagnostics

Diagnostic	Mnemonic
0–124K Excercizer	DZQMBG* or higher revision
KT-11C Excercizer	DCKTGB or higher revision
11 Family Instruction Excercizer	DZQKAA or higher revision
MOS and Core Parity	DCMFA or higher revision

*If not available, order from Software Distribution.

Table 5
MOS Margin Voltages

	Pin	Nominal (Vdc)	Margin (Vdc)	Regulator
V_{SS}	18U2	19.7	18.7 → 20.7	H side potentiometer
V_{BB}	18V2	≅23.2	22.2 → 24.2	H top potentiometer

On older regulators there is only one potentiometer. On new regulators, adjust both voltages simultaneously in the same direction.

CAUTION

Do not exceed margins, since overvoltage on V_{SS} ($V_{SS} > 20.7$ V) may damage MOS chips.

Side potentiometer adjusts V_{BB}. Top potentiometer adjusts $V_{BB} - V_{SS}$ i.e., the difference (3 to 4 volt range) between full output (V_{BB}) and reduced voltage output (V_{SS}). $V_{BB} - V_{SS}$ is normally set to 3.5 V.

Table 6
Noise On Matrix

Noise on a matrix is generally indicated by any or all of bits 8, 9, 10, and 11 being incorrect on precharge 2 or 3.

Noise can be observed on TTL CENABLE and WRITE PULSE lines into 3207 level shifters at E105 and E92.

To observe noise, look at E105 pin 11 (CENABLE) or pin 14 (WRITE PULSE) and run a BR. instruction at location with maximum address lines asserted. For example, if the second 4K matrix is being tested, run 000777 at location 037774. If noise spikes of 2.0 V or more are observed, the board is marginal and may fail, depending on the 3207 input thresholds. The 3207A-1 tends to aggravate the problem.

Table 7
PDP-11/45 Voltage Check Points

Regulator Slot Location	Supply	Measure at Pin	Voltage (Vdc)	Ripple P-P (Vdc)	Regulator Slot Location	Supply	Measure at Pin	Voltage (Vdc)	Ripple P-P (Vdc)
Slot A	H744 + 5 V (FPP)	A02 A2	+5.0	0.15	Slot H	H744 + 5 V (bipolar)	A19 A2	+5.0	0.15
Slot B	H744 + 5 V	A06 A2	+5.0	0.15	Slot J	H744 + 5 V	A16 A2	+5.0	0.15
Slot C	H744 + 5 V	A10 A2	+5.0	0.15	Slot K	H744 + 5 V (bipolar)	A21 A2	+5.0	0.15
Slot D	H744 + 5 V	A26 A2	+5.0	0.15	Slot L	H744 + 5 V (bipolar)	A24 A2	+5.0	0.15
Slot E	H745 - 15 V	E02 B2	-15.0	0.15	Top Bulk*	H742 (switched)	E15 A1	+15.0 (13.5–16.5)	0.45
Slot H*	H746 MOS	A17 V2	+23.2	0.70	Top Bulk	H742 (switched)	E01 B1	+8.0 (6.8–9.2)	0.24
Slot H*	H746 MOS	A17 U2	+19.7	0.60	Bottom Bulk*	H742 (unswitched)	E16 B2 & E21 B2	-15.0 (-13.5 to -16.5)	0.45
Slot H*	H746 MOS	F17 C1	-5.0	0.15					

*Check these voltages in reference to MOS problems.

Table 8
Refresh Timing Check

REFRESH CLOCK H (E127 PIN 11)

Deposit a branch self (000777) at any location within MOS. Use a maintenance card to single TP through the instruction a couple of times. Examine the location to see if the instruction is still there.

Table 9
Forcing MOS Timing

B ETCH M8110 REV E2

1. Jumper E12711 (REFRESH CLOCK H) to E3604 (PWRS MEM DC LO L) forcing A DONE L. This procedure does not find a problem in the DONE flip-flop or associated circuitry.
2. To force DONE circuitry, put scotch tape over finger CK 2 (BUST OUT).
3. Jumper E12711 to E4104 (BUST OUT) E5404 [RREQ B (L)] to E0611 (MEM H).
4. This does not generate MEM SYNC (B) L at E5506. To check this, gate jumper E5502 to E4013.
5. To force a BREQ, jumper E12711 to E10010.

C ETCH M8110 REV H

1. PWRS MEM DC LO L is at E3704.
2. Same
3. BUST OUT is at E4204; MEM H is at E0603.
4. Same

NOTES ON FLOWCHART

The note numbers correspond to the numbers on the flowchart.

[1] If this is an add-on or if the controller or the matrix have been reassigned to new addresses, the jumpers may be wrong. An indication of this is a deposit of 0s that read back as 1s.

The types of problem indications due to incorrect controller (M8110) timing are too numerous to be listed here.

Installation procedures for MOS only and for MOS-and-Bipolar systems are also included in Table 1. These procedures show the power supply and power distribution requirements for these systems.

[2] Various ECOs fix related MOS problems. Processor ECOs should also be checked: they may help fix some problems which are not documented.

[3] This is the simplest function that can be performed.

[4] If software like RSTS-E or some customer software fails, it might take a long time for diagnostics to fail or they might not fail at all.

RUN is defined as a minimum of 15 minutes per matrix.

[5] To test Unibus side of controller.

[6] If no failure occurs at nominal voltages, margins might help locate the problem.

[7] If no problem can be found, this is the only thing left to try. Jumpers and timing must be checked after installing new modules.

[8] If the system has been replaced and the software still will not run, and if the problem is definitely an MOS problem, support is needed.

[9] A C etch G401 cannot be ECOed to fix noise problems. A D etch G401 can be ECOed to fix noise problems.

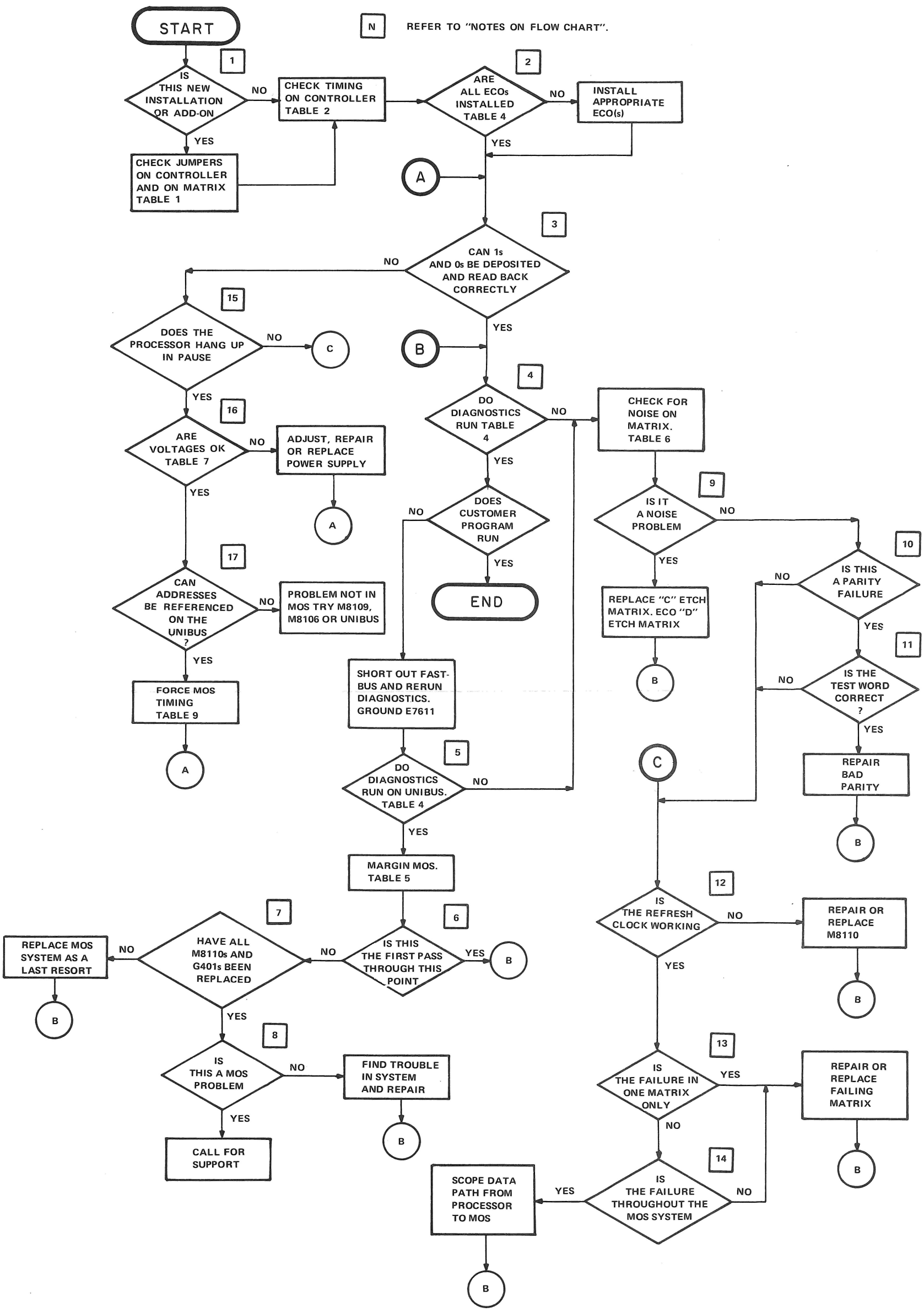
A C etch G401 should not cause noise problems if less than half of the 37 level shifters are 3207A-1s.

[10] [11] To check if a parity failure is caused by a parity IC or a data IC.

[12] Data storage problems in a matrix are generally caused either by a missing voltage or by an inoperative refresh clock.

[13] [14] To determine if the failure is in the matrix or elsewhere in the system.

[15] [16] [17] To find out why the processor is hanging up in PAUSE.



PDP-11/45, 11/50 MOS Troubleshooting Chart

Reader's Comments

PDP-11/45 MOS MEMORY
TROUBLESHOOTING GUIDE
DEC-11-HMSTS-A-D

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