pdp11

DZ11
maintenance manual

digital

EK-DZ11-MM-PRE

DZ11
maintenance manual

PRELIMINARY

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CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The DZ11 is an asynchronous multiplexer that provides an interface between a PDP-11 processor and eight (8) asynchronous serial lines. It can be used with PDP-11 systems in a variety of applications that include communications processing, time sharing, transaction processing and real time processing. Local operation to terminals or computers is possible at speeds up to 9600 baud using either EIA RS232C interfaces or 20 mA current loop signaling. Remote operation using the public switched telephone network is possible with DZ11 models offering EIA RS232C interfaces. Enough data-set control is provided to permit dial up (auto answer) operation with modems capable of full duplex* operation such as the Bell models 103 or 113 or equivalent. Remote operation over private lines for full duplex* point to point or full duplex* multipoint as 2 control (master) station is also possible. Figure 1-1 depicts several of the possible applications for the DZ11 in a PDP-11 system.

The DZ11 has several features that provide flexible control of communications' parameters such as baud rate, character length, number of stop bits for each line, odd or even parity for each line, and transmitter–receiver interrupts. Additional features include limited data set control, zero receiver baud rate, break generation and detection, silo buffering of received data, module plug-in to hex SPC slots, and line turnaround.

Each DZ11 module provides for operation of eight (8) asynchronous serial lines. Since the module interfaces to these channels with a sixteen (16) line distribution panel, two (2) DZ11 modules can be used with one panel. Also note that the two versions of the DZ11 (EIA or 20 mA output) consists of different module and panel types. This fact allows a system to mix EIA and 20 mA by using multiple DZ11s.

1.2 PHYSICAL DESCRIPTION

The DZ11 (8-line configuration) comprises a single hex SPC module and a 5.25-inch, unpowered distribution panel, connected by a 15-foot ribbon cable. Several types of interconnecting cables are used between the distribution panel and the modem or terminal, depending on the device. A 16-line configuration uses two modules and a single distribution panel connected by two ribbon cables. The DZ11 modules and distribution panel are shown in Figures 1-2 and 1-3. The subsequent paragraphs present a detailed description of the physical and electrical specifications of the various DZ11 options and configurations.

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*The DZ11 data-set control does not support half duplex operations or the secondary transmit and receive operations available with some moderns such as the Bell model 202, etc.

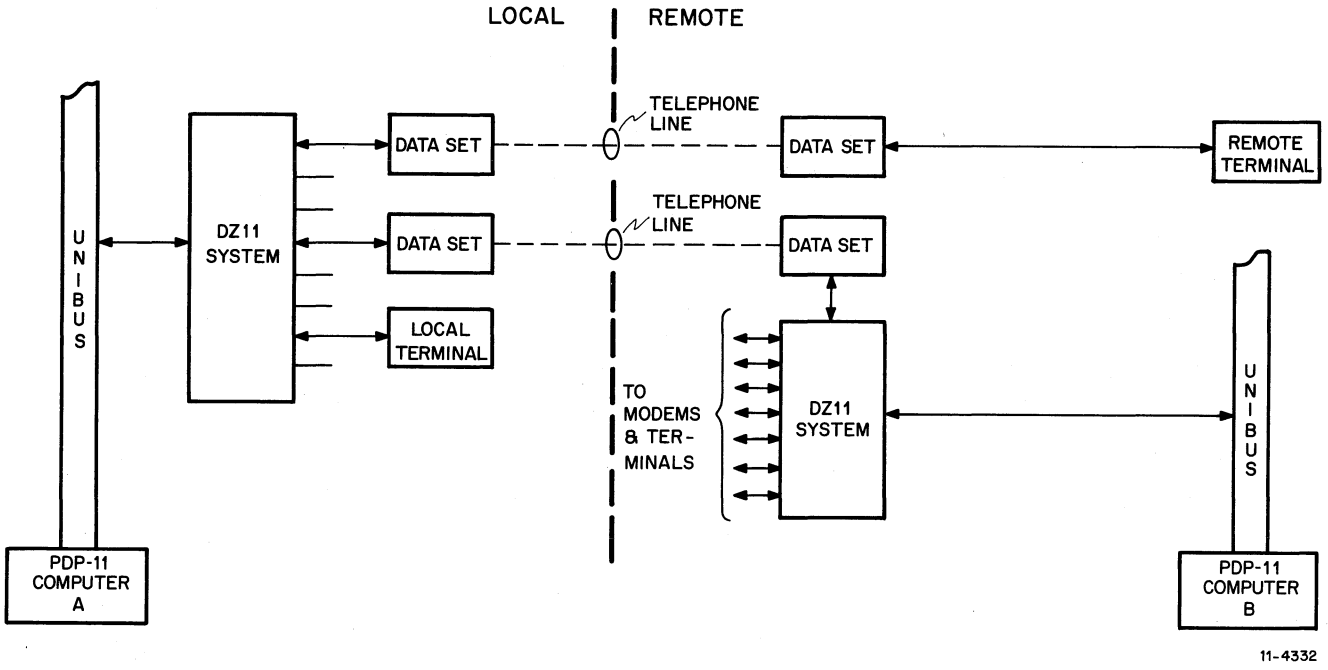
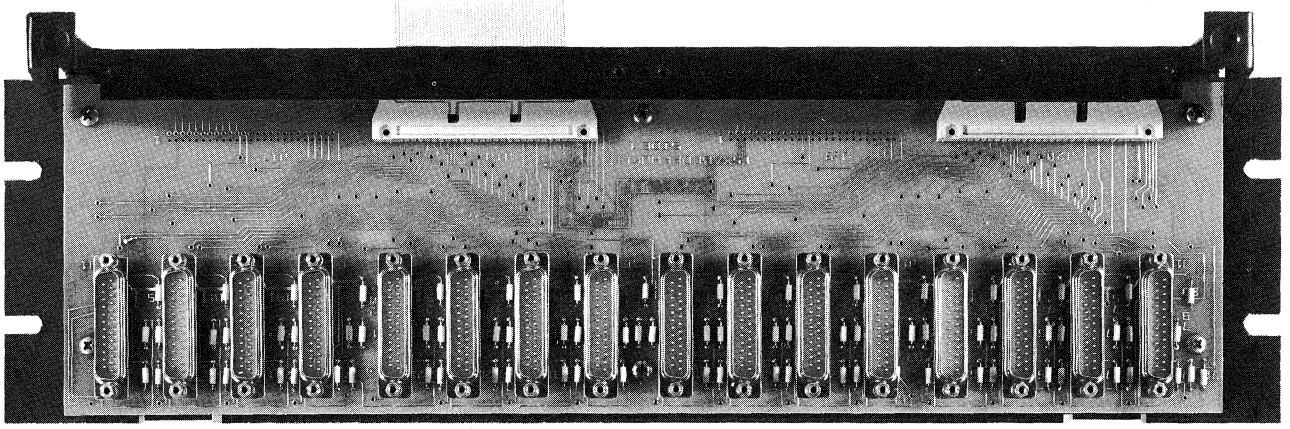
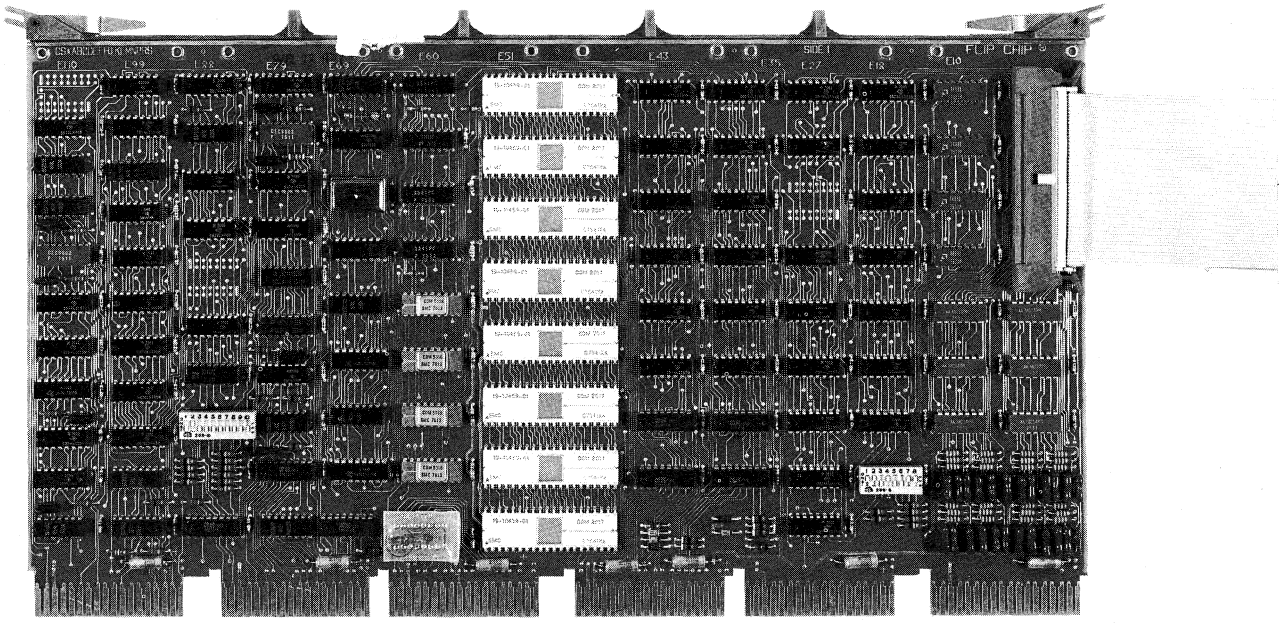


Figure 1-1 DZ11 System Applications



DISTRIBUTION
PANEL



M7819

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Figure 1-2 DZ11 EIA Module (M7819), and
Distribution Panel (H317-E)

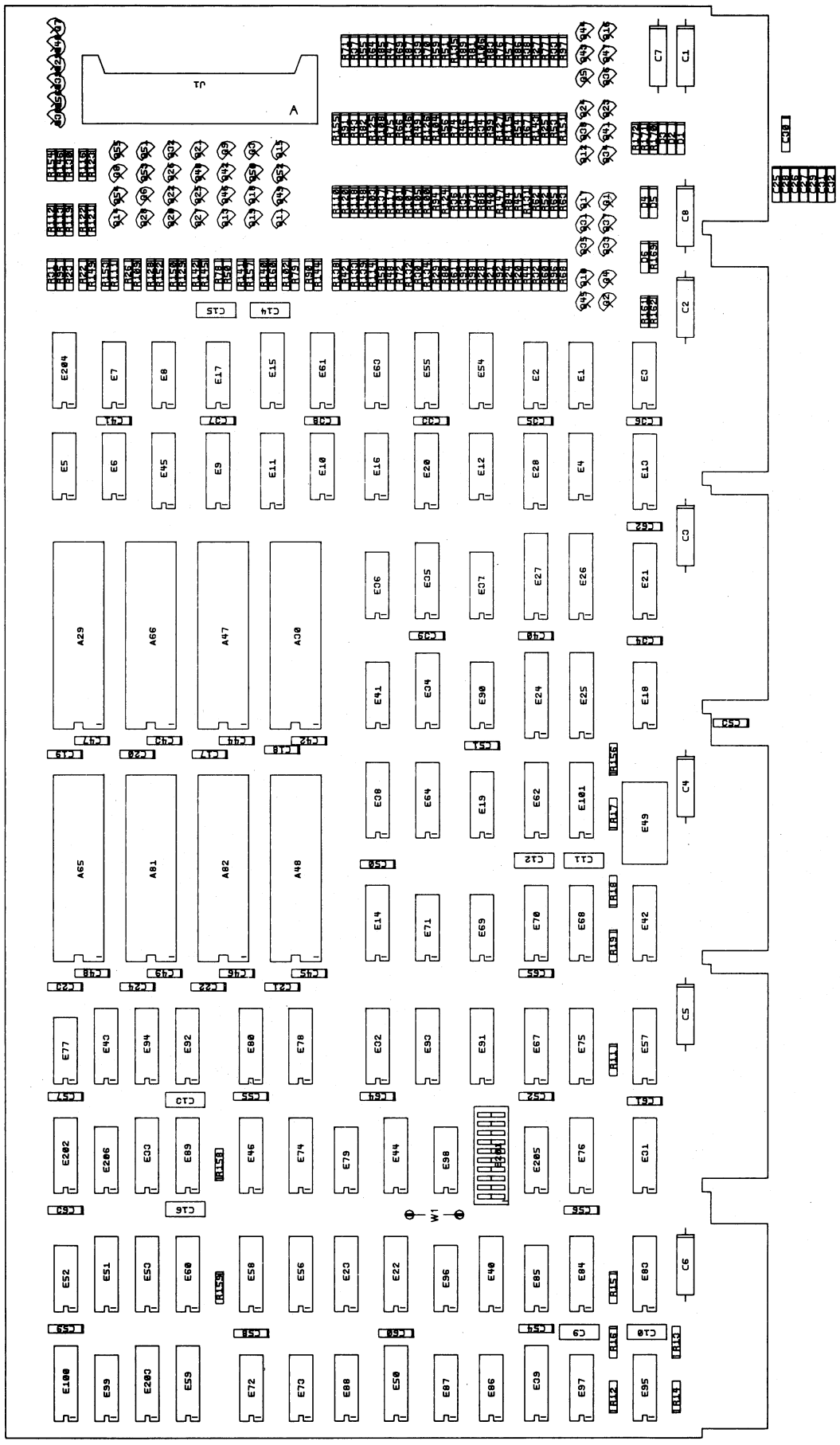


Figure 1-3 DZ11 20 mA Module (M7814)

1.2.1 DZ11 Configurations

The DZ11 can be supplied in six different configurations, each designated by a suffix letter (A, B, C, D, E, or F). The DZ11-A and the DZ11-B options are EIA devices with partial modem control. The DZ11-E is the combination of a DZ11-A and a DZ11-B. The DZ11-C and the DZ11-D are 20-mA loop output versions. The DZ11-F is the combination of a DZ11-C and a DZ11-D. Table 1-1 shows the various option configurations and the required hardware for the various configurations is shown in Figure 1-4.

Table 1-1 DZ11 Model Configurations

Model	Output	Module	Panel	Connector
DZ11-A	EIA	M7819	H317-E	H325/H327
DZ11-B	EIA	M7819	—	H327
DZ11-E	EIA	*M7819	H317-E	H325/*H327
DZ11-C	20 mA	M7814	H317-F	—
DZ11-D	20 mA	M7814	—	—
DZ11-F	20 mA	*M7814	H317-F	—

* = quantity of two

The DZ11-A and DZ11-B each utilize an M7819 module that plugs into slot 2 or 3 of a DD11-B, or any system unit with a hex SPC slot; however, slots in the PDP-11/20 BA11 box cannot be used. The H317-E distribution panel provides 16 communications' lines from two M7819 modules (8 lines per module), and is included with the DZ11-A and DZ11-E configurations. The H317-F distribution panel provides 16 lines for the DZ11-C and DZ11-F configurations, which utilize the M7814 modules (20-mA system). The distribution panels require no power and can be mounted in an H960 19-inch cabinet.

Modems or terminals are connected to the H317-E, the EIA panel, by cables that attach to its 16 cinch DB25P connectors. These cables are not provided by the DZ11, therefore are bought separately by the customer. The BC05D-25 cable is recommended for data set to telephone line interconnections, and the BC03M cable is recommended for local terminal interconnections. A BC05W-15, 50-conductor flat shielded cable connects from the M7819 module to the EIA panel. This conductor carries the data and control signals of all 8 lines. Connections between terminals and the H317-F, the 20 mA panel, are by customer supplied cables to its 16 four screw terminal strips. The data and control signals of all 8 lines are carried to the distribution panel by a BC08S-15 40 conductor, flat shielded ribbon cable.

Two accessory test connectors, H325 and H327, are provided with each DZ11-A, and the H327 is provided with the DZ11-B. The H325 plugs into an EIA connector on the distribution panel to loop back data and modem signals onto a single line. The H327 connector plugs into the M7819 module socket housing and staggers the data and modem lines as shown in Figure 1-5. The connectors are shown in Figure 1-6.

A priority level 5 insert plugs into a socket on the M7819 module to establish interrupts at level 5 on the Unibus.

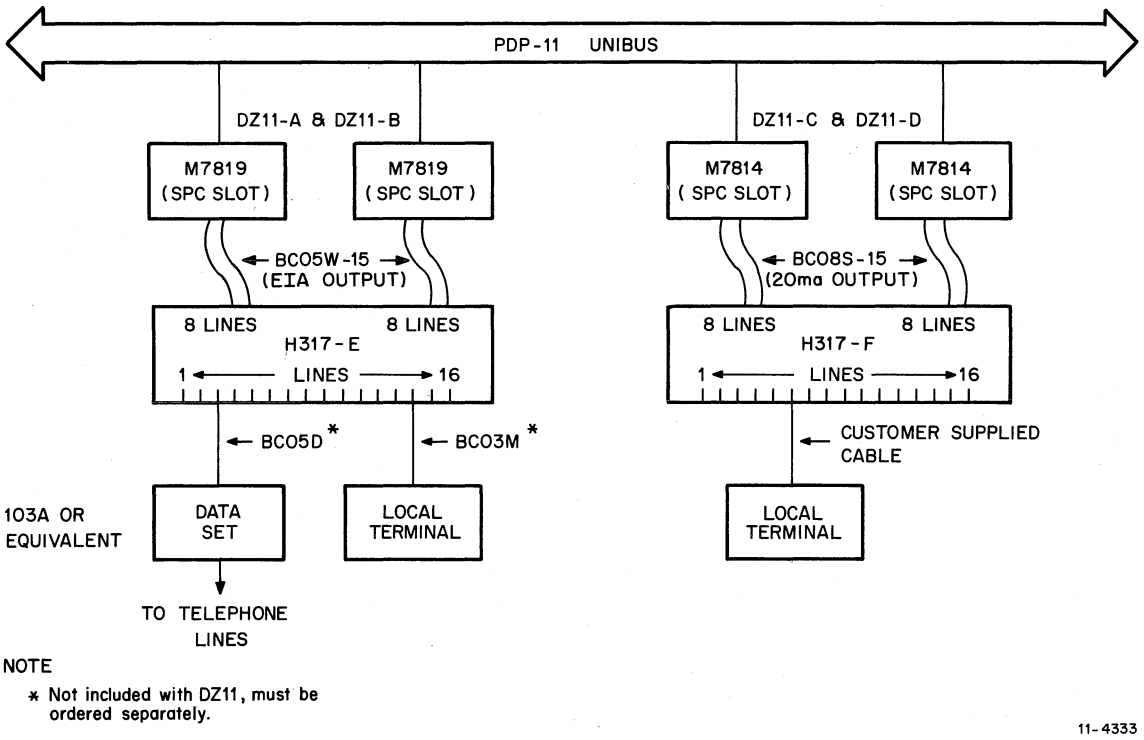


Figure 1-4 DZ11 Hardware Interconnections

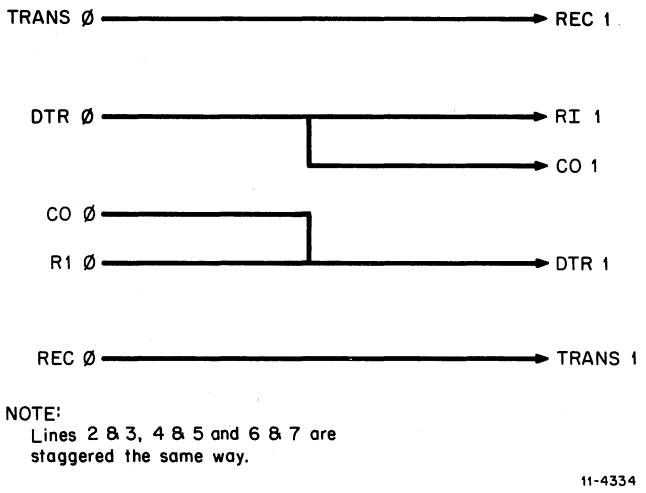
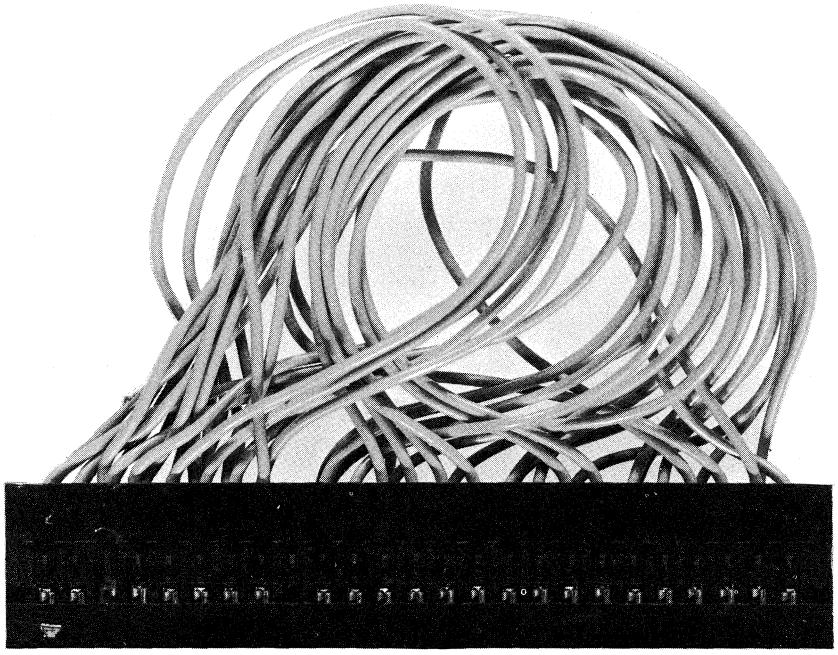
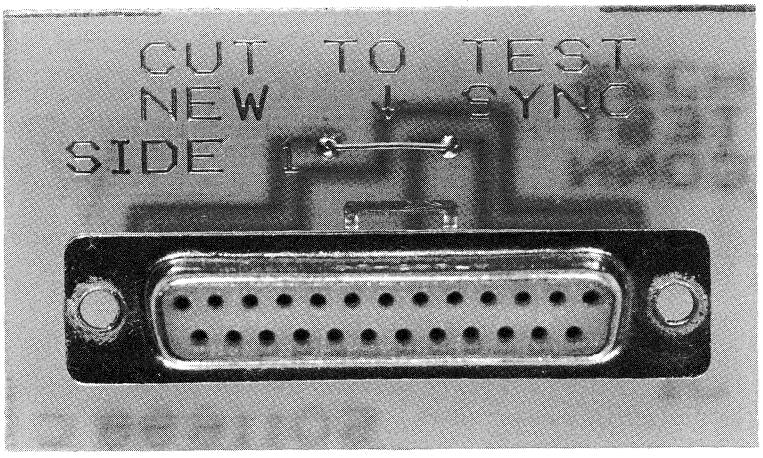


Figure 1-5 Line Turnaround



H327



H325

7974-3

Figure 1-6 Test Connectors, H327 and H325

1.2.2 General Specifications

The following are electrical, environmental, and performance specifications for all DZ11 configurations:

OUTPUTS

DZ11-A, -B, and -E

For each line, the DZ11 provides a voltage level interface whose levels and connector pinnings conform to ELECTRONIC INDUSTRIES ASSOCIATION (EIA) standard RS232C and CCITT recommendation V.24. The leads supported by this option are:*

a. Circuit AA (CCITT 101) - Pin 1 Protective ground
b. Circuit AB (CCITT 102) - Pin 7 Signal ground
c. Circuit BA (CCITT 103) - Pin 2 Transmitted data
d. Circuit BB (CCITT 104) - Pin 3 Received data
e. Circuit CD (CCITT 108.2) - Pin 20 Data terminal Ready
f. Circuit CE (CCITT 125) - Pin 22 Ring indicator
g. Circuit CF (CCITT 109) - Pin 8 Carrier

NOTE
Signal ground and Protective ground are connected together.

*Circuit CA (CCITT 105), Request to Send, is connected to circuit CD (DTR) through a jumper on the distribution panel. This allows the H325 connector to turn around DTR into both CO and RI (circuits CF and CE). It also allows control of the Request to Send (RTS) (CA) line for modem data set 202 applications.

DZ11-C, -D, and -F

20 mA loop versions. SPEC will be supplied at a later date.

INPUTS

The PDP-11 Unibus is the input for all DZ11s. The DZ11-A, B, C, and D presents one unit load to the Unibus and the DZ11-E and -F present two unit loads to the Unibus.

Power Requirements, DZ11-A, -B, and -E*

Typical	Maximum	
2.2	2.5	amperes at + 5.0 volts, dc
0.13	0.15	amperes at -15.0 volts, dc
0.1	0.13	amperes at +15.0 volts, dc

*DZ11-E power is twice the above values

Power Requirements, DZ11-C,-D, and -F

To Be Supplied

Environmental Requirements, all DZ11s

Class C Environment Operating Temperature:	5° C to 40° C* (50° C to 122 ° F)
Relative Humidity:	10% or less to 95%, with a maximum wet bulb of 32° C (90° F) and a minimum dew-point of 2 ° (36° F)

*Maximum operating temperature is reduced 1.8° C per 1000 meters (1.0° F per 1000 feet) for operation at altitude.

Cooling

DZ11-A, -B, and -E: Air flow 3 cu. feet/min.

DZ11-C, -D, and -F: To Be Supplied

Heat Dissipation

DZ11-A, -B, and -E: 57 Btu/hr

DZ11-C, -D, and -F: To Be Supplied

Distortion

DZ11-A, -B, and -E

The maximum "space to mark" and "mark to space" distortion allowed in a received character is 40%.

The maximum speed distortion allowed in a received character for 2000 baud is 3.8%. All other baud rates allow 4%.

The maximum speed distortion from the transmitter for 2000 baud is 2.2%. All other baud rates have less than 2%.

Table 1-2 lists the performance parameters of DZ11 operation.

Interrupts

RDONE – Occurs each time a character appears at output of the silo.

SA – Silo Alarm, occurs after 16 characters enter the silo. Rearmed by reading the silo. This interrupt disables the RDONE interrupt.

TRDY – Occurs when the scanner finds a line ready to transmit on.

NOTE: There are no modem interrupts.

Table 1-2 DZ11 Performance Parameters

Operating Mode:	Full Duplex		
Data Format:	Asynchronous, serial by bit, one start and 1, 1-1/2 (5 level codes only), or 2 stop bits supplied by the hardware under program control.		
Character Size:	5, 6, 7, or 8 bits – program selectable. (Does not include parity bit.)		
Parity:	Parity is program selectable. There may be none, or it may be odd or even.		
Bit Polarities	Unibus	Interface	EIA Out
MODEM DATA	Low = 1 High = 0	High = 1 Low = 0	Low = 1 = MARK High = 0 = SPACE
MODEM CONTROL	Low = 1 High = 0	High = 1 Low = 0	Low = OFF High = ON
Order of Bit Transmission/reception	Low order bit first		

Interrupt Level

Normally Level 5 is supplied. It can be modified by a priority plug.

Maximum Configuration

16 DZ11 modules per Unibus

Distance

DZ11-A, -B, and -E:

50 feet – up to 9600 baud, if cable is less than 2500 pf.

DZ11-C, -D, and -F:

To Be Supplied

1.3 FUNCTIONAL DESCRIPTION

The following paragraphs present a general description of DZ11 operation. A more detailed description is found in Chapter 3 (Programming) and Chapter 4 (Theory of Operation). Figure 1-7 is a general functional block diagram that divides the DZ11 into three basic components: Unibus Interface, Control Logic, and Line Interface.

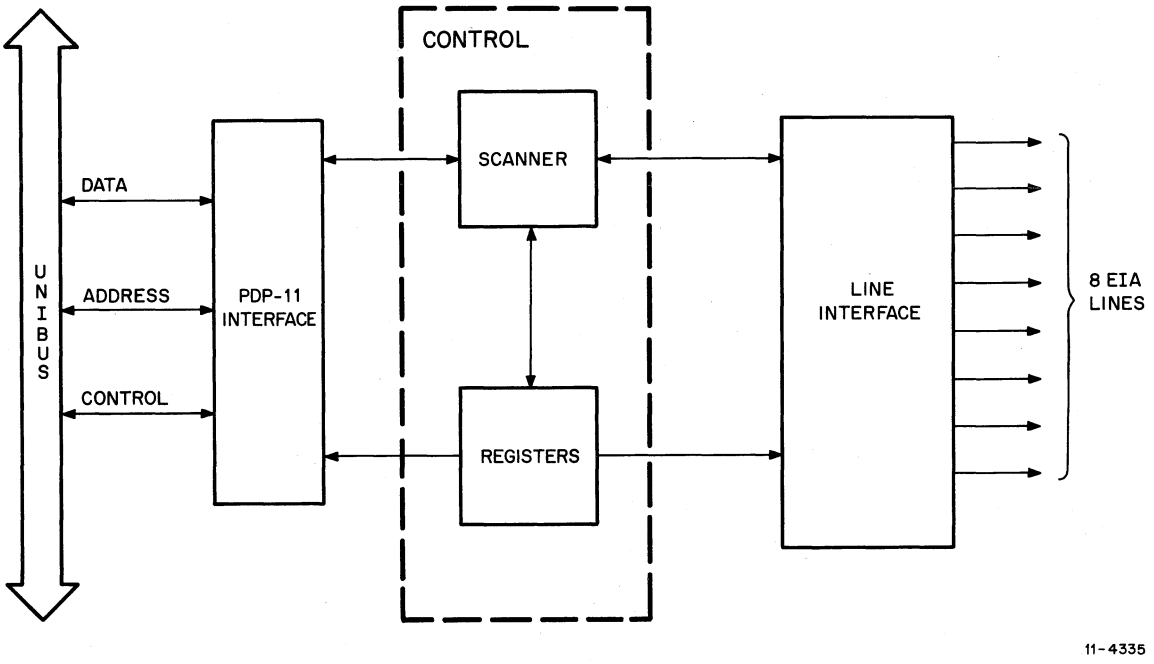


Figure 1-7 General Functional Block Diagram

1.3.1 PDP-11 Unibus Interface

The PDP-11 Unibus Interface component of the DZ11 handles all transactions between the Unibus and the DZ11 Control Logic. The Unibus Interface performs three functions: data handling, address recognition, and interrupt control. In its data handling function, the Interface routes data to and from the various registers in the Control Logic and provides the voltage conditioning necessary to transmit and receive data to and from the PDP-11 Unibus. The address recognition and control logic activates the proper load and read signals when it recognizes its preselected address on the Unibus. These signals are used by the data handling function to route the incoming and outgoing data to the desired locations. The interrupt control function initiates and controls interrupt processing between the DZ11 and the PDP-11 processor.

1.3.2 Control Logic

The Control Logic provides the required timing and control signals to handle all transmitter and receiver operations. The Control Logic can be divided into two major sections: the scanner and the registers. The scanner continuously examines each line in succession, and based on information from the Line Interface and the registers, it generates signals that causes data to flow to or from the appropriate line. The scanner comprises a 5.068 MHz oscillator (clock), a 64-word FIFO receiver buffer, a four-phase clocking network, and other control generating logic.

The DZ11 uses four Device Registers in a manner that yields six unique and accessible registers, each having a 16-bit word capacity. The six discrete registers temporarily store input and output data, monitor control signal conditioning, and establish DZ11 operating status. Depending on their functions, some of the registers are accessible in bytes or words; others are restricted to word-only operation. Registers can be read or loaded (written), depending on the operation. The ability to read or write a register allows the use of two of the Device Registers as four independent registers.

1.3.3 Line Interface

Two of the most important operations in the DZ11 are the conversions from serial-to-parallel and parallel-to-serial data formats. These conversions are required since the DZ11 is located between the PDP-11 Unibus (a parallel data path) and either local terminals or telephone lines (serial data paths). Conversions for each line in the DZ11 are performed by independent Universal Asynchronous Receiver–Transmitter (UART) integrated circuits. Another component of the Line Interface, the Line Receiver or Driver, converts the TTL voltage levels in the DZ11 so that they correspond to those in the external device input lines (modem or terminal).

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter contains the procedures for the unpacking, installation, and initial checkout of the DZ11 Asynchronous Multiplexer. More detailed checkout procedures are outlined in Chapter 5 of this manual.

2.2 CONFIGURATION DIFFERENCES

The DZ11 can be supplied with or without a Distribution panel. The DZ11-B and -D do not have Distribution panels. The following list describes the variations:

DZ11-A EIA level conversion with distribution panel
DZ11-B EIA level conversion without distribution panel
DZ11-C 20-mA loop conversion with distribution panel
DZ11-D 20-mA loop conversion with distribution panel
DZ11-E DZ11-A and DZ11-B with distribution panel
DZ11-F DZ11-C and DZ11-D with distribution panel

2.3 UNPACKING AND INSPECTION

The DZ11 is packaged in accordance with commercial packaging practices. First, remove all packing material and check the equipment against the shipping list. Damage or shortages should be reported to the shipper immediately, and notification given the DEC representative. Inspect all parts and carefully inspect the module for cracks, loose components, and separations in the etched paths.

2.4 INSTALLATION PROCEDURE

The following procedure should be followed to completely check and install the DZ11 module in a PDP-11 system:

1. Check the shipment for a complete agreement with the shipping list. The following items per configuration should be supplied:

Quantity	Description	A	B	E	C	D	F
1	M7819 Module	x	x	*			
1	H327 Test Connector	x	x	*			
1	Priority Insert (5)	x	x	*			
1	H317-E Distribution Panel Assembly	x		x			
1	H325 Test Connector	x		x			
1	BC05W-15 Cable	x	x	*			
1	Panel Mounting Hardware Set	x		x			
1	Printset (B-TC-DZ11-0-6)	x		x			
1	Printset (B-TC-DZ11-0-10)			x			
1	Software Kit	x		x			
1	DZ11 Maintenance Manual	x		x			
1	M7814 Module				X	X	*
1	BC08S Cable				X	X	*
1	Printset (DZ11-C and F)				X		X
1	Printset (DZ11-D)						X

*The DZ11-E shipment contains two of the items listed.

2. Check all parts for damage.

3. Install the H317 Distribution Panel according to the Unit Assembly Drawing D-UA-DZ11-0-0.

4. Check to ensure that all of the machine-insertable jumpers on the Distribution Panel are in place. See Drawing D-CS-5411928-0-1 in the Printset for jumper locations.

5. Module Installation

   a. Check the module(s) for obvious damage.

   b. Ensure that the Priority Insert (level 5) is properly seated in socket E52 on the module(s). Refer to drawing D-UA-M7819-0-0.

   c. Refer to Chapter 3, the paragraph describing Address Selection, and set the switches at E81 such that the module will respond to its assigned address. (Refer to Chapter 3 for the address assignment scheme.) When a switch is closed, a binary 1 is decoded, and an open switch decodes as a binary 0. Note that the switch labeled #1 corresponds to bit 3, #2 corresponds to bit 4, etc.

d. Vector selection is accomplished by the eight-position switch at E11. Switch position #1 and #8 are not used. Switch position #2 corresponds to vector bit 3, #3 corresponds to vector bit 4, etc. An open switch decodes as binary 1, and a closed switch decodes as binary 0.

e. Ensure that the H327 Test Connector is properly installed at J1 (the cable connector at the top of the module).

f. Insert the module in its SPC slot and run Diagnostics in the staggered mode to verify module operation. Refer to MAINDEC-11-DZDZA, the diagnostic listing, and to Chapter 5, Programming, of this manual for the correct procedure. Run at least two passes without error.

CAUTION

Insert and remove modules slowly and carefully to avoid snagging module components on the card guides, and possibly changing switch settings inadvertently.

g. Replace the H327 Test Connector with the BC05W-15 cable (RIB-SIDE UP), and observe the same caution as in Step f above. Insert the other end of the cable (SMOOTH-SIDE UP) at J18 or J20 of the Distribution panel. BE CERTAIN THAT THE CORRECT SIDE OF THE CABLE IS UP IN EACH CASE! See Figure 2-1.

h. Connect the H325 (or an H315) connector to the first line and run the Diagnostics in External mode. Repeat this step for each line.

i. Run DEC/X11 System Exerciser to verify the absence of Unibus interference with other system devices.

j. The DZ11 is now ready for connection to external equipment. If the connection is to be made to a terminal, a null modem cable must be used. The BC03M, H312-A, or BC03P null modem cables will suffice for connection between the Distribution panel and the terminal. However, if the H312-A null modem unit is used, two BC05D EIA cables (one on each side of the null modem unit) are required. If connection is to be made to a Bell 103 or equivalent modem, a BC05D-25 feet cable is required between the Distribution panel and the modem. All of the cables mentioned in this step must be ordered separately as they are NOT components of a standard DZ11 shipment.

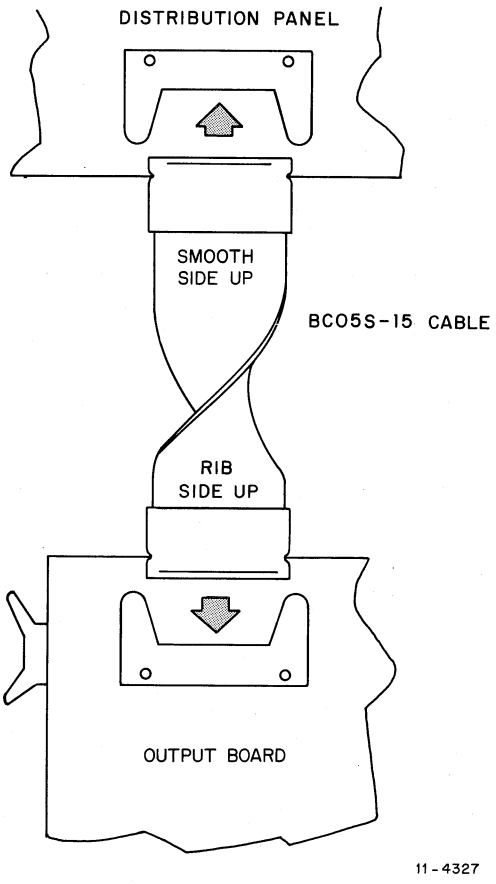


Figure 2-1 BC05W-15 Interconnection

CHAPTER 3
PROGRAMMING

3.1 INTRODUCTION

This chapter provides basic information for programming DZ11 system operation. A description of each DZ11 register, its format, programming constraints, and bit functions are presented to aid programming and maintenance efforts. Special programming features are also presented in this chapter.

3.2 REGISTER BIT ASSIGNMENTS

A comprehensive pictorial of all register bit assignments is shown in Figure 3-1. The four device registers (DR0, DR2, DR4, and DR6) are subdivided to form six unique registers. This subdivision is accomplished in DR2 and DR6 by assigning read-only (RO) or write-only (WO) status to each register. Since the reading and writing of DR2 and DR6 accesses two registers, PDP-11 processor instructions that perform a read-modify-write (DATIP) bus cycle cannot be used with DR2 or DR6. Also, DR2 permits only word instructions, but either byte or word instructions may be used with DR6. DR0 and DR4 have no programming constraints. In all register operations, the following applies: read-only bits are not affected by an attempt to write, and write-only and "not-used" bits appear as a binary 0 if a read operation is performed. Specific programming constraints for each register are discussed in the subsequent paragraphs. A description of each bit function is presented in Tables 3-1 through 3-3.

The DZ11's device and vector addresses are selected from the floating vector and device address space.

NOTE: The device floating address space is 160010_8 to 163776_8.
The vector floating address space is 300_8 to 776_8.

Its floating address space follows the DJ11; DH11; DQ11; DU11; DUP11; LK11; and DMC11.

Its floating vector space follows the DC11; KL11/DL11-A, B; DP11; DM11-A; DN11; DM11-BB and other modem control vectors; DR11-A; DR11-C; PA611 reader, PA611 punch; DT11; DX11; DL11-C, D, E; DJ11; DH11; GT40; LPS11; DQ11; KW11-W; DU11; DUP11; DV11; LK11-A; DWUN; and DMC11. If a DZ11 is installed in a system with any of the above listed options, then its assigned vector and device address should follow the vector and device address of the other options.

Two examples follow:

First, the simplest case where there is only one DZ11:

Option	Address	Vector	Comment
GAP	160010		No DJ11s
GAP	160020		No DH11s
GAP	160030		No DQ11s
GAP	160040		No DU11s
GAP	160050		No DUP11s
GAP	160060		No LK11s
GAP	160070		No DMC11s
DZ11	160100	300	
GAP	160110		No more DZ11s

Next, a system with one DJ11, one DH11, one GT40, one KW11-W and two DZ11s.

Option	Address	Vector	Comment
DJ11	160010	300	
GAP	160020		No more DJ11s
GAP	160030		DH11 must start on an address boundary that is a multiple of 20.
DH11	160040 160050	310	
GAP	160060		No more DH11s
GT40		320	GT40 address is not in the floating address space.
KW11-W		330	KW11-W address is not in the floating address space.
GAP	160070		No DQ11s
GAP	160100		No DU11s
GAP	160110		No DUP11s
GAP	160120		No LK11s
GAP	160130		No DMC11s
DZ11	160140	340	
DZ11	160150	350	
GAP	160160		No more DZ11s

	BYTES HIGH MSB 15	14	13	12	11	10	09	08	LOW 07	06	05	04	03	02	01	LSB 00
CONTROL & STATUS (CSR)	RO TX RDY	RW TX INTR ENAB	RO SILO ALARM	RW SILO ALARM ENAB	NOT USED	RO TX LINE C	RO TX LINE B	RO TX LINE A	RO RX DONE	RW RX INTR ENAB	RW MAST SCAN ENAB	RW CLEAR	RW MAINT	NOT USED	NOT USED	NOT USED
RECEIVER BUFFER (RBUF)	RO DATA VALID	RO OVRN	RO FRAM ERR	RO PAR ERR	NOT USED	RO RX LINE C	RO RX LINE B	RO RX LINE A	RO RBUF D7	RO RBUF D6	RO RBUF D5	RO RBUF D4	RO RBUF D3	RO RBUF D2	RO RBUF D1	RO RBUF D0
LINE PARAMETER (LPR)	NOT USED	NOT USED	NOT USED	WO RX ON	WO FREQ D	WO FREQ C	WO FREQ B	WO FREQ A	WO ODD PAR	WO PAR ENAB	WO STOP CODE	WO CHAR LGTH B	WO CHAR LGTH A	WO LINE C	WO LINE B	WO LINE A
TRANSMIT CONTROL (TCR)	RW DATA TERM RDY 7	RW DATA TERM RDY 6	RW DATA TERM RDY 5	RW DATA TERM RDY 4	RW DATA TERM RDY 3	RW DATA TERM RDY 2	RW DATA TERM RDY 1	RW DATA TERM RDY 0	RW LINE 7	RW LINE 6	RW LINE 5	RW LINE 4	RW LINE 3	RW LINE 2	RW LINE 1	RW LINE 0
MODEM STATUS (MSR)	RO CO 7	RO CO 6	RO CO 5	RO CO 4	RO CO 3	RO CO 2	RO CO 1	RO CO 0	RO RING IND 7	RO RING IND 6	RO RING IND 5	RO RING IND 4	RO RING IND 3	RO RING IND 2	RO RING IND 1	RO RING IND 0
TRANSMIT DATA (TDR)	WO BRK 7	WO BRK 6	WO BRK 5	WO BRK 4	WO BRK 3	WO BRK 2	WO BRK 1	WO BRK 0	WO TBUF 7	WO TBUF 6	WO TBUF 5	WO TBUF 4	WO TBUF 3	WO TBUF 2	WO TBUF 1	WO TBUF 0

Figure 3-1 Register Bit Assignments

Table 3-1 CSR Bit Functions

Bit	Title	Function
0–2	Not Used	
3	MAINT	A read/write bit, when set, causes the serial output data from the transmitter to be fed back as serial input data to the receiver. All lines are turned around. Bit is cleared by BUS INIT and CLR.
4	CLR	A read/write bit that fires a one-shot to generate a 15-microsecond reset to clear the receiver silo, all UARTs, and the CSR. After a CLR is issued, the CSR and line parameters must be set again. CLR in progress is indicated by CLR = 1. Modem control registers are not affected, nor bits 00 through 14 of RBUF.
5	Master Scan Enable	A read/write bit that activates the scanner to enable the Receiver and Transmitter. Cleared by CLR and BUS INIT.
6	RCV INT Enable	A read/write bit that enables the receiver interrupt. Cleared by CLR and BUS INIT.
7	RDONE	A read only bit (hardware set) that generates a RCV INT if bit 06 = 1 and bit 12 = 0. The bit clears when the RBUF is read and resets when another word reaches the output of the silo (RBUF). If bit 06 = 0, RDONE can be used as a flag to indicate that the silo contains a character. If bit 12 = 1, RDONE does not cause interrupts but otherwise acts the same.
8–10	Tran Line #	When bit 15 = 1, these three read-only bits indicate that the line that is ready to transmit a character. Bit 15 clears when the character is loaded into the transmit buffer, but sets again if another line is ready. A new line number appears within a minimum of 1.9 microseconds. The bits 08–10 return to line 0 after a CLR or BUS INIT. These bits are meaningful only when bit 15 (TRDY) is true.
11	Not Used	
12	SAE (Silo Alarm Enable)	A read/write bit that enables the silo alarm and prevents RDONE from interrupting if RIE (bit 06 = 1). If bit 06 = 1, the SAE allows the SA (bit 13) to cause an interrupt after 16 entries in the silo. If bit 06 = 0, the SA can be used as a flag. The bit is cleared by CLR and RESET.

Table 3-1 CSR Bit Functions

Bit	Title	Function
13	SA (Silo Alarm)	A read-only bit set by hardware after 16 characters enter the silo that causes an interrupt if bit 06 = 1. Cleared by CLR, RESET, and reading the RBUF. When the silo flag occurs (SA = 1), the silo must be emptied to prepare the flag for recognition of 16 additional characters.
14	TIE (Tran Int Enab)	A read/write bit that allows an interrupt if bit 15 = 1 (TRAN Ready).
15	TRDY (Tran Ready)	A read-only bit set by hardware when a line number is found whose buffer can be loaded and whose TCR bit has been set by the program. See bits 08–10 functional description

Table 3-2 RBUF Bit Functions

Bit	**Title**	**Function**
0–7	RCV Character	These bits contain the received character. If the selected code level is less than 8 bits wide, the high order bits are forced to zero.
8–10	Line Number	These bits present the line number on which the character was received.
11	Not Used	
12	Parity Error	This bit indicates whether the received bit had a parity error. The parity bit is generated by hardware and does not appear in the RBUF word.
13	Framing Error	This bit indicates improper framing (stop bit not a mark) of the received character, and can be used for break detection.
14	Overrun	This bit indicates receiver buffer overflow. The result is a received character which is replaced by another received character before storage in the silo. A character is lost but the received character put in the silo is valid.
15	Data Valid	This bit indicates that the character read from the silo (RBUF) is valid. The RBUF should read until the DV bit = 0, indicating an invalid character and empty silo. Bit is cleared by CLR and BUS INIT.

Table 3-3 LPR Bit Functions

Bit	Title	Function
0–2	Line Number	These bits select the line for parameter loading.
3–4	Character Length	These bits set the character length for the selected line. The parity bit is not part of the character length. 4 3 0 0 5 bits 0 1 6 bits 1 0 7 bits 1 1 8 bits
5	Stop Code	This bit sets the Stop Code length. (0 = One-unit stop, 1 = Two-unit stop or 1.5-unit stop if a 5-level code is employed.)
6	Parity	This bit selects the parity option (0 = No parity check, 1 = Parity enabled on TRAN and RCV.)
7	Odd Parity	This bit selects the kind of parity selected (0 = Even Parity Select, 1 = Odd Parity Select.) Bit 06 must be set for this bit to have effect.
8–11	Speed Select	These bits select the TRAN and RCV speed for the line selected by bits 0–2. Refer to Table 3-4 for list of available baud rates.
12	RCVR ON	This bit must be set when loading parameters to activate the receiver clock. (Transmitter clock is always on.)A CLR or BUS INIT turns the receiver clock off.
13–15	Not Used	

3.2.1 Control and Status Register (CSR)

The control and status register (CSR) contains the states of flags and enable bits for scanning, processor interrupts, clearing, and maintenance. The 16-bit CSR has no programming constraints. The CSR format is depicted in Figure 3-1, and bit functions are described in Table 3-1. Write-only and "not-used" bits read as zeros to the Unibus, and read-only bits are not affected by write attempts.

3.2.2 Receiver Buffer (RBUF)

The receiver buffer (RBUF) register contains the received character bits, with line identification, error status, and data validity flag. As one of two registers in DR2 (RBUF and LPR), RBUF is accessed when a read operation is performed on DR2 (write operation accesses the LPR). The RBUF register has several programming constraints which are:

1. Byte instructions cannot be used.
2. It is a "Read Only" register.

3. TST or BIT instructions cannot be used as they cause the loss of a character.

4. Bits 00 through 14 are not affected by CLR or BUS INIT. Bit 15 (Data Valid) is explained in Table 3-2.

The register format of RBUF is depicted in Figure 3-1, and bit functions are described in Table 3-2. Each reading of the RBUF register advances the silo and presents the next character to the program.

3.2.3 Line Parameter (LPR)

The line parameter register (LPR) is a 16-bit write only register that sets the parameters (character and stop code lengths, parity, speed, and receiver clock) for each line. Bits 00–02 select the line for parameter loading. Line parameters for each line must be reloaded after a CLR (bit 04 of CSR) or BUS INIT operation. The programming constraints for the LPR are:

1. BIS or BIC instructions are not allowed.
2. Byte operations have no effect.

The LPR format is depicted in Figure 3-1, and bit functions are described in Table 3-3.

3.2.4 Transmit Control (TCR)

The 16-bit (two-byte) transmit control register (TCR) has read and write capability. The TCR low byte corresponds to lines in the multiplexer, and when a line bit is set, it enables the scanner to transmit on the line. Line interrupts are generated by the AND condition of TCRXX • TRDY • TIE.

Clearing a TCR bit prevents the line from transmitting. To transmit to a line, the TBUF Register (DR6, low byte) is loaded with the desired character. The TCR high byte contains a DTR bit for each line. The TCR low byte is cleared by a CLR or BUS INIT; the high byte is cleared by BUS INIT only. To ensure transmission of the last character on a line, the TCR line bit must not be cleared for at least 2.0 microseconds after the character is loaded into the TBUF register.

3.2.5 Modem Status (MSR)

The modem status register (MSR) consists of two 8-bit, read-only registers. The low byte provides a ring indicator (RI) for each line, and the high byte reads the state of the carrier (CO) lead for each line. The MSR is the read-only component of DR6. The MSR is not affected by CLR and BUS INIT.

3.2.6 Transmit Data (TDR)

The transmit data register (TDR) is the write-only segment of DR6. The TDR constitutes two 8-bit registers, the low byte (TBUF) containing the character to be transmitted, and the high byte containing a BREAK bit for each line. If a BREAK bit is set, the line transmits zeros continuously. Clearing the BRK bit (CLR, BUS INIT, or writing zeros in the bit position) terminates the break condition. The break time interval is program controlled. The break feature cannot be used when the data lines are turned around by bit 03 of the CSR. For character lengths less than 8 bits, the character must be right-justified, as the most significant bits are forced to zero by the DZ11 hardware.

3.3 PROGRAMMING FEATURES

The DZ11 has several programming features that allow control of baud rate, character length, stop bits, parity, and interrupts. This section discusses the application of these controls to achieve the desired operating parameters.

3.3.1 Baud Rate

The selection of the desired transmission and reception speed is controlled by the conditions of bits 08 through 11 of the LPR. Table 3-4 depicts the required bit configuration for each operating speed. Also, the baud rate for each line is the same for both the transmitter and receiver. Furthermore, the receiver clock is turned on and off by setting and clearing bit 12 in the LPR for the selected line.

Table 3-4 Baud Rate Selection Chart

Bits				
11	**10**	**09**	**08**	**Baud Rate**
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Not Used

3.3.2 Character Length

The selection of one of the four available character lengths is controlled by bits 03 and 04 of the LPR. The bit conditions for bits 04 and 03, respectively, are as follows: 00 (5 level), 01 (6 level), 10 (7 level), and 11 (8 level). For character lengths of 5, 6, and 7, the high order bits are forced to zero.

3.3.3 Stop Bits

The length of the stop bits in a serial character string is determined by the 05 bit of the LPR. If bit 05 is a zero, the stop length is one unit; bit 05 set to a one selects a two-unit stop, unless the 5-level character length (bits 03 and 04 at zero) is selected, then the stop bit length is 1.5 units.

3.3.4 Parity

The parity option is selected by bit 06 of the LPR. Parity is enabled on transmission and reception by setting bit 06 to one. Bit 07 of the LPR allows selection of even or odd parity, and bit 06 must be set for bit 07 to be significant. The parity bit is generated and checked by hardware, and does not appear in the RBUF or TBUF. The parity error (bit 12, RBUF) flag is set when the received character had a parity error.

3.3.5 Interrupts

The Receiver Interrupt Enable (RIE) and Silo Alarm Enable (SAE) bits in the CSR control the circumstances upon which the DZ11 receiver interrupts the PDP-11 processor.

If RIE and SAE are both clear, the DZ11 never interrupts the PDP-11 processor. In this case, the program must periodically check for the availability of data in the SILO and empty the SILO when data is present. If the program operates off a clock it should check for characters in the SILO at least as often as the time it takes for the SILO to fill, allowing a safety factor to cover processor response delays and time to empty the silo. The RDONE bit in the CSR will set when a character is available in the SILO. The program can periodically check this bit with a TSTB or BIT instruction. When RDONE is set the program should empty the SILO.

If RIE is set and SAE is clear, the DZ11 will interrupt the PDP-11 processor to the DZ11 receiver vector address when RDONE is set, indicating the presence of a character at the bottom of the SILO. The interrupt service routine can obtain the character by performing a MOV instruction from the RBUF. If the program then dismisses the interrupt, the DZ11 will interrupt when a subsequent character is available (which may be immediately if additional characters were placed in the SILO while the interrupt was being serviced). Alternately, the interrupt service routine may respond to the interrupt by emptying the SILO before dismissing the interrupt.

If RIE and SAE are both set, the DZ11 will interrupt the PDP-11 processor to the DZ11 receiver vector when the SILO ALARM (SA) bit in the CSR is set. The SA bit will be set when sixteen characters have been placed in the silo since the last time the program has accessed the RBUF. Accessing the RBUF will clear the SA bit and the associated counter. The program should follow the procedure described in Paragraph 3.3.6 to empty the silo completely in response to a silo alarm interrupt. This will ensure that any characters placed in the silo while it is being emptied are processed by the program.

NOTE

If the program processes only 16 entries in response to each silo alarm interrupt, characters coming in while interrupts are being processed will build up without being counted by the silo alarm circuit and the silo may eventually overflow without the alarm being issued.

If the silo alarm interrupt is used, the program will not be interrupted if fewer than 16 characters are received. In order to respond to short messages during periods of moderate activity the PDP-11 program should periodically empty the silo. The scanning period will depend on the required responsiveness to received characters. While the program is emptying the silo it should ensure that DZ11 receiver interrupts are inhibited. This should be done by raising the PDP-11 processor priority. The silo alarm interrupt feature can significantly reduce the PDP-11 processor overhead required by the DZ11 receiver by eliminating the need to enter and exit an interrupt service routine each time a character is received.

The transmitter interrupt enable bit (TIE) controls transmitter interrupts to the PDP-11 processor. If enabled, the DZ11 will interrupt the PDP-11 processor to the DZ11 transmitter interrupt vector when the Transmitter Ready (TRDY) bit in the CSR is set, indicating that the DZ11 is ready to accept a character to be transmitted.

3.3.6 Emptying the Silo

The program can empty the SILO by repeatedly performing MOV instructions from the RBUF to temporary storage. Each MOV instruction will copy the bottom character in the SILO so it won't be lost and will clear out the bottom of the SILO, allowing the next character to move down for access by a subsequent MOV instruction. The program can determine when it has emptied the SILO by testing the DATA VALID bit in each word moved out of the RBUF. A zero value indicates that the SILO has been emptied. The test can be performed conveniently by branching on the condition code following each MOV instruction. A TST or BIT instruction must not access the RBUF because these instructions will cause the next entry in the SILO to move down without saving the current bottom character. Furthermore, following a MOV from the RBUF, the next character in the silo may be available within 1 microsecond. On fast CPUs, the program must use sufficient instructions or NOPs to ensure that successive MOVs from the RBUF are separated by at last 1 microsecond. This will prevent a false indication of an empty silo.

3.3.7 Transmitting a Character

The program controls the DZ11 transmitter through five registers on the Unibus: the Control and Status Register (CSR) previously mentioned, the Line Parameter Register (LPR), the Line Register, the Transmitter Buffer (TBUF) and the Break Register (BRK).

Following DZ11 initialization, the program must use the LPR register to specify the speed and character format for each line to be used and must set the Master Scan Enable (MSE) bit in the CSR. The program should set the Transmitter Interrupt Enable (TIE) bit in the CSR if it wants the DZ11 transmitter to operate on a program interrupt basis.

The Line Register is used to enable and disable transmission on each line. One bit in this eight bit register is associated with each line. The program can set and clear bits in this register by using MOV, MOVB, BIS, BISB, BIC and BICB instructions. (If word instructions are used, the Line and DTR registers will be simultaneously accessed.)

The DZ11 transmitter is controlled by a scanner which is constantly looking for an enabled line (Line bit set) which has an empty UART transmitter buffer. When the scanner finds such a line it loads the number of the line into the 3-bit Transmit Line Number (TLINE) field of the CSR and sets the TRDY bit, interrupting the PDP-11 processor if the TIE bit is set. The program can clear the TRDY bit by moving a character for the indicated line into the TBUF or by clearing the Line bit.

Clearing the TRDY bit frees the scanner to resume its search for lines needing service.

To initiate transmission on an idle line, the program should set the TCR bit for that line and wait for the scanner to request service on the line, as indicated by the scanner loading the number of the line into TLINE and setting TRDY. The program should then load the character to be transmitted into the TBUF by using a MOVB instruction. If interrupts are to be used, a convenient way of starting up a line is to set the TCR bit in the main program and let the normal transmitter interrupt routine load the character into the TBUF.

NOTE

The scanner may find a different line needing service before it finds the line being started up. This will occur if other lines request service before the scanner can find the line being started. The program must always check the TLINE field of the CSR when responding to TRDY to ensure it loads characters for the correct line. Assuming the program services lines as requested by the scanner, the scanner will eventually find the line being started. If several lines require service, the scanner will request service in priority order as determined by line number. Line 7 has the highest priority and line 0 the lowest.

To continue transmission on a line, the program should load the next character to be transmitted into the TBUF each time the scanner requests service for the line as indicated by TLINE and TRDY.

To terminate transmission on a line, the program may use either of two approaches. In the first approach the program clears the Line bit after loading the last character into the TBUF. The program must ensure that a minimum of 2 microseconds elapses between loading the TBUF and clearing the Line bit, otherwise the last character may be lost. In the second approach, the program loads the last character normally and waits for the scanner to request an additional character for the line. The program clears the TCR bit at this time instead of loading the TBUF.

The normal rest condition of the Transmitted Data lead for any line is the marking (1) state. The Break Register (BRK) is used to apply a continuous spacing signal to the line. One bit in this eight bit register is associated with each line. The line will remain in the spacing condition so long as the bit remains set. The program should use a MOVB instruction to access the BRK register. If the program continues to load characters for a line after setting the break bit, transmitter operation will appear normal to the program despite the fact that no characters can be transmitted while the line is in the continuous spacing state. The program may use this facility for sending precisely timed spacing signals by setting the break bit and using Transmit Ready interrupts as a timer.

It should be remembered that each line in the DZ11 is double buffered. The program must not set the BRK bit too soon or the two data characters preceding the spacing may not be transmitted. The program must also ensure that the line returns to the mark state at the end of the spacing period before transmitting any additional data characters. The following procedure will accomplish this. When the scanner requests service the first time after the program has loaded the last data character, the program should load an all-zero character. When the scanner requests service the second time, the program should set the BRK bit for the line. At the end of the spacing period the program should load an all-zero character to be transmitted. When the scanner requests service indicating this character has begun transmission the program should clear the BRK bit and load the next data character.

3.3.8 Data Set Control

DZ11 models with EIA interfaces include data set control as a standard feature. The program may sense the state of the Carrier and Ring Indicator signals from each data set and may control the state of the Data Terminal Ready signal to each data set.

The program uses three 8-bit registers to access the DZ11 data set control logic. One bit in each register is associated with each of the 8 lines. There are no hardware interlocks between the data set control logic and the receiver and transmitter logic. Any required coordination should be done under program control.

The Data Terminal Ready (DTR) register is a read/write register. Setting or clearing a bit in this register will turn the appropriate Data Terminal Ready signal on or off. The program may access this register with word or byte instructions. (If word instructions are used the DTR and Line registers will be simultaneously accessed.) The DTR register is cleared by the INIT signal on the Unibus but is not cleared if the program clears the DZ11 by setting the CLR bit of the CSR.

The Carrier Register (CAR) and Ring Register (RING) are read-only registers. The program can determine the current state of the carrier signal for a line by examining the appropriate bit of the CAR register. It can determine the current state of the ring signal by examining the appropriate bit of the RING register. The program can examine these registers separately by using MOVB or BITB instructions or can examine them as a single 16 bit register by using MOV or BIT instructions. The DZ11 data set control logic does not interrupt the PDP-11 processor when a carrier or ring signal changes state. The program should periodically sample these registers to determine the current status. Sampling at a high rate is not necessary.

3.4 PROGRAMMING EXAMPLES

The following five examples are sample programs for the DZ11 option. These examples are presented only to indicate how the DZ11 can be used.

Example 1 – Initializing the DZ11
The DZ11 is initialized by: a power-up sequence, a reset instruction, or a device clear instruction.

Device Clearing the DZ11

```
001000  012737  START:  MOV #20, DZCSR   ;Set bit 4 in the DZ11
001002  000020                          ;control and status
                                        ;registers.
001004  160100
001006  032737  1$:     BIT #20, DZCSR  ;Test bit 4.
001010  000020
001012  160100
001014  001374          BNE 1$          ;If bit 4 is still set, the
                                        ;branch condition is true
                                        ;and the device clear
                                        ;function is still in
                                        ;progress.
001016  000000          HALT            ;The device clear
                                        ;function is complete and
                                        ;the DZ11 has been
                                        ;cleared.
```

DZCSR = 160100 = control and status register address

Example 2 – Transmit binary count pattern on one line

```
001000  012737  START:  MOV #20, DZCSR   ;Set bit 4 in the DZ11
001002  000020                          ;control and status
                                        register.
001004  160100
001006  032737  1$:     BIT #20, DZCSR  ;Test bit 4.
001010  000020
001012  160100
001014  001374          BNE 1$          ;If bit 4 is still set, the
                                        ;branch condition is true
                                        ;and the device clear
                                        ;function is still in
                                        progress.
001016  012737          MOV #n, DZLPR   ;Load the parameters for
001020  001070                          ;line 0: 8 bit character;
001022  160102                          ;2 stop bit; 110 baud.
001024  012737          MOV #1, DZTCR   ;Enable line 0
                                        transmitter.
001026  000001
001030  160104
001032  012737          MOV #m, DZCSR   ;Set scanner enable bit
001034  000040                          ;5 in the control and
001036  160100                          ;status register.
001040  005000          CLR R0          ;Set binary count pattern
                                        ;to zero.
001042  005737  2$:     TST DZCSR       ;Test the transmitter
001044  160100                          ;ready flag (bit 15).
```

Example 2 (Cont)

```
001046    100375          BPL 2$          ;If branch condition is
                                          ;false, continue;
                                          ;otherwise test again.
001050    110037          MOVB R0, DZTDR  ;Load character to be
001052    160106                          ;transmitted.
001054    105200          INCB R0         ;Increment binary count.
001056    100371          BPL 2$          ;If branch condition is
                                          ;false, the binary count
                                          ;pattern is complete.
001060    000000          HALT
```

R0 = Register 0 = Binary Count Pattern
DZCSR = DZ11 Control and Status Register Address = 160100
DZLPR = DZ11 Line Parameter Register Address = 160102
DZTCR = DZ11 Transmit Control Register Address = 160104
DZTDR = DZ11 Transmit Data Register Address = 160106

Example 3 – Transmit a binary count to a terminal in Maintenance Loopback mode, with the receiver "On" in the interrupt mode. Transmit received data to console.

```
001200    005000          CLR R0          ;Set binary count to zero.
001202    012701          MOV 1400, R1    ;Set R1 to first address of
001204    001400                          ;data buffer.
001206    012706          MOV #SP, R6     ;Initialize stack pointer.
001210    001100
001212    012737          MOV #INT, RVEC  ;Set DZ11 vector address
001214    001304                          ;to start of receiver
001216    000300                          ;interrupt routine.
001220    005037          CLR (RVEC+2)    ;Set up processor status
001222    000302          ;word for DZ11 receiver
                                          ;interrupt.
001224    012737          MOV#20, DZCSR   ;Set bit 4 in the DZ11
001226    000020                          ;control and status
                                          register.
001230    160100
001232    032737    1$:   BIT #20 DZCSR   ;Test bit 4.
001234    000020
001236    160100
001240    001374          BNE 1$          ;if bit 4 is still set, the
                                          ;branch condition is true
                                          ;and the device function
                                          ;is still in progress.
001242    012737          MOV #PAR, DZLPR ;Load the parameters for
001244    011070                          ;line 0: 8 bit character;
001246    160102                          2 stop bits; 110 baud;
                                          ;no parity; receiver on.
001250    012737          MOV #1, DZTCR   ;Enable line 0
                                          transmitter.
001252    000001
001254    160104
```

Example 3 (Cont)

```
001256  012737          MOV #150, DZCSR   ;Turn scanner on, enable
001260  000150                            ;receiver interrupts, and
001262  160100                            ;loop lines back on
                                          themselves.
001264  005737  2$:     TST DZCSR         ;Test the transmitter
001266  160100                            ;ready flag.
001270  100375          BPL 2$            ;If branch condition is
                                          ;false, continue
                                          ;otherwise test again.
001272  110037          MOVB R0, DZTBUF   ;Load character to be
001274  160106                            ;transmitted.
001276  105200          INCB R0           ;Increment binary count.
001300  001371          BNE 2$            ;If branch condition is
                                          ;false, the binary count
                                          ;pattern is complete.
001302  000777          BR .              ;Wait for last character
                                          ;transmitted to be
                                          ;received.
```

Receiver Interrupt Service Routine

```
001304  013711          MOV DZRBUF, (R1)  ;Store in memory
001306  160102                            ;table.
001310  022721          CMP #100377, (R1)+ ;Check for last
001312  100377                            ;character.
001314  001401          BEQ .+2           ;Branch condition is
                                          ;true when last
                                          ;character is found.
001316  000002          RTI               ;Exit routine.
001320  012701          MOV #1400, R1     ;Initialize pointer
001322  001400                            ;to start of data
                                          ;in memory.
001324  105737  3$:     TSTB TPS          ;Test to see if
001326  177564                            ;console punch is ready.
001330  100375          BPL 3$            ;Wait, and test again.
                                          ;If condition is met,
001332  111137          MOVB (R1), TPB    ;transfer character
001334  177566                            ;to console punch.
001336  022721          CMP #100377, (R1)+ ;Check for last
001340  100377                            ;character.
001342  001370          BNE 3$            ;Not finished if
                                          ;condition is true.
001344  000000          HALT              ;finished.
```

RVEC = DZ11 Receiver Interrupt Vector Address
DZCSR = DZ11 Control and Status Word Address
DZLPR = DZ11 Line Parameter Register (Write Only) Address
DZTCR = DZ11 Transmit Control Register Address
DZTBUF = DZ11 Transmit Buffer Address
DZRBUF = DZ11 Receiver Buffer Address (Read Only Register)
TPS = Teletype Punch Status Register Address
TPB = Teletype Punch Data Register Address

Example 4 – Transmit and receive in Maintenance mode on a single line. The Switch register bits SWR00 – SWR07 holds the desired data pattern (character).

```
001000  012737          START:  MOV #LINE, DZTCR    ;Select the line for
001002  000002                                      ;transmitting on.
                                                    Choose one of eight.
001004  160104                                      ;Line #1 selected.
001006  012737                  MOV #PAR, DZLPR     ;Select desired line
001010  017471                                      ;parameters for
                                                    transmitting line
001012  160102                                      ;and turn on receiver for
                                                    that line.
                                                    ;8 level code, 2 stop bits,
                                                    ;and no parity selected.
                                                    ;19.2K baud selected
                                                    ;Note: 19.2K baud is
                                                    ;not used by the customer
                                                    ;but can be used for
                                                    ;diagnostic purposes to
                                                    ;speed up the
                                                    ;transmit-receive
                                                    ;loop to make
                                                    ;it easier to scope.)
001014  012737                  MOV #N, DZCSR      ;Start scanner and set
001016  000050                                      ;maintenance bit 3.
001020  160100
001022  005737          Test 1: TST, DZCSR          ;Test for bit 15
001024  160100                                      ;(transmitter ready).
001026  100375                  BPL Test 2         ;If the branch condition
                                                    ;is false, the transmitter is
                                                    ;ready; if true, go back
                                                    :and test again.
001030  113737                  MOVB SWR, DZTBUFF  ;Load the transmit
001032  177570                                      ;character from the
001034  160106                                      ;Switch register.
001036  000240                  NOP                ;No operation. This
                                                    ;location can be changed
                                                    ;to a branch instruction
                                                    ;if only test 1 is
                                                    ;desired (replace 000240
                                                    ;with 000771).
001040  012701                  MOV # DEL, R1       ;Delay equals a
        177670                                      ;constant that will
                                                    ;allow enough time for
                                                    ;the receiver done
                                                    ;flag to set before
                                                    ;recycling the test. The
                                                    ;value will change with
                                                    ;baud rate and
                                                    ;processor. The
                                                    ;constant given is
                                                    ;good for 19.2K baud
                                                    ;on a PDP-11/05.
```

Example 4 (Cont)

```
001042  105737          Test 2:  TSTB DZCSR      ;Test bit 2 - receiver
001044  160100                                   ;done flag.
001046  100402                   BMI 1$         ;When the branch
                                                ;condition is true,
                                                ;the receiver done
                                                ;flag is set.
001050  005201                   INC R1         ;Increment delay.
001052  001373                   BNE TEST 2     ;If the branch
                                                ;condition is true, the
                                                ;delay is not finished.
001054  013700          1$:      MOV DZRBUF, R0 ;Read the DZ11
001056  160102                                   ;receiver buffer to
                                                ;register 0.
001060  000760                   BR TEST 1      ;Loop back and
                                                ;test again.
```

Example 5 - Single line using silo alarm in Maintenance mode.

```
001200  012706                   MOV #1100, R6  ;Initialize stack pointer.
001202  001100
001204  012737                   MOV #3$, TVEC  ;Initialize transmitter
001206  001274                                  ;vector address.
001210  000304
001212  005037                   CLR TVEC+2     ;Initialize transmitter
001214  000306                                  ;vector processor status
                                                word.
001216  012700                   MOV #DBUF, R0  ;Set first address of input
001220  001304                                  ;data table into R0.
001222  012737                   MOV #1, DZTCR  ;Enable line 0
                                                transmitter.
001224  000001
001226  160104
001230  012737                   MOV #17470, DZLPR ;Set up line parameters
001232  017470                                  ;and turn on the receiver
001234  160102                                  ;clock for line 0.
001236  012737                   MOV #50050, DZCSR ;Enable transmitter
001240  050050                                  ;interrupt and silo alarm.
001242  160100                                  ;Turn on scanner and
                                                ;Maintenance mode.
001244  032737          1$:      BIT #20000, DZCSR ;Test for silo alarm.
001246  020000
001250  160100
001252  001774                   BEQ 1$         ;Loop until silo alarm
                                                ;flag sets.
001254  013720          2$:      MOV DZRBUF, (R0)+ ;Read DZ11 silo receiver
001256  160102                                  ;buffer output.
001260  000240                   NOP            ;Delay to allow next
001262  000240                   NOP            ;word in silo to filter
                                                ;down to the
                                                ;silo output.
```

Example 5 (Cont)

```
001264   100773          BMI 2$          ;Data valid set says that
                                         ;word is good; go back
                                         ;for more.
001266   012700          MOV #DBUF, R0   ;Silo has been emptied.
001270   001304                          ;Reinitialize data table
                                         ;address pointer.
001272   000764          BR 1$           ;Do it again.
```

Transmitter Interrupt Service Routine

```
001274   112737    3$:   MOVB DAT, DZTBUF  ;Transmit
001276   000252                            ;character 252
001300   160106
001302   000002          RTI
```

Data Table

```
1304     100252                    ;Word #1
1306     100252
   •        •                        •
   •        •                        •
   •        •                        •
   •        •                        •
   •        •                        •
   •        •                        •
1340     100252                    ;Word #16
1342     000252                    ;Data valid not set
                                   ;character is invalid
```

NOTE: It is possible to get more than 16 words because they are being put into the silo simultaneously with the reading of the silo.

CHAPTER 4
DETAILED DESCRIPTION

4.1 INTRODUCTION

The detailed descriptions of DZ11 circuit operation are contained in this chapter. Signal flow, generation, and interaction with external devices are discussed to facilitate understanding of DZ11 operation as a component of a PDP-11 system. The text is supplemented by references to DEC engineering drawings and specifications, simplified diagrams, and material in the Appendices of this manual.

The DZ11 module performs three basic data functions: control, storage, and transformation.

Data travels in two directions through the module circuitry: from the PDP-11 Unibus to the selected terminal or modem line, and in the opposite direction. When data flows from the Unibus, through the module, to the selected output line, the DZ11 is assumed to be in the transmit mode. Flow from the external device, through the module, to the Unibus is considered the receive mode. The subsequent paragraphs discuss data flow within the DZ11 system during the transmit and receive modes.

4.1.1 Modem-To-Unibus Data Flow (Receive)

When receiving data from a terminal or modem, the DZ11 module interprets a serial data stream, and performs a serial-to-parallel conversion before transferring the data to the Unibus. Refer to Figure 4-1. Each terminal connects to one serial data line, REC (7:00), through the Distribution panel to connector J1. The EIA receivers match the incoming signal levels to that of the DZ11, and feed the data to the receiver control logic. At this point, the data passes through a maintenance control circuit which allows the DZ11 to "receive" its own transmissions during maintenance tests. From the receiver control logic, the data is fed into the appropriate UART for the serial-to-parallel conversion. A parallel data format, corresponding to its serial input, is moved to a FIFO storage "tank," called a silo, which has a 64-character capacity. When requested by the processor, each character is read from the "bottom" of the silo (a register called RBUF), causing the remaining characters to shift one position downward, and the read character is multiplexed through the bus drivers to the Unibus. Modem Control signals for each line are routed directly to the output multiplexer.

4.1.2 Unibus-To-Modem Data Flow (Transmit)

During a transmit cycle, parallel data is brought in from the Unibus for transmission to one of the eight terminals (or modems). Refer to Figure 4-2. The 16 bus lines BD(15:00) are fed through data transceivers and distributed to the device registers and UARTs. When the DZ11 is ready to transmit, a character is read from the TBUF and loaded into the appropriate UART for the line. The UART then performs the parallel-to-serial data conversion, adds the desired character control bits, and sends the data to the selected transmission line, through an EIA line driver, and subsequently to the modem or terminal connected to that line. The Break register connects directly to the EIA drivers, setting the break by forcing the drivers into a continuous "space" condition. The DTR modem or terminal control lines also go directly to the EIA drivers.

4.2 UNIBUS INTERFACE

The DZ11 Unibus Interface provides access for the DZ11 system to the PDP-11 Unibus. All signals that pass between the Unibus and the DZ11 are routed through the Interface.

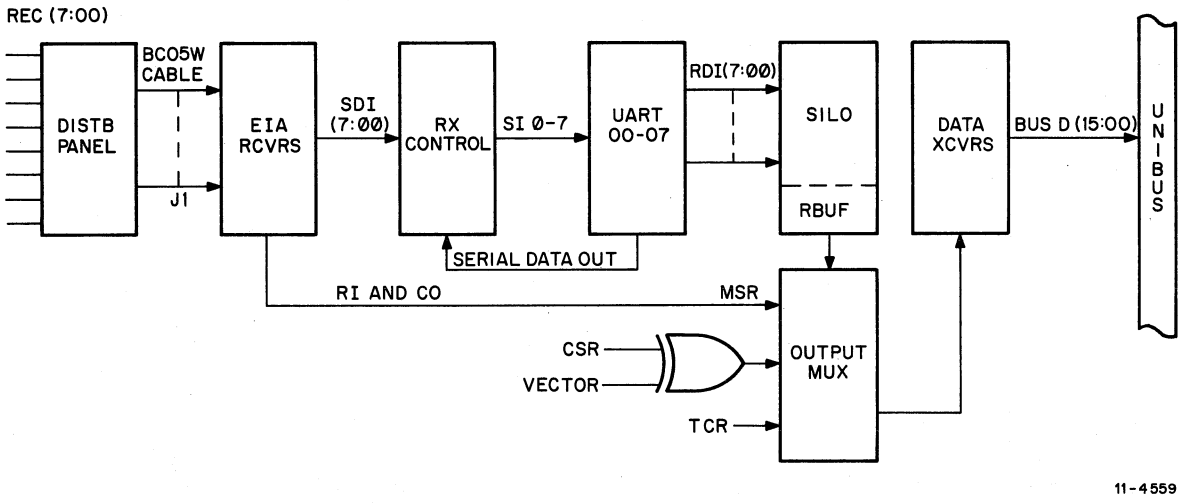


Figure 4-1 Modem-to-Unibus Data Flow (Receive)

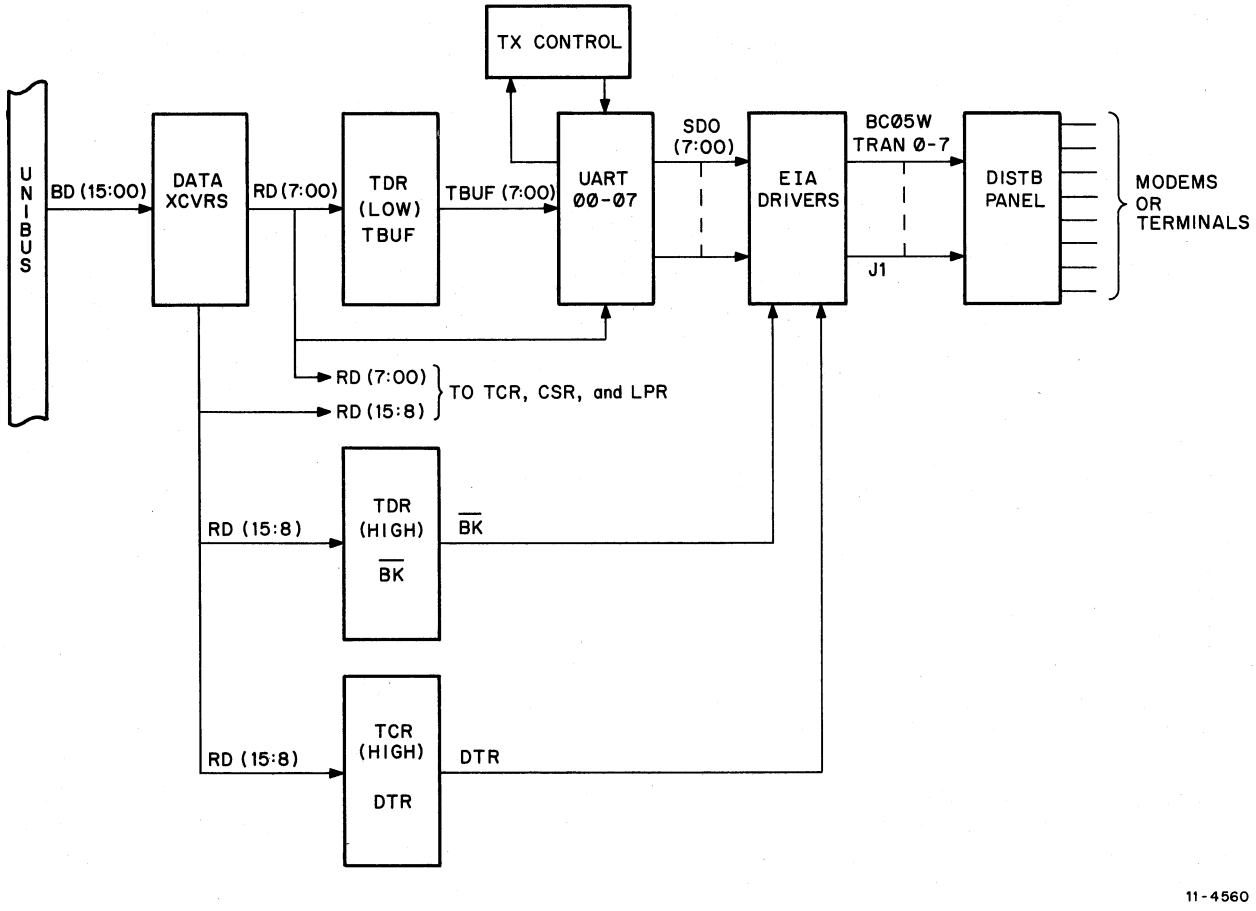


Figure 4-2 Unibus-to-Modem Data Flow (Transmit)

The Interface logic can be divided into three major areas: Address Selection, Data Transceiving and Multiplexing, and Interrupt Control. Each of these components is shown in Figure 4-3. The Interface performs several functions for the remainder of the DZ11 system. In general, these functions are:

1. Selection and recognition of the DZ11 addresses and device registers.
2. Determination of the DZ11 mode of operation with the PDP-11 processor (DATI or DATO, word or byte).
3. Handling of data to and from the device registers and other DZ11 control elements.
4. Control interrupts between the DZ11 and the PDP-11 processor.
5. Transmission of responses to master signals from the PDP-11 processor during interlocked communications ("master and slave").
6. Transmission of DZ11 and modem status signals to the PDP-11 processor.

4.2.1 Address Selection

The address selection logic determines the DZ11 device address and recognizes that address when it appears on the Unibus. A recognized address indicates that the DZ11 has been selected by the processor or another bus "master".

The desired address is selected by switches that correspond to Unibus address bits 03 through 12 (Figure 4-4). Bits 13 through 17 are always decoded as binary one's (Figure 4-5). Bits 00 through 02 determine which device register is to be selected. This bit scheme allows device addresses from $16000X_8$ to $17777X_8$. However, the DZ11 does not use the entire range, but makes use of the floating address space 160010_8 to 163770_8. A detailed description of DZ11 address assignments is presented in Chapter 3.

4.2.1.1 Device Address Selection (Figure 4-6) – Three 6-bit comparators (DM8136) are in parallel with each other and provide a common output that is fed to a NAND gate (E73). These comparators (E71, E80, and E61) receive inputs from the Unibus. E71 and E61 receive Unibus inputs at B1–B6 and E80 receives Unibus inputs at B2–B5. These sixteen inputs are compared with their associated logic levels at the D inputs. The D inputs at comparators E71 and E80 are selected by ten switches at E81. An open switch produces a high at the corresponding D input and a closed switch produces a low. Each switch position is selected so that the comparators will accept only the appropriate address from the Unibus. The D1–D6 inputs at E61 are kept low by being hard-wired to ground. If the Unibus address bits match the preset address bits at E71 and E80, and the six Unibus inputs at E61 are low, with an asserted low at B2 (MYSN) from the Unibus, then a high output is generated at OUT 9 for each comparator. When all three comparator outputs are high, the NAND gate (E73) is enabled.

4.2.1.2 Register and Mode Selection (Figure 4-6) – Unibus address lines A(2:00) and control lines C0 and C1 are used to select the DZ11 register and establish the direction of the data transfer. Two decoders (74LS138) at E74 and E75 use the signals from the Unibus to generate the register select signals. E74 produces a load pulse (DATO bus cycle) and a read pulse (DATI bus cycle). The load pulse is routed to each register, and the read pulse is sent to the receive scanner control. E75 generates two pulses for each register, excluding the LPR. The signals from E74 are used only during a word operation. For byte operations, one pulse from E75 is used to load the low byte of a word and the other pulse loads the high byte. When a byte operation is performed, only one of the signals from E75 is used as in a DATOB cycle.

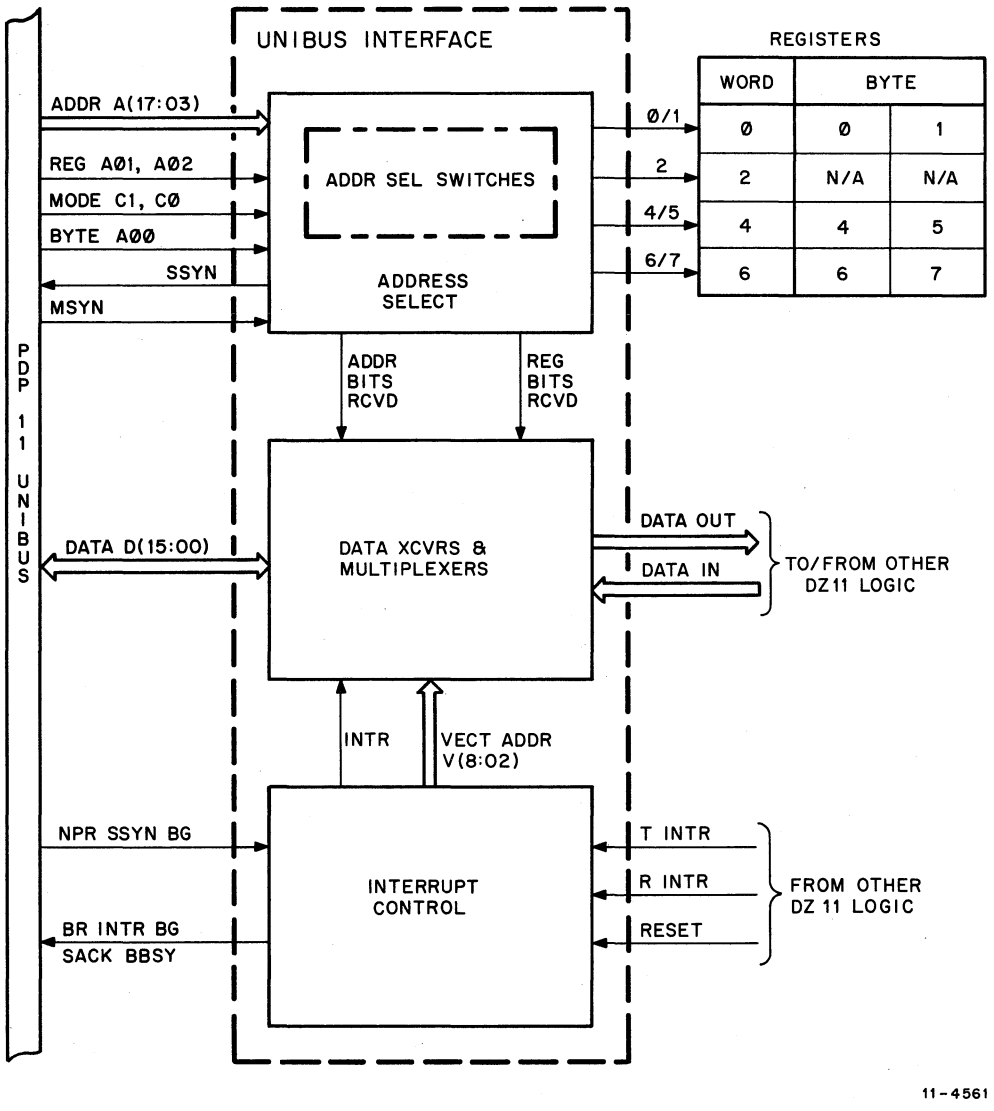
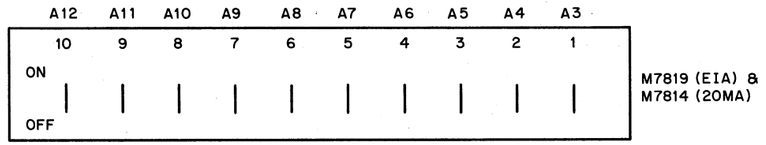


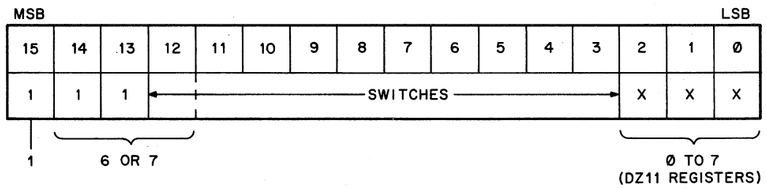
Figure 4-3 Unibus Interface Block Diagram



NOTE:
Address 160000 – A12 through A3, OFF
160010 – A12 through A4, OFF; A3, ON
177770 – A12 through A3, ON

11-4562

Figure 4-4 Address Selection Switches



11-4563

Figure 4-5 Address Word Format

160140

12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 1 1 0 0 0 0 0

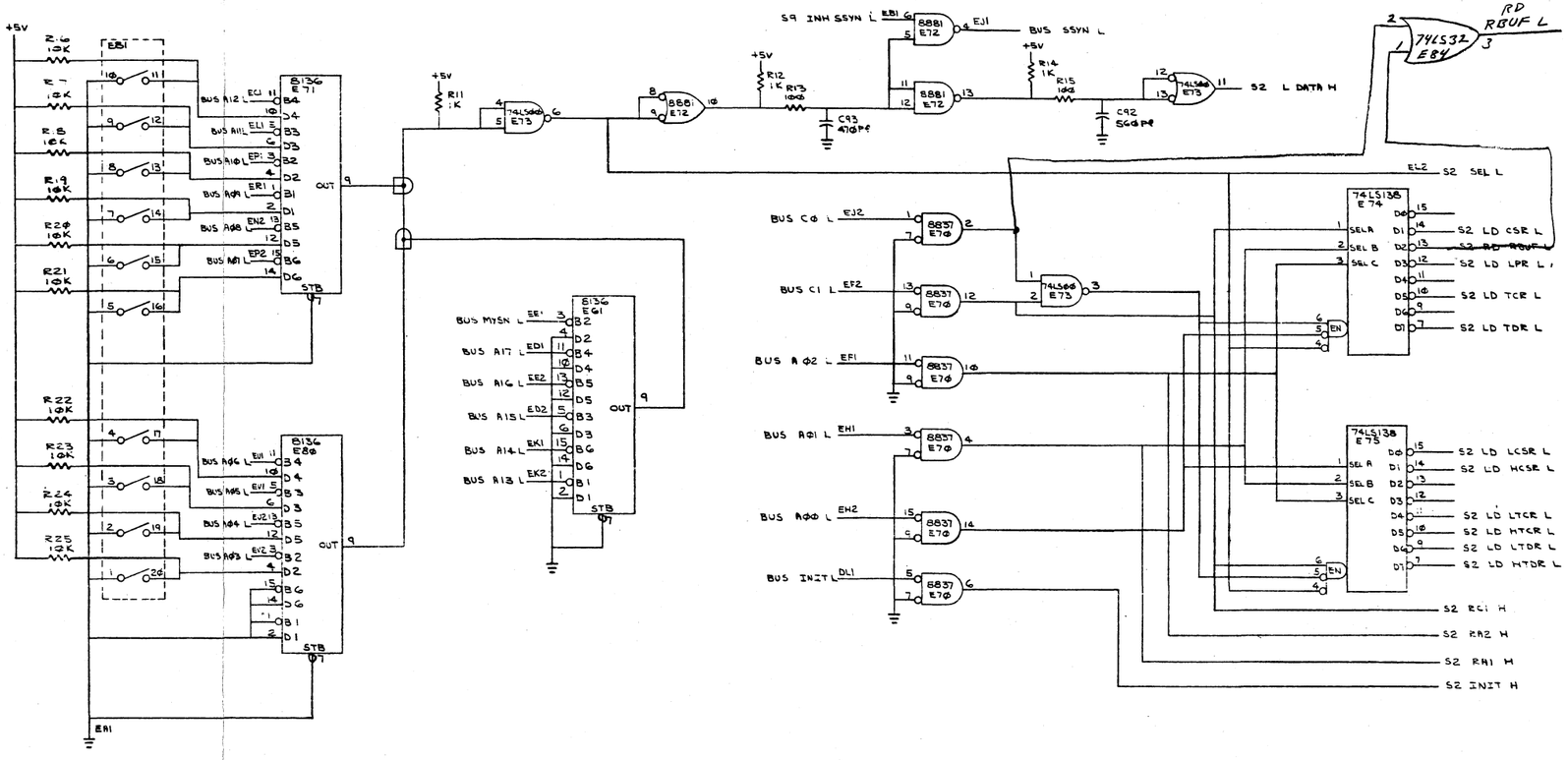


Figure 4-6 Address Selection Logic

Received address lines RA1 and RA2, and control line RC1 are sent to the output data multiplexer (refer to Paragraph 4.2.3) to select the register to be loaded onto the Unibus during a read (DATI) operation. Receipt of MSYN and bits A(17:03) from the Unibus and subsequent assertion of SEL causes generation of SSYN and LDATA. SSYN is the DZ11 response to MSYN, and occurs 100 nanoseconds after receipt of MSYN. The delayed response is produced by the network R12, R13, and C93. However, when the LPR is accessed, a 500-nanosecond INH SSYN pulse on one input of E72 is used to prevent SSYN from being put on the Unibus. The LDATA pulse (delayed an additional 100 nanoseconds) is used to generate a strobe signal for the LPR. Figure 4-7 shows the timing for loading the LPR. The delays and inhibit signals allow proper data "setup" time before strobing the line parameters. The BUS INIT signal is also received (at E70) and used to clear the DTR register and generate a device reset pulse.

4.2.2 Interrupt Control

The interrupt control logic handles the processor – Unibus – DZ11 dialog to permit processor interrupts. The logic generates vector addresses for processor location of instructions, and receives interrupt commands from the CSR. The DZ11 operates at priority levels 5A (receiver) and 5B (transmitter). When two DZ11 modules are used, the first module (slot 1) has priority over the second (slot 2). The priority insert establishes the DZ11 priority level by directing the Unibus request and grant signals from the appropriate Unibus lines to the DZ11. A series of switches permit alteration of the vector address to suit programming requirements. Refer to Chapter 3 of this manual for vector selection and assignment.

4.2.2.1 Receiver Interrupt (Figure 4-8) – The receiver interrupt signals the processor when the DZ11 receives a character from the terminal, and stores the character in the RBUF (silo buffer). After processing by the UART, the character is loaded into the silo, and CSR bit 07 (RDONE) is set; RDONE causes generation of the RINT signal. RINT is fed to the 8647 receiver interrupt logic and the BR A signal is transmitted to the processor via the Unibus at priority level 5A. When the processor status goes below level 5, a BG5 signal is routed through the priority insert (on the DZ11 module) to the GRANT IN input of the 8647, causing generation of MASTER, BUS SACK, and BUS BBSY. The MASTER signal is inverted and gated to create the BUS INTR for transmission to the Unibus and the INTR created for use in other DZ11 logic. The vector address is strobed to the Unibus from the output data multiplexer by the INTR signal.

4.2.2.2 Transmitter Interrupt(Figure 4-8)– The transmitter interrupt occurs when the DZ11 is engaged in character transmission to the terminal, and the processor must be interrupted to request additional data for transmission. The interrupt sequence begins with assertion of TRDY and TIE signals, which generate the TINT pulse. The TINT signal begins the procesor-DZ11 interrupt dialog via the Unibus. The 8647 transmitter interrupt priority is less than that of the receiver, therefore, bus grants are received only when a receiver interrupt is not in process. The transmitter interrupt logic causes generation of the same signals as the receiver logic, including strobing the vector address; however, the transmitter vector is located two words after the receiver vector. For example, a receiver vector of 300 automatically places the transmitter vector at 304.

4.2.3 Data Transceivers and Output Multiplexers (Figure 4-9)

The data transceivers and output multiplexers control data flow to and from the Unibus. The 4:1 multiplexers select the contents of the CSR, RBUF, TCR, and MSR for transmission to the Unibus. Figure 4-10 details the correlation between the Unibus lines and the DZ11 register bits. The vector bits are also transferred to the Unibus by the same logic. The INTR pulse determines whether the vector or the CSR bits are to be transferred. The reset logic is triggered by bit 04 of the CSR (DEVICE CLR), or by the received BUS INIT signal. The reset pulses are 15 microseconds in duration. RA1 and RA2 drive the multiplexer's select lines and the SEL signal is ANDed with RC1 (DATI bus cycle) to gate the selected register to the Unibus transceivers.

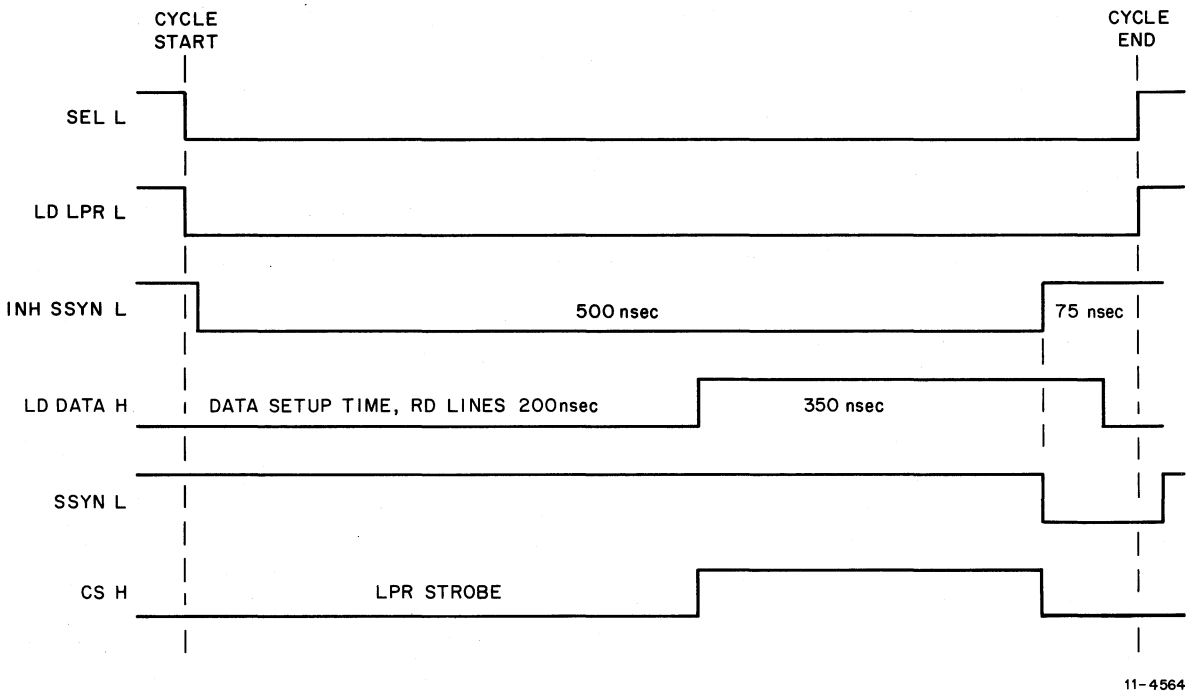


Figure 4-7 Line Parameter Loading

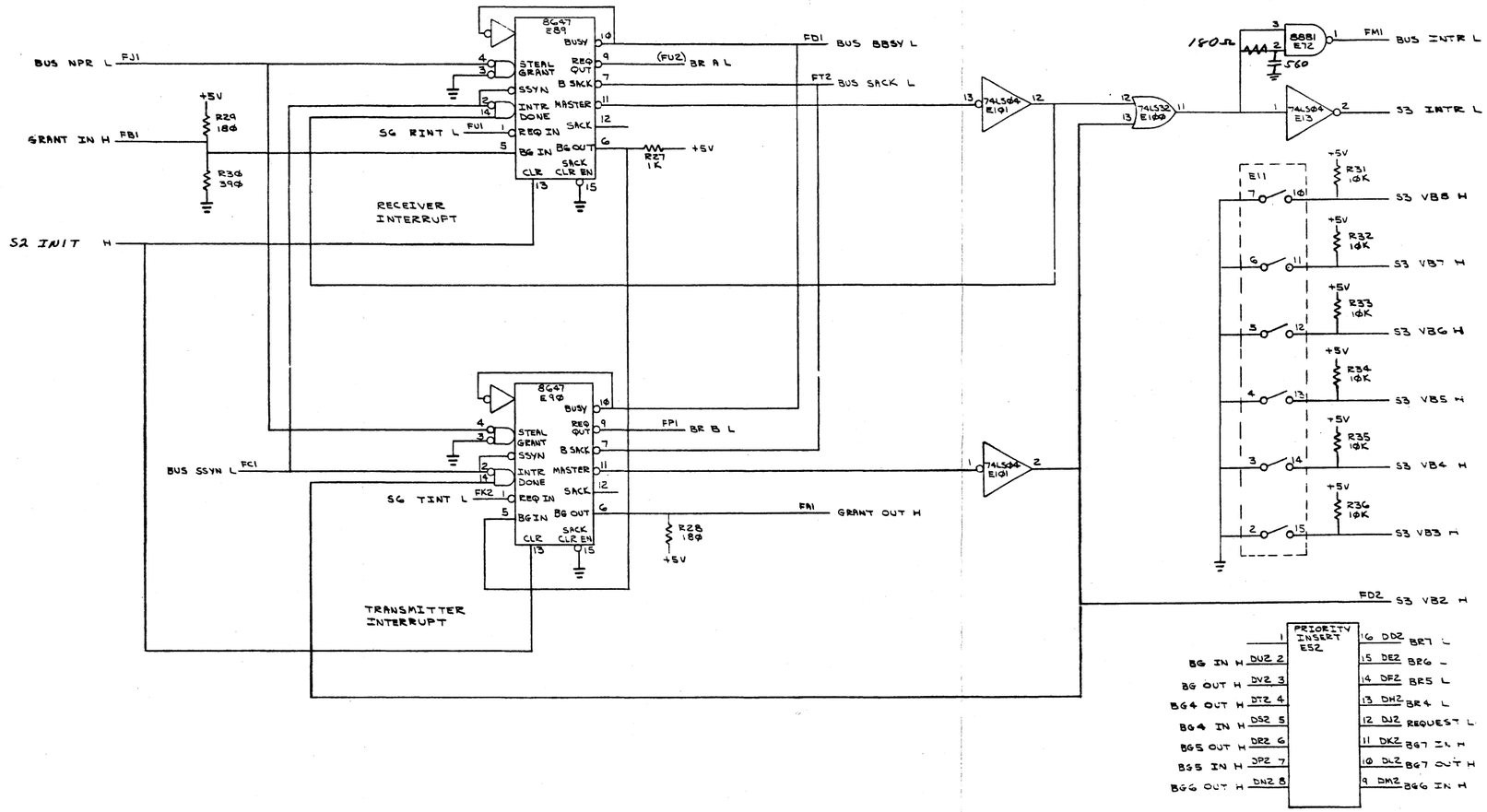


Figure 4-8 Interrupt Control Logic

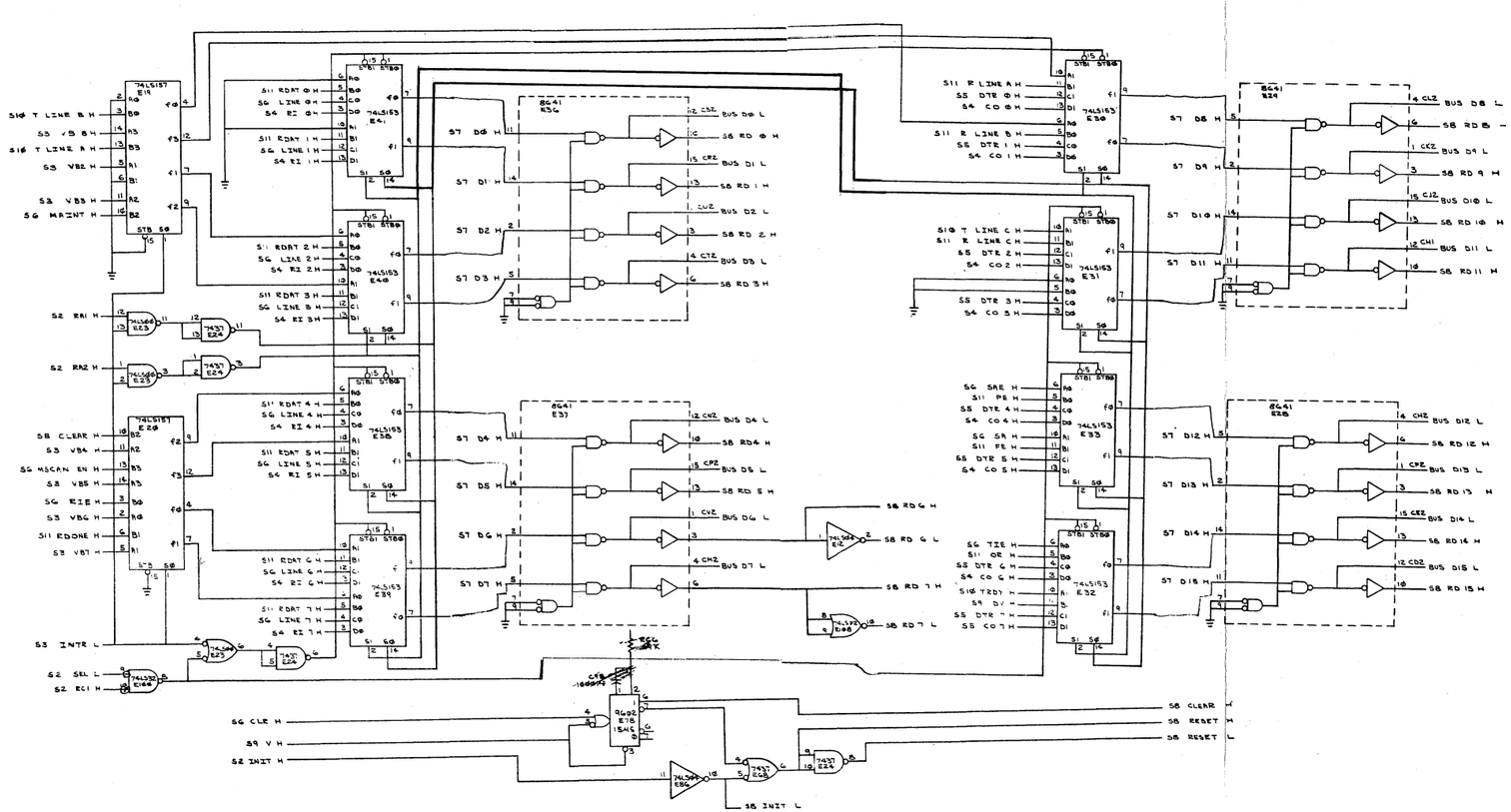


Figure 4-9 Unibus Data Flow

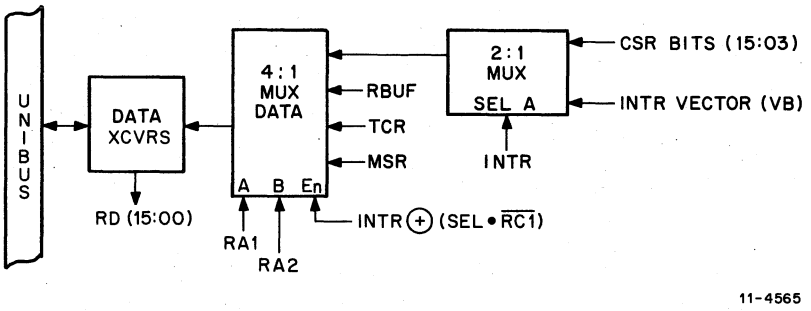


Figure 4-10 Output Data Multiplex Bit Correlation

4.3 SCANNER

The scanner generates timing signals for transmission and reception of data between the Unibus and the UARTs. The scanner timing signals originate at the 5.068-MHz clock, a continuously running signal that is inverted twice to yield MASTER CLK L and MASTER CLK H pulses. These pulses control the baud rate logic, and a divide-by-five counter uses the pulses to generate the CLK H pulses that drive the phase generator logic. Line-sampling occurs during a 4.0-microsecond period, which is divided into four equal phases. Phase 1 triggers a line counter, which produces the SCAN A, B, and C line-select signals. Each line is sampled sequentially. Refer to Figure 4-11.

4.3.1 Receive Control

The scanner times the operation of loading a character into the silo and reading the RBUF. Refer to the timing diagram in Figure 4-12. At the trailing edge of phase 4 (the leading edge of phase 1), the scanner is incremented to the next line for sampling. During phase 1, the Data Available (DA) flag is sampled, and if set and the silo is not full, a Shift-In (SHI) pulse (leading edge of phase 2) moves a character from the UART for that line to the silo. At the trailing edge of phase 2 (start of phase 3), the Reset Data Available (RDA) pulse resets the DA flag if the SHI occurred during phase 2. Phase 4 terminates the RDA pulse and the scanner increments to the next line at the leading edge of the next phase 1. To complete the scanner operation, the Unibus initiates a character shift out of the silo by reading the RBUF. Refer to Figure 4-13.

4.3.2 Transmit Control

The transmission of a character from the DZ11 is primarily controlled by a network of logic circuits called the Transmit Control section (Figure 4-14). This network generates the timing signals for line selection, UART control, and data transfer to the modem or terminal connected to the DZ11. When the TBMT signal goes high, it indicates that the transmitter buffer is empty for the UART being sampled. The inverted signal is fed to a 74LS151 chip at E91 and strobes the appropriate line enable (LINE 0–7) signal to the A0 input of E92. The SCAN A, B, C signals feed E91 and E102 (a 74LS157) to provide the proper selected line. As in the receiver control, the transmitter operates in four phases. The phase 1 pulse is delayed 30 nanoseconds before being routed to the 74LS157 at E102 to allow propagation time through the circuit and avoid race conditions; as phase 1 ends and phase 2 begins, the delay ensures that the 8-bit addressable latch at E103 is latched before data is changed in E102. The latches at E103 hold their conditions when pins 14 and 15 are high; latch selection is determined by line selection outputs from E102 (Figure 4-15). The 8-bit addressable latch outputs to two 74LS175 chips at E93 and E104, which are controlled by MSCAN EN H and the output of the AND gate at E107. The priority encoder chip at E82 (a 9318) receives the line select data from E93 and E104, and produces the T LINE A, B, C signals which are sent to the output data multiplexers. The signals GS from the 9318 Priority Encoder disables the 74LS08 AND E107 gate feeding the clock inputs of E93 and E104. This prevents the inputs to the 9318 from changing until the line has been serviced or disabled by the programmer.

Character transmission is allowed for the first 300 nanoseconds of each phase during CLK H pulses only, except in phase 1, when transmission is inhibited to allow sampling of the line enable bits. The GS output from pin 14 of the priority encoder (9318 at E82) and the output from the 74LS74 at E109 are used to generate the TRDY H pulse, signifying that a line is available for transmission and a character is loaded in the TBUF.

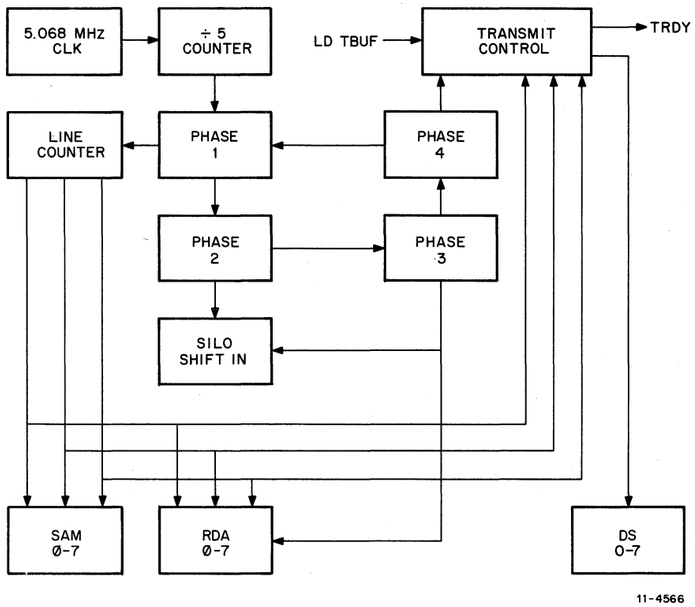


Figure 4-11 Scanner Block Diagram

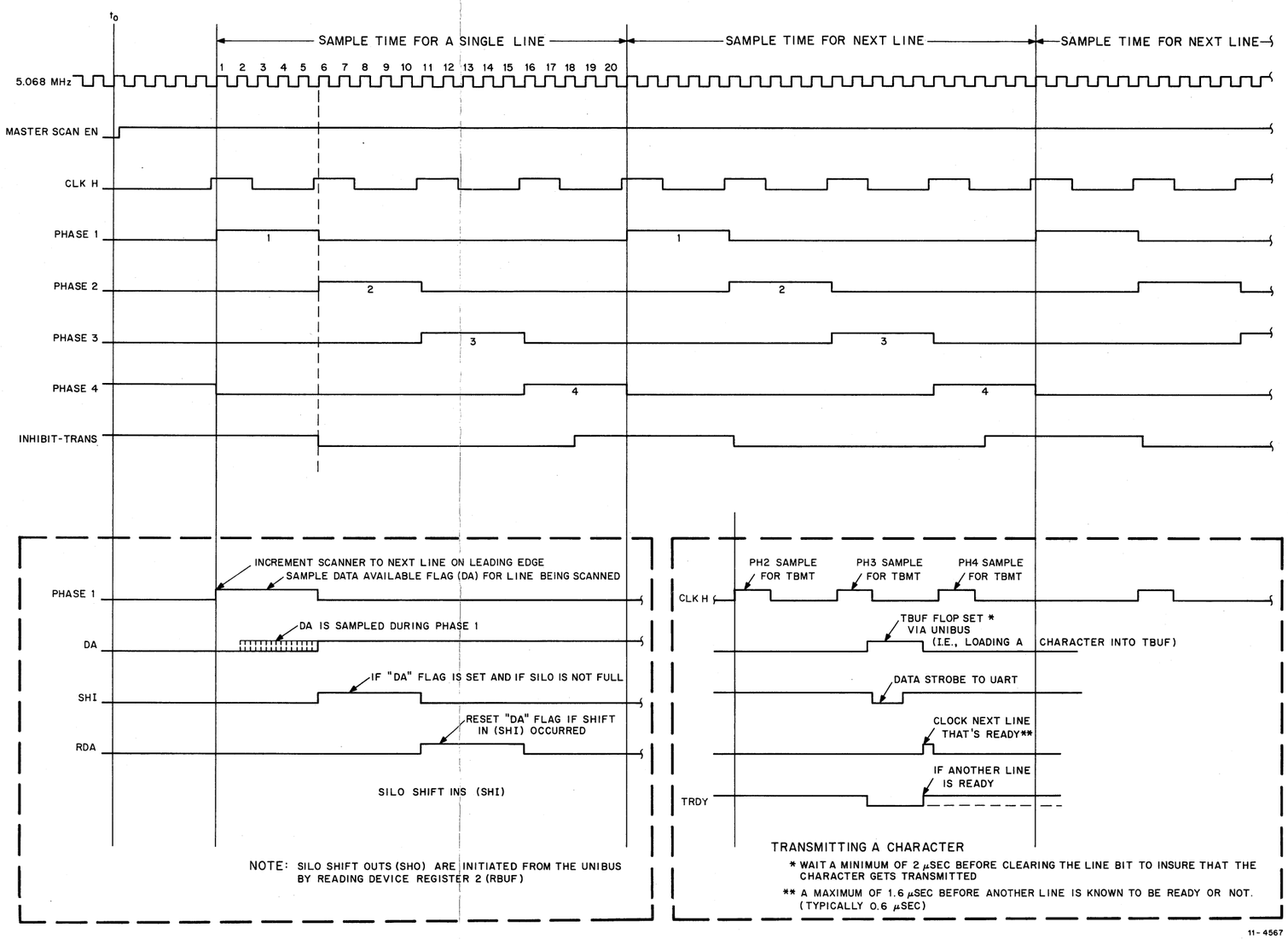


Figure 4-12 DZ11-A Scanner Timing

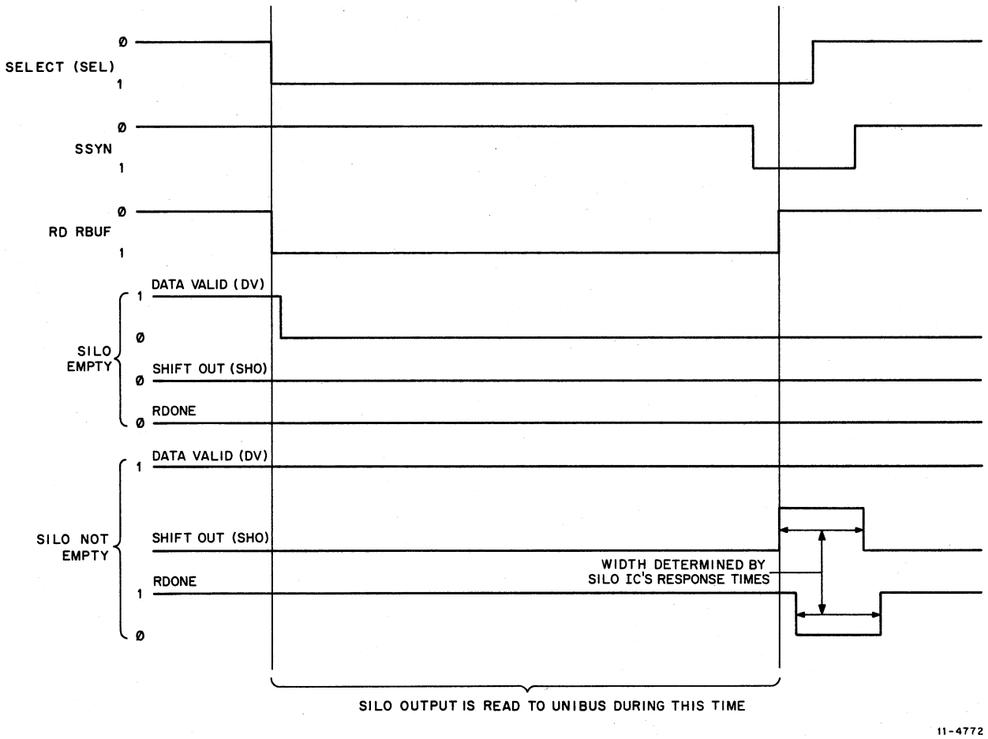


Figure 4-13 Silo Character Shift Out Timing Diagram

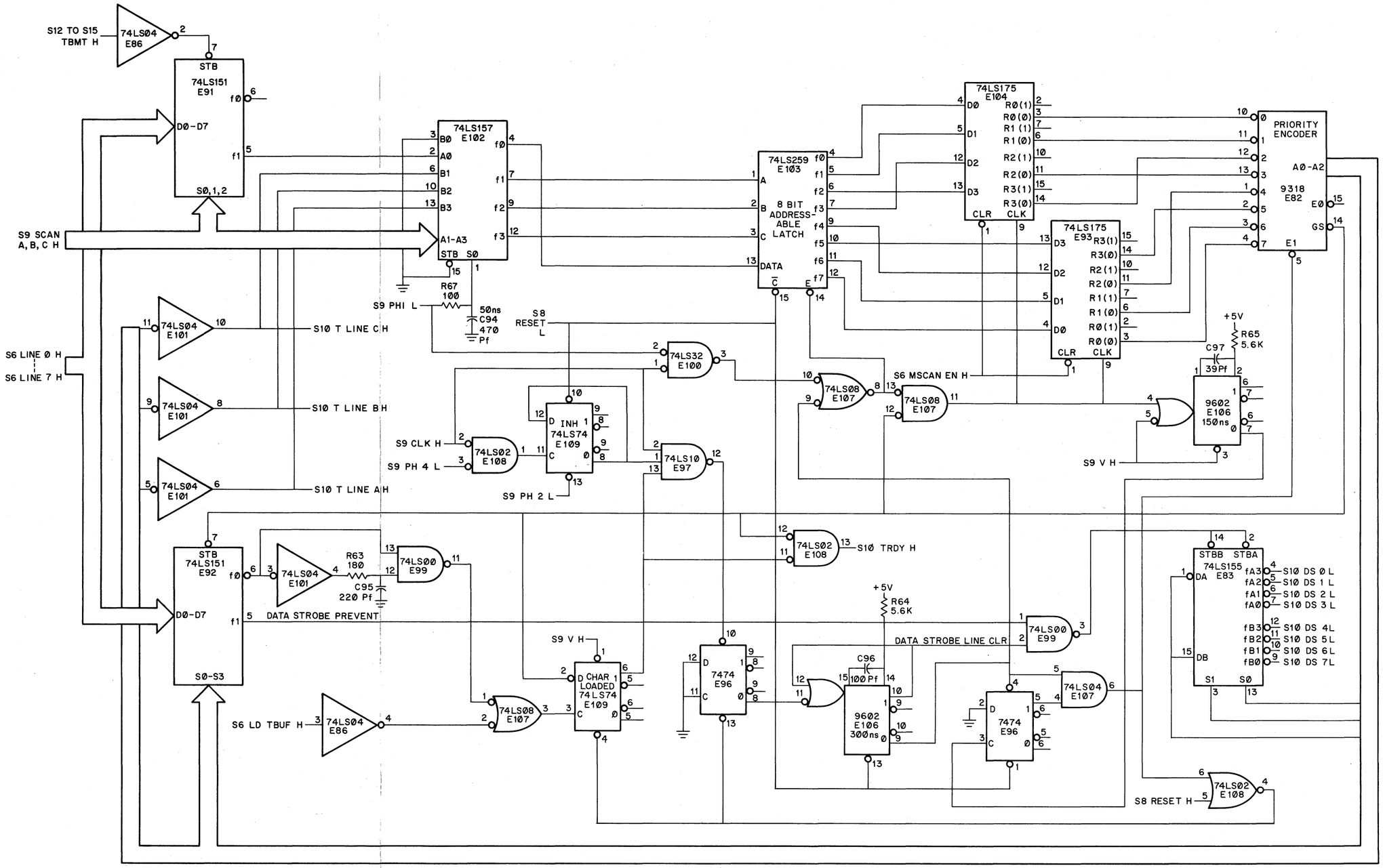


Figure 4-14 Transmit Control Logic

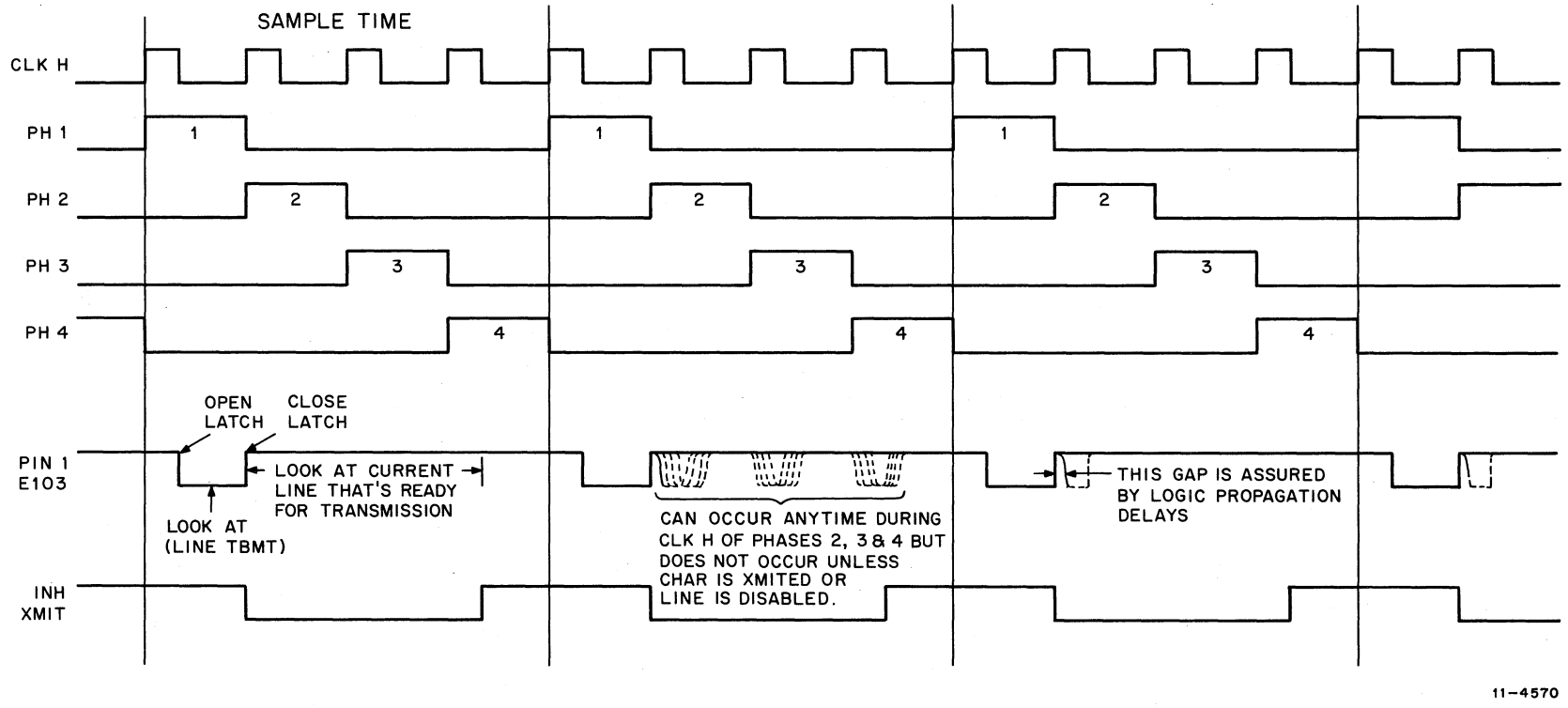


Figure 4-15 Transmit Control Timing

Transmission is initiated by loading the Transmit Buffer register (TBUF). This causes flip-flop E109, pin 6 to set; and Transmit Ready (TRDY) drops and cannot be asserted again until this flip-flop is cleared. Pin 13 of E97 is now true and if the scanner is not in phase 1 (pin 1 input) and CLK H is true (pin 2 input) then pin 12 of E97 will cause flip-flop E96, pin 8 to direct set. The output triggers E106, pin 11 (9602 one-shot, 300 nsec) and does the following:

1. The pulse is gated to the Strobe Input of E83 to generate a Data Strobe (DS) pulse to the UART. DS loads the contents of the TBUF into the UART and transmission starts. The correct DS pulse is selected by input pins 1, 15, 3, and 13 of E83 which are connected to the TLINE bit outputs of the priority encoder (E82).

2. The pulse is gated to pin 14 of E103 and opens the latch selected by input pins 1, 2, and 3. During phase 2, 3, and 4, these inputs are the TLINE bits from the priority encoder and the data input, pin 13, is at ground level; so that the latch for this line is cleared.

3. The pulse causes the priority encoder to turn off after it times out. This makes pin 14 of E82 (priority encoder) go high and causes a clock output from pin 11, E107. This output updates the 8-bit register from the E103 addressable latch outputs and presents a new set of inputs to E82 (priority encoder). Pin 11 of E107 also triggers a 150 nsec one-shot which allows for propagation delay and data settling time at the priority encoder inputs (E82). When this delay times out, flip-flop E96, pin 5 is cleared and E107, pin 4 is disabled. The output of this gate goes low and turns the priority encoder back on.

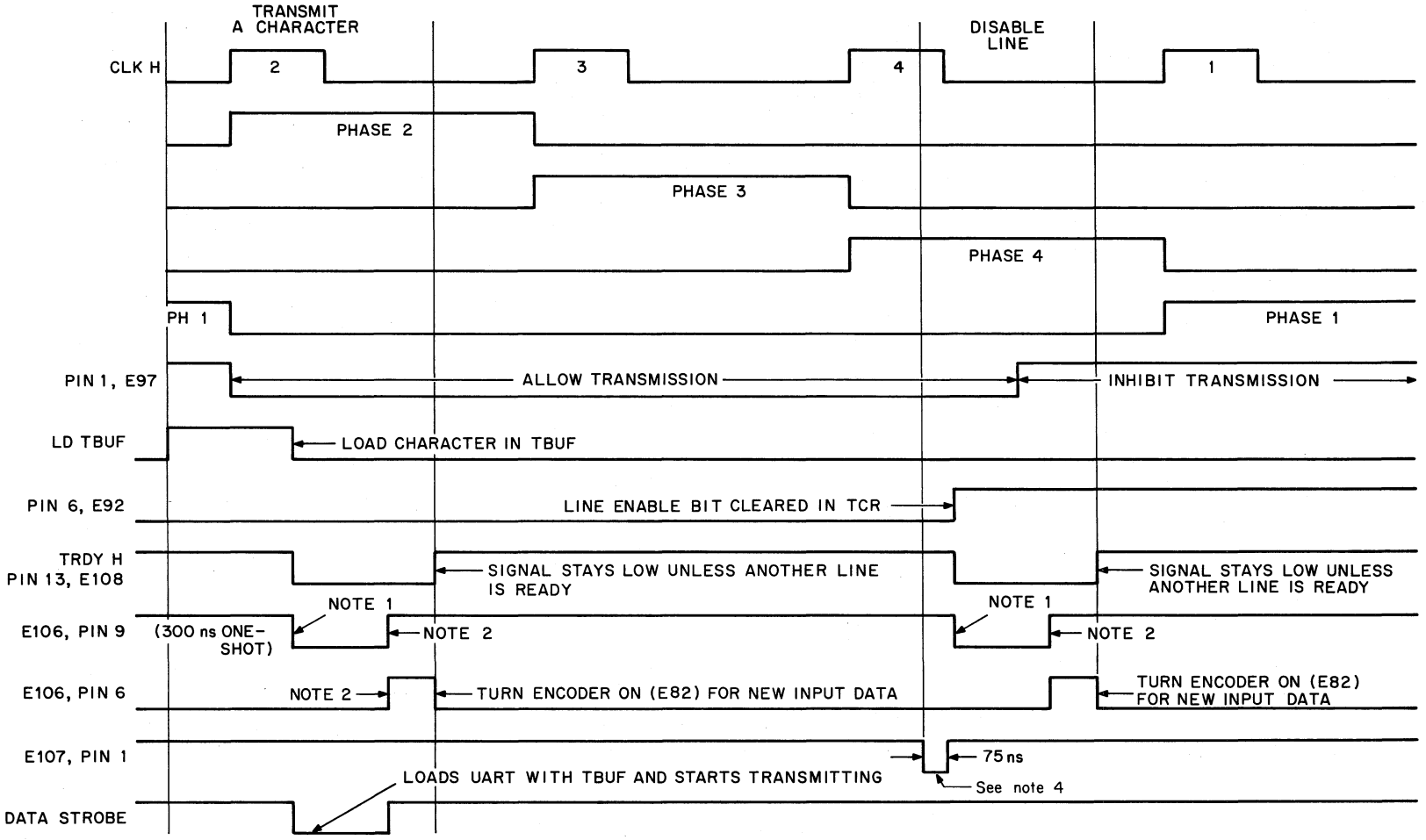
4. The pulse, also goes to flip-flops E109 and E96 to clear for the next transmission. If another line is ready to transmit, pin 14, E82 (priority encoder) will go low and the TRDY signal will be reasserted. The TLINEs will contain the value of the next line ready for transmission.

If the line enable bit is turned off instead of loading the TBUF, then pin 6, E92 will go high. This will produce a pulse on E99, pin 11 and set E109, pin 6. This will trigger E106 (9602 one-shot) and generate the same 300 nsec pulse that occurred when transmitting by loading the TBUF. However, this time there will be no DS pulse to start the UART. This is because E92, pin 5 is low and disables gate E99, pin 1. Figure 4-16 shows the timing for both a character transfer and a line disabling situation.

E82 is a 9318 priority encoder. Its inputs are labeled 0 to 7. Each ascending numbered input has priority over the input with a lower number, i.e., input 7 has priority over input 6; input 6 has priority over input 5; . . . . . and input 1 has priority over input 0. The output – A0, A1 and A2 – is a BCD number representing the highest priority input that is true. The output labeled GS indicates that one or more of the inputs are true. A truth table for the IC can be found in Appendix A.

4.3.3 Silo and UART Clocks

The receiver silo consists of four 3341 integrated circuits configured to form a 16-bit × 64-word register. As serial data comes into the DZ11, the UART transforms each character to a parallel format, and loads the silo with the character, the line number on which the character was received, and the character overrun and error bits. The character is fed into the silo on the RDI(7:00) lines from the UART. A SHI pulse enables the silo to store the character whenever the Input Ready (IR) signal is available from the silo and the DA flag is set. The IR and DA signals allow generation of the SHI pulse in phase 2. Output from the silo is the RBUF, and is enabled by a Shift Out (SHO) command to the silo. The SHO signal is generated if the RDONE signal is true, signifying an output ready condition, and if the RBUF is being read to the Unibus. As a character is read from the RBUF, the remaining characters in the silo shift down one position, and the RBUF is reloaded. The character from the RBUF is sent to the output data multiplexers to be transferred to the Unibus. The UART timing for the reception and transmission of data is supplied by transmitter and receiver clocks (XCLK) and RCLK) for each UART. The clock frequencies are determined by RD(11:08) which are used to drive four 5016 integrated circuits. The receiver clock is the sum of the transmitter clocks for each corresponding line and the bit conditions of RD(2:00 line number) and RD12 (receiver on). The transmitter and receiver for each line must operate at the same baud rate.



NOTES:

1. The latch (E103) is opened and the output for the transmitting line is cleared.
2. The latch is closed and the priority encoder (E82) is turned off: new inputs for the encoder are clocked into E93 and E104 .
3. All logic for this diagram is shown in figure 4-14
4. Sets E109-6 to cause a transmit sequence without issuing a data strobe.

11-4571

Figure 4-16 Character Transfer and Line Disable Timing

4.4 REGISTERS

The DZ11 uses four Device Registers in a manner to yield six uniquely accessible registers, each having a 16-bit word capacity. The six discrete registers temporarily store input/output data, establish DZ11 operating status, and monitor control signal conditioning. Depending on the function of the register, some are accessible in bytes or words; others are restricted to word-only operations. Since registers can be read or written, the selection of either a read or write operation allows two of the device Registers to function as four independent registers.

The subsequent paragraphs describe the operation of each DZ11 register. Refer to Chapter 3 of this manual for additional information regarding register bit assignments, bit functions, and programming techniques.

4.4.1 Control and Status Register (CSR)

The Control and Status Register (CSR) comprises two 74LS175 chips at locations E26 and E27 (Figure 4-17). Additional gates are used to control the register and generate signals that are CSR bits but are not stored in the 74LS175 chips. The Unibus lines, after routing through the DZ11 bus transceivers, direct the operation of the DZ11 in accord with the PDP-11 system requirements. Bits RD(3:06), RD12, and RD14 are stored in the CSR chips since these bits are read or write. The CSR is controlled by LD HCSR, LD LCSR, and LD CSR signals from the address selection logic. These signals are gated to the CSR chips through NOR logic to yield selection of the upper (HCSR) or lower (LCSR) portions of the register. The RINT and TINT signals are produced by the outputs of the CSR and gates that receive other signals required to generate receiver and transmitter interrupt commands. The CSR is reset by a RESET L pulse to the CLR input of the chips. The LD CSR signal activates both CSR bytes and accomplishes the loading of the entire CSR. Several bits (0, 1, 2, and 11) are not used and have no effect on DZ11 operation.

4.4.2 Receiver Buffer (RBUF)

The Receiver Buffer (RBUF) is a read-only register that contains the received character (lower byte), the receiver line number (bits 8–10), and four character-condition signals relating to errors in reception (bits 12–15). Bit 11 is not used in the RBUF. The RBUF read command is generated in the address select logic whenever a DATI from Device Register 2 is decoded from the Unibus. The RD RBUF signal is inverted and fed to the receiver control logic to cause the first-in character of the silo to be read from the "bottom" (RBUF) of the silo (four 3341 chips at E59, E60, E57, and E58). The trailing edge of RD RBUF command causes a SHO H signal to be sent to the silo to shift the next character down through the 16-character positions.

4.4.3 Line Parameter Register (LPR)

The Line Parameter Register (LPR) is the write-only segment of Device Register 2 (Figure 4-18). The LPR contains various line parameters such as line number, character length, stop code, parity, DZ11 baud rate, and a receiver-on bit. The bits 13–15 are not used. The LD LPR signal is generated by the address select logic and fed to a 9602 one-shot (500 nanoseconds) that drives E62, an eight-bit addressable latch, and inhibits SSYN from being asserted on the Unibus. The latch is open and the LDATA L signal on pin 13 is gated to the proper UART, selected by RD(2:0) on pins 1, 2, and 3. This is the Control Strobe (CS) signal that loads the line parameter data for that line (e.g., character length, stop bits, and parity). The CS signal occurs approximately midway into the Inhibit SSYN signal; this allows proper data set-up time for the UART inputs. Refer to Figure 4-7 for the timing of the CS signal.

Latch E62 records bit 12 for the line selected and turns on the receiver clock (RCLK) for the selected line. Bits 8 through 12 are strobed into the baud rate generator chips by the CS pulse. The output of this chip is the transmitter clock (XCLK), which is gated by the condition of the output from latch E62 to give the RCLK for the UART.

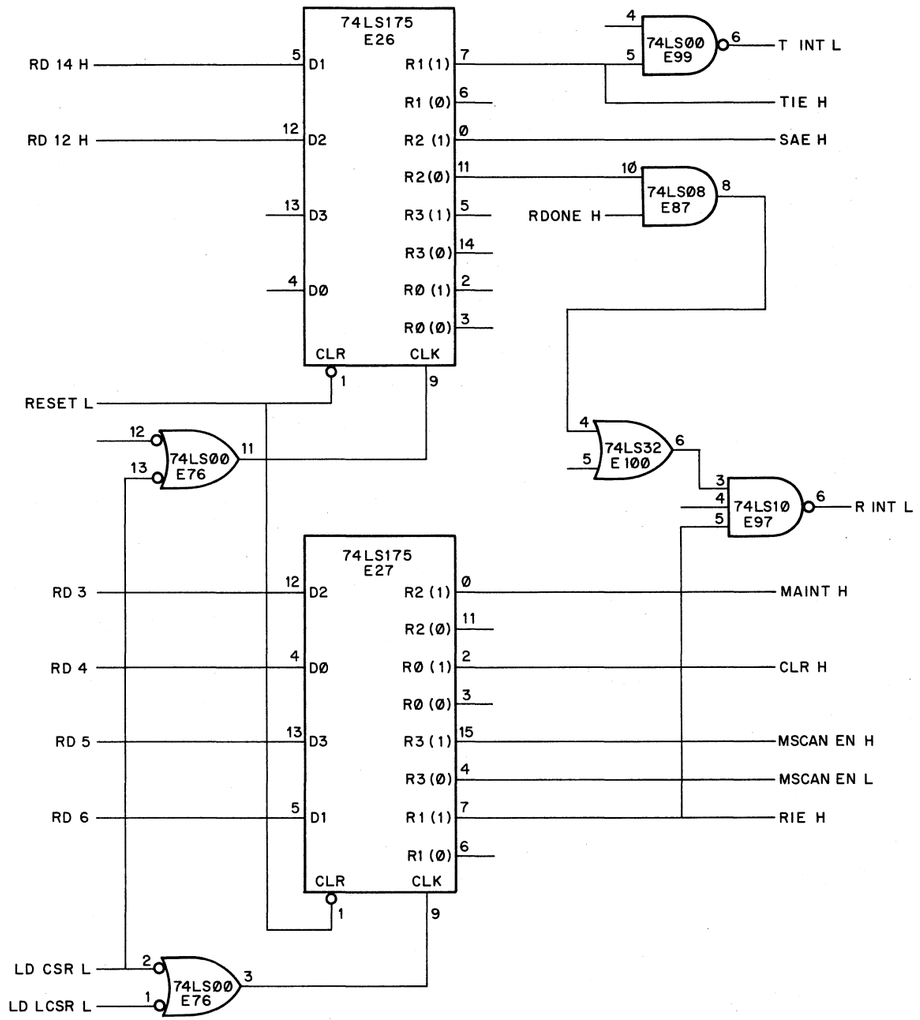


Figure 4-17 CSR Diagram

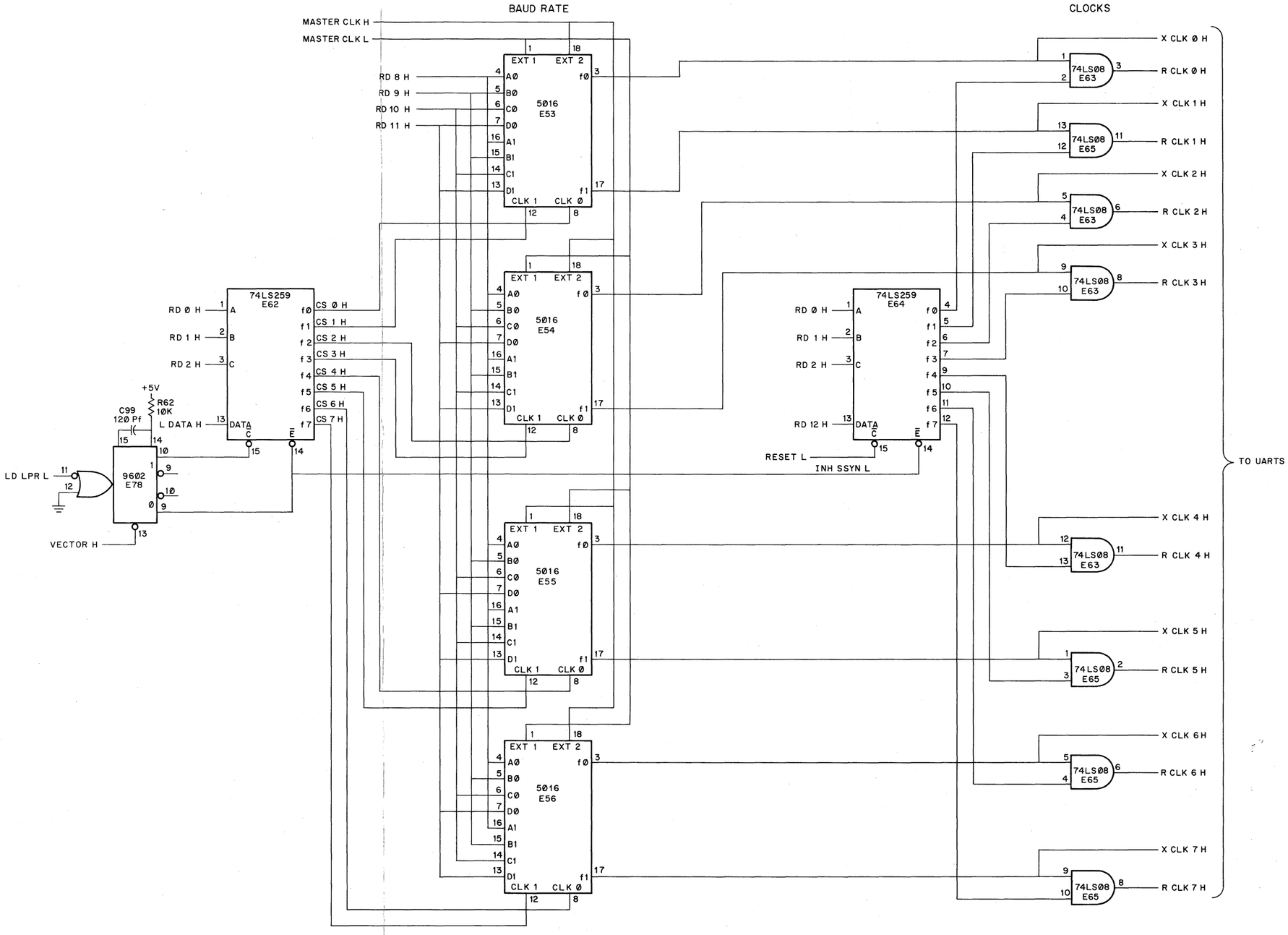


Figure 4-18 LPR Diagram

4.4.4 Transmit Control Register (TCR)

The Transmit Control Register (TCR) is a read-write register that comprises four 74LS175 chips, two for the low byte (line transmission enable) at E34 and E42, and two for the high byte (data terminal ready flags) at E15 and E18 (Figure 4-19). The register is controlled by LD TCR, LD LTCR, and LD HTCR signals from the address select logic. The inputs to the register originate from the Unibus lines and pass through the bus transceivers. The low byte of the TCR is cleared by RESET L and the high byte is cleared by INIT L.

4.4.5 Modem Status Register (MSR)

The Modem Status Register (MSR) is a read-only segment of Device Register 6. The MSR shown in Figure 4-20 examines data relative to the status of modem operation on each line, such as ring indication (low byte) and carrier-on flags (high byte). The register is dynamic in that it represents the current state of these lines. These lines must be continuously monitored as transitions on them do not cause interrupts.

4.4.6 Transmit Data Register (TDR)

The Transmit Data Register (TDR) is the write-only segment of Device Register 6. The TDR, using four 74LS175 chips, comprises two bytes, the low (E35 and E43) containing the character (TBUF) to be transmitted, and the high (E16 and E17) containing the break (BRK) bits for each line. When the BRK bit is set, the line transmits zeros continuously. This is accomplished by a NAND gate for each line that requires the BRK signal and SDO (serial data out) to produce the TRANS 0–7 L signals. The TDR is cleared by the RESET L pulse; for character lengths less than eight bits, the character must be right-justified, as the most significant bits are forced to zero. The TDR is controlled by LD HTDR, LD LTDR, and LD TDR commands from the address select logic.

4.5 UNIVERSAL ASYNCHRONOUS RECEIVER-TRANSMITTER (UART)

The UART is a complete integrated circuit subsystem that transmits and receives asynchronous data in duplex/half-duplex operation. The transmitter and receiver operate independently, and thus can operate simultaneously. The transmitter accepts parallel binary-coded characters and converts them to serial formats, and the receiver performs the reverse operation (serial-to-parallel). The UART requires several control signals to properly time its operation with that of the remaining DZ11 circuitry. Each UART is a 1602 integrated circuit, and one chip is used for each line. The UART chips are located at E44 through E51 on the DZ11 module. The baud rate, character length, parity mode, and number of stop bits are selected external to the UART. Figure 4-21 presents a block diagram of UART operation. A more detailed description of the UART is presented in the Appendix A of this manual.

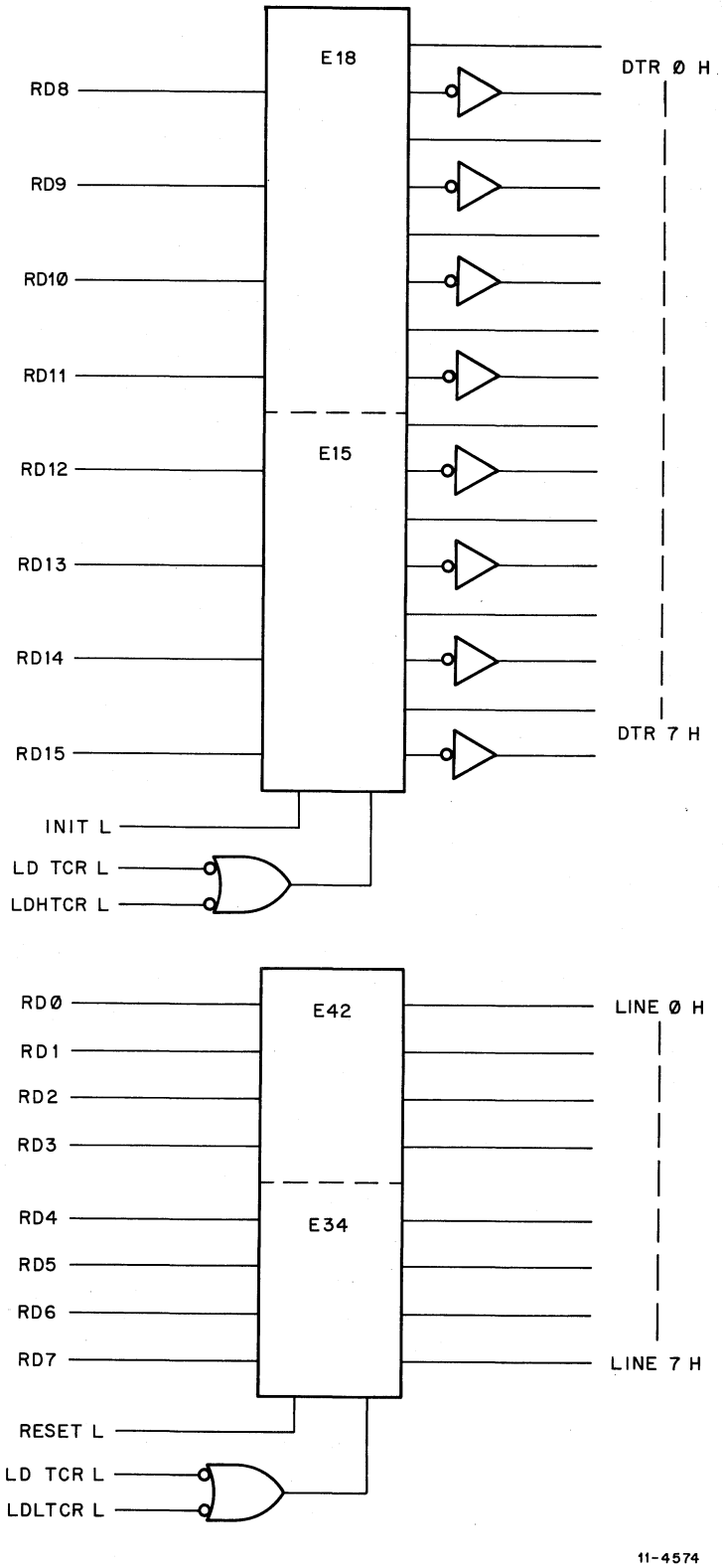


Figure 4-19 TCR Diagram

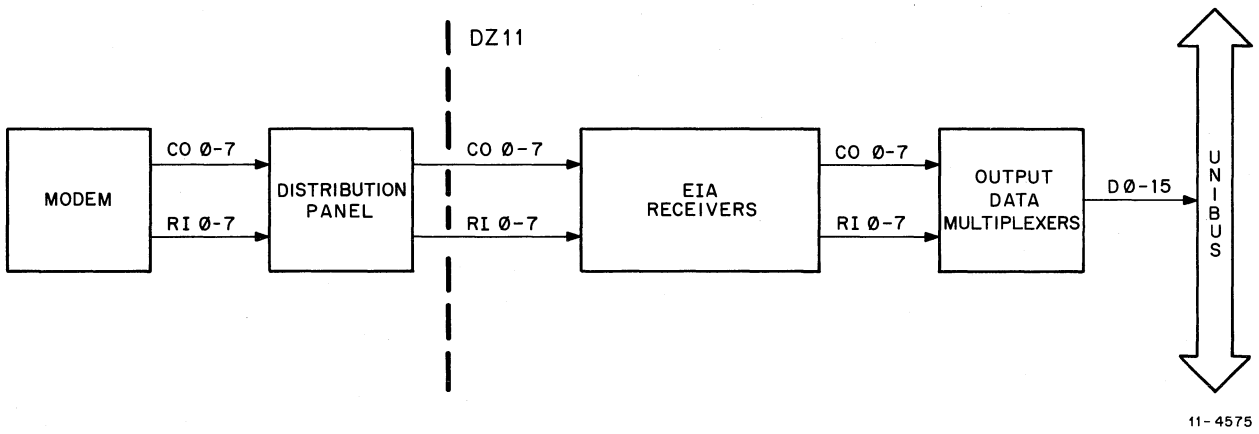


Figure 4-20 MSR Diagram

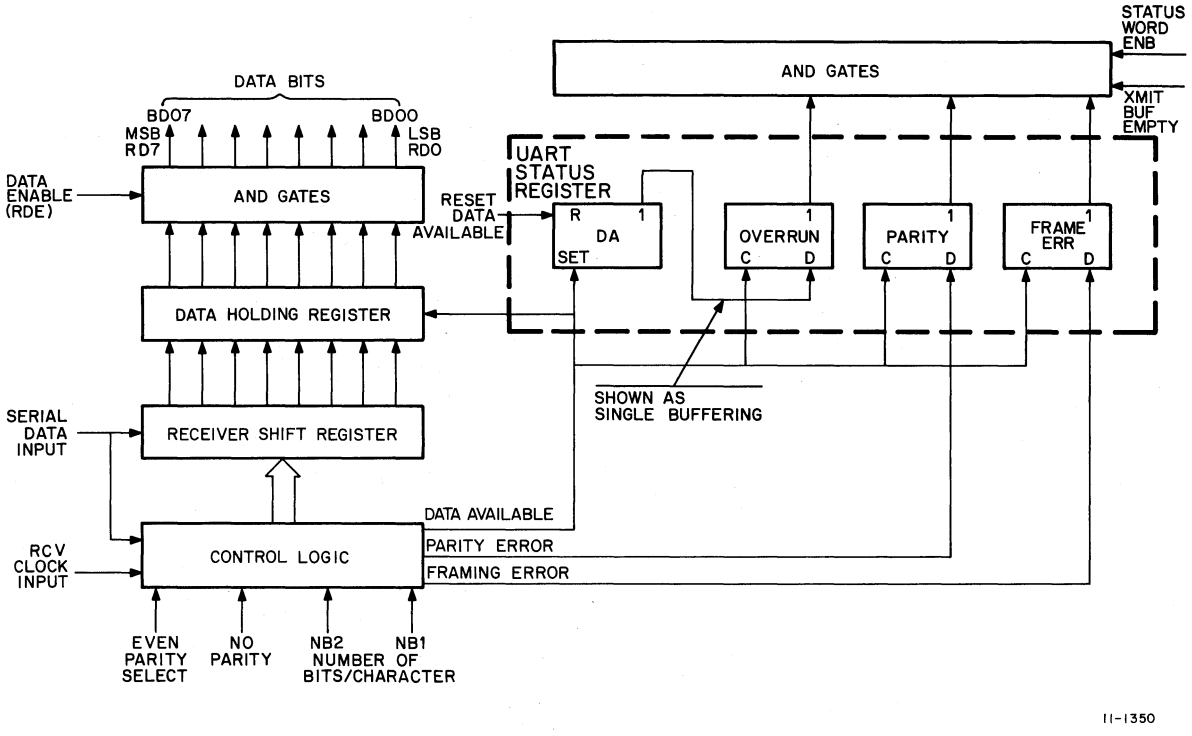


Figure 4-21 UART RCVR Block Diagram

CHAPTER 5
MAINTENANCE

5.1 INTRODUCTION

NOTE

This chapter will be revised in the final version of the manual.

The DZ11 maintenance philosophy assumes that proper and regular preventive maintenance can eliminate most equipment failures before they occur. The DZ11 module is designed such that module replacement can restore the system to operating status in minimum time. The corrective maintenance procedures contained in this manual and chapter are designed to assist the field service personnel in detecting commponent malfunctions on the DZ11 module, and ensuring proper DZ11 operation within the integrated system. Prior to performing the procedures outlined in this chapter, the material presented in the previous chapters should be thoroughly understood.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed at periodic intervals to ensure proper equipment operation and minimum unscheduled downtime. These tasks consist of running diagnostics, visual inspection, operational checks, adjustments, and replacement of marginally operating components. The preventive maintenance schedule depends on the environmental and operating conditions that exist at the installation site. Normally, preventive maintenance consists of inspection and cleaning every 600 hours of operation or every four months, whichever occurs first. For extreme conditions of temperature, humidity, or dust, and with abnormally heavy workloads, more frequent maintenance may be necessary. It is recommended that the DZ11 diagnostic (MAINDEC-11-DZDZA-REV-PB), be run once a week as part of the normal preventive maintenance schedule.

5.2.1 Mechanical Checks

Periodically inspect the DZ11 and the distribution panel for general mechanical condition. Inspect all wiring and cables for cuts, breaks, frays, deterioration, kinks, strain, and mechanical security. Check the module for proper seating and the security of all connecting cables; repair or replace any defective wiring or cable covering.

5.2.2 Test Equipment Required

Maintenance activities for the DZ11 require the standard test equipment and diagnostic programs listed in Table 5-1, in addition to standard hand tools, cleaners, test cables, and probes. Special test equipment required for any adjustments are given as part of that procedure.

Table 5-1 Test Equipment Required

Multimeter	Triplett or Simpson	Model 630NA or 260
Oscilloscope	Tektronix	Type 454 or equivalentl
Module Extender	Hex double-sided	W904
Diagnostics	MAINDEC-11-DZDZA MAINDEC-11-DZDZA	

5.3 DZ11 MAINTENANCE SOFTWARE

The DZ11 makes use of three different software packages which diagnose problems at the module level; verify operation at the system level; and verify operation over a communication's network channel. This software includes:

1. The DZ11 diagnostic - MAINDEC-11-DZDZA
2. The DZ11 system software exercisor module - MAINDEC-11-DXDZA
3. The Interprocessor Test Program (ITEP) overlay - MAINDEC-11-DZDZB.

The following paragraphs will describe each of them.

5.3.1 DZ11 Diagnostic

The DZ11 has one diagnostic that tests the two basic options available: The DZ11-A, B, and E which use the M7819 module with EIA output and the DZ11-C, D, and F which use the M7814 module with 20 mA output. Although both modules may be found in the same system, only one type at a time can be tested by the diagnostic. However, more than one module of the same type (up to 16) can be tested.

The function of the DZ11 diagnostic is to verify operation according to specifications and for proper operation in its actual environment. Test parameters can be supplied to the program by either AUTO-SIZING or by inputs from the user on the console. Console input can be performed at any time, however, auto-sizing is performed only the first time the program is started with all the computer console switches set to zero.

The diagnostic tests all parts of the DZ11 such as cables, distribution panel, and the interface module. To run the tests, several items are required:

Any PDP-11 family CPU with a minimum 8K memory
ASR-33 or equivalent console
If EIA Options, H315 (or H325) and H327 (if parity and break are tested) test connectors.

5.3.1.1 Storage - The program uses all 8K of memory except where ABL and BOOTSTRAP LOADER reside. Locations 1500 through 2000 are to be noted especially so that they remain untouched after the parameters have been input by console or auto-sizing. These locations may be changed only if the user understands their meaning and significance, and if different parameters are required for the tests.

5.3.1.2 Loading - All programs are in absolute format and are loaded using the ABSOLUTE LOADER. If the diagnostics are stored on another medium, such as disk, magnetic tape, DECtape, or cassette, follow the instructions for the monitor provided for that medium. The ABSOLUTE LOADER address is 500, with the following sizes corresponding to the memory capacities: 4k - 17, 8K - 37, 12K - 57, 16K - 77, 20K - 117, 24K - 137, 28K - 157. To load the diagnostics, perform the following:

1. Place the address of the ABSOLUTE LOADER (500) into the switch register, and place the HALT switch to its up position.

2. Depress LOAD ADDRESS key on the console, then release the key.

3. Depress START KEY on the console and release. The program should now be loading into the CPU.

5.3.1.3 Starting - After loading the program, the following procedure will begin the diagnostics:

1. Set switch register to 000200.

2. Depress and release LOAD ADDRESS key.

3. Set SWR to zero for AUTO-SIZING, or set SW00 = 1 for user input.

4. Depress START key and release. The program will type "Maindec", "name", and "program name" if this was the first start-up of the program or parameters were changed by SW00 = 1. Also, the program will type the following.

MAP OF DZ11 STATUS

1500	160010
1502	000300
1504	000005
1506	000377
1510	017470
1512	000000

The above printout is only an example that would indicate that the Status Table starts at address 1500. The Status Table must be verified by the user if auto-sizing is done. For additional information on the Status Table, refer to Paragraph 5.8. After the Status Table, the program will type "RUNNING", and proceed to run the diagnostic. The following control switch settings can be made:

SW15	Halt on Error
SW14	Loop on Current Test
SW13	Inhibit Error Printout
SW12	Bell on Error
SW11	Inhibit Iterations (Quick Pass)
SW10	Escape to Next Test
SW09	Loop with Current Data
SW08	Catch Error and Loop
SW07	No Auto Size, CLR Do Auto Size (if first start after loading)
SW06	Reselect DZ11's Desired Active
SW05	Reserved
SW04	Allows selection of test delays from console (used only as troubleshooting aid)
SW03	Extra Parameter Input
SW02	Lock on Selected Test
SW01	Restart Program at Selected Test
SW00	Get User's Parameters from Console

5.3.1.4 Register Restrictions – The following register restrictions must be observed by the user:

1. RESELECT DZ11 DESIRED ACTIVE (SW06) – If the system has four DZ11's, a message is typed out for setting the switch register equal to the DZ11's active, meaning that bits 00, 01, 02, 03 will be set in memory location DZACTV from the switch register. Switch SW06 alters the DZACTV location, therefore, if four DZ11s are in the system, DO NOT set switches greater than SW03 to the up positions. Also, DO NOT select more active DZ11s than information given in the parameter input with SW00 = 1. The correct procedure is as follows:

   a. Load address 200, and start with SW06 = 1. Program will type message.

   b. Set the binary number of DZ11's desired active (for example, 1 = 1 DZ11, 3 = 2 DZ11s, 7 = 3 DZ11s, 17 = 4 DZ11s, etc.).

   c. Press CONTINUE and the number set in the switch resistor will be displayed in the data lights (on all but the 11/05).

   d. Set other desired switch settings and press CONTINUE.

2. RESTART PROGRAM AT SELECTED TEST (SW01) – It is suggested that at least one pass has been made before trying to select a test not in the sequential order, since the program has to clear areas and set parameters. If running multiple DZ11s, the DZ11 desired to be under test must be selected by SW06 before test lock-on; in other words, each time the program is started, the first DZ11 will be selected to be under test unless SW06 is used to select the desired one.

3. LOOP ON CURRENT DATA (SW09) – This switch is active only if the call SCOP1 is in the test. Since most tests deal with blocks of different data, one pattern cannot be singled out unless specified.

4. SELECT DELAY (SW04) – This switch allows the diagnostic delays to be selected from the console. It is strictly used for trouble-shooting in order to shorten loops so that a problem can easily be checked with an oscilloscope. The switch should be used with switch 1 and 2 to start and lock on the test that is failing. The normal delay count is "36". The shortest count is 1 (0 cannot be used); also, care should be taken not to introduce failures because of too short a delay count.

5.3.1.5 SWITCH REGISTER PRIORITIES

ERROR SWITCHES

SW12	Bell on error
SW13	Delete error printout
SW15	Halt on the error
SW08	Go to beginning of the test (on error)
SW10	Go to next test (on error)

5.3.1.6 SCOPE SWITCHES

SW09 (if enabled by 'SCOP1') on an error; if an '*' is printed in front of the test no. (ex. * TEST
NO. 10) SW09 is incorporated in that test and therefore SW09 is * usually * the best switch for the scope loop (SW14=0, SW10=0, SW09=1, SW08=0). If SW09 is not enabled; and there is a * HARD * error (constant); SW08 is best.
(SW14=1,0, SW10=0, SW09=0, SW08=1), for intermittent errors; SW14=1 will loop on test regardless of error or not error.
(SW14=1, SW10=0, SW09=0, SW8=1,0)

SW14
SW11

5.3.1.7 STARTING ADDRESS

SA200 Address 200 is for normal execution of the diagnostic. This will do the major testing necessary for verification of hardware.

SA210 CABLE/ECHO – Terminal Tests. Starting at address 210 will give the user the option to verify the EIA cables at the dist pnl or verify a true link to any DEC supported EIA terminal supported by the DZ11. 20 mA modules cannot do Cable Test but only the ECHO Test to a terminal.

NOTE

If address 000042 is non-zero the program assumes it is under ACT11 or XXDP control and will act accordingly. After * ALL * available DZ11s are tested the program will return to "XXDP" or "ACT-11."

5.3.1.8 Operations Procedure

(a) NORMAL START OF DIAGNOSTIC

On the first start of the diagnostic at address 200; if auto sizing is not used or whenever SW00=1; the following questions are asked and must be answered.

1ST CSR ADDRESS (160000:163700):

You must type in the first DZ11 CSR in the system you wish testing to begin at. RANGE: 160000:163700

1ST VECTOR ADDRESS (300:770):

You must type in the vector of the first DZ11 in the system under test. RANGE: 300:770

BR LEVEL (4:7):

Type in the priority level of the DZ11 that the above information has been given about. RANGE 4 or 5 or 6.

TYPE "A" FOR EIA MODULE OR "B" FOR 20 mA (A:B):

Type "A" if running a DZ11-A, B, E (EIA)
Type "B" if running a DZ11-C, D, F (20 mA)
Typing a <CR> defaults to EIA MODULES.

MAINTENANCE MODE
[EXTERNAL <H325> (E)]
[INTERNAL <DZCSR03=1> (I)]
[STAGGERED <H327> (S)

Type "E" or "I" or "S" depending on which mode you wish to run in. If running "EXTERNAL"; all selected lines must be terminated by a H325 test connector.

$ OF DZ11s <IN OCTAL> (1:20):

Type total number of DZ11s to be tested in the system. RANGE is 1 thru 20 in octal.

********** IF SW03=1 THEN **********
If SW03=1 the following will be printed.

LINES ACTIVE BY BIT <IN OCTAL> (001:377):

Each bit represents a line and any combination of lines may be selected (HOWEVER IN STAGGERED MODE TWO ADJACENT LINES MUST BE SELECTED (0-1, 2-3, 4-5, 6-7)).

DEFAULT BAUD RATE <IN OCTAL> (00:17):

This gives the user a chance to change the default baud rate used in APP, 90% of the test. Normal operation is a "17" (19.2K) or "16" (9.6K), "00" (50 baud) - Not advised.

****
It is important to note that all DZ11s in the system must be CONTIGUOUS for both ADDRESS and VECTORS, also all the EXTRA PARAMETERS other than CSR and VECTORS are given to the EXISTING DZ11s in the system. If not all DZ11s are same priority or if the mode of operation is different for each DZ11; THIS MUST BE "PATCHED" INTO THE CORRECT STATUS MAP ENTRY which is printed at start time. An alternative is to put SW00=1 at start time; answer questions about DZ11 under test and INDICATE ONLY 1 DZ11 in the system. IF THE STATUS MAP IS TO BE "PATCHED" IT MUST BE DONE AFTER THE QUESTIONS ARE ANSWERED OR AFTER THE AUTO SIZE.

(b) HOW TO RUN THE "CABLE/ECHO" TESTS

Normal starting for the first time would be: LOAD ADDRESS 210; START WITH THE SWR EQUAL TO 213.

NOTE
SW00=1 ASKS FOR "VECTOR" AND "CSR"
SW01=1 ASKS FOR "WHICH TEST ECHO OR CABLE", "BAUD RATE", "LINE" UNDER TEST. Program will print out:

VECTOR ADDRESS–

You type vector with a <CR>.

CONTROL REGISTER ADDRESS–

You type in DZCSR under test.

WHICH TEST? ECHO OR CABLE (E OR C)

Lets do the CABLE TEST first. **THIS TEST IS ONLY TO BE DONE ON THE EIA VERSION OF THE DZ11 NOT THE 20 mA VERSION". Type "C" <CR>

BAUD RATE–

Type either 50, 110, 135, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 followed by <CR>

LINE:

You type the line which has the H325 test connector. (Type either 0, 1, 2, 3, 4, 5, 6, 7). Program will then print:

CABLE TEST

and if everything is working; the following will be printed:

PASS DONE.
PASS DONE.
etc.

to change lines; HIT ANY PRINTING KEY ON YOUR CONSOLE TERMINAL WHILE THE PROGRAM IS RUNNING and the following will be printed:

LINE:

Now change the H325 test connector to another line and type the new line. Program will then print:

CABLE TEST
PASS DONE.
PASS DONE.

Continue this operation until all lines are tested.

(c) ECHO TEST

If program has already been started at 210 and the vector and address have been typed in; just load address 210 and start with SWR equal to 212. Program will print:

WHICH TEST? ECHO OR CABLE (E OR C)

Now type an "E" to do the ECHO TEST. Program will print:

BAUD RATE–

Type BAUD RATE at which the terminal is set that is connected to the DZ11 dist pnl. Program will print:

LINE:

Type the line the terminal is connected to at the dist pnl, then the program will print:

TERMINAL ECHO TEST

*** AT THIS POINT THE MESSAGE:

THE QUICK BROWN FOX JUMPED OVER THE LAZY DOGS BACK 0123456789

SHOULD BE PRINTED ON THE TERMINAL CONNECTED TO THE DZ11. IF THIS MESSAGE IS DESIRED TO BE CONTINUOUSLY OUTPUT; SET THE SWR TO 377 (SWR=377) WHILE IT IS BEING OUTPUT OR WHEN PROGRAM IS STARTED AT 210. WHEN THIS MESSAGE IS DONE AND THE SWR IS NOT EQUAL TO 377; THE CONSOLE WILL PRINT:

TYPE A CHAR. ON DZ11 TERMINAL

any printable char hit on DZ11 terminal should be echoed back on the terminal. **IF YOU HIT CNTRL C <-C> ON THE DZ11 TERMINAL THE PROGRAM WILL PRINT:

PASS DONE.

on the console terminal and the "QUICK BROWN FOX" will be printed on DZ11 terminal again and the echo test will be running. TO CHANGE LINES; do like cable test. HIT PRINTABLE KEY ON CONSOLE TERMINAL, and change the line on which the terminal is connected, and enter the new line to the program.

5.3.1.9 Program and/or Operator Action

The typical approach should be

1. Halt on error (via SW15=1) whenever an error occurs.
2. Clear SW15.
3. Set SW14: (loop on this test)
4. Set SW13: (inhibit error printout)

The TEST NUMBER and PC will be typed out and possibly an error message (this depends on the test) to give the operator an idea as to the source of the problem. If it is necessary to know more information concerning the error report; LOOK IN THE LISTING for that TEST NUMBER which was typed out and then NOTE THE PC of the ERROR REPORT this way the EXACT FUNCTIONING of the test CAN BE INTERPRETED.

ERRORS

As described previously there will always be a TEST NUMBER and PC typed out at the time of an error (providing SW13=0 and SW12=0), in most cases additional information will be supplied to the error message which is to give the operator an indication of the error.

ERROR RECOVERY

If for some reason the DZ11 should "HANG THE BUS" (gain control of bus so that console manual functions are inhibited) an init or power down/up is necessary for operator to regain control of CPU. If this should happen; look in location "TSTNO" (address 1216) for the number of the test that was running at the time of the catastrophic error. In this way the operator will have an idea as to what the DZ11 was doing at the time of the error.

RESTRICTIONS

STARTING RESTRICTIONS

Status table should be verified regardless of how program was started. Also it is important to use this listing along with the information printed on the TTY to completely isolate problems.

OPERATING RESTRICTIONS

Parameter must be input from user if "AUTO SIZING" is not used.

MISCELLANEOUS

EXECUTION TIME

All DZ11 device diagnostics will give an "END PASS" message (providing no errors and SW12=0) within 1 min. This is assuming SW11=1 (DELETE ITERATIONS) is set to give the fastest possible execution. The actual execution time depends greatly on the PDP-11 CPU configuration.

PASS COMPLETE

NOTE: * EVERY * time the program is started; the tests will run as if SW11 (delete iterations) was up (=1). This is to "VERIFY NO * HARD * ERRORS" as soon as possible. Therefore the first pass -EACH TIME PROGRAM IS STARTED- will be a "QUICK PASS" until all DZ11s in system are tested. When the diagnostic has completed a pass the following is an example of the printout to be expected.

END PASS DZDZA-A CSR: 160010 VEC: 300 PASSES: 000001 ERRORS: 000000

NOTE

The numbers for CSR and VEC are not necessarily the values for the device. They are only for this example.

KEY LOCATIONS

RETURN	(1204)	Contains the address where program will return when iteration count is reached or if loop on test is asserted.

NEXT	(1206)	Contains the address of the next test to be performed.
TSTNO	(1216)	Contains the number of the test now being performed.
RUN	(1304)	The bit in "RUN" always points one past the DZ11 currently being tested. EXAMPLE: (RUN) 1304/0000000001000000 Means that DZ11 no. 05 is the DZ11 now running.
STATUS MAP (1500) -	(2000)	These locations contain the information needed to test up to 16 (decimal) DZ11s sequentially. They contain the CSR, VECTOR and STATUS concerning the configuration of each DZ11.
DZACTV	(1300)	Each bit set in this location indicates that the associated DZ11 will be tested in turn. EXAMPLE: (DZACTV) 1300/0000000000011111 means that DZ11 no. 00,01,02,03,04 will be tested. EXAMPLE: (DZACTV) 1300/0000000000010001 Means that DZ11 no. 00,04 will be tested.
DZSCR	(1420)	Contains the receiver CSR of the current DZ11 under test.

MORE ON THAT "STATUS TABLE" (1500–2000)

MAP OF DZ11 STATUS

1500	160010
1502	000300
1504	000005
1506	000377
1510	017470
1512	000000

The above information will be repeated for each of up to 8 DZ11s in the system (these will follow under this table). EXPLANATION:

1500	160010	This is the system control register for the 1st DZ11 in the system.
1502	000300	This is vector "A" for the first DZ11 in the system.
1504	000005	This represents the bus interrupt priority level of the DZ11. Bit 15 of this location indicates either EIA or 20 mA, if bit 15=0 module should be EIA; if bit 15=? module should be 20 mA.
1506	000377	This is the binary representation of what lines are to be tested.
1510	017470	This is the parameter location used in most of the tests. It indicated parameters of: RX ON, SPEED SELECT 17 (19, 2K Baud) EIGHT BITS PER CHAR, AND TWO STOP BITS. The user may alter the stop bits and the speed, but the remaining parameters should be left alone.

1512	000000	This location will contain either all zeros indicating that internal loop was selected as mode of operation or it will contain 10000 indicating that "staggered mode" was selected or it will contain 000200 indicating that "external" was the mode selected.

The above is repeated for each DZ11 in the system. The table is filled by AUTO SIZING or by the manual parameter input program as described previously. Also if desired by user, the locations may be altered by hand (toggled in) to suit the specific configuration.

5.3.2 DZ11 System Exerciser

Each PDP-11 system has associated with it a DEC X/11 system exerciser program made by linking together software modules that exercise the various hardware in the system. The software module for the DZ11 runs up to eight consecutively addressed M7819 or M7814 modules (two software modules are needed if 16 or more than 8 DZ11 interfaces are on the system). It uses the maintenance mode (bit 3 of CSR set) to transmit and receive a binary count pattern outfitted and received in 64 character bursts. All devices selected for test are activated and run concurrently with all eight lines on each active device selected.

5.3.2.1 Storage – Each software module requires 1289 words.

PASS DEFINITION:

One pass of the DZA module consists of transmitting and receiving 8960. Characters for each line of each DZ11 selected.

EXECUTION TIME:

Execution time is proportional to the baud rate but should take an average of one minute to complete one pass when running alone on a PDP-11/40 at 9600 baud.

CONFIGURATION PARAMETERS:

Default Parameters:
DVA: 1, VCT: 1, BR1: 5, BR2: 5, DVC: 1, SR1: 0

Required Parameters:
At configuration time the user must specify:

DVA Address of first DZ11 CSR reg.
VCT Vector address of first DZ11
DVC No. of DZ11s if greater than 1

Module location DVID1 (APC=14) may be modified (MOD. CMMD) to exercise any combination of eight DZ11s.

Module location SR1 (APC=16) may be modified to select a different baud rate. The following table should be used:

For the Baud Rate	SR1=	LOC 336=
7200	1	2060
4800	2	2000
3600	4	1730
2400	10	1460
2200	20	1350
1800	40	1350
1200	100	1200
600	200	630
300	400	330
150	1000	150
134.5	2000	144
110	4000	120
75	10000	70
50	20000	45

(Location 336 is the location of the iteration constant. Using these values will yield an End of Pass close to one minute for each baud rate.)

The Default Rate is 9600 baud (SR1=0).

Module location SLCTLIN (APC=310) may be modified to run any combination of eight lines. The combination is then run on all selected devices. The default selection is all eight lines.

NOTE

SLCTLIN falls on a byte boundary. Be sure to restore the bits set in the other byte.

Module location RESTRT +2 (APC=336) May be modified to vary the period between End of Pass Reports.

Module Location TMRSET +2 (APC=752) May be modified to vary the period of the Watch-dog Timer. It is presently set to expire after seventy-five seconds when DZA is running alone.

NON-STANDARD PRINTOUTS:

When a status error is detected, DZA uses the ERRORN call to report it. The first number given is the number of the device (0 to 7). The second is the contents of the read buffer (DZRDBUF= CSR + 2, e.g., 160042).

When all characters are not received, an ERRORN call is reported. The first number is the number of characters expected. The second is the number of characters that were not received.

All other printout is standard.

MNEMONICS

The following information should be useful in understanding names given to variables in this program.

XMT refers to the transmitter
RCV refers to the receiver
ERR refers to anything to do with error handling
FLG refers to a software flag, usually a bit flag
QUE refers to a first in, first out buffer
TMR refers to software timing functions
CNT refers to a word used as a counter
QP refers to a pointer associated with a queue buffer
I is an insertion pointer, 0 is an output pointer
LN refers to something involving a given line
XM is another reference to transmitter
CT generally refers to a count

e.g.:XMTQPO=transmitter queue pointer out

Others are basically self-explanatory.

5.3.3 DZ11 ITEP OVERLAY

1.0 ABSTRACT
This program is designed as a maintenance aid for Field Service Personnel. It will verify the proper operation of a complete communication link from one PDP-11 system to another or to a communication test center.

This program must be used in conjunction with the interprocessor test program (DZITP) on a PDP-11 system with a DL-11 interface.

2.0 REQUIREMENTS

2.1 EQUIPMENT

A. PDP-11 system with 4K of core.
B. A DZ11 communication interface.

2.2 STORAGE
4K of core

3.0 LOADING PROCEDURE
This program is in absolute format. The ABS loader must be used to load the program.

4.0 OPERATING PROCEDURES

A. Two methods of entering parameters are provided.

1. Load Address 200 and start to enter params from console TTY. Proceed to Section B.

2. Load Address 200 and set switch register bit 15 before starting to enter params from console switches. Proceed to Section C.
NOTE: The program may be restarted at Loc 204 (once parameters have already been selected).

B. Console dialogue parameter input (current values for parameters are found in overlay).

1. The program will type out the name of the variable overlay.

   a. If you wish to set up just the indicated overlay, type a carriage return.
   b. If you wish to set up a DN11, type in DN.
   c. If you wish to set up a DM11BB, type in DMB.

   If DN or DMB was typed in step 1 above, then the Bus Address, Vector, etc. referred to in steps 2 through 7, pertain to the DN11 or DMBB.

2. The program will type the default Bus Address of the interface under test.

   a. Type a car, return to use default Bus Address.
   b. Type in actual Bus Address.

3. The program will type out the default Vector Address.

   a. Type a car, return to use default address.
   b. Type in actual Vector Address.

4. The program will type out the default interface priority.
   NOTE: 200=PR10 4, 240=PR10 5, 300=PR10 6, etc.

   a. Type a car, return to use default value
   b. Type in actual value

5. The program will type out the default value of param #1, if required by the ISR. (See Section 10.0 in Overlay Listing for Parameter.
   a. Type a car. return to use default value.
   b. Type in actual value

6. The program will type out the default value of param #2 if required by the ISR.
   a. Type a car. return to use default value.
   b. Enter actual value.

7. The program will type out the default value of param #3 if required by the Overlay.
   a. Type a car. return to use default value. The DN-11 will use param #3 as the # to dial. If using a modem without automatic handshaking, the number must terminate with an "End-of-Number" character (:).
   b. Enter actual value.

8. The program will return to step B1 if this setup was for DN11 or DM11BB.

9. The program will request that switch register be set.
   a. Set up switch register as specified in step D, and type a car. return.

   NOTE: If any of the above items 2 through 7 were changed by entering new values, the new value becomes the default value for subsequent restarts of the program.

C. Manual parameter input from Switch register.

1. The program halts for ISR (Interface Service Routine) specification.
   SWR14=Set up DM-11B ISR
   SWR13=Set up DN-11 ISR
   SWR=000000=Set up Variable ISR

2. The following halts are repeated for each ISR specified. Setup sequence is: DN11, DM11-BB then Variable Overlay. (Each entry set switches then hit CONTINUE)
   a. HALT for Bus Address of Interface
   b. HALT for Vector Address of Interface
   c. HALT for Priority of Interface
   d. HALT for Interface param #1 (See Section 10.0 in Overlay Listing for parameter description)
   e. HALT for Interface param #2 (DN11 and DMBB parameters are discussed in Section 10.0 of the MON
   f. Go back to step A if this setup was for DN or DMB.

3. HALT for operational switch settings. (See Step D.)
   a. Press CONTINUE to start testing.

Before attempting to run this program, the operator must ascertain the complete communication loop and procedures to be used, including the type of modems, the type of interface being used at the other CPU and the modes of operation, data and parameters to be used at each CPU.

This will require vocal communication with the operator at the other CPU unless its configuration and operation are fixed as a Test Center.

After determining that the equipment is compatible and agreeing on the mode and variable parameters to be used. The system which is to receive data first should be loaded and started. If the modem being used on this system has an automatic answer feature, it should be enabled.

The system which is to transmit first should then be loaded and started and the connection established either manually or automatically (via DN-11).

D. Operational Switch Settings

SW15=1 Halt on Error
SW14=1 Single Pass
  SW14 has no effect if SW04=0
SW13=1 Inhibit Error Typeouts
SW12=1 Inhibit all Typeouts Except Errors
  If SW12=0 and SW04=1 end pass is typed and transmitted/received data is typed
SW11=1 Use previously specified data
SW10=1 Data Select (with SW09)
SW09=1 Data Select (with SW10)
  00=1 Get data from operator
  01=1 Test message #1 ($A QUICK BROWN FOX)
  10=1 Test message #2 ($B NUMERICS)
  11=1 Test message #3 ($C COMTEST/QUICK BROWN FOX/NUMERICS)
SW08=1 Transmit received data (Internal Loopback mode)

SW07=1 Do not test received data
SW06=1 Monitor transmitted data on console TTY.*
SW05=1 Monitor received data on console TTY.*

*In many cases, not all data will appear on the console TTY. This is especially true when the COMM Interface is running at a faster baud than the console, but even at equal or slower bauds, all characters may not appear on the console.

SW04=1 Return to monitor for end pass
When SW04=0 program loops in the overlay never returning to the monitor.
SW03=1 Internal Loopback mode
SW02=1 External Loopback mode
SW01=1 One-Way-In mode
SW00=1 One-Way-Out mode

If operator specified data was indicated, the program will type a request for the data. Data may be entered as ASCII characters or octal code. Type in the data terminated with a CR. Octal code may be entered by typing an ↑ (up arrow) followed by the octal code (in the range 000 to 377) separated by spaces and terminated by ↑ (up arrow).
i.e., ABCD↑ 000 123 377↑ EFG (Car. return)

A typical switch setting for half-duplex=003150. This setting uses internal loopback mode, loops in overlay, monitors transmitted and received data on the console TTY, and tests received data using test message #3.

A typical switch setting for full-duplex=003144. This setting is the same as above except it uses the external loopback mode.

All standard messages (test messages 1–3) are preceded by 2 fill characters (177), and are followed by a CR(015), LF(012), receive terminating character(001), 4 fills(177); and a transmit terminating character (000). During transmission, when a 000 character is seen, the transmission is stopped. During reception, when a 001 character is received, the receiver is shut off. If the message was input by the operator, the terminating characters are added.

TEST MODES

INTERNAL LOOPBACK MODE

1. The overlay waits to receive a message (terminated by <001>)
2. Verifies the data against the data selected by SW09 and SW10 (SW7=0)
3. Transmit the data selected by SW09 and SW10 (SW8=0) or transmit the received data (SW8=1)
4. Returns to monitor for "END PASS" (Sw4=1) or go to step 1. (SW4=0)

EXTERNAL LOOPBACK MODE

1. The overlay sets request to send
2. Wait for clear to send
3. Transmits the selected data
4. Resets request to send
5. Wait for message to be received
6. Verifies the data (SW07=0)
7. Returns to monitor for "END PASS", (SW04=1) or go to step 1 (SW04=0)

ONE-WAY-IN MODE

1. The overlay waits for message to be received
2. Verifies the data (SW07=0)
3. Returns to monitor for "END PASS" (SW04=1) or go to step 1 (SW04=0)

ONE-WAY-OUT MODE

1. The overlay sets request to send
2. Waits for clear to send
3. Transmits selected data
4. Returns to monitor for "END PASS", (SW04=1) or go to step 1 (SW04=0)

E. The overlay is then entered and a connection established either manually or automatically.

If One-Way-In or Internal Loopback modes are selected, the overlay will set data terminal ready and wait for data.

If One-Way-Out or External Loopback modes were selected, the overlay will set data terminal ready and request to send. The overlay will then wait for clear to send before attempting to transmit data.

The program will printout a "WAITING FOR CLEAR TO SEND" message and the contents of the XMIT CSR every 60 seconds until Clear to Send is asserted.

F. If SW0=0, the overlay will continue to transmit/receive data.

If SW04=1, the overlay will return to the monitor and type "END PASS".

If both SW04=1 and SW14=1, the program will request new interface params after one pass of the selected test mode.

Test execution may be interrupted by typing the following characters on the console TTY.
LINE FEED = Restart program at location 200.
QUESTION MARK = Printout first 8 words of input buffer (ASCII).
Set Switch 15 and press CONTINUE for next 8 words.
Program must be restarted at 2?? after printing.
CARRIAGE RETURN = Restart at request for new operational switches.

PROGRAM AND/OR OPERATOR ACTION

If the operator wishes to manually examine the transmit or receive buffers, do the following: To find the starting address of the receive buffer, load address 10020 and examine. To find the starting address of the transmit buffer, load address 10022 and examine.

ERROR REPORTING

The only error report from the control program occurs if the interface specified is not loaded.

If data is received and switch 7 (no data compare) is reset, the data will be compared against the preselected data after a line feed character is received. If there is a mismatch, the following error report is printed.

RECEIVED DATA=RRRRRR

DATA SHOULD BE TTTTTT

DATA COMPARE ERROR: BAD DATA=BBB GOOD DATA=GGG

Where RRRRRR is the receive buffer (up to 512 characters)
TTTTTT is the transmit buffer (Up to 512 characters)
BBB is the bad data character
GGG is the good data character

If the interface detects a data error, the following will be printed before the data is compared:

There was a receiver error, Receiver Data register =XXXXXX

Where XXXXXX is the contents of the Receiver Data register, the low byte is the data, and the high byte is the error bits.

If a receive terminating character <001> is not detected within 512 characters a "BUFFER FULL" printout will occur.

RESTRICTIONS

The operation of this program requires coordination between the operator and the operator of another PDP-11 system unless one of the systems is always operating in a fixed mode. The following table lists the valid combinations:

CPU #1	CPU #2
One-Way-Out	One-Way-In
One-Way-In	One-Way-Out
External–Loopback	Internal–Loopback
Internal–Loopback	External–Loopback
External–Loopback	External–Loopback (full duplex)

When the communication link involves modems the following restrictions apply.

If running in full duplex mode both systems must be in External Loopback mode.

Both systems should be running identical routines. Example: Switches 14, 13, 7, 4 should be the same on both CPUs

If program is waiting in a scan routine and types out a "WAITING MESSAGE", if an incoming message starts during the typeout, it will be lost because the typeout priority is at level 7, this will result in overrun or silo overrun errors, depending on the device. To avoid this situation, run with switch 13 up. If overrun does occur during a typeout the program should be restarted.

If using an asynchronous device, modems and the Maynard Test Station and initialize does not clear the connection (Example: the DJ11), if the program is restarted in the middle of a message at Loc 204 or by hitting CR, an immediate error message from Maynard will be received, this is because the test station is still looking for the rest of the interrupted message. To avoid this error, restart program only at the end of the message currently being transmitted.

MISCELLANEOUS

ITEP was checked out using the following Bell Telephone modems.

201A (half-duplex synchronous 2000 baud)
202C (half-duplex asynchronous 1200 baud)
103A (full-duplex asynchronous 110 baud)

PROGRAM DESCRIPTION

The DZ11 interface service params are set up, as specified by the operator, by the ITEP control program.

TIME: Provides a means of measuring elapsed time. It is incremented every second by a clock interrupt routine in ETEP.

When the overlay is first entered by ITEP at location START1, the contents of the Switch register are stored in Register 0. The Mode and Data selections are fixed at this time and cannot be altered without returning to the control program. The interrupt vectors and variables are then set up. The selected routine determined by the mode is then entered.

The overlay then loops in routines: $OWI,if "ONE-WAY-IN" mode was selected. $OWO, if "ONE-WAY-OUT" mode was selected. $ILB, if "INTERNAL LOOP BACK" mode was selected. $XLB, if "EXTERNAL LOOP BACK" was selected.

$OWI: In this routine the receiver is initialized ans program loops waiting for the receiver to finish. If nothing is received for 60 seconds, a "WAITING" message is typed. When the receiver is done, the program checks data if switches permit, and types END PASS depending on switch settings.

$OWO: The transmitter is initialized and program loops waiting for transmitter to finish. A "WAITING" message is typed every 60 seconds if there is no action. When the transmitter is done, the program either loops back to $OWO or types END PASS depending on switch settings.

$ILB: The receiver is initialized and program loops waiting for receiver to finish. A "WAITING" message is typed every 60 seconds if no action. When receiver is done, program checks data if switch settings permit, and END PASS is typed if switch settings permit, then the transmitter is initializd. A "WAITING" message is typed every 60 seconds if no action. When transmitter is done, program returns to start of routine, ($ILB).

$XLB: If in half-duplex, the transmitter is initialized. A "WAITING " message is typed every 60 seconds if there is no action. When the transmitter is done, the receiver is initialized. A "WAITING" message is typed every 60 seconds if there is no action. When the receiver is done, data is checked if switch settings permit and END PASS is typed if switches allow. The program now repeats cycle starting at $XLB.

If in full-duplex, the receiver and transmitter are initialized. A "WAITING" message is typed every 60 seconds if there is no action. When both the receiver and transmitter are done, data is checked, END PASS is typed, and program loops to $XLB depending on the switch settings.

9.4 The Return to Monitor Routine for END PASS at EOP: Locks out interrupts and saves the transmitter interrupt enable bit and all General registers. It then returns to the monitor to type "END PASS". The monitor checks SW14; if up, it returns to enter:, otherwise it restarts the program.

9.5 ENTER: is entered from the monitor after typing "END PASS", it restores the General registers and the transmitter CSR as saved in EOP. The delay flag is set and program returns to the scan routine (OWO, OWI, ILB, XLB) where it came from.

9.6 The Initialize Transmit Subroutine at STARTX: Sets up the interface and pointers necessary to initiate a transmit operation. After setting "DATA TERMINAL READY" and "REQUEST TO SEND", a check is made on param 2 to determine if half-duplex operation was selected by the operator. If it was, the subroutine waits for Clear to Send. A "WAITING FOR CLEAR TO SEND" printout occurs every 30 seconds until CLEAR TO SEND is asserted.

9.7 The Initialize Received Subroutine at STARTR: Sets up the interface and pointers necessary to receive a message.

9.8 The Transmit Interrupt Service Routine, at XISR:, is entered via transmit interrupts from the interface. A test is made to see if the last character transmitted was a NULL (all zeros) character. If it was, the Transmit Logic in the interface is reset and the transmit complete flag is set. At XISR1: the next character is transmitted and printed on the TTY if the monitor transmit switch is set.

9.9 The Receive Interrupt Service Routine, at RISR:, is entered via receiver interrupts from the interface. The received character is stored in the input buffer and printed on the TTY if the monitor receiver switch is set. If the input buffer is full, a "BUFFER FULL" printout will occur. This indicates that a line feed character was not recognized in the received data (within 1000 characters). If the received character is a line feed, the received logic is reset and the receive complete flag is set. If a "RECEIVE ERROR" is detected at RISR:, the CSR and DBR will be saved and printed out after the complete message has been received.

9.10 The Data Test Subroutine at TESTD: is entered after a complete message has been received. If a "RECEIVE ERROR" had been detected, the contents of the "RECEIVE BUFFER" at the time the error occurred will be printed. The data is compared until a "ALL ZEROS" character is recognized. "FILL" (all ones) characters are ignored. If a mismatch is detected, the complete contents of the input buffer and good data is printed.

10.0 PARAMETERS FOR THE DZ11

Param #1 is loaded into the Line Parameter register (DZLPR)

Bits 0–2	Line number being used. Default = Line 0
Bits 3, 4	Character Length, Default = eight bits
Bit 5	Stop Bit Count, Default is two stop bits
Bit 6, 7	Parity Enable and Select, Default is No Parity
Bits 8–11	Baud Rate Select, Default is 110 Baud
Bit 12	Receiver on (this should always be set)

Param #2 is not used at this point in time.

Param #3 is not used (177777).

DZ11 RESTRICTIONS

The RTS modem signal on the DZ11 is jumper selectable at the termination panel. It is either always asserted or asserted when Data Terminal Ready (DTR) is set. Consequently, at this point in time, DZ11 ITEP cannot be used with series 200 and other half-duplex modems. All ITEP modes are valid with full-duplex modems, and all modes may be used to terminals (only one way out and in are recommended here, however).

5.4 CORRECTIVE MAINTENANCE

The following paragraphs outline standard troubleshooting techniques to assist in determining whether the DZ11 module has a defective component or the malfunction is caused by external equipment. Prior to beginning DZ11 corrective maintenance procedures, ensure that all external equipment is functioning properly. Refer to the appropriate maintenance manuals and examine the DZ11 Maintenance Log to determine whether the fault is recurring and check previous repair techniques.

5.4.1 DZ11 Test Procedures

The following procedures will test the DZ11 and its various options. Prior to performing these procedures, it is recommended that the reader is thoroughly familiar with the operational theory of the PDP-11 Unibus and the DZ11. Maintenance of the DZ11 is accomplished by following this test procedure while using the DZ11 diagnostics. The test procedure may be divided into five general areas: Visual Inspection, Internal Loopback, Staggered Loopback, External, and On-Line with Terminal.

5.4.1.1 Visual Inspection – A visual check for solder shorts and damaged or missing components can save considerable checkout time.

5.4.1.2 Internal Loopback – The internal loopback is the simplest maintenance mode, and is run first in the test procedure. With bit 03 of the DZ11 CSR set, the output serial data from the UARTs are turned around into their respective serial data inputs. All lines are turned around simultaneously, but the output EIA converters (or 20-mA loop circuits) are excluded.

5.4.1.3 Staggered Loopback – The staggered loopback mode is used only with the DZ11-A, B, and E (EIA) options. This test mode uses the H327 test connector in the 50-pin PC socket housing that normally accepts the BC05W-15 cable. Bit 03 of the CSR must not be set. The lines are turned around in the following manner: Line 0 transmits data to Line 1 receiver, Line 1 transmits to Line 0 receiver, Line 0 DTR to Line 1 carrier and ring indicator, and Line 1 DTR to Line 0 carrier and ring indicator. The remaining lines are connected in the same manner, with Lines 2 and 3 paired, 4 and 5, and 6 and 7. This test mode allows testing of the output level converters in addition to the checking out of all UART parameters.

5.4.1.4 External – This maintenance mode runs the lines to the point where the customer or user connects, and requires an H315 or H325 loopback connector attached to the end of the BC05D cable that originates at the distribution panel. The test connector is placed at the customer end of the cable with the distribution panel end of the cable remaining connected.

5.4.1.5 On-Line with Terminal – In this test, a 20-mA or EIA terminal is connected to a single line on the distribution panel, and all lines are checked individually by means of an ECHO test that is a part of the DZ11 diagnostics.

5.4.2 DZ11 Option Testing

The following procedure checks all options of the DZ11, and differences in the procedure that apply to a specific option are noted:

a. Although the board has been GR tested, it is still a good idea to check for power shorts to ground and for shorts between different voltages. The power distribution from the module pins is shown on sheet #1 of the circuit schematics and below.

+5 V pin A2 section A, B, C, D, E and F
+15 V pin U1 section C
-15 V pin B2 section C
Gnd pin C2 and T1 section A, B, C, D, E and F.

b. Check the jumper labeled "W1" on the board. This should be in at all times. It is taken out only for GR testing.

c. Check to see that the priority 5 insert is plugged into socket E52 on the M7819 module or E41 on the M7814 module.

d. Set the address to 160000 (all switches off) and the vector to 300 (all switches on except switches for vector bits 6 and 7). If a second module exists (DZ11-E or DZ11-F) set its address to 160010 and vector to 310.

e. On an M7819 module, make sure that the H327 connector (it comes with the module) is inserted properly. The arrow on the connector should match the arrow on the 50 pin PC socket housing.

f. With all power off, insert the module -WITH CARE- into the SPC slot being used. Watch for wires on any H327 connector getting snagged and components near the module's edge getting caught in the card guides. Also, be sure the address and vector switch settings don't change while inserting the module.

g. Turn on power and load the DZ11 diagnostic (MAINDEC-DZDZA) into memory.

h. Load address 200 into the switch register and depress the load address key. Set swich register bit 0 to a one. Start the program and answer the following questions as they appear on the teletype:

"1st CSR ADDRESS (160000:163700):"

Type in the first's DZ11 address; 160000 (carriage return)

"1st VECTOR ADDRESS (300:770):"

Type in the first's DZ11 vector; 300 (carriage return)

"BR LEVEL (4:7):"

Type in priority level (all DZ11's) 5 (carriage return)

"TYPE 'A' FOR EIA MODULE OR 'B' FOR 20 mA (A:B):"

Type 'A' for DZ11-A, B and E (carriage return)
Type 'B' for DZ11-C, D and F (carriage return)

"MAINTENANCE MODE
EXTERNAL (H325) 'E'
INTERNAL (DZCSR03=1) 'I'
STAGGERED (H327) 'S' "

Type 'I' (carriage return)

"# OF DZ11s (IN OCTAL) - (1:20):"

Type 1 for DZ11-A, B, C or D (carriage return)
Type 2 for DZ11-E or F (carriage return)

i. The first pass of the program goes through each test once (approximately 1-1/2 minutes). Subsequent passes go through several iterations of each test in about 3 minutes (if no errors occur). Switch register switch 11 can be set to inhibit these iterations if so desired. Run at least one error-free pass without iterations.

NOTE

The diagnostic will run up to 16 DZ11 modules (must be all one type, EIA or 20 mA). It does this by running a complete pass on each one in sequence (the DZ11 CSR address is typed out with each pass complete). Therefore, if more than one module is being tested, an error-free pass must occur for each one. For example, if two modules are being tested then two passes of the program are required to check both modules.

j. If 20 mA module go to step "o" (DZ11-C, D, and F). Rerun each module under test for 2 passes without error, and with iterations. Do this by restarting at address 200 and answering "S" to question "MAINTENANCE MODE?" or load address 1512 for the 1st DZ11. 1526 for the 2nd DZ11, etc. and deposit 100000 (was 000000).

k. Halt program and power down system.

l. Remove the module and unplug the staggered turn-around connector (H327).

Connect the BC05W-15 cable to the 50 pin socket on the module and connect the other end to the H317E distribution panel; to J18 for the 1st DZ11 and J20 for a second DZ11.

NOTE

BC05W-15 cables used with the DZ11 have labels that say "This Side Up". If there are no labels, plug in the cable with rib side up at the module and with smooth side up at the distribution panel.

m. Turn power on.
Start at address 200 and answer "E" to question "MAINTENANCE MODE?" or load address 1512 for the 1st DZ11, 1526 for the 2nd DZ11, etc. and deposit 200. Run 2 passes without errors and with iterations.

n. Stop program and run the cable test in the following manner:

Load address 210.
Start with 213 in the switch register.
Answer the following questions on the teletype:

"VECTOR ADDRESS?" 300 carriage return
"CONTROL REGISTER ADDRESS?" 160000 carriage return
"WHICH TEST? ECHO OR CABLE (E OR C)" C carriage return
"BAUD RATE?" 9600 carriage return
"LINE?" 0 carriage return

The program will run the cable test and print out a "PASS DONE".
Run this test on lines 0 thru 7 without error.

NOTE: To change lines; hit any printing key on your console terminal while the program is running and type the new line number.

o. The ECHO test can be run on both EIA and 20 mA loop modules. Each line should be tested a single line at a time in the following manner:

For EIA disconnect the H315 or H325 from the BC05D-25 cable and use a BC03M or BC03P null modem cable between the BC05D and the EIA terminal. Connect the 20 mA loop cable directly from the terminal block on the panel to the terminal.

Load address 210.
Start with 213 in the switch register.
Answer the following questions on the teletype:

"VECTOR ADDRESS?" 300 carriage return
"CONTROL REGISTER ADDRESS?" 160000 carriage return
"WHICH TEST? ECHO OR CABLE (E OR C)" E carriage return
"BAUD RATE?" enter baud rate and carriage return (baud rate of terminal being used)
"LINE?" 0 carriage return
The program will print:

"TERMINAL ECHO TEST"
"THE QUICK BROWN FOX JUMPED OVER THE LAZY DOG'S BACK 0123456789"
"TYPE A CHAR: ON DZ11 TERMINAL"

The program now allows you to type characters. Type several characters and then hit control C and do the next line. This test should run without any errors.

NOTE: To change lines, hit any printable character on the teletype console. Change terminal to next line. Type in value of next line (i.e., the line number). Repeat this step until all lines are tested.

p. After running all of the above steps so that the diagnostic runs completely without error, run the module or modules in a heat chamber that cycles between 50° F and 130° F. Run the modules in Internal mode for two cycles as shown.

Any errors that develop must be corrected. Unit must run at least one cycle error free.

q. DZ11 is now ready for acceptance.

5.4.3 System Checkout Procedure

The DZ11 is a priority 5 device that has its addresses assigned to it from the floating address and floating vector space. It is ordered after the DMC11 in the floating address space and after the DMC11 in the floating vector space. Reference to Chapter 3 of this manual can be made for further details on DZ11 vector and address assignments.

The following lists itemize the hardware, software, and reference materials to be used during the subsequent procedure:

Required Hardware

DZ11-A, B or E
H327 test connector
H375 or H315 test connector
BC05W-15 cable
BC03P or BC03M null modem cable
EIA terminal (VT05, VT50, LA36, etc.)
PDP-11 system

DZ11-C, D or F

BC08S-15 cable
Cable to go from panel to 20 mA terminal
20 mA terminal (ASR 33, 35, LA36, etc.)

Required Software

MAINDEC-11-DZDZA

DEC/X11 System Exerciser Software

References

DZ11 manual

DZ11 Field Maintenance Print Set

a. Check the DZ11 modules for their proper address, vector and priority.

CAUTION

Insert and remove the DZ11 modules (M7819 or M7814) slowly and carefully to avoid snagging components in the card guides. Also, to prevent the vector and address switch settings from being changed by rubbing against an adjacent module.

b. If a DZ11-C, D or F go to step k or else insert or verify that the H327 test connector is in J1 of the module (arrows of connector and J1 should match).

c. Load the DZ11 diagnostic and run 2 passes in staggered mode without any errors. Reference the diagnostic listing in this manual.

d. When step "C" is complete, replace the H327 test connector with the BC05W-15 cable (rib side up or with label showing). Observe the same caution as above for removal and insertion of the module. Insert the other end of the cable into J18 or J20 on the H317E distribution panel (smooth side up or with label showing).

NOTE

The distribution panel can handle 16 lines. J18 distributes to the right 8 lines (i.e., J1 to J8 read from right to left). J20 distributes to the left 8 lines (J9 to J16).

e. Connect an H325 or H315 test connector to the first line and run in external mode for 2 error free passes. Do this for each line.

f. Repeat step e, but run the cable test for each line.

g. Remove the test connector and with a BC03P or BC03M, null modem cable, connect to an EIA terminal.

h. Run the echo test on each line one pass without error.

i. Run the DEC/X11 system exercisor (select several other devices too) for 15 minutes without error.

j. System checkout complete.

DZ11-C,D,F Procedure

k. Load the DZ11 diagnostic and run 2 passes in internal mode without error.

l. When step k is complete, connect the BC08S-15 cable from J1 on the module to J1 or J2 on the H317F distribution panel.

m. Connect a 20 mA terminal to line 0 and run the echo test one pass without error. Do this for each line.

n. Run the DEC/X11 system exercisor (select several other devices too) for 15 minutes without error.

o. System checkout complete.

5.4.4 Diagnostic Tests

The following table lists all the tests of the diagnostic and can be used for easy reference while troubleshooting. Also, a short toggle in program is included below to aid in debugging the transmitter and receiver sections.

Location	Instruction		Mnemonic
0	012737	START,	MOV #LINE, TCR
2	LINE #		
4	TCR Address		
6	012737		MOV #PAR, LPR
10	Parameters		
12	LPR Address		
14	012737		MOV #50, CSR
16	000050		
20	CSR Address		
22	005737	TEST1,	TST TRDY
24	CSR Address		
26	100375		BPL TEST1
30	013737		MOV (SWR), TBUF
32	177570		
34	TBUF Address		
36	000771	NOP,	BR TEST1
40	012701		MOV #DEL, R1
42	DELAY		
44	105737	TEST2,	TSTB CSR
46	CSR Address		
50	005201		INC R1
52	001374		BNE TEST2
54	013700		MOV RBUF, R0
56	RBUF Address		
60	000760		BR TEST1

NOTE

a. If the TRDY bit is failing to set, put the Branch Instruction in Location 36 (NOP).

b. If "TRDY" is not failing but "RDONE" fails to set; put a NOP instruction (000240) in location 36; put a constant into location 42 (Delay) – 177650 for a PDP-11/40. This allows recycling of the test about every 700 μs. Other processors might require a different constant.

c. In location 2 (Line #).Set the line bit that is failing (Bits 0–7 only).Only one bit should be set.

d. In location 10 (Par), put in line parameters; 01747X (X = line number) 1 is recommmended. This gives an 11-bit character (1 = start, 2 = stop, 8 data.)

MAINDEC-11-DZDZAA/<377>/EIGHT LINE ASYNC MUX TESTS

TEST 1

This test proves the slave sync response during a read or write to the following address:
DZCSR, DZRBUF, DZTCR, DZMSR

TEST 2

This test proves that bit "DCLR" can be set and that it will clear by itself after a period of time.

TEST 3

Test to verify that bit "MAINT" can be set. Then verify that bit "MAINT" can be cleared (written to a zero), and finally verify that after being set again, it can be cleared by a "DEVICE CLEAR".

TEST 4

Test to verify that bit "MSENAB" can be set. Then verify that bit "MSENAB" can be cleared (written to a zero), and finally verify that after being set again it can be cleared by a "DEVICE CLEAR".

TEST 5

Test to verify that bit "SILOEN" can be set, then verify that bit "SILOEN" can be cleared (written to a zero), and finally verify that after being set again it can be cleared by a "DEVICE CLEAR".

TEST 6

Test to verify that bit "RIE" can be set, then verify that bit "RIE' can be cleared (written to a zero), and finally verify that after being set again it can be cleared by a "DEVICE CLEAR".

TEST 7

Test to verify that bit "TIE" can be set, then verify that bit "TIE" can be cleared (written to a zero), and finally verify that after being set again it can be cleared by a "DEVICE CLEAR".

TEST 10

This tests that all of the following bits can be: Set, Cleared, Cleared By "DEVICE CLEAR".
Bits tested are:

TCR0, TCR1, TCR2, TCR3, TCR4, TCR5, TCR6, TCR7

TEST 11

This tests that all of the following bits can be: Set, Cleared, Cleared By "RESET INSTR * NOT * DEVICE CLEAR". Bits tested are:
DTR0, DTR1, DTR2, DTR3, DTR4, DTR5, DTR6, DTR7
This test is not done if module is 20 mA version.

TEST 12

This test performs reset testing and testing of write only or read only bit.
Test bits "RDONE, BIT11, BIT10, BIT9, BIT8, BIT2, BIT1, BIT0, SILOAL" are read only and that TRDY is zero until a line is selected and MSENAB is set.

TEST 13

This test performs reset testing and testing of read only and write only bits in register DZCSR. Verify that "TIE", "SILOEN", "RIE", "MSENAB", "MAINT" are the only R/W bits in the DZCSR, then set "DCLR" and verify they are cleared.

TEST 14

This test performs reset testing and testing of read only register DZRBUF and testing of write only register DZLPR.

TEST 15

This test performs reset testing and testing of read only register DZMSR and testing of write only register DZTDR.

TEST 16

Verify that if we are in "STAGGERED" mode that setting "DTR" for a line will bring up "RING" and "CARRIER" for the associated line in which we are staggered!

LINE0 DTR=LINE1 RING AND CARRIER
LINE1 DTR=LINE0 RING AND CARRIER
LINE2 DTR=LINE3 RING AND CARRIER
LINE3 DTR=LINE4 RING AND CARRIER
ETC...

TEST 17

Test to verify that if in "EXTERNAL" mode; setting DTR for selected lines will bring up "CARRIER" and "RING" for that same line.
NOTE: If you have selected mode as "EXTERNAL"; the H325 test connector must be used on all specified lines, lines may be specified by SWR03=1 and SWR00=1 at start time or altering status map.

TEST 20

This test verifies that TRDY is set when a line is ready to be loaded, and that the line specified in bits 8–10 of DZCSR correspond to the line selected in DZTCR.

TEST 21

Test to transmit one char and receive one char on one line at a time. The char is "252" and all selected lines will be turned on one at a time. This is the first time any data is checked in the receiver.

TEST 22

This test proves that the transmitter transmits characters (FLAG MODE) and the receiver receives (FLAG MODE) (one line at a time, based upon valid lines). This is the first time that all data is checked.

TEST 23

This test will prove that:
(1) The transmitter "BREAK BIT" works.
(2) The receiver can flag "FRAMING ERRORS".
(3) The receiver can flag "PARITY ERRORS"
Only one line at a time will be exercised. This test will not be exercised unless connected by external plug.

TEST 24

This test verifies that the device does not interrupt while the processor status is set exactly to what the DZ11 priority is set to.
Default priority is at level 5 (240).

TEST 25

This test verifies that the device does interrupt while the processor status is set to exactly one level lower than the DZ11. DZ11 priority default to level 5 minus one level is level 4.

TEST 26

This test verifies that the receiver will interrupt before the transmitter even though the transmitter was enabled first. Set PS to level 7; get RDONE and TRDY to set; Set TX IE and RX IE; clear PS and expect RX to interrupt first.

TEST 27

This test verifies overrun and silo alarm one line at a time – based upon valid lines as each of the first 16 chars are sent; silo alarm is tested to be cleared, on the 16th char the program then expects silo alarm to set. Then the entire silo is filled and an overrun is expected on the 65th char pulled out of the silo.

TEST 30

This test that "SILO ENABLE" will inhibit receiver interrupts and that on the 16th char that "SILO ALARM" will cause an interrupt with "RIE" set.
This will do all selected lines one at a time.

TEST 31

This test runs all lines full bore based upon qualified lines
. .This is an interrupt test on the receiver and transmitter.

TEST 32

DZ11 Relative Timing Test.
Each selected line will in turn run 16. Chars at all baud rates and then the highest baud with all char lengths. Each new parameter should decrease in time from the previous parameters selected. The time is checked against the last parameter used and a lower time is expected on the current parameter.
Parameters are:

Eight Bits/per/char – Two stop bits at 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 baud, 19.2K baud – Two stop bits at seven, six, five bits/per/char.

After each line has finished all the above parameters the next selected line is the tested.

TEST 33

This test verifies that even parity works for all odd lines selected and that odd parity works for all even lines selected.
The main function of this test is to verify that "PE" (parity error) can be flagged by the UARTs. This test will not be done unless you are in "staggered" mode.
40(8) chars are used for this test.
All selected lines will be enabled at the same time!

TEST 34

This test verifies that odd parity works for all odd lines selected and that even parity works for all even lines selected. The main function of this test is to verify that "PE" (parity error) can be flagged by the UARTs. This test will not be done unless you are in "STAGGERED" mode.
40(8) chars are used for this test.
All selected lines will be enabled at the same time!

APPENDIX A
INTEGRATED CIRCUITS

3341	4-Bit × Word Propagatable Register
5016	Baud Rate Generator
74LS74	Dual Flip-Flop
74LS90	4-Bit Decade Counter
8136	6-Bit Unified Bus Comparator
8641	Quad Unified Bus Transceiver
8647	Unibus Chip
9318	Priority Encoder
9602	Multivibrator Flip-Flop
74LS138	Decoder Multiplexer
74LS151	8 to 1 Multiplexer
74LS153	Dual 4 to 1 Multiplexer
74LS155	2 to 4 Line Decoder
74LS157	Quad 2 to 1 Multiplexer
74LS175	Quad Storage Register
74LS193	4-Bit Up/Down Counter
74LS259	8-Bit Address

APPENDIX B
GLOSSARY OF TERMS

BRK BREAK. Bits 0 through 7 correspond to lines 0 through 7. When a bit is set, the serial output line is held in the spacing condition. These bits are write only from the Unibus as part of the TDR or Transmit Data Register (device word #6, upper byte).

CLK CLOCK is used by the scanner to generate the scan phases and to synchronize the loading of the "UART" transmit buffer with the scan cycle. It is approximately 1 MHz with a 40% on, 60% off duty cycle. It is derived by dividing the 5.0668 MHz crystal oscillator output by 5.

CLR CLEAR is bit 4 of the Control and status register. When set, it generates a 15 microsecond reset pulse that clears everything including itself. The one exception is the DTR Byte. This eight bit register is cleared by "BUS INIT" or by program control.

CS CONTROL STROBE clocks in the various line parameter information to the UARTS. There is one for each UART line.

CSR CONTROL and STATUS REGISTER of the device. It is device word 0.

CO CARRIER is a modem signal indicating that a channel (line) is established and ready to send data. The device monitors the state of this line for all eight channels. These states can be read to the Unibus by reading device word #6 (Modem Status Register), the upper 8 bits or the high byte containing the state of the "CO" lines.

DA DATA AVAILABLE is a "UART" signal indicating that it has a character ready. The DA lines are bussed together as the UARTS are sampled one at a time.

DV DATA VALID is read as bit 15 of the silo output and indicates the character is valid.

DS DATA STROBE clocks the contents of the transmit buffer into the UARTS transmit buffer. There is a DS pulse for each UART line.

DTR DATA TERMINAL READY is a signal sent to the modem indicating a ready condition to send or receive data. There is a DTR line for each channel and it is controlled from the Unibus by addressing the upper byte of the Transmit Control Register (device word #4). These read/write bits are cleared by Bus Init or by program control only [i.e., CSR bit 4 (CLR) does not reset these bits].

FE (FER) Uart status bit indicating a FRAMING ERROR when set.

TRDY TRDY indicates that a transmitter line is enabled and its transmit buffer is empty. This signal has to be true for a transmit interrupt to occur.

INH SSYN — This level is generated when loading the line parameters of the Uarts (CS Pulse) from the Unibus. This level prevents the Address Selection Logic from returning "SSYN" until the Uart has had time to sample the received data bus lines.

INIT — The received "Bus Init Signal" is used to clear the "DTR" register and generates a reset to initialize the rest of the logic.

IR — IN READY, when true, indicates that the silo has room for and is able to accept another word.

INTR — INTERRUPT initiates the processor interrupt and gates the vector onto the Unibus data lines.

LD CSR — LOAD CSR

LD HCSR — LOAD HIGH byte of CSR

LD HTCR — LOAD HIGH byte of TCR

LD HTDR — LOAD HIGH byte of TDR

LD LCSR — LOAD LOW byte of CSR

LD LPR — LOAD LINE PARAMETERS

LD LTCR — LOAD LOW byte of TCR

LD LTDR — LOAD LOW byte of TDR

LD TBUF — LOAD TRANSMIT BUFFER

LD TCR — LOAD TCR

LD TDR — LOAD TDR

LINE — There are eight "line" bits, one for each channel. They are accessed from the Unibus via the lower byte of the TCR (Transmit Control Register – word #4). When set, it allows a line with its transmit buffer empty to cause a transmit interrupt (if TIE is set).

MSCAN EN — MASTER SCAN ENABLE. Bit 5 of the CSR. This bit turns on the scanner when set.

OR (OVR) — Uart status bit indicating an overrun condition, i.e., another character was received before the last one was taken from the buffer.

PE (PER) — Uart status bit indicating a PARITY ERROR.

RA1 — RECEIVED ADDRESS BIT 1

RA2 — RECEIVED ADDRESS BIT 2

RC1 — RECEIVED C1 BIT

RD <15:00> RECEIVED BUS DATA BITS

RDA RESET DATA AVAILABLE. A level used to reset the "DA" bit on the Uart that was currently sampled.

RD RBUF READ RECEIVER BUFFER, the output of the silo, to the Unibus and arm logic for next receiver interrupt.

RESET A master clearing pulse 15 microseconds long that is generated by "BUS INIT" and/or CSR bit 4 being set (clear).

RI RING INDICATOR from modem. Each channel is monitored and can be accessed by reading the TDR register. The lower byte of this register has a corresponding bit for each ring line (device monitor).

RDONE RECEIVER DONE. This read only bit of the CSR register is set when a character is loaded into the silo. It is bit 7 of the CSR (device word #0).

RIE RECEIVER INTERRUPT ENABLE. Read/write bit 6 of the CSR. When set, it enables a receiver interrupt to occur.

SA SILO ALARM. This flag is true after 16 characters have entered the silo if SAE is true.

SAE SILO ALARM ENABLE. The flag enables the silo alarm flag.

SAM SAMPLE. A sample level is generated for each line by the receiver scanner.

SCAN A, B, C Three-bit output indicating the line number being currently scanned.

SDO SERIAL DATA OUT of the Uart.

SEL SELECT. This level is true when the device recognizes its base address.

SHI SHIFT INTO silo.

SI Serial data into Uart.

SILO 64 × 16 first in, first out buffer.

SO SHIFT OUT of silo.

TBUF TRANSMIT BUFFER. An 8 bit register that holds the character to be transmitted by the Uart.

TBMT The Uarts transmit buffer is empty (TRDY) when this level is true.

TCR TRANSMIT CONTROL REGISTER (device word #4).

TD <15:00> DATA TO BE TRANSMITTED OVER THE UNIBUS DATA LINES.

TDR TRANSMIT DATA REGISTER (device word #6).

TI TRANSMIT INTERRUPT. True when TIE - LINE - TRDY are true (CSR bit 15). Is read only.

TIE TRANSMIT INTERRUPT ENABLE. (CSR bit 14). Is read/write.

TRDY Uart's transmit buffer is empty. This level is ANDed with LINE and if TIE is set will cause a transmit interrupt.

TLINE A, B, C The line number whose Uart has its transmit buffer empty and caused the interrupt. A 3 bit read out in CSR bit 8 through 10.

UART UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER.

5,0668 MHz The output of the crystal oscillator.

APPENDIX C
UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

C.1 INTRODUCTION

This appendix provides a functional description of the UART. It includes a table of UART signal functions and simplified block diagrams and timing diagrams of the UART receiver and transmitter.

C.2 UART FUNCTIONAL DESCRIPTION

The UART is a MOS/LSI device packaged in a 40-pin DIP. It is a complete subsystem that transmits and receives asynchronous data in duplex or half duplex operation. The receiver and transmitter can operate simultaneously. The transmitter accepts parallel binary characters and converts them to a serial asynchronous output.

The receiver accepts serial asynchronous binary characters and converts them to a parallel output. The receiver and transmitter clocks are separate and must be 16 times the desired Baud rate. The allowable clock rate is DC to 160 kHz.

Control bits are provided to select: character length of 5, 6, 7, or 8 bits, (excluding parity) mode, odd or even parity, and one or two stop bits for 6, 7, or 8-bit characters. For 5-bit characters, 1 or 1-1/2 start bits are used. The format of a typical input/output serial word is shown in Figure C-1.

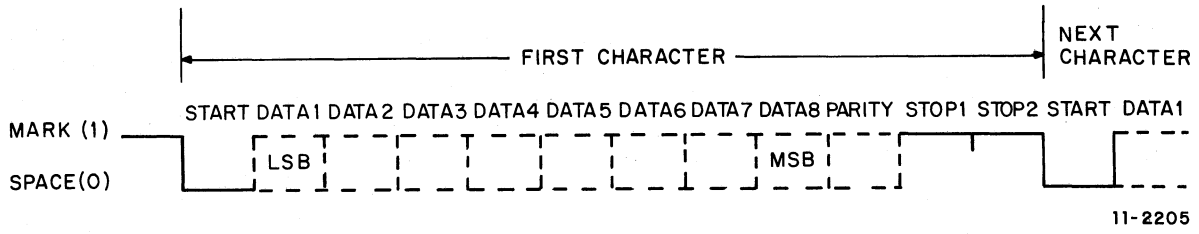


Figure C-1 Format of Typical Input/Output Serial Character

Both the receiver and transmitter have double character buffering so that at least one complete character is always available. A register is also provided to store control information.

A block diagram and simplified timing diagram for the UART transmitter are shown in Figure C-2. The transmitter data buffer (holding) register can be loaded with a character when the TBMT (Transmitter Buffer Empty) line goes high. Loading is accomplished by generating a short negative pulse on the DS (Data Strobe) line. The positive-going trailing edge of the DS pulse performs the load operation. The character is automatically transferred to the UART transmitter Shift Register when this register becomes empty. The desired start, stop and parity bits are added to the data and transmission-begins. One sixteenth of a bit time before a complete character (included stop bits) has been transmitted, the EOC (End of Character) line goes high and remains in this state until transmission of a new character begins.

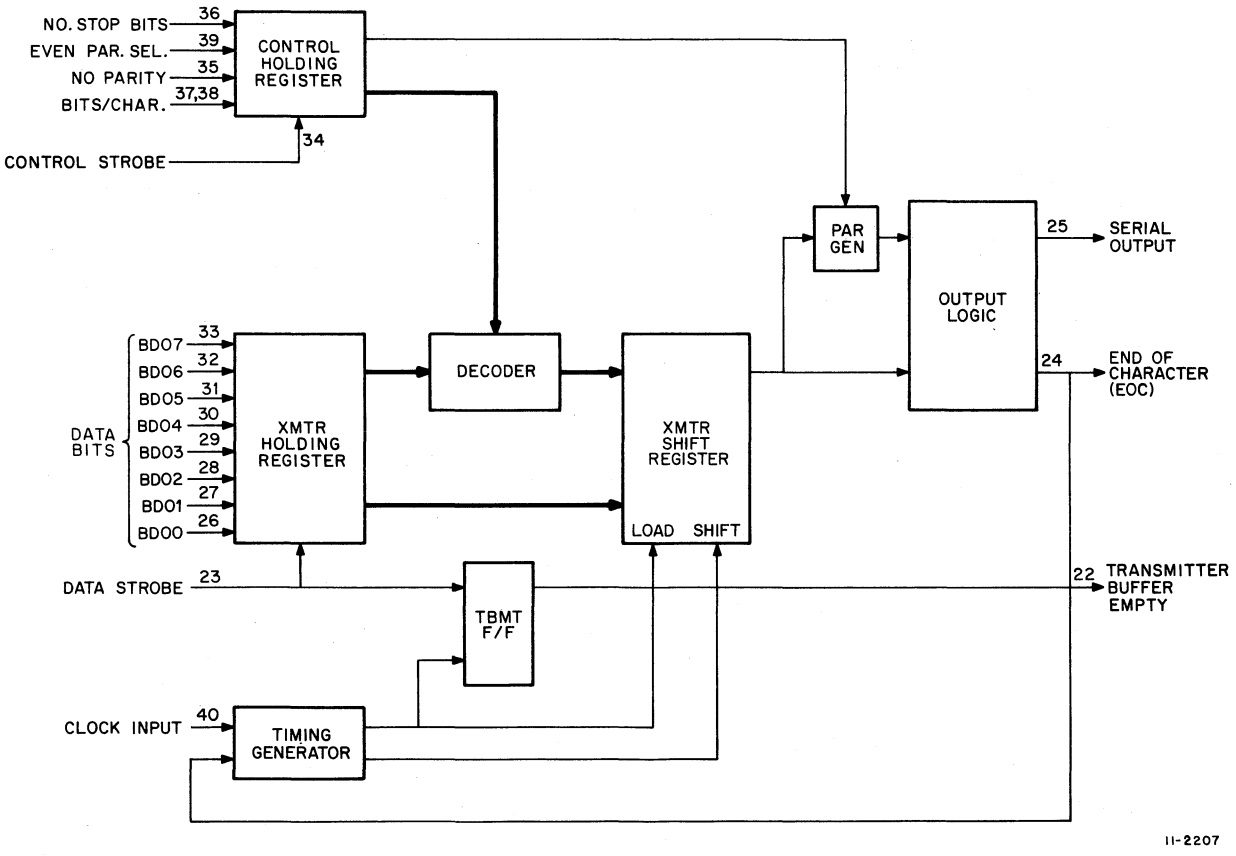


Figure C-2 UART Transmitter, Block Diagram and Simplified Timing Diagram

A block diagram and simplified timing diagram for the UART receiver are shown in Figure C-3. Serial asynchronous data is sent to the SI (Serial Input) line. The UART searches for a high to low (mark to space) transition on the SI line. If this transition is detected, the receiver looks for the center of the start bit as the first sampling point. If this point is low (space), the signal is assumed to be a valid start bit and sampling continues at the center of the subsequent data and stop bits. The character is assembled bit by bit in the receiver Shift Register in accordance with the control signals that determine the number of data bits and stop bits and the type of parity, if selected. If parity is selected and does not check, the PER (Receive Parity Error) line goes high. If the first stop bit is low, the FER (Framing Error) line goes high. After the stop bit is sampled, the receiver transfers in parallel the contents of the receiver Shift Register into the receiver data buffer (holding) register. The receiver then sets the DA (Received Data Available) line and transfers the state of the framing error and parity error to the Status Holding Register. When the DZ11 accepts the receiver output, it drives the RDA (Reset Data Available) line low which clears the DA line. If this line is not reset before a new character is transferred to the receiver Holding Register, the OR (Overrun) line goes high and is held there until the next character is loaded into the receiver Holding Register.

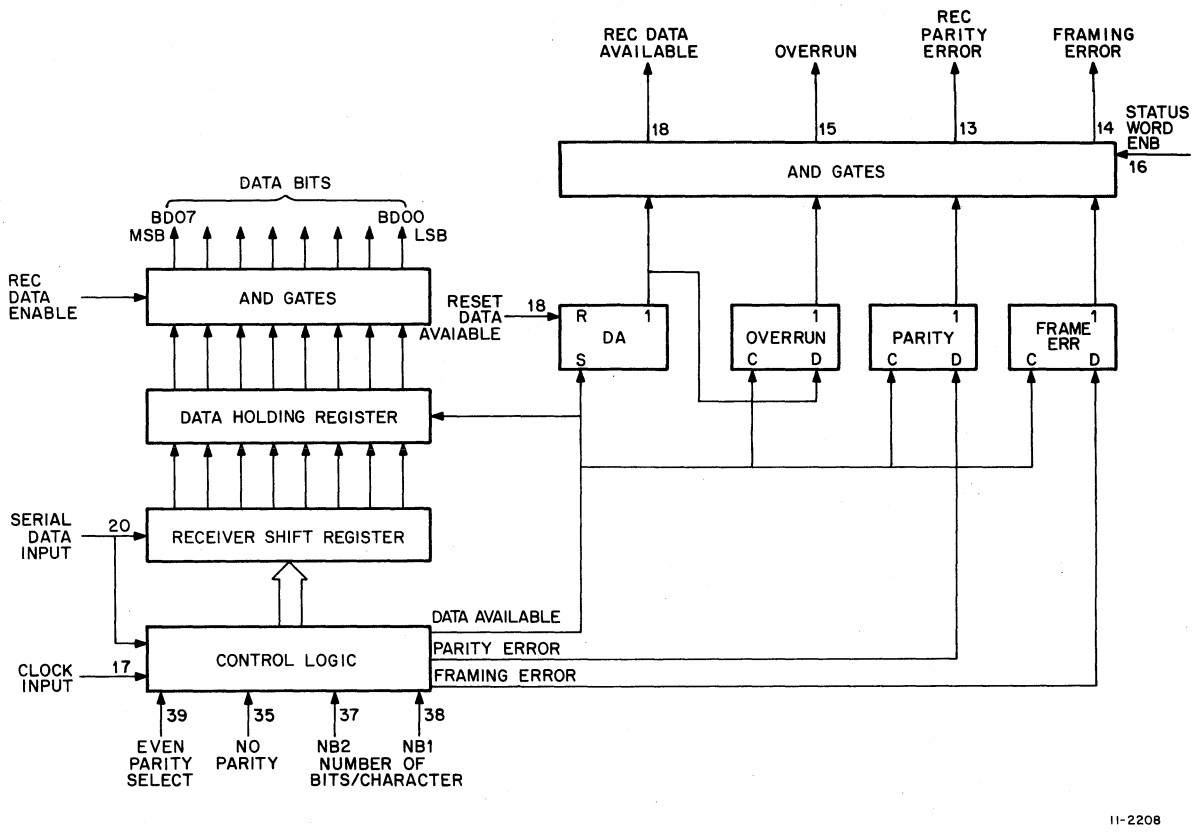


Figure C-3 UART Receiver, Block Diagram and Simplified Timing Diagram

Figure C-4 is a pin/signal designation diagram for the UART. The function of each signal is given in Table C-1. In the Function column, the references to high and low signals are with respect to the pins on the UART. This information is used during servicing of the device. Programmers should refer to the DZ11 register descriptions (Chapter 3) for information concerning the function of these signals.

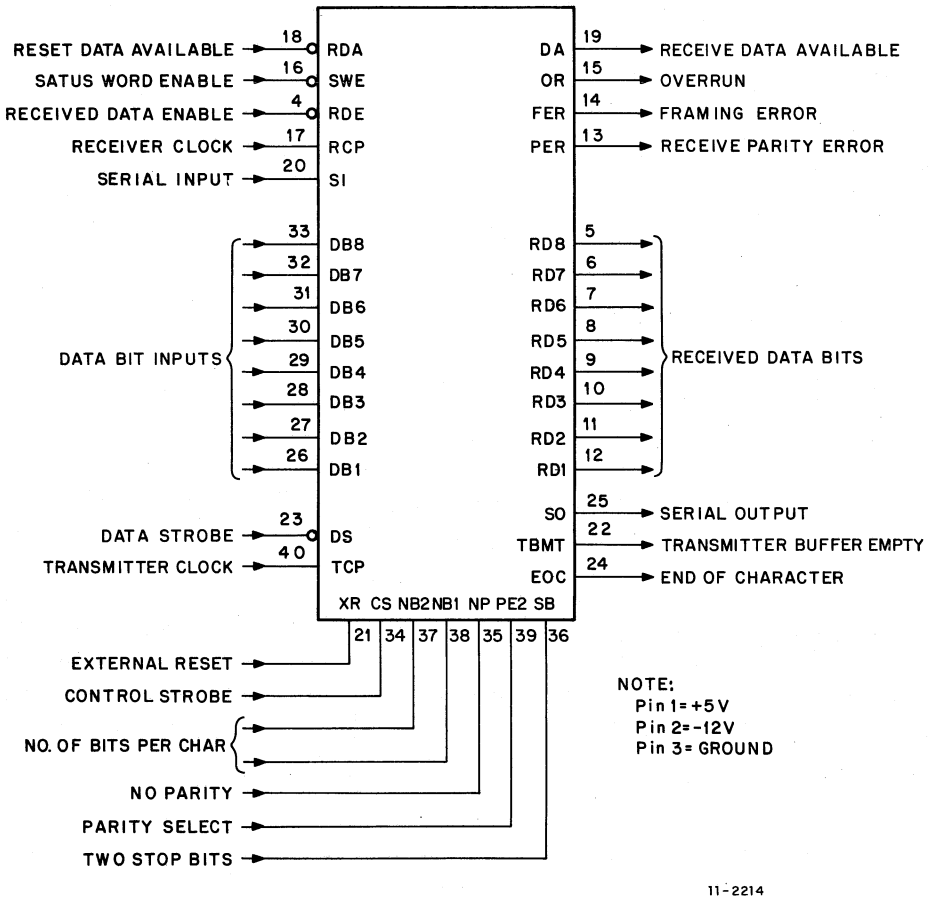


Figure C-4 UART Signal/Pin Designations

Table C-1 UART Signal Functions

Pin No.	Mnemonic	Name	Function
5-12	RD1-RD8	Received Data	Eight data out lines that can be wire ORed. RD8 (pin 5) is the MSB and RD1 (pin 12) is the LSB. When 5, 6, or 7 bit character is selected, the most significant unused bits are low. Character is right justified into the least significant bits.
13	PER	Receive Parity Error	Goes high if the received character parity does not agree with the selected parity.
14	FER	Framing Error	Goes high if the received character has no valid stop bit.
15	OR	Overrun	Goes high if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver Holding Register.
16	SWE	Status Word Enable	When low, places the status word bits (PE, OR, TBMT, FE, and DA) on the output lines.
17	RCP	Receiver Clock	Input for an external clock whose frequency must be 16 times the desired receiver Baud rate.
18	RDA	Reset Data Available	When low, resets the received DA (Data Available) line.
19	DA	Received Data Available	Goes high when an entire character has been received and transferred to the receiver Holding Register.
20	SI	Serial Input	Input for serial asynchronous data.
21	XR	External Reset	After power is turned on, this line should be pulsed high which resets all registers, sets serial output line high, sets end of character line high, and sets transmitter buffer empty line high.
22	TBMT	Transmitter Buffer Empty	Goes high when the transmitter Data Holding Register may be loaded with another character.
23	DS	Data Strobe	Pulsed low to load the data bits into the transmitter Data Holding Register during the positive-going trailing edge of the pulse.
24	EOC	End of Character	Goes high each time a full character, including stop bits, is transmitted. It remains high until transmission of the next character starts. This is defined as the mark (high) to space (low) transition of the start bit. This line remains high when no data is being transmitted. When full speed transmission occurs, this lead goes high for 1/16 bit time at the end of each character.

Table C-1 UART Signal Functions (Cont)

Pin No.	Mnemonic	Name	Function
25	SO	Serial Output	Output for transmitted character in serial asynchronous format. A mark is high and a space is low. Remains high when no data is being transmitted.
26-33	DB1-DB8	Data Input	Eight parallel Data In lines. DB8 (pin 33) is the MSB and DB1 (pin 26) is the LSB. If 5, 6, or 7 bit characters are selected, the least significant bits are used.
34	CS	Control Strobe	When high, places the control bits (POE, NP, SB, NB1 and NB2) into the control bits Holding Register.
35	NP	No Parity	When high, eliminates the parity bit from the transmitted and received character and drives the received parity error (PER) line low. As a result, the receiver does not check parity on reception and during transmission the stop bits immediately follow the last data bit.
36	2 SB	Two Stop Bits	Selects the number of stop bits that immediately follow the parity bit. A low inserts 1 stop bit and a high inserts 2 stop bits.
37,38	NB2, NB1	Number of Bits per Character (Excluding Parity)	Select 5, 6, 7, or 8 data bits per character as follows. **Bits/ Char** / **NB2 (37)** / **NB1 (38)** 5 / L / L 6 / L / H 7 / H / L 8 / H / H
39	POE	Even Parity Select	Selects the type of parity to be added during transmission and checked during reception. A low selects odd parity and a high selects even parity.
40	TCP	Transmitter Clock	Input for an external clock whose frequency must be 16 times the desire transmitter Baud rate.

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