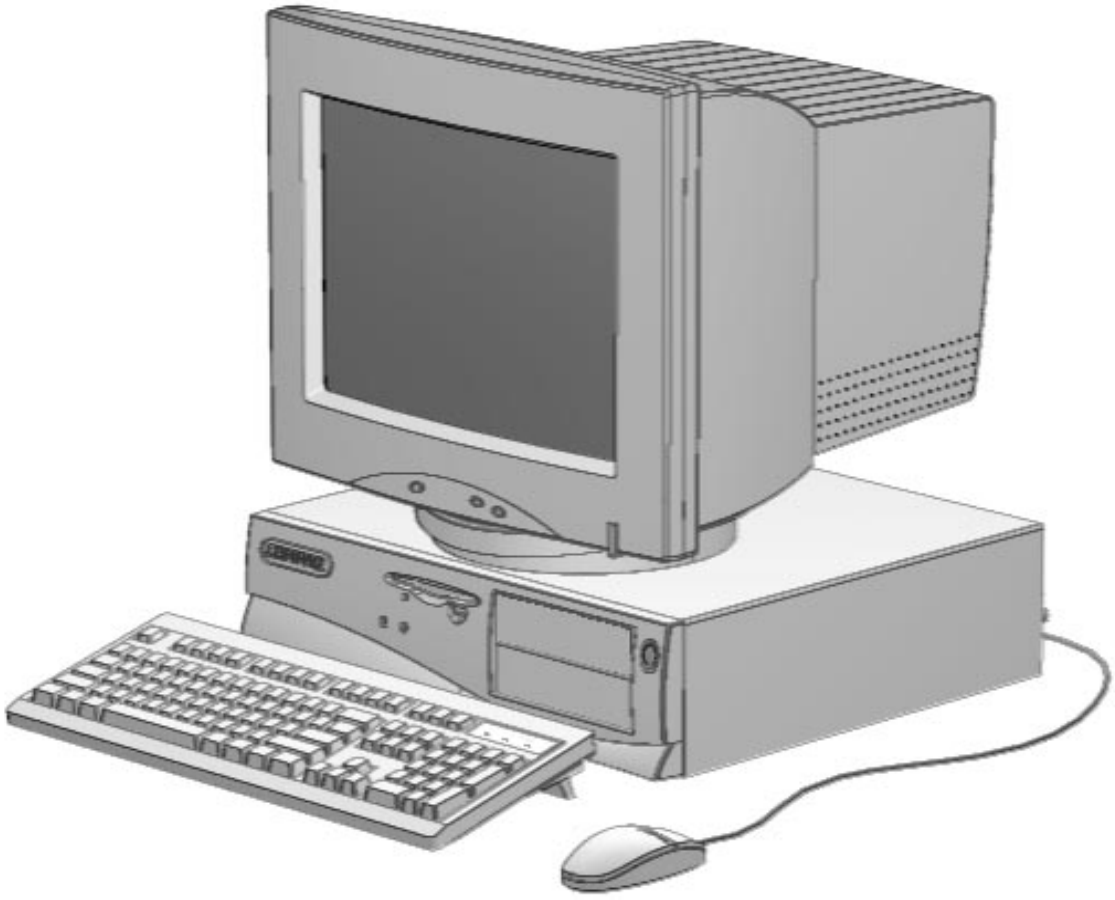
COMPAQ

Deskpro 2000 Personal Computers

Technical Reference Guide



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COMPAQ Deskpro 2000 Personal Computers ***TRG***

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Compaq Deskpro 2000 Personal Computers Technical Reference Guide
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Chapter 1
INTRODUCTION

1.1 ABOUT THIS GUIDE

This guide provides technical information about the Compaq Deskpro 2000 Series of Personal Computers. This document includes information regarding system design, function, and features that can be used by programmers, engineers, technicians, and system administrators.

1.1.1 USING THIS GUIDE

This guide consists of chapters and appendices. The chapters primarily describe the hardware and firmware elements contained within the chassis. The appendices contain general information in tabular format and describe standard peripheral devices such as the keyboard.

1.1.2 ADDITIONAL INFORMATION SOURCES

This guide does not describe in detail other manufacturer's components used in the product covered by this manual. For more information on individual commercial-off-the-shelf (COTS) components refer to the indicated manufacturers' documentation. The product covered by this guide uses architecture based on industry-standard specifications. For a detailed description on industry-standard designs and architecture referred to in this guide refer to the following publications:

- The Lotus/Intel/Microsoft Expanded Memory Specification, Ver. 4.0
- PCI Local Bus Specification Revision 2.1
- Extended Industry Standard Architecture Expansion Bus Technical Reference Guide, p/n 130584, Second Edition, Compaq Computer Corporation
- Compaq Basic Input/Out System (BIOS) Technical Reference Guide
  Doc.# 074A/0693, Fourth Edition, Compaq Computer Corporation

1.2 NOTATIONAL CONVENTIONS

1.2.1 VALUES

Hexadecimal values are indicated by the letter “h” following an alpha-numerical value. Binary values are indicated by the letter “b” following a value of ones and zeros. Memory addresses expressed as “SSSS:OOOO” (SSSS = 16-bit segment, OOOO = 16-bit offset) can be assumed as a hexadecimal value. Values that have no succeeding letter can be assumed to be decimal.

1.2.2 RANGES

Ranges or limits for a parameter are shown as a pair of values separated by two dots:

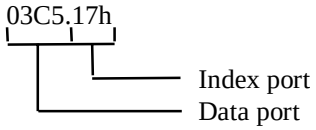
Example: Bits <7..4> = bits 7, 6, 5, and 4.

1.2.3 SIGNAL LABELS

Signal names are indicated using abbreviations, acronyms, or, if possible, the full signal name in all capital letters. Signals that are meant to be active low are indicated with a dash immediately following the name.

1.2.4 REGISTER NOTATION AND USAGE

This guide uses standard Intel naming conventions in discussing microprocessor (CPU) registers. Registers that are accessed using an indexing scheme are indicated using the following format:



In the example above, register 03C5.17h is accessed by writing the index port value 17h to the index address (03C4h), followed by a write to or a read from port 03C5h.

1.2.5 BIT NOTATION

Bit values are labeled with bit <0> representing the least-significant bit (LSb) and bit <7> representing the most-significant bit (MSb) of a byte. Bytes, words, double words, and quad words are typically shown with most-significant portions on the left or top and the least-significant portions on the right or bottom respectively.

1.3 COMMON ACRONYMS AND ABBREVIATIONS

Table 1-1 lists the acronyms and abbreviations used in this guide.

Table 1-1.
Acronyms and Abbreviations

Acronym/Abbreviation	Description
A	ampere
AC	alternating current
ACE	asynchronous communications element
ACK	acknowledge
A/D	analog-to-digital
API	application programming interface
APM	advanced power management
ASIC	application-specific integrated circuit
AT	1. attention (commands) 2. 286-based PC architecture
ATA	AT attachment (mode)
AVI	audio-video interleaved
AVGA	Advanced VGA
BCD	binary-coded decimal
BIOS	basic input/output system
bis	second/new revision
bpi	bits per inch
bps or b/s	bits per second
BitBLT	bit block transfer
CAS	column address strobe
CD	compact disk
CD-ROM	compact disk read-only memory
CDS	compct disk system
CEMM	Compaq expanded memory manager
CF	carry flag
CGA	color graphics adapter
Ch	channel
CLUT	color look-up table (pallete)
cm	centimeter
CMC	cache/memory controller
CMOS	complimentary metal-oxide semiconductor (configuration memory)
Cntlr	controller
codec	compressor/decompressor
CPQ	Compaq
CPU	central processing unit
CRT	cathode ray tube
CSM	Compaq system management / Compaq server management
CTFT	color TFT
DAA	direct access arrangement
DAC	digital-to-analog converter
db	decibel
dbm	decibel referenced to one milliwatt
DC	direct current
DCE	data communications equipment
DDC	Display Data Channel
DF	direction flag
DIN	Deutche IndustriNorm (connector standard)
DIP	dual inline package
DMA	direct memory access
dpi	dots per inch
DRAM	dynamic random access memory
DRQ	data request
DOS	disk operating system
DSP	digital signal processor
DSTN	dual-scan STN

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
DTE	data terminal equipment
DTMF	dual-tone multi-frequency
ECC	error correction code
ECP	extended capabilities port
EDID	extended display identification data
EDO	extended data out (RAM type)
EEPROM	electrically eraseable PROM
EGA	enhanced graphics adapter
EIA	Electronic Industry Association
EISA	extended ISA
EPP	enhanced parallel port
EIDE	enhanced IDE
ExCA	Exchangeable Card Architecture
FIFO	first in / first out
FL	flag (register)
FM	frequency modulation
FPM	fast page mode (RAM type)
FPU	Floating point unit (numeric or math coprocessor)
ft	foot
GB	gigabyte
GND	ground
GPIO	general purpose I/O
GUI	graphics user interface
h	hexadecimal
HW	hardware
hex	hexadecimal
Hz	hertz
IDE	integrated drive element
IEEE	Institute of Electrical and Electronic Engineers
IF	interrupt flag
I/F	interface
in	inch
INT	interrupt
I/O	input/output
IrDA	InfraRed Data Association
IRQ	interrupt request
ISA	industry standard architecture
Kb / KB	kilobits / kilobytes (x 1024 bits / x 1024 bytes)
Kb/s	kilobits per second
kg	kilogram
KHz	kilohertz
kv	kilovolt
lb	pound
LCD	liquid crystal display
LED	light-emitting diode
LIF	low insertion force
Li-ion	lithium-ion
LPB	local peripheral bus
LSI	large scale integration
LSb / LSB	least significant bit / least significant byte
m	meter
mA	milliampere
Mb / MB	megabit / megabyte (1×2^{20} for memory, 1×10^{6} for mass storage)
MDA	monochrome display adapter

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
MIDI	musical instrument digital interface
ML	multiplexed local bus
MPEG	Motion Picture Experts Group
ms	millisecond
MSb / MSB	most significant bit / most significant byte
mux	multiplex
MVA	motion video acceleration
MVW	motion video window
n	variable parameter/value
NiCad	nickel cadmium
NiMH	nickel-metal hydride
NMI	non-maskable interrupt
ns	nanosecond
NT	nested task flag
NTSC	National Television Standards Committee
NVRAM	non-volatile random access memory
OS	operating system
PAL	1. programmable array logic 2. phase altering line
PC	personal computer
PCI	peripheral component interconnect
PCM	pulse code modulation
PCMCIA	Personal Computer Memory Card International Association
PF	parity flag
PIN	personal identification number
POST	power-on self test
PROM	programmable read-only memory
PTR	pointer
RAM	random access memory
RAS	row address strobe
rcvr	receiver
RF	resume flag
RGB	red/green/blue
RH	Relative humidity
RMS	root mean square
ROM	read-only memory
RPM	revolutions per minute
RTC	real time clock
R/W	read/write
SCSI	small computer system interface
SECAM	sequential colour avec memoire (sequential color with memory)
SF	sign flag
SIMM	single in-line memory module
SIT	system information table
SMI	system management interrupt
SMM	system management mode
SMRAM	system management RAM
SPP	standard parallel port
SRAM	static RAM
STN	super twist pneumatic
SVGA	super VGA
SW	software
TAD	telephone answering device

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
TAM	telephone answering machine
TCP	tape carrier package
TF	trap flag
TFT	thin-film transistor
TIA	Telecommunications Information Administration
TPE	twisted pair ethernet
TPI	track per inch
TTl	transistor-transistor logic
TV	television
TX	transmit
UART	universal asynchronous receiver/transmitter
us	microsecond
USB	Universal Serial Bus
V	volt
VESA	Video Electronic Standards Association
VGA	video graphics adapter
vib	vibrato
VLSI	very large scale integration
VRAM	Video RAM
W	watt
WRAM	Windows RAM
ZF	zero flag
ZIF	zero insertion force (socket)

Chapter 2
SYSTEM OVERVIEW

2.1 INTRODUCTION

The Compaq Deskpro 2000 Personal Computers (Figure 2-1) include minitower and desktop models designed with an emphasis on speed, storage capacity, and multimedia compatibility to meet the requirements of the business environment. The Deskpro 2000 features architectures based on Pentium and Pentium Pro microprocessors incorporating the PCI and ISA busses. All models are easily upgradeable and expandable to keep pace with the needs of the office or home.

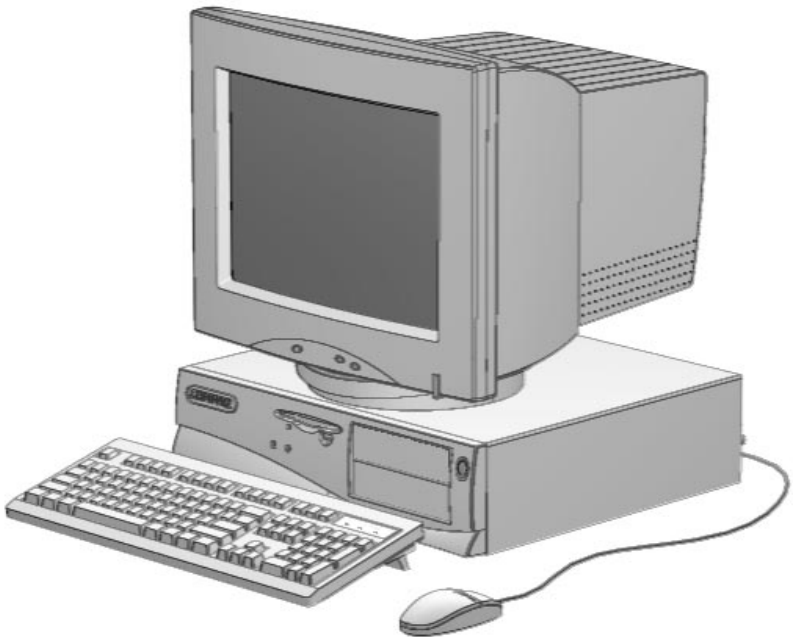


Figure 2–1. Compaq Deskpro 2000 Desktop Personal Computer with Monitor

2.2 FEATURES

This section describes the standard and distinguishing features.

2.2.1 STANDARD FEATURES

The following standard features are included on all models:

- Pentium or Pentium Pro microprocessor
- Support for 256-KB second-level cache
- 3.5 inch, 1.44-MB diskette drive
- Extended IDE controller support for up to four IDE drives
- Hard drive fault prediction
- Serial interface
- Parallel interface
- Universal serial bus (not supported on early version Pentium-based systems)
- Three PCI connectors
- Three ISA connectors
- Compaq Space Saver keyboard w/Windows support
- Compaq PS/2-type mouse
- APM 1.2 power management support
- Plug ’n Play compatible (with ESCD support)
- Client management support (Intelligent Manageability)
- Security features including:
    - Flash ROM write-protect
    - Diskette drive disable, boot disable, write protect
    - Power-on password
    - Administrator password
    - QuickLock/QuickBlank
    - Serial port disable
    - Parallel port disable

2.2.2 OPTIONS

Options that are specific to the Compaq Deskpro 2000 Series Personal Computers include:

- Memory:
  - 4-MB Memory Module
  - 8-MB Memory Module
  - 16-MB Memory Module
  - 32-MB memory Module

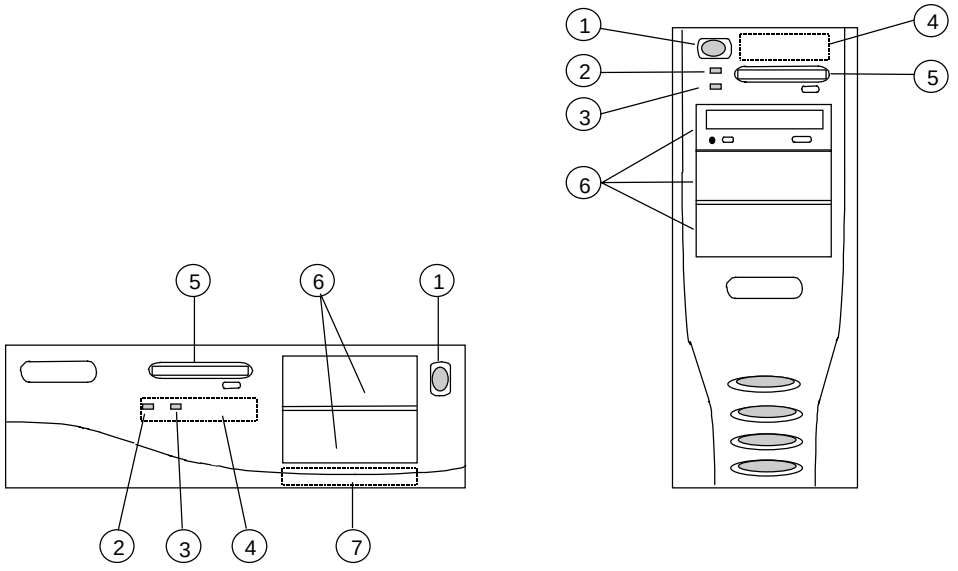
- Graphics:
  - 1-MB Frame Buffer Memory Module (GD5436/GD5446-based cntlrs.)
  - 2-/6-MB WRAM Upgrade Modules (for Matrox Millennium Graphics Card)

Compaq Deskpro 2000 Personal Computers are easily upgraded and enhanced with peripheral devices designed to meet PCI and ISA standards. The Compaq Deskpro 2000 Personal Computers are compatible with peripherals design for Plug 'n Play operation.

2.3 MECHANICAL DESIGN

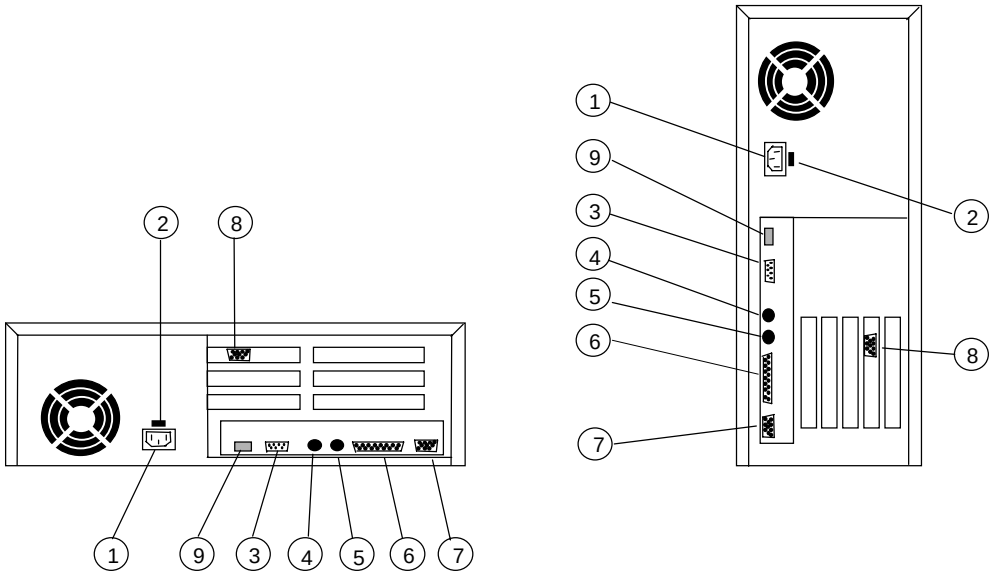
The Compaq Deskpro 2000 Series features two formfactors; desktop and minitower. This section illustrates the layouts used by these two formfactors. In addition, this section includes the layouts of the system boards.

2.3.1 CABINET LAYOUTS



Item	Function
1	Power Switch
2	Power-On Light
3	Hard Drive Activity Light
4	1/3 Height Internal Drive Bay (3.5” Drive)
5	1.44 MB Diskette Drive (3.5” Drive)
6	½ Height Drive Bay (3.5” or 5.25” Drive)
7	1/3 Height Internal Drive Bay (5.25” Drive)

Figure 2–2. Cabinet Layout, Front View



Item	Function
1	AC Line In Connector
2	Line Voltage Select Switch
3	Serial Interface
4	Keyboard Interface
5	Mouse Interface
6	Parallel Interface
7	Monitor Interface (Pentium-based system)
8	Monitor Interface (Pentium Pro-based system)
9	Universal serial bus interface [1]

NOTE:

[1] Not present on early version Pentium-based systems.

Figure 2–3. Cabinet Layout, Rear View

2.3.2 CHASSIS LAYOUTS

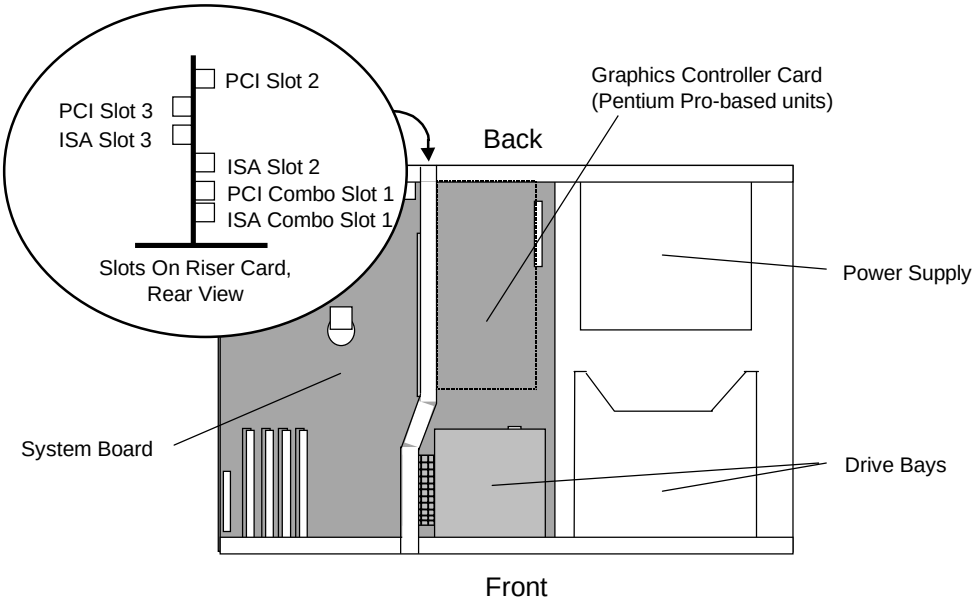


Figure 2–4. Desktop Chassis Layout, Top View

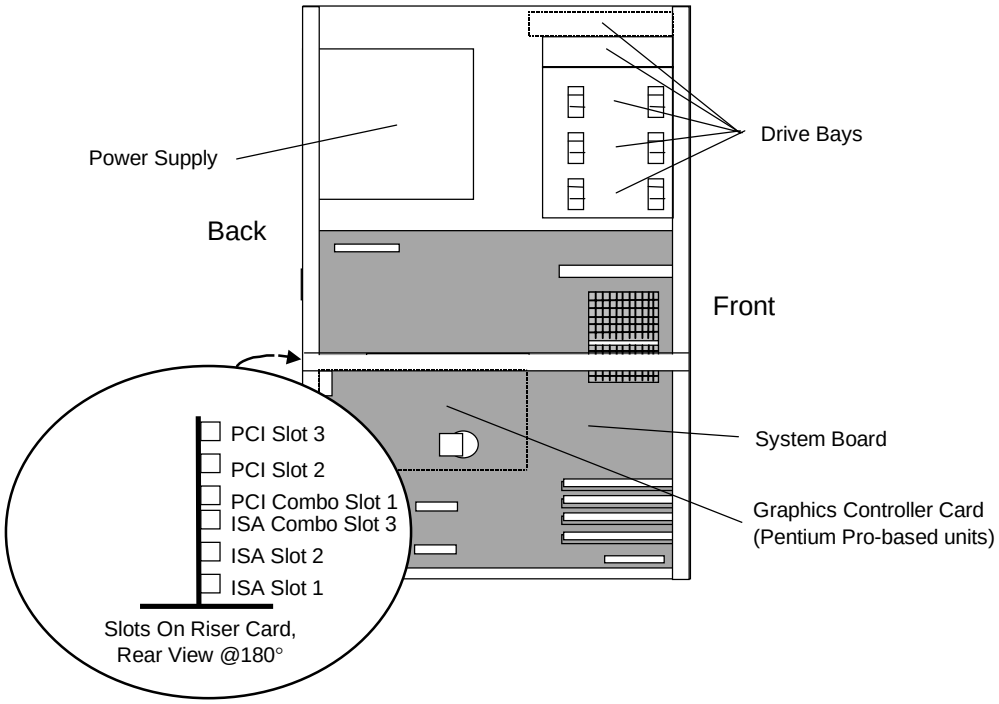
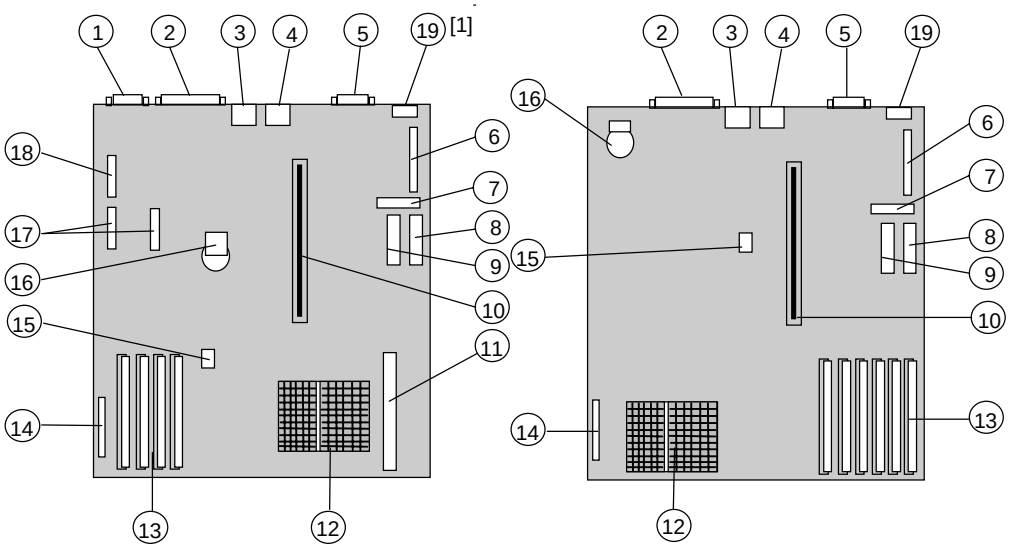


Figure 2–5. Minitower Chassis Layout, Left Side View

2.3.3 SYSTEM BOARD LAYOUTS



Pentium-Based System Board Pentium Pro-Based System Board

Item	Function
1	Graphics monitor connector
2	Parallel interface connector
3	Mouse interface connector
4	Keyboard interface connector
5	Serial interface connector
6	Power supply connector
7	Diskette drive connector
8	Hard drive connector (primary)
9	Hard drive connector (secondary)
10	Riser card connector
11	L2 Cache module connector
12	Microprocessor (in socket)
13	SIMM sockets
14	Jumper header
15	Processing frequency configuration switch
16	RTC/CMOS battery
17	Graphics controller expansion memory connector
18	Graphics controller VESA interface connector
19	Universal serial bus interface connector

NOTE:

[1] Not present on early version Pentium-based system boards.

Figure 2–6. System Board Layout, Component Side

2.4 SYSTEM ARCHITECTURE

The Compaq Deskpro 2000 Personal Computer is based on a Pentium or Pentium Pro microprocessor matched with a support chipset that is complimentary in design. Both minitower and desktop systems share the same basic architecture (Figure 2-7), which utilizes three main buses: the Host bus, the Peripheral Component Interconnect (PCI) bus, and the Industry Standard Architecture (ISA) bus.

The Host bus provides high performance support for CPU, cache and system memory accesses, and operates at 50 to 75 % of the processing speed of the microprocessor. The PCI bus provides support for the graphics subsystem, the EIDE controllers, and expansion devices designed for high performance. The PCI bus operates at typically 50 % of the Host bus speed. The ISA bus provides a standard 8-MHz interface for the input/output (I/O) devices such as the keyboard, diskette drive, serial and parallel interfaces, as well as the addition of 16- or 8-bit expansion devices.

The CPU/PCI and PCI/ISA bridge functions are handled by the specific support chipset matched with the microprocessor employed. The support chipset also provides memory controller and data buffering functions., as well as bus control and arbitration functions.

The I/O port functions and diskette drive controller are integrated into the PC87306 I/O Controller. This component also includes the real time clock and battery-backed configuration memory (CMOS).

The Compaq Deskpro 2000 Series consists of architectural variations based on the baseline microprocessor. These variations are compared in Table 2-1. Note that table 2-1 lists only differences.

Table 2-1.
Architectural Comparison

Component(s)	Pentium-Based	Pentium Pro 180-Based	Pentium Pro 200-Based
Support Chipset	82430	Intel 8244x	Intel 8244x
System Memory			
Standard inst.	8/16 MB	16 MB	16 MB
Expandable to:	128 MB	192 MB	192 MB
Cache Memory			
L1:	16 KB [1]	16 KB [1]	16 KB [1]
L2:	256 KB Module [2]	256 KB [1]	256 KB [1]
Graphics Subsystem	GD5436-based w/I MB DRAM	GD5446-based PCI Card w/1 MB DRAM	Matrox MGA Millennium PCI Card w/2 MB WRAM

NOTES:
[1] Integrated with the microprocessor
[2] Optional

The following subsections provide a description of the key functions and subsystems.

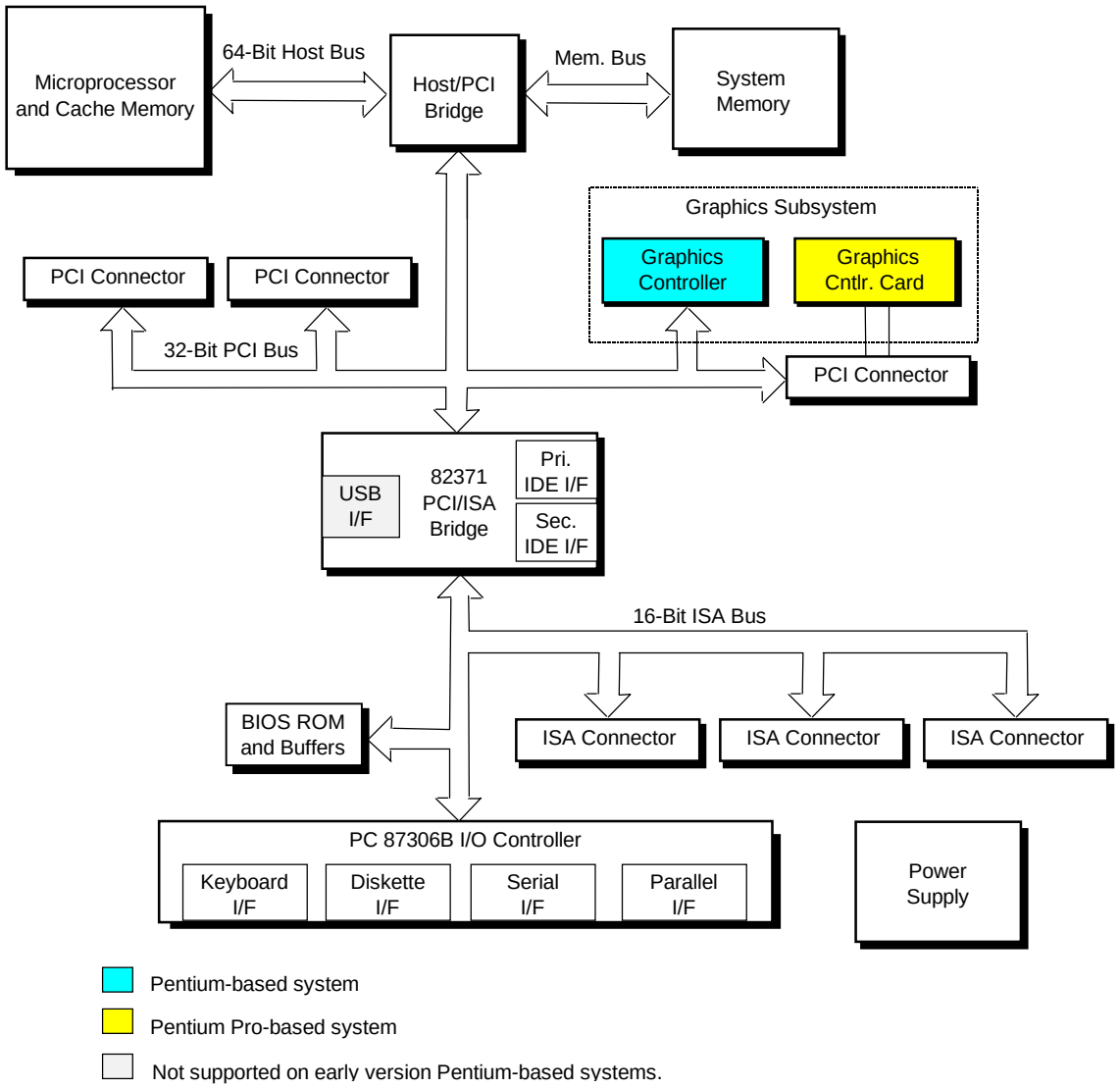


Figure 2–7. Compaq Deskpro 2000 System Architecture, Block diagram

2.4.1 MICROPROCESSOR

The Compaq Deskpro 2000 Personal Computers feature Pentium and Pentium Pro microprocessors. These microprocessors are backward-compatible with software written for x86-type microprocessors, but provide a dramatic increase in performance over earlier x86-type components. The Pentium microprocessor includes a dual-ALU central processing unit (CPU) with branch prediction support and an integrated 16-KB cache along with a math coprocessor. The Pentium Pro microprocessor adds an integrated 256-KB secondary cache and supports out-of-order instruction processing. The microprocessor is mounted in a zero-insertion-force (ZIF) socket for easy upgrading.

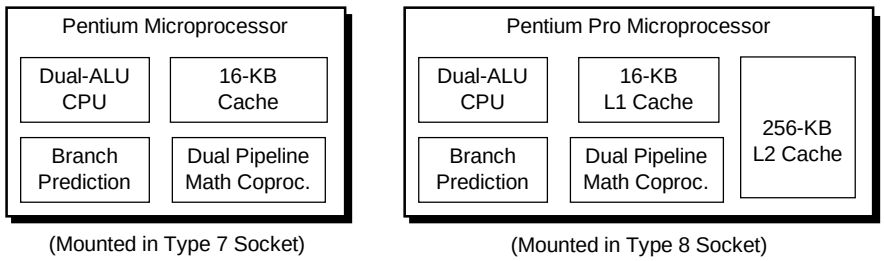


Figure 2–8. Microprocessor Comparison Diagram

2.4.2 MEMORY SUBSYSTEM

The memory subsystem consists of the memory controller, data buffers, and system memory (DRAM). All models use 60 ns, EDO DRAM SIMMs. The Pentium-based system provide four SIMM sockets and come standard with 8 or 16 megabytes of RAM. The Pentium Pro-based unit provides six SIMM sockets and includes 16 megabytes of RAM as standard.

Additional memory can be added using 4-, 8-, 16-, and 32-MB SIMMs. All models are designed to use 60 ns SIMMs but can be configured for using 70 ns SIMMs.

NOTE: SIMMs must be installed in matched pairs. Refer to chapter 3 for more details on installing expansion memory.

2.4.3 GRAPHICS SUBSYSTEM

The Compaq Deskpro 2000 Personal Computer uses one of three variations of graphics subsystems, depending on model. The graphics subsystem of all models operates off the PCI bus and uses a Cirrus Logic graphics controller. Table 2-2 outlines the key differences between the graphics subsystems.

Table 2-2.
Graphics Subsystem Comparison

	Pentium-Based System	Pentium Pro 180-Based	Pentium Pro 200-Based
Graphics Controller	CL-GD5436 [1]	GD5446 [2]	Matrox MGA [2]
Graphics Memory			
Standard installed:	1 MB EDO DRAM	1 MB EDO DRAM	2 MB WRAM
Expandable to:	2 MB EDO DRAM	2 MB EDO DRAM	4/8 MB WRAM
Maximum Resolution			
w/ standard mem.	1280x1024 @ 16 colors	1600x1200 @ 256 colors	1600x1200 @ 256 colors
w/ max. mem.	1280x1024 @ 256 colors	1280x1024 @ 256 colors	1600x1200 @ 16M colors

NOTES:
[1] Integrated onto the system board.
[2] Separate PCI card

The Pentium-based system features a CL-GD5436 graphics controller and one megabyte of EDO DRAM for the graphics memory. An optional 1-MB EDO DRAM module can be added to bring the total to two megabytes of graphics memory.

The 180-MHz Pentium Pro-based system features a PCI graphics card that is based on the CL-GD5446 graphics controller. The card includes one megabyte of EDO DRAM as standard and can be expanded to two megabytes by adding a 1-MB EDO DRAM module.

The 200-MHz Pentium Pro-based system features a Matrox MGA Millennium graphics controller card that is installed in a PCI slot. This controller includes two megabytes of WRAM as standard and can be expanded to four or eight megabytes by adding a 2- or 6-MB WRAM module.

2.4.4 MASS STORAGE

All models include a 3.5 inch 1.44-MB diskette drive installed. An 840-MB, 1.0-GB, 1.2-GB, or 2.5-GB IDE hard drive may also be installed, depending on model. All models include a PCI bus mastering Enhanced IDE (EIDE) controller (integrated into the 82371 component) that provides two EIDE interfaces four supporting up four IDE devices. Master/slave drive selection is determined using the cable-select method, eliminating the need to move jumpers when re-configuring drives. The mass storage drive bay capacity is determined by the form factor (refer to Section 2.3, Mechanical Design).

2.4.5 SERIAL AND PARALLEL INTERFACES

All models include a serial and parallel port available at the rear of the unit chassis. The serial and parallel ports are integrated into a PC87306 I/O Controller component. The serial port is RS-232-C/16550-compatible and operates at baud rates up to 19,000. The parallel interface is Enhanced Parallel Port (EPP) and Enhanced Capability Port (ECP) compatible, and supports bi-directional data transfers.

2.4.6 UNIVERSAL SERIAL BUS INTERFACE

All Pentium Pro-based systems and later version Pentium-based systems feature a Universal Serial Bus (USB) port that provides a high speed interface for future systems and/or peripherals. The USB operates at 12 Mbps and provides hot plugging/unplugging (Plug 'n Play) functionality.

2.5 SPECIFICATIONS

This section includes the environmental, electrical, and physical specifications for the Compaq DESKPRO 2000 Series Personal Computers.

Table 2-3.
Environmental Specifications

Parameter	Operating	Nonoperating
Air Temperature	50° to 95° F (10° to 35° C)	-40° to 158° F (-40° to 70° C)
Shock	2.0 g for 11 ms half-sine pulse	30.0 g for 11 ms half-sine pulse
Vibration	1 G for 5-200 Hz sinusoidal	N/A
Humidity	80% RH @ 36° C (no hard drive)	95% RH @ 36° C
Maximum Altitude	10,000 ft (3048 m)	50,000 ft (15,240 m)

Table 2-4.
Electrical Specifications

Parameter	Domestic	International
Input Line Voltage:		
Nominal:	100 - 120 VAC	200 - 240 VAC
Maximum:	90 - 135 VAC	180 - 265 VAC
Input Line Frequency Range:		
Nominal:	50 - 60 Hz	50 - 60 Hz
Maximum:	47 - 63 Hz	47 - 63 Hz
Power Supply:		
Maximum Continuous Power:		
Desktop:	145 watts	145 watts
Minitower:	185 watts	185 watts
Maximum Peak Power:	200 watts	200 watts
Maximum Line Current Draw:	5.0 A	3.0 A

Table 2-5.
Physical Specifications

Parameter	Desktop	Minitower
Height	5.0 in (12.7 cm)	16.69 in (42.39 cm)
Width	17.69 in (44.93 cm)	7.3 in (18.54 cm)
Depth	15.75 in (38.0 cm)	18.56 in (47.14 cm)
Weight	17.2 lb (7.49 kg)	34.0 lb (15.40 kg)

NOTE:
Metric measurements shown in parenthesis.

Table 2-6.
Diskette Drive Specifications

Paramemter	Measurement
Media Type	3.5 in 1.44 MB/720 KB diskette
Height	1/3
Bytes per Sector	512
Sectors per Track:	
High Density	18
Low Density	9
Tracks per Side:	
High Density	80
Low Density	80
Read/Write Heads	2
Average Access Time:	
Track-to-Track (high/low)	3 ms/3 ms
Average (high/low)	94 ms/94ms
Settling Time	15 ms
Latency Average	100 ms

Table 2-7.
8x CD-ROM Drive Specifications

Paramemter	Measurement
Media Type	Mode 1,2, Mixed Mode, CD-DA, Photo CD, Cdi, CD-XA
Center Hole Diameter	15 mm
Disc Diameter	8/12 cm
Disc Thickness	1.2 mm
Track Pitch	1.6 um
Laser	
Beam Divergence	53.5 +/- 1.5 °
Output Power	53.6 0.14 mW
Typr	GaAs
Wave Length	790 +/- 25 nm
Average Access Time:	
Random	150 ms
Full Stroke	350 ms
Audio Output Level	0.7 Vrms
Cache Buffer	128 KB (min)
Data Transfer Time	
Sustaiined	1200 KB/s
Startup Time	7 secs (nom)

Table 2-8.
Hard Drive Specifications

Parameter	630 MB	1.08 GB	1.2 GB	1.6 GB	2.5 GB
Capacity (Formatted)	631.7 MB	1083.4 MB	1281.9 MB	1622 MB	2560 MB
Drive Type	65	65	65	65	65
Drive Size	3.5 in	3.5 in	5.25 in	3.5 in	5.25 in
Transfer Rate	22.9 MB/s	16.7 MB/s	16.7 MB/s	16.7 MB/s	16.7 MB/s
Seek Time (w/settling)					
Single Track	5.0 ms	3.0 ms	5.0 ms	3.0 ms	3.5 ms
Average	14.0 ms	12.0 ms	15.5 ms	12.0 ms	15.5 ms
Full Stroke	34.0 ms	22.0 ms	30.0 ms	25.0 ms	30.0 ms
Disk RPM	3811	5378	5400	4480	4500
Cylinders	1224	2100	2484	3148	4969
Data Heads (logical)	16	16	16	16	16
Sectors per Track (logical)	63	63	63	63	63

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Chapter 3
PROCESSOR/ MEMORY SUBSYSTEM

3.1 INTRODUCTION

This chapter describes the processor/cache memory subsystem of the Compaq Deskpro 2000 Series of Personal Computers. Two subsystem designs are used. One subsystem is based on a 586-class microprocessor and the other subsystem is based on the Pentium Pro microprocessor.

This chapter includes the following topics:

As shown in Table 3-1, there are two variations of processor/memory architecture in the Compaq Deskpro 2000 Series of Personal Computers.

Table 3-1.
Processor/Memory
Architectural Comparison

Feature	Pentium-Based	Pentium Pro-Based
Support Chipset	82430	Intel 8244x
System Memory		
Standard installed:	16 MB	16 MB
Expandable to:	128 MB	192 MB
Cache Memory		
L1:	16 KB [1]	16 KB [1]
L2:	256 KB Module	256 KB [1]

NOTES:
[1] Integrated into the microprocessor

3.2 PROCESSOR/MEMORY SUBSYSTEM DESCRIPTIONS

This section provides a comparison of the three processor/memory subsystem designs used in the Compaq Deskpro 2000 Series.

3.2.1 PENTIUM-BASED PROCESSOR/MEMORY SUBSYSTEM

The processor/memory subsystem in Pentium-based systems use an 82430 TXC system controller and comes standard with 16 megabytes of 60 ns DRAM for system memory (Figure 3-1).

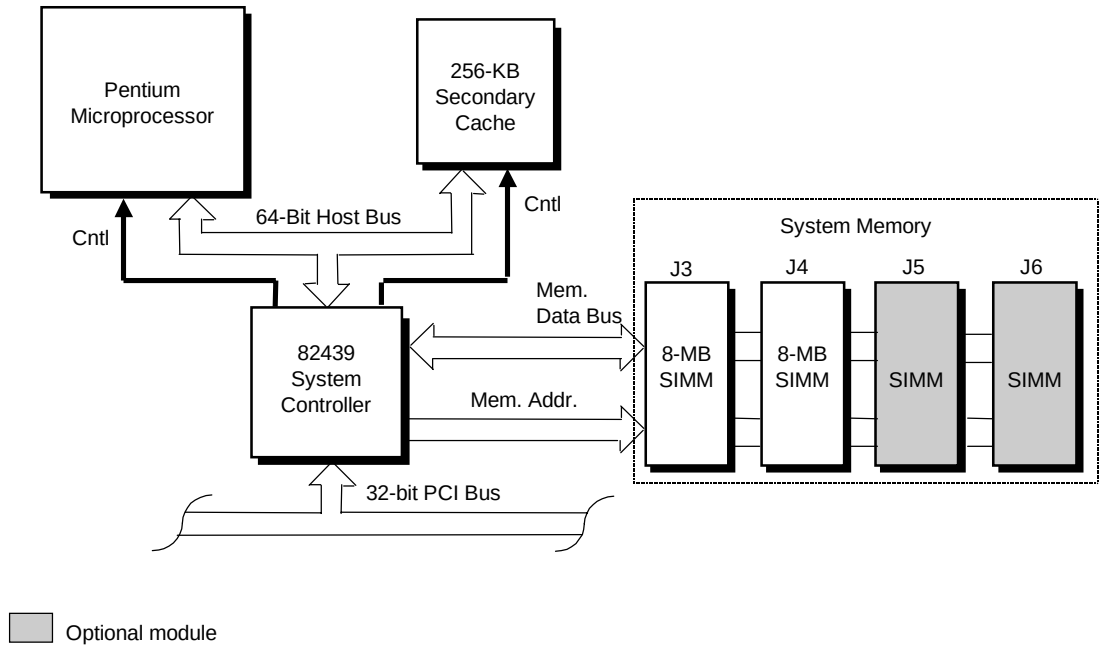


Figure 3–1. Pentium-Based Processor/Memory Subsystem Architecture

The microprocessor is mounted in a ZIF type 7 socket that facilitates easy changing/upgrading. Replacing the microprocessor may require reconfiguring a DIP switch to select the correct bus frequency/core frequency combination. Frequency selection is described in detail later in this chapter in Section 3.3 “Microprocessor Descriptions.”

The 82439 system controller provides the Host/PCI bridge functions and controls transfers with the 64-bit memory data bus. The Pentium-based system includes the 256-KB cache module, which is controlled by the 82439 system controller as a direct-mapped L2 cache to the L1 cache integrated into the Pentium microprocessor. The system supports synchronous, pipelined burst SRAM/DRAM for the L2 cache, providing 3-1-1-1 read/write cycles at 60 and 66 MHz on a cache hit.

The system memory comes with 16 megabytes of standard DRAM that can be expanded to 128 megabytes.

3.2.2 PENTIUM PRO-BASED PROCESSOR/MEMORY SUBSYSTEM

The processor/memory subsystem used in the Pentium Pro-based systems use an 82442 data buffer/controller, an 82441 system controller, and comes standard with 16 megabytes of 60 ns DRAM for system memory (Figure 3-2).

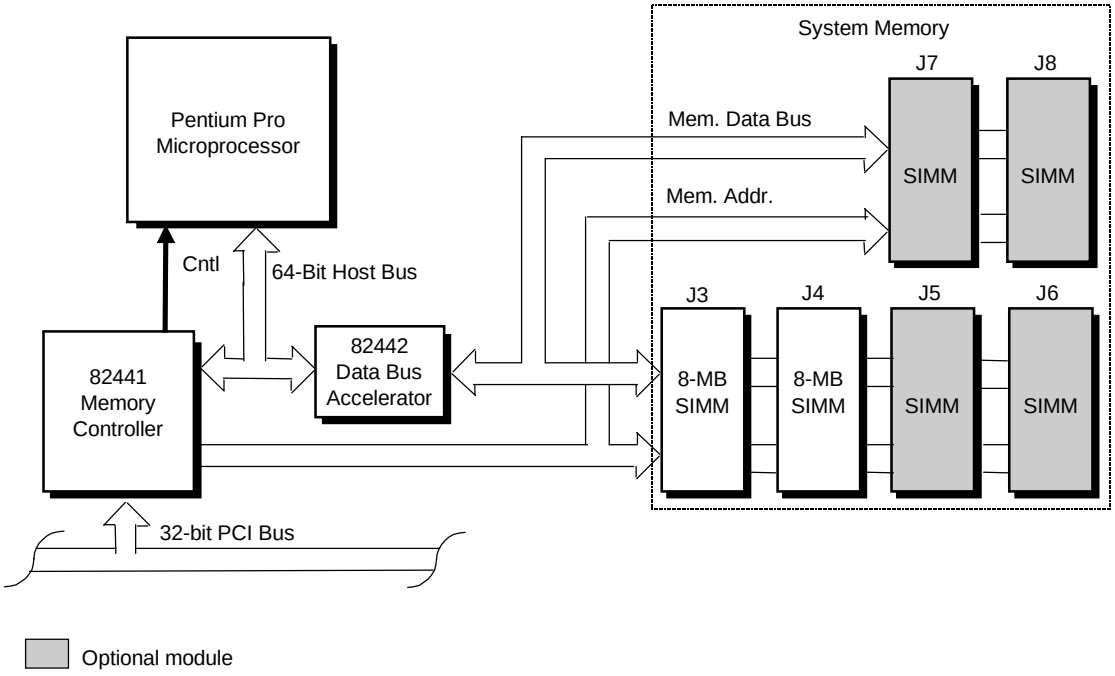


Figure 3–2. Pentium Pro-Based Processor/Memory Subsystem Architecture

The microprocessor is mounted in a ZIF type 8 socket that facilitates easy changing/upgrading. Replacing the microprocessor may require reconfiguring a DIP switch to select the correct bus frequency/core frequency combination, and is described in detail later in this chapter in Section 3.3 “Microprocessor Descriptions.”

NOTE: The L2 cache is integral with the Pentium Pro microprocessor.

The 82441 system controller provides the Host/PCI bridge functions and drives the memory address lines. The 82441 memory controller handles transfers with the 64-bit memory data bus. The system provides six SIMM sockets. In the standard configuration, two sockets are populated with 8-MB SIMMs providing 16 megabytes of RAM that can be expanded up to 192 megabytes using the same SIMMs used with the other models on the Compaq Deskpro 2000 Series.

3.3 MICROPROCESSOR DESCRIPTIONS

This section describes the Pentium and Pentium Pro microprocessors used in the Compaq Deskpro 2000 Series of Personal Computers.

3.3.1 PENTIUM MICROPROCESSOR

The Pentium microprocessor is software-compatible with earlier generation x86 microprocessors but provides significantly higher performance due to both higher processing speed and enhanced design (Figure 3-3.).

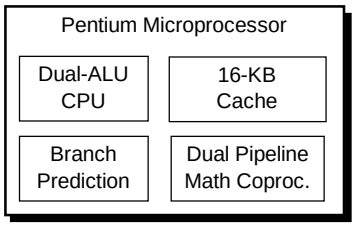


Figure 3–3. Pentium Microprocessor Internal Architecture

The Pentium microprocessor supports dual-instruction processing and includes a pipelined floating point unit (math coprocessor) and cache memory. The integrated cache memory acts as an L1 cache when the 256-KB cache module is installed.

> **NOTE:** The 256-KB cache module does not support the linear burst mode of the Cyrix M1. Only standard Intel bursts are supported by the 256-KB cache module.

For more information on the internal architecture of the Pentium microprocessor refer to applicable Intel documentation.

The Pentium microprocessor is mounted in a ZIF type 7 socket for easy changing/upgrading of the microprocessor. Replacing the microprocessor may require reconfiguring the settings of DIP switch SW1 to properly set the speed of the Host bus and the core (processing) frequencies. The following section describes the speed configurations.

3.3.1.1 Bus/Processing Speed Configuration (Pentium-Based System)

The Pentium-based system board includes a four-position DIP switch (SW1) that is used to select the Host bus frequency and the processing frequency of the system. Switch positions 1 and 2 control the Frequency Select (FS0,1) signals that determine the frequency of the clock signal to the microprocessor. Switch positions 3 and 4 control the Bus Fraction (BF0,1) inputs to the microprocessor and determine the Host bus speed-to-core speed ratio, i.e., the processing speed. Table 3-2 shows the switch configurations to be used with a particular microprocessor.

Table 3-2.
Pentium Microprocessor
Bus/Core Speed Switch Settings

DIP SW1 Settings 1 2 3 4 [1]	Intel P54C(s)
0 0 0 0	50/125
0 0 0 1	50/100
0 0 1 0	50/150
0 0 1 1	50/75
0 1 0 0	60/150
0 1 0 1	60/120
0 1 1 0	60/180
0 1 1 1	60/90
1 0 0 0	66/167
1 0 0 1	66/133
1 0 1 0	66/200
1 0 1 1	66/100
1 1 0 0	55/137.5
1 1 0 1	55/110
1 1 1 0	55/165
1 1 1 1	55/82.5

NOTES:
[1] 0 = Closed, 1 = Open
[2] Host bus speed / Core speed (both in MHz)
Microprocessor bus/core speed combo that is either not recommended or not available.

The status of all four switch positions is readable through general-purpose I/O (GPIO) port 78h bits <3..0>, allowing BIOS and/or diagnostic software to check an installed microprocessor with the switch configuration. Table 3-3 shows the switch position-to-GPIO-to-I/O port E8h input wiring.

Table 3-3.
Bus/Core Speed Switch
I/O Controller GPIO Assignments
for Pentium-Based Systems

Switch Position	Signal Name	GPIO Number	I/O Port E8h
S1	FS0	10	bit <0>
S2	FS1	11	bit <1>
S3	BF0	12	bit <2>
S4	BF1	13	bit <3>

FS = Frequency Select BF = Bus Fraction

3.3.2 PENTIUM PRO MICROPROCESSOR

The Pentium Pro microprocessor provides all the functionality of the 586-class microprocessor and includes additional functions such as an integrated 256-KB L2 cache (Figure 3-4).

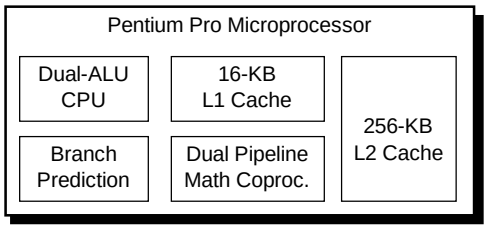


Figure 3–4. Pentium Pro Microprocessor

The Pentium Pro microprocessor is software-compatible with earlier x86-type microprocessors but provides significantly enhanced performance due to a number of design features such as:

- Integrated L1 cache with separate sections for code and data
- Integrated 256-KB second-level cache
- Super-scalar architecture
- Internal error checking (Machine Check Architecture)
- Model-specific register programming
- Out-of-order instruction processing support

The Pentium Pro microprocessor is mounted in a 387-pin ZIF socket for convenient upgrading. Replacing the microprocessor may require reconfiguring the systems's clock speeds to accommodate the speed of the new microprocessor. The following section describes the possible speed configurations for the Pentium Pro-based systems.

For detailed information on the Pentium Pro microprocessor refer to the manufacturer's documentation.

3.3.2.1 Bus/Processing Speed Configuration (Pentium Pro-Based System)

The Pentium Pro-based system board includes a six-position DIP switch (SW1) that is used to select the Host bus frequency and the processing frequency of the system. Switch positions 1 and 2 select the host bus frequency while positions 3 through 6 determine the bus-to-core frequency ratio, i.e., the processing speed. Table 3-4 shows the possible switch configurations and their respective results.

Table 3-4.
Pentium Pro Microprocessor
Bus/Core Speed Switch Settings

DIP SW1 Settings 1 2 3 4 5 6 [1]	Bus/Core Speed (in MHz)	DIP SW1 Settings 1 2 3 4 5 6 [1]	Bus/Core Speed (in MHz)
0 0 0 0 0 0	50/100	1 0 0 0 0 0	60/120
0 0 0 0 0 1	50/125	1 0 0 0 0 1	60/150
0 0 0 0 1 0	50/150	1 0 0 0 1 0	60/180
0 0 0 0 1 1	50/175	1 0 0 0 1 1	60/210
0 0 0 1 0 0	50/200	1 0 0 1 0 0	60/240
0 0 0 1 0 1	50/225	1 0 0 1 0 1	60/270
0 0 0 1 1 0	50/250	1 0 0 1 1 0	60/300
0 0 0 1 1 1	50/275	1 0 0 1 1 1	60/330
0 1 0 0 0 0	66/133	1 1 0 0 0 0	55/110
0 1 0 0 0 1	66/167	1 1 0 0 0 1	55/137
0 1 0 0 1 0	66/200	1 1 0 0 1 0	55/164
0 1 0 0 1 1	66/233	1 1 0 0 1 1	55/190
0 1 0 1 0 0	66/266	1 1 0 1 0 0	55/220
0 1 0 1 0 1	66/300	1 1 0 1 0 1	55/250
0 1 0 1 1 0	66/333	1 1 0 1 1 0	55/275
0 1 0 1 1 1	66/366	1 1 0 1 1 1	55/300

NOTES:

[1] 0 = Closed or “On”, 1 = Open or “Off”
If SW’s 1-6 = x x 1 x x x then Reserved
If SW’s 1-6 = x x 1 1 1 1 then 2/4 bus/core speed ratio takes effect.

The status of switch positions 3 through 6 is readable through the GPIO port E8h bits <3..0>, allowing BIOS and/or diagnostic software to check an installed microprocessor with the switch configuration. Table 3-5 shows the switch position-to-GPIO input wiring.

Table 3-5.
Bus/Core Speed Switch
I/O Controller GPIO Assignments
for Pentium Pro-Based Systems

Switch Position	Signal Name	GPIO Number	I/O Port E8h
S3	CFG NMI	13	bit <3>
S4	CFG A20M	12	bit <2>
S5	CFG IGNNE	11	bit <1>
S6	CFG INTR	10	bit <0>

3.4 SYSTEM MEMORY

All models of the Compaq Deskpro 2000 Series use industry standard, 72-pin SIMMs. Table 3-6 shows the basic differences in system memory between the series.

Table 3-6.
System Memory Comparison

System Memory	Pentium-Based	Pentium Pro-Based
Standard Installed	16 MB	16 MB
Maximum Amount:		
Installable w/32-MB SIMMs:	128 MB	192 MB
Supported by chipset:	xxx MB	768 MB
No. of Banks	2	3
No. of SIMM Sockets	4	6

Although all models ship with 60 ns SIMMs, 70 ns SIMMs can be used. All systems ship with Extended Data Out (EDO) DRAM SIMMs, although the system will accept Fast Page Mode (FPM) SIMMs. Different SIMM speeds and types can be mixed within a system as long as the two SIMMs in each bank are of the same speed and type.

> **NOTE:** Two SIMMs that have different access times but are otherwise identical may be used together in the same bank without problems.

The SIMMs must be installed in pairs to satisfy the 64-bit bandwidth of each memory bank. If a system includes both 60 and 70 ns SIMMs, the BIOS will detect the slowest speed installed and set the system to run at the slower (70 ns) speed. Detection is affected by pin 69 (Presence Detect (PD3) signal) of the SIMM socket. A 70 ns SIMM grounds the PD3 line while a 60 ns SIMM leaves the PD3 line floating. The PD3 line of both sockets of each bank are connected together and applied to a General Purpose pin of the 87306 I/O controller. Two 60 ns SIMMs result in a logic 1 at the pin while two 70 ns SIMMs or a 60/70 ns mix result in a logic 0 on the pin. The General Purpose pins are assigned as follows:

Gen. Purpose Pin	Mem. Bank
P13	0
P14	1
P15	3 (Pentium Pro-based only)

To read the P15..13 pins of the I/O controller, the value C0h must first be written to I/O port 64h. As soon as the keyboard controller function of the I/O controller responds by setting bit <0> of 64h, a read of port 60h yields the status of pins P17..10.

The following subsections describe aspects of system memory that are unique to each series of Deskpro 2000 systems.

3.4.1 PENTIUM-BASED SYSTEM MEMORY

The Pentium-based system uses the 82439 TXC component for controlling the two banks of system memory. The 82430 provides complete control of the system memory, driving the address lines and handling the data transfers.

Using EDO SIMMs and a 66-MHz bus speed, 5-2-2-2 memory cycles are possible with bank 1. The address lines to bank 2 (sockets J5 and J6) are buffered, resulting in x-3-3-3 performance.

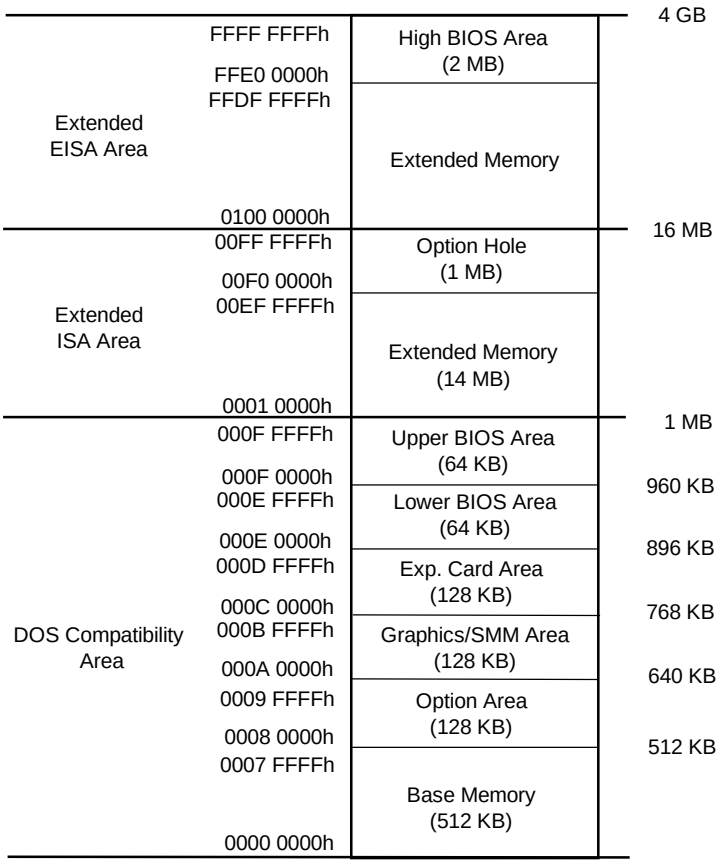


Figure 3–5. Pentium-Based System Memory Map

3.4.2 PENTIUM PRO-BASED SYSTEM MEMORY

The Pentium Pro-based system uses the 8244x components for controlling up to three banks of system memory. The 82441 memory controller drives the address lines while the data transfers are handled by the 82442 data bus buffer. Using 60-nsEDO SIMMs and a 66-MHz bus speed, x-3-3-3 memory cycles are possible with all banks.

The memory map for the Pentium Pro-based system is shown in Figure 3-6 and includes areas of variable usage. The 128-KB Option Area can be mapped as a DOS region or for PCI purposes. The 128-KB graphics/SMM area is mapped as PCI space in normal operation and is also used when the system is in system management mode (SMM). The next 12 16-KB blocks and the BIOS areas can have four possible attributes: read only (from DRAM for reads, to PCI for writes), write only (to DRAM for writes, from PCI for reads), read/write (all DRAM accesses), and disabled (all PCI accesses). ROM shadowing is accomplished by first setting the appropriate area to write-only. A read access will then obtain the data from the ROM. Next, a write to the same address will result in the data being written into DRAM. After the copy function is complete, the attributes of the appropriate area can be set to read-only or read-write. The ROM can be unshadowed by resetting the attributes to write-only.

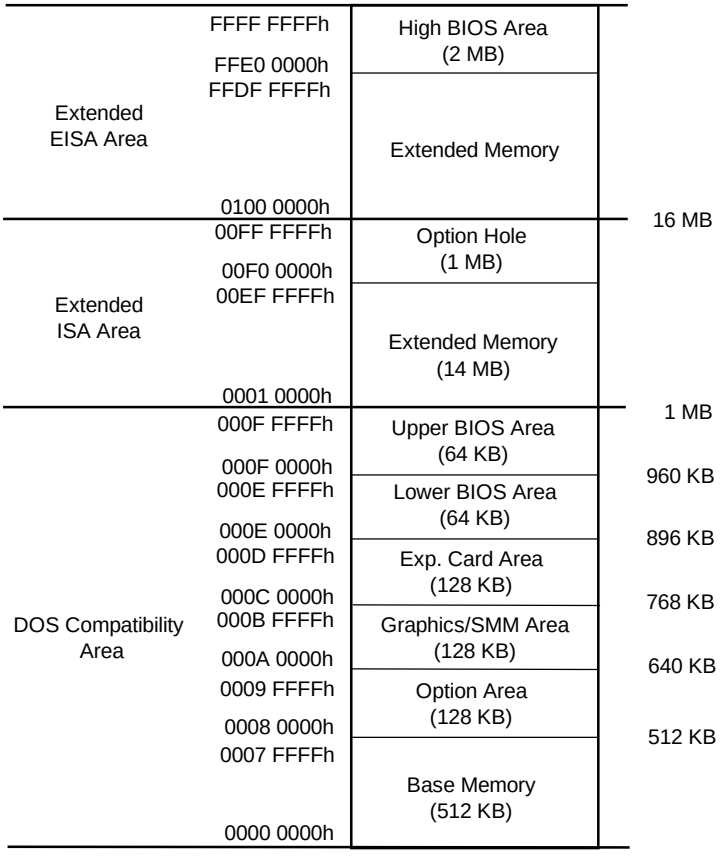


Figure 3–6. Pentium Pro-Based System Memory Map

Chapter 4
SYSTEM SUPPORT

4.1 INTRODUCTION

This chapter covers subjects dealing with basic system architecture and covers the following topics:

This chapter covers functions provided by off-the-shelf chipsets and therefore describes only basic aspects of these functions as well as information unique to the Compaq Deskpro 2000 Series. For detailed information on specific components, refer to the applicable manufacturer's documentation.

4.2 PCI BUS OVERVIEW

NOTE: This section describes the PCI bus in general and highlights bus implementation in this particular system. For detailed information regarding PCI bus operation, refer to the *PCI Local Bus Specification Revision 2.1*.

The 32-bit PCI bus uses a shared address/data bus design. On the first clock cycle of a PCI bus transaction, the bus carries address information. On subsequent cycles, the bus carries data. PCI transactions occur synchronously with the Host bus at a rate of up to 33 MHz, depending on the speed of the microprocessor used. All I/O transactions involve the PCI bus. All ISA transactions involving the microprocessor, cache, and memory also involve the PCI bus. Memory cycles will involve the PCI if the access is initiated by a device or subsystem other than the microprocessor.

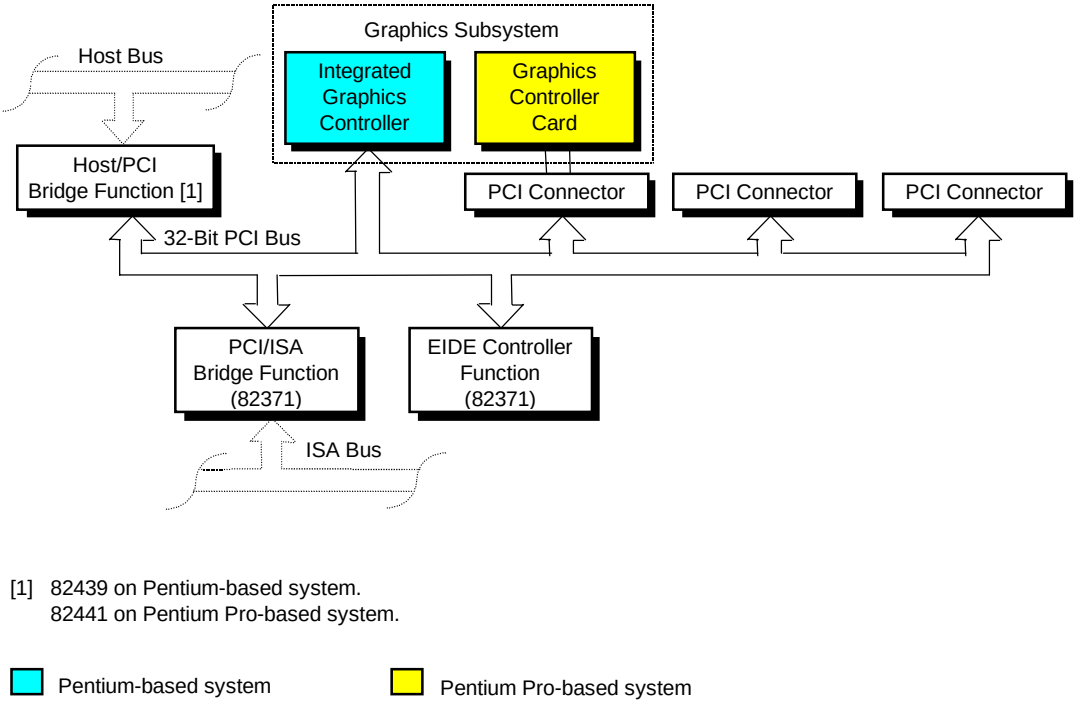


Figure 4–1. Compaq Deskpro 2000 Series PCI Bus Devices and Functions

4.2.1 PCI SLOT DESCRIPTIONS

Slot 1 Standard PCI 5-volt 32-bit connector with all common PCI signals and slot-specific signals including REQ0- and GNT0-. Configured as PCI Device # 2.

Slot 2 Standard PCI 5-volt 32-bit connector with all common PCI signals and slot-specific signals including REQ1- and GNT1-. Configured as PCI Device # 3.

Slot 3 Standard PCI 5-volt 32-bit connector with all common PCI signals and slot-specific signals including REQ2- and GNT2-. Configured as PCI Device # 4.

4.2.2 PCI CONNECTOR

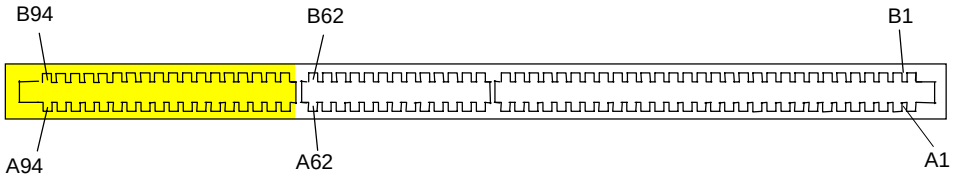


Figure 4–2. PCI Bus Connector (5V Type)

Table 4-1.
PCI Bus Connector Pinout

Pin	B Signal	A Signal	Pin	B Signal	A Signal	Pin	B Signal	A Signal
01	-12 VDC	TRST-	32	AD17	AD16	63	Reserved	GND
02	TCK	+12 VDC	33	C/BE2-	+3.3 VDC	64	GND	C/BE7-
03	GND	TMS	34	GND	FRAME-	65	C/BE6-	C/BE5-
04	TDO	TDI	35	IRDY-	GND	66	C/BE4-	+5 VDC
05	+5 VDC	+5 VDC	36	+3.3 VDC	TRDY-	67	GND	PAR64
06	+5 VDC	INTA-	37	DEVSEL-	GND	68	AD63	AD62
07	INTB-	INTC-	38	GND	STOP-	69	AD61	GND
08	INTD-	+5 VDC	39	LOCK-	+3.3 VDC	70	+5 VDC	AD60
09	PRSNT1-	Reserved	40	PERR-	SDONE	71	AD59	AD58
10	RSVD	+5 VDC	41	+3.3 VDC	SBO-	72	AD57	GND
11	PRSNT2-	Reserved	42	SERR-	GND	73	GND	AD56
12	GND	GND	43	+3.3 VDC	PAR	74	AD55	AD54
13	GND	GND	44	C/BE1-	AD15	75	AD53	+5 VDC
14	RSVD	Reserved	45	AD14	+3.3 VDC	76	GND	AD52
15	GND	RST-	46	GND	AD13	77	AD51	AD50
16	CLK	+5 VDC	47	AD12	AD11	78	AD49	GND
17	GND	GNT-	48	AD10	GND	79	+5 VDC	AD48
18	REQ-	GND	49	GND	AD09	80	AD47	AD46
19	+5 VDC	Reserved	50	Key	Key	81	AD45	GND
20	AD31	AD30	51	Key	Key	82	GND	AD44
21	AD29	+3.3 VDC	52	AD08	C/BE0-	83	AD43	AD42
22	GND	AD28	53	AD07	+3.3 VDC	84	AD41	+5 VDC
23	AD27	AD26	54	+3.3 VDC	AD06	85	GND	AD40
24	AD25	GND	55	AD05	AD04	86	AD39	AD38
25	+3.3 VDC	AD24	56	AD03	GND	87	AD37	GND
26	C/BE3-	IDSEL	57	GND	AD02	88	+5 VDC	AD36
27	AD23	+3.3 VDC	58	AD01	AD00	89	AD35	AD34
28	GND	AD22	59	+5 VDC	+5 VDC	90	AD33	GND
29	AD21	AD20	60	ACK64-	REQ64-	91	GND	AD32
30	AD19	GND	61	+5 VDC	+5 VDC	92	Reserved	Reserved
31	+3.3 VDC	AD18	62	+5 VDC	+5 VDC	93	Reserved	GND
--	--	--	--	--	--	94	GND	Reserved

64-bit extension not present in this system.

4.2.3 PCI BUS MASTER ARBITRATION

The PCI bus uses a bus master/target arbitration scheme. A bus master is a device that has been granted control of the bus for the purpose of initiating a transaction. A target is a device that is the recipient of a transaction. Request (REQ), Grant (GNT), and FRAME signals are used by PCI bus masters for gaining access to the PCI bus. When a PCI device needs access to the PCI bus (and does not already own it), the PCI device asserts it's REQ*n* signal to the PCI bus arbiter (a function of the system controller component). If the bus is available, the arbiter asserts the GNT*n* signal to the requesting device, which then asserts FRAME and conducts the address phase of the transaction with a target. If the PCI device already owns the bus, a request is not needed and the device can simply assert FRAME and conduct the transaction. Table 4-1 shows the grant and request signals assignments for the devices on the PCI bus.

Table 4-2.
PCI Bus Mastering Devices

PCI Device	REQ/GNT Line
PCI/ISA Bridge 82371 PIIX3	PHOLD-/PHLDA-
Graphics Controller (integrated)	REQn-/GNTn-
PCI Connector (slot 1)	REQ0-/GNT0-
PCI Connector (slot 2)	REQ1-/GNT1-
PCI Connector (slot 3)	REQ2-/GNT2-

PCI bus control is granted according to a Least Recently Used (LRU) algorithm. During times that the bus is not used or requested, bus control is given to the Host/PCI bridge. After a device has given up control of the bus or has not executed a transaction for 16 PCI clock cycles (PCICLKs) after gaining bus control, it loses access and is placed on the bottom of the priority list.

The PCI/ISA bridge is given special consideration. If the PCI/ISA bridge gains control of the PCI bus but does not execute a transaction after 16 PCICLKs, the PCI/ISA bridge retains ownership of the PCI bus until the current ISA bus master relinquishes the ISA bus. The PCI/ISA bridge is then placed on the bottom of the priority list.

PCI bus priority can be altered in two ways: by a master needing to perform a retry of a data cycle, or by the master locking the bus. When a master is retried, it releases the bus and negates its REQ*n*- line for a minimum of two PCICLKs and then requests the bus again. If the master is granted the bus before the condition that caused the retry is resolved, the master is retried again, which may result in bus "thrashing." Bus thrashing is minimized by masking the REQ*n*- line of a particular device that has had a transaction retried.

If a master locks the PCI bus, it retains top priority, allowing it to quickly finish a lock sequence. The PCI/ISA bridge cannot become master until the locking device unlocks the bus. Consequently, a master should not lock the bus for long periods of time or latency problems could occur.

4.2.4 PCI BUS TRANSACTIONS

The PCI bus consists of a 32-bit path (AD31-00 lines) that uses a multiplexed scheme for handling both address and data transfers. A bus transaction consists of an address cycle and one or more data cycles, with each cycle requiring a clock (PCICLK) cycle. High performance is realized during burst modes in which a transaction with contiguous memory locations requires that only one address cycle be conducted and subsequent data cycles are completed using auto-incremented addressing. Four types of address cycles can take place on the PCI bus; I/O, memory, configuration, and special. Address decoding is distributed (left up to each device on the PCI bus).

Two types of address decoding are allowed on the PCI bus; positive and subtractive. Positive decoding provides higher performance because PCI devices respond immediately to an address within a certain range. For this system, the Host/PCI bridge and any devices installed in the PCI expansion slots use positive decoding. The PCI/ISA bridge uses positive decoding for all functions except accesses to DMA register space and memory accesses below 16-MB that are claimed by a PCI device.

4.2.4.1 I/O and Memory Cycles

For I/O and memory cycles, a standard 32-bit address decode (AD31..0) for byte-level addressing is handled by the appropriate PCI device. For memory addressing, PCI devices decode the AD31..2 lines for dword-level addressing and check the AD1,0 lines for burst (linear-incrementing) mode. In burst mode, subsequent data phases are conducted a dword at a time with addressing assumed to increment accordingly (four bytes at a time).

4.2.4.2 Configuration Cycles

Devices on the PCI bus must comply with PCI protocol that allows configuration of that device by software. In this system, configuration mechanism #1 (as described in the PCI Local Bus specification Rev. 2.1) is employed. This method uses two 32-bit registers for initiating a configuration cycle for accessing the configuration space of a PCI device. The configuration address register (CONFIG_ADDRESS) at 0CF8h holds a value that specifies the PCI bus, PCI device, and specific register to be accessed. The configuration data register (CONFIG_DATA) at 0CFCh contains the configuration data.

PCI Configuration Address Register
I/O Port 0CF8h, R/W access (32-bit only)

Bit	Function
31	Configuration Enable 0 = Disabled 1 = Enable
30..24	Reserved - read/write 0s
23..16	Bus Number. Selects PCI bus
15..11	PCI Device Number. Selects PCI device for access
10..8	Function Number. Selects function of selected PCI device.
7..2	Register Index. Specifies config. reg.
1,0	Configuration Cycle Type ID. 00 = Type 0 01 = Type 1

PCI Configuration Data Register
I/O Port 0CFCh, R/W access (8-, 16-, 32-bit)

Bit	Function
31..0	Configuration Data.

Figure 4-2 shows how the loading of 0CF8h results in a Type 0 configuration cycle on the PCI bus. The Device Number (bits <15..11> determines which one of the AD31..11 lines is to be asserted high for the IDSEL signal, which acts as a "chip select" function for the PCI device to be configured.

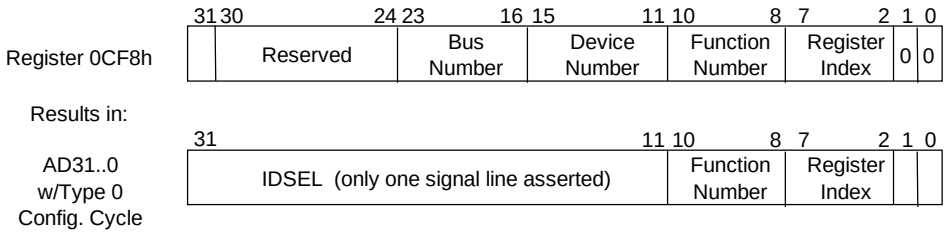


Figure 4–3. Type 0 Configuration Cycle

Systems in a standard configuration will run only Type 0 configuration cycles since only one PCI bus is present. Table 4-3 shows the device numbers and IDSEL connections for the PCI devices.

Table 4-3.
PCI Device Configuration Access

PCI Device	Device No. (CF8h <15..11>)	IDSEL Wired to:
Support Chipset:		
Pentium-Based System		
82439 (TXC)	0	AD11
82371 (PIIX3)	7	AD18
Pentium Pro-Based System		
82441 (PMC)	0	AD11
82371 (PIIX3)	7	AD18
Graphics Controller:		
Pentium-Based System (integrated)	15	AD26
Pentium Pro-based system (PCI card)	(slot x)	(slot x)
PCI Connector (slot 1)	2	AD13
PCI Connector (slot 2)	3	AD14
PCI Connector (slot 3)	4	AD15

The function number (CF8h, bits <10..8>) is used to select a particular function within a multifunction PCI device as shown in Table 4-4.

Table 4-4.
PCI Function Configuration Access

PCI Function	Device No.	Function No.
Host/PCI Bridge	0	0
PCI/ISA Bridge	7	0
EIDE Interface	7	1
USB Function	7	2

The register index identifies the 32-bit location within the configuration space of the PCI device to be accessed. All PCI devices can contain up to 256 bytes of configuration data (see Figure 4-4), of which the first 64 bytes comprise the configuration space header.

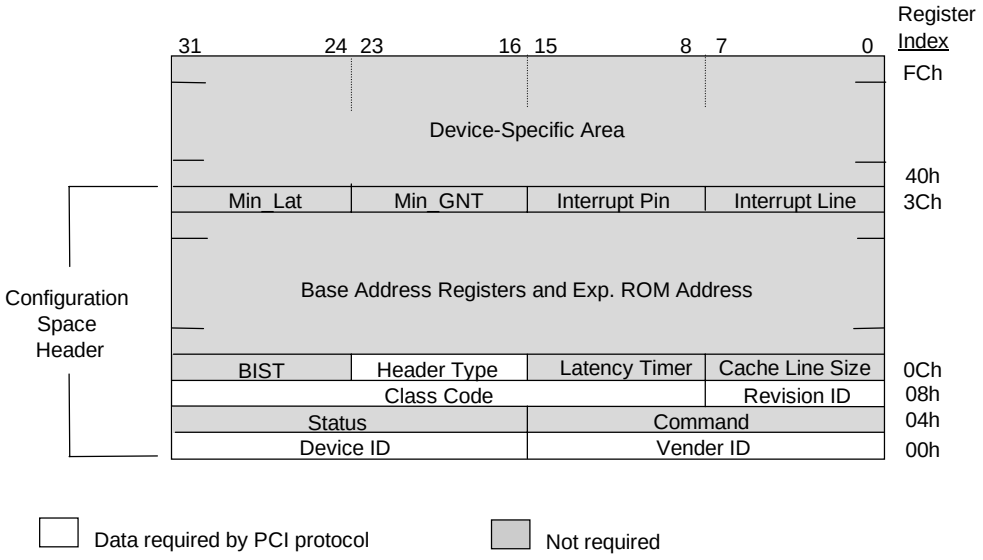


Figure 4–4. PCI Configuration Space Map

Each PCI device is identified with a vender ID (assigned to the vender by the PCI Special Interest Group) and a device ID (assigned by the vender). The device and vender IDs for the devices used in these systems are listed in Table 4-5.

Table 4-5.
PCI Device Identification

PCI Device	Vender ID	Device ID
Support Chipset:		
Pentium-Based System		
82439 (TXC)	8086h	1250h
82371 (PIIX3)	8086h	7000h
Pentium Pro-Based System		
82441 (PMC)	8086h	1237h
82371 (PIIX3)	8086h	7000h
Graphics Controller:		
Pentium-Based System	1013h	00A8h
Cirrus Logic GD5446-based Card	1013h	00B8h
Matrox Millennium Card	102Bh	0519h

4.2.4.3 Special Cycles

There are two types of special cycles that may occur on the PCI bus. The first type iS initiated by the host and is used to perform the following functions: Shutdown, Flush, Halt, Write Back, Flush Acknowledge, Branch Trace Message, and Stop/Grant. These cycles start like all other PCI cycles and terminate with a master abort.

The second type of special cycle is initiated by writing to 0CF8h, Bus # = all 0s, Device = all 1s, Function # all 1s, and Register = all 0s) and 0CFCh to generate a Type 0 configuration cycle. This type 0 cycle, however, does not assert any of the IDSEL lines and therefore results in a master abort with FFFFh returned to the microprocessor.

4.2.5 OPTION ROM MAPPING

During POST, the PCI bus is scanned for devices that contain their own specific firmware in ROM. Such option ROM data, if detected, is loaded into system memory's DOS compatibility area (refer to the system memory map shown in chapter 3).

4.2.6 PCI CONFIGURATION

PCI bus operations, especially those that require ISA bus interaction, require the configuration of certain parameters such as PCI IRQ routing, top of memory accessable by ISA, SMI generation, and clock throttling characteristics. These parameters are handled by the PCI/ISA bridge function (PCI function #0)of the 82371 component and configured through the PCI configuration space registers listed in Table 4-6. Configuration is provided by BIOS at power-up but re-configurable by software.

Table 4-6.
PCI/ISA Bridge Configuration Registers

PCI Config. Addr.	Register	Reset Value	PCI Config. Addr.	Register	Reset Value
00-01h	Vender ID	8086h	69h	Top of Memory	02h
02-03h	Device ID	7000h	6A-6Bh	Miscellaneou Status	xxh
04-05h	PCI Command	0007h	70h	Sys. Bd. IRQ0 Route Cntrl.	80h
06-07h	PCI Status	0280h	76h	Sys. Bd. DMA Config. 0	04h
08h	Revision ID	00h	77h	Sys. Bd. DMA Config. 1	04h
09h	Programming I/F	00h	78-79h	Chip Select Control	0002h
0Ah	Sub Class Code	01h	80h	APIC Base Addr. Relocater	00h
0Bh	Base Class Code	06h	82h	Deterministic Latency Cntrl.	00h
0Eh	Header Type	80h	A0h	SMI Control	08h
4Ch	ISA I/O Recovery Timer	4Dh	A2-A3h	SMI Enable	0000h
4E-4Fh	X-Bus Chip Select En.	0003h	A4-A7h	System Event Enable	All 0's
60h	PIRQ0 Route Cntl.	80h	A8h	Fast-Off timer	0Fh
61h	PIRQ1 Route Cntl.	80h	AA-ABh	SMI Request	0000h
62h	PIRQ2 Route Cntl.	80h	ACh	Clock Throttle Timer (Low)	00h
63h	PIRQ3 Route Cntl.	80h	AEh	Clock Throttle Timer (High)	00h

4.3 ISA BUS OVERVIEW

NOTE: This section describes the ISA bus in general and highlights bus implementation in this particular system. For detailed information regarding ISA bus operation, refer to the *Compaq Extended Industry Standard Architecture (EISA) Technical Reference Guide*.

The industry standard architecture (ISA) bus provides an 8-/16-bit path for standard I/O peripherals as well as for optional devices that can be installed in the ISA expansion slots. Figure 4-5 shows the key functions and devices that reside on the ISA bus.

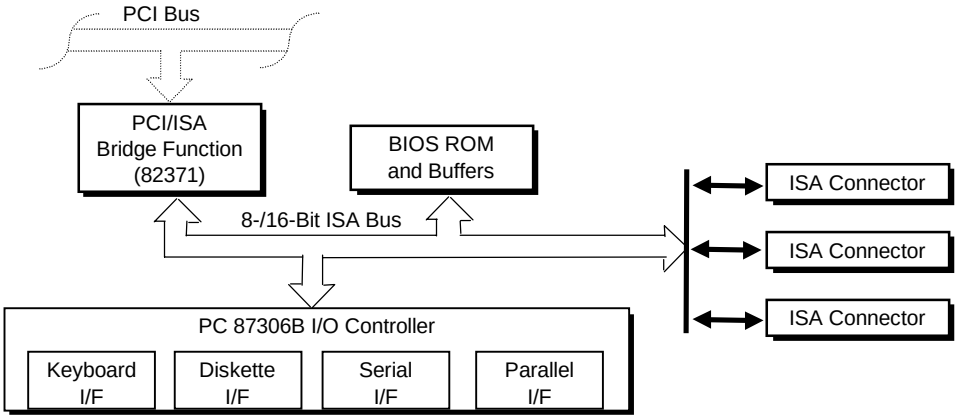


Figure 4–5. Compaq Deskpro 2000 Series ISA Bus Devices and Functions

4.3.1 ISA SLOT DESCRIPTIONS

Slot 1 Standard 16-bit ISA connector with all common ISA signals.

Slot 2 Standard 16-bit ISA connector with all common ISA signals.

Slot 3 Standard 16-bit ISA connector with all common ISA signals.

4.3.2 ISA CONNECTOR

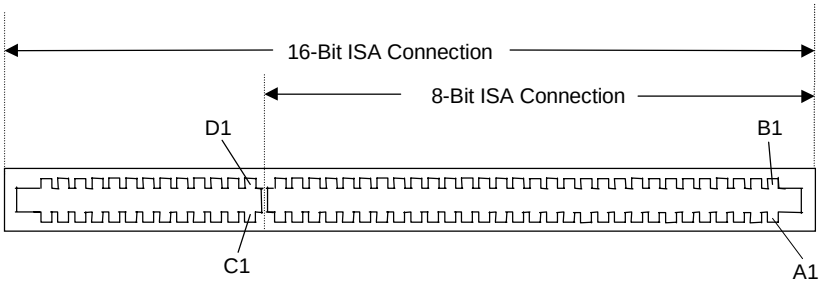


Figure 4–6. ISA Expansion Connector

Table 4-7.
ISA Expansion Connector Pinout

8-Bit ISA Interface				16-Bit ISA Interface			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
B01	GND	A01	I/O CHK-	D01	M16-	C01	SBHE-
B02	RESDRV	A02	SD7	D02	I/O16-	C02	LA23
B03	+5 VDC	A03	SD6	D03	IRQ10	C03	LA22
B04	IRQ9	A04	SD5	D04	IRQ11	C04	LA21
B05	-5 VDC	A05	SD4	D05	IRQ12	C05	LA20
B06	DRQ2	A06	SD3	D06	IRQ15	C06	LA19
B07	-12 VDC	A07	SD2	D07	IRQ14	C07	LA18
B08	NOWS-	A08	SD1	D08	DAK0-	C08	LA17
B09	+12 VDC	A09	SD0	D09	DRQ0	C09	MRDC-
B10	GND	A10	BUSRDY	D10	DAK5-	C10	MWTC-
B11	SMWTC-	A11	DMA	D11	DRQ5	C11	SD8
B12	SMRDC-	A12	SA19	D12	DAK6-	C12	SD9
B13	IOWC-	A13	SA18	D13	DRQ6	C13	SD10
B14	IORC-	A14	SA17	D14	DAK7-	C14	SD11
B15	DAK3-	A15	SA16	D15	DRQ7	C15	SD12
B16	DRQ3	A16	SA15	D16	+5 VDC	C16	SD13
B17	DAK1	A17	SA14	D17	GRAB-	C17	SD14
B18	DRQ1	A18	SA13	D18	GND	C18	SD15
B19	REFRESH-	A19	SA12				
B20	BCLK	A20	SA11				
B21	IRQ7	A21	SA10				
B22	IRQ6	A22	SA9				
B23	IRQ5	A23	SA8				
B24	IRQ4	A24	SA7				
B25	IRQ3	A25	SA6				
B26	DAK2-	A26	SA5				
B27	T-C	A27	SA4				
B28	BALE	A28	SA3				
B29	+5 VDC	A29	SA2				
B30	OSC	A30	SA1				
B31	GND	A31	SA0				

4.3.3 ISA BUS OPERATION

The ISA bus supports 8- and 16-bit transfers at an 8-MHz rate. Devices limited to 8-bit transfers use the lower byte portion (data lines 7..0) while 16-bit transfers use the full bandwidth (data lines 15..0). Addressing is handled by two classifications of address signals: latched and latchable. Latched address signals (SA19..0) select the specific byte within the 1-MB section of memory defined by address lines LA23..17. Latchable address lines (LA23..17) provide a longer setup time for pre-chip selection or for pre-address decoding for high-speed memory and allow access to up to 16-MB of physical memory on the ISA bus. The SA19..17 signals have the same values as the LA19..17 signals for all memory cycles. The I/O cycles use only the SA15..0 signals.

The key control signals are described as follows:

- MRDC- (Memory Read Cycle): MRDC- is active on all ISA memory reads accessing memory from 000000h to FFFFFFh.
- SMEMR- (System Memory Read): SMEMR- is asserted by the PCI/ISA bridge to request an ISA memory device to drive data onto the data lines for accesses below one megabyte. SMEMR- is a delayed version of MRDC-.
- MWTC- (Memory Write Cycle): MWTC- is active on all ISA memory write cycles accessing memory from 000000h to FFFFFFh.
- SMEMW- (System Memory Write): SMEMW- is asserted by the PCI/ISA bridge to request an ISA memory device to accept data from the data lines for access below one megabyte. SMEMW- is a delayed version of MWTC-.
- IORC- (Input/Output Read Cycle): IORC- commands an ISA I/O device to drive data onto the data lines.
- IOWC- (Input/Output Write Cycle): IOWC- commands an ISA I/O device to accept data from the data lines.
- SBHE- (System Byte High Enable): SBHE- indicates that a byte is being transferred on the upper half (D15..8) of the data lines.
- SA0- (System Address Bit <0>): This bit is the complement of SBHE- and indicates that a byte is being transferred on the lower half (D7..0) of the data lines.
- M16- (16-bit Memory Cycle): M16- is asserted by 16-bit ISA devices to indicate 16-bit memory cycle capability.
- IO16- (16-bit I/O Cycle): IO16- is asserted by 16-bit ISA devices to indicate 16-bit I/O cycle transfer capability.

If the address on the SA lines is above one megabyte, SMRDC- and SMWTC- will not be active. The MRDC- and MWTC- signals are active for memory accesses up to 16 megabytes and can be used by any device that uses the full 16-bit ISA bus. To request a 16-bit transfer, a device asserts either the M16- (memory) or IO16- (I/O) signal when the device is addressed.

When another device (such as a DMA device or another bus master) takes control of the ISA, the Bus Address Latch Enable (BALE) signal is held active for the duration of the operation. As a result , signals LA23..17 are always enabled and must be held stable for the duration of each bus cycle.

When the address changes, devices on the bus may decode the latchable address (LA23..17) lines and then latch them. This arrangement allows devices to decode chip selects and M16- before the next cycle actually begins.

The following guidelines apply to optional ISA devices installed in the system:

- On bus lines that can be driven by a controller board, the driver should be able to sink a minimum of 20 ma at 0.5 VDC and source 2 ma at 3.75 VDC.
- On bus lines that are driven in the low direction only (open collector), the driver should be able to sink 20 ma at 0.5 VDC.
- The load on any logic line from a single bus slot should not exceed 2.0 ma in the low state (at 0.5 VDC) or 0.1 ma in the high state (at 3.75 VDC).
- The logic-high voltage at the bus ranges from 3.75 VDC to 5.5 VDC. The logic low voltage ranges from 0 VDC to 0.8 VDC.

4.3.4 ISA CONFIGURATION

The working relationship between the PCI and ISA buses requires that certain parameters be configured. The PC/ISA bridge function of the 82371 includes configuration registers to set parameters such as PCI IRQ routing and top-of-memory available to ISA/DMA devices. These parameters are programmed by BIOS during power-up, using registers listed previously in Table 4-6.

4.4 DIRECT MEMORY ACCESS

Direct Memory Access (DMA) is a method by which an ISA device accesses system memory without involving the microprocessor. DMA is normally used to transfer blocks of data to or from an ISA I/O device. DMA reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks.

> **NOTE:** This section describes DMA in general. For detailed information regarding DMA operation, refer to the *Compaq Extended Industry Standard Architecture (EISA) Technical Reference Guide*. Note, however, that EISA enhancements as described in the referenced document are not supported in this (ISA only) system.

The 82371 controller includes the equivalent of two 8237 DMA controllers cascaded together to provide eight DMA channels. Table 4-8 lists the default configuration of the DMA channels.

Table 4-8.
Default DMA Channel Assignments

DMA Channel	Device ID
Controller 1 (byte transfers)	
0	Spare & ISA conn. pins D8, D9
1	Spare & ISA conn. pins B17, B18
2	Diskette drive & ISA conn. pins B6, B26
3	ECP LPT1 & ISA conn. pins B15, B16
Controller 2 (word transfers)	
4	Cascade for controller 1
5	Spare & ISA conn. pins D10, D11
6	Spare & ISA conn. pins D12, D13
7	Spare & ISA conn. pins. D14, D15

All channels in DMA controller 1 operate at a higher priority than those in controller 2. Note that channel 4 is not available for use other than its cascading function for controller 1. The DMA controller 2 can transfer words only on an even address boundary. The DMA controller and page register define a 24-bit address that allows data transfers within the address space of the CPU. The DMA controllers operate at 8 MHz.

4.4.1 DMA CONTROLLER ACCESS

The DMA logic is accessed through two types of I/O mapped registers; page registers and controller registers. The mapping is the same regardless of the support chipset used.

4.4.1.1 Page Registers

The DMA page register contains the eight most significant bits of the 24-bit address and works in conjunction with the DMA controllers to define the complete (24-bit)address for the DMA channels. Table 4-9 lists the page register port addresses.

Table 4-9.
DMA Page Register Addresses

DMA Channel	Page Register I/O Port
Controller 1 (byte transfers)	
Ch 0	087h
Ch 1	083h
Ch 2	081h
Ch 3	082h
Controller 2 (word transfers)	
Ch 4	n/a
Ch 5	08Bh
Ch 6	089h
Ch 7	08Ah
Refresh	08Fh [see note]

NOTE:
The DMA memory page register for the refresh channel must be programmed with 00h for proper operation.

The memory address is derived as follows:

24-Bit Address - Controller 1 (Byte Transfers)

8-Bit Page Register	8-Bit DMA Controller
A23..A16	A15..A00

24-Bit Address - Controller 2 (Word Transfers)

8-Bit Page Register	16-Bit DMA Controller
A23..A17	A16..A01, (A00 = 0)

Note that address line A16 from the DMA memory page register is disabled when DMA controller 2 is selected. Address line A00 is not connected to DMA controller 2 and is always 0 when word-length transfers are selected.

By not connecting A00, the following applies:

- The size of the the block of data that can be moved or addressed is measured in 16-bits (words) rather than 8-bits (bytes).
- The words must always be addressed on an even boundary.

DMA controller 1 can move up to 64 Kbytes of data per DMA transfer. DMA controller 2 can move up to 64 Kwords (128 Kbytes) of data per DMA transfer. Word DMA operations are only possible between 16-bit memory and 16-bit peripherals.

The RAM refresh is designed to perform a memory read cycle on each of the 512 row addresses in the DRAM memory space. Refresh operations are used to refresh memory on the 32-bit memory bus and the ISA bus. The refresh address is provided on lines SA00 through SA08. Address lines LA23..17, SA18,19 are driven low.

The remaining address lines are in an undefined state during the refresh cycle. The refresh operations are driven by a 69.799-KHz clock generated by Interval Timer 1, Counter 1. The refresh rate is 128 refresh cycles in 2.038 ms.

4.4.1.2 DMA Controller Registers

Table 4-10 lists the DMA Controller Registers and their I/O port addresses. Note that there is a set of registers for each DMA controller.

Table 4-10.
DMA Controller Registers

Register	Controller 1	Controller 2	R/W
Status	008h	0D0h	R
Command	008h	0D0h	W
Mode	00Bh	0D6h	W
Write Single Mask Bit	00Ah	0D4h	W
Write All Mask Bits	00Fh	0DEh	W
Software DRQx Request	009h	0D2h	W
Base and Current Address - Ch 0	000h	0C0h	W
Current Address - Ch 0	000h	0C0h	R
Base and Current Word Count - Ch 0	001h	0C2h	W
Current Word Count - Ch 0	001h	0C2h	R
Base and Current Address - Ch 1	002h	0C4h	W
Current Address - Ch 1	002h	0C4h	R
Base and Current Word Count - Ch 1	003h	0C6h	W
Current Word Count - Ch 1	003h	0C6h	R
Base and Current Address - Ch 2	004h	0C8h	W
Current Address - Ch 2	004h	0C8h	R
Base and Current Word Count - Ch 2	005h	0CAh	W
Current Word Count - Ch 2	005h	0CAh	R
Base and Current Address - Ch 3	006h	0CCh	W
Current Address - Ch 3	006h	0CCh	R
Base and Current Word Count - Ch 3	007h	0CEh	W
Current Word Count - Ch 3	007h	0CEh	R
Temporary (Command)	00Dh	0DAh	R
Reset Pointer Flip-Flop (Command)	00Ch	0D8h	W
Master Reset (Command)	00Dh	0DAh	W
Reset Mask Register (Command)	00Eh	0DCh	W

NOTE:
For a detailed description of the DMA registers, refer to the *Compaq EISA Technical Reference Guide*.

4.5 INTERRUPTS

The microprocessor uses two types of interrupts; maskable and nonmaskable. A maskable interrupt can be enabled or disabled within the microprocessor by the use of the STI and CLI instructions. A nonmaskable interrupt cannot be masked off within the microprocessor but may be inhibited by hardware or software means external to the microprocessor.

4.5.1 MASKABLE INTERRUPTS

The maskable interrupt is a hardware-generated signal used by peripheral functions within the system to get the attention of the microprocessor. Each peripheral function produces a unique IRQn signal that is routed to interrupt processing logic that asserts the interrupt (INTR) input to the microprocessor. The microprocessor halts execution to determine the source of the interrupt and then services the peripheral as appropriate.

The interrupt (IRQn) processing function is provided by the 82371 component in all Deskpro 2000 systems. The 82371includes the equivalent of two 8259 interrupt controllers cascaded together to handle the standard AT-type (ISA) interrupt signals IRQ0-15. Table 4-11 lists the possible sources for maskable interrupts and their priorities. The highest priority (lowest number) is processed first.

Table 4-11.
Maskable Interrupt Priorities and Assignments

Priority	Signal Label	Controller	Source (Typical)
1	IRQ0	1	Interval timer 1, counter 0
2	IRQ1	1	Keyboard
3	IRQ8-	1	Real-time clock
4	IRQ9	2	Spare and ISA connector pin B04
5	IRQ10	2	Spare and ISA connector pin D03
6	IRQ11	2	Spare and ISA connector pin D04
7	IRQ12	2	Mouse and ISA connector pin D05
8	IRQ13	2	Coprocessor (math)
9	IRQ14	2	IDE primary I/F and ISA connector pin D07
10	IRQ15	2	IDE secondary I/F and ISA connector pin D06
11	IIRQ3	2	Spare and ISA connector pin B25
12	IRQ4	1	Serial port (COM1) and ISA connector pin B24
13	IRQ5	1	Parallel port (LPT1) and ISA connector pin B23
14	IRQ6	1	Diskette drive controller and ISA connector pin B22
15	IRQ7	1	Spare
--	IRQ2	1	NOT AVAILABLE (Cascade from interrupt controller 2)

IRQ Mapping Options:

PCI interrupts: Refer to following text.
Parallel Port: IRQ5,7,9,10,11,14, or 15

NOTE: Interrupts generated by devices on the PCI bus (PIRQn) can be configured to share specific IRQn lines with ISA peripherals. This routing function is controlled through PCI configuration registers 60h-63h (function 0 of the 82371) for PIRQA-PIRQD respectively. In this system the default configuration disables PIRQn routing.

Interrupt processing is controlled and monitored through standard AT-type I/O-mapped registers. These registers are listed in Table 4-12.

Table 4-12.
Maskable Interrupt Control Registers

I/O Port	Register
020h	Base Address, Int. Cntlr. 1
021h	Initialization Command Word 2-4, Int. Cntlr. 1
0A0h	Base Address, Int. Cntlr. 2
0A1h	Initialization Command Word 2-4, Int. Cntlr. 2

The initialization and operation of the interrupt control registers follows standard AT-type protocol. For a detailed description of maskable interrupt operation refer to the Compaq Extended Industry Standard Architecture Expansion Bus Technical Reference Guide. Note that extended (EISA) interrupt functionality is not supported in this system.

Interrupts generated by PCI devices can be configured to share the standard AT (IRQn) interrupt lines. Configuration is through PCI configuration registers 60h-63h for PIRQA through PIRQD respectively. The default configuration has PIRQn routing disabled.

PCI Config. Reg. (Device 7, Function 0) 60h-63h PIRQA-PIRQD Routing
Default Value = 80h (all locations)

Bit	Function	
7	Interrupt Routing Enable; 0 = Enable 1 = Disable (default)	
6..4	Reserved - read 0's	
3..0	Interrupt Routing: 0000 = Reserved 0001 = Reserved 0010 = Reserved 0011 = IRQ3 0100 = IRQ4 0101 = IRQ5 0110 = IRQ6 0111 = IRQ7	 1000 = Reserved 1001 = IRQ9 1010 = IRQ10 1011 = IRQ11 1100 = IRQ12 1101 = Reserved 1110 = IRQ14 1111 = IRQ15

4.5.2 NONMASKABLE INTERRUPTS

Nonmaskble interrupts cannot be masked (inhibited) within the microprocessor itself but may be maskable by software using logic external to the microprocessor. There are two nonmaskable interrupt signals: the NMI- and the SMI-. These signals have service priority over all maskable interrupts, with the SMI- having top priority over all interrupts including the NMI-.

4.5.2.1 NMI- Generation

The Non-Maskable Interrupt (NMI-) signal is caused by:

- Parity errors on any ISA expansion boards that pull the IOCHK- line low.
- Parity errors detected on the PCI bus.

The NMI Status Register at I/O port 061h contains NMI source and status data as follows:

NMI Status Register 61h

Bit	Function
7	NMI Status: 0 = No NMI from system board parity error. 1 = NMI requested, read only
6	IOCHK- NMI: 0 = No NMI from IOCHK- 1 = IOCHK- is active (low), NMI requested, read only
5	Interval Timer 1, Counter 2 (Speaker) Status
4	Refresh Indicator (toggles with every refresh)
3	IOCHK- NMI Enable/Disable: 0 = NMI from IOCHK- enabled 1 = NMI from IOCHK- disabled and cleared (R/W)
2	System Board Parity Error NMI Enable: 0 = Parity error NMI enabled 1 = Parity error NMI disabled and cleared (R/W)
1	Speaker Data (R/W)
0	Inteval Timer 1, Counter 2 Gate Signal (R/W) 0 = Counter 2 disabled 1 = Counter 2 enabled

Functions not related to NMI activity.

After the active NMI has been processed, status bits <7> or <6> are cleared by pulsing bits <2> or <3> respectively.

The NMI Enable Register (070h, <7>) is used to enable/disable the NMI signal. Writing 80h to this register masks generation of the NMI-.

> **NOTE:** The lower six bits of register at I/O port 70h affect RTC operation and should be considered when changing NMI- generation status.

4.5.2.2 SMI- Generation

The SMI- (System Management Interrupt) is typically used for power management functions. When power management is enabled, inactivity timers are monitored. When a timer times out, SMI- is asserted and invokes the microprocessor's SMI handler. The SMI- handler works with the APM BIOS to service the SMI- according to the cause of the timeout.

The SMI- is also generated by the user invoking the Quicklock feature, even though this function is not considered a power management function.

4.6 INTERVAL TIMER

The interval timer generates pulses at software (programmable) intervals. A 8254-compatible timer is integrated into the support chip that provides the PCI/ISA bridge function. The timer function provides three counters, the functions of which are listed in Table 4-13.

Table 4-13.
Interval Timer Functions

Counter	Function	Gate	Clock In	Clock Out
0	System Clock	Always on	1.193 MHz	IRQ0
1	Refresh	Always on	1.193 MHz	Refresh Req.
2	Speaker Tone	Port 61, bit<0>	1.193 MHz	Speaker Input

The interval timer is controlled through the I/O mapped registers listed in Table 4-14.

Table 4-14.
Interval Timer Control Registers

I/O Port	Register
040h	Read or write value, counter 0
041h	Read or write value, counter 1
042h	Read or write value, counter 2
043h	Control Word

Interval timer operation follows standard AT-type protocol. For a detailed description of timer registers and operation, refer to the *Compaq Extended Industry Standard Architecture Expansion Bus Technical Reference Guide.*

4.7 SYSTEM CLOCK DISTRIBUTION

The system uses an ICS9159-14 or compatible part for generation of most clock signals. Table 4-15 lists the clock signals and to which components they are distributed.

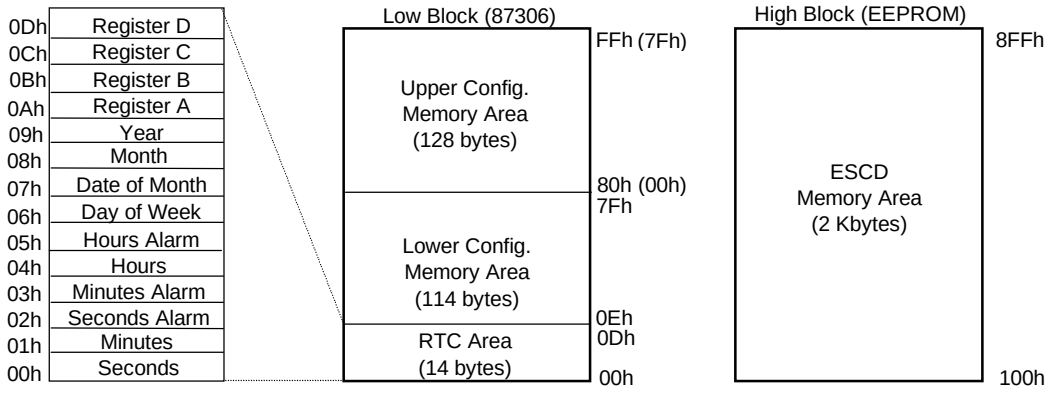
Table 4-15.
Clock Generation and Distribution

Signal	Source	Destination
25, 30, 33*, 50, 60, 66*, MHz	ICS9159	CPU, 82441, 82442, 82430, 82371, PCI slots
48 MHz	"	82371
24 MHz	"	87306
14.31818 MHz	"	82371, GD5436, ISA slots
8 MHz (BCLK)	82371	ISA slots
32 KHz	Crystal	87306

* Depending on CPU configuration.

4.8 REAL-TIME CLOCK AND CONFIGURATION MEMORY

The Real-time clock (RTC) and configuration memory (also referred to as CMOS) are integrated into the PC87306 I/O controller used in all models. The RTC uses the first 14 of 256 bytes of configuration memory and is MC146818-compatible. Figure 4-7 shows the configuration memory mapping.



NOTE: Addresses in parenthesis ( ) should be used if accessing using conventional OUT/IN instructions.

Figure 4–7. Configuration Memory Map

As indicated above, the 87306 controller provides 256 bytes of configuration memory, divided into two banks. In addition, a 2-KB EEPROM provides additional non-volatile storage of Extended System Configuration Data (ESCD). The 2-KB EEPROM is accessed through the 87306's GPIO15 (CLK), 14 (data) pins using the I²C interface protocol.

The RTC/configuration memory is I/O mapped and can be accessed using conventional OUT and IN assembly language instructions. This method requires accessing I/O ports 398h/399h (the 87306's Configuration Register access ports) to select the lower or upper configuration memory area of the 87306 and then using I/O ports 70h/71h.

The BIOS function INT15, AX=E823h is the preferred method for accessing the RTC/configuration memory. This function is described as follows:

INPUT:

AX = E823h
BH = 0, Read
1, Write
BL = Value to write if BH = 1
CX = 00h-FFh, Low configuration memory block
100h-8FFh, High configuration memory block

OUTPUT (if successful):

AL = Byte data if a read
CF = 0

A 3-VDC battery is used for maintaining the RTC and configuration memory while the system is powered down. This battery is soldered on the system board and is designed to last from 5-7 years. Once expired, the soldered battery is by-passed by connecting a replacement battery (Compaq p/n 160274-001 or equivalent 4.5 VDC @ 660 ma alkaline battery) to header E50 (586-based) or P24 (Pentium Pro-based) pins 9-12.

4.8.1 CONFIGURATION MEMORY BYTE DEFINITIONS

Table 4-16 lists the mapping of the configuration memory.

Table 4-16.
Configuration Memory (CMOS) Map

Location	Function	Location	Function
00-0Dh	Real-rime clock	40h- 42h	Super Ext. Mem. Tested Good
0Eh	Diagnostic status	43h	Microprocessor ID
0Fh	System reset code	44h	Microprocessor revision
10h	Diskette drive type	45h	SW SMI command byte
11h	Reserved	46h	SW SMI data byte
12h	Hard drive type	47h	APM command
13h	Security functions	4Bh	SIMM information
14h	Equipment installed	4Ch	Reserved
15h	Base memory size, low byte/KB	4Dh-4Fh	POST error logging
16h	Base memory size, high byte/KB	50h, 51h	Super Ext. Mem. configured
17h	Extended memory, low byte/KB	52h	Miscellaneous configuration byte
18h	Extended memory, high byte/KB	53h	PCI configuration byte
19h	Hard drive 1, primary controller	54h-5Bh	Reserved
1Ah	Hard drive 2, primary controller	5Ch	Mode 2 configuration byte
1Bh	Hard drive 1, secondary controller	5Dh	ESS audio configuration byte
1Ch	Hard drive 2, secondary controller	5Eh	Reserved
1Dh	Enhanced hard drive support	5Fh-6Fh	Asset tag serial number
1Eh	Reserved	70h-74h	Custom drive type 65
1Fh	Power management functions	75h-79h	Custom drive type 66
20h-23h	Reserved	7Ah-7Eh	Custom drive type 68
24h	System board ID	7Fh-83h	Custom drive type 15
25h	System architecture data	84h-85h	Reserved
26h	Auxiliary peripheral configuration	86h-96h	System board PnP support
27h	Speed control external drive	97h	Auto setup test byte
28h	Expanded/base mem. size, IRQ12	98h-9Dh	Reserved
29h	Miscellaneous configuration	9Eh, 9Fh	Checksum of locations 50h-5Dh
2Ah	Hard drive timeout	A0h-A5h	Manufacturing diagnostic data
2Bh	System inactivity timeout	A6h-BFh	Reserved
2Ch	Monitor timeout, Num Lock Cntrl	C0h-DFh	Client Management error log
2Dh	Additional flags	E0h-F1h	Backup serial number
2Eh-2Fh	Checksum of locations 10h-2Dh	F2h	ROM internal use
30h-31h	Total extended memory tested	F3h-F7h	Reserved
32h	Century	F8h-FFh	Administrator password
33h	Miscellaneous flags set by BIOS	100h-111h	Chassis serial number
34h	International language	112h-115h	BIOS boot spec (IPL order)
35h	APM status flags	116h-119h	BIOS boot spec (BCV order)
37h-3Fh	Power-on password	11Ah-8FFh	PCI and ISA PnP ESCD data

NOTE: Assume unmarked gaps are reserved.

The configuration memory can be zero'ed out by BIOS when GPIO23 indicates such action is necessary. This bit reads 1 when normal and 0 when configuration memory can be cleared. The following pages provide individual descriptions for the registers. Default values (where applicable) are given for a standard system as shipped from the factory. The contents of configuration memory can be cleared by moving the jumper on header E50 (Pentium-based) or P24 (Pentium Pro-based) pins 1,2 to pins 2,3.

RTC Control Register A, Byte 0Ah

Bit	Function
7	Update in Progress. Read only. 0 = Time update will not occur before 2444 us 1 = Time update will occur within 2444 us
6..4	Divider Chain Control. R/W. 00x = Oscillator disabled. 010 = Normal operation (time base frequency = 32.768 KHz). 11x = Divider chain reset.
3..0	Periodic Interrupt Control. R/W. Specifies the periodic interrupt interval. 0000 = none 1000 = 3.90625 ms 0001 = 3.90625 ms 1001 = 7.8125 ms 0010 = 7.8125 ms 1010 = 15. 625 ms 0011 = 122.070 us 1011 = 31.25 ms 0100 = 244.141 us 1100 = 62.50 ms 0101 = 488.281 us 1101 = 125 ms 0110 = 976.562 us 1110 = 250 ms 0111 = 1.953125 ms 1111 = 500 ms

RTC Control Register B, Byte 0Bh

Bit	Function
7	Time Update Enable/disable 0 = Normal operation, 1 = Disable time updating for time set
6	Periodic Interrupt Enable/Disable. 0 = Disable, 1 = Enable interval specified by Register A
5	Alarm Interrupt Enable/disable 0 = Disabled, 1 = Enabled
4	End-of-Update Interrupt Enable/Disable 0 = Disabled, 1 = Enabled
3	Reserved (read 0)
2	Time/Date Format Select 0 = BCD format, 1 = Binary format
1	Time Mode 0 = 12-lhour mode, 1 = 24-hour mode
0	Automatic Daylight Savings Time Enable/Disable 0 = Disable 1 = Enable (Advance 1 hour on 1st Sunday in April, retreat 1 hour on last Sunday in October).

RTC Status Register C, Byte 0Ch

Bit	Function
7	If set, interrupt output signal active (read only)
6	If set, indicates periodic interrupt flag
5	If set, indicates alarm interrupt
4	If set, indicates end-of-update interrupt
3..0	Reserved

RTC Status Register D, Byte 0Dh

Bit	Function
7	RTC Power Status 0 = RTC has lost power 1 = RTC has not lost power
6..0	Reserved

Configuration Byte 0Eh, Diagnostic Status

Default Value = 00h

This byte contains diagnostic status data.

Configuration Byte 0Fh, System Reset Code

Default Value = 00h

This byte contains the system reset code.

Configuration Byte 10h, Diskette Drive Type

Bit	Function
7..4	Primary (Drive A) Diskette Drive Type
3..0	Secondary (Drive B) Diskette Drive Type

Valid values for bits <7..4> and bits <3..0>:

0000 = Not installed
0001 = 360-KB drive
0010 = 1.2-MB drive
0011 = 720-KB drive
0100 = 1.44-MB/1.25-MB drive
0110 = 2.88-MB drive
(all other values reserved)

Configuration Byte 12h, Hard Drive Type

Bit	Function
7..4	Primary Controller 1, Hard Drive 1 Type: 0000 = none 1000 = Type 8 0001 = Type 1 1001 = Type 9 0010 = Type 2 1010 = Type 10 0011 = Type 3 1011 = Type 11 0100 = Type 4 1100 = Type 12 0101 = Type 5 1101 = Type 13 0110 = Type 6 1110 = Type 14 0111 = Type 7 1111 = other (use bytes 19h)
3..0	Primary Controller 1, Hard Drive 2 Type: 0000 = none 1000 = Type 8 0001 = Type 1 1001 = Type 9 0010 = Type 2 1010 = Type 10 0011 = Type 3 1011 = Type 11 0100 = Type 4 1100 = Type 12 0101 = Type 5 1101 = Type 13 0110 = Type 6 1110 = Type 14 0111 = Type 7 1111 = other (use bytes 1Ah)

Configuration Byte 13h, Security Functions

Default Value = 00h

Bit	Function
7	Reserved
6	QuickBlank Enable After Standby: 0 = Disable 1 = Enable
5	Administrator Password: 0 = Not present 1 = Present
4	Reserved
3	Diskette Boot Enable: 0 = Enable 1 = Disable
2	QuickLock Enable: 0 = Disable 1 = Enable
1	Network Server Mode/Security Lock Override: 0 = Disable 1 = Enable
0	Password State (Set by BIOS at Power-up) 0 = Not set 1 = Set

Configuration Byte 14h, Equipment Installed

Bit	Function
7,6	No. of Diskette Drives Installed: 00 = 1 drive 10 = Reserved 01 = 2 drives 11 = Reserved
5..2	Reserved
1	Coprocessor Present 0 = Coprocessor not installed 1 = Coprocessor installed
0	Diskette Drives Present 0 = No diskette drives installed 1 = Diskette drive(s) installed

Configuration Byte 15h and 16h, Base Memory Size

Bytes 15h and 16h hold a 16-bit value that specifies the base memory size in increments of 1-KB (1024) bytes. Valid base memory sizes are 512-KB and 640-KB.

Configuration Byte 17h and 18h, Extended Memory Size

Bytes 17h and 18h hold a 16-bit value that specifies the extended memory size in increments of 1-KB (1024) bytes.

Configuration Bytes 19h-1Ch, Hard Drive Types

Byte 19h contains the hard drive type for drive 1 of the primary controller if byte 12h bits <7..4> hold 1111b. Byte 1Ah contains the hard drive type for drive 2 of the primary controller if byte 12h bits <3..0> hold 1111b. Bytes1Bh and 1Ch contain the hard drive types for hard drives 1 and 2 of the secondary controller.

Configuration Byte 1Dh, Enhanced IDE Hard Drive Support

Default Value = F0h

Bit	Function
7	EIDE - Drive C (83h)
6	EIDE - Drive D (82h)
5	EIDE - Drive E (81h)
4	EIDE - Drive F (80h)
3..0	Reserved

Values for bits <7..4> :

0 = Disable

1 = Enable for auto-configure

Configuration Byte 1Fh, Power Management Functions

Default Value = 00h

Bit	Function
7..4	Reserved
3	Slow Processor Clock for Low Power Mode 0 = Processor runs at full speed 1 = Processor runs at slow speed
2	Reserved
1	Monitor Off Mode 0 = Turn monitor power off after 45 minutes in standby 1 = Leave monitor power on
0	Energy Saver Mode Blinking 0 = Disable 1 = Enable

Configuration Byte 24h, System Board Identification

Default Value = 7Eh

Configuration memory location 24h holds the system board ID.

Configuration Byte 25h, System Architecture Data

Default Value = 0Bh

Bit	Function
7..4	Reserved
3	Unmapping of ROM: 0 = Allowed 1 = Not allowed
2	Reserved
1,0	Diagnostic Status Byte Address 00 = Memory locations 80C00000h-80C00004h 01 = I/O ports 878h-87Ch 11 = neither place

Configuration Byte 26h, Auxiliary Peripheral Configuration

Default Value = 00h

Bit	Function
7,6	I/O Delay Select 00 = 420 ns (default) 01 = 300 ns 10 = 2600 ns 11 = 540 ns
5	Alternative A20 Switching 0 = Disable port 92 mode 1 = Enable port 92 mode
4	Reserved
3	Graphics Type 0 = Color 1 = Monochrome
2	Hard Drive Primary/Secondary Address Select: 0 = Primary 1 = Secondary
1,0	Reserved

Configuration Byte 27h, Speed Control/External Drive

Default Value = 00h

Bit	Function
7	Boot Speed 0 = Max MHz 1 = Fast speed
6..0	Reserved

Configuration Byte 28h, Expanded and Base Memory, IRQ12 Select

Default Value = 00h

Bit	Function
7	IRQ12 Select 0 = Mouse 1 = Expansion bus
6,5	Base Memory Size: 00 = 640 KB 01 = 512 KB 10 = 256 KB 11 = Invalid
4..0	Internal Compaq Memory: 00000 = None 00001 = 512 KB 00010 = 1 MB 00011 = 1.5 MB . . 11111 = 15.5 MB

Configuration Byte 29h, Miscellaneous Configuration Data

Default Value = 00h

Bit	Function
7..5	Reserved
4	Primary Hard Drive Enable (Non-PCI IDE Controllers) 0 = Disable 1 = Enable
3..0	Reserved

Configuration Byte 2Ah, Hard Drive Timeout

Default Value = 00h

Bit	Function
7..5	Reserved
4..0	Hard Drive Timeout 00000 = Disabled 00001 = 1 minute 00010 = 2 minutes . . 10101 = 21 minutes

Configuration Byte 2Bh, System Inactivity Timeout

Default Value = 41h

Bit	Function
7,6	Power Conservation Boot 00 = Reserved 01 = PC on 10 = PC off 11 = Reserved
5	Reserved
4..0	System Inactive Timeout. (Index to SIT system timeout record) 00000 = Disabled

Configuration Byte 2Ch, ScreenSave and NUMLOCK Control

Default Value = 01h

Bit	Function
7	Reserved for Use On Portables
6	Numlock Control 0 = Numlock off at power on 1 = Numlock on at power on
5..0	ScreenSave Timeout. (Index to SIT monitor timeout record) 000000 = Disabled

Configuration Byte 2Dh, Additional Flags

Default Value = 00h

Bit	Function
7..5	Reserved
4	Memory Test 0 = Test memory on power up only 1 = Test memory on warm boot
3	POST Error Handling (BIOS Defined) 0 = Display “Press F1 to Continue” on error 1 = Skip F1 message
2..0	Reserved

Configuration Byte 2Eh, 2Fh, Checksum

These bytes hold the checksum of bytes 10h to 2Dh.

Configuration Byte 30h, 31h, Total Extended Memory Tested

This location holds the amount of system memory that checked good during the POST.

Configuration Byte 32h, Century

This location holds the Century value in a binary coded decimal (BCD) format.

Configuration Byte 33h, Miscellaneous Flags

Default Value = 80h

Bit	Function
7	Memory Above 640 KB 0 = No, 1 = Yes
6	Reserved
5	Weitek Numeric Coprocessor Present: 0 = Not installed, 1 = Installed
4	Standard Numeric Coprocessor Present: 0 = Not installed, 1 = Installed
3..0	Reserved

Configuration Byte 34h, International Language Support

Default Value = 00h

Configuration Byte 35h, APM Status Flags

Default Value = 00h

Bit	Function
7..6	Power Conservation State: 00 = Ready 01 = Standby 10 = Suspend 11 = Off
5,4	Reserved
3	32-bit Connection: 0 = Disconnected, 1 = Connected
2	16-bit Connection 0 = Disconnected, 1 = Connected
1	Real Mode Connection 0 = Disconnected, 1 = Connected
0	Power Management Enable: 0 = Disabled 1 = Enabled

Configuration Byte 38h-3Fh, Power-On Password

These eight locations hold the power-on password.

Configuration Byte 41h, 42h, Total Super Extended Memory Tested

This byte holds the value of the amount of extended system memory that tested good during POST. The amount is given in 64-KB increments.

Configuration Byte 43h, 44h, Microprocessor Identification

These bytes hold the component ID and chip revision of the microprocesor.

Configuration Byte 45h, 46h, SW SMI Command/Data Bytes

Configuration Byte 47h, APM Command Byte

Configuration Byte E0h-F1h, Backup Chassis Serial Number

These 17 locations hold the chassis serial number.

Configuration Byte 4Bh, SIMM Information

Configuration Byte 4Dh-4Fh, POST Error Logging
Default Value = 00h (all locations)
These bytes hold the logging errors. When all bits are cleared, the bytes are ready to record errors.

Configuration Byte 50h, 51h, Total Super Extended Memory Configured

This byte holds the value of the amount of extended system memory that is configured. The amount is given in 64-KB increments.

Configuration Byte 52h, Miscellaneous Configuration Byte
Default Value = 00h

Bit	Function
7..5	Reserved
4	Diskette Write Enable 0 = Disable 1 = Enable
3..0	Reserved

Configuration Byte 53h, PCI Configuration Byte

Default Value = 00h

Bit	Function
7..2	Reserved
1	PCI Bus Master Enable 0 = Enabled 1 = Disabled
0	PCI VGA Palette Snoop 0 = Disable 1 = Enable

If palette snooping is enabled, then a primary PCI graphics card may share a common palette with the ISA graphics card. Palette snooping should only be enabled if all of the following conditions are met:

- An ISA card connects to a PCI graphics card through the VESA connector.
- The ISA card is connected to a color monitor.
- The ISA card uses the RAMDAC on the PCI card
- The palette snooping feature (sometimes called “RAMDAC shadowing”) on the PCI card is enabled and functioning properly.

Configuration Byte 5Ch, Mode-2 Configuration Byte

Default Value = 3Ch

Bit	Function
7,6	Reserved
5	Mode 2 Support 0 = Disable 1 = Enable
4	Secondary Hard Drive Controller 0 = Disable 1 = Enable
3,2	Secondary Hard Drive Controller IRQ 00 = IRQ10 01 = IRQ11 10 = IRQ12 11 = IRQ15
1,0	Reserved

Configuration Byte 5Dh, ESS Audio Configuration Byte

Default Value = 01h

Bit	Function
7	Reserved for Game Port Enable
6,5	Audio Address 00 = 22xh 01 = 23xh 10 = 24xh 11 = 25xh
4,3	DMA Channel 00 = Disabled 01 = DMA0 10 = DMA1 11 = DMA3
2,1	IRQ Select 00 = IRQ9 01 = IRQ5 10 = IRQ7 11 = IRQ10
0	ESS Audio Chip Enable 0 = Enabled 1 = Disabled

Configuration Byte 5Fh-6Fh, Asset Tag Serial Number

Configuration Bytes 70h-83h; Custom Hard Drive Information

These bytes contain the number of cylinders, heads, and sectors per track for hard drives C, D, E, and F respectively. The mapping for each drive is as follows:

Drive 65 (C)	Drive 66 (D)	Drive 68 (E)	Drive 15 (F)	Function
70h	75h	7Ah	7Fh	No. of Cylinders, Low Byte
71h	76h	7Bh	80h	No. of Cylinders, High Byte
72h	77h	7Ch	81h	No. of Heads
73h	78h	7Dh	82h	Max ECC Bytes
74h	79h	7eh	83h	No. of Sectors Per Track

Configuration Bytes 86h-96h; System Board PnP Support

These bytes contain information regarding Plug and Play support.

Configuration Byte 97h, Auto Setup Test Byte

Configuration Bytes 9Eh, 9Fh; Checksum of Locations 50h-5Dh

Configuration Byte A0h-A5h, Manufacturing Diagnostic Bytes

The data stored in this location is accessable with the INT 15, AX=E821h BIOS function.

Configuration Bytes C0h-DFh; Client Management Error Log

Configuration Bytes E0h, F1h, Backup Chassis Serial Number

Configuration Byte F2h, ESCD Caching Flag (Bit <0> Only, Others Reserved)

Configuration Bytes F8h-FFh, Administrator Password

Configuration Byte 100h, 111h, Chassis Serial Number

Configuration Byte 112h-115h, BIOS Boot Spec (Initial Program Load Order)

Configuration Byte 116h-119h, BIOS Boot Spec (Boot Connection Vector Order)

Configuration Byte 11Ah-8FFh, PCI and ISA PnP ESCD Storage Area

4.9 I/O MAP AND REGISTER ACCESSING

This section includes a list of the system I/O map and discusses the method of accessing indexed registers.

4.9.1 SYSTEM I/O MAP

NOTE: Assume that gaps in addresses are reserved and/or not used.

Table 4-17.
System I/O Map

Port	Function
0000..000Fh	DMA Controller 1
0020..0021h	Interrupt Controller 1
002E..002Fh	Reserved
0040..0043h	Timer 1
0044..0059h	Reserved
0060h	Keyboard Controller Data Byte
0061h	NMI, Speaker Control
0064h	Keyboard Controller Command/Status Byte
0070h	NMI Enable, RTC Address
0071h	RTC Data
0080..008Fh	DMA Page Registers
0092h	Port A, Fast A20/Reset
00A0..00A1h	Interrupt Controller 2
00B2h	APM Control Port
00B3h	APM Status Port
00C0..00DFh	DMA Controller 2
00E8h	General Purpose I/O Port 1
00E9h	General Purpose I/O Port 2
00EE..00EFh	Alternate Fast A20/Reset
00F0h	Math Coprocessor Busy Clear
00F1..016Fh	Reserved
0170..0177h	Hard Drive (IDE) Controller 2
01F0..01FFh	Hard Drive (IDE) Controller 1
0278..027Bh	Parallel Port (LPT2)
02F8..02FFh	Serial Port (COM2)
0371.. 0375h	Diskette Drive Controller Alternate Addresses
0376h	IDE Controller Alternate Address
0377h	IDE Controller Alternate Address, Diskette Drive Controller Alternate Address
0378..037Fh	Parallel Port (LPT1)
0398, 0399h	87306 Controller Configuration Registers (Index, Data)
03B0..03DFh	Graphics Controller
03E8..03EFh	Serial Port (COM3)
03F0..03F5h	Diskette Drive Controller Primary Addresses
03F6, 03F7h	Diskette Drive Controller Primary Addresses, Hard Drive Controller Primary Addresses
03F8..03FFh	Serial Port (COM1)
04D0..04D1h	Edge/Level INTR Control Register
0CF8h	PCI Configuration Address (dword access)
0CFCh	PCI Configuration Data (dword access)
FF00..FF07h	IDE Bus Master Register

4.9.2 87306 I/O CONTROLLER CONFIGURATION

The 87306 I/O controller contains various functions such as the keyboard interface, diskette interface, serial interface, and parallel interface. While the control of these interfaces uses standard AT-type I/O addressing, the configuration of these functions must be through indexed ports unique to the 87306. In this system, ports 0398h and 0399h are used for accessing the indexed configuration registers of the 87306 I/O controller.

Table 4-18 lists the indexed configuration registers of the 87306. In accessing an indexed configuration register, the index value is written to 0398h and the data is then either written to or read from port 0399h.

Table 4-18.
87306 I/O Controller
Indexed Configuration Registers

Index	Function
00h	Function Enable Register (Parallel/serial ports, diskette drive cntlr.)
01h	Function Address Register (parallel/serial ports)
02h	Power and Test Register (power down, serial port cntrl., config. lock, EPP/ECP cntrl.)
03h	Function Control Register
04h	Printer Control Register (parallel port, RTC)
05h	Keyboard and RTC Control Register
06h	Power Management Control Register
07h	Tape, UART and Parallel Port Register
08h	Super I/O Identification Register
09h	Advanced Super I/O Configuration Register
0Ah	Chip Select 0 Low Address Register
0Bh	Chip Select 0 Configuration Register
0Ch	Chip Select 1 Low Address Register
0Dh	Chip Select 1 Configuration Register
0Eh	Infrared Configuration Register
0Fh	GPIO Port Base Address Configuration Register
10h	Chip Select 0 High Address Register
11h	Chip Select 1 High Address Register
12h	Super I/O Configuration Register 0
18h	Super I/O Configuration Register 1
19h	LPT Base Address Configuration Register
1Bh	Plug ‘n Play Configuration Register 0
1Ch	Plug ‘n Play Configuration Register 1

4.10 BIOS ROM FUNCTIONS

> **NOTE:** This section describes BIOS in general and highlights BIOS functions unique to this particular system. For detailed information regarding the BIOS, refer to the *Compaq Basic Input/Output System Technical Reference Guide.*

The Basic Input/Output System (BIOS) of the computer is a collection of machine language programs stored as firmware in read-only memory (ROM). The BIOS controls the functions and utilities of the system such as:

- Execution of Power-On Self Test (POST)
- Initialization of the system, including chipset configuration code
- PCI bus functions
- Plug and Play functions
- Client Management functions
- APM functions
- Security features
- Setup Utility

The firmware contained in the BIOS ROM supports the following operating systems:

- DOS 6.2
- Windows 3.1
- Windows for Workgroups 3.11
- Windows 95
- Windows NT 3.5
- OS/2 ver 2.1
- OS/2 Warp
- SCO Unix

The microprocessor accesses the BIOS ROM as a 128-KB block from E0000h to FFFFFh. The BIOS data is shadowed in a 64-KB block in the upper memory area. The BIOS segments are dynamically paged in and out of the 64-KB block as they are needed.

4.10.1 SYSTEM IDENTIFICATION

The INT 15, AX=E800h BIOS function can be used to identify the system board. The system ID will be returned in the BX register as follows:

System	System ID
Pentium-based	0304h
Pentium Pro-based	030Ch

The INT 15 AX=E800h BIOS function points to the System Information Table (SIT). The SIT is a comprehensive list of fixed configuration information. Bytes 2 and 3 of SIT record 06h are the low and high order bytes (respectively) of the decimal value of the processor speed. Refer to the *Compaq Basic Input/Output System (BIOS) Technical Reference Guide* for more information on the SIT.

4.10.2 SETUP UTILITY

The ROM-based Setup Utility displays the system's current configuration and allows the user to set the system parameters. The configuration parameters are stored in configuration memory described in section 4.8 "RTC/Configuration." A backup copy of configuration data is also saved in the boot block flash ROM. The user activates Setup by either pressing F1 during the boot sequence (while the cursor is located at the upper right corner of the display).

Some changes made in Setup may take effect immediately upon exiting Setup, while other changes may require rebooting the system before taking effect. The following parameters take effect immediately upon exiting Setup:

- Date/time
- Power conservation (when/how much)
- Hibernation (on/off settings)
- Warning beep
- Setup password
- Port disables (diskette, serial. Parallel)
- Monitor energy saving
- Resume password

Changes to the following parameters will not take place until after the next system boot:

- POST memory test
- Keyboard Numlock
- Boot sequence/display
- Port settings (serial, parallel)
- Power-on password
- Diskette boot disable
- Language selection
- Network settings

4.10.3 PNP SUPPORT

The BIOS includes Plug 'n Play (PnP) support. Table 4-19 shows the PnP functions supported:

Table 4-19.
PnP BIOS Functions

Function	Register
00h	Get number of system device nodes
01h	Get system device node
02h	Set system device node
03h	Get event
04h	Send message

4.10.4 CLIENT MANAGEMENT SUPPORT

The BIOS provides specific INT 15 functions for dealing with Client Management features. These functions are listed Table 4-20.

Table 4-20.
PnP Client Management Functions (INT15)

AX	Function	Mode
E800h	Get system ID	Real, 16-, & 32-bit Prot.
E813h	Get monitor information	Real, 16-, & 32-bit Prot.
E814h	Get system revision	Real, 16-, & 32-bit Prot.
E817h	Get drive attribute	Real
E818h	Get drive off-line test	Real
E819h	Get chassis serial number	Real, 16-, & 32-bit Prot.
E81Ah	Write chassis serial number	Real
E81Bh	Get drive threshold	Real
E81Ch	Write network error log	Real, 16-, & 32-bit Prot.
E81Dh	Read network error log	Real, 16-, & 32-bit Prot.
E81Eh	Get drive ID	Real
E823h	Access NVS	Real, 16-, & 32-bit Prot.
E827h	Return EVV Status	Real, 16-, & 32-bit Prot.

All other client management functions are not supported and should return the appropriate settings (AH=86h, CF=1) if called. All 32-bit protected mode calls are accessed by using the BIOS32 Service Directory. The service identifier for client management is “$CLM.”

The monitor information (EDID and DDC) is obtained during POST and stored in shadow memory. This is done using a VESA call, which works only in real mode. Once the EDID and DDC information is in shadow memory, the data can be accessed either in real or protected mode.

The chassis number in this system is not stored on the backplane assembly as in previous systems but is stored instead in the EEPROM (high CMOS block) on the system board.

4.10.5 POWER MANAGEMENT SUPPORT

The Compaq Deskpro 2000 system includes Advanced Power Management (APM) support that provides, if so configured, for the automatic shutdown of certain areas within a system after a specified time of inactivity has elapsed. When activity is detected, APM brings the system back up to full power to provide complete user support. For maximum energy-conservation benefit, APM functionality should be implemented using the following three layers:

- BIOS layer (APM BIOS)
- Operating system layer (APM driver)
- Application layer (APM-aware application or device driver)

The APM BIOS for this system supports APM 1.2 as well as previous versions 1.1 and 1.0. The APM BIOS functions are listed in Table 4-21.

Table 4-21.
APM BIOS Functions (INT15)

AX	Function
5300h	APM Installation Check
5301h	APM Connect (Real Mode)
5302h	APM Connect (16-bit Protected Mode)
5303h	APM Connect (32-bit Protected Mode)
5304h	Interface Disconnect
5305h	CPU Idle
5306h	CPU Busy
5307h	Set Power State [1]
5308h	Enable/Disable Power Management
5309h	Restore Power On Defaults
530Ah	Get Power Status
530Bh	Get PM Event
530Ch	Get Power State
530Dh	Enable/Disable Device Power Management
530Eh	APM Driver Version
530Fh	Engage/Disengage Power Management
5380h	OEM (Compaq) Specific APM Function

NOTE:
[1] Limited functionality on this system (does not support setting power state of specific components).

With power management enabled, inactivity timers are monitored. When an inactivity timer times out, an SMI to the microprocessor is generated to invoke the SMI handler. The SMI handler works with the APM driver and APM BIOS to take appropriate action based on which inactivity timer timed out.

Two I/O ports are used for APM communication with the SMI handler:

Port Address	Name
0B2h	APM Control
0B3h	APM Status

4.10.5.1 Hard Drive Spindown Control

The timeout parameter stored in the SIT record 04h and indexed through CMOS location 2Ah (bits <4..0>) represents the period of hard drive inactivity required to elapse before the hard drive is allowed to spin down. The timeout value is downloaded from CMOS to a timer on the hard drive. The timeout period can be set in incremental values of 0 (timeout disabled), 10, 15, 20, 30, and 60 minutes. A timed-out and spun-down hard drive will automatically spin back up upon the next drive access. It is normal for the user to detect a certain amount of access latency in this situation.

4.10.5.2 Monitor Control

This system provides monitor power control for monitors that conform to the VESA display power management signaling protocol. This protocol defines different power consumption conditions and uses the HSYNC and VSYNC signals to select a monitor's power condition. Table 4-22 lists the monitor power conditions.

Table 4-22.
Monitor Power Management Conditions

HSYNC	VSYNC	Power Mode	Description
Active	Active	On	Monitor is completely powered up. If activated, the inactivity counter counts down during system inactivity and if allowed to tiemout, generates an SMI to initiate the Suspend mode.
Active	Inactive	Suspend	Monitor's high voltage section is turned off and CRT heater (filament) voltage is reduced from 6.6 to 4.4 VDC. The Off mode inactivity timer counts down from the preset value and if allowed to timeout, another SMI is generated and serviced, resulting in the monitor being placed into the Off mode. Wake up from Suspend mode is typically a few seconds.
Inactive	Inactive	Off	Monitor's high voltage section and heater circuitry is turned off. Wake up from Off mode is a little longer than from Suspend.

The timeout parameter set in the SIT record 03h and indexed at CMOS location 2Ch (bits <4..0>) represents the period of system I/O inactivity required to elapse before the monitor is placed into Suspend mode.

A separate timer function (enabled through CMOS location 1Fh, bit <1>) can be enabled to place the monitor into the Off mode after 45 minutes of being in Suspend mode.

4.10.5.3 Microprocessor Control

The Pentium Pro microprocessor can be configured to enter a low power condition. By setting bit <26> of the microprocessor's Power-On Configuration Model Specific Register (EBL_CR_POWERON @ 2Ah), the Pentium Pro will turn off it's core clocks when a HLT (Halt) instruction is received.

4.10.6 SECURITY FEATURE SUPPORT

4.10.6.1 Flash ROM Write Protection

The system BIOS firmware is contained in a flash ROM device that can be re-written with updated code if necessary. The ROM is write-protected through I/O port 78h bit<6> (GPIO16), which needs to be cleared (the power-up state is a "1") before new BIOS can be written into the flash ROM. During the boot sequence, the BIOS checks for the presence of the ROMPAQ diskette and, if detected, clears bit <6> allowing the flash ROM to be updated.

4.10.6.2 Power-On Password

The Power-On password is stored in eight bytes at configuration memory locations 38h-3Fh. If the Power-On password function is enabled, the BIOS sets bit <0> of the SIO register (399.12h) to lock the CMOS and the user is prompted to enter the password during POST. If an incorrect entry is made, the system halts and does not boot.

4.10.6.3 Administrator Password

The administrator password is stored in eight bytes at configuration memory locations F8h-FFh. If the administrator password function is enabled, the BIOS clears bit <5> of the KRR register (399.05h) to select the lower half of CMOS (inhibiting access to the upper half where the administrator password is stored) and the user is prompted to enter the password before running F10-Setup or before booting from a ROMPAQ diskette. If an incorrect entry is made, the system halts and does not boot.

4.10.6.4 Quicklock/QuickBlank

The QuickLock feature allows, if enabled in F10-Setup through CMOS location 13h bit <2>, the user to lock the keyboard and mouse by invoking the **Ctrl-Alt-L** keystrokes. This initiates an SMI and the SMI handler then takes the appropriate action. If the QuickBlank feature is enabled at that time then the screen will be blanked as well.

> **NOTE:** Although the SMI is used for initiating QuickLock/QuickBlank functions, these functions are not considered power management features.

4.10.6.5 Diskette Drive Control

The diskette drive is locked out of the boot process if CMOS location 13h bit <3> is set. In this instance the BIOS will only boot from the hard drive. In addition, no writes to the diskette drive will be allowed if I/O port 78h bit <7> is cleared (the power-up default is a "1"). The diskette drive is completely disabled if bit <3> of the FER register (399.00h) is cleared.

4.10.6.6 Serial/Parallel Port Disable

The serial and parallel ports can be disabled through bits <1> and <0> respectively of the FER register (399.00h) as follows:

Bit = 1, port is enabled
Bit = 0, port is disabled.

4.10.7 RESET ROUTINE

There are two types of reset events: hard and soft. Traditionally, a hard reset is generated only during power-up and produced only by the circuitry driving the PWRGOOD signal. However, the 82371 controller has the ability to generate a hard reset through software. First, a one (1) must be written to bit <1> of I/O port 0CF9h. A one must then be written to bit 2 of the same I/O port. These two steps cause the PIIX-3 to create a hard reset by asserting its CPURST#, PCIRST#, and RSTDRV outputs for at least 1 ms. After the reset, the PIIX-3 automatically clears bit 2 of I/O port 0CF9h.

Chapter 5
INPUT/OUTPUT INTERFACES

5.1 INTRODUCTION

This chapter describes the system's interfaces that provide input and output (I/O) porting of data and specifically discusses interfaces that are controlled through I/O-mapped registers. The I/O interfaces are integrated functions of the support chipset and the 87306 I/O controller. The following I/O interfaces are covered in this chapter:

5.2 ENHANCED IDE INTERFACE

The enhanced IDE (EIDE) interface consists of a controller (integrated into the 82371 component) that supports up to four IDE devices. Devices that may connect to the IDE interface include:

- Hard drives
- CD-ROM drives
- Power Drives (writeable CD-ROM drives)
- 120-MB floppy drives

Two 40-pin keyed IDE data connectors are provided on the system board. Each connector can support two devices. In the standard configuration the hard drive is attached to the primary connector and the CD-ROM (if installed) is attached to the secondary connector. The enhanced IDE is capable of performing PCI bus master transfers at rates up to 22 MBps.

5.2.1 IDE PROGRAMMING

The IDE interface is configured as a PCI device and controlled through standard I/O mapped registers.

5.2.1.1 IDE Configuration Registers

The IDE controller is integrated into the 82371 component and configured as a PCI device with bus mastering capability. The PCI configuration registers for the IDE controller function (PCI function #1) are listed in Table 5-1.

Table 5-1.
IDE PCI Configuration Registers

PCI Conf. Address	Register	Value on Reset
00-01h	Vender ID	8086h
02-03h	Device ID	7010h
04-05h	PCI Command	0000h
06-07h	PCI Status	0280h
08h	Revision ID	00h
09h	Programming	80h
0Ah	Sub-Class	01h
0Bh	Base Class Code	01h
0Dh	Master Latency Timer	00h
0Eh	Header Type	80h
20-23h	Bus Master Base Address	0000 0001h
40,41h	IDE Timing Modes (Primary)	0000h
42, 43h	IDE Timing Modes (Secondary)	0000h
44h	Slave IDE Timing	00h

5.2.1.2 IDE Bus Master Control Registers

The IDE interface can perform PCI bus master operations using the I/O mapped control registers listed in Table 5-2.

Table 5-2.
IDE Bus Master Control Registers

I/O Addr. Offset	Size (Bytes)	Register	Default Value
00h	2	Bus Master IDE Command (Primary)	00h
02h	2	Bus Master IDE Status (Primary)	00h
04h	4	Bus Master IDE Descriptor Ptr (Pri.)	0000 0000h
08h	2	Bus Master IDE Command (Secondary)	00h
0Ah	2	Bus Master IDE Status (Secondary)	00h
0Ch	4	Bus Master IDE Descriptor Ptr (Sec.)	0000 0000h

5.2.1.3 IDE ATA Control Registers

The IDE controller of the 82371 decodes the addressing of the standard AT attachment (ATA) registers for the connected drive, which is where the ATA control registers actually reside. The primary and secondary interface connectors are mapped as shown in Table 5-3.

Table 5-3.
IDE ATA Control Registers

Primary I/O Addr.	Secondary I/O Addr.	Register	R/W
1F0h	170h	Data	R/W
1F1h	171h	Error	R
1F1h	171h	Features	W
1F2h	172h	Sector Count	R/W
1F3h	173h	Sector Number	R/W
1F4h	174h	Cylinder Low	R/W
1F5h	175h	Cylinder High	R/W
1F6h	176h	Drive/Head	R/W
1F7h	177h	Status	R
1F7h	177h	Command	W
3F6h	376h	Alternate Status	R
3F6h	376h	Drive Control	W
3F7h	377h	Drive Address	R
3F7h	377h	n/a for hard drive	W

The following paragraphs describe the IDE ATA control registers.

Data Register, I/O Port 1F0h/170h

This register is used for transferring all data to and from the hard drive controller. This register is also used for transferring the sector table during format commands. All transfers are high-speed 16-bit I/O operation except for Error Correction Code (ECC) bytes during Read/Write Long commands.

Error Register, I/O Port 1F1h/171h (Read Only)

The Error register contains error status from the last command executed by the hard drive controller. The contents of this register are valid when the following conditions exist:

- Error bit is set in the Status register
- Hard drive controller has completed execution of its internal diagnostics

The contents of the Error register are interpreted as a diagnostic status byte after the execution of a diagnostic command or when the system is initialized.

Bit	Function
7	Bad Block Mark Detected in Requested Sector ID Field (if set)
6	Non-correctable Data Error (if set)
5	Reserved
4	Requested Sector ID Field Not Found (if set)
3	Reserved
2	Requested Command Aborted Due To Invalid Hard Drive Status or Invalid Command Code (if set)
1	Track 0 Not Found During Re-calibration Command (if set)
0	Data Address Mark Not Found After Correct ID Field (if set)

Set Features Register, I/O Port 1F1h/171h (Write Only)

This register is command-specific and may be used to enable and disable features of the interface.

Sector Count Register, I/O Port 1F2h/172h

This register defines either:

- the number of sectors of data to be read or written
  or
- the number of sectors per track for format commands

If the value in this register is zero, a count of 256 sectors is specified. The sector count is decremented as each sector is accessed, so that the value indicates the number of sectors left to access when an error occurs in a multi-sector operation. During the Initialize Drive Parameters command, this register contains the number of sectors per track.

Sector Number Register, I/O Port 1F3h/173h

The Sector Number register contains the starting sector number for a hard drive access.

Cylinder Low, Cylinder High Registers, I/O Port 1F4h, 1F5h/174h, 175h

These registers contain the starting cylinder number for each hard drive access. The three most-significant bits of the value are held in byte address 1F5h (bits <2..0>) while the remaining bits are held in location 1F4h.

Drive Select/Head Register, I/O Port 1F6h/176h

Bit	Function
7	Reserved
6,5	Sector Size: 00 = Reserved 01 = 512 bytes/sector 10, 11 = Reserved
4	Drive Select: 0 = Drive 1 1 = Drive 2
3..0	Head Select Number: 0000 = 0 1000 = 8 0001 = 1 1001 = 9 0010 = 2 1010 = 10 0011 = 3 1011 = 11 0100 = 4 1100 = 12 0101 = 5 1101 = 13 0110 = 6 1110 = 14 0111 = 7 1111 = 15

NOTE:

Setting bit <4> to 1 when Drive 2 is not present may cause remaining controller registers to not respond until Drive 1 is selected again.

Status Register, I/O Port 1F7h/177h (Read Only)

The contents of this register are updated at the completion of each command. If the Busy bit is set, no other bits are valid. Reading this register clears the IRQ14 interrupt.

Bit	Function
7	Controller Busy. If set, controller is executing a command.
6	READY- Signal Active (if set).
5	WRITE FAULT- Signal Active (if set).
4	SEEK COMPLETE- Signal Active (if set)
3	Data Request. If set, the controller is ready for a byte or word-length data transfer. Bit should be verified before each transfer.
2	Correctable Data Error Flag. If set, data error has occurred and has been corrected.
1	INDEX- Signal Active (if set).
0	Error Detected. When set, indicates error has occurred. O.ther bits in register should be checked to determine error source.

NOTE:

Register status of an error condition does not change until register is read.

The alternate Status register at location 3F6h holds the same status data as location 1F7h but does not clear hardware conditions when read.

Command Register, I/O Port 1F7h/177h (Write Only)

The IDE controller commands are written to this register. The command write action should be prefaced with the loading of data into the appropriate registers. Execution begins when the command is written to 1F7h/177h. Table 5-4 lists the standard IDE commands.

Table 5-4.
IDE Controller Commands

Command	Value
Initialize Drive Parameters	91h
Seek	7xh
Recalibrate	1xh
Read Sectors with Retries	20h*
Read Long with Retries	22h*
Write Sectors with Retries	30h*
Write Long with Retries	32h*
Verify Sectors with Retries	40h
Format Track	50h
Execute Controller Diagnostic	90h
Idle	97h, E3h
Idle Immediate	95h, E1h
Enter Low Power and Enable/Disable Timeout	96h
Enter Idle and Enable/Disable Timeout	97h
Check Status	98h
Identify	Ech
Read Buffer	E4h
Write Buffer	E8h
NOP	00h
Read DMA with Retry	C8h
Read DMA without Retry	C9h
Read Multiple	C4h
Set Features	Efh
Set Multiple Mode	C6h
Sleep	99h, E6h
Standby	96h, E2h
Standby Immediate	94h, E0h
Write DMA with Retry	CAh
Write DMA without Retry	CBh
Write Multiple	C5h
Write Same	E9h
Write Verify	3Ch

* Without retries, add one to the value.

Alternate Status Register, I/O Port 3F6h/376h (Read Only)

The alternate Status register at location 3F6h holds the same status data as location 1F7h but does not clear hardware conditions when read.

Drive Control Register, I/O Port 3F6h/376h (Write Only)

Bit	Function
7..3	Reserved
2	Controller Control: 0 = Re-enable 1 = Reset
1	Interrupt Enable/Disable 0 = Disable interrupts 1 = Enable interrupts
0	Reserved

Drive Access Register, I/O Port 3F7h/377h (Read Only)

Bit	Function
7	Reserved
6	WRITE GATE- Signal Active (if set)
5..2	Head Select: 0000 = 15 1000 = 7 0001 = 14 1001 = 6 0010 = 13 1010 = 5 0011 = 12 1011 = 4 0100 = 11 1100 = 3 0101 = 10 1101 = 2 0110 = 9 1110 = 1 0111 = 8 1111 = 0
1,0	Drive Select: 00 = Disabled 01 = Drive 1 selected 10 = Drive 0 selected 11 = Invalid

5.2.2 IDE CONNECTOR

This system uses a standard 40-pin connector for IDE devices. Device power is supplied through a separate connector.

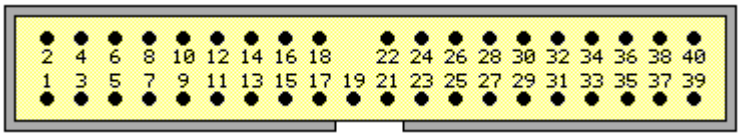


Figure 5–1. 40-Pin IDE Connector.

Table 5-5.
40-Pin IDE Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	RESET-	Reset	21	DRQ	DMA Request
2	GND	Ground	22	GND	Ground
3	DD7	Data Bit <7>	23	IOW-	I/O Write
4	DD8	Data Bit <8>	24	GND	Ground
5	DD6	Data Bit <6>	25	IOR-	I/O Read
6	DD9	Data Bit <9>	26	GND	Ground
7	DD5	Data Bit <5>	27	IORDY	I/O Channel Ready
8	DD10	Data Bit <10>	28	CSEL	Cable Select
9	DD4	Data Bit <4>	29	DAK-	DMA Acknowledge
10	DD11	Data Bit <11>	30	GND	Ground
11	DD3	Data Bit <3>	31	IRQn	Interrupt Request [1]
12	DD12	Data Bit <12>	32	IO16-	16-bit I/O
13	DD2	Data Bit <2>	33	DA1	Address 1
14	DD13	Data Bit <13>	34	DSKPDIAG	Pass Diagnostics
15	DD1	Data Bit <1>	35	DA0	Address 0
16	DD14	Data Bit <14>	36	DA2	Address 2
17	DD0	Data Bit <0>	37	CS0-	Chip Select
18	DD15	Data Bit <15>	38	CS1-	Chip Select
19	GND	Ground	39	HDACTIVE-	Drive Active (front panel LED) [2]
20	--	Key	40	GND	Ground

NOTES:

[1] Primary connector wired to IRQ14, secondary connector wired to IRQ15.

[2] Pin 39 is used for spindle sync and drive activity (becomes SPSYNC/DACT-) when synchronous drive are connected.

5.3 DISKETTE DRIVE INTERFACE

The diskette drive interface supports up to two diskette drives, each which connect to a standard 34-pin diskette drive connector. All models come standard with a 3.5 inch 1.44-MB diskette drive installed as drive A. An additional diskette drive (either a 3.5 inch 720-KB, 1.44-MB, or 2.88-MB drive or a 5.25 inch 360-KB or 1.2-MB drive) may also be installed as drive B. The drive designation is determined by which connector is used on the diskette drive cable. The drive attached to the end connector is drive A while the drive attached to the second (next to the end) connector) is drive B.

On all models, the diskette drive interface function is integrated into the 87306 I/O controller component. The internal logic of the 87306 I/O controller is software-compatible with standard 82077-type logic. The diskette drive controller has three operational phases in the following order:

- Command phase - The controller receives the command from the system.
- Execution phase - The controller carries out the command.
- Results phase - Status and results data is read back from the controller to the system.

The Command phase consists of several bytes written in series from the CPU to the data register (3F5h/375h). The first byte identifies the command and the remaining bytes define the parameters of the command. The Main Status register (3F4h/374h) provides data flow control for the diskette drive controller and must be polled between each byte transfer during the Command phase.

The Execution phase starts as soon as the last byte of the Command phase is received. An Execution phase may involve the transfer of data to and from the diskette drive, a mechnical control function of the drive, or an operation that remains internal to the diskette drive controller. Data transfers (writes or reads) with the diskette drive controller are by DMA, using the DRQ2 and DACK2- signals for control.

The Results phase consists of the CPU reading a series of status bytes (from the data register (3F5h/375h)) that indicate the results of the command. Note that some commands do not have a Result phase, in which case the Execution phase can be followed by a Command phase.

During periods of inactivity, the diskette drive controller is in a non-operation mode known as the Idle phase.

5.3.1 DISKETTE DRIVE PROGRAMMING

5.3.1.1 Diskette Drive Interface Configuration

The diskette drive controller must be configured for a specific address and also must be enabled before it can be used. Address selection and enabling of the diskette drive interface are affected through the non-shaded bits of the following configuration register of the 87306 I/O controller:

Function Enable Register, Indexed Addr. 399.00h

Bit	Function
7	Not used on this system
6	IDE Enable (always = 0 on this system)
5	Diskette Drive Controller Base Address Select: 0 = Primary address (3F1h), 1 = Secondary address (371h)
4	Diskette Drive Controller Encoding (always = 0 on this system)
3	Diskette Drive Controller Enable: 0 = Disabled, 1 = Enabled
2	Not used on this system.
1	Serial Interface (UART 1) Enable: 0 = Disabled, 1 = Enabled
0	Parallel Interface Enable: 0 = Disabled, 1 = Enabled

Non-related functions.

5.3.1.2 Diskette Drive Interface Control

The BIOS function INT 13 provides basic control of the diskette drive interface. The diskette drive interface can be controlled by software through I/O-mapped registers listed in Table 5-6.

Table 5-6.
Diskette Drive Controller Registers

Primary Address	Alternate Address	Register	R/W
3F1h	371h	Media ID	R
3F2h	372h	Drive Control	W
3F4h	374h	Main Status	R
3F5h	375h	Data	R/W
3F7h	377h	Drive Status	R
		Data Transfer Rate	W

The base address (3F1h or 371h) and enabling of the diskette drive controller is selected through the Function Enable Register (FER, addr. 399.00h) of the 87306 I/O controller. Address selection and enabling is automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The following paragraphs describe the diskette drive interface control registers.

Media ID Register, I/O Port 3F1h/371h (Read Only)

Bit	Function
7..5	Media Type: xx1 = Invalid 000 = 5.25 inch drive 010 = 2.88 MB (3.5 inch drive) 100 = 1.44 MB (3.5 inch drive) 110 = 720 KB (3.5 inch drive)
4..2	Reserved
1,0	Tape Select: 00 = None 10 = Drive 2 01 = Drive 1 11 = Drive 3

Drive Control Register, I/O Port 3F2h/372h (Write Only)

Bit	Function
7,6	Reserved
5	Drive 2 Motor 0 = Off, 1 = On
4	Drive 1 Motor 0 = Off, 1 = On
3	Interrupt / DMA Enable 0 = Disabled, 1 = Enabled
2	Controller Enable 0 = Reset controller, 1 = Enable controller
1,0	Drive Select 00 = Drive 1 01 = Drive 2 10 = Reserved 11 = Tape drive

Main Status Register, I/O Port 3F4h/374h (Read Only)

Bit	Function
7	Request for Master. When set, indicates the controller is ready to send or receive data from the CPU. Cleared immediately after a byte transfer. Indicates interrupt pin status during non-DMA phase.
6	Data I/O Direction. 0 = Expecting a write 1 = Expecting a read
5	Non-DMA Execution. When set, indicates controller is in the execution phase of a byte transfer in non-DMA mode.
4	Command In Progress. When set, indicates that first byte of command phase has been received. Cleared when last byte in result phase is read.
3..0	Drive Busy Indicators. Bit is set after the last byte of the command phase of a seek or recalibrate command is given by the corresponding drive: <3>, Drive 3 <2>, Drive 2 <1>, Drive 1 <0>, Drive 0

Data Register, I/O Port 3F5h/375h

Data commands are written to, and data and status bytes are read from this register.

Data Transfer Rate Register, I/O Port 3F7h/377h (Write Only)

Bit	Function
7	Software Reset
6	Low Power Mode (if set)
5	Reserved
4..2	Write Precompensation Delay 000 = Default values for selected data rate (default)
1,0	Data Rate Select: 00 = 500 Kb/s 01 = 300 Kb/s 10 = 250 Kb/s 11 = 1 or 2 Mb/s (depending on TUP reg. Bit <1>)

5.3.2 DISKETTE DRIVE CONNECTOR

This system uses a standard 34-pin connector (refer to Figure 5-2 and Table 5-7 for the pinout) for diskette drives. Drive power is supplied through a separate connector.

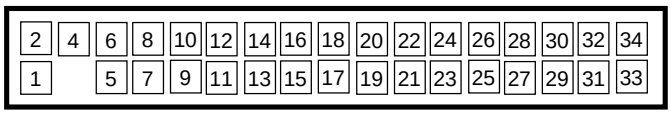


Figure 5–2. 34-Pin Diskette Drive Connector.

Table 5-7.
34-Pin Diskette Drive Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	18	DIR-	Drive head direction control
2	LOW DEN-	Low density select	19	GND	Ground
3	---	(KEY)	20	STEP-	Drive head track step control
4	MEDIA ID-	Media identification	21	GND	Ground
5	GND	Ground	22	WR DATA-	Write data
6	DRV 4 SEL-	Drive 4 select	23	GND	Ground
7	GND	Ground	24	WR ENABLE-	Enable for WR DATA-
8	INDEX-	Media index is detected	25	GND	Ground
9	GND	Ground	26	TRK 00-	Heads at track 00 indicator
10	MTR 1 ON-	Activates drive motor	27	GND	Ground
11	GND	Ground	28	WR PRTK-	Media write protect status
12	DRV 2 SEL-	Drive 2 select	29	GND	Ground
13	GND	Ground	30	RD DATA-	Data and clock read off disk
14	DRV 1 SEL-	Drive 1 select	31	GND	Ground
15	GND	Ground	32	SIDE SEL-	Head select (side 0 or 1)
16	MTR 2 ON-	Activates drive motor	33	GND	Ground
17	GND	Ground	34	DSK CHG-	Drive door opened indicator

5.4 SERIAL INTERFACE

The serial interface transmits and receives asynchronous serial data with external devices at selectable baud rates up to 115,200. The serial interface function is provided by the 87306 I/O controller component, which integrates a 16550/16450-compatible UART that complies with EIA standard RS-232-C. The serial interface provides serial-to-parallel conversion of receive data and parallel-to-serial conversion of transmit data. All standard modem control signals are provided.

5.4.1 SERIAL INTERFACE PROGRAMMING

5.4.1.1 Serial Interface Configuration

The serial interface must be configured for a specific address range (COM1, COM2, etc.) and also must be enabled before it can be used. Address selection and enabling of the serial interface are affected through the non-shaded bits of the following configuration registers of the 87306 I/O controller. Address selection and enabling are automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

Function Enable Register, Indexed Addr. 399.00h

Bit	Function
7	Not used on this system
6	IDE Enable (always = 0 on this system)
5	Diskette Drive Controller Base Address Select 0 = Primary address (3F1h), 1 = Secondary address (371h)
4	Diskette Drive Controller Encoding (always = 0 on this system)
3	Diskette Drive Controller Enable: 0 = Disabled, 1 = Enabled
2	Not used on this system.
1	Serial Interface (UART 1) Enable: 0 = Disabled, 1 = Enabled
0	Parallel Interface Enable: 0 = Disabled, 1 = Enabled

Non-related functions.

Function Address Register, Indexed Addr. 399.01h

Bit	Function
7,6	COM3/COM4 Base Address Selection COM3 IRQ4 COM4 IRQ3 00 = 3E8h 2E8h 01 = 338h 238h 10 = 2E8h 2E0h 11 = 220h 228h
5,4	Not used on this system.
3,2	Serial Interface COMn Select: 00 = COM1 10 = COM3 (refer to bits <7,6>) 01 = COM2 11 = COM4 (refer to bits <7,6>)
1,0	Parallel Interface Base Address (LPTn) & IRQ Select: 00 = 378h (LPT1), IRQ5 10 = 278h (LPT2), IRQ5 01 = 3BCh (LPT3), IRQ7 11 = Reserved

Non-related functions.

5.4.1.2 Serial Interface Control

The BIOS function INT 14 provides basic control of the serial interface. The serial interface can be controlled by software through the registers listed in Table 5-8.

Table 5-8.
Serial Interface Control Registers

Address	Register	R/W
Base	Receive Buffer / Transmit Holding [1]	R/W
Base, Base + 1	Baud Rate Divisor Latch [2]	R/W
Base + 1	Interrupt Enable	R/W
Base + 2	Interrupt ID	RO
Base + 3	Line Control	R/W
Base + 4	Modem Control	R/W
Base + 5	Line Status	RO
Base + 6	Modem Status	RO
Base + 7	Scratch Pad	R/W

NOTES:

Base Address:
COM1 = 3F8h COM3,4 = refer to reg. 399.01h
COM2 = 2F8h

[1] This register holds receive data when read from and transmit data when written to.
[2] When bit <7> of the Line Control register is set (1), writing to 3F8h and 3F9h programs the divisor rate for the baud rate generator.

Receive Buffer / Transmit Holding Register, I/O Port 3F8h/2F8h

When read by the CPU, this byte contains receive data. When written to by the CPU, the byte contains data to be transmitted.

Baud Rate Divisor Latch Register, I/O Port 3F8h, 3F9h/2F8, 2F9h

When bit <7> of the Line Control register is set (1), a write to this pair of locations loads the decimal value used to divide the 1.8462-MHz clock to create the desired baud rate for serial transmission. The possible baud rates are shown as follows:

Baud Rate	Decimal Divisor	Baud Rate	Decimal Divisor
50	2304	2400	48
75	1536	3600	32
110	1047	4800	24
134.5	857	7200	16
150	768	9600	12
300	384	19200	6
600	192	38400	3
1200	96	57600	2
1800	64	115200	1
2000	58		

Divisor = 1846200 / (Desired baud rate X 16)

Interrupt Enable Register, I/O Port 3F9h/2F9h

Bits <3..0> of this register are used for enabling interrupt sources. A set bit enables interrupt generation by the associated source.

Bit	Function
7..4	Reserved
3	Modem Status Interrupt Enable (if set) (CTS, DSR, RI, CD)
2	Receiver Line Status Interrupt Enable (if set) (Overrun error, parity error, framing error, break)
1	Transmitter Holding Register Empty Interrupt Enable (if set)
0	Baud Rate Divisor Interrupt Enable (if set)

Interrupt ID Register, I/O Port 3FAh/2FAh (Read Only)

This read-only register indicates the serial controller as the source of the interrupt (bit <0>) as well as the reason (bits <3..1>) for the interrupt. Reading this register clears the interrupt and sets bit <0>.

Bit	Function
7,6	FIFO Enable/Disable 0 = Disabled 1 = Enabled
5,4	Reserved
3..1	Interrupt Source: 000 = Modem status (lowest priority) 001 = Transmitter holding reg. Empty 010 = Received data available 011 = Receiver line status reg. 100,101 = Reserved 110 = Character time-out (highest priority) 111 = Reserved
0	Interrupt Pending (if cleared)

FIFO Control Register, I/O Port 3FAh/2FAh (Write Only)

This write-only register enables and clears the FIFOs and set the trigger level and DMA mode.

Bit	Function
7,6	Receiver Trigger Level 00 = 1 byte 10 = 8 bytes 01 = 4 bytes 11 = 14 bytes
5..3	Reserved
2	Transmit FIFO Reset (if set)
1	Receive FIFO Reset (if set)
0	FIFOs Enable/Disable 0 = Disable TX/RX FIFOs, 1 = Enable TX/RX FIFOs

Line Control Register, I/O Port 3FBh/2FBh

This register specifies the data transmission format.

Bit	Function
7	RX Buffer / TX Holding Reg. And Divisor Rate Reg. Access 0 = RX buffer, TX holding reg., and Interrupt En. Reg. Are accessable. 1 = Divisor Latch reg. is accessable.
6	Break Control (forces SOUT signal low if set)
5	Stick Parity. If set, even parity bit is logic 0, odd parity bit is logic 1
4	Parity Type 0 = Odd, 1 = Even
3	Parity Enable: 0 = Disabled, 1 = Enabled
2	Stop Bit: 0 = 1 stop bit, 1 = 2 stop bits
1,0	Word Size: 00 = 5 bits 10 = 7 bits 01 = 6 bits 11 = 8 bits

Modem Control Register, I/O Port 3FCh/2FCh

This register controls the modem signal lines

Bit	Function
7..5	Reserved
4	Internal Loopback Enabled (if set)
3	Serial Interface Interrupts Enabled (if set)
2	Reserved
1	RTS Signal Active (if set)
0	DTR Signal Active (if set)

Line Status Register, I/O Port 3FDh/2FDh (Read Only)

This register contains the status of the current data transfer. Bits <2..0> are cleared when read.

Bit	Function
7	Parity Error, Framing Error, or Break Cond. Exists (if set)
6	TX Holding Reg. and Transmitter Shift Reg. Are Empty (if set)
5	TX Holding Reg. Is Empty (if set)
4	Break Interrupt Has Occurred (if set)
3	Framing Error Has Occurred (if set
2	Parity Error Has Occurred (if set)
1	Overrun Error Has Occurred (if set)
0	Data Register Ready To Be Read (if set)

Modem Status Register, I/O Port 3FEh/2FEh (Read Only)

This register contains the status of the modem signal lines. A set bit indicates that the associated signal is active.

Bit	Function
7	DCD- Active
6	RI- Active
5	DSR Active
4	CTS Active
3	DCD- Changed Since Last Read
2	RI- Changed From Low to High Since Last Read
1	DSR- Has Changed State Since Last Read
0	CTS- Has Changed State Since Last Read

Scratch Pad Register, I/O Port 3FFh/2FFh

This register id not used in this system.

5.4.2 SERIAL INTERFACE CONNECTOR

The serial interface uses a male DB-9 connector (Figure 5-3). The pinout of this connector is listed in Table 5-9.

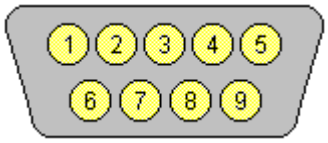


Figure 5–3. Serial Interface Connector (Male DB-9 as viewed from rear of chassis)

Table 5-9.
DB-9 Serial Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	CD	Carrier Detect	6	DSR	Data Set Ready
2	RX Data	Receive Data	7	RTS	Request To Send
3	TX Data	Transmit Data	8	CTS	Clear To Send
4	DTR	Data Terminal Ready	9	RI	Ring Indicator
5	GND	Ground	--	--	--

5.5 PARALLEL INTERFACE

The parallel interface provides connection to a peripheral device that has a compatible interface, the most common being a printer. The parallel interface function is integrated into the 87306 I/O controller component and provides bi-directional 8-bit parallel data transfers with a peripheral device. The parallel interface supports three modes of operation:

- Standard Parallel Port (SPP) mode
- Enhanced Parallel Port (EPP) mode
- Extended Capabilities Port (ECP) mode

These three modes provide complete support as specified for an IEEE 1284 parallel port.

5.5.1 STANDARD PARALLEL PORT MODE

The Standard Parallel Port (SPP) mode uses software-based protocol and includes two sub-modes of operation, compatible and extended, both of which can provide data transfers up to 150 KB/s. In the compatible mode, CPU write data is simply presented on the eight data lines. A CPU read of the parallel port yields the last data byte that was written.

The following steps define the standard procedure for communicating with a printing device:

1. The system checks the Printer Status register. If the Busy, Paper Out, or Printer Fault signals are indicated as being active, the system either waits for a status change or generates an error message.
2. The system sends a byte of data to the Printer Data register, then pulses the printer STROBE signal (through the Printer Control register) for at least 500 ns.
3. The system then monitors the Printer Status register for acknowledgment of the data byte before sending the next byte.

In extended mode, a direction control bit (CTR 37Ah, bit <5>) controls the latching of output data while allowing a CPU read to fetch data present on the data lines, thereby providing bi-directional parallel transfers to occur.

The SPP mode uses three registers for operation: the Data register (DTR), the Status register (STR) and the Control register (CTR). Address decoding in SPP mode includes address lines A0 and A1.

5.5.2 ENHANCED PARALLEL PORT MODE

In Enhanced Parallel Port (EPP) mode, increased data transfers are possible (up to 2 MB/s) due to a hardware protocol that provides automatic address and strobe generation. EPP revisions 1.7 and 1.9 are both supported. For the parallel interface to be initialized for EPP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with EPP mode. If compatible, then EPP mode can be used. In EPP mode, system timing is closely coupled to EPP timing. A watchdog timer is used to prevent system lockup.

Five additional registers are available in EPP mode to handle 16- and 32-bit CPU accesses with the parallel interface. Address decoding includes address lines A0, A1, and A2.

5.5.3 EXTENDED CAPABILITIES PORT MODE

The Extended Capabilities Port (ECP) mode, like EPP, also uses a hardware protocol-based design that supports transfers up to 2 MB/s. Automatic generation of addresses and strobes as well as Run Length Encoding (RLE) decompression is supported by ECP mode. The ECP mode includes a bi-directional FIFO buffer that can be accessed by the CPU using DMA or programmed I/O. For the parallel interface to be initialized for ECP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with ECP mode. If compatible, then ECP mode can be used.

Ten control registers are available in ECP mode to handle transfer operations. In accessing the control registers, the base address is determined by address lines A2-A9, with lines A0, A1, and A10 defining the offset address of the control register. Registers used for FIFO operations are accessed at their base address + 400h (i.e., if configured for LPT1, then 378h + 400h = 778h).

The ECP mode includes several sub-modes as determined by the Extended Control register. Two submodes of ECP allow the parallel port to be controlled by software. In these modes, the FIFO is cleared and not used, and DMA and RLE are inhibited.

5.5.4 PARALLEL INTERFACE PROGRAMMING

5.5.4.1 Parallel Interface Configuration

The parallel interface must be configured for a specific address range (LPT1, LPT2, etc.) and also must be enabled before it can be used. When configured for EPP or ECP mode, additional considerations must be taken into account. Address selection, enabling, and EPP/ECP mode parameters of the parallel interface are affected through the non-shaded bits of the following configuration registers of the 87306 I/O controller. Address selection and enabling are automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

Function Enable Register, Indexed Addr. 399.00h

Bit	Function
7	Not used on this system
6	IDE Enable (always = 0 on this system)
5	Diskette Drive Controller Base Address Select 0 = Primary address (3F1h), 1 = Secondary address (371h)
4	Diskette Drive Controller Encoding (always = 0 on this system)
3	Diskette Drive Controller Enable: 0 = Disabled, 1 = Enabled
2	Not used on this system.
1	Serial Interface (UART 1) Enable: 0 = Disabled, 1 = Enabled
0	Parallel Interface Enable: 0 = Disabled, 1 = Enabled

Non-related functions.

Function Address Register, Indexed Addr. 399.01h

Bit	Function
7,6	COM3/COM4 Base Address Selection COM3 IRQ4 COM4 IRQ3 00 = 3E8h 2E8h 01 = 338h 238h 10 = 2E8h 2E0h 11 = 220h 228h
5,4	Not used on this system.
3,2	Serial Interface COMn Select: 00 = COM1 10 = COM3 (refer to bits <7,6>) 01 = COM2 11 = COM4 (refer to bits <7,6>)
1,0	Parallel Interface Base Address (LPTn) & IRQ Select: 00 = 378h (LPT1), IRQ5 10 = 278h (LPT2), IRQ5 01 = 3BCh (LPT3), IRQ7 11 = Reserved

Non-related functions.

Printer Control Register, Indexed Addr. 399.04h

Bit	Function
7	RTC RAM Mask
6	Parallel I/F Interrupt Control 0 = Interrupt line has Tristate output 1 = Interrupt line has open drain output (drive low or tristate).
5	Parallel I/F Interrupt Polarity 0 = Polarity defined by SIO3 register 1 = Polalrity is inverted
4	Reserved
3	ECP Clock Freeze 0 = ECP mode does not affect stopping of crystal. 1 = Crystal/ECP clock is not stopped in ECP mode.
2	ECP Mode Enable/Disable 0 = Disabled 1 = Enabled
1	EPP Version Select: 0 = Ver. 1.7 1 = Ver. 1.9
0	EPP Enable/Disable 0 = Disabled 1 = Enabled (if bit <2> is 0)

Non-related functions.

Tape, UARTs, and Parallel Port Register, Indexed Addr. 399.07h

Bit	Function
7..3	Reserved
2	EPP Timeout Interupt Enable/Disable 0 = Disable 1 = Timeout interrupt is generated on selected IRQ line
1,0	Reserved

Non-related functions.

5.5.4.2 Parallel Interface Control

The BIOS function INT 17 provides simplified control of the parallel interface. Basic functions such as initialization, character printing, and printer status are provide by subfunctions of INT 17. The parallel interface is controllable by software through a set of I/O mapped registers. The number and type of registers available depends on the mode used (SPP, EPP, or ECP). Table 5-10 lists the parallel registers and associated functions based on mode.

Table 5-10.
Parallel Interface Control Registers

Register	I/O Address	SPP Mode Ports	EPP Mode Ports	ECP Mode Ports
Data	Base	LPT1,2,3	LPT1,2	LPT1,2,3
Status	Base + 1h	LPT1,2,3	LPT1,2	LPT1,2,3
Control	Base + 2h	LPT1,2,3	LPT1,2	LPT1,2,3
Address	Base + 3h	--	LPT1,2	--
Data Port 0	Base + 4h	--	LPT1,2	--
Data Port 1	Base + 5h	--	LPT1,2	--
Data Port 2	Base + 6h	--	LPT1,2	--
Data Port 3	Base + 7h	--	LPT1,2	--
Parallel Data FIFO	Base + 400h	--	--	LPT1,2,3
ECP Data FIFO	Base + 400h	--	--	LPT1,2,3
Test FIFO	Base + 400h	--	--	LPT1,2,3
Configuration Register A	Base + 400h	--	--	LPT1,2,3
Configuration Register B	Base + 401h	--	--	LPT1,2,3
Extended Control Register	Base + 402h	--	--	LPT1,2,3

Base Address:
LPT1 = 378h
LPT2 = 278h
LPT3 = 3BCh

The following paragraphs describe the individual registers. Note that only the LPT1-based addresses are given in these descriptions.

Data Register, I/O Port 378h

Data written to this register is presented to the data lines D0-D7. A read of this register when in SPP-compatible mode yields the last byte written. A read while in SPP-extended or ECP mode yields the status of data lines D0-D7 (i.e., receive data).

In ECP mode in the forward (output) direction, a write to this location places a tagged command byte into the FIFO and reads have no effect.

Status Register, I/O Port 3F9h, Read Only

This register contains the current printer status. Reading this register clears the interrupt condition of the parallel port.

Bit	Function
7	Printer Busy (if 0)
6	Printer Acknowledgment Of Data Byte (if 0)
5	Printer Out Of Paper (if 1)
4	Printer Selected/Online (if 1)
3	Printer Error (if 0)
2	Reserved
1	EPP Interrupt Occurred (if set while in EPP mode)
0	EPP Timeout Occurred (if set while in EPP mode)

Control Register, I/O Port 37Ah

This register provides the printer control functions.

Bit	Function
7,6	Reserved
5	Direction Control for PS/2 and ECP Modes: 0 = Forward. Drivers enabled. Port writes to peripheral (default) 1 = Backward. Tristates drivers and data is read from peripheral
4	Acknowledge Interrupt Enable 0 = Disable ACK interrupt 1 = Enable interrupt on rising edge of ACK
3	Printer Select (if 0)
2	Printer Initialize (if 1)
1	Printer Auto Line Feed (if 0)
0	Printer Strobe (if 0)

Address Register, I/O Port 37Bh (EPP Mode Only)

This register is used for selecting the EPP register to be accessed.

Data Port Registers 0-3, I/O Ports 37C-Fh (EPP Mode Only)

These registers are used for reading/writing data. Port 0 is used for all transfers. Ports 1-3 are used for transferring the additional bytes of 16- or 32-bit transfers through port 0.

FIFO Register, I/O Port 7F8h (ECP Mode Only)

While in ECP/forward mode, this location is used for filling the 16-byte FIFO with data bytes. Reads have no effect (except when used in Test mode). While in ECP/backward mode, reads yield data bytes from the FIFO.

Configuration Register A, I/O Port 7F8h (ECP Mode Only)

A read of this location yields 10h, while writes have no effect.

Configuration Register B, I/O Port 7F9h (ECP Mode, Read Only)

A read of this location yields the status defined as follows:

Bit	Function
7	Reserved (always 0)
6	Status of Selected IRQ*n*.
5,4	Selected IRQ Indicator: 00 = IRQ7 11 = IRQ5 All other values invalid.
3	Reserved (always 1)
2..0	Reserved (always 000)

Extended Control Register B, I/O Port 7FAh (ECP ModeOnly)

This register defines the ECP mode functions.

Bit	Function
7..5	ECP Submode Select: 000 = Standard forward mode (37Ah <5> forced to 0). Writes are controlled by software and FIFO is reset. 001 = PS/2 mode. Reads and writes are software controlled and FIFO is reset. 010 = Parallel Port FIFO forward mode (37Ah <5> forced to 0). Writes are hardware controlled. 011 = ECP FIFO mode. Direction determined by 37Ah, <5>. Reads and writes are hardware controlled.
4	ECP Interrupt Mask: 0 = Interrupt is generated on ERR- assertion. 1 = Interrupt is inhibited.
3	ECP DMA Enable/Disable. 0 = Disabled 1 = Enabled
2	ECP Interrupt Generation with DMA 0 = Enabled 1 = Disabled
1	FIFO Full Status (Read Only) 0 = Not full (at least 1 empty byte 1 = Full
0	FIFO Empty Status (Read Only) 0 = Not empty (contains at least 1 byte) 1 = Empty

5.5.5 PARALLEL INTERFACE CONNECTOR

Figure 5-4 and Table 5-11 show the connector and pinout of the parallel inrteface connector.

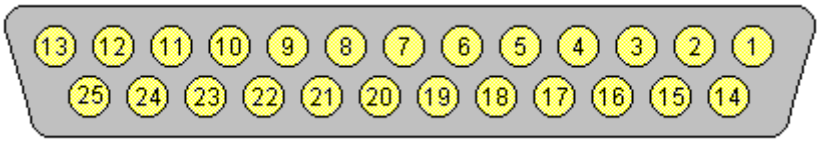


Figure 5–4. Parallel Interface Connector (Female DB-25 as viewed from rear of chassis)

Table 5-11.
DB-25 Parallel Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	STB-	Strobe	14	LF-	Line Feed
2	D0	Data 0	15	ERR-	Error
3	D1	Data 1	16	INIT-	Initialize Paper
4	D2	Data 2	17	SLCTIN-	Select In
5	D3	Data 3	18	GND	Ground
6	D4	Data 4	19	GND	Ground
7	D5	Data 5	20	GND	Ground
8	D6	Data 6	21	GND	Ground
9	D7	Data 7	22	GND	Ground
10	ACK-	Acknowledge	23	GND	Ground
11	BSY	Busy	24	GND	Ground
12	PE	Paper End	25	GND	Ground
13	SLCT	Select	--	--	--

5.6 KEYBOARD/POINTING DEVICE INTERFACE

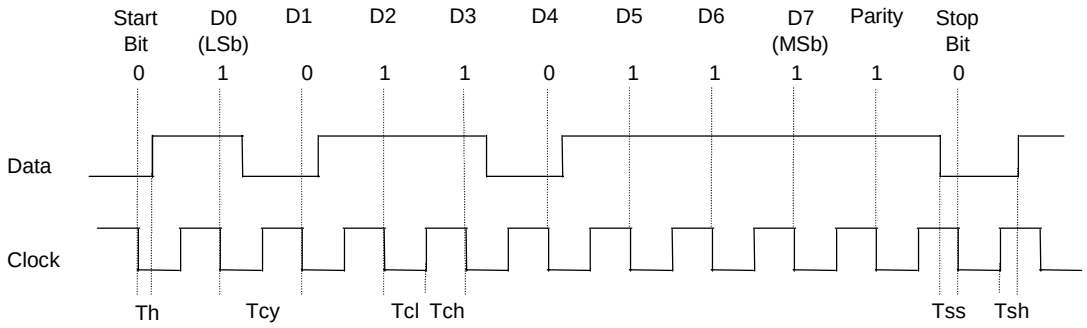
The keyboard/pointing device interface provides the connection of an enhanced keyboard and a mouse using PS/2-type connections. The keyboard/pointing device interface function is provided by the 87306 I/O controller component, which integrates 8042-compatible keyboard controller logic (hereafter referred to as simply the "8042") to communicate with the keyboard and pointing device using bi-directional serial data transfers. The 8042 handles scan code translation and password lock protection for the keyboard as well as communications with the pointing device. This section describes the interface itself. The keyboard is discussed in the Appendix B.

5.6.1 KEYBOARD INTERFACE OPERATION

The data/clock link between the 8042 and the keyboard is uni-directional for Keyboard Mode 1 and bi-directional for Keyboard Modes 2 and 3. (These modes are discussed in detail in Appendix C). This section describes Mode 2 (the default) mode of operation.

Communication between the keyboard and the 8042 consists of commands (originated by either the keyboard or the 8042) and scan codes from the keyboard. A command can request an action or indicate status. The keyboard interface uses IRQ1 to get the attention of the CPU.

The 8042 can send a command to the keyboard at any time. When the 8042 wants to send a command, the 8042 clamps the clock signal from the keyboard for a minimum of 60 us. If the keyboard is transmitting data at that time, the transmission is allowed to finish. When the 8042 is ready to transmit to the keyboard, the 8042 pulls the data line low, causing the keyboard to respond by pulling the clock line low as well, allowing the start bit to be clocked out of the 8042. The data is then transferred serially, LSb first, to the keyboard (Figure 5-5). An odd parity bit is sent following the eighth data bit. After the parity bit is received, the keyboard pulls the data line low and clocks this condition to the 8042. When the keyboard receives the stop bit, the clock line is pulled low to inhibit the keyboard and allow it to process the data.



Parameter	Minimum	Maximum
Tcy (Cycle Time)	0 us	80 us
Tcl (Clock Low)	25 us	35 us
Tch (clock High)	25 us	45 us
Th (Data Hold)	0 us	25 us
Tss (Stop Bit Setup)	8 us	20 us
Tsh (Stop Bit Hold)	15 us	25 us

Figure 5–5. 8042-To-Keyboard Transmission of Code EDh, Timing Diagram

Control of the data and clock signals is shared by the 8042and the keyboard depending on the originator of the transferred data. Note that the clock signal is always generated by the keyboard. After the keyboard receives a command from the 8042, the keyboard returns an ACK code. If a parity error or timeout occurs, a Resend command is sent to the 8042.

Table 5-12 lists and describes commands that can be issued by the 8042 to the keyboard.

Table 5-12.
8042-To-Keyboard Commands

Command	Value	Description
Set/Reset Status Indicators	EDh	Enables LED indicators. Value EDh is followed by an option byte that specifies the indicator as follows: Bits <7..3> not used Bit <2>, Caps Lock (0 = off, 1 = on) Bit <1>, NUM Lock (0 = off, 1 = on) Bit <0>, Scroll Lock (0 = off, 1 = on)
Echo	EEh	Keyboard returns EEh when previously enabled.
Invalid Command	EFh/F1h	These commands are not acknowledged.
Select Alternate Scan Codes	F0h	Instructs the keyboard to select another set of scan codes and sends an option byte after ACK is received: 01h = Mode 1 02h = Mode 2 03h = Mode 3
Read ID	F2h	Instructs the keyboard to stop scanning and return two keyboard ID bytes.
Set Typematic Rate/Display	F3h	Instructs the keyboard to change typematic rate and delay to specified values: Bit <7>, Reserved - 0 Bits <6,5>, Delay Time 00 = 250 ms 01 = 500 ms 10 = 750 ms 11 = 1000 ms Bits <4..0>, Transmission Rate: 00000 = 30.0 ms 00001 = 26.6 ms 00010 = 24.0 ms 00011 = 21.8 ms : 11111 = 2.0 ms
Enable	F4h	Instructs keyboard to clear output buffer and last typematic key and begin key scanning.
Default Disable	F5h	Resets keyboard to power-on default state and halts scanning pending next 8042 command.
Set Default	F6h	Resets keyboard to power-on default state and enable scanning.
Set Keys - Typematic	F7h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Make/Brake	F8h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Make	F9h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Typematic/Make/Brake	FAh	Clears keyboard buffer and sets default scan code set. [1]
Set Type Key - Typematic	FBh	Clears keyboard buffer and prepare to receive key ID. [1]
Set Type Key - Make/Brake	FCh	Clears keyboard buffer and prepare to receive key ID. [1]
Set Type Key - Make	FDh	Clears keyboard buffer and prepare to receive key ID. [1]
Resend	FEh	8042 detected error in keyboard transmission.
Reset	FFh	Resets program, runs keyboard BAT, defaults to Mode 2.

Note:
[1] Used in Mode 3 only.

5.6.2 POINTING DEVICE INTERFACE OPERATION

The pointing device (typically a mouse) connects to a 6-pin DIN-type connector that is identical to the keyboard connector both physically and electrically. The operation of the interface (clock and data signal control) is the same as for the keyboard. The pointing device interface uses the IRQ12 interrupt.

5.6.3 KEYBOARD/POINTING DEVICE INTERFACE PROGRAMMING

5.6.3.1 8042 Configuration

The keyboard/pointing device interface must be enabled and configured for a particular speed before it can be used. Enabling and speed parameters of the 8042 logic are affected through the non-shaded bits of the configuration register (shown below) of the 87306 I/O controller. Enabling and speed control are automatically set by the BIOS during POST but can also be accomplished with the Setup utility and other software.

Keyboard and RTC Control Register, Indexed Addr. 399.05h

Bit	Function
7	8042 Clock Source Select: 0 = X1 clock 1 = SYSCLK
6	Reserved
5	RAMSEL (CMOS Bank Select): 0 = Lower CMOS area 1 = Higher CMOS area
4	Reserved
3	RTC Enable: 0 = Disabled 1 = Enabled
2	Reserved (but must read/write 1 for 8042 functionality)
1	8042 Speed Control (In effect if bit <7> is 0) 0 = 8042 clock = X1 freq. / 3 (8 MHz nom.) 1 = 8042 clock = X1 freq. / 2 (12 MHz nom.)
0	8042 Enable: 0 = Disable (8042 clock inhibited) 1 = Enable

Non-related functions.

5.6.3.2 8042 Control

The BIOS function INT 16 is typically used for controlling interaction with the keyboard. Sub-functions of INT 16 conduct the basic routines of handling keyboard data (i.e., translating the keyboard's scan codes into ASCII codes). The keyboard/pointing device interface is accessed by the CPU through I/O mapped ports 60h and 64h, which provide the following functions:

- Output buffer reads
- Input buffer writes
- Status reads
- Command writes

Ports 60h and 64h can be accessed using the IN instruction for a read and the OUT instruction for a write. Prior to reading data from port 60h, the "Output Buffer Full" status bit (64h, bit <0>) should be checked to ensure data is available. Likewise, before writing a command or data, the "Input Buffer Empty" status bit (64h, bit <1>) should also be checked to ensure space is available.

I/O Port 60h

I/O port 60h is used for accessing the input and output buffers. This register is used to send and receive data from the keyboard and the pointing device. This register is also used to send the second byte of multi-byte commands to the 8042 and to receive responses from the 8042 for commands that require a response.

A read of 60h by the CPU yields the byte held in the output buffer. The output buffer holds data that has been received from the keyboard and is to be transferred to the system.

A CPU write to 60h places a data byte in the input byte buffer and sets the CMD/ DATA bit of the Status register to DATA. The input buffer is used for transferring data from the system to the keyboard. All data written to this port by the CPU will be transferred to the keyboard **except** bytes that follow a multibyte command that was written to 64h

I/O Port 64h

I/O port 64h is used for reading the status register and for writing commands. A read of 64h by the CPU will yield the status byte defined as follows:

Bit	Function
7..4	General Purpose Flags.
3	CMD/DATA Flag (reflects the state of A2 during a CPU write). 0 = Data 1 = Command
2	General Purpose Flag.
1	Input Buffer Full. Set (to 1) upon a CPU write. Cleared by IN A, DBB instruction.
0	Output Buffer Full (if set). Cleared by a CPU read of the buffer.

A CPU write to I/O port 64h places a command value into the input buffer and sets the CMD/DATA bit of the status register (bit <3>) to CMD. Table 5-13 lists the commands that can be sent to the 8042 by the CPU. The 8042 uses IRQ1 for gaining the attention of the CPU.

Table 5-13.
CPU Commands To The 8042

Value	Command Description
20h	Put current command byte in port 60h.
60h	Load new command byte. This is a two-byte operation described as follows: 1. Write 60h to port 64h. 2. Write the command byte to port 60h as follows: Bit <7> Reserved <6> Keyboard Code Conversion 0 = Do not convert codes 1 = Convert codes to 9-bit 8088/8086-compatible format Bit <5> Pointing Device Enable 0 = Enable pointing device 1 = Disable pointing device Bit <4> Keyboard Enable 0 = Enable keyboard 1 = Disable keyboard Bit <3> Reserved Bit <2> System Flag 0 = Cold boot 1 = CPU reset (exit from protected mode) Bit <1> Pointing Device Interrupt Enable 0 = Disable interrupt 1 = Enable interrupt Bit <0> Keyboard Interrupt Enable 0 = Disable interrupt 1 = Enable interrupt
A4h	Test password installed. Tests whether or not a password is installed in the 8042: If FAh is returned, password is installed. If F1h is returned, no password is installed.
A5h	Load password. This multi-byte operation places a password in the 8042 using the following manner: 1. Write A5h to port 64h. 2. Write each character of the password in 9-bit scan code (translated) format to port 60h. 3. Write 00h to port 60h.
A6h	Enable security. This command places the 8042 in password lock mode following the A5h command. The correct password must then be entered before further communication with the 8042 is allowed.
A7h	Disable pointing device. This command sets bit <5> of the 8042 command byte, pulling the clock line of the pointing device interface low.
A8h	Enable pointing device. This command clears bit <5> of the 8042 command byte, activating the clock line of the pointing device interface.
A9h	Test the clock and data lines of the pointing device interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
AAh	Initialization. This command causes the 8042 to inhibit the keyboard and pointing device and places 55h into the output buffer.
ABh	Test the clock and data lines of the keyboard interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
ADh	Disable keyboard command (sets bit <4> of the 8042 command byte).
AEh	Enable keyboard command (clears bit <4> of the 8042 command byte).

Continued

Table 5-13. CPU Commands To The 8042 *(Continued)*

Value	Command Description
C0h	Read input port of the 8042. This command directs the 8042 to transfer the contents of the input port to the output buffer so that they can be read at port 60h. The contents are as follows: Bit <7> Password Enable: 0 = Disabled 1 = Enabled Bit <6> External Boot Enable: 0 = Enabled 1 = Disabled Bit <5> Setup Enable: 0 = Enabled 1 = Disabled Bit <4> VGA Enable: 0 = Enabled 1 = Disabled Bit <3> Diskette Writes: 0 = Disabled 1 = Enabled Bit <2> Reserved Bit <1> Pointing Device Data Input Line Bit <0> Keyboard Data Input Line
C2h	Poll Input Port High. This command directs the 8042 to place bits <7..4> of the input port into the upper half of the status byte on a continous basis until another command is received.
C3h	Poll Input Port Low. This command directs the 8042 to place bits <3..0> of the input port into the lower half of the status byte on a continous basis until another command is received.
D0h	Read output port. This command directs the 8042 to transfer the contents of the output port to the output buffer so that they can be read at port 60h. The contents are as follows: Bit <7> Keyboard data stream Bit <6> Keyboard clock Bit <5> IRQ12 (pointing device interrupt) Bit <4> IRQ1 (keyboard interrupt) Bit <3> Pointing device clock Bit <2> Pointing device data Bit <1> A20 Control: 0 = Hold A20 low 1 = Enable A20 Bit <0> Reset Line Status; 0 = Inactive 1 = Active
D1h	Write output port. This command directs the 8042 to place the next byte written to port 60h into the output port (only bit <1> can be changed).
D2h	Echo keyboard data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the keyboard. No 11-to-9 bit translation takes place but an interrupt (IRQ1) is generated if enabled.
D3h	Echo pointing device data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the pointing device. An interrupt (IRQ12) is generated if enabled.
D4h	Write to pointing device. Directs the 8042 to send the next byte written to 60h to the pointing device.
E0h	Read test inputs. Directs the 8042 to transfer the test bits 1 and 0 into bits <1,0> of the output buffer.
F0h-FFh	Pulse output port. Controls the pulsing of bits <3..0> of the output port (0 = pulse, 1 = don't pulse). Note that pulsing bit <0> will reset the system.

5.6.4 KEYBOARD/POINTING DFEVICE INTERFACE CONNECTOR

There are separate connectors for the keyboard and pointing device. Both connectors are identical both physically and electrically. Figure 5-6 and Table 5-14 show the connector and pinout of the keyboard/pointing device interface connectors.

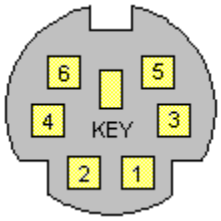


Figure 5–6. Keyboard or Pointing Device Interface Connector (as viewed from rear of chassis)

Table 5-14.
Keyboard/Pointing Device Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	DATA	Data	4	+ 5 VDC	Power
2	NC	Not Connected	5	CLK	Clock
3	GND	Ground	6	NC	Not Connected

5.7 UNIVERSAL SERIAL BUS INTERFACE

The Universal Serial Bus (USB) interface (not present on early Pentium-based systems) provides up to 12 Mb/s data transfers between the host system and peripherals designed with a compatible USB interface. This high speed interface supports hot-plugging of compatible devices, making possible system configuration changes without powering down or even rebooting systems. The USB interface supports both isochronous and asynchronous communications, and integrates a 5 VDC power bus that can eliminate the need for external powering of small remote peripherals.

Table 5-15.
USB Interface Configuration Registers

PCI Config. Addr.	Register	Reset Value
00h-01h	Vender ID	8086h
02h-03h	Device ID	7020h
04h-05h	PCI Command	0000h
06h-07h	PCI Status	0280h
08h	Revision ID	00h
09h	Programming I/F	00h
0Ah	Sub Class Code	03h
0Bh	Base Class Code	0Ch
0Dh	Latency Timer	00h
0Eh	Header Type	80h
24h-27h	I/O Space Base Address	All 0's
3Ch	Interrupt Line	00h
3Dh	Interrupt Pin	04h
60h	Serial Base Release Number	00h

NOTE:
PCI configuration space resides in 82371(device 7), function 2.

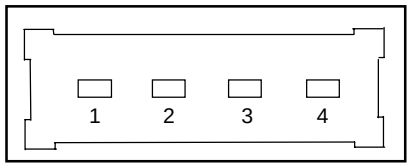


Figure 5–7. Universal Serial Bus Connector (as viewed from rear of chassis)

Table 5-16.
USB Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	Vcc	+5 VDC	3	USB+	Data (plus)
2	USB-	Data (minus)	4	GND	Ground

Chapter 6
GRAPHICS SUBSYSTEM

6.1 INTRODUCTION

This chapter describes the graphics subsystem used in the Compaq Deskpro 2000 Series of Personal Computers. Depending on model, the graphics subsystem is either integrated onto the system board or contained on a separate card that is installed in a PCI slot. All graphics subsystems are backward-compatible with software written for VGA, EGA, and CGA graphics modes. Topics covered in this chapter include:

NOTE: This chapter provides an overview of graphics subsystem architecture and it's capabilities. Common graphics modes (VGA, EGA, and CGA) and text modes are not discussed in detail nor are programmable registers described in detail in this chapter. For additional information on graphics controller operation and control refer to the applicable Cirrus Logic and Matrox documentation.

6.2 SUBSYSTEM DIFFERENCES OVERVIEW

The graphics subsystem of all models operates off the PCI bus. Table 6-1 outlines the key differences between the graphics subsystems.

Table 6-1.
Graphics Subsystem Comparison

Parameter	Integrated Subsystem	Cirrus Logic Card	Matrox Millennium Card
Graphics Controller	CL-GD5436	CL-GD5446	MGA 2064W
Graphics Memory			
Standard installed:	1 MB EDO	1 MB EDO	2 MB WRAM
Expandable to:	2 MB EDO	2 MB EDO	8 MB WRAM
Maximum Resolution			
w/ standard memory	1280x1024 @ 16 colors	1280x1024 @ 16 colors	1600x1200 @ 256 colors
w/ max. memory	1280x1024 @ 256 colors	1280x1024 @ 256 colors	1600x1200 @ 16M colors

The standard graphics controllers used in the Deskpro 2000 Series are PCI bus types that can be identified by software reading the "Vendor ID" and "Device ID" words in PCI configuration address space locations 00h and 02h respectively. The values are as follows:

Vendor ID	Device ID	Graphics ASIC	System
1013h	00ACh	GD5436	Pentium-based
1013h	00B8h	GD5446	180-MHz Pentium Pro-based
102Bh	0519h	MGA 2064W	200-MHz Pentium Pro-based

6.3 INTEGRATED GRAPHICS SUBSYSTEM

The Pentium-based system integrates the graphics subsystem (Figure 6-1) onto the system board and consists of the GD5436 graphics controller and one megabyte of EDO DRAM as standard for the frame buffer memory. The graphics BIOS code is included in the system BIOS ROM.

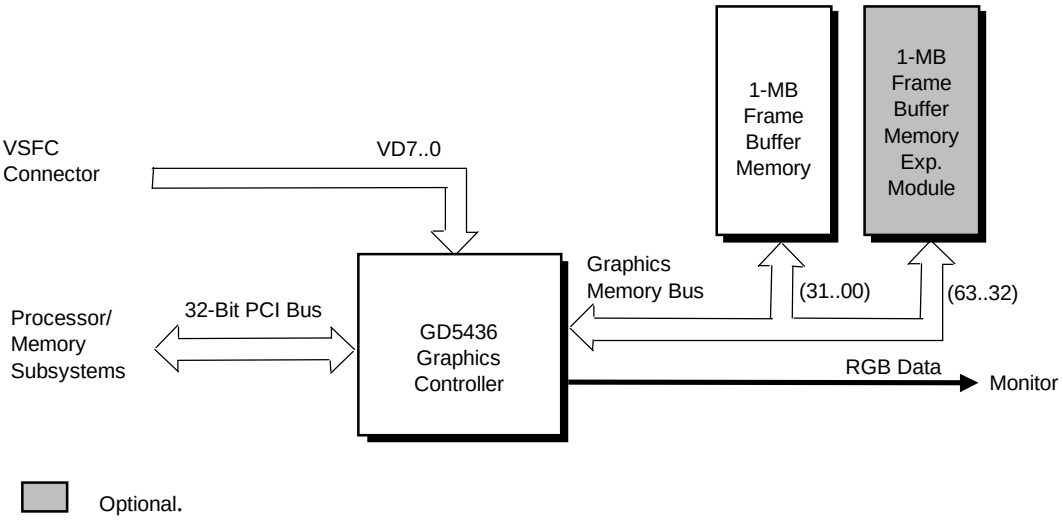


Figure 6–1. Integrated Graphics Subsystem Block diagram

The standard frame buffer configuration provides a 32-bit bandwidth with the GD5436. The frame buffer memory can be expanded to two megabytes with the addition of a 1-MB EDO DRAM module (Figure 6-4). Adding the expansion module increases the bandwidth to 64 bits.

6.3.1 CL-GD5436 GRAPHICS CONTROLLER

The GD5436 graphics controller provides most of the functionality of the integrated graphics subsystem and contains the features listed below:

- 64-bit GUI acceleration
- 64-bit EDO DRAM interface support
- Integrated 24-bit DAC
- Memory mapping of BitBLT functions
- VESA standard feature port
- VESA DDC1 and DDC2B support
- Green PC power management support

Figure 6-2 shows the basic architecture of the GD5436, which is compatible with software written for VGA, EGA, and CGA modes. Drivers are supplied for control of graphics (GUI) accelerator engines used in extended VGA modes. The GD5436 includes multimedia support such as video overlay and DAC mode switching as well as VESA advanced feature connector (VAFC) baseline support.

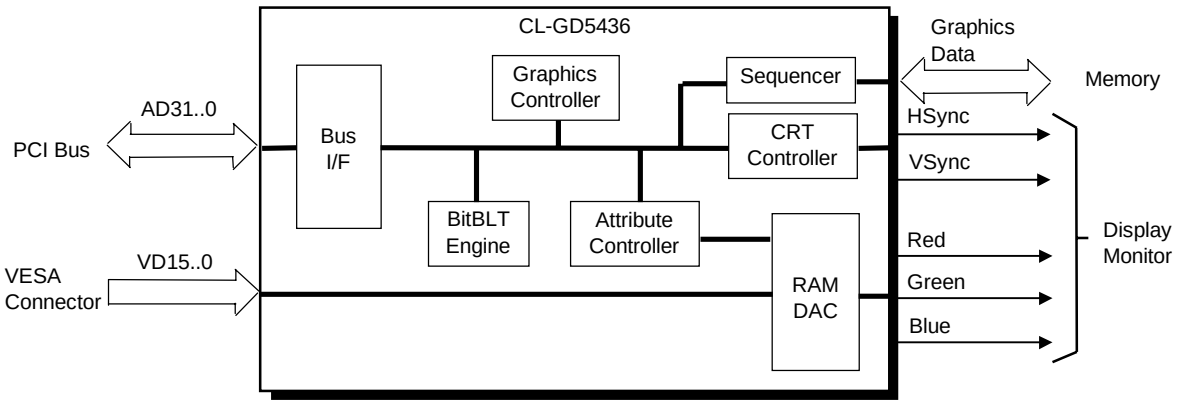


Figure 6–2. CL-GD5436 Graphics Controller Internal Architecture

The GD5436 graphics controller provides increased performance over the GD5434 component used in previous systems. The performance increase is due mainly to higher refresh clocks and support for using EDO DRAM for the frame buffer. The chart shown in Figure 6-3 illustrates the increased WinBench 95 score possible with the GD5436 depending on the amount of graphics memory installed and whether or not an L2 cache is employed.

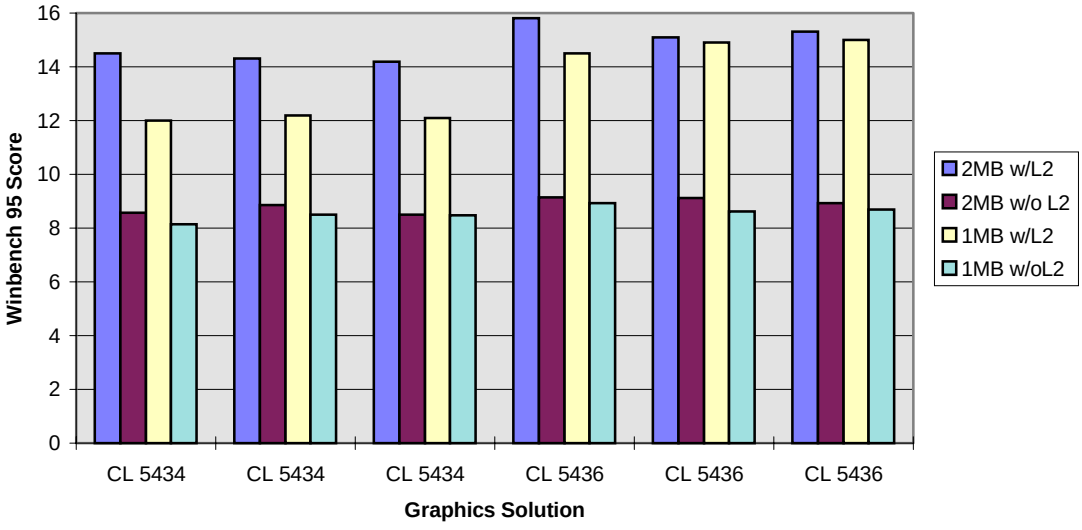


Figure 6–3. GD5436 / GD5434 WinBench 95 Performance Comparison at 1024 x 768 x 256 @ 60 Hz

6.3.2 DISPLAY CONFIGURATIONS

The integrated graphics controller provides one of two type of displays; text or graphics.

6.3.2.1 Text Configurations

The text display uses a multiplane configuration where a character, its attributes, and fonts are stored in separate frame buffer memory planes. Table 6-4 lists the text configurations provided by the graphics subsystem. Note that text configurations for CGA.MDA, EGA, and VGA share common video BIOS modes that result in same format, but provide different pixel resolutions.

Table 6-2.
Text Configuration Display Modes

Software Interface	BIOS Mode	Pixel Resolution	Color Depth	Format
CGA	00h	320 x 200	16	40 x 25
	01h	320 x 200	16	40 x 25
	02h	640 x 200	16	80 x 25
	03h	640 x 200	16	80 x 25
MDA	07h	720 x 350	Mono	80 x 25
EGA	00h	320 x 350	16	40 x 25
	01h	320 x 350	16	40 x 25
	02h	640 x 350	16	80 x 25
	03h	640 x 350	16	80 x 25
VGA	00h	360 x 400	16	40 x 25
	01h	360 x 400	16	40 x 25
	02h	720 x 400	16	80 x 25
	03h	720 x 400	16	80 x 25
	07h	720 x 400	Mono	80 x 25
EVGA	14h	1056 x 400	16	132 x 25
	45h	1056 x 350	16	132 x 43
	55h	1056 x 350	16	132 x 25

6.3.2.2 Graphics Configurations

The integrated graphics subsystem can operate in one of two graphics configurations: multiplane and packed pixel. The multiplane (MP) configuration provides four planes in frame buffer memory, each plane simultaneously supplying one bit of the 4-bit code that defines the color for a pixel. The packed pixel (PP) configuration allows software to use as many as 32 bits to determine the color of a pixel. The graphics modes supported by both the GD5436 and its video BIOS are listed in Table 6-3.

Table 6-3.
Integrated Graphics Subsystem
Graphics Configuration Display Modes

Software Interface	BIOS Mode	Pixel Resolution	Color Depth	Exp. Mem. Module Required?
CGA	04h	320 x 200 @ 2 bpp	4	No
	05h	320 x 200 @ 2 bpp	4	No
	06h	640 x 200 @ 1 bpp	2	No
EGA	0Dh	320 x 200 (MP)	16	No
	0Eh	640 x 200 (MP)	16	No
	0Fh	640 x 350 (MP)	Mono	No
	10h	640 x 350 (MP)	16	No
VGA	11h	640 x 480 (MP)	2	No
	12h	640 x 480 (MP)	16	No
	13h	320 x 200 @ 8 bpp	256	No
EVGA	5Ch	800 x 600 @ 8 bpp	256	No
	5Fh	640 x 480 @ 8 bpp	256	No
	60h	1024 x 768 @ 8 bpp	256	No
	64h	640 x 480 @ 16 bpp	64K	No
	65h	800 x 600 @ 16 bpp	64K	No
	66h	640 x 480 @ 15 bpp	32K	No
	67h	800 x 600 @ 15 bpp	32K	No
	68h	1024 x 768 @ 15 bpp	32K	Yes
	71h	640 x 480 @ 32 bpp	16M	No
	74h	1024 x 768 @ 16 bpp	64K	Yes
	78h	800 x 600 @ 32 bpp	16M	Yes

6.3.3 INTEGRATED GRAPHICS SUBSYSTEM PROGRAMMING

6.3.3.1 Subsystem Configuration

The integrated graphics subsystem works off the PCI bus and is configured through the GD5436's PCI configuration space registers (listed in Table 6-4) using PCI protocol. These registers are configured by BIOS during POST to the default configuration.

Table 6-4.
GD5436 PCI Configuration Space Registers

PCI Config. Address	Function	PCI Config. Address	Function
00h	Vender ID (1013h)/Device ID (00ACh)	14h	Relocateable I/O Base Address
04h	PCI Command	30h	Expansion ROM Base Address
08h	Status	3Ch	Interrupt Line / Interrupt Pin
10h	Display Memory Base Address	--	--

For a discussion of accessing PCI configuration space registers refer to chapter 4. For a detailed description of registers refer to the *Cirrus Logic Alpine VGA Family CL-GD543X/4X Technical Reference Manual*, p/n 385439-004.

6.3.3.2 Subsystem Control

Tables 6-5 through 6-7 list the control registers of the GD5436. For a detailed description of the registers refer to the *Cirrus Logic Alpine VGA Family CL-GD543X/'4X Technical Reference Manual*, p/n 385439-004.

Table 6-5.
Standard VGA Mode I/O Mapping

I/O Address	Function	I/O Address	Function
3B5.00..26h*	CRT Controller (mono)	3C6h..3C9h	RAMDAC
3BAh	VSYNC Control, Display Status	3CAh	Read VSYNC Status
3C1.00..14h*	Attribute Controller	3CCh	Misc. Control, Read
3C2h	Misc. Control / Status	3CF.00..08h	Graphics Controller
3C5h.00..04h*	Sequencer	3D5.00..26h*	CRT Controller (color)
--	--	3DAh	VSYNC Control, Display Status (color)

* Index at base minus 1 (i.e., if base is 3B5h, index is at 3B4h.

Table 6-6 lists the control registers used for operating the graphics accelerators used in extended VGA modes.

Table 6-6.
Extended VGA Mode I/O Mapping

I/O Address	Function	I/O Address	Function
3C5.00..04h [1]	Sequencer	3CFh	BitBLT Engine
3CF.00..15h [2]	Graphics Controller	3D5.19..27h [3]	CRT Controller (color)

[1] Index at 3C4h
[2] Index at 3CEh
[3] Index at 3D4h

The GD5436 allows for memory-mapping of the registers that control BitBLT functions (Table 6-7) for increased performance of up to four times that of I/O operation. Memory-mapped I/O is enabled by writing a "1" to bit <2> of extended register 3C5.17h. Graphics controller 3CF.06h bits <3,2> must be written as "01" to specify a 64-KB display memory window (A000:0 to AFFF:F). A 256-byte block of memory space is reserved beginning at B800:0. The BitBLT registers, which are all write-only except for the Start/Status register, can be accessed using byte, word, or dword cycles.

Table 6-7.
Extended VGA Mode Memory-Mapped I/O

Memory Offset	Function	Memory Offset	Function
00h	Background Color Byte 0	0Fh	BLT Source Pitch Byte 1
01h	Background Color Byte 1	10h	BLT Destination Address Byte 0
04h	Foreground Color Byte 0	11h	BLT Destination Address Byte 1
05h	Foreground Color Byte 1	12h	BLT Destination Address Byte 2
08h	BLT Width Byte 0	14h	BLT Source Address Byte 0
09h	BLT Width Byte 1	15h	BLT Source Address Byte 1
0Ah	BLT Height Byte 0	16h	BLT Source Address Byte 2
0Bh	BLT Height Byte 1	18h	BLT Mode
0Ch	BLT Destination Pitch Byte 0	1Ah	BLT Raster Operation(ROP)
0Dh	BLT Destination Pitch Byte 1	40h	BLT Start/Status
0Eh	BLT Source Pitch Byte 0	--	--

NOTES:

All locations are write-only except for 40h.
Locations 02h, 03h, 06h, 07h, 19h, 1Bh, 1C..3Fh, 41..FFh are reserved.

6.4 CIRRUS LOGIC GRAPHICS CARD

The 180-MHz Pentium Pro-based systems include a Cirrus Logic GD5446-based graphics card (Figure 6-4). This card contains one megabyte of EDO DRAM frame buffer memory expandable to 2 megabytes with an optional 1-MB module. The graphics BIOS code is contained in BIOS ROM.

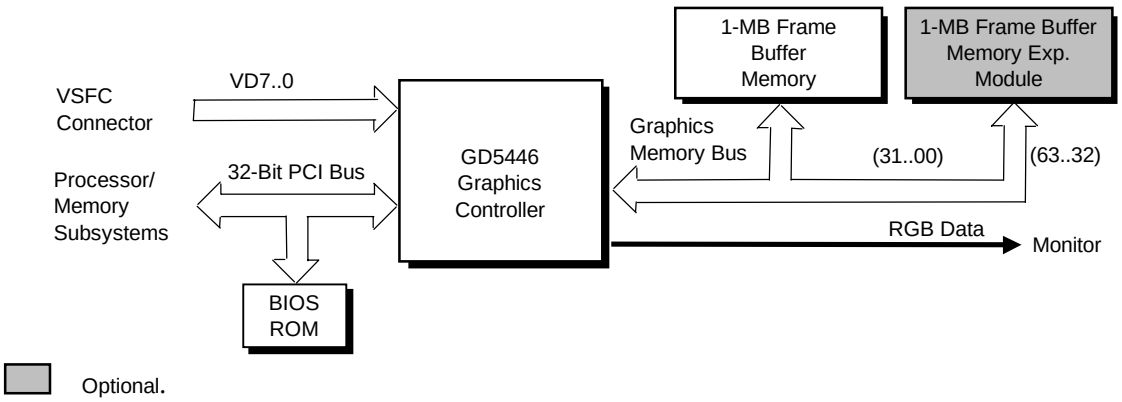


Figure 6–4. Cirrus Logic Graphics Card Block diagram

6.4.1 CL-GD5446 GRAPHICS CONTROLLER

The Cirrus Logic GD5446 graphics controller is software-compatible with the GD5436 controller described for the integrated graphics subsystem. Graphic modes listed in Tables 6-4 and 6-5 are applicable to the GD5446. The programming and control interfaces identified in Tables 6-6 through 6-8 are also applicable the GD5446. Figure 6-5 shows the internal architecture of the GD5446. The primary difference from the GD5436 is the GD5446's additional video processing capability. The GD5446 accelerates video playback by providing format conversion, interpolated x and y zooming, and color space conversion for the video display area (window).

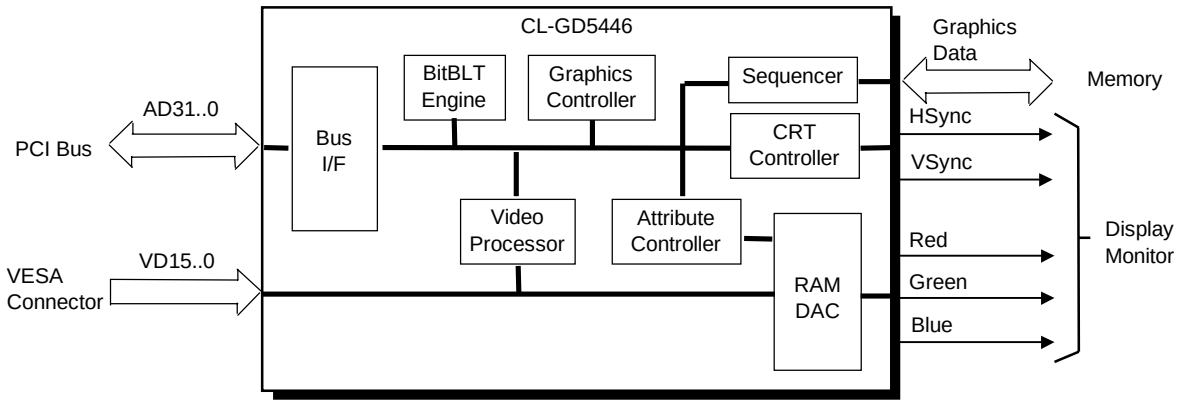


Figure 6–5. CL-GD5446 Graphics Controller Internal Architecture

6.5 MATROX MGA MILLENNIUM GRAPHICS CARD

The 200-MHz Pentium Pro-based system comes standard with the Matrox MGA Millennium Graphics Controller card that is installed in a PCI slot. This graphics card (Figure 6-6) is based on the MGA 2064W graphics controller and comes standard with two megabytes of WRAM for the frame buffer. The RAMDAC functions are provided by the TVP 3026 component. The graphics BIOS is contained in a separate ROM.

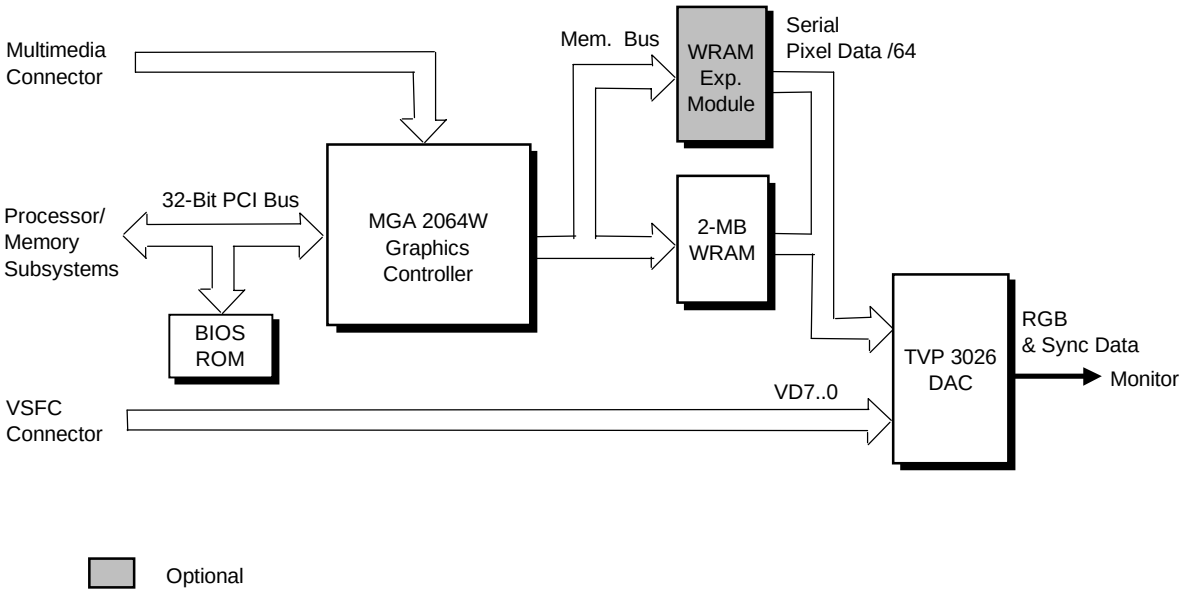


Figure 6–6. Matrox MGA Millennium Graphics Card Block diagram

The Matrox Millennium Graphics Card includes the following features:

- Hardware-accelerated true-color mode support
- Hardware-assited texture mapping
- Aligned BitBLT support
- WRAM Dual-color block write mode support
- Phase-Locked-Loop (PLL) clock select for programmable dot/memory frequencies
- Hardware cursor controller (64x64x2 cursor) compatible with XGA and X-Windows
- Overscan support for creating custom screen borders

The Windows RAM (WRAM) used by the Millennium card provides high performance for full motion video requirements. By handling most block transfers (BLTs) internally, the WRAM relieves the graphics controller from having to provide direct support for most video and drawing tasks.

6.5.1 DISPLAY CONFIGURATIONS

The Matrox Millennium graphics card provides one of two type of displays; text or graphics.

6.5.1.1 Text Configurations

The Matrox Millennium graphics card provides the same level of text mode support as does the previously described graphics subsystems. Refer to table 6-4 for the text configurations.

6.5.1.2 Graphics Configurations

The Matrox Millennium graphics card directly supports standard CGA, EGA, and VGA modes (refer to table 6-5). Using the supplied drivers, the Matrox Millennium graphics card supports the extended VGA modes listed in the following table:

Table 6-8.
Matrox Millennium Graphics Card
Extended VGA Display Modes

VESA Mode	Pixel Resolution	Color Depth	Max. Refresh Rate [1]	Amount of WRAM Required
100h	640 x 400 @ 8 bpp	256	200 Hz	2 MB
101h	640 x 480 @ 8 bpp	256	200 Hz	2 MB
102h	800 x 600 @ 4 bpp	16	200 Hz	2 MB
103h	800 x 600 @ 8 bpp	256	200 Hz	2 MB
104h	1024 x 768 @ `4 bpp	16	130 Hz	2 MB
105h	1024 x 768 @ 8 bpp	256	130 Hz	2 MB
107h	1280 x 1024 @ 8 bpp	256	100 Hz	2 MB
110h	640 x 480 @ 15 bpp	32K	200 Hz	2 MB
111h	640 x 480 @ 16 bpp	64K	200 Hz	2 MB
112h	640 x 480 @ 32 bpp	16M	200 Hz	2 MB
113h	800 x 600 @ 15 bpp	32K	200 Hz	2 MB
114h	800 x 600 @ 16 bpp	64K	200 Hz	2 MB
115h	800 x 600 @ 32 bpp	16M	200 Hz	2 MB
116h	1024 x 768 @ 15 bpp	32K	130 Hz	2 MB
117h	1024 x 768 @ 16 bpp	64K	130 Hz	2 MB
118h	1024 x 768 @ 32 bpp	16M	130 Hz	4 MB
119h	1280 x 1024 @ 15 bpp	32K	100 Hz	4 MB
11Ah	1280 x 1024 @ 16 bpp	64K	100 Hz	4 MB
11Bh	1280 x 1024 @ 32bpp	16M	100 Hz	8 MB
11Ch	1600 x 1200 @ 8 bpp	256	78 Hz	2 MB
11Dh	1600 x 1200 @ 15 bpp	32K	78 Hz	4 MB
11Eh	1600 x 1200 @16 bpp	64K	78 Hz	4 MB

NOTES:

[1] Default refresh rate for VESA modes is 60 Hz. Higher rates can be set through MGA CAD and DOS software.

Operation is non-interleaved for all modes. The Matrox Millennium graphics card includes a ROM that contains the video graphics BIOS firmware and is directly compatible with software written for VGA, EGA, and CGA modes. For extended graphics modes, drivers are supplied with systems that include this card. For detailed programming information refer to appropriate Matrox documentation.

6.6 GRAPHICS SUBSYSTEM CONNECTORS

There are two connectors associated with the graphics subsystem; the display monitor connector and the VGA passthrough connector (also known as the VESA Standard Feature Connector (VSFC)).

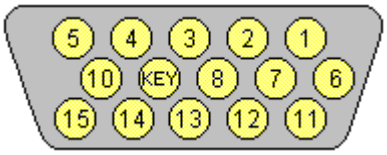


Figure 6–7. VGA Monitor Connector, (Female DB-15, as viewed from the rear of chassis).

Table 6-9.
DB-15 Monitor Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	R	Red Analog	9	NC	Not Connected
2	G	Blue Analog	10	GND	Ground
3	B	Green Analog	11	Mon. ID	Monitor Identification
4	Mon ID	Monitor Identification	12	SDA	DDC2-B Data
5	GND	Ground	13	HSync	Horizontal Sync
6	R GND	Red Analog Ground	14	VSync	Vertical Sync
7	G GND	Blue Analog Ground	15	SCL	DDC2-B Clock
8	B GND	Green Analog Ground	--	--	--

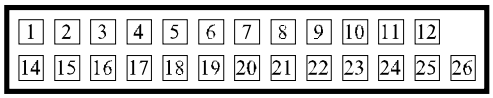


Figure 6–8. VGA Pass-Through Connector (VSFC) (26-Pin Header)

Table 6-10.
VGA Passthrough Connector (VSFC) Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	14	P0	Pixel Data 0
2	GND	Ground	15	P1	Pixel Data 1
3	GND	Ground	16	P2	Pixel Data 2
4	EVIDEO-	Overlay Enable	17	P3	Pixel Data 3
5	ESYNC-	External Sync Enable	18	P4	Pixel Data 4
6	EDCLK	External Clock Enable	19	P5	Pixel Data 5
7	NC	not connected	20	P6	Pixel Data 6
8	GND	Ground	21	P7	Pixel Data 7
9	GND	Ground	22	DCLK	Pixel Data Clock
10	GND	Ground	23	BLANK	DAC Output Blanking
11	GND	Ground	24	HSYNC	Horizontal Sync
12	NC	not connected	25	VSYNC	Vertical Sync
13	--	KEY	26	GND	Ground

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Chapter 7
POWER SUPPLY and DISTRIBUTION

7.1 INTRODUCTION

This chapter describes the power supply and method of power distribution in the Compaq Deskpro 2000 Series Personal Computer. All models use the same switching-type power supply. Power distribution is basically similar in all models, although the PentiumPro-based system board includes additional low voltage production. Topics covered in this chapter include:

7.2 POWER SUPPLY ASSEMBLY

The power supply assembly is contained in a single unit that features a selectable input voltage: 90-135 VAC and 180-265 VAC. The power supply provides +5 VDC, -5 VDC, +12 VDC, and -12 VDC.

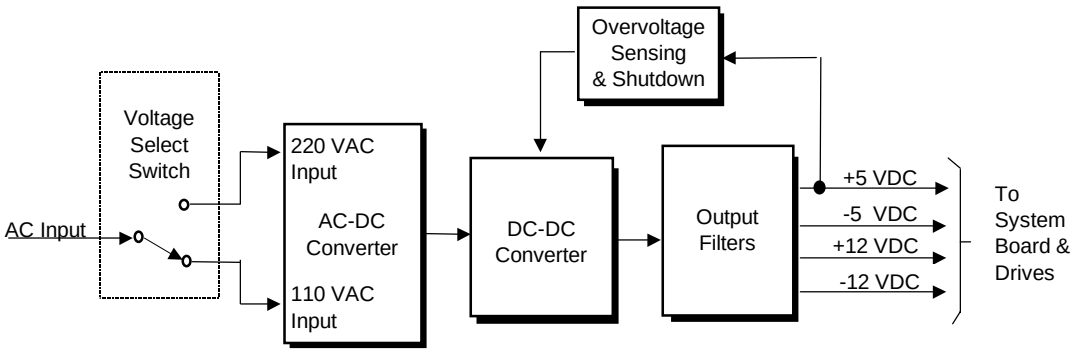


Figure 7–1. Power Supply Assembly, Block Diagram

A fault-detection circuit automatically shuts down the power supply until all faults are removed and the AC power switch is cycled (turned Off, ,then On). The minimum time period required to recycle the AC power and return to normal power supply operation is 10 seconds. Power supply faults that can trigger the protection circuitry include:

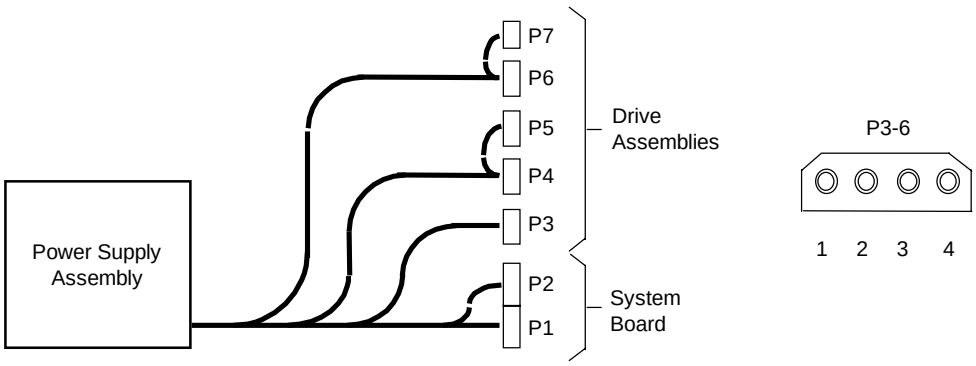
- Thermal overload - The protection circuit triggers if the power supply becomes too hot as a result of fan failure or a restriction of air flow.
- Overvoltage - The +5 VDC output will activate the overvoltage crowbar circuit that triggers the protection circuit when the output exceeds +5.60 VDC /to +6.80 VDC.
- Short Circuit - The protection circuit triggers if any power supply output is shorted to ground or to another output. This function reduces shock or fire hazard

NOTE: The minimum loading requirements for the power supply must be met at all times to ensure normal operation and to meet specifications.

7.3 POWER DISTRIBUTION

7.3.1 5/12 VDC DISTRIBUTION

The power supply assembly includes a multi-connector cable assembly that routes +5 VDC, -5 VDC, +12 VC, and -12 VDC to the system board as well as to the individual drive assemblies.



Connector	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6
P1	NC	+5	+12 VDC	-12 VDC	GND	GND
P2	GND	GND	-5 VDC	+5 VDC	+5 VDC	+5 VDC
P3-P7	+12 VDC	GND	GND	+5 VDC	--	--

Figure 7–2. Power Cable Diagram

7.3.2 LOW VOLTAGE DISTRIBUTION

The Pentium Pro-based system board includes DC/DC converters that provide low voltages (less than +5 VDC) used by various components including the microprocessor. Figure 7-3 shows a block diagram of these switching-type converters.

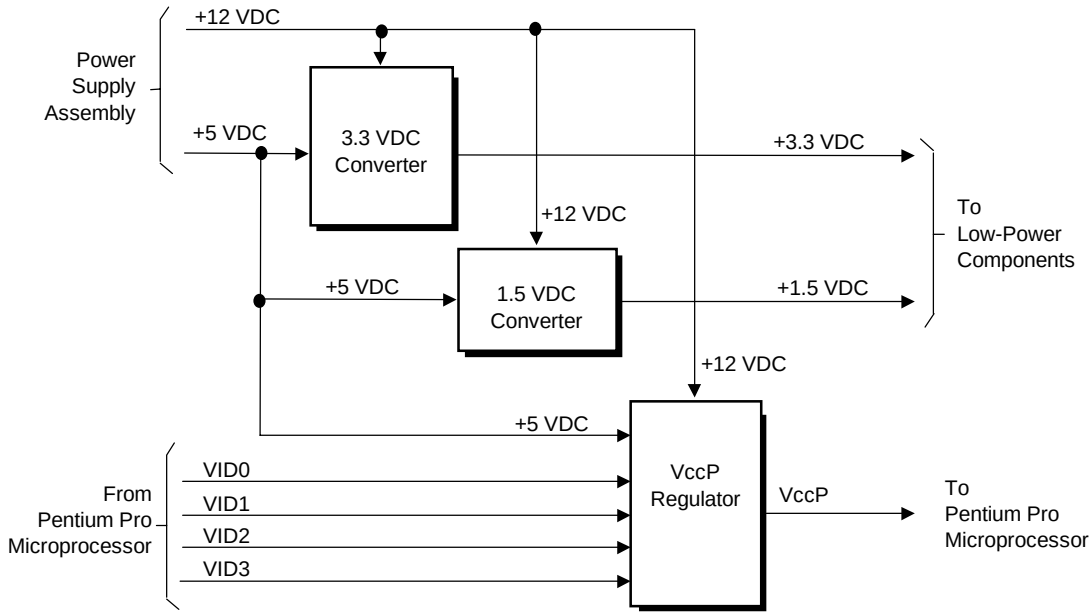


Figure 7–3. Low Voltage Power Converters, Block Diagram

The VccP regulator produces the VccP (Pentium Pro processor core) voltage according to the state of the VID3..0 signals from the Pentium Pro microprocessor. This allows automatic selection of the proper core voltage depending on the installed microprocessor component. The possible voltages available are listed as follows:

VID3..0	VccP
0000	3.5 VDC
0001	3.4 VDC
0010	3.3 VDC
0011	3.2 VDC
0100	3.1 VDC
0101	3.0 VDC
0110	2.9 VDC
0111	2.8 VDC
1000	2.7 VDC
1001	2.6 VDC
1010	2.5 VDC
1011	2.4 VDC
1100	2.3 VDC
1101	2.2 VDC
1110	2.1 VDC
1111	CPU not installed

7.4 SPECIFICATIONS

Table 7-1 shows the specifications for the power supply.

Table 7-1.
Power Supply Specifications

Parameter			
Input Line Voltage Range:			
110 VAC (North American) Setting:	90 - 132 VAC		
220 VAC Setting:	180-264 VAC		
Line Frequency	47 - 63 Hz		
Input Current Requirement:			
Cold Start:	< 80 A		
Hot Start:	< 80 A		
Maximum Steady State:	< 4.0 A rms		
Voltage Regulation:	Nominal	Regulation	
+5 VDC	+5.0	+/-5 %	
-5 VDC	-5.0	+/-10 %	
+12 VDC	+12.0	+/-5 %	
-12 VDC	-12.0	+/-10 %	
Maximum Output Ripple	1 % P/P of voltage		
Current Loading:	Minimum	Maximum	Surge
+5 VDC	1.5 A	22.0 A	26.0 A
-5 VDC	0.0 A	0.15 A	0.15 A
+12 VDC	0.1 A	7.0 A	10.0 A
-12 VDC	0.0 A	0.15 A	0.15 A

Appendix A
ERROR MESSAGES AND CODES

A.1 INTRODUCTION

This appendix lists the error codes and a brief description of the probable cause of the error. Note that not all errors listed in this appendix may be applicable to a particular system depending on the model and/or configuration.

A.2 POWER-ON MESSAGES

Table A-1.
Power-On Messages

Message	Beeps	Probable Cause
CMOS Time and Date Not Set	(None)	Invalid time or date
(none)	2 short	Power-On successful
Run Setup	(None)	Any failure

A.3 BEEP CODE MESSAGES

Table A-2.
Beep Code Messages

Beeps	Error	Probable Cause
1	Refresh Failure	Faulty memory refresh circuitry.
3	Base 64-KB Memory Failure	Memory failure in first 64-KB.
4	Timer Not Operational	Same as above or timer 1 not functioning.
5	Processor Error	CPU-generated error.
6	8042 Gate A20 Failure	Keyboard controller faulty, BIOS cannot switch to protected mode.
7	Processor Exception Interrupt Error	CPU-generated exception interrupt.
8	Display Memory R/W Error	Missing graphics/video adapter or faulty video memory (system still boots).
9	ROM Checksum Error	Checksum value does not match value in BIOS.
10	CMOS Shutdown Register R/W Error	CMOS RAM shutdown register failure.
11	Cache Error	Faulty cache.

A.4 POWER-ON SELF TEST (POST) MESSAGES

Table A-3.
Power-On Self Test (POST) Messages

Error Message	Probable Cause
Bad PnP Serial ID Checksum	Serial ID checksum of PnP card was invalid.
Address Lines Short!	Error in address decoding circuitry on system board.
Cache Memory Failure, Do Not Enable Cache!	Defective cache memory, CPU has failed.
CMOS Battery Failed	Low RTC/CMOS battery
CMOS Checksum Invalid	Previous and current checksum value mismatch.
CMOS System Options Not Set	Corrupt or non-existant CMOS values.
CMOS Display Type Mismatch	Graphics/video type in CMOS does not match type detected by BIOS.
CMOS Memory Size Mismatch	Memory amount detected does not match value stored in CMOS.
CMOS Time and Date Not Set	Time and date are invalid.
Diskette Boot Failure	Boot disk in drive A: is corrupt.
DMA Bus Timeout	Bus driven by device for more than 7.8 us
DMA Controller Error	Error in one or both DMA controllers.
Drive Not Ready Error	BIOS cannot access the diskette drive.
Diskette Drive Controller Failure	BIOS cannot communicate with diskette drive controller.
Diskette Drive Controller Resource Conflict	Diskette drive controller has requested a resource already in use.
Diskette Drive A: Failure	BIOS cannot access drive A:.
Diskette Drive B: Failure	BIOS cannot access drive B:
Gate A20 Failure	Gate A20 of keyboard controller not working.
Invalid Boot Diskette	BIOS can read but cannot boot system from drive A:.
Keyboard Controller Error	Keyboard controller failure.
Keyboard is Locked…Please Unlock It	Locked keyboard.
Keyboard Stuck Key Detected	Key pressed down.
Master DMA Controller Error	Error exists in master DMA controller.
Master Interrupt Controller Error	Master interrupt controller failure.
Memory Size Decreased	Amount of memory detected is less than stated value in CMOS.
NVRAM Checksum Error, NVRAM Cleared	ESCD data was re-initialized due to NVRAM checksum error.
NVRAM Cleared By Jumper	NVRAM has been cleared by removal of jumper.
NVRAM Data Invalid, NVRAM Cleared	Invalid entry in ESCD.
Off Board Parity Error Addr. (HEX) = X	Parity error occurred in expansion memory, x= address of error.
Parallel Port Resource Conflict	Parallel port has requested a resource already in use.
PCI Error Log is Full	PCI conflict error limit (15) has been reached.
PCI I/O Port Conflict	Two devices requested the same resource.
PCI Memory Conflict	Two devices requested the same resource.
Primary Boot Device Not Found	Designated primary boot device could not be found.
Primary IDE Cntrl. Resource Conflict	Primary IDE controller requested a resource already in use.
Primary Input Device Not Found	Designated primary input device could not be found.
Secondary IDE Controller Resource	Secondary IDE controller has requested a resource already in use.
Serial Port 1 Resource Conflict	Serial port 1 requested a resource already in use.
Serial Port 2 Resource Conflict	Serial port 2 requested a resource already in use.
Slave DMA Controller Error	Error exists in slave DMA controller.
Slave Interrupt Controller Error	Slave interrupt controller failure.
Static Device Resource Conflict	A non-PnP ISA card has requested a resource already in use.
System Board Device Resource Conflict	A non-PnP ISA card has requested a resource already in use.
System Memory Size Mismatch	Amount of memory detected on system board is different from amount indicated in CMOS.

NOTE:
PCI and PnP messages are displayed with bus, device, and function information.

A.5 PROCESSOR ERROR MESSAGES (1xx-xx)

Table A-4.
Processor Error Messages

Message	Probable Cause	Message	Probable Cause
101-01	CPU test failed	105-08	Port 61 bit <1> not at one
101-02	32-bit CPU test failed	105-09	Port 61 bit <0> not at one
101-91..94	Multiplication test failed	105-10	Port 61 I/O test failed
102-01	FPU initial sts. word incorrect	105-11	Port 61 bit <7> not at zero
102-02	FPU initial cntrl. Word incorrect	105-12	Port 61 bit <2> not at zero
102-03	FPU tag word not all ones	105-13	No interrupt generated by failsafe timer
102-04	FPU tag word not all zeros	105-14	NMI not triggered by failsafe timer
102-05	FPU exchange command failed	106-01	Keyboard controller test failed
102-06	FPU masked exception error	107-01	CMOS RAM test failed
102-07	FPU unmasked exception error	108-02	CMOS interrupt test failed
102-08	FPU wrong mask status bit set	108-03	CMOS not properly initialized (interrupt test)
102-09	FPU unable to store real number	109-01	CMOS clock load data test failed
102-10	FPU real number calc test failed	109-02	CMOS clock rollover test failed
102-11	FPU speed test failed	109-03	CMOS not properly initialized (clock test)
102-12	FPU pattern test failed	110-01	Programmable timer load data test failed
102-15	FPU is inoperative or not present	110-02	Programmable timer dynamic test failed
102-16	Weitek not responding	110-03	Program timer 2 load data test failed
102-17	Weitek failed register trnsfr. Test	111-01	Refresh detect test failed
102-18	Weitek failed arithemetic ops test	112-01	Speed test Slow mode out of range
102-19	Weitek failed data conv. Test	112-02	Speed test Mixed mode out of range
102-20	Weitek failed interrupt test	112-03	Speed test Fast mode out of range
102-21	Weitek failed speed test	112-04	Speed test unable to enter Slow mode
103-01	DMA page registers test failed	112-05	Speed test unable to enter Mixed mode
103-02	DMA byte controller test failed	112-06	Speed test unable to enter Fast mode
103-03	DMA word controller test failed	112-07	Speed test system error
104-01	Master int. cntlr. test fialed	112-08	Unable to enter Auto mode in speed test
104-02	Slave int. cntlr. test failed	112-09	Unable to enter High mode in speed test
104-03	Int. cntlr. SW RTC inoperative	112-10	Speed test High mode out of range
105-01	Port 61 bit <6> not at zero	112-11	Speed test Auto mode out of range
105-02	Port 61 bit <5> not at zero	112-12	Speed test variable speed mode inoperative
105-03	Port 61 bit <3> not at zero	113-01	Protected mode test failed
105-04	Port 61 bit <1> not at zero	114-01	Speaker test failed
105-05	Port 61 bit <0> not at zero	116-xx	Way 0 read/write test failed
105-06	Port 61 bit <5> not at one	199-00	Installed devices test failed
105-07	Port 61 bit <3> not at one	--	--

A.6 MEMORY ERROR MESSAGES (2xx-xx)

Table A-5.
Memory Error Messages

Message	Probable Cause
200-04	Real memory size changed
200-05	Extended memory size changed
200-06	Invalid memory configuration
200-07	Extended memory size changed
200-08	CLIM memory size changed
201-01	Memory machine ID test failed
202-01	Memory system ROM checksum failed
202-02	Failed RAM/ROM map test
202-03	Failed RAM/ROM protect test
203-01	Memory read/write test failed
203-02	Error while saving block in read/write test
203-03	Error while restoring block in read/write test
204-01	Memory address test failed
204-02	Error while saving block in address test
204-03	Error while restoring block in address test
204-04	A20 address test failed
204-05	Page hit address test failed
205-01	Walking I/O test failed
205-02	Error while saving block in walking I/O test
205-03	Error while restoring block in walking I/O test
206-xx	Increment pattern test failed
210-01	Memory increment pattern test
210-02	Error while saving memory during increment pattern test
210-03	Error while restoring memory during increment pattern test
211-01	Memory random pattern test
211-02	Error while saving memory during random memory pattern test
211-03	Error while restoring memory during random memory pattern test
213-xx	Incompatible DIMM in slot x
214-xx	Noise test failed
215-xx	Random address test

A.7 KEYBOARD ERROR MESSAGES (30x-xx)

Table A-6.
Keyboard Error Messages

Message	Probable Cause	Message	Probable Cause
300-xx	Failed ID test	303-05	LED test, LED command test failed
301-01	Kybd short test, 8042 self-test failed	303-06	LED test, LED command test failed
301-02	Kybd short test, interface test failed	303-07	LED test, LED command test failed
301-03	Kybd short test, echo test failed	303-08	LED test, command byte restore test failed
301-04	Kybd short test, kybd reset failed	303-09	LED test, LEDs failed to light
301-05	Kybd short test, kybd reset failed	304-01	Keyboard repeat key test failed
302-xx	Failed individual key test	304-02	Unable to enter mode 3
302-01	Kybd long test failed	304-03	Incorrect scan code from keyboard
303-01	LED test, 8042 self-test failed	304-04	No Make code observed
303-02	LED test, reset test failed	304-05	Cannot /disable repeat key feature
303-03	LED test, reset failed	304-06	Unable to return to Normal mode
303-04	LED test, LED command test failed	--	--

A.8 PRINTER ERROR MESSAGES (4xx-xx)

Table A-7.
Printer Error Messages

Message	Probable Cause	Message	Probable Cause
401-01	Printer failed or not connected	402-10	Interrupt test and control reg. failed
402-01	Printer data register failed	402-11	Interrupt test, data/cntrl. reg. failed
402-02	Printer control register failed	402-12	Interrupt test and loopback test failed
402-03	Data and control registers failed	402-13	Int. test, LpBk. test., and data register failed
402-04	Loopback test failed	402-14	Int. test, LpBk. test., and cntrl. register failed
402-05	Loopback test and data reg. failed	402-15	Int. test, LpBk. test., and data/cntrl. reg. failed
402-06	Loopback test and cntrl. reg. failed	402-16	Unexpected interrupt received
402-07	Loopback tst, data/cntrl. reg. failed	402-01	Printer pattern test failed
402-08	Interrupt test failed	498-00	Printer failed or not connected
402-09	Interrupt test and data reg. failed	--	--

A.9 VIDEO (GRAPHICS) ERROR MESSAGES (5xx-xx)

Table A-8.
Video (Graphics) Error Messages

Message	Probable Cause	Message	Probable Cause
501-01	Video controller test failed	508-01	320x200 mode, color set 0 test failed
502-01	Video memory test failed	509-01	320x200 mode, color set 1 test failed
503-01	Video attribute test failed	510-01	640x200 mode test failed
504-01	Video character set test failed	511-01	Screen memory page test failed
505-01	80x25 mode, 9x14 cell test failed	512-01	Gray scale test failed
506-01	80x25 mode, 8x8 cell test failed	514-01	White screen test failed
507-01	40x25 mode test failed	516-01	Noise pattern test failed

A.10 DISKETTE DRIVE ERROR MESSAGES (6xx-xx)

Table A-9.
Diskette Drive Error Messages

Message	Probable Cause	Message	Probable Cause
6xx-01	Exceeded maximum soft error limit	6xx-20	Failed to get drive type
6xx-02	Exceeded maximum hard error limit	6xx-21	Failed to get change line status
6xx-03	Previously exceeded max soft limit	6xx-22	Failed to clear change line status
6xx-04	Previously exceeded max hard limit	6xx-23	Failed to set drive type in ID media
6xx-05	Failed to reset controller	6xx-24	Failed to read diskette media
6xx-06	Fatal error while reading	6xx-25	Failed to verify diskette media
6xx-07	Fatal error while writing	6xx-26	Failed to read media in speed test
6xx-08	Failed compare of R/W buffers	6xx-27	Failed speed limits
6xx-09	Failed to format a tract	6xx-28	Failed write-protect test
6xx-10	Failed sector wrap test	--	--

600-xx = Diskette drive ID test
601-xx = Diskette drive format
602-xx = Diskette read test
603-xx = Diskette drive R/W compare test
604-xx = Diskette drive random seek test
605-xx = Diskette drive ID media
606-xx = Diskette drive speed test
607-xx = Diskette drive wrap test
608-xx = Diskette drive write-protect test
609-xx = Diskette drive reset controller test
610-xx = Diskette drive change line test
694-00 = Pin 34 not cut on 360-KB drive
697-00 = Diskette type error
698-00 = Drive speed not within limits
699-00 = Drive/media ID error (run Setup)

A.11 SERIAL INTERFACE ERROR MESSAGES (11xx-xx)

Table A-10.
Serial Interface Error Messages

Message	Probable Cause	Message	Probable Cause
1101-01	Port test, UART DLAB bit failure	1101-12	Port test, DRVR/RCVR cntrl. signal failure
1101-02	Port test, line input or UART fault	1101-13	Port test, UART cntrl. signal interrupt failure
1101-03	Port test, address line fault	1101-14	Port test, DRVR/RCVR data failure
1101-04	Port test, data line fault	1109-01	Clock register initialization failure
1101-05	Port test, UART cntrl. signal failure	1109-02	Clock register rollover failure
1101-06	Port test, UART THRE bit failure	1109-03	Clock reset failure
1101-07	Port test, UART Dta RDY bit failure	1109-04	Input line or clock failure
1101-08	Port test, UART TX/RX buffer failure	1109-05	Address line fault
1101-09	Port test, interrupt circuit failure	1109-06	Data line fault
1101-10	Port test, COM1 set to invalid INT	1150-xx	Comm port setup error (run Setup)
1101-11	Port test, COM2 set to invalid INT	--	--

A.12 MODEM COMMUNICATIONS ERROR MESSAGES (12xx-xx)

Table A-11.
Serial Interface Error Messages

Message	Probable Cause	Message	Probable Cause
1201-XX	Modem internal loopback test	1204-03	Data block retry limit reached [4]
1201-01	UART DLAB bit failure	1204-04	RX exceeded carrier lost limit
1201-02	Line input or UART failure	1204-05	TX exceeded carrier lost limit
1201-03	Address line failure	1204-06	Time-out waiting for dial tone
1201-04	Data line fault	1204-07	Dial number string too long
1201-05	UART control signal failure	1204-08	Modem time-out waiting for remote response
1201-06	UART THRE bit failure	1204-09	Modem exceeded maximum redial limit
1201-07	UART DATA READY bit failure	1204-10	Line quality prevented remote response
1201-08	UART TX/RX buffer failure	1204-11	Modem time-out waiting for remote connection
1201-09	Interrupt circuit failure	1205-XX	Modem auto answer test
1201-10	COM1 set to invalid inturrupt	1205-01	Time-out waiting for SYNC [5]
1201-11	COM2 set to invalid	1205-02	Time-out waiting for response [5]
1201-12	DRVR/RCVR control signal failure	1205-03	Data block retry limit reached [5]
1201-13	UART control signal interrupt failure	1205-04	RX exceeded carrier lost limit
1201-14	DRVR/RCVR data failure	1205-05	TX exceeded carrier lost limit
1201-15	Modem detection failure	1205-06	Time-out waiting for dial tone
1201-16	Modem ROM, checksum failure	1205-07	Dial number string too long
1201-17	Tone detect failure	1205-08	Modem time-out waiting for remote response
1202-XX	Modem internal test	1205-09	Modem exceeded maximum redial limit
1202-01	Time-out waiting for SYNC [1]	1205-10	Line quality prevented remote response
1202-02	Time-out waiting for response [1]	1205-11	Modem time-out waiting for remote connection
1202-03	Data block retry limit reached [1]	1206-XX	Dial multi-frequency tone test
1202-11	Time-out waiting for SYNC [2]	1206-17	Tone detection failure
1202-12	Time-out waiting for response [2]	1210-XX	Modem direct connect test
1202-13	Data block retry limit reached [2]	1210-01	Time-out waiting for SYNC [6]
1202-21	Time-out waiting for SYNC [3]	1210-02	Time-out waiting for response [6]
1202-22	Time-out waiting for response [3]	1210-03	Data block retry limit reached [6]
1202-23	Data block retry limit reached [3]	1210-04	RX exceeded carrier lost limit
1203-XX	Modem external termination test	1210-05	TX exceeded carrier lost limit
1203-01	Modem external TIP/RING failure	1210-06	Time-out waiting for dial tone
1203-02	Modem external data TIP/RING fail	1210-07	Dial number string too long
1203-03	Modem line termination failure	1210-08	Modem time-out waiting for remote response
1204-XX	Modem auto originate test	1210-09	Modem exceeded maximum redial limit
1204-01	Time-out waiting for SYNC [4]	1210-10	Line quality prevented remote response
1204-02	Time-out waiting for response [4]	1210-11	Modem time-out waiting for remote connection

NOTES:

[1] Local loopback mode
[2] Analog loopback originate mode
[3] Analog loopback answer mode
[4] Modem auto originate test
[5] Modem auto answer test
[6] Modem direct connect test

A.13 HARD DRIVE ERROR MESSAGES (17xx-xx)

Table A-12.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
17xx-01	Exceeded max. soft error limit	17xx-51	Failed I/O read test
17xx-02	Exceeded max. Hard error limit	17xx-52	Failed file I/O compare test
17xx-03	Previously exceeded max. soft error limit	17xx-53	Failed drive/head register test
17xx-04	Previously exceeded max.hard error limit	17xx-54	Failed digital input register test
17xx-05	Failed to reset controller	17xx-55	Cylinder 1 error
17xx-06	Fatal error while reading	17xx-56	Failed controller RAM diagnostics
17xx-07	Fatal error while writing	17xx-57	Failed controller-to-drive diagnostics
17xx-08	Failed compare of R/W buffers	17xx-58	Failed to write sector buffer
17xx-09	Failed to format a track	17xx-59	Failed to read sector buffer
17xx-10	Failed diskette sector wrap during read	17xx-60	Failed uncorrectable ECC error
17xx-19	Cntlr. failed to deallocate bad sectors	17xx-62	Failed correctable ECC error
17xx-40	Cylinder 0 error	17xx-63	Failed soft error rate
17xx-41	Drive not ready	17xx-65	Exceeded max. bad sectors per track
17xx-42	Failed to recalibrate drive	17xx-66	Failed to initialize drive parameter
17xx-43	Failed to format a bad track	17xx-67	Failed to write long
17xx-44	Failed controller diagnostics	17xx-68	Failed to read long
17xx-45	Failed to get drive parameters from ROM	17xx-69	Failed to read drive size
17xx-46	Invalid drive parameters from ROM	17xx-70	Failed translate mode
17xx-47	Failed to park heads	17xx-71	Failed non-translate mode
17xx-48	Failed to move hard drive table to RAM	17xx-72	Bad track limit exceeded
17xx-49	Failed to read media in file write test	17xx-73	Previously exceeded bad track limit
17xx-50	Failed I/O write test	--	--

1700-xx = Hard drive ID test
1701-xx = Hard drive format test
1702-xx = Hard drive read test
1703-xx = Hard drive read/write compare test
1704-xx = Hard drive random seek test
1705-xx = Hard drive controller test
1706-xx = Hard drive ready test
1707-xx = Hard drive recalibrate test
1708-xx = Hard drive format bad track test
1709-xx = Hard drive reset controller test
1710-xx = Hard drive park head test
1714-xx = Hard drive file write test
1715-xx = Hard drive head select test
1716-xx = Hard drive conditional format test
1717-xx = Hard drive ECC test
1719-xx = Hard drive power mode test
1721-xx = SCSI hard drive imminent failure
1724-xx = Net work preparation test
1736-xx = Drive monitoring test
1799-xx = Invalid hard drive type

A.14 HARD DRIVE ERROR MESSAGES (19xx-xx)

Table A-13.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
19xx-01	Drive not installed	19xx-21	Got servo pulses second time but not first
19xx-02	Cartridge not installed	19xx-22	Never got to EOT after servo check
19xx-03	Tape motion error	19xx-23	Change line unset
19xx-04	Drive busy erro	19xx-24	Write-protect error
19xx-05	Track seek error	19xx-25	Unable to erase cartridge
19xx-06	Tape write-protect error	19xx-26	Cannot identify drive
19xx-07	Tape already Servo Written	19xx-27	Drive not compatible with controller
19xx-08	Unable to Servo Write	19xx-28	Format gap error
19xx-09	Unable to format	19xx-30	Exception bit not set
19xx-10	Format mode error	19xx-31	Unexpected drive status
19xx-11	Drive recalibration error	19xx-32	Device fault
19xx-12	Tape not Servo Written	19xx-33	Illegal command
19xx-13	Tape not formatted	19xx-34	No data detected
19xx-14	Drive time-out error	19xx-35	Power-on reset occurred
19xx-15	Sensor error flag	19xx-36	Failed to set FLEX format mode
19xx-16	Block locate (block ID) error	19xx-37	Failed to reset FLEX format mode
19xx-17	Soft error limit exceeded	19xx-38	Data mismatch on directory track
19xx-18	Hard error limit exceeded	19xx-39	Data mismatch on track 0
19xx-19	Write (probably ID) error	19xx-40	Failed self-test
19xx-20	NEC fatal error	19xx-91	Power lost during test

1900-xx = Tape ID test failed
1901-xx = Tape servo write failed
1902-xx = Tape format failed
1903-xx = Tape drive sensor test failed
1904-xx = Tape BOT/EOT test failed
1905-xx = Tape read test failed
1906-xx = Tape R/W compare test failed
1907-xx = Tape write-protect failed

A.15 VIDEO (GRAPHICS) ERROR MESSAGES (24xx-xx)

Table A-14.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
2402-01	Video memory test failed	2418-02	EGA shadow RAM test failed
2403-01	Video attribute test failed	2419-01	EGA ROM checksum test failed
2404-01	Video character set test failed	2420-01	EGA attribute test failed
2405-01	80x25 mode, 9x14 cell test failed	2421-01	640x200 mode test failed
2406-01	80x25 mode, 8x8 cell test failed	2422-01	640x350 16-color set test failed
2407-01	40x25 mode test failed	2423-01	640x350 64-color set test failed
2408-01	320x200 mode color set 0 test failed	2424-01	EGA Mono. text mode test failed
2409-01	320x200 mode color set 1 test failed	2425-01	EGA Mono. graphics mode test failed
2410-01	640x200 mode test failed	2431-01	640x480 graphics mode test failed
2411-01	Screen memory page test failed	2432-01	320x200 256-color set test failed
2412-01	Gray scale test failed	2448-01	Advanced VGA controller test failed
2414-01	White screen test failed	2451-01	132-column AVGA test failed
2416-01	Noise pattern test failed	2456-01	AVGA 256-color test failed
2417-01	Lightpen text test failed, no response	2458-xx	AVGA BitBLT test failed
2417-02	Lightpen text test failed, invalid response	2468-xx	AVGA DAC test failed
2417-03	Lightpen graphics test failed, no resp.	2477-xx	AVGA data path test failed
2417-04	Lightpen graphics test failed, invalid resp.	2478-xx	AVGA BitBLT test failed
2418-01	EGA memory test failed	2480-xx	AVGA linedraw test failed

A.16 AUDIO ERROR MESSAGES (3206-xx)

Table A-15.
Audio Error Message

Message	Probable Cause
3206-xx	Audio subsystem internal error

A.17 NETWORK INTERFACE ERROR MESSAGES (60xx-xx)

Table A-16.
Network Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6000-xx	Pointing device interface error	6054-xx	Token ring configuration test failed
6014-xx	Ethernet configuration test failed	6056-xx	Token ring reset test failed
6016-xx	Ethernet reset test failed	6068-xx	Token ring int. loopback test failed
6028-xx	Ethernet int. loopback test failed	6069-xx	Token ring ext. loopback test failed
6029-xx	Ethernet ext. loopback test failed	6089-xx	Token ring open

A.18 SCSI INTERFACE ERROR MESSAGES (65xx-xx, 66xx-xx, 67xx-xx)

Table A-17.
SCSI Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6nyy-02	Drive not installed	6nyy-33	Illegal controller command
6nyy-03	Media not installed	6nyy-34	Invalid SCSI bus phase
6nyy-05	Seek failure	6nyy-35	Invalid SCSI bus phase
6nyy-06	Drive timed out	6nyy-36	Invalid SCSI bus phase
6nyy-07	Drive busy	6nyy-39	Error status from drive
6nyy-08	Drive already reserved	6nyy-40	Drive timed out
6nyy-09	Reserved	6nyy-41	SSI bus stayed busy
6nyy-10	Reserved	6nyy-42	ACK/REQ lines bad
6nyy-11	Media soft error	6nyy-43	ACK did not deassert
6nyy-12	Drive not ready	6nyy-44	Parity error
6nyy-13	Media error	6nyy-50	Data pins bad
6nyy-14	Drive hardware error	6nyy-51	Data line 7 bad
6nyy-15	Illegal drive command	6nyy-52	MSG, C/D, or I/O lines bad
6nyy-16	Media was changed	6nyy-53	BSY never went busy
6nyy-17	Tape write-protected	6nyy-54	BSY stayed busy
6nyy-18	No data detected	6nyy-60	Controller CONFIG-1 register fault
6nyy-21	Drive command aborted	6nyy-61	Controller CONFIG-2 register fault
6nyy-24	Media hard error	6nyy-65	Media not unloaded
6nyy-25	Reserved	6nyy-90	Fan failure
6nyy-30	Controller timed out	6nyy-91	Over temperature condition
6nyy-31	Unrecoverable error	6nyy-92	Side panel not installed
6nyy-32	Controller/drive not connected	6nyy-99	Autoloader reported tape not loaded properly

n = 5, Hard drive
= 6, CD-ROM drive
= 7, Tape drive.

yy = 00, ID
= 03, Power check
= 05, Read
= 06, SA/Media
= 08, Controller;
= 23, Random read
= 28, Media load/unload

A.19 POINTING DEVICE INTERFACE ERROR MESSAGES (8601-xx)

Table A-18.
Pointing Device Interface Error Messages

Message	Probable Cause	Message	Probable Cause
8601-01	Mouse ID fails	8601-06	Left block not selected
8601-02	Left mouse button is inoperative	8601-07	Right block not selected
8601-03	Left mouse button is stuck closed	8601-08	Timeout occurred
8601-04	Right mouse button is inoperative	8601-09	Mouse loopback test failed
8601-05	Right mouse button is stuck closed	8601-10	Pointing device is inoperative

A.20 CEMM PRIVILEDGED OPS ERROR MESSAGES

Table A-19.
CEMM Privileged Ops Error Messages

Message	Probable Cause	Message	Probable Cause
00	LGDT instruction	04	LL3 instruction
01	LIDT instruction	05	MOV CRx instruction
02	LMSW instruction	06	MOV DRx instruction
03	LL2 instruction	07	MOV TRx instruction

A.21 CEMM EXCEPTION ERROR MESSAGES

Table A-20.
CEMM Exception Error Messages

Message	Probable Cause	Message	Probable Cause
00	Divide	10	Invalid TSS
01	Debug	11	Segment not present
02	NMI or parity	12	Stack full
03	INT 0 (arithmetic overflow)	13	General protection fault
04	INT 3	14	Page fault
05	Array bounds check	16	Coprocessor
06	Invalid opcode	32	Attempt to write to protected area
07	Coprocessor device not available	33	Reserved
08	Double fault	34	Invalid software interrupt
09	Coprocessor segment overrun	--	--

Appendix B
ASCII CHARACTER SET

B.1 INTRODUCTION

This appendix lists, in Table B-1, the 256-character ASCII code set including the decimal and hexadecimal values. All ASCII symbols may be called while in DOS or using standard text-mode editors by using the combination keystroke of holding the **Alt** key and using the Numeric Keypad to enter the decimal value of the symbol. The extended ASCII characters (decimals 128-255) can only be called using the **Alt** + Numeric Keypad keys.

NOTE: Regarding keystrokes, refer to notes at the end of the table. Applications may interpret multiple keystroke accesses differently or ignore them completely.

Table B-1.
ASCII Character Set

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
0	00	Blank	32	20	Space	64	40	@	96	60	‘
1	01	☺	33	21	!	65	41	A	97	61	a
2	02	☻	34	22	“	66	42	B	98	62	b
3	03	♥	35	23	#	67	43	C	99	63	c
4	04	♦	36	24	$	68	44	D	100	64	d
5	05	♣	37	25	%	69	45	E	101	65	e
6	06	♠	38	26	&	70	46	F	102	66	f
7	07	•	39	27	‘	71	47	G	103	67	g
8	08	◘	40	28	(	72	48	H	104	68	h
9	09	○	41	29	)	73	49	I	105	69	I
10	0A	◙	42	2A	*	74	4A	J	106	6A	j
11	0B	♂	43	2B	+	75	4B	K	107	6B	k
12	0C	♀	44	2C	`	76	4C	L	108	6C	l
13	0D	♪	45	2D	-	77	4D	M	109	6D	m
14	0E	♫	46	2E	.	78	4E	N	110	6E	n
15	0F	☼	47	2F	/	79	4F	O	111	6F	o
16	10	►	48	30	0	80	50	P	112	70	p
17	11	◄	49	31	1	81	51	Q	113	71	q
18	12	↕	50	32	2	82	52	R	114	72	r
19	13	‼	51	33	3	83	53	S	115	73	s
20	14	¶	52	34	4	84	54	T	116	74	t
21	15	§	53	35	5	85	55	U	117	75	u
22	16	▬	54	36	6	86	56	V	118	76	v
23	17	↨	55	37	7	87	57	W	119	77	w
24	18	↑	56	38	8	88	58	X	120	78	x
25	19	↓	57	39	9	89	59	Y	121	79	y
26	1A	→	58	3A	:	90	5A	Z	122	7A	z
27	1B	←	59	3B	;	91	5B	[	123	7B	{
28	1C	∟	60	3C	<	92	5C	\	124	7C	|
29	1D	↔	61	3D	=	93	5D	]	125	7D	}
30	1E	▲	62	3E	>	94	5E	^	126	7E	~
31	1F	▼	63	3F	?	95	5F	_	127	7F	△ [1]

Continued

Table B-1. ASCII Code Set *(Continued)*

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
128	80	Ç	160	A0	á	192	C0	•	224	E0	•
129	81	ü	161	A1	í	193	C1	•	225	E1	ß
130	82	é	162	A2	ó	194	C2	•	226	E2	•
131	83	â	163	A3	ú	195	C3	•	227	E3	•
132	84	ä	164	A4	ñ	196	C4	•	228	E4	•
133	85	à	165	A5	Ñ	197	C5	•	229	E5	•
134	86	å	166	A6	ª	198	C6	•	230	E6	µ
135	87	ç	167	A7	º	199	C7	•	231	E7	•
136	88	ê	168	A8	¿	200	C8	•	232	E8	•
137	89	ë	169	A9	•	201	C9	•	233	E9	•
138	8A	è	170	AA	¬	202	CA	•	234	EA	•
139	8B	ï	171	AB	½	203	CB	•	235	EB	•
140	8C	î	172	AC	¼	204	CC	•	236	EC	•
141	8D	ì	173	AD	¡	205	CD	•	237	ED	•
142	8E	Ä	174	AE	«	206	CE	•	238	EE	•
143	8F	Å	175	AF	»	207	CF	•	239	EF	•
144	90	É	176	B0	•	208	D0	•	240	F0	•
145	91	æ	177	B1	•	209	D1	•	241	F1	±
146	92	Æ	178	B2	•	210	D2	•	242	F2	•
147	93	ô	179	B3	•	211	D3	•	243	F3	•
148	94	ö	180	B4	•	212	D4	•	244	F4	•
149	95	ò	181	B5	•	213	D5	•	245	F5	•
150	96	û	182	B6	•	214	D6	•	246	F6	÷
151	97	ù	183	B7	•	215	D7	•	247	F7	•
152	98	ÿ	184	B8	•	216	D8	•	248	F8	°
153	99	Ö	185	B9	•	217	D9	•	249	F9	·
154	9A	Ü	186	BA	•	218	DA	•	250	FA	·
155	9B	¢	187	BB	•	219	DB	•	251	FB	•
156	9C	£	188	BC	•	220	DC	•	252	FC	•
157	9D	¥	189	BD	•	221	DD	•	253	FD	²
158	9E	•	190	BE	•	222	DE	•	254	FE	•
159	9F	*f*	191	BF	•	223	DF	•	255	FF	Blank

NOTES:

[1] Symbol not displayed.

Keystroke Guide:

Dec #	Keystroke(s)
0	Ctrl 2
1-26	Ctrl A thru Z respectively
27	Ctrl [
28	Ctrl
29	Ctrl]
30	Ctrl 6
31	Ctrl -
32	Space Bar
33-43	Shift and key w/corresponding symbol
44-47	Key w/corresponding symbol
48-57	Key w/corresponding symbol, numerical keypad w/Num Lock active
58	Shift and key w/corresponding symbol
59	Key w/corresponding symbol
60	Shift and key w/corresponding symbol
61	Key w/corresponding symbol
62-64	Shift and key w/corresponding symbol
65-90	Shift and key w/corresponding symbol or key w/corresponding symbol and Caps Lock active
91-93	Key w/corresponding symbol
94, 95	Shift and key w/corresponding symbol
96	Key w/corresponding symbol
97-126	Key w/corresponding symbol or Shift and key w/corresponding symbol and Caps Lock active
127	Ctrl -
128-255	Alt and decimal digit(s) of desired character

Appendix C
KEYBOARD

C.1 INTRODUCTION

This appendix describes the Compaq keyboard that is included as standard with the system unit. The keyboard complies with the industry-standard classification of an “enhanced keyboard” and includes a separate cursor control key cluster, twelve “function” keys, and enhanced programmability for additional functions.

This appendix covers the following keyboard types (some of which may be available only as an option):

- The Windows-version keyboard includes three additional keys for specific support of the Windows operating system.
- The Erase-Ease keyboard features a split spacebar that can be user-programmed to provide easy access to the backspace function or set to operate as the normal spacebar.
- The scanner keyboard includes a built-in document scanner for scanning loose-leaf hardcopy.

> **NOTE:** This appendix discusses only the keyboard unit. The keyboard interface is a function of the system unit and is discussed in Chapter 5, Input/Output Interfaces.

Topics covered in this appendix include the following:

C.2 KEYSTROKE PROCESSING

A functional block diagram of the keystroke processing elements is shown in Figure C-1. Power (+5 VDC) is obtained from the system through the PS/2-type interface. The keyboard uses a Z86C14 (or equivalent) microprocessor. The Z86C14 scans the key matrix drivers every 10 ms for pressed keys while at the same time monitoring communications with the keyboard interface of the system unit. When a key is pressed, a Make code is generated. A Break code is generated when the key is released. The Make and Break codes are collectively referred to as scan codes. All keys generate Make and Break codes with the exception of the Pause key, which generates a Make code only.

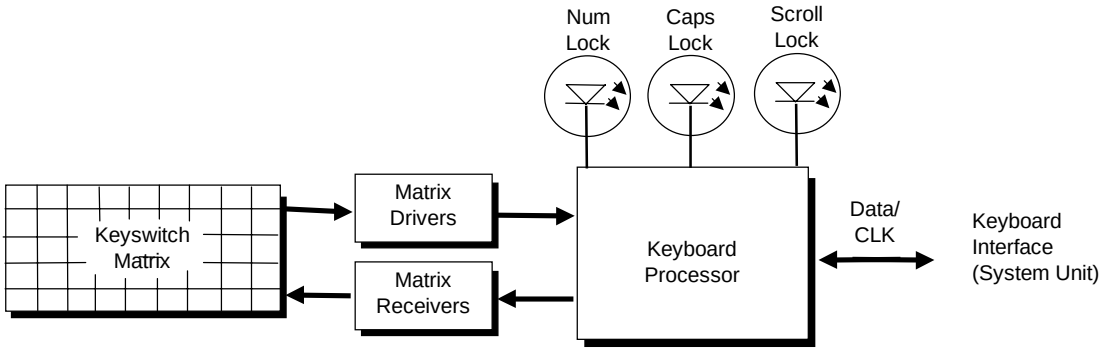


Figure C–1. Keystroke Processing Elements, Block Diagram

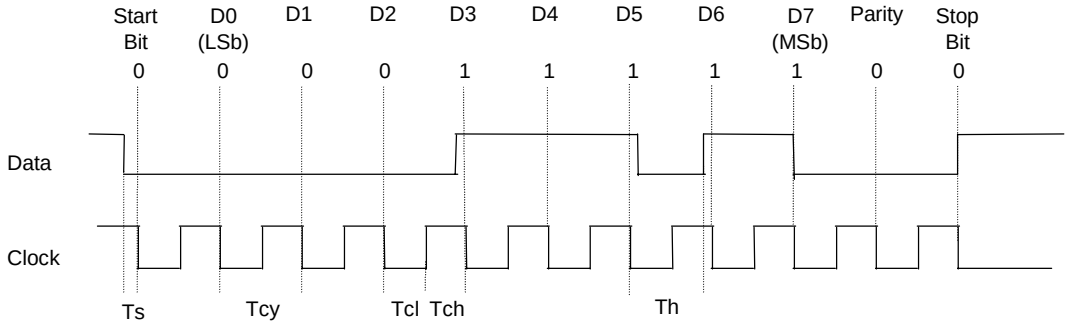
When the system is turned on, the keyboard processor generates a Power-On Reset (POR) signal after a period of 150 ms to 2 seconds. The keyboard undergoes a Basic Assurance Test (BAT) that checks for shorted keys and basic operation of the keyboard processor. The BAT takes from 300 to 500 ms to complete.

If the keyboard fails the BAT, an error code is sent to the CPU and the keyboard is disabled until an input command is received. After successful completion of the POR and BAT, a completion code (AAh) is sent to the CPU and the scanning process begins.

The keyboard processor includes a 16-byte FIFO buffer for holding scan codes until the system is ready to receive them. Response and typematic codes are not buffered. If the buffer is full (16 bytes held) a 17th byte of a successive scan code results in an overrun condition and the overrun code replaces the scan code byte and any additional scan code data (and the respective key strokes) are lost. Multi-byte sequences must fit entirely into the buffer before the respective keystroke can be registered.

C.2.1 TRANSMISSIONS TO THE SYSTEM

The keyboard processor sends two main types of data to the system; commands (or responses to system commands) and keystroke scan codes. Before the keyboard sends data to the system (specifically, to the 8042-type logic within the system), the keyboard verifies the clock and data lines to the system. If the clock signal is low (0), the keyboard recognizes the inhibited state and loads the data into a buffer. Once the inhibited state is removed, the data is sent to the system. Keyboard-to-system transfers consist of 11 bits as shown in Figure C-2.



Parameter	Minimum	Maximum
Tcy (Cycle Time)	60 us	80 us
Tcl (Clock Low)	30 us	35 us
Tch (clock High)	30 us	45 us
Th (Data Hold)	45 us	62 us
Ts (Data Setup)	8 us	14 us

Figure C–2. Keyboard-To-System Transmission of Code 58h, Timing Diagram

The system can halt keyboard transmission by setting the clock signal low. The keyboard checks the clock line every 60 us to verify the signal state. If a low is detected, the keyboard will finish the current transmission **if** the rising edge of the clock pulse for the parity bit has not occurred.

The enhanced keyboard has three operating modes:

- Mode 1 - PC-XT compatible
- Mode 2 - PC-AT compatible (default)
- Mode 3 - Select mode (keys are programmable as to make-only, break-only, typematic)

Modes can be selected by the user or set by the system. Mode 2 is the default mode. Each mode produces a different set of scan codes. When a key is pressed, the keyboard processor sends that key's make code to the 8042 logic of the system unit. The When the key is released, a release code is transmitted as well (except for the Pause key, which produces only a make code). The 8042-type logic of the system unit responds to scan code reception by asserting IRQ1, which is processed by the interrupt logic and serviced by the CPU with an interrupt service routine. The service routine takes the appropriate action based on which key was pressed.

C.2.2 KEYBOARD LAYOUTS

C.2.2.1 Standard Enhanced Keyboards

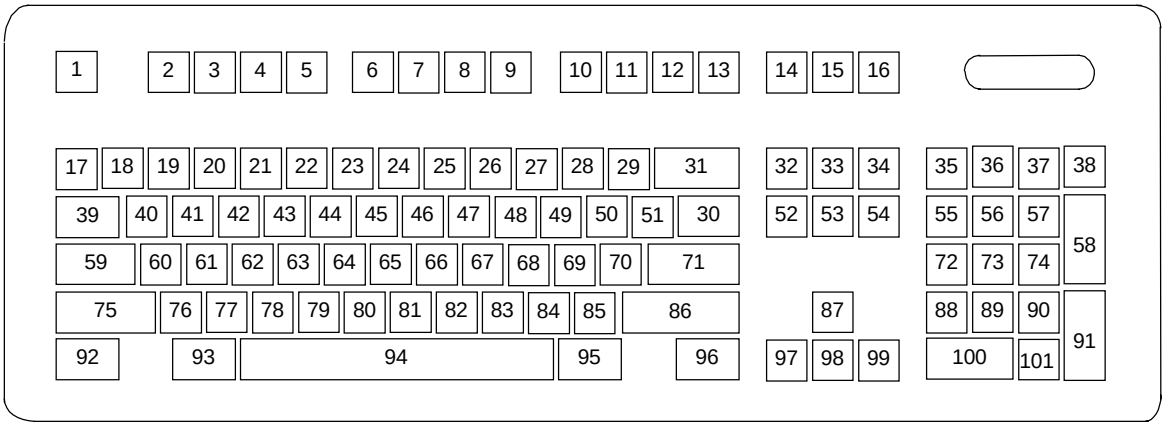


Figure C–3. U.S. English (101-Key) Keyboard Key Positions

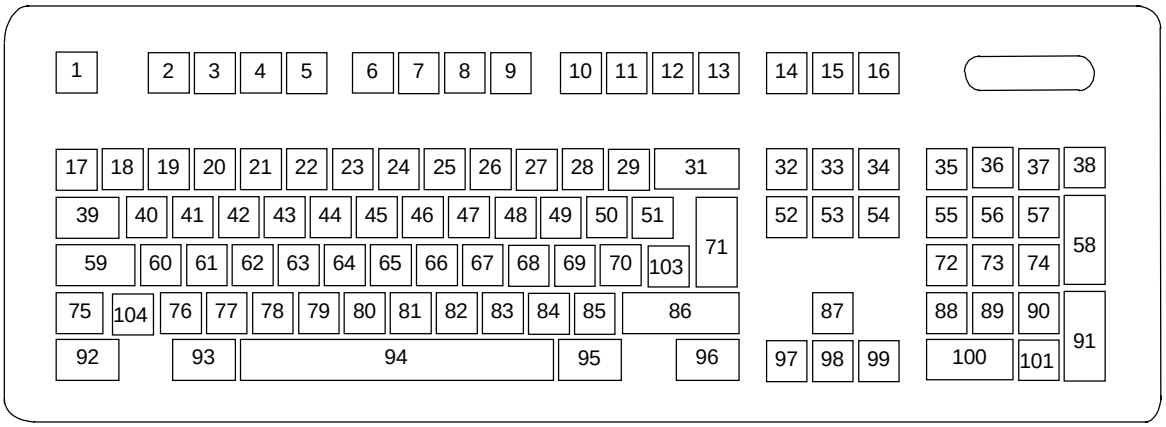


Figure C–4. National (102-Key) Keyboard Key Positions

C.2.2.2 Windows Enhanced Keyboards

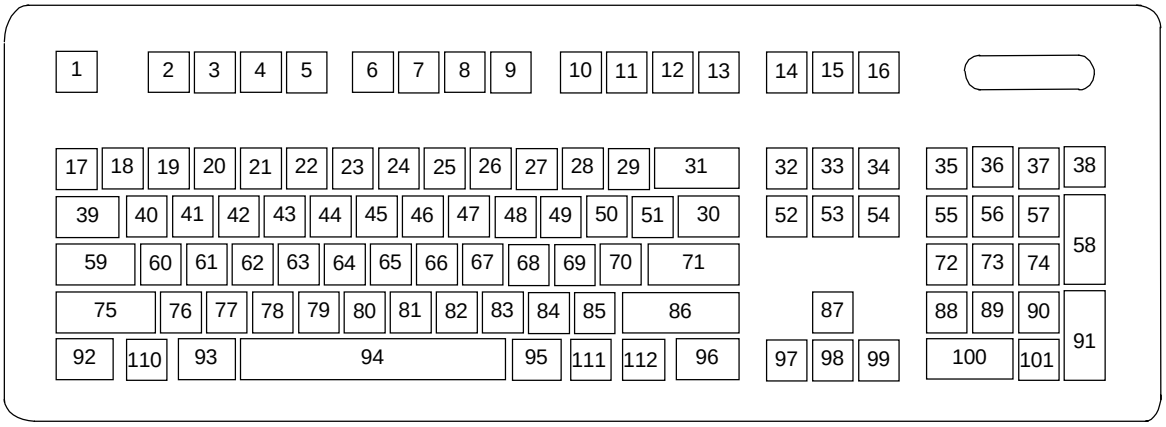


Figure C–5. U.S. English Windows (101W-Key) Keyboard Key Positions

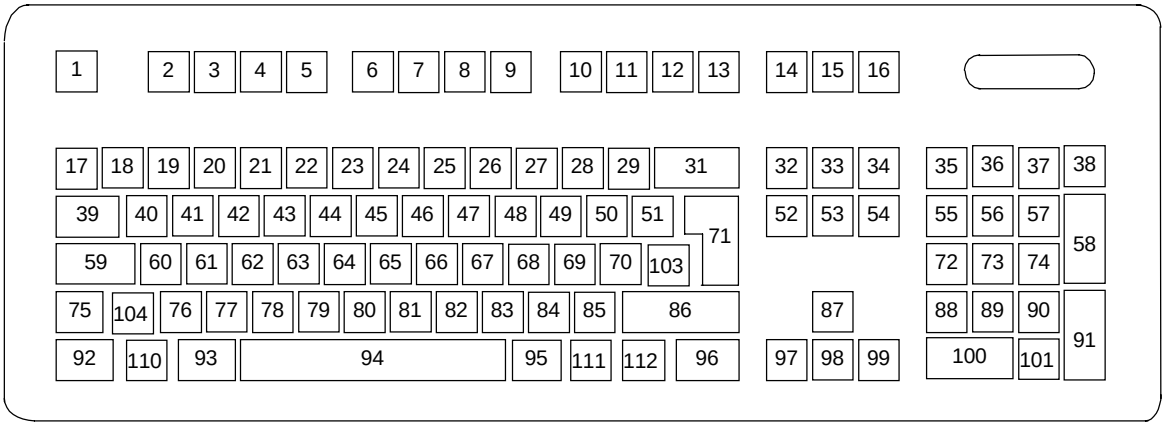


Figure C–6. National Windows (102W-Key) Keyboard Key Positions

C.2.2.3 Windows Enhanced Keyboards w/Erase-Ease

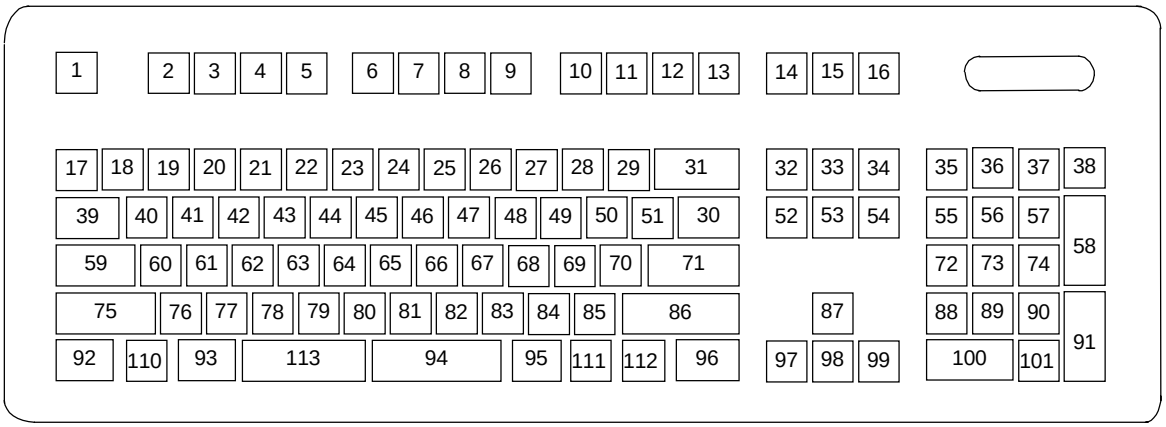


Figure C–7. U.S. English Windows (101WE-Key) Keyboard Key Positions

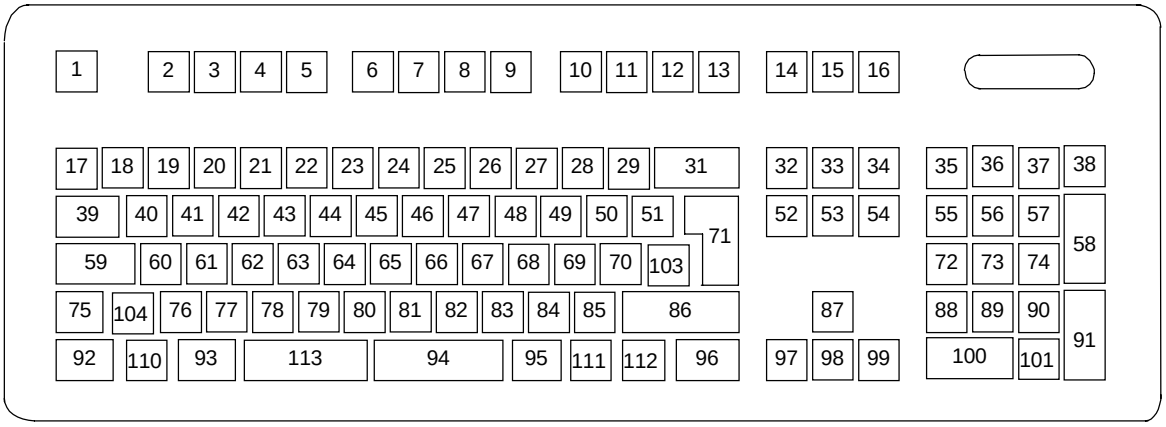


Figure C–8. National Windows (102WE-Key) Keyboard Key Positions

C.2.3 KEYS

All keys generate a make code (when pressed) and a break code (when released) with the exception of the **Pause** key (pos. 16), which produces a make code only. All keys, again, with the exception of the **Pause** key, are also typematic, although the typematic action of the **Shift**, **Ctrl**, **Alt**, **Num Lock**, **Scroll Lock**, **Caps Lock**, and **Ins** keys is suppressed by the BIOS. Typematic keys, when held down, send the make code repetitively at a predetermined rate until the key is released. If two keys are held down, the last key pressed will be typematic.

C.2.3.1 Special Single-Keystroke Functions

The following keys provide the intended function in most applications and environments.

Caps Lock - The **Caps Lock** key (pos. 59), when pressed and released, invokes a BIOS routine that turns on the caps lock LED and shifts into upper case key positions 40-49, 60-68, and 76-82. When pressed and released again, these keys revert to the lower case state and the LED is turned off. Use of the **Shift** key will reverse which state these keys are in based on the **Caps Lock** key.

Num Lock - The **Num Lock** key (pos. 32), when pressed and released, invokes a BIOS routine that turns on the num lock LED and shifts into upper case key positions 55-57, 72-74, 88-90, 100, and 101. When pressed and released again, these keys revert to the lower case state and the LED is turned off.

The following keys provide special functions that require specific support by the application.

Print Scrn - The **Print Scrn** (pos. 14) key can, when pressed, generate an interrupt that initiates a print routine. This function may be inhibited by the application.

Scroll Lock - The **Scroll Lock** key (pos. 15) when pressed and released, , invokes a BIOS routine that turns on the scroll lock LED and inhibits movement of the cursor. When pressed and released again, the LED is turned off and the function is removed. This keystroke is always serviced by the BIOS (as indicated by the LED) but may be inhibited or ignored by the application.

Pause - The **Pause** (pos. 16) key, when pressed, can be used to cause the keyboard interrupt to loop, i.e., wait for another key to be pressed. This can be used to momentarily suspend an operation. The key that is pressed to resume operation is discarded. This function may be ignored by the application.

The **Esc**, **Fn** (function), **Insert**, **Home**, **Page Up**/**Down**, **Delete**, and **End** keys operate at the discretion of the application software.

C.2.3.2 Multi-Keystroke Functions

Shift - The **Shift** key (pos. 75/86), when held down, produces a shift state (upper case) for keys in positions 17-29, 30, 39-51, 60-70, and 76-85 as long as the **Caps Lock** key (pos. 59) is toggled off. If the **Caps Lock** key is toggled on, then a held **Shift** key produces the lower (normal) case for the identified pressed keys. The **Shift** key also reverses the **Num Lock** state of key positions 55-57, 72, 74, 88-90, 100, and 101.

Ctrl - The **Ctrl** keys (pos. 92/96) can be used in conjunction with keys in positions 1-13, 16, 17-34, 39-54, 60-71, and 76-84. The application determines the actual function. Both **Ctrl** key positions provide identical functionality. The pressed combination of **Ctrl** and **Break** (pos. 16) results in the generation of BIOS function INT 1Bh. This software interrupt provides a method of exiting an application and generally halts execution of the current program.

Alt - The **Alt** keys (pos. 93/95) can be used in conjunction with the same keys available for use with the **Ctrl** keys with the exception that position 14 (**SysRq**) is available instead of position 16 (**Break**). The **Alt** key can also be used in conjunction with the numeric keypad keys (pos. 55-57, 72-74, and 88-90) to enter the decimal value of an ASCII character code from 1-255. The application determines the actual function of the keystrokes. Both **Alt** key positions provide identical functionality.

The combination keystroke of **Alt** and **SysRq** results in software interrupt 15h, AX=8500h being executed. It is up to the application to use or not use this BIOS function.

The **Ctrl** and **Alt** keys can be used together in conjunction with keys in positions 1-13, 17-34, 39-54, 60-71, and 76-84. The **Ctrl** and **Alt** key positions used and the sequence in which they are pressed make no difference as long as they are held down at the time the third key is pressed. The **Ctrl**, **Alt,** and **Delete** keystroke combination (required twice if in the Windows environment) initiates a system reset (warm boot) that is handled by the BIOS.

C.2.3.3 Windows Keystrokes

Windows-enhanced keyboards include three additional key positions. Key positions 110 and 111 (marked with the Windows logo) have the same functionality and are used by themselves or in combination with other keys to perform specific "hot-key" type functions for the Windows operating system. The defined functions of the Windows logo keys are listed as follows:

Keystroke	Function
Window Logo	Open Start menu
Window Logo + F1	Display pop-up menu for the selected object
Window Logo + TAB	Activate next task bar button
Window Logo + E	Explore my computer
Window Logo + F	Find document
Window Logo + CTRL + F	Find computer
Window Logo + M	Minimize all
Shift + Window Logo + M	Undo minimize all
Window Logo + R	Display Run dialog box
Window Logo + PAUSE	Perform system function
Window Logo + 1-0	Reserved for OEM use (see following text)

The combination keystroke of the Window Logo + 1-0 keys are reserved for OEM use for auxiliary functions (speaker volume, monitor brightness, password, etc.).

Key position 112 (marked with an application window icon) is used in combination with other keys for invoking Windows application functions.

C.2.3.4 Erase-Ease Keystrokes

The Erase-Ease keyboards feature a split space-bar key that operates as two separate keys (positions 113 and 94). The two keys can be configured for one of three modes:

Mode A:
(Power-on default)

113	94
Backspace	Spacebar

Mode B:

113	94
Spacebar	Backspace

Mode C:

113	94
Spacebar	Spacebar

To switch between modes the user holds down the left **ALT**, left **CTRL**, and left **Shift** keys while pressing the Erase-Ease (pos. 113) key once.

C.2.4 KEYBOARD COMMANDS

Table C-1 lists the commands that the keyboard can send to the system (specifically, to the 8042-type logic).

Table C-1.
Keyboard-to-System Commands

Command	Value	Description
Key Detection Error/Over/run	00h [1] FFh [2]	Indicates to the system that a switch closure couldn't be identified.
BAT Completion	AAh	Indicates to the system that the BAT has been successful.
BAT Failure	FCh	Indicates failure of the BAT by the keyboard.
Echo	EEh	Indicates that the Echo command was received by the keyboard.
Acknowledge (ACK)	FAh	Issued by the keyboard as a response to valid system inputs (except the Echo and Resend commands).
Resend	FEh	Issued by the keyboard following an invalid input.
Keyboard ID	83ABh	Upon receipt of the Read ID command from the system, the keyboard issues the ACK command followed by the two IDS bytes.

Note:
[1] Modes 2 and 3.
[2] Mode 1 only.

C.2.5 SCAN CODES

The scan codes generated by the keyboard processor are determined by the mode the keyboard is operating in.

- Mode 1: In Mode 1 operation, the keyboard generates scan codes compatible with 8088-/8086-based systems. To enter Mode 1, the scan code translation function of the keyboard controller must be disabled. Since translation is not performed, the scan codes generated in Mode 1 are identical to the codes required by BIOS. Mode 1 is initiated by sending command F0h with the 01h option byte. Applications can obtain system codes and status information by using BIOS function INT 16h with AH=00h, 01h, and 02h.

- Mode 2: Mode 2 is the default mode for keyboard operation. In this mode, the 8042 logic translates the make codes from the keyboard processor into the codes required by the BIOS. This mode was made necessary with the development of the Enhanced III keyboard, which includes additional functions over earlier standard keyboards. Applications should use BIOS function INT 16h, with AH=10h, 11h, and 12h for obtaining codes and status data. In Mode 2, the keyboard generates the Break code, a two-byte sequence that consists of a Make code immediately preceded by F0h (i.e., Break code for 0Eh is "F0h 0Eh").

- Mode 3: Mode 3 generates a different scan code set from Modes 1 and 2. Code translation must be disabled since translation for this mode cannot be done.

Table C-2.
Keyboard Scan Codes

Key Pos.	Legend	Make / Break Codes (Hex) Mode 1	Mode 2	Mode 3
1	Esc	01/81	76/F0 76	08/na
2	F1	3B/BB	05/F0 05	07/na
3	F2	3C/BC	06/F0 06	0F/na
4	F3	3D/BD	04/F0 04	17/na
5	F4	3E/BE	0C/F0 0C	1F/na
6	F5	3F/BF	03/F0 03	27/na
7	F6	40/C0	0B/F0 0B	2F/na
8	F7	41/C1	83/F0 83	37/na
9	F8	42/C2	0A/F0 0A	3F/na
10	F9	43/C3	01/FO 01	47/na
11	F10	44/C4	09/F0 09	4F/na
12	F11	57/D7	78/F0 78	56/na
13	F12	58/D8	07/F0 07	5E/na
14	Print Scrn	E0 2A E0 37/E0 B7 E0 AA E0 37/E0 B7 [1] [2] 54/84 [3]	E0 2A E0 7C/E0 F0 7C E0 F0 12 E0 7C/E0 F0 7C [1] [2] 84/F0 84 [3]	57/na
15	Scroll Lock	46/C6	7E/F0 7E	5F/na
16	Pause	E1 1D 45 E1 9D C5/na E0 46 E0 C6/na [3]	E1 14 77 E1 F0 14 F0 77/na E0 7E E0 F0 7E/na [3]	62/na
17	`	29/A9	0E/F0 E0	0E/F0 0E
18	1	02/82	16/F0 16	46/F0 46
19	2	03/83	1E/F0 1E	1E/F0 1E
20	3	04/84	26/F0 26	26/F0 26
21	4	05/85	25/F0 25	25/F0 25
22	5	06/86	2E/F0 2E	2E/F0 2E
23	6	07/87	36/F0 36	36/F0 36
24	7	08/88	3D/F0 3D	3D/F0 3D
25	8	09/89	3E/F0 3E	3E/F0 3E
26	9	0A/8A	46/F0 46	46/F0 46
27	0	0B/8B	45/F0 45	45/F0 45
28	-	0C/8C	4E/F0 4E	4E/F0 4E
29	=	0D/8D	55/F0 55	55/F0 55
30	\	2B/AB	5D/F0 5D	5C/F0 5C
31	Backspace	0E/8E	66/F0 66	66/F0 66
32	Insert	E0 52/E0 D2 E0 AA E0 52/E0 D2 E0 2A [4] E0 2A E0 52/E0 D2 E0 AA [6]	E0 70/E0 F0 70 E0 F0 12 E0 70/E0 F0 70 E0 12 [5] E0 12 E0 70/E0 F0 70 E0 F0 12 [6]	67/na
33	Home	E0 47/E0 C7 E0 AA E0 52/E0 C7 E0 2A [4] E0 2A E0 47/E0 C7 E0 AA [6]	E0 6C/E0 F0 6C E0 F0 12 E0 6C/E0 F0 6C E0 12 [5] E0 12 E0 6C/E0 F0 6C E0 F0 12 [6]	6E/na
34	Page Up	E0 49/E0 C9 E0 AA E0 49/E0 C9 E0 2A [4] E0 2A E0 49/E0 C9 E0 AA [6]	E0 7D/E0 F0 7D E0 F0 12 E0 7D/E0 F0 7D E0 12 [5] E0 12 E0 7D/E0 F0 7D E0 F0 12 [6]	6F/na
35	Num Lock	45/C5	77/F0 77	76/na
36	/	E0 35/E0 B5 E0 AA E0 35/E0 B5 E0 2A [1]	E0 4A/E0 F0 4A E0 F0 12 E0 4A/E0 F0 4A E0 12 [1]	77/na
37	*	37/B7	7C/F0 7C	7E/na
38	-	4A/CA	7B/F0 7B	84/na
39	Tab	0F/8F	0D/F0 0D	0D/na
40	Q	10/90	15/F0 15	15/na

Continued

([x] Notes listed at end of table.)

Table C-2. Keyboard Scan Codes *(Continued)*

Key Pos	Legend	Make / Break Codes (Hex) Mode 1	Mode 2	Mode 3
41	W	11/91	1D/F0 1D	1D/F0 1D
42	E	12/92	24/F0 24	24/F0 24
43	R	13/93	2D/F0 2D	2D/F0 2D
44	T	14/94	2C/F0 2C	2C/F0 2C
45	Y	15/95	35/F0 35	35/F0 35
46	U	16/96	3C/F0 3C	3C/F0 3C
47	I	17/97	43/F0 43	43/F0 43
48	O	18/98	44/F0 44	44/F0 44
49	P	19/99	4D/F0 4D	4D/F0 4D
50	[	1A/9A	54/F0 54	54/F0 54
51	]	1B/9B	5B/F0 5B	5B/F0 5B
52	Delete	E0 53/E0 D3 E0 AA E0 53/E0 D3 E0 2A [4] E0 2A E0 53/E0 D3 E0 AA [6]	E0 71/E0 F0 71 E0 F0 12 E0 71/E0 F0 71 E0 12 [5] E0 12 E0 71/E0 F0 71 E0 F0 12 [6]	64/F0 64
53	End	E0 4F/E0 CF E0 AA E0 4F/E0 CF E0 2A [4] E0 2A E0 4F/E0 CF E0 AA [6]	E0 69/E0 F0 69 E0 F0 12 E0 69/E0 F0 69 E0 12 [5] E0 12 E0 69/E0 F0 69 E0 F0 12 [6]	65/F0 65
54	Page Down	E0 51/E0 D1 E0 AA E0 51/E0 D1 E0 2A [4] E0 @a E0 51/E0 D1 E0 AA [6]	E0 7A/E0 F0 7A E0 F0 12 E0 7A/E0 F0 7A E0 12 [5] E0 12 E0 7A/E0 F0 7A E0 F0 12 [6]	6D/F0 6D
55	7	47/C7 [6]	6C/F0 6C [6]	6C/na [6]
56	8	48/C8 [6]	75/F0 75 [6]	75/na [6]
57	9	49/C9 [6]	7D/F0 7D [6]	7D/na [6]
58	+	4E/CE [6]	79/F0 79 [6]	7C/F0 7C
59	Caps Lock	3A/BA	58/F0 58	14/F0 14
60	A	1E/9E	1C/F0 1C	1C/F0 1C
61	S	1F/9F	1B/F0 1B	1B/F0 1B
62	D	20/A0	23/F0 23	23/F0 23
63	F	21/A1	2B/F0 2B	2B/F0 2B
64	G	22/A2	34/F0 34	34/F0 34
65	H	23/A3	33/F0 33	33/F0 33
66	J	24/A4	3B/F0 3B	3B/F0 3B
67	K	25/A5	42/F0 42	42/F0 42
68	L	26/A6	4B/F0 4B	4B/F0 4B
69	;	27/A7	4C/F0 4C	4C/F0 4C
70	‘	28/A8	52/F0 52	52/F0 52
71	Enter	1C/9C	5A/F0 5A	5A/F0 5A
72	4	4B/CB [6]	6B/F0 6B [6]	6B/na [6]
73	5	4C/CC [6]	73/F0 73 [6]	73/na [6]
74	6	4D/CD [6]	74/F0 74 [6]	74/na [6]
75	Shift (left)	2A/AA	12/F0 12	12/F0 12
76	Z	2C/AC	1A/F0 1A	1A/F0 1A
77	X	2D/AD	22/F0 22	22/F0 22
78	C	2E/AE	21/F0 21	21/F0 21
79	V	2F/AF	2A/F0 2A	2A/F0 2A
80	B	30/B0	32/F0 32	32/F0 32

Continued

([x] Notes listed at end of table.)

Table C-2. Keyboard Scan Codes *(Continued)*

Key Pos.	Legend	Make / Break Codes (Hex) Mode 1	Mode 2	Mode 3
81	N	31/B1	31/F0 31	31/F0 31
82	M	32/B2	3A/F0 3A	3A/F0 3A
83	,	33/B3	41/F0 41	41/F0 41
84	.	34/B4	49/F0 49	49/F0 49
85	/	35/B5	4A/F0 4A	4A/F0 4A
86	Shift (right)	36/B6	59/F0 59	59/F0 59
87	↑	E0 48/E0 C8 E0 AA E0 48/E0 C8 E0 2A [4] E0 2A E0 48/E0 C8 E0 AA [6]	E0 75/E0 F0 75 E0 F0 12 E0 75/E0 F0 75 E0 12 [5] E0 12 E0 75/E0 F0 75 E0 F0 12 [6]	63/F0 63
88	1	4F/CF [6]	69/F0 69 [6]	69/na [6]
89	2	50/D0 [6]	72/F0 72 [6]	72/na [6]
90	3	51/D1 [6]	7A/F0 7A [6]	7A/na [6]
91	Enter	E0 1C/E0 9C	E0 5A/F0 E0 5A	79/F0 79[6]
92	Ctrl (left)	1D/9D	14/F0 14	11/F0 11
93	Alt (left)	38/B8	11/F0 11	19/F0 19
94	(Space)	39/B9	29/F0 29	29/F0 29
95	Alt (right)	E0 38/E0 B8	E0 11/F0 E0 11	39/na
96	Ctrl (right)	E0 1D/E0 9D	E0 14/F0 E0 14	58/na
97	←	E0 4B/E0 CB E0 AA E0 4B/E0 CB E0 2A [4] E0 2A E0 4B/E0 CB E0 AA [6]	E0 6B/Eo F0 6B E0 F0 12 E0 6B/E0 F0 6B E0 12[5] E0 12 E0 6B/E0 F0 6B E0 F0 12[6]	61/F0 61
98	↓	E0 50/E0 D0 E0 AA E0 50/E0 D0 E0 2A [4] E0 2A E0 50/E0 D0 E0 AA [6]	E0 72/E0 F0 72 E0 F0 12 E0 72/E0 F0 72 E0 12[5] E0 12 E0 72/E0 F0 72 E0 F0 12[6]	60/F0 60
99	→	E0 4D/E0 CD E0 AA E0 4D/E0 CD E0 2A [4] E0 2A E0 4D/E0 CD E0 AA [6]	E0 74/E0 F0 74 E0 F0 12 E0 74/E0 F0 74 E0 12[5] E0 12 E0 74/E0 F0 74 E0 F0 12[6]	6A/F0 6A
100	0	52/D2 [6]	70/F0 70 [6]	70/na [6]
101	.	53/D3 [6]	71/F0 71 [6]	71/na [6]
102	na	7E/FE	6D/F0 6D	7B/F0 7B
103	na	2B/AB	5D/F0 5D	53/F0 53
104	na	36/D6	61/F0 61	13/F0 13
110	(Win95) [7]	E0 5B/E0 DB E0 AA E0 5B/E0 DB E0 2A [4] E0 2A E0 5B/E0 DB E0 AA [6]	E0 1F/E0 F0 1F E0 F0 12 E0 1F/E0 F0 1F E0 12 [5] E0 12 E0 1F/E0 F0 1F E0 F0 12 [6]	8B/F0 8B
111	(Win95) [7]	E0 5C/E0 DC E0 AA E0 5C/E0 DC E0 2A [4] E0 2A E0 5C/E0 DC E0 AA [6]	E0 2F/E0 F0 27 E0 F0 12 E0 27/E0 F0 27 E0 12 [5] E0 12 E0 27/E0 F0 27 E0 F0 12 [6]	8C/F0 8C
112	(Win Apps) [7]	E0 5D/E0 DD E0 AA E0 5D/E0 DD E0 2A [4] E0 2A E0 5D E0 DD E0 AA [6]	E0 2F/E0 F0 2F E0 F0 12 E0 2F/E0 F0 2F E0 12 [5] E0 12 E0 2F/E0 F0 2F E0 F0 12 [6	8D/F0 8D
113	(Erase-Ease) [8]	0E/8E	66/F0 66	66/na

NOTES:

All codes assume Shift, Ctrl, and Alt keys inactive unless otherwise noted.
NA = Not applicable
[1] Shift (left) key active.
[2] Ctrl key active.
[3] Alt key active.
[4] Left Shift key active. For active right Shift key, substitute AA/2A make/break codes for B6/36 codes.
[5] Left Shift key active. For active right Shift key, substitute F0 12/12 make/break codes for F0 59/59 codes.
[6] Num Lock key active.
[7] Windows keyboards only
[8] Erase-Ease keyboards only

C.3 SCANNER DESCRIPTION

The scanner keyboard, available as an option, integrates a scanner with a SpaceSaver Windows ’95 keyboard, providing the ability to scan hardcopy looseleaf documents for faxing or electronic storage. The scanner provides resolutions up to 400 dpi and 256 shades of gray and outputs through a standard serial interface to the system unit. Using optical character recognition (OCR) support software, printed textual data can be converted into editable files.

Operation of the scanner starts automatically when a sheet is inserted into the Contact Image Sensor (CIS). A button on the left side of the keyboard allows then operator to open a menu, halt scanning in progress, or invoke a serial port test. Figure C-9 shows a block diagram of the key scanner elements.

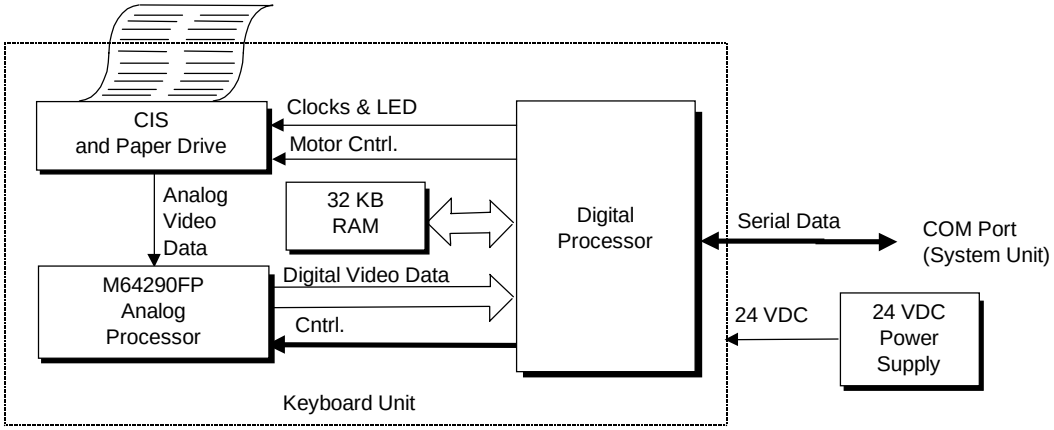


Figure C–9. Scanner Elements, Block Diagram

The Contact Image Sensor (CIS) and paper drive unit handles the hardcopy input. As each sheet is placed into the input slot, the sheet activates the mechanism and is drawn through and scanned by an LED illumination/photodiode sensor array. The drive motor provides 96 steps per revolution (3.75 degress per step) and is geared for 0.005 inch document movement per step for a resolution of 200 dpi. Half-stepping provides 400 dpi vertical resolution.

An analog video data stream is developed and routed to the Digital-to-Analog (D/A) Processor for conversion to digital video data that is routed to the Digital Processor. The Digital Processor provides most of the control of the scanner operation. A 32-KB RAM provides storage of executable code, pixel-to-pixel correction values, image processing line/diffusion data, and transmission data buffering.

The scanner elements are powered from an external 24 VDC power supply. Internal components use +5, +9, and -12 VDC.

C.3.1 SCANNER OPERATION

The scanner requires minimum user interface for normal operation. Insertion of a sheet of hardcopy activates the scanner. Operating parameters such as resolution, brightness, and motor speed are programmable for optimum performance. Other characteristics such as gamma correction, modulation transfer function (MTF), image compression, and pixel normalization are optimized through the use of pre-computed tables that are downloaded for image correction and adjustments when necessary.

The user interface is provided through a button located to the left of the sheet insertion tray. This normally-open switch provides the following functions depending on when pressed:

When Pressed	Function
During Power-Up	Scanner enters communications loopback mode. Mode remains in effect until the next power cycle (cold boot).
Scanner at idle	Actives a menu for changing/viewing parameters.
During a scan	Aborts the scan and reverses the motor, backing the document out of the scanner.

An inserted document activates one or more of five sensing fingers mounted on a shaft. The shaft begins rotation, turning an opaque flag that breaks an opto-interrupter beam between an LED and a phototransistor. The paper sensor signal goes active high, initiating the Digital Processor to begin the scanning process.

An LED/phototransistor assembly similar to the paper sensor is used for skew control. Sensing fingers on each side of the paper path check for misalignment (skew) of the document as it is pulled through the scan area. If the document comes in contact with one of the sensor fingers, an opaque flag is engaged to rotate, blocking an opto-interrupter beam and initiating an abort sequence. The skew LEDs , along with the LEDs used for scanning, are only powered up during the scan operation (i.e., while a document is in the scanner).

A flow chart of the scanning operation is shown in Figure C-10. Photo-Response Non-Uniformity (PRNU) refers to the fact that not every photosensor in the CIS has the same sensitivity. The PRNU correction stage adjusts for each photosensor's sensistivity level by applying a unique offset and gain value for it. A calibration procedure (initially done at the factory) is used to determine the compensation values for the photo array of the CIS. This data is stored in the CALIBRAT.DAT file on the installation disk and copied to the system unit's hard drive. The data is downloaded to the scanner after power up.

The modulation transfer function (MTF) of the optical system and document motion is corrected by downloading the MTF compensation parameters from the system unit to improve the quality of the scanned image.

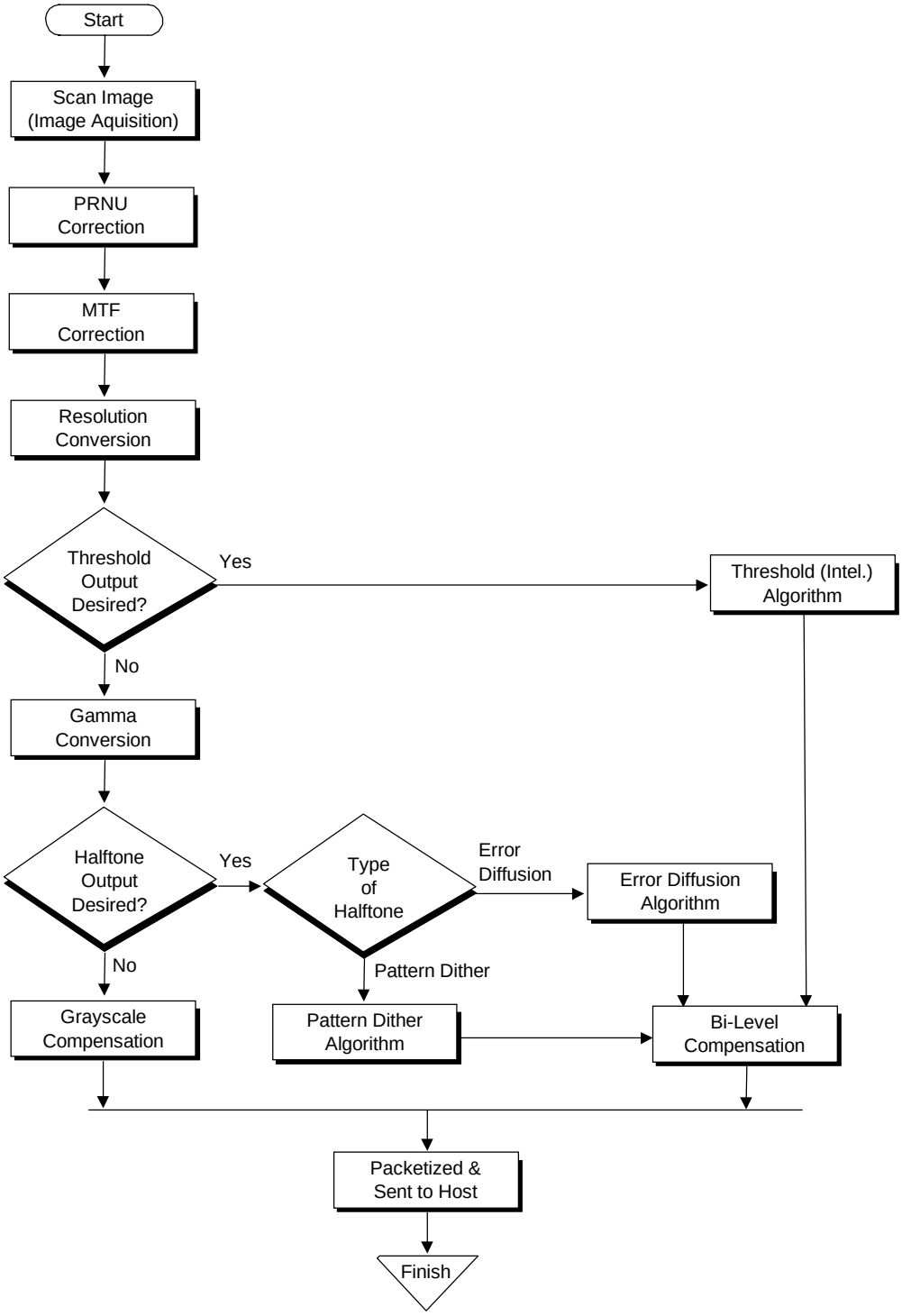


Figure C–10. Scanner operation Flow Chart

C.3.1.1 Resolution/Shade Depth

The drive motor mechanism of the CIS supports a vertical resolution of 400 dpi. The CIS provides a maximum horizontal resolution of 200 dpi. These factors provide true spatial resolutions of 100 and 200 dpi. Using horizontal interpolation, pseudo 300 and 400 dpi spatial resolutions are possible. Shade depth is determined by the number of bits used to control each pixel. The bits per pixel (bpp) parameter can be set to one (for black and white), two, four, or eight (for 256 shades of gray).

The selected resolution/shade depth determines the scanning time of a given sheet. Table C-3 lists the approximate scanning times for a standard 11 inch sheet using specified resolution/shade depths based on the line integration time of 2.5 ms.

Table C-3.
Scanner Performance Chart

		Scan Time for 11" Page		
X / Y	**DPI**	**1 bpp**	**4 bpp**	**8 bpp**
100 / 100	100	7 sec	11 sec	14 sec
200 / 200	200	7 sec	27 sec	36 sec
200 / 300	300 (Pseudo)	12 sec	60 sec	60 sec
200 / 400	400 (Pseudo)	17 sec	62 sec	80 sec

NOTE:
Scan times measured on a Pentium/90-based system with 16 MB RAM.

C.3.1.2 Image Quality

Brightness is fully programmable and independently adjustable using either normal or intelligent methods. The normal method slices each gray scale pixel into either black or white depending on the threshold value selected. The intelligent method automatically adjusts the pixel to the background for the best detail.

The grayscale transfer function can be tailored by gamma correction values that are downloaded from the system. This function can be disabled if desired.

Compensation for the Modulation Transfer Function (MTF) of the optical system and document motion is provided for improving image quality. The MTF parameters are /downloaded from the host if (if enabled).

Image compression is provided through a table-driven compressor. Compression values are loadable from the host and used by one of two types of algorithms: Huffman DPCM for 2- to 8-bit grayscale images, and a proprietary 1-bit compression.

C.3.2 SCANNER INTERFACE

The scanner communicates with the system unit (host) using a serial port as the primary choice of connection. The scanner interface is adaptable to several types of host connections as shown in Table C-4 (unshaded portion describes standard scanner interface with Compaq system unit).

Table C-4.
Scanner I/F Signals

Scanner Signals		Serial Port (PC)			Parallel Port		Serial Port (MacIntosh)	
Pnyb Mode	Mser Mode	RS232 Signal	DB9 Pin	DB25 Pin	Signal	DB25 Pin	Signal	DIN8 Pin
P0	SCLK	CTS	8	5	Select	13	HSKIn	2
P1		DSR	6	6	Paper Out	12	--	--
P2		RI	9	22	Ack	10	--	--
P3		DCD	1	8	Busy	11	--	--
PCLK	DTR	DTR	4	20	Strobe	1	HSKOut	1
SOUT	TXD	RTS	7	4	Init	16	TXD	6
GND	--	GND	5	7	GND	18	GND/RXD+	4/8
PnP	RXD	--	2	3	--	--	RXD-	5

Optional interface configuration.

The scanner uses one of two communication modes; Pnyb and Mser. The scanner selects the mode based on the idle status of the DTR/PCLK signal. If detected in a low state, the scanner uses the Pnyb mode. If PCLK is detected in a high state at idle, then the Mser mode is used.

Switching between the Pnyb and Mser modes is automatic and transparent to the operating system and application. This allows the scanner to be configured through an A/B box to two systems using different interfaces. The system unit (host) must drive the DTR signal at the appropriate level for at least 20 us before transmitting data packets.

A packet consists of an exchange of one or more bytes between the scanner and the host. A session is an exchange of packets between the scanner and the host. A session begins with a single-byte packet called a wakeup code and ends with the transfer of an acknowledgment (ACK) of the last packet received. Either the scanner or the host can initiate a session, and a session can be ended or cancelled by the scanner or the host, regardless of which initiated the session. A session is restricted to the action specified in the wakeup code.

C.3.2.1 Pnyb Mode

In the parallel nibble or "Pnyb" mode, the scanner transfers scanned information to the system unit (host) four bits (a nibble) at a time using the P3..P0 signals, which conform to RS-232 voltage and timing specifications. The P3..P0 signals are mapped to bits <7..4> respectively of the Modem Status Register (primary address 3FEh). The nibbles are clocked into the host with each transition of the PCLK signal. PCLK transitions from low to high clock in a high nibble, which transitions from high to low clock in a low nibble. The host can assume a nibble from the scanner is ready to be read 3.3 us after the PCLK transition requesting it. At the end of a scanner-to-host packet transfer, the host toggles the PCLK signal an extra time (0-to-1-to-0). This extra toggle indicates to the scanner that the last nibble has been read and sets the P3..P0 lines signals to a waiting state.

Data from the system unit (host) is transferred serially (bit-by-bit) as the SO signal along with the PCLK signal. A data bit is clocked with each transition of the PCLK signal so that a byte is transferred with four PCLK cycles. These signals also conform to RS-232 voltage and timing specifications and are mapped at bits <1,0> of the Modem Control Register (primary address 3FCh). The scanner can read data as long as the setup time is at least 1 us and the hold time is at least 3.3 us. The host must allow an additional 50 us after sending the LSb of each of the first five bytes of a multi-byte packet to the scanner. During host-to-scanner transfers, the scanner uses the P3..P0 lines for indicating transmission status to the host.

In the Pnyb mode, the host must insure that the high state of the first PCLK cycle of a session completes in less than 10 us so that the scanner does not interpret a Mser mode transfer.

C.3.2.2 Mser Mode (MacIntosh Connection Only)

The MacIntosh Serial or "Mser" mode uses bit-serial transfers for both scanner-to-host (RXD signal) as well as host-to-scanner (TXD signal) transfers. Transfers are accomplished using 10-bit frames that consist of a start bit, a data byte (LSb first), and a stop bit. The clock (SCLK) signal is provided by the scanner. The Mser mode is similar to isochronous transmission.

C.3.3 SCANNER SPECIFICATIONS/REQUIREMENTS

Table C-5.
Scanner Specifications

Parameter	Specification [1]
Dimensions (Complete keyboard unit):	
Width	20.5 in (52.07 cm)
Height	2.5 in (6.35 cm)
Depth	9 in (22.86 cm)
Weight (Complete keyvoard unit)	10.1 lb (4.58 kg)
Scanner Paper Sizes:	
Minimum	2.0 x 3.0 in (5.1 x 7.6 cm)
Maximum	8.5 x 30 in 21.6 x 76.2 cm)
Maximum Scanned Resolution (input)	2400 x 2400 dpi
Maximum Scanning Resolution (output)	400 dpi
Maximum Scan Time (8.5 x 11" sheet)	6 seconds [2]
Power Requirements (Scanner only):	
Input Voltage	24 VDC
Maximum Current Drain (scanning)	990 ma
Environmental Conditions:	
Tempurature, operating	50°-104° F (10°-40° C)
Tempurature, non-operating	-4°-140° F (-20°-60° C)
Humidity, operating	20-80% RH
Humidity, non-operating	5-95% RH

NOTE:
[1] Metric numbers shown in parenthesis.
[2] Based on Pentium/90-based system w/16 MB RAM

The scanner imposes the following requirements on the host system:

- 486 or better microprocessor
- Serial port
- Windows 3.1, Windows for Workgroups 3.11, or Windows 95 or later
- 4 megabytes of RAM (8 megabytes recommended)
- 50 megabytes free disk space

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