Enterprise Server Group

Intel® Astor II Server Chassis
Technical Product Specification

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Revision History

Revision	Revision History	Date
Rev 0.9	Initial release of the Intel Astor II Server Chassis Technical Product Specification	12/98
Rev 1.0	Release of the Intel Astor II Server Chassis Technical Product Specification	3/1999

Reference Documents

- *L440GX+ Technical Product Specification (TPS) Rev 1.0*
- *Intelligent Management Bus (IMB) Specification, Version 1.1,* February 1, 1997.
- *SCSI Accessed Fault-Tolerant Enclosures Interface Specification*, © Conner Peripherals and Intel Corporation, Revision 1.00, October 17, 1995
- *SCSI Parallel Interface-2*, draft proposal revision 20a
- *Single Connector Attachment for Small SCSI Disk Drives.* Small Form Factor Committee, revision 3.2
- *Symbios* SYM53C80E/S SCSI Protocol Controller Data Sheet,* Version 1.0, 12/96.
- *AIC-3860 Single-ended-to-Low Voltage Differential SCSI Transceiver Data Sheet,* Rev. A, 12/97.
- *The I^2C Bus and How to Use It,* January 1992, © 1992 Philips Semiconductors

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1 INTRODUCTION

This specification details the feature set of the Astor II server chassis, an entry-level server chassis offering designed for the Intel® L440GX+ and N440BX Server boards. The Astor II chassis has user friendly features, is readily accessible and serviceable, and is flexible for use with multiple platforms and multiple configurations.

The Intel® Astor II server chassis retains the dimensions of the original Intel Astor chassis: approximately 19" high, 18" deep, and 8" wide, however, the Astor II design provides a LVD (Low Voltage Differential) SCSI backplane in the hot-swap hard drive peripheral bay. The hot-swap bay supports up to five 1" SCA2 hot-swap SCSI hard drives to enhance serviceability, availability, and upgradability of the chassis. An additional new feature of the Astor II server chassis is an internal IDE drive bay capable of supporting up to two IDE "boot" drives for operating system mirroring.

The chassis is designed to use PS/2* form factor power supplies rated up to 300 watts. Fans of various sizes (80 or 92mm) may be used as required by specific configurations.

1.1 Chassis Color

The primary exterior chassis color will match Intel Color Standard 513505.

1.2 Front Bezel Features

The standard front bezel is molded plastic with two removable 5.25" peripheral bay covers. Behind each peripheral bay cover a removable EMI (Electromagnetic Interference) shield is installed.

Opening an exterior plastic door, followed by a lockable metal EMI door easily accesses hot-swap hard drives. This adds flexibility to the bezel design by making EMI performance independent of the cosmetic plastic parts.

1.3 Security

At the chassis level a variety of security options are provided.

- A Padlock loop on the rear of the chassis side cover can be used to prevent access to the microprocessors, memory, and add-in cards. A variety of lock sizes can be accommodated by the .300 diameter loop.
- A Padlock loop on the hard drive bay EMI door provides security for the hot swap hard drives. The allotted space accommodates a MasterLock* model 120-D or equivalent lock. Dimensions: .815" H x .830" W x .430" D. Pall diameter .145"
- An alarm switch is provided for the chassis side cover that may be connected directly to the front panel, where server management software, such as Intel Server Control can process alarm switch activity as desired.
- The front bezel assembly is designed so as not be removable with the side access cover in place, preventing extraction of the 5.25" peripherals.
- Additionally, a number of security features can be configured in the server board's BIOS set-up. For example, the front panel power and reset switches, as well as the floppy disk can all be disabled. Refer to the appropriate server board Product Guide or Technical Product Specification (TPS) for a detailed description of Software and BIOS security features.

1.4 I/O panel

All input/output connectors are accessible on the rear of the chassis and an ATX 2.02 compatible cutout is provided for I/O shield installation. A metal I/O shield is required for installation in the cutout in order to maintain Electromagnetic Compatibility. The appropriate I/O shield for either the N440BX or the L440GX+ server board is provided with the boxed server board. The I/O cutout dimensions are shown in Figure 1 below for reference.

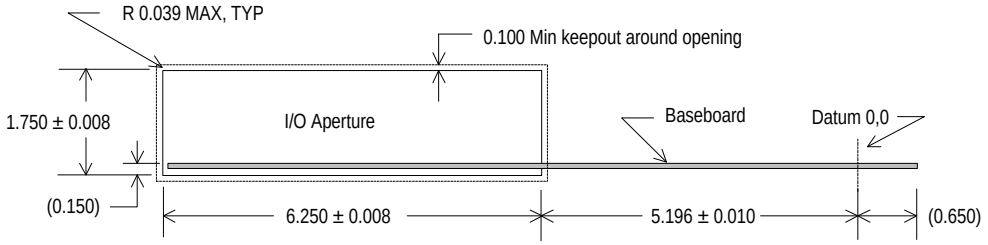

Figure 1: ATX 2.02 I/O Aperture

1.5 Chassis Views

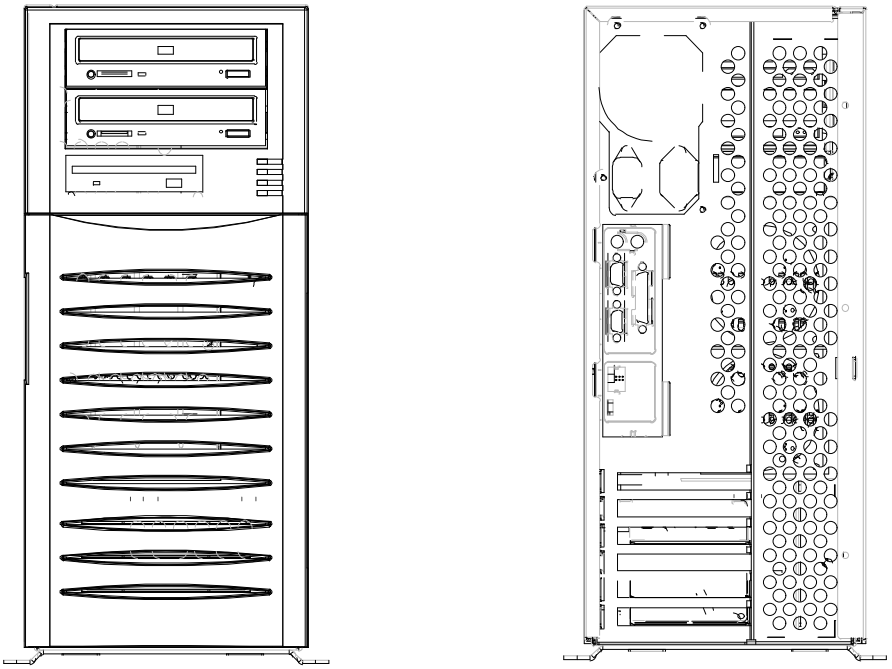

Figure 2: Front and Rear Chassis Views

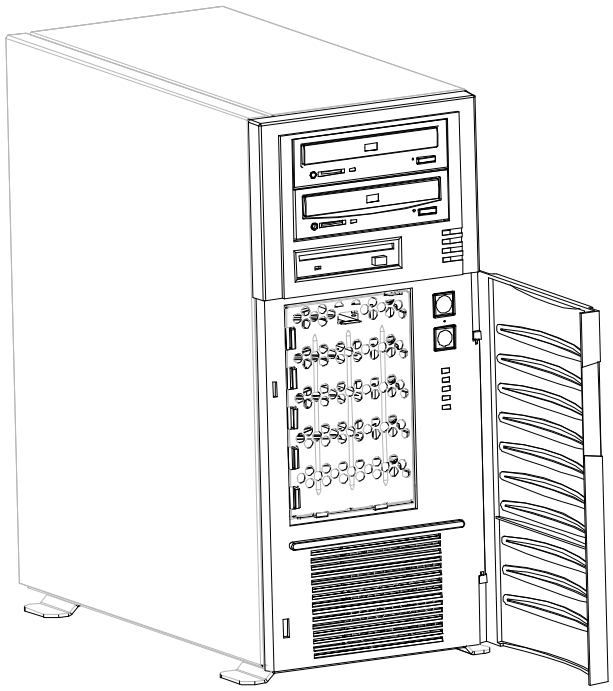

Figure 3: Front Isometric View, open Drive Access Door

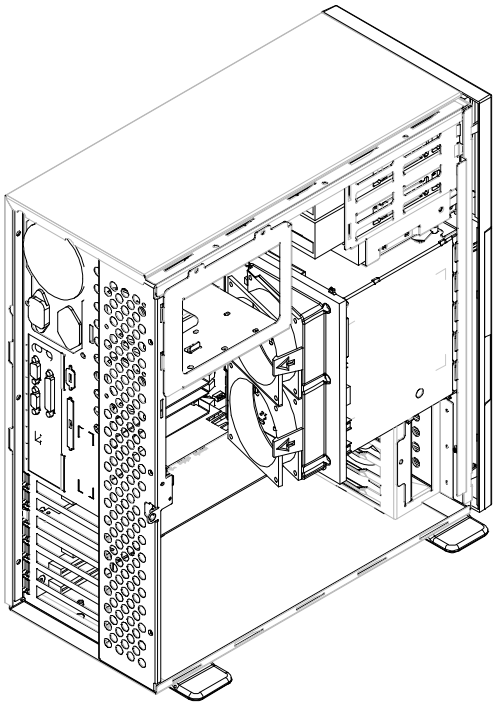

Figure 4: Rear Isometric View, open Access Cover

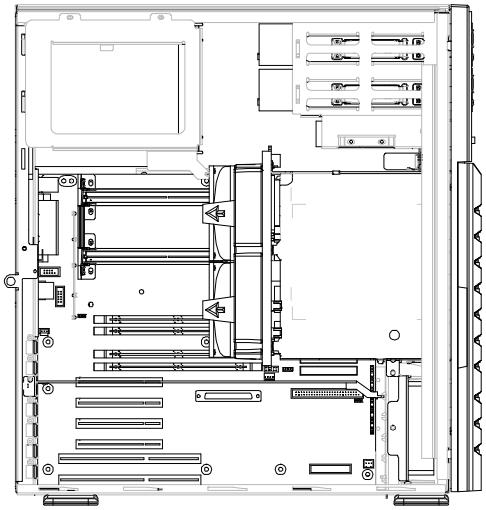

Figure 5: Side View showing N440BX DP Server board

1.6 Chassis Dimensions

Height	19.3 inches
Width	8.3 inches (chassis), 10 inches (feet)
Depth	17.7 inches
Clearance Front	8.5 inches
Clearance Rear	5 inches
Clearance Side	3 inches (additional side clearance required for service)

Table 1: Chassis Dimensions

2 CHASSIS POWER Sub-system

This chassis uses a standard PS/2 form factor power supply. Variations may be chosen for future board sets to satisfy the chassis power, power distribution, thermal performance, acoustic noise and cost requirements.

The form factor was chosen to optimize the overall chassis dimensions. The typical PS/2 form factor power supply with a remote enable feature can be used. The remote enable feature permits the chassis power to be activated from a variety of sources, allowing the implementation of "Wake On LAN*" (WOL) or other remote management features. The 300 watt power supply features a SSI compliant (Server Standards Infrastructure) "Modified ATX" server board power connector (ATX 20 pin + 4 additional pins) to accommodate the addition of +3.3 VDC and remote sense lines.

The following table is a brief overview:

	SSI compliant 300 Watt w/PFC 719680-XXX
+5 VDC Output	26 Amp Max
+12 VDC Output	10 Amp Sustained 13Amp/12sec peak current
-12 VDC Output	0.5 Amp Max
-5 VDC Output	0.25 Amp Max
+3.3 VDC Output	16 Amp Max
+5 VDC Standby	800 mA Max
Output balancing	Total combined output power of +3.3v and +5v shall not exceed 167 W.
AC Line Voltage	Autoranging for either 100-120 VAC or 200-240 VAC
AC Line Frequency	50/60 Hz
AC Input Current	4.6 Amp at 115 VAC 2.3 Amp at 220 VAC

Table 2: Power Supply Output Summary

2.1 Mechanical Outline

The mechanical outline and dimensions are the standard PS/2 Form factor. The approximate dimensions are 140mm high by 86mm wide by 150mm deep.

Figure 6: Chassis Power Supply Enclosure

2.2 Fan Requirements

The power supply incorporates a 80mm low acoustic noise fan to exhaust air. The sound pressure level is measured at a distance of 1.0 meter from each side of the power supply in a free field. The worst case peak value of the measurements shall not exceed 38 dBA at 23°C ±2°C.

Due to the increased output power requirements of the 5V standby circuit, power supply thermal margins are difficult to maintain while the system is in the “off” state. For this reason, the power supply fan will run at a reduced RPM when the chassis is off.

2.3 AC Power Line

The power supply is specified to operate from 100-120VAC, 200-240VAC, at 50 or 60Hz and is autoranging. The power supply is tested to meet these line voltages, and has been tested (but not specified) in a configured system at ±10% of the voltage ranges, and similarly ±3 Hz on the line input frequency.

The power supply, in a configured system, is specified to operate without error at full power supply output load, nominal input voltage, with line source interruptions not to exceed one period of the AC input power frequency (i.e., 20 milliseconds at 50 Hz).

The power supply is not damaged by AC surge ring wave up to 3.0kV/500A. This ring wave is a 100kHz damped oscillatory wave with a specified rise-time for the linear portion of the initial half-cycle of 0.5µsec. Additionally, the chassis will not be damaged by a unidirectional surge wave form of up to 1.5kV /3000A, with a 1.2µsec rise time and 50µsec duration. Further details on these waveforms can be obtained in ANSI/IEEE STD C62.45-1992.

2.4 DC Output

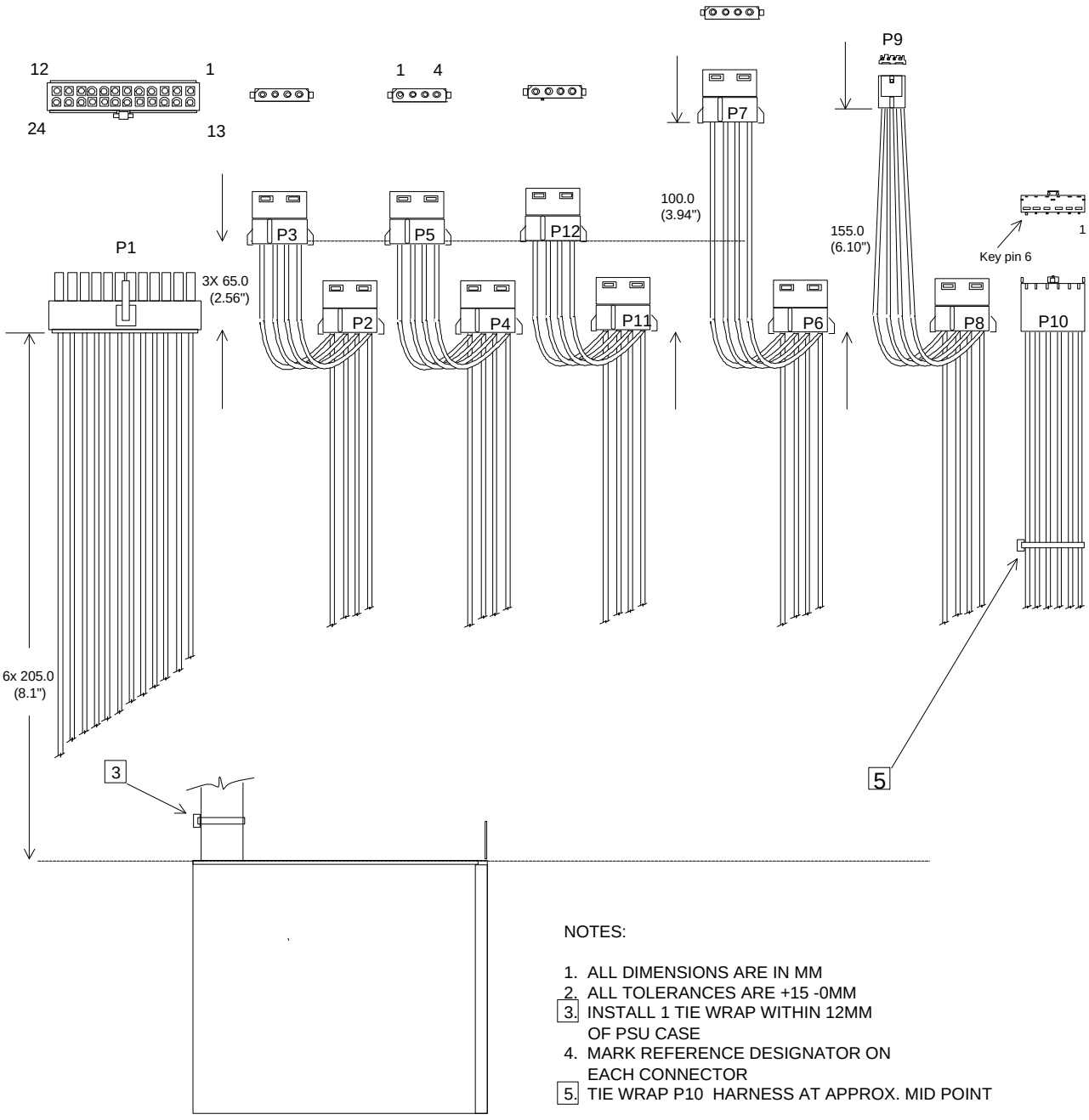

Figure 7: Power Supply Cabling

2.5 Power Supply Connector Pin Assignments

2.5.1 P1 Main power Connector:

Housing: 24 Pin Molex 39-01-2240, Contact: Molex 39-00-0038

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	+3.3Vdc	Orange	13	+3.3Vdc	Orange
2**	+3.3Vdc +3.3V remote sense	Orange Orange	14	-12Vdc	Blue
3**	COM 3.3V remote sense RTN	Black Black	15	COM	Black
4	+5 Vdc	Red	16	PS_ON_L	Green
5	COM	Black	17	COM	Black
6	+5 Vdc	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR OK	Gray	20	-5V	White
9	5VSB	Purple	21	+5 Vdc	Red
10	+12Vdc	Yellow	22	+5 Vdc	Red
11	+12Vdc	Yellow	23	+5 Vdc	Red
12	+3.3Vdc	Orange	24	COM	Black

Table 3: 20 + 4 pin "Modified ATX" Power Supply Connector

- Note**: The 3.3V power and 3.3V remote sense are double crimped into a single contact at pin 2. The 3.3V remote sense return and COM are double crimped into a single contact at pin 3.

- The "Modified ATX" main power connector is configured as the standard ATX 20 (2x10) pin connector plus a 2x2 (4) pinout designed to supply additional +5Vdc to the board. For connecting this into the L440GX+ server board, use the 24 pin power connector on the board. For connecting this into N440BX you must connect the first 20 pins of the power supply to the board's ATX power connector. In that case the last four pins will overhang relative to the main power connector.

2.5.2 P10 ATX AUX Power Connector

Housing: 6 Pin Molex 90331-0010, Contact: Molex 08-50-0277

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	COM	Black	4	+3.3Vdc	Orange
2	COM	Black	5	+3.3Vdc	Orange
3	COM	Black	6	+5 Vdc	Red

Table 4: Aux ATX Power Supply connector

2.5.3 P2-P8, P11, P12 Peripheral Power Connector:

Housing: Amp 1-480424-0, Contact: Amp 61314-1

PIN	Signal	18 AWG COLOR
1	+12Vdc	Yellow
2	COM	Black
3	COM	Black
4	+5 Vdc	Red

Table 5: Peripheral Power Connector

2.5.4 P9 Floppy Power Connector:

Amp 171822-4

PIN	SIGNAL	22 AWG COLOR
1	+5 Vdc	Red
2	COM	Black
3	COM	Black
4	+12Vdc	Yellow

Table 6: Floppy Drive Power connector

2.6 Power Supply/Chassis Configuration

The Astor II server chassis can only be configured with a single supply. For a more detailed specification on the power supply, see document 719680, the specification for the 300-Watt Power Supply w/PFC.

3 CHASSIS COOLING

Three system fans and the power supply fan will provide cooling for the processor(s), hard drives, and add-in cards. All chassis fans provide a signal for RPM detection that the server board can make available for server management monitoring and alert functions. Removal of the side cover gives access to the fans, which then can be easily changed with the system shut down. The single system fan located in the lower front of the chassis is configured for compatibility with the fan connector pin-out of either the L440GX+ or the N440BX server board. The fan should be connected to the server board with fan connector marked “ATX” for the L440GX+ server board and to the fan connector marked “N440” for the N440BX server board, see figure 6 below. The two fans mounted to the Hot-Swap SCSI backplane function identically but maintain only an ATX pin-out as they are connected directly to fan connectors on the backplane.

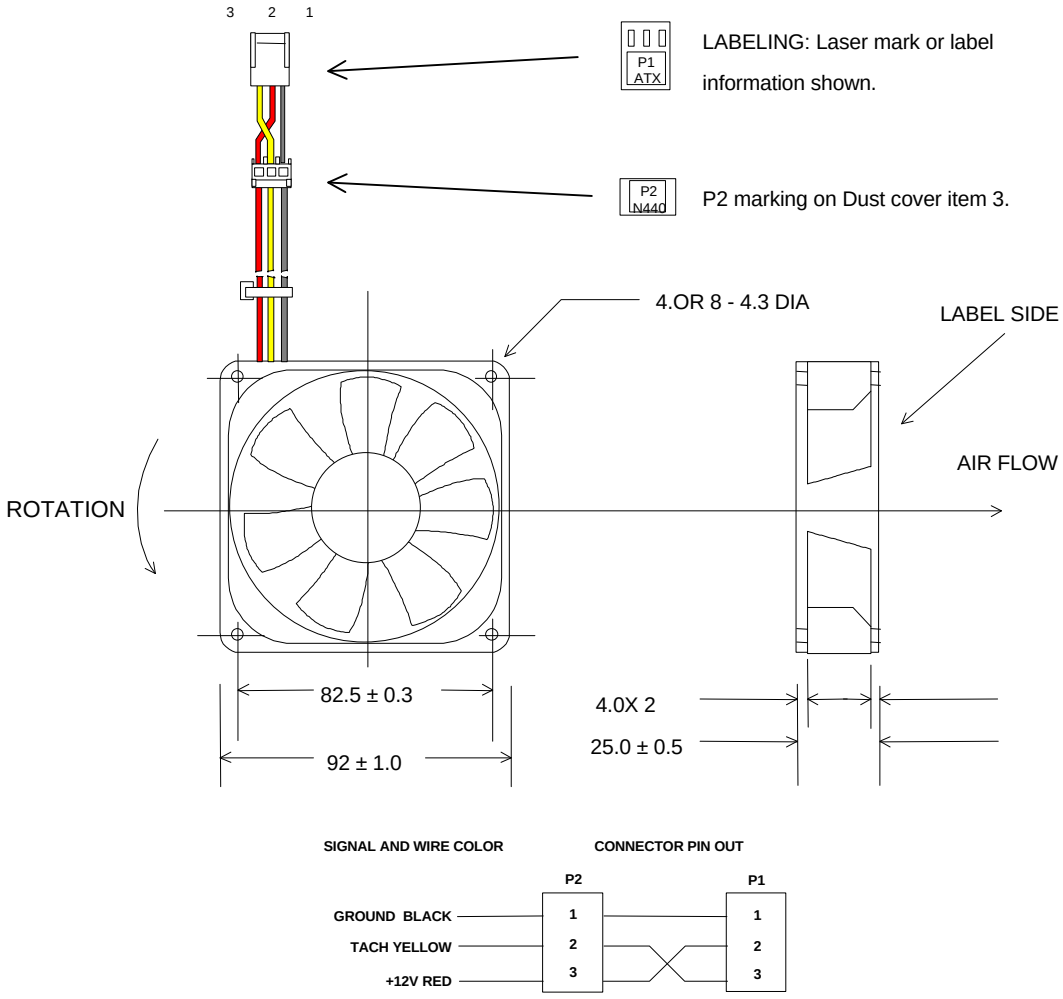

Figure 8: System Fan

4 CHASSIS PERIPHERAL BAYS

4.1 3.5" Floppy Drive Bay

The chassis kit provides for the installation of a 3.5“ floppy drive beneath the 5.25” peripheral bays. Removal of the side cover provides access for replacement of the floppy drive.

4.2 5.25" Drive Bays

The chassis supports two half height (1” high) or one full height 5.25" removable media peripheral devices (e.g. Magnetic/Optical disk, CD-ROM or tape drive), up to 9” deep. As a guideline based on cooling capabilities, the maximum recommended power per device is 17W. Thermal performance of specific devices must be verified to ensure compliance to the Drive manufacturer’s specifications.

The 5.25" peripherals are removable directly from the front of the chassis after removal of the side cover and front bezel. Cosmetic cover panels and EMI shield panels are installed in unused 5.25" bays.

> ***Caution****: These bays are not recommended for hard disk drives. Problems include hard disk drive generated EMI, increased ESD susceptibility (i.e., less hardened to ESD), and inadequate airflow for cooling.*

4.3 3.5" Hot Swap Hard Drive Bays

The Astor II server chassis supports up to five 3.5" SCA2 LVDS (Low Voltage Differential SCSI) hard drives which are accessible by opening the front access doors. Five low cost plastic carriers are provided with the chassis to be installed on the hard drives.

The Hot swap drive bay is designed to accept 1” peripherals that consume up to 17 Watts of power each. This wattage number is intended as a guideline based on chassis cooling capability. Thermal performance of specific hard drives must be verified to ensure compliance to the drive manufacturer’s specifications. Peripherals must be specified to operate at a maximum ambient temperature of 50^{O}C.

4.4 IDE Boot Drive Bracket

The Astor II chassis provides a bracket to support 2 IDE hard drives in the rear of the chassis, mounted sideways and vertically. These drives can be used to hold the operating system, and may be mirrored to provide operating system redundancy.

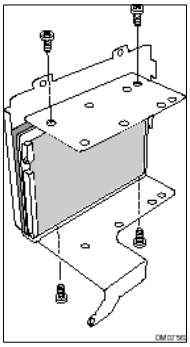

Figure 9: IDE Boot Drive Bracket

5 FRONT PANEL

The front panel is located in the right hand side of the front bezel. Opening the exterior hard drive access door accesses the momentary Power On/Off button, Chassis Reset button, and tool activated NMI switch. The front panel includes a green power on LED, a green hard drive activity LED, a green network activity LED and an amber fan failure LED, which are visible with the exterior hard drive access door closed. Five amber Hard drive fault LEDs indicate the specific drive failure, and are visible upon opening the exterior hard drive access door.

A 10-pin IDC ribbon cable connects the Front Panel board to the Hot-swap backplane to transfer drive, fan, and backplane temperature status to the server board and LED indicators.

A three-pin connector is provided on the front panel for connection of a chassis intrusion alarm switch, mounted in the rear of the chassis.

A 16-pin IDC ribbon cable connects the Server board to the Front Panel board to transfer all status information from the Hot-Swap SCSI backplane and the chassis intrusion switch, in addition to power, reset, and NMI control signals.

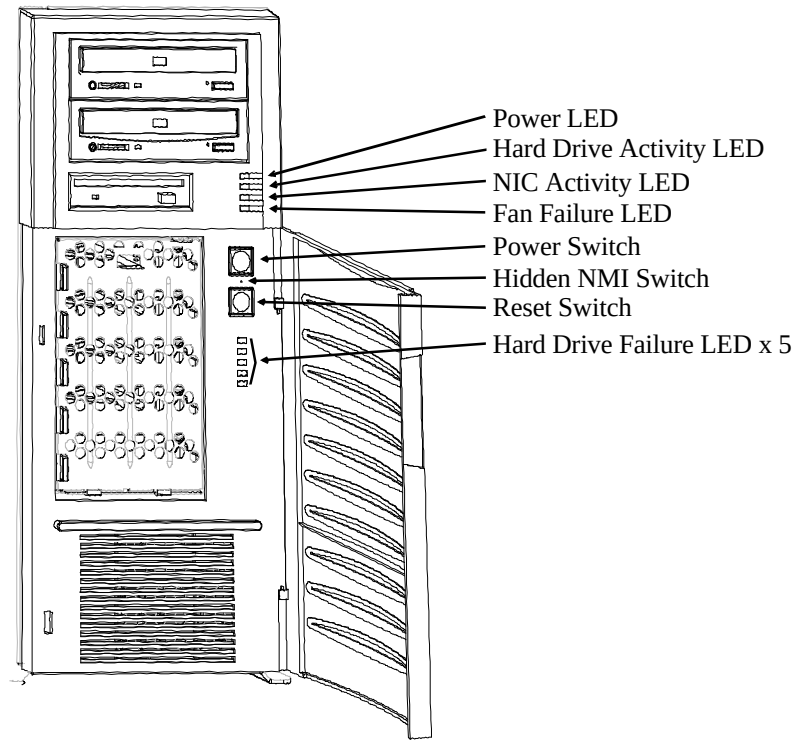

Figure 10: Front Panel and Functions

6 Hot-Swap SCSI Sub-System

The Hot-swap SCSI Sub-system supports the following features:

- Hot-swapping of SCSI drives, that allows connection of SCSI devices while the power is on.
- Enclosure management and monitoring functions conforming to the *SCSI-Accessed Fault-Tolerant Enclosures Specification* (SAF-TE), Revision 1.00.
- Full dual mode LVD/SE operation, compliant with Fast, Ultra and Ultra-2 SCSI bus operation.

6.1 Subsystem Purpose

The Astor II server chassis Hot-Swap SCSI Backplane performs the tasks associated with hot-swappable SCSI drives, and enclosure (chassis) monitoring and management, as specified in the *SAF-TE Specification*, Revision 1.00. The SAF-TE specified features supported by the Hot-swap SCSI Backplane include, but are not limited to, the following:

- Monitoring the SCSI bus for enclosure services messages, and acting on them appropriately. Examples of such messages include:
  - ⇒ Activate a drive fault indicator.
  - ⇒ Power down a drive that has failed.
  - ⇒ Report backplane temperature
- SAF-TE intelligent agent, which acts as proxy for "dumb" I^2C devices (that have no bus mastering capability) during intra-chassis communications.

6.1.1 Minimum Design Goals

The Astor II Hot-Swap SCSI Backplane is designed to provide at least the following:

1. Five SCA2 connectors for five SCA2 compatible SCSI drives
2. Active termination on SCSI bus (SCSI-3 compatible)
3. Per-drive power control, including automatic slot power down upon drive removal
4. Per-drive fault indicator support
5. Internal I^2C bus with temperature sensor
6. Two +12V connectors for fans with tachometers, with software power control
7. Intra-chassis I^2C bus support
8. Damage protection from defective drives

6.2 Abstract

The Astor II Hot-Swap SCSI Backplane is an embedded application subsystem, which during normal operation does the following:

1. Responds to SAF-TE messages (transmitted to the backplane via the SCSI bus).
2. Monitors the temperature on the backplane, and reports a warning or critical error if outside programmed limits.
3. Monitors the speed of the fans (if present), and reports a warning or critical error if outside programmed limits.

The Astor II Hot-Swap SCSI Backplane is made up of the following functional blocks:

- SCSI Bus with SCA (Single Connector Attach) drive connectors, and active terminators
- Microcontroller (Hot-Swap Controller or HSC) with program Flash and RAM
- SCSI interface that allows the microcontroller to respond as a SCSI target
- I^2C interface to chassis
- SCSI drive power control
- Fault indicator support
- Support for two cooling fans (fan-tachometer inputs and power control)
- Temperature sensor
- Configuration jumpers

6.3 Hot-Swap Backplane Board Layout

The Hot-Swap SCSI Backplane resides in the hot-swap drive bay of the Astor II server chassis.

The following diagram shows the layout of components and connectors on the Hot-swap SCSI Backplane printed circuit board. The ovals in the diagram below represent ventilation holes for the hard drive bay.

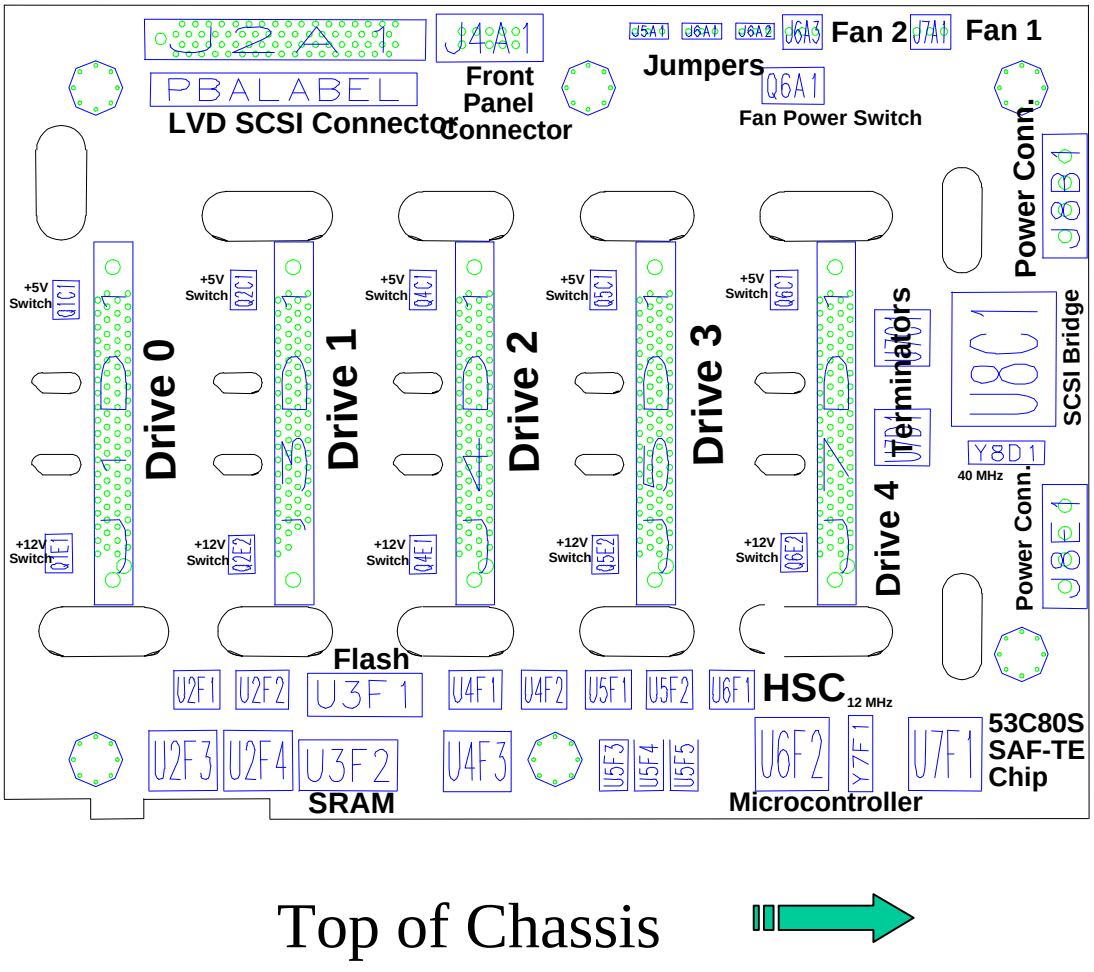

Figure 11. Astor II Hot-Swap SCSI Backplane Component and Connector Placement

6.3.1 Configuration Options

The following table describes the various configuration options on the Astor II Hot-Swap SCSI Backplane along with their function and intended usage.

Option	Jumper ID	Description
Firmware Update	J6A1	Placing this jumper in the "FORCE UPDATE" position forces external firmware update of the program code stored in Flash memory. Placing this jumper in the "NORMAL OPERATION" position allows normal operation.
Flash Boot Block Write	J6A2	This jumper allows the boot block of the program flash to be updated. "PROTECT" does not allow the boot block to be written to. "WRITE" allows updating of the boot block.

Table 7: HSBP Configuration Jumpers

**Jumper J5A1 depopulated on production chassis Hot-swap SCSI Backplane.

6.4 Design Constraints and Assumptions

This section specifies certain assumptions and limitations taken into consideration during the design of the Astor II Hot-Swap SCSI Backplane.

6.4.1 Single-Ended SCSI Bus Considerations

The Single-Ended (non LVS) SCSI bus, is based on the SCSI-3 specification, is designed to allow any SCSI device to communicate with any other SCSI device. To that end, SCSI-3 requires that all SCSI devices be at least 0.3m (11.81") apart (refer to draft-Proposed SCSI-3, section 6.4). Since this is a backplane, this specification is violated (drives are 1.3" apart). Therefore, certain design constraints must be placed on the backplane for the correct operation.

Only one initiator is allowed on the hot-swap SCSI bus. All SCSI devices on the backplane are targets. This arrangement eliminates communication over the SCSI bus devices when one of the devices (initiator or target) is not on the end of the bus, significantly reducing the signal reflections seen by the devices, and thereby increasing the signal quality at the receiver.

The SCSI Fast-20 specification requires the SCSI bus to be 59 inches (1.5m) or less in length. The backplane uses approximately 20 inches (0.51m). Therefore, the SCSI cable to the backplane must be 39 inches (0.99m) or less.

The SCSI cable must meet the following specification:

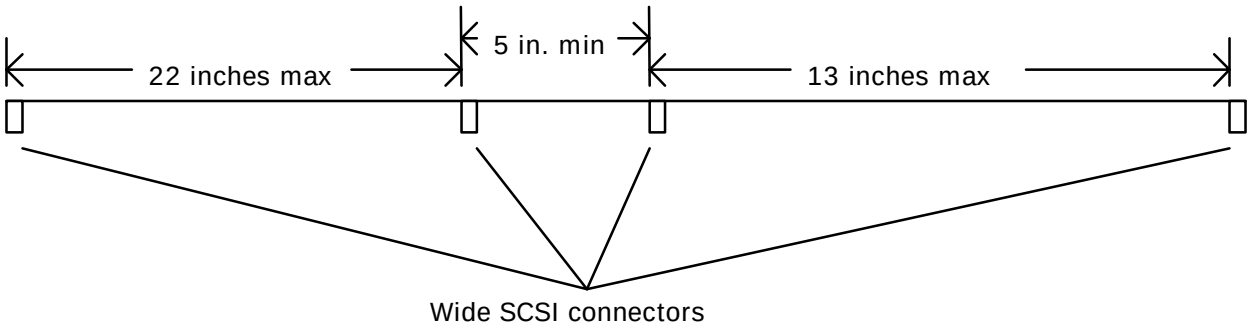

Figure 12. Single-Ended SCSI Bus Cable Length Specifications

The SCSI Fast-20 specification requires all SCSI devices on the bus to implement active-negation drivers. Since this requirement is new for Fast-20 SCSI, this product will require only those devices employing Fast-20 SCSI interfaces to implement active-negation drivers (non Fast-20 SCSI devices do not need to implement active-negation drivers).

6.4.2 Low Voltage Differential SCSI Considerations

LVD SCSI is backwards compatible to all previous SCSI specifications. The bus will autonegotiate to the slowest bandwidth device on the bus. Allowable cable lengths are much more forgiving and are inconsequential relative to the LVD SCSI backplane in the Astor II chassis.

6.4.3 Deviations from SAF-TE Specification

The SAF-TE specification, rev 1.00, requires the use of a “PAIR” signal. The intended use of this signal is to allow inter-backplane processor communication. This signal has not been implemented in prior designs. Therefore, this signal is deemed unnecessary and is not implemented here.

6.4.4 Miscellaneous

Per-drive power and activity indicators are not supported on the Astor II SCSI backplane. This information is provided through the IMB bus to the Baseboard Management Controller.

6.5 Functional Description

This chapter defines the architecture of the Astor II Hot-swap SCSI Backplane, including descriptions of functional blocks and how they operate. The following figure shows the functional blocks of the Hot-swap SCSI Backplane. An overview of each block follows.

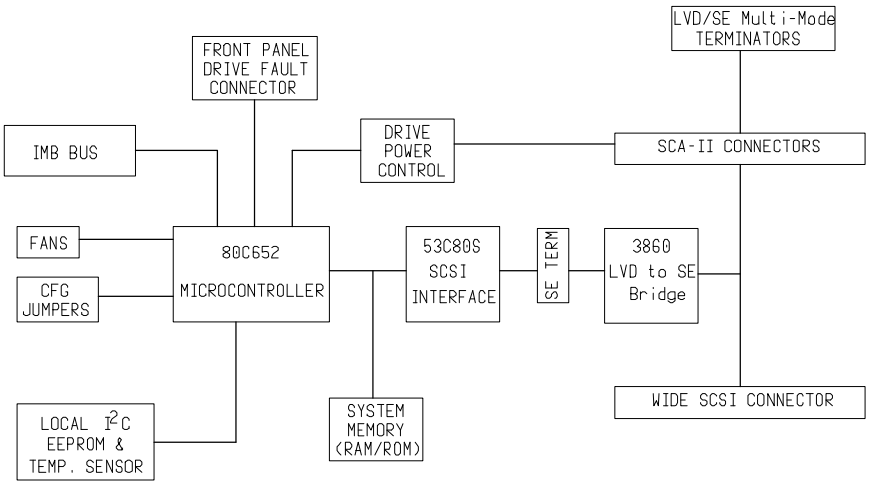

Figure 13. Functional Block Diagram

6.5.1 SCA2 Hot-Swap Connectors

The Astor II Hot-swap SCSI Backplane provides five hot-swap SCA2 connectors, which provide power and SCSI signals using a single connector. Each SCA drive attaches to the backplane using one of these connectors.

6.5.2 SCSI Interface

The SCSI interface on the Astor II Hot-swap SCSI Backplane provides the required circuitry between the SCSI bus and the microcontroller, which contains the intelligence for the Backplane. This allows the microcontroller to respond as a SCSI target. The interface consists of a Symbios* 53C80S SCSI Interface Chip, which functions as translator between the SCSI bus and the microcontroller. The 53C80S is a single-ended, narrow device.

6.5.3 LVD to SE Bridge

Since the 53C80S is a single-ended, narrow device, an Adaptec* AIC-3860 LVD-to-SE Transceiver (Bridge) is used to create a single-ended extension of the LVD bus. This allows the 53C80S to communicate with the LVD bus.

6.5.4 SE Termination

Passive SE termination is used for the single-ended extension of the SCSI bus that the 53C80S is on.

6.5.5 LVD/SE Multi-mode Active SCSI Termination

The SCSI active terminators provide SCSI-3 compliant active termination for the backplane end of the SCSI bus. It is assumed that the other end of the SCSI segment is properly terminated as required by the SCSI-3 specification. Multi-mode termination is implemented on the Astor II Hot-swap SCSI Backplane using two Unitrode* UCC5638 Multi-mode SCSI 15 line terminators.

6.5.6 Power Control

Power control on the Astor II Hot-swap SCSI Backplane supports the following features.

Power-down of a drive when failure is detected and reported (using enclosure services messages) via the SCSI bus. This decreases the likelihood that the drive, which may be under warranty, is damaged during removal from the hot-swap drive bay. When a new drive is inserted, the power control waits a small amount of time for the drive to be fully seated, and then applies power to the drive in preparation for operation.

- If system power is on, the Hot-swap SCSI Backplane immediately powers off a drive slot when it detects that a drive has been removed. This prevents possible damage to the drive when it is partially removed and re-inserted while full power is available, and disruption of the entire SCSI array from possible sags in supply voltage and resultant current spikes.

- Hot-spare drive support, where spare drives are kept in the hot-swap bay, but are left unpowered until a drive is determined to have failed. In this case, the hot spare can be powered up and put into service automatically without requiring immediate operator intervention to replace the drive.

- The Hot-swap SCSI Backplane will automatically bypass the power control circuitry if a shorted drive is inserted or if a drive develops a short during operation. This prevents the Hot-swap SCSI Backplane from being damaged by a drive which draws excessive current.

6.5.7 Power Requirements

The Hot-swap SCSI Backplane provides power to up to five peripherals, and if not provided by the SCSI host, termination power from the +5V supply. The following table shows the required amount of power that the backplane must supply:

Voltage:	+12V	+5V
Current, no drives installed	30mA	550mA
Current, 5 drives installed	3.03A*	3.55A*
Tolerance	+5% / -4%	+5% / -4%

*Based on 0.6A per drive

Table 8: HSBP Power Requirements

Note: Tolerance is specified at the power connectors on the backplane, and not at the output from the connector on the power supply (e.g., if the wiring loss from power supply to backplane is 1%, then the tolerance at the power supply must be +6% / -3%).

6.5.8 Microcontroller and Memory

The microcontroller provides the intelligence for the Astor II Hot-swap SCSI Backplane. It is implemented with a Phillips 80C652 microcontroller, with a built-in I^2C interface. The microcontroller uses a 2 Mbit FLASH EEPROM for program code storage, and a 32 KB SRAM for program execution.

6.5.9 Front Panel Drive Fault LEDs

The Drive Fault Indicators are not physically part of the Astor II Hot-swap SCSI Backplane, but rather located on the system front panel. They are referenced here because the driving circuitry is entirely contained on the backplane. The drive fault LEDs are activated by the microcontroller, and indicate failure status for each drive. A front panel interface connector is provided for an electrical path between the Hot-swap SCSI Backplane, drive fault LEDs, and front panel drive activity indication.

During initialization, the microcontroller flashes the LEDs for 1 second as part of the POST. Refer to "Front Panel Interface Connector" in Chapter 5 for more information.

6.5.10 IMB Bus

The IMB bus is a system-wide server management bus, based on the Phillips I^2C bus specification. It provides a way for various system components to communicate independently of the standard system interfaces (e.g., PCI bus or processor/memory bus). The I^2C bus controller is integrated into the microcontroller. IMB connectivity is provided to the Backplane via the front panel connector.

6.5.11 Fans

The Astor II Hot-swap SCSI Backplane supports the connection of two ATX-style fans with tachometer outputs that can be used by the microcontroller to assess the fans' operating condition before total failure (which may result in collateral hardware damage). The fans' digital outputs are connected to inputs on the microcontroller. Microcontroller program code is responsible for monitoring the fan speed and reporting of fan condition. Power to the fans can be switched on or off from the host via the I^2C bus through the microcontroller.

6.5.12 Local I^2C EEPROM & Temperature Sensor

An I^2C bus temperature sensor is connected to the microcontroller on a "private" I^2C bus. Microcontroller programming implements the private I^2C connection by explicitly setting and clearing appropriate clock and data signals, to emulate an I^2C-like interface to the sensor. Temperature information is made available to other devices in the chassis using Enclosure Services messages (refer to Chapter 4). A Dallas DS1624 Serial EEPROM/Temperature Sensor implements this function. The EEPROM stores the Field Replaceable Unit (FRU) information for the Backplane.

6.6 Programming Information

This section briefly describes the programming and firmware information for the Astor II Hot-swap SCSI Backplane.

The firmware for the Astor II Hot-swap SCSI Backplane is stored in the Flash ROM. It is divided into two sections, the 8KB boot block area and the 24KB operational code area. The boot block area contains the basic IMB communication routines and the firmware transfer commands. The code in this area is permanently stored and can only be updated if the Flash Boot Block Update jumper is in the proper position. The operational code area contains the run-time code, including the SCSI and SAF-TE routines, monitoring routines, and IMB routines. All code in this area can be updated using the firmware transfer commands.

6.6.1 Software Upgrade Process

Firmware update is accomplished by entering Firmware Transfer Mode, either through an IMB command or placing the Firmware Update Jumper in the Force Update position. The jumper position can be changed only when the system is powered off. Firmware transfers are done only through the IMB.

If an IMB command was used to enter Firmware Transfer Mode, the corresponding exit command is used to return to normal operation. If the jumper was used, the system must be powered down and the jumper restored to the Normal Operation position to return to operational mode.

7 CHASSIS INTERCONNECTION

7.1 Chassis Internal Cables

Intrusion Alarm cable

The side access cover depresses an open momentary switch. It is cabled to the baseboard by a 22AWG twisted pair, terminated with a 3-pin keyed latching connector or to the 3-pin header on the front panel board.

I^2C, Front Panel to Hot-swap Backplane

A 10-pin IDC ribbon cable connects the Front Panel board to the Hot-swap backplane to transfer drive, fan, and backplane temperature status to the server board and LED indicators.

Server board to Front Panel

A 16-pin IDC connector connects the Server board to the Front Panel board.

Server board to SCSI devices

A Wide SCSI cable (68 pin) is provided to interface from the installed server board to the Hot-Swap backplane.

Five SCA2 connectors provide interface between the Hot-Swap SCSI backplane and hot-swap SCSI devices.

Fan Connectors

The installed system fan provides two connectors, one designed to mate with an ATX compatible fan header used on the L440GX+, or the N440BX header. The system fan is depicted in figure 8, above. The connector pinouts are shown in the figure 18, below.

7.2 Connector Interfaces

Each pin is classified by type, as shown in the following table.

Type	Description
PWR	power connection (power or ground)
I/O	bi-directional signal
O	output signal
I	input signal
O/C	Open-collector output signal
O/D	Open-drain output signal

Table 9. Pin types

7.2.1 LVD SCSI Connector

The Wide SCSI connector is a 0.050” spacing 68-pin, unshielded connector.

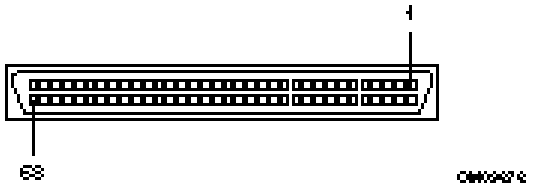

Figure 14: 68 pin SCSI wide connector

7.2.2 SCA2 connector

The SCA2 connector is a 80-pin, unshielded connector as defined in the SPI-2 specification.

Figure 15: 80 pin SCA2 connector

7.2.3 Hot-Swap Backplane and Peripheral Power Connectors

The Hot-swap backplane has two input power connectors. They are standard four-pin shrouded plastic PC power connectors with mechanical keying. Pinouts are below.

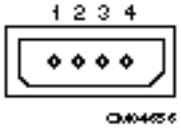

Figure 16: Peripheral power connector

Name	Pin	Description
+12V	1	+12 Volt power supply (yellow wire)
GND	2	0V Electrical ground (black wire)
GND	3	0V Electrical ground (black wire)
+5V	4	+5 Volt power supply (red wire)

Table 10: HSBP and Peripheral power connectors

7.2.4 Front Panel – Hot-Swap Backplane Interface Connector

The Front Panel Interface connector allows the Hot-swap SCSI Backplane to interface to the Front Panel board. This connector and its cable provide the chassis-wide I2C bus, and the electrical path between the drive fault indicators (LEDs) and the SCSI backplane that controls them.

The Front Panel Interface connector is a standard 0.1-inch spacing header with 0.025-inch square posts.

The front panel connector and cable provide the chassis wide IMB bus and the electrical path between the drive fault indicators (LEDs) and the SCSI backplane that controls them.

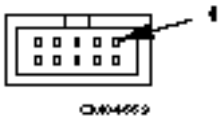

Figure 17: Front Panel to SCSI HSBP

Name	Pin	Description	Type	V/I Char.
GND	1	Electrical ground (0V)	PWR	
I2C_SDA	2	I^2C SDA (Serial Data)	I/O	
KEY	3	Pin removed for keying	N/A	
I2C_SCL	4	I^2C SCL (Serial Clock)	I/O	
PRI_SEC_L	5	Primary/Secondary backplane. The front panel connects this signal, via a resistor, to either VCC or GND, depending on which SCSI Backplane connector is used.	I	VIL = 0.8V @ .1mA
FAULT1_L	6	Fault signal for drive 1 (logical drive 0). Active low signal	O/C	VOL = 0.4V @ 24mA
FAULT2_L	7	Fault signal for drive 2 (logical drive 1) . Active low signal	O/C	VOL = 0.4V @ 24mA
FAULT3_L	8	Fault signal for drive 3 (logical drive 2) . Active low signal	O/C	VOL = 0.4V @ 24mA
FAULT4_L	9	Fault signal for drive 4 (logical drive 3) . Active low signal	O/C	VOL = 0.4V @ 24mA
FAULT5_L	10	Fault signal for drive 5 (logical drive 4) . Active low signal	O/C	VOL = 0.4V @ 24mA

Table 11: HSBP - Front Panel Interface Signal Descriptions

7.2.5 Fan Connectors

The hot-swap backplane contains two fan connectors. The Fan connectors are standard 0.1-inch spacing 3-pin headers with 0.025-inch square posts. They are mechanically keyed to prevent improper insertion. Pins are laid out in the ATX-style, with the power in the middle. The single system fan is configured with two connectors in order to accommodate the system fan pinout of both the L440GX+ and N440BX server boards, depicted below.

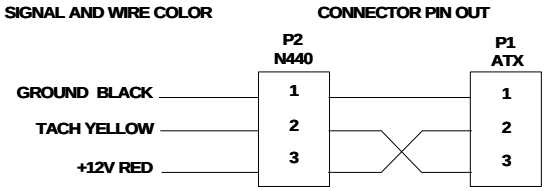

Figure 18: System Fan pinouts

8 SUPPORTED SERVER BOARDS

8.1 L440GX+ DP Server Board

- Support for Single or Dual Pentium® II processors of identical speed and stepping, current revision
- Designed around the Intel® 440GX AGPSet, PIIX4e, I/O APIC devices for full MPS 1.4 compliance.
- 100MHz System Bus (Front Side Bus)
- Up to 2 GB 100MHz “PC/100” compliant unbuffered or registered ECC or Non-ECC SDRAM DIMMs (4 sites)
- Dual Peer PCI buses with 4 full length PCI-33MHz/32bit slots and 2 full length “Universal (5v)” PCI-66MHz/32bit slots, backwards compatible to PCI-33MHz. PCI-66 implemented via Intel® 211150 AGP to PCI-66 bridge chip.
- 6 PCI full length slots
- Adaptec* AIC-7896 Dual function PCI SCSI controller providing Ultra2 (LVDS) wide and Ultra wide SCSI channels. Support for Adaptec ARO-1130U2 RAID*Port** “zero channel” RAID controller.
- Intel® 82559 PCI 10/100Mbit Ethernet controller with integrated physical layer.
- Cirrus Logic* GD5480 PCI SVGA graphics controller, 2MB of Synchronous Graphics memory (SGRAM)
- PCI IDE controller (in PIIX4E) providing dual independent Ultra DMA/33 IDE interfaces, each able to support 2 IDE drives.
- 1 ISA expansion slot.
- Compatibility I/O device integrating floppy, dual serial and parallel ports, all connectors provided.
- Universal Serial Bus (USB) support with two USB connectors.
- Integration of server management features, including thermal, voltage, fan, and chassis monitoring into one controller. Emergency Management Port (EMP) feature. Introducing Platform Event Paging (PEP) Feature enabling remote notification of significant server management events.
- Flash BIOS support for all of the above.

8.2 N440BX DP Server Board

- Support for Single or Dual Pentium® II processors of identical speed and stepping, current revision
- Designed around the Intel® 440BX AGPSet, PIIX4e, I/O APIC devices for full MPS (Multi-Processor Specification) 1.4 compliance.
- 100 MHz System Bus (Front Side Bus)
- Up to 1 GB with Dual Chip Select 100MHz “PC/100” compliant unbuffered or registered ECC or Non-ECC SDRAM DIMMs (4 sites)
- 3 PCI Full length slots
- 1 shared full length PCI/ISA slot
- 1 Full length ISA slot
- 1x32 bit PCI bus
- Symbios* 53C876 PCI Dual SCSI controller, Ultra Wide and Ultra Narrow
- Intel® 82558 PCI 10/100Mb Ethernet controller with integrated physical layer.
- Cirrus Logic* GD5480 PCI SVGA graphics controller, 2MB of Synchronous Graphics memory (SGRAM)
- PCI IDE controller (in PIIX4E) providing dual independent Ultra DMA/33 IDE interfaces, each able to support 2 IDE drives
- Integration of server management features, including thermal, voltage, fan, and chassis monitoring into one controller. Introduction of the Emergency Management Port (EMP) feature enabling remote server monitoring and management.
- keyboard, mouse ports (stacked 6 pin)
- 1-parallel port
- 2-serial ports (one 9-pin D-sub, one 10-pin header)
- USB header
- Flash BIOS support for all of the above.

9 Regulatory Information

CAUTION

Integration of this subassembly is a regulated activity: you must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product regulations. Use only the described, regulated components specified in this guide. Use of other products / components will void the UL listing of the product, will most likely void other compliance markings provided, and may result in noncompliance with product regulations in the region(s) in which the product is sold.

9.1 Regulatory Compliance

This subassembly, when correctly integrated per this guide, complies with the following safety and electromagnetic compatibility (EMC) regulations.

9.1.1 Safety Standards

9.1.2 EMC Regulations

9.1.2.1 FCC Class B

Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)

9.1.2.2 CISPR 22, 2nd Edition, 1993, Amendment 1, 1995

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)

9.1.2.3 EN 55 022, 1995

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)

9.1.2.4 EN 50 082-1, 1992

Generic Immunity Standard. Currently, compliance is determined via testing to IEC 801-2, -3 and -4. (Europe)

9.1.2.5 VCCI Class B (ITE)

Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)

9.1.2.6 ICES-003, Issue 2

Interference Causing Equipment Standard, Digital Apparatus. (Canada)

9.1.2.7 Australian Communication Authority (ACA)

Australian C-tick mark, limits and methods of measurement radio interference characteristics of information technology equipment to ASNZS 3548 (Australian requirements based on CISPR 22 requirements).

9.1.2.8 New Zealand Ministry of Commerce

Australian C-tick mark, limits and methods of measurement radio interference characteristics of information technology equipment to ASNZS 3548 (New Zealand requirements based on CISPR 22 requirements). New Zealand authorities accept ACA C-Tick Compliance Mark.

9.1.3 Regulatory Compliance Markings

This Astor II chassis subassembly is provided with the following Product Certification Markings.

- UL and cUL Listing Marks
- CE Mark
- The CE marking on this product indicates that it is in compliance with the European community's EMC (89/336/EEC) and low voltage directives (73/23/EEC)
- NEMKO Mark
- FCC, Class B Markings (Declaration of Conformity)
- ICES-003 (Canada Compliance Marking)

9.2 Electromagnetic Compatibility Notice (USA)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on; the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

✏ NOTE

If a Class A device is installed within this system, then the system is to be considered a Class A system. In this configuration, operation of this equipment in a residential area is likely to cause harmful interference.

9.2.1 FCC Declaration of Conformity

Product Type: ASTNIT, ASTLAN

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: 1) This device may not cause harmful interference, and 2) this device must accept any interference received, including interference that may cause undesired operation.

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124-6497
Phone: 1-800-628-8686

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe B prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadian des Communications.

(English translation of the notice above) This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the interference causing equipment standard entitled "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

9.3 Electromagnetic Compatibility Notices (International)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＢ情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
取扱説明書に従って正しい取り扱いをして下さい。

(English translation of the notice above) This is a Class B product based on the standard of the Voluntary Control Council For Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

When used near a radio or TV receiver, it may become the cause of radio interference.

Read the instructions for correct handling.

This equipment has been tested for radio frequency emissions and has been verified to meet CISPR 22 Class B.

10 ENVIRONMENTAL LIMITS

10.1 System Office Environment

Parameter	Limits
Operating Temperature	+5^{o}C to +35^{o}C with the maximum rate of change not to exceed 10^{o}C per hour.
Non-Operating Temperature	-40^{o}C to +70^{o}C
Non-Operating Humidity	95%, non-condensing @ 30^{o}C
Acoustic noise	< 45 dBA in an idle state at typical office ambient temperature (65-75F)
Operating Shock	No errors with a half sine wave shock of 2G (with 11 millisecond duration).
Package Shock	Operational after a 24 inch free fall, although cosmetic damage may be present
ESD	20kV per Intel Environmental test specification

Table 12: System Office Environment Summary

10.2 System Environmental Testing

The system will be tested per the Environmental Standards Handbook, Intel Doc.#662394-03. These tests shall include:

Temperature Operating and Non-Operating

Humidity Non-Operating

Packaged and Unpackaged Shock

Packaged and Unpackaged Vibration

AC Voltage, Freq. & Source Interrupt

AC Surge

Acoustics

ESD

EMC Radiated Investigation

11 RELIABILITY, SERVICEABILITY AND AVAILABILITY

11.1 Mean-Time-Between-Failure (MTBF)

MTBF data was being collected at the time of the generation of this specification. It will be provided in a future revision of this specification or a Specification Update.

11.2 Serviceability

The system is designed to be serviced by qualified technical personnel only.

The desired Mean Time To Repair (MTTR) of the system is 30 minutes including diagnosis of the system problem. To meet this goal, the system enclosure and hardware have been designed to minimize the MTTR.

Following are the maximum times that a trained field service technician should take to perform the listed system maintenance procedures, after diagnosis of the system.

Remove cover	1 minute
Remove and replace hard disk drive	1 minute
Remove and replace 5 ¼ peripheral device	5 minutes
Remove and replace power supply	5 minutes
Remove and replace drive cage fan	2 minutes
Remove and replace card cage fan	5 minutes
Remove and replace expansion board	5 minutes
Remove and replace front panel board	5 minutes
Remove and replace baseboard (with no expansion boards)	10 minutes
Overall MTTR	20 minutes