Intel® L440GX+ Server Board Specification Update

Release Date: Aug., 1999

Order Number: 245145-006

The L440GX+ Server Board may contain design defects or errors known as errata that may cause the product to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

REVISION HISTORY

Date of Revision	Description
April, 1999	This document is the first Specification Update for the L440GX+ Server Board and Astor II and the Columbus III Chassis
May 1999	Astor II and Columbus III updates have been removed from the original and placed in their own documents.
June, 1999	Updated Erratum 7 to fixed, added erratum 14. Updated Documentation changes 1-3 to fixed, added documentation change 4.
July, 1999	Added BIOS 6.0 and erratum 15.
Aug., 1999	Added BIOS 6.1, added Doc erratum #5

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PREFACE

This document is an update to the information contained in the *L440GX+ Server Board Technical Product Specification.* It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Specification Clarifications, Errata, and Document Changes.

Refer to the *Pentium® II Processor Specification Update* (Order Number 243337) for specification updates concerning the Pentium II processor. Items contained in the Pentium II Processor Specification Update that either do not apply to the L440GX+ Server Board or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Refer to the latest *Intel 82440GX AGPset Specification Update* for specification updates concerning the Intel 82440GX AGPset. Items contained in these Specification Updates that either do not apply to the L440GX+ Server Board or have been worked around are noted in this document. Otherwise, it should be assumed that any AGPset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications for the L440GX+ Server Board. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specification.

Errata are design defects or errors. Errata may cause the L440GX+ Server Board to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.

GENERAL INFORMATION

Identification Information

Below are the specific boards, BIOS and components covered by this update. The information in the table shows BIOS and Firmware revisions associated with PBA and AA numbers as they were shipped from the factory. Updated revisions of the BIOS and Firmware may be available from the WEB and not yet implemented into the factory.

L440GX+

Baseboard PBA #	Baseboard AA #	BIOS	BMC Firmware Rev.
704293-404	721242-002	Production Rel. 2	Release 0.12
704293-405	721242-003	Production Rel. 3	Release 0.12
704293-407	721242-005	Production Rel. 6	Release 1.02
704293-408	721242-006	Production Rel. 7	Release 1.04

Summary Table of Changes

The following tables indicate the Errata and the Document Changes that apply to the L440GX+ Server Board. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Intel intends to update the appropriate documentation in a future revision.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	Plans	ERRATA
1	Fixed	ISC 1.8 shows the slot width for PCI Slot #4 as a 64 bit slot
2	No Fix	Turning on an external modem will power up the system
3	No Fix	Master read I2C command (app 51h) fails on public/private I2C bus
4	No Fix	Wake On LAN fails after AC power is applied to the board the 1st time
5	Fix	Wake On LAN does not wake up system from an S1 sleep state in Windows* 98
6	Fix	Wake on Ring does not wake up system from an S1 sleep state in Windows* 98
7	Fixed	Modem Does not issue page
8	Fixed	L440GX+ incorrectly identifies the Pentium® III as a Pentium® II during POST
9	Fixed	Early versions of the Intel® Pro100+ NIC cause the L440GX+ to power on after exiting NT.
10	No Fix	The BMC will not generate SEL events for either Upper or Lower non-recoverable threshold crossings for analog sensors, even when enabled to do so.
11	No Fix	Manually re-arming digital sensors events via the “Re-Arm Sensor Event” command does not work.
12	Fixed	BMC Firmware is not able to accurately report lower critical temperature events accurately
13	Fixed	Voltage events incorrectly logged in SEL for LVD termination voltage sensors
14	Fixed	Data errors from DMI type 6 and type 17 inquiries
15	Fixed	L440GX+ Diagnostics 1.01 does not accurately detect Pentium® III processors
16	Fix	System Hangs when using BMC forced update
17	Fix	Enabling fixed disk boot sector write protect option fails
18	Fixed	L440GX+ Diagnostics 1.01 or 1.02 dos not detect 256MB and 512MB DIMMS properly

NO.	Plans	DOCUMENT CHANGES
1	Fixed	L440GX+ rev. 0.9 TPS – AT Style Front Panel Connector Table 2-13 corrected
2	Fixed	Clarifications made to which Adaptec ARO RAID card is supported in TPS
3	Fixed	All references to Intel® Pentium® Pro in the L440GX+ 0.9 TPS will be changed to Intel® Pentium® II
4	Fixed	Clarification of SCSI termination in product guide
5	Doc	Clarification of PERR# in L440GX+ TPS
6	Doc	Corrected BIOS table showing proper System Event Logging formats

ERRATA

1. ISC 1.8 shows the slot width for PCI Slot #4 as a 64 bit slot

Problem: PCI Slot-4 as referenced by ISC 1.8 shows a 64 bit slot when it is actually a 32 bit slot.

Workaround: None

Status: FIXED - UPGRADING SYSTEM BIOS TO PRODUCTION RELEASE 5 OR GREATER WILL CORRECT THIS ISSUE

2. Turning on an external modem will power up the system

Problem: If the system is configured with the modem enabled and EMP is disabled, applying power to the modem will cause the system to power up. When an external modem is attached to either COM port, the system powers up when the modem is turned on.

Implication: This is a side effect of having the wake on ring event enabled

Workaround: If the system and modem are both powered at the same time with power state retention not set, both the system and modem will function as expected. Or, If the system has AC removed but the modem has AC power applied, both the modem and the system will function as expected.

Status: No Fix planned

3. Master read I2C command (app 51h) fails on public/private I2C bus

Problem: The Master Read I2C command fails to operate correctly on either the public IPMB or the private I2C bus. If used on the public bus, the command may cause the bus to hang, disrupting communication to other controllers on that bus.

Implication: The IPMB or I2C bus may hang

Workaround: None. The Master Read I2C command should not be used

Status: Will not be fixed for the L440GX+. But will be fixed for future products

4. Wake On LAN fails after AC power is applied to the board the 1st time

Problem: Failure only seen when a device is attached to the IMB connector that is powered when the board has ac power removed. This condition causes the 5V_stby rail to maintain 0.5V. This is enough power to hold the data stored in the SRAM of the BMC

Workaround: Cold Boot system after Wake On LAN fails the 1st time.

Status: No Fix

5. Wake On LAN does not wake up system from an S1 sleep state in Windows 98*

Problem: WOL works for powering on the system, but fails to bring the system out of Standby mode.

Workaround: None

Status: Fix - Windows 98 does not support WOL from Standby with the current release of the OS. This will be fixed in a future Windows 98 Service Pack.

6. Wake on Ring does not wake up system from an S1 sleep state in Windows 98*

Problem: Using Windows 98, the system will not exit from an S1 Sleep state with a ring indication from a modem attached to any com port.

Workaround: NONE

Status: Fix - Windows 98 does not support WOR in the initial release of the OS. It will be supported in a future Windows 98 Service Pack.

7. Modem Does not issue page

Problem: While issuing pages using an external modem, only TR light on modem remains lit and no pages are issued.

Workaround: None

Status: Fixed – This was fixed in version BMC firmware 1.02

8. L440GX+ incorrectly identifies the Pentium® III as a Pentium® II during POST

Problem: BIOS revisions up to and including Production Release 1 do not post the correct banner during Post when a Pentium III processor is detected.

Workaround: Upgrade to later BIOS

Status: Fixed – This issue has been addressed in BIOS Production Release 3.

9. Early versions of the Intel® EtherExpress™ Pro100+ NIC cause the L440GX+ to power on after exiting NT.

Problem: EtherExpress Pro100+ NICs with PBA# 668081-00x use an A-step of the 82558 network controller which has ESD errata against it causing improper behavior of a system's Power-On capabilities. Therefore, a problem was seen when performing a "Shutdown" from Windows* NT that after the system was powered down the system would automatically Power back up after approximately 2-4 seconds.

Workaround: Upgrade to an EtherExpress Pro100+ NIC with PBA# 697680-001 or later

Status: - Fixed

10. The BMC will not generate SEL events for either Upper or Lower non-recoverable threshold crossings for analog sensors, even when enabled to do so.

Problem: If the Baseboard Management Controller (BMC) detects an Upper or Lower value for a "Non-Recoverable" event, the event is not logged in the System Event Log (SEL). This affects all analog voltage, temperature and fan sensors.

Implications: If "Non-Recoverable" events are programmed into the Server Management Software, the Upper and Lower limits programmed for these events are not logged.

Workaround: Only program the BMC to log Upper and Lower limits for critical and Non-critical events.

Status: – No Fix for L440GX+. This will be addressed in future platforms.

11. Manually re-arming digital sensor events via the "Re-Arm Sensor Event" command does not work

Problem: Manually re-arming digital sensor events via the "Re-Arm Sensor Event" command does not work. This affects the digital fans and chassis intrusion sensor.

Workaround: None – The sensors will automatically re-arm when the sensor state goes from a triggered to a non-triggered state.

Status: No fix for L440GX+ - this will be addressed in future platforms

12. BMC Firmware Rel 0.12 is not able to accurately report lower critical temperature events accurately

Problem: If the temperature sensors read temperatures below 0 Degrees Celsius, the BMC firmware incorrectly reports the temperature as a high temperature value in the system event log.

Workaround: None.

Status: Fixed – Upgrading BMC Firmware to release 1.02 or later will fix this problem.

13. Voltage events are incorrectly logged in SEL for LVD termination voltage sensors

Problem: During POST, the BMC firmware may report Low voltage events to the system event log. This may occur if the BMC firmware scans the LVD voltage sensors before they are set. This is only seen if POST requires additional time prior to the BMC firmware scanning these sensors. Systems with large memory configurations may experience this problem do to the time required to test the memory during POST.

Workaround: Disable the LVD voltage sensors until the BMC firmware is updated to a later release that fixes this problem.

Status: Fixed – Upgrading BMC firmware to release 1.02 or later will fix this issue.

14. Data errors from DMI type 6 and type 17 inquiries.

Problem: During DMI type 6 and type 17 inquiries, incorrect data may be returned

Workaround: None.

Status: Fixed – Upgrading system BIOS to Production release 6 or later will fix this issue.

15. L440GX+ Diagnostics 1.01 does not accurately detect Pentium III processors.

Problem: When the L440GX+ Diagnostics utility auto detects installed hardware, it wrongly displays Pentium® III processors as Pentium® II processors.

Workaround: None. The diagnostics utility will run normally with Pentium III processors installed. This is only a cosmetic reporting issue.

Status: Fixed – L440GX+ Diagnostics 1.02 fixes this issue.

16. System Hangs when using BMC forced update

Problem: When attempting to force update the BMC Firmware using the “BMC FRC Up” jumper, the system will hang after setting the jumper and rebooting to start the update procedure.

Workaround: Use the standard procedure for updating BMC firmware. The “BMC FRC UP” jumper will not be supported until the issue is addressed

Status: FIX – This will be fixed in a future release of the BIOS

17. Enabling fixed disk boot sector write protect option fails

Problem: After enabling the BIOS option “Fixed Disk Boot Sector Write Protect” the hard disk’s boot block is still not protected.

Workaround: None

Status: Fix – This option will be fixed in a later release of the BIOS

18. L440GX+ Diagnostics 1.01 or 1.02 dos not detect 256MB and 512MB DIMMS properly

Problem: The L440GX+ Diagnostic Utility 1.01 and 1.02 does not accurately detect 256MB or 512MB DIMMs if all DIMM slots are populated.

Workaround: To validate the memory subsystem on the L440GX+ using the Diagnostic Utility, use either up to 3 of the larger DIMMS, listed above, or use DIMMs smaller than 256MB.

Status: FIXED – This issue has been addressed in L440GX+ Diagnostics rev 1.03

DOCUMENTATION CHANGES

1. AT style front panel pinout table corrected

A 19-pin single inline header labeled J6J1 is provided for AT-style front panel connections, e.g., power, LED indicators, and reset. The connector has the following pinout:

Table 2-13. AT Front Panel Header Pinout

Pin	Signal
1	Pwr_Cntrl_Fp – 5V_STNDBY
2	Ground
3	No Pin
4	Hd_LED_Pwr – VCC
5	No Pin
6	Fp_HD_Act
7	Hd_LED_Pwr – VCC
8	Ground
9	No Pin
10	Spkr_Int
11	Spkr_Out
12	Ground
13	No Pin
14	Pwr_LED
15	No Pin
16	Ground
17	Rst_Fp
18	Fp_Sleep
19	Ground

Status: This was updated in the L440GX+ Technical Product Specification (TPS) rev. 1.0

2. Clarifications made to which Adaptec ARO RAID card is supported

In the L440GX+ Technical Product Specification (TPS), all references for the Adaptec ARO SCSI RAID card will be changed to “Adaptec ARO-1130U2 RAIDPort”, to better identify which Adaptec ARO card the L440GX+ server board has support for.

Status: This was updated in the L440GX+ Technical Product Specification (TPS) rev. 1.0

3. All references to Intel® Pentium® Pro in the L440GX+ 0.9 TPS will be changed to Intel® Pentium® II

To avoid confusion, all references to Intel® Pentium® Pro in the L440GX+ 0.9 TPS will be changed to Intel® Pentium® II

Status: This was updated in the L440GX+ Technical Product Specification (TPS) rev. 1.0

4. Clarification of SCSI termination in L440GX+ Product Guide

To avoid confusion about termination of the L440GX+ SCSI bus when using LVDS devices the following text has been rewritten on page 15 in the second paragraph of the SCSI controller section.

> "The SCSI bus is terminated on the server board with active terminators that cannot be disabled. The onboard device must always be at one end of the bus. The device at the end of the cable must be terminated. LVDS devices generally do not have termination capabilities. Non-LVDS devices generally are terminated through a jumper or resistor pack. If your device does not have a termination jumper or resistor pack, you must add a terminator to the end of the cable. A terminator is not supplied with your board. You must purchase one separately."

Status: To be updated in the L440GX+ Server Board Product Guide, Order Number: 722077-003

5. Clarification of PERR# in the L440GX+ TPS

To avoid confusion about the function of the PCI error (PERR#) signal the L440GX+, Section 7.3.1 PCI Bus Error, located on page 78 of the L440GX+ TPS will be corrected as follows.

> The second sentence reads "the BIOS can be instructed to enable or disable reporting PERR# and SERR# through NMI." This will be corrected to remove all references to PERR#. The Eighth sentence reading "The same is true for PERR#" will be removed.

Status: To be updated in the L440GX+ Technical Product Specification (TPS)

6. Corrected Table showing System Event Logging Formats

The "System Event Logging Format" table located in the L440GX+ BIOS EPS rev 1.0 showed an incorrect format for Single Bit Memory Errors and Multi Bit Memory Errors.

> BIOS complies with the Platform Sensor and Event Interface EPS, Revision 1.0. The BIOS always uses a software ID of 0 to log POST errors. SMM handler uses software ID of 10h. OEM user binary should use software IDs of 1 and SMM User Binary should use an ID of 11h. The Software ID allows external software to find the origin of the event message.
>
> The BIOS uses the following sensor numbers while logging events. Application software can examine the sensor number field in the log record to determine the source of error. The *Platform Sensor and Event Interface EPS* requires that distinct sensor numbers are used for different error sources.

System Event Logging Format

Event Types	**Sensor Type/Sensor #/ Type Code/Data bytes 1,2,3.**
single bit memory error	0C *EF E7 40 DIMM# FF
multi bit memory error	0C *EF E7 41 DIMM# FF
memory parity error	0C *EF E7 02 FF FF
front panel NMI	13 28 E7 00 FF FF
bus timeout	13 *EF E7 01 FF FF
I/O chk	13 *EF E7 02 FF FF
software NMI	13 *EF E7 03 FF FF
PCI PERR	13 *EF E7 04 FF FF
Note: * Sensor # = 0EFh (not applicable). Other fields are sufficient enough to identify type of errors.	

> *The BIOS treats all the above sensors as discrete sensors*. The 4 bit offset field in the first event data byte indicates the exact cause of the error. In all the events logged by the BIOS, up to 2

OEM data bytes are used to indicate the physical location of the error, such as the DIMM row number. Application software must examine these bytes to point to the exact source of error within a 'virtual sensor' Table X describes the various fields in the event request message, as sent by the BIOS.

Status: The table and paragraphs shown will replace the original document entry in the next EPS revision.