Enterprise Server Group
Intel N440BX Server
Technical Product Specification

Version 2.0
Order Number: 243701-002
April, 1999

The Intel N440BX Server may contain design defects or errors known as errata. Characterized errata that may cause the N440BX Server's behavior to deviate from published specifications are documented in the N440BX Server Specification Update.

Revision History

Revision	Revision History	Date
Rev 1.0	Initial release of the Intel N440BX Server Technical Product Specification	2/98
Rev 2.0	Updated and included specification updates changes.	4/99

***NOTE**: If printing this document from an electronic file, use a PostScript printer with the appropriate PostScript print driver to insure the drawings print clearly.*

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1. Board Set Descriptions

1.1. Product Overview

The Intel N440BX Server is a flat baseboard design featuring a dual Pentium® II processor or Pentium® III processor based server system that combines the latest technology and integrated features to provide a high-performance platform optimized for 100 MHz system bus operation.

The N440BX Server baseboard utilizes the Intel 440BX PCIset, the latest in chipset technology from Intel, to maximize system performance for 32-bit application software and operating systems. The N440BX Server baseboard high performance is driven by a 100 MHz processor/memory architecture enabled by the Intel 440BX PCIset.

The N440BX Server design is complemented with an array of features. These include:

- Two Single Edge Contact (SEC) cartridge connectors (to accommodate dual Pentium II processors or Pentium III processor).
- Using dual processors, the system is fully MPS 1.4 compliant (with appropriate Slot 1 Pentium II processor extensions or Pentium III processor extensions). In addition, support is provided for MP operating systems that may not be fully MPS 1.4 compliant.
- System design based on Intel 440BX, PIIX4, and I/O APIC devices.
- 100 MHz main memory interface supporting up to 1GB of PC/100-compliant commodity SDRAM DIMMs.
- PCI I/O system, compliant with revision 2.1 of the PCI specification. PCI interface is provided by the NBX host bridge
- Dual function PCI SCSI controller (Symbios 53C876*) providing Ultra wide and legacy narrow SCSI channels.
- Intel EtherExpress™ PRO/100+ 10/100 NIC with integrated physical layer (Intel 82558)
- Cirrus Logic CL-GD5480* 2D PCI video controller with 2MB of video memory onboard.
- PCI IDE controller (in PIIX4) providing dual independent Ultra DMA/33 IDE interfaces, each able to support 2 IDE drives.
- National Super I/O* 87309 I/O controller which provides floppy, parallel, serial, keyboard, mouse).
- 4 PCI expansion slots, 2 ISA expansion slots (1 shared with a PCI slot).
- Compatibility I/O device integrating floppy, dual serial and parallel ports.
- Integration of server management features, including thermal, voltage, fan, and chassis monitoring into one controller. Introduction of Emergency Management Port (EMP) feature.
- Optional Universal Serial Bus (USB) support.

The N440BX Server baseboard supports dual 266, 300, 333, 350, 400, 450 MHz Pentium® II processors and the 500MHz Pentium® III processors contained on Single Edge Contact (SEC) or SECC2 cartridges. The SEC and SECC2 cartridges enclose the processor with 512KB of integrated ECC L2 cache to enable high-frequency operation. Two SEC cartridge connectors are embedded on the N440BX Server baseboard. The N440BX Server baseboard design will accommodate identified upgrades to future Intel processing technology.

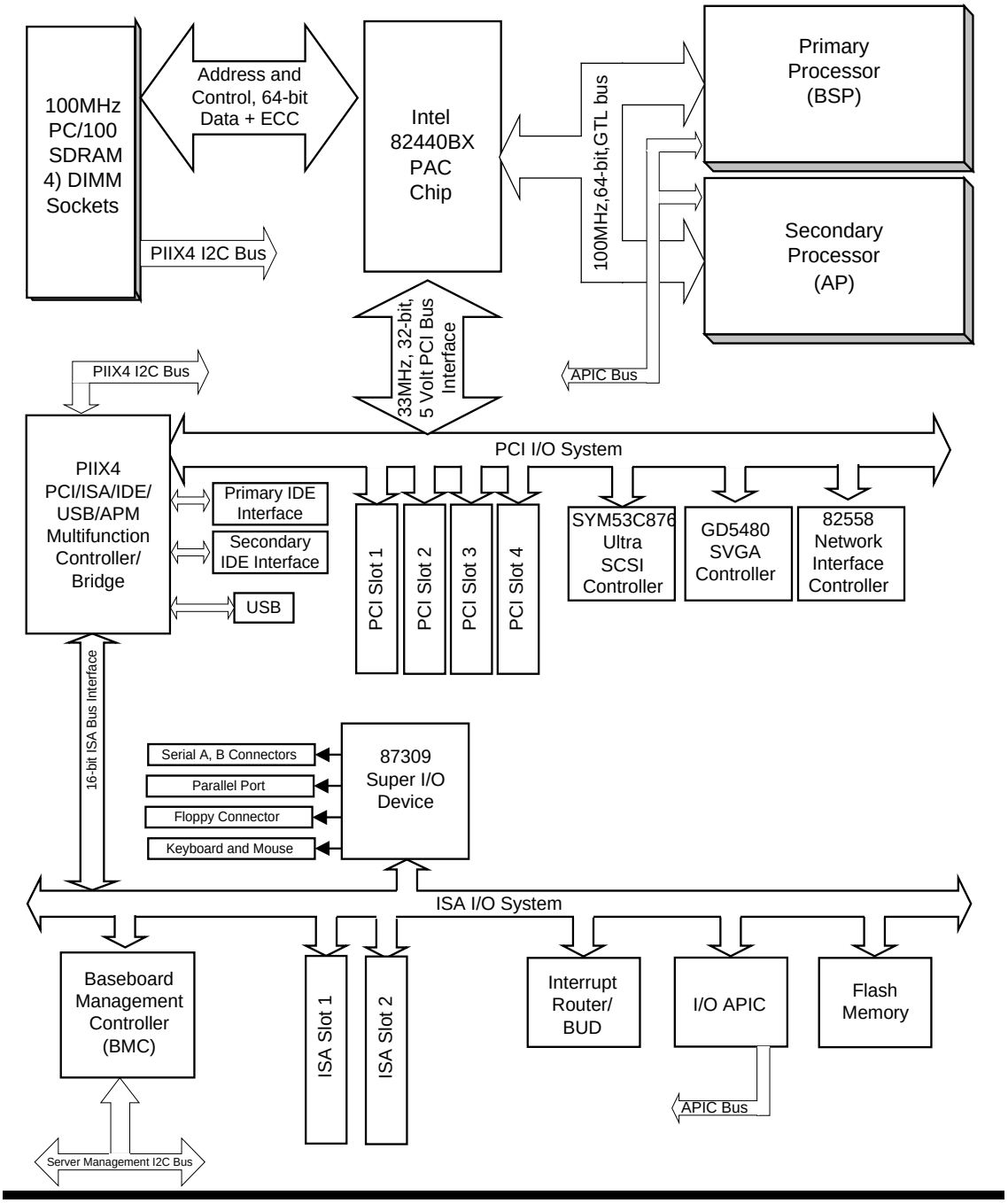
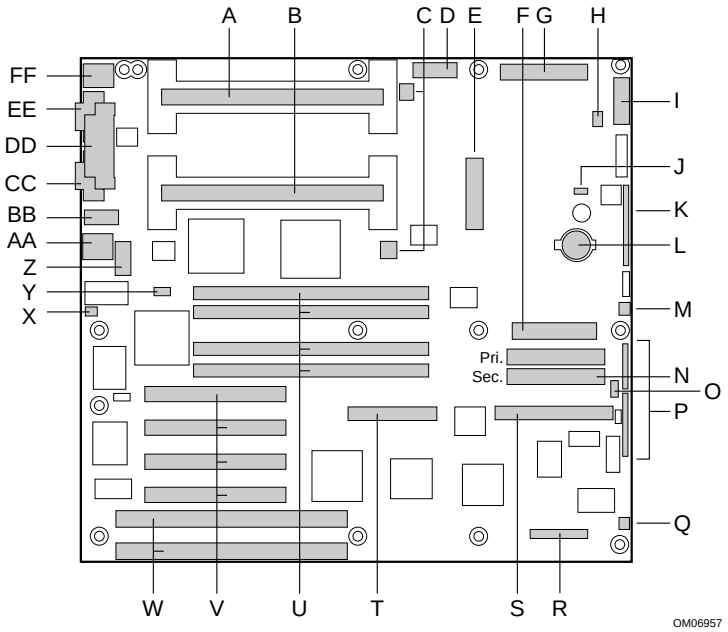


Figure 1.1 N440BX Server Functional Block Architecture

1.2. Baseboard Diagram

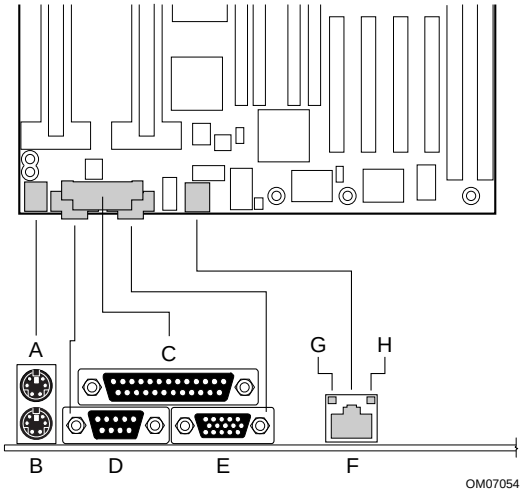
The following diagram shows the placement of major components and connector interfaces on the N440BX Server baseboard. A mechanical layout is available in the appendix. Server Board Components



A. Secondary processor connector	Q. System fan connector (fan2)
B. Primary processor connector	R. Server monitor module (SMM) connector
C. Processor Heatsink fan connectors	S. Narrow SCSI connector
D. Aux power connector	T. Wide SCSI connector
E. ATX power connector	U. Memory sockets for four DIMM components
F. Diskette drive connector	V. PCI slots for add-in boards
G. Main power connector	W. ISA slots for add-in boards
H. Hard drive LED connector	X. Chassis intrusion connector
I. Front panel connector, 16 pin	Y. WOL enable jumper
J. Speaker connector	Z. USB header
K. AT† front panel connector	AA. RJ-45 network connector
L. Lithium backup battery	BB. Serial port 2 header
M. System fan connector (fan1)	CC. VGA† monitor port
N. IDE connectors, primary and secondary	DD. Parallel port connector
O. External IMB connector	EE. Serial port 1 connector
P. Configuration jumper blocks	FF. Keyboard and Mouse PS/2† compatible connectors

Figure 1.2 N440BX Baseboard Layout

1.3 Back Panel Connectors



A.	Mouse Connector
B.	Keyboard Connector
C.	Parallel Port Connector
D.	Serial Port Connector
E.	VGA Connector
F.	Network Connector
G.	Green NIC LED
H.	Orange NIC LED

Figure 1.3 N440BX Back Panel Connectors

NOTE

Serial Port 2 connector required for EMP: *If you wish to use the Emergency Management Port (EMP) features and software, you must install a serial port connector and connect it to the header on the server board. If there is no opening on the chassis I/O shield, use the included expansion slot cover.*

NICLED Color	If it's on	If it's blinking	If it's off
Orange	100 Mbps network connection.	NA	10 Mbps network connection.
Green	Linked to network, no network traffic.	Linked to network, sending or receiving data.	Not linked to network.

1.4 Jumpers

One 12-pin single inline header and one 9-pin single inline header provide seven 3-pin jumper blocks that control various configuration options, as shown in the figure below. The shaded areas show default jumper placement for each configurable option. Refer to the *N440BX Product Guide* for more information.

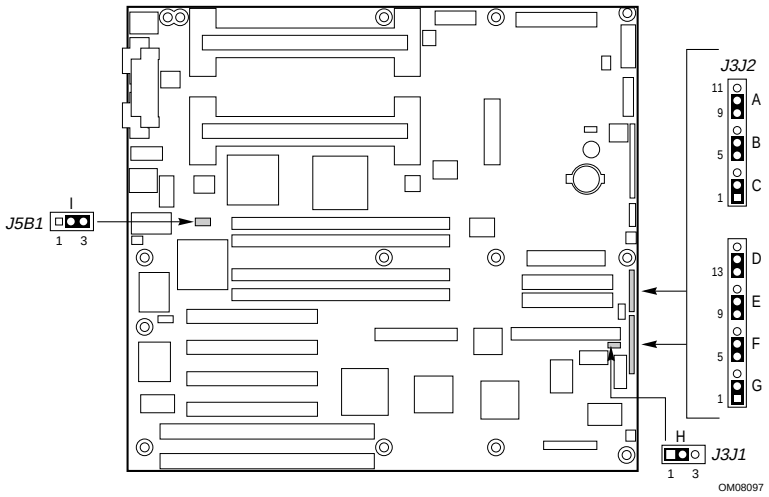


Figure 1.4 N440BX Jumper Connectors

Jumper Block	Pins (default in bold)	What it does at system reset
A. BMC Forced Update Mode	**9-10, Normal**	System boots normally.
	10-11, Program	System tries to update BMC firmware.
B. Chassis Intrusion Detection	**5-6, Enable**	Switch installed on chassis indicates when cover has been removed.
	6-7, Disable	Chassis intrusion switch is bypassed.
C. FRB Timer Enable	**1-2, Enable**	FRB operation is enabled (system boots from processor 1 if processor 0 fails).
	2-3, Disable	FRB is disabled.
D. Boot Block Write Protect	**13-14, Protect**	BIOS boot block is write-protected.
	14-15 Erase/Program	BIOS boot block is erasable and programmable.
E. Recovery Boot	**9-10, Normal**	System attempts to boot using the BIOS stored in flash memory.
	10-11, Recovery	BIOS attempts a recovery boot, loading BIOS code from a floppy diskette into the flash device. This is typically used when the BIOS code has been corrupted.
F. Password clear	**5-6, Protect**	Maintains the current system password.
	6-7, Erase	Clears the password.
G. CMOS clear	**1-2, Protect**	Preserves the contents of NVRAM.
	2-3, Erase	Replaces the contents of NVRAM with the manufacturing default settings.
H. BMC boot block write protect	**1-2, Protect**	BMC boot block is write protected.
	2-3, Erase/Program	BMC boot block is erasable and programmable.
I. WOL Enable	**1-2, Disabled**	Disables Wake On LAN. If your power supply does not provide 0.8 A of +5 V Standby current, you must move the WOL Enable jumper to

		this position.
	2-3, Enabled	Enables Wake On LAN.

⚠ CAUTION

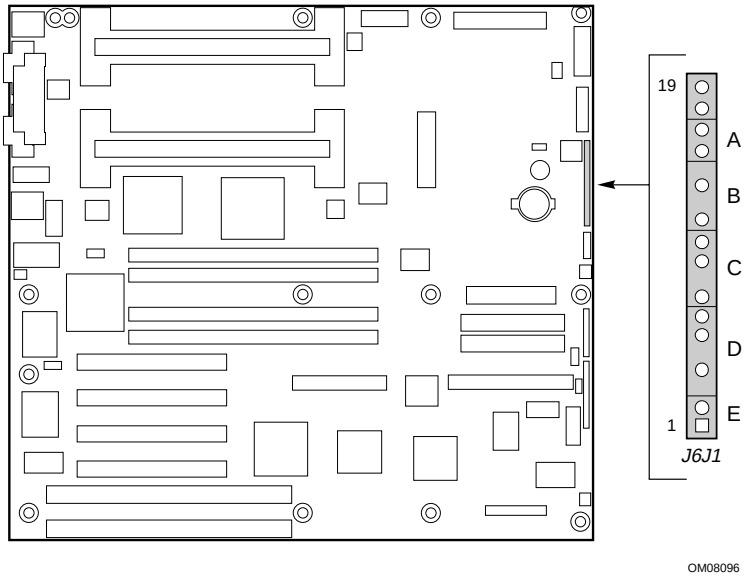
Moving either of the boot block write protect jumpers (J3J2-D or J3J1) may cause significant damage to the server board. Only move these jumpers when directed to by your customer service representative.

NOTE

+5 V Standby required for WOL: *If you wish to use the WOL feature, your power supply must provide 0.8 A of +5 V Standby current. If it does not, your server board may not boot. Move the WOL Enable jumper to the Disabled position if your power supply does not provide the required current.*

1.4.1 ATX (Front Panel) Controls and Indicators

The N440BX server board has connectors that meet the standard AT interface for LED indicators and other functions. The connector block is at J6J1.



Connector		Pin	Signal
A.	**Reset switch**	17	Reset switch
		16	GND
B.	**Power LED**	14	GND
		13	N/C
		12	+5V
C.	**Speaker**	11	SPKR_HDR
		10	PIEZO_IN
		9	N/C
		8	GND
D.	**Hard drive activity LED**	7	+5V
		6	HD activity LED
		5	N/C
		4	+5V
E.	**Power switch**	2	GND
		1	Power button

Figure 1.4.1 N440BX ATX Front Panel Connectors

1.5. Baseboard Architecture Overview

N440BX Server baseboard architecture is based on a design supporting dual processor operation using Pentium® II SEC or SECC2 cartridges, Pentium® III SECC2 cartridges and the Intel 440BX PCIset. N440BX provides a PCI-based I/O subsystem containing embedded devices for video, NIC, SCSI, and IDE, along with an ISA bridge to support compatibility devices. The baseboard also provides Server Management, and monitoring hardware support and interrupt control that supports dual processor and PC/AT compatible operation. This section provides an overview of these N440BX Server subsystems:

- Support for one to two identical Pentium II processor SEC or SECC2 cartridges, and Pentium III processor SECC2 cartridges.
- Two "Slot 1" edge connectors operating at 100MHz
- Two embedded VRM 8.1-compliant voltage regulators for primary and secondary processor cards.
- Intel 440BX chipset providing processor host interface, PCI bridge, and memory controller with 100MHz pathway to memory.
- 4 DIMM sockets that support PC/100-compliant SDRAM devices.
- 33MHz, 5V PCI segment with four expansion connectors and four embedded devices.
- PCI/ISA/IDE Accelerator (PIIX4) for PCI-to-ISA bridge, and PCI IDE interface, USB controller, and power management controller.
- PCI video controller - Cirrus Logic GD5480.
- PCI dual function SCSI controller - Symbios SYM53C876, supporting narrow and wide SCSI interfaces onboard.
- "RAID-upgradeable" PCI slot with special interrupt capabilities supporting I^2O RAID card by AMI (RAIDExpress* 762)**.**
- PCI Network Interface Controller (NIC) with integrated physical layer - Intel 82558.
- ISA bus segment with two expansion connectors and four embedded devices.
- National Semiconductor 87309 SuperI/O controller chip providing all PC-compatible I/O (floppy, parallel, serial, keyboard, mouse).
- I/O APIC
- Flash memory for system BIOS.
- Server management host interface.
- Interrupt Router and BUD (Basic Utility Device) implemented using an Altera PLD.
- Single server management micro-controller providing monitoring, alerting, and logging of critical system information from embedded sensors on baseboard. N440BX introduces the EMP (Emergency Management Port) interface for remote access to this information, along with reset and power control, via external modem.

1.6. Pentium® II/ Pentium® III Processor(s)

The N440BX Server is optimized to function with the Pentium® II processor SEC or SECC2 cartridges and Pentium® III processor cartridges. The Pentium II processor and Pentium III processor core/L1 cache appears on one side of a pre-assembled printed circuit board, approximately 2.5" x 5" in size, with the L2 cache on the backside. The L2 cache and processor core/L1 cache connect using a private bus isolated from the processor host bus. The L2 cache bus operates at half of the processor core frequency.

The Pentium II and Pentium III processor packages follows Single Edge Contact (SEC) or SECC2 cartridge form factor, and provides a thermal plate for heatsink attachment with a plastic cover located opposite the thermal plate.

The Pentium II processor and Pentium III processor internal core can operate at frequencies of 266, 300, 333, 350, 400, 450, and 500MHz.

The Pentium II processor's and the Pentium III processor's external interface is designed to be MP-ready. Each processor contains a local APIC section for interrupt handling. When two processors are installed, the pair must be of identical revision, core voltage, and bus/core speeds. If only one processor is installed, the other Slot 1 connector must have a terminator card installed.

1.7. VRM

The N440BX Server provides two embedded VRM 8.1-compliant voltage regulator (DC-to-DC converter) to provide VCC_P to each of the Pentium II processors or Pentium III processor. One VRM is powered from the 5V supply and the other by the 12V supply. Each VRM automatically determines the proper output voltage as required by each processor.

1.8. 440BX Host Bridge / Memory Controller

N440BX architecture is designed around the Intel 440BX PCIset. This device provides 100MHz processor host bus interface support, DRAM controller, PCI bus interface, AGP interface (not used on N440BX), and power management functions. The host bus/memory interface in the NBX is optimized for 100MHz operation, using 100MHz SDRAM main memory. The PCI interface is PCI 2.1-compliant, providing a 33 MHz / 5V signaling environment for embedded controllers and slots in the single PCI segment on N440BX. The NBX memory controller supports up to 1 GB of ECC memory, using PC/100 compliant Synchronous DRAM (SDRAM) devices on DIMM plug-in modules. ECC can detect and correct single-bit errors, and detect multiple-bit errors.

The AGP interface is not used on N440BX.

1.8.1. Memory

The N440BX Server baseboard only supports 100MHz, PC/100-compliant SDRAM DIMMs. Two types of memory devices on the DIMMs are supported: registered or unbuffered. The baseboard provides four DIMM sites. Only ECC (72-bit) DIMMs are specified for use in the N440BX Server system.

The PIIX4 provides a local IMB interface to SDRAM DIMM information, SDRAM clock buffer control, and processor core speed configuration. The BIOS code uses this interface during auto-configuration of the processor/memory subsystem, as part of the overall server management scheme.

1.8.2. PCI I/O Subsystem

The primary I/O bus for N440BX Server is PCI, compliant with revision 2.1 of the PCI specification. The PCI bus on N440BX Server supports embedded SCSI, network control, video, and a multi-function device that provides a PCI-to-ISA bridge, bus master IDE controller, Universal Serial Bus (USB) controller, and power management controller. The PCI bus also supports four slots for full-length PCI add-in cards (one shared with an ISA slot).

1.9. PCI SCSI Subsystem

The embedded SCSI controller on N440BX Server is the Symbios SYM53C876 dual function controller. This device provides both Ultra wide and legacy narrow SCSI interfaces as two independent PCI functions[1]. PCI slot 3 is RAID-upgradeable, providing additional support for an Intelligent I/O (I^2O) RAID controller by AMI.

1.10. PCI Network Interface Subsystem

The network interface on N440BX Server is implemented using an Intel 82558, which provides a 10/100Mbit Ethernet interface supporting 10baseT and 10baseTX, integrated with an RJ45 physical interface. The 82558 also provides Wake-On-LAN functionality if the power supply supports a minimum of 800mA of 5V standby current (configurable via baseboard jumper).

1.11. PCI Video Subsystem

The embedded SVGA-compatible video controller on N440BX Server is a Cirrus Logic GD5480 SGRAM GUI Accelerator. The SVGA subsystem also contains 2MB of SGRAM (synchronous graphics RAM), which is provided as a factory built option and is not upgradeable.

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[1] The PIIX4 and SYM53C876 are “Multi-function” PCI devices that provide separate sets of configuration registers for each function, while sharing a single PCI hardware connection. Refer to the PCI specification.

1.12. ISA I/O Subsystem

N440BX Server contains a full-featured ISA I/O subsystem with two full length ISA slots (one shared with a PCI slot), and local ISA bus interface to embedded SuperI/O, I/O APIC, Flash BIOS, Basic Utility Device (BUD), and server management features.

1.13. National 87309 SuperI/O Controller

Compatibility I/O on N440BX Server is implemented using a National PC87309VLJ component. This device integrates a floppy disk controller, keyboard and mouse controller, two enhanced UARTs, full IEEE 1284 parallel port, and support for power management. The chip provides separate configuration register sets for each supported function. Connectors are provided for all compatibility I/O devices.

1.14. I/O APIC

The N440BX Server baseboard incorporates an Intel S82093AA Advanced Programmable Interrupt Controller to handle interrupts in accordance with Multiprocessor Specification 1.4.

1.15. Flash BIOS

The BIOS for the N440BX Server baseboard resides in an Intel 28F008S5 FlashFile Memory Family, 8Mbit, symmetrically blocked (64KB) flash device.

1.16. Server Management Subsystem

The N440BX Server incorporates a Dallas 82CH10 micro-controller as baseboard management controller (BMC). The BMC controls and monitors server management features on the baseboard, and provides the ISA interface to two independent IMB-based serial buses. In previous Intel Server baseboard products, the Server Management features were handled by three controllers. On the N440BX Server, all functions of the former Front Panel Controller (FPC) and the Processor Board Controller (PBC) are integrated into the BMC. This includes power supply on/off control, hard reset control, video blanking, watchdog timers, Fault Resilient Booting (FRB) functionality, and all temperature, voltage, fan and chassis intrusion monitoring. The BMC can be polled for current status, or configured to automatically send an alert message when an error condition is detected either manually or by software.

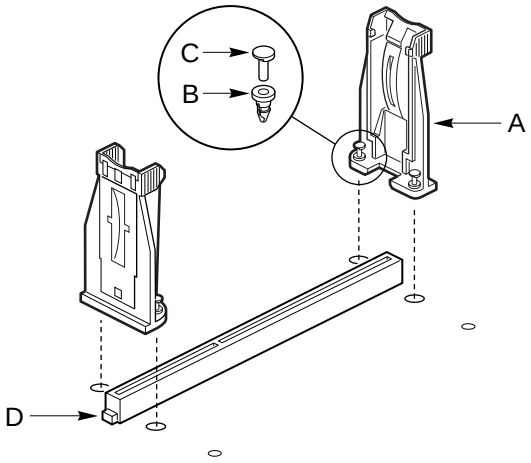
In addition, the N440BX Server baseboard provides a new server management feature: EMP (Emergency Management Port). This allows, when using an external modem, remote reset, power up/down control, and access to the event log, or run-time information. This port also supports console redirection and with additional software support, the EMP can also be used to download firmware and BIOS upgrades in future upgrades.

1.17. Basic Utility Device

The N440BX Server provides the Basic Utility Device (BUD) for ISA and PCI interrupt routing, SMI/NMI routing, and PCI arbitration expansion. The physical device is an Altera 7128 CPLD. Other features formerly handled by an external CPLD on previous servers, such as the host ISA interface to server management functions, now appear in the BMC.

1.18. Universal Retention Module

The Pentium® II processor/Pentium® III processor universal retention module is used to add stability to the SEC connector. The SEC cartridges are mounted with a retention mechanism, which is provided with the N440BX server board.



1 Orient the retention mechanism (A) so the grommets (B) line up with the holes in the server board.

2 Press the pins (C) so they are flush with the grommets.

3 Repeat for both sides of both processor slots.

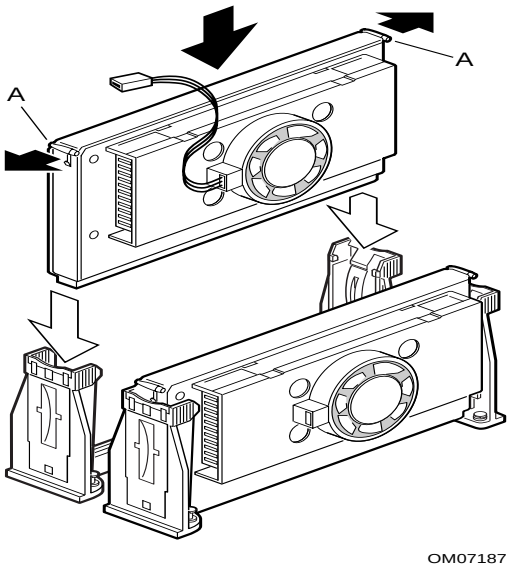


Figure 1.18 N440BX Universal Retention Modules

1.18.1. Cartridge Connector

The Pentium® II processor/Pentium® III processor SEC connector conforms to the "Slot 1" specification, which can also accommodate future processor SEC cartridges. The baseboard provides two SEC/SECC2 cartridge connectors. Processors and Slot 1 connectors are keyed to ensure proper orientation.

1.18.2. Processor Heat/Fan Sinks

The N440BX Server baseboard is not dependent on having fansinks. The term "fansinks" comes from the fan assembly that attaches to the SEC cartridge. The use of the fansink is not required, unless the thermal characteristics of the chassis require extra cooling. For the proper cooling of the processor please refer to the Pentium II processor and Pentium III processor specifications.

1.19. Processor Bus Termination/Regulation/Power

The termination circuitry required by the Pentium II processor/Pentium III processor bus (GTL+) signaling environment and the circuitry to set the GTL+ reference voltage, are implemented directly on the SEC or SECC2 cartridges. The baseboard provides 1.5V GTL+ termination power (VTT), and VRM 8.1-compliant DC-to-DC converters to provide processor power (VCCP) at each connector. Power for primary processor is derived from the +12V supply, and the secondary processor utilizes the +5V supply using an embedded DC-DC converter onboard. Both VRM's are on the baseboard.

1.20. Termination Card

Logic is provided on the baseboard to detect the presence and identity of installed processor or termination cards. If only one Pentium II processor or Pentium III processor is installed in a system, a termination card ***must*** be installed in the vacant SEC connector to ensure reliable system operation. The termination card contains GTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector.

The board will not boot if a termination card is not installed in the vacant slot.

1.21. Functional Architecture

The following diagram illustrates the functional architecture of the N440BX Server baseboard, with dotted lines showing major functional blocks. This chapter describes the operation of each block and associated circuitry. In addition, this chapter provides high level descriptions of functionality distributed between functional blocks (e.g., interrupt structure, clocks, resets, and server management).

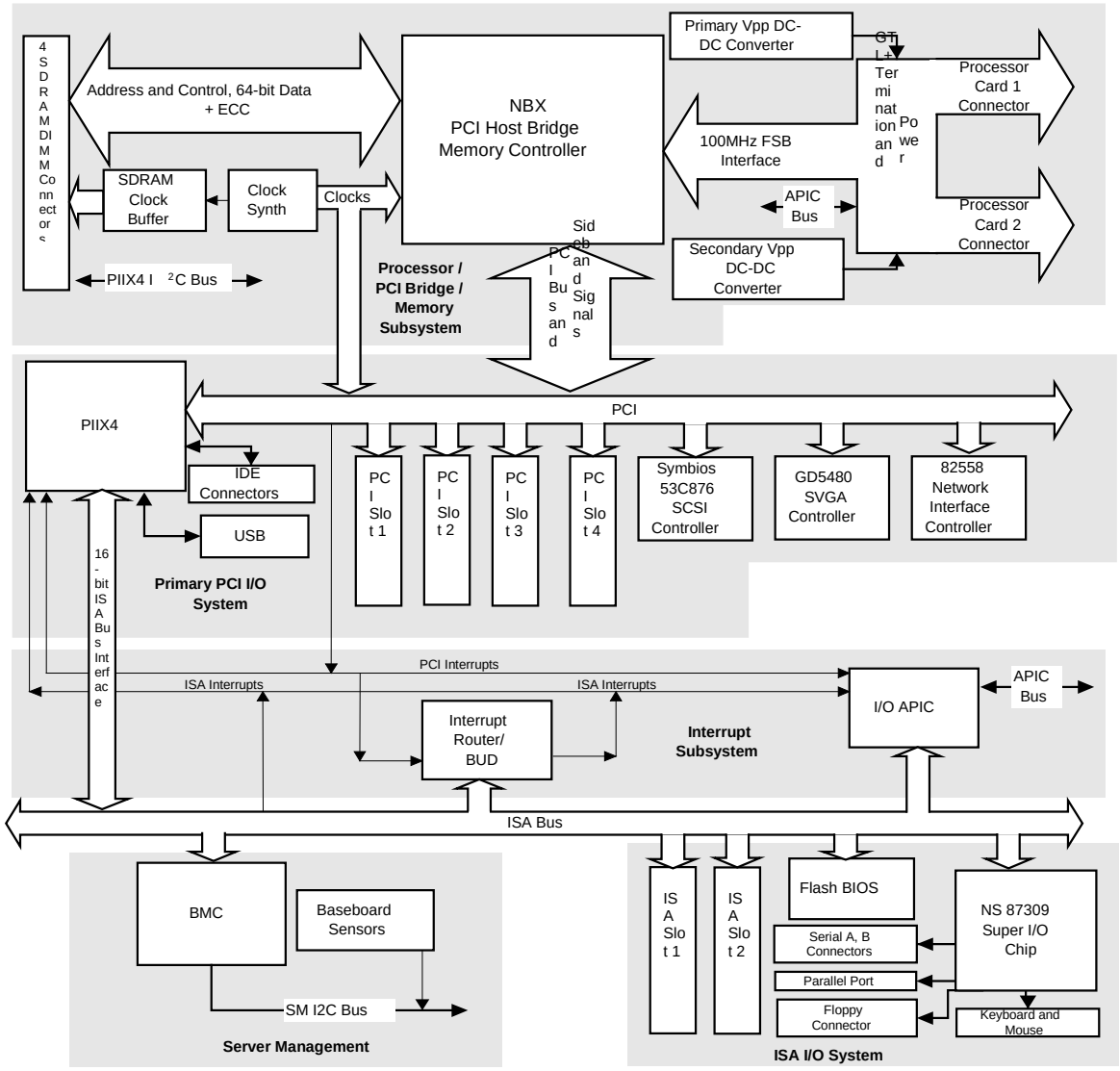


Figure 1.21 N440BX Server Baseboard Functional Blocks

1.22. Processor/PCI Host Bridge/Memory Subsystem

The processor/PCI bridge/memory subsystem consists of support for one to two identical Pentium® II processor or Pentium® III processor cartridges, and up to four SDRAM DIMMs. This support circuitry on the baseboard consists of the following:

- Intel 440BX (NBX) PCI host bridge, memory, and power management[2] controller chip.
- Dual 100MHz system bus Slot 1 edge connectors that accept identical processor cards (if using 1 processor, a GTL+ terminator card goes in the empty slot).
- Four 168-pin DIMM connectors for interface to SDRAM memory.
- Processor host bus GTL+ support circuitry, including termination power supply.
- Embedded DC-to-DC voltage converters for processor power.
- APIC bus.
- Miscellaneous logic for reset configuration, processor card presence detection, and ITP port.

1.22.1. N440BX Host Bridge

The NBX is a BGA device with a 3.3V core and mixed 5V, 3.3V, and GTL+ signal interface pins. The PCI host bridge in the NBX provides the sole pathway between processor and I/O systems, performing control signal translations and managing the data path in transactions with PCI resources onboard. This includes translation of 64-bit operations in the GTL+ signaling environment at 100MHz, to a 32-bit PCI Rev. 2.1 compliant, 5V signaling environment at *33MHz*. The NBX also handles arbitration for PCI bus master access. For more information on N440BX Server arbitration specifics, refer to "PCI Arbitration" later in this chapter. Although the NBX is capable of being clocked to operate with multiple processor system bus frequencies, on N440BX Server the host bridge only supports a 100MHz system bus. The device also features 32-bit addressing (not 36-bit), 4 or 1 deep in-order and request queue (IOQ), dynamic deferred transaction support, and Desktop Optimized (DTO) GTL bus driver support (gated transceivers for reduced power operation). The PCI interface provides greater than 100 MB/s data streamlining for PCI to SDRAM accesses (120 MB/s for writes), while supporting concurrent processor host bus and PCI transactions to main memory. This is accomplished using extensive data buffering, with processor-to-SDRAM and PCI-to-SDRAM write data buffering and write-combining support for processor-to-PCI burst writes.

1.22.2. N440BX Memory Controller

The N440BX performs the function of memory controller for N440BX Server. Total memory of 32MB to 256MB per DIMM is supported. Although the memory controller supports a variety of memory devices, the N440BX Server implementation only supports PC/100 compliant, 72-bit, unbuffered or registered SDRAM DIMMs. For complete information on supported devices, refer to the *PC/100 SDRAM Specification*, *4-Clock 100MHz 64-bit and 72-bit Unbuffered SDRAM DIMM*, and *4-Clock 100MHz 64-bit and 72-bit Unbuffered SDRAM DIMM* documents.

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[2] Refer to "Power Management" later in this chapter, for information on how NBX and PIIX4 power management features are used on N440BX Server.

The N440BX provides ECC that can detect and correct single-bit errors (SED/SEC), and detect all double-bit and some multiple-bit errors (DED). Parity checking and ECC can be configured under software control; higher performance is possible if ECC is disabled (1 clock savings). At initial power-up, ECC and parity checking are disabled.

1.22.3. SDRAM Memory DIMM Sites

N440BX Server provides 4 connectors that accept 168-pin JEDEC, 3.3V, 72-bit unbuffered or registered SDRAM DIMMs. You cannot use EDO DIMMs, only SDRAM DIMMs are allowed. You can mix various sizes of DIMMs, mixing unbuffered and registered DIMMs is not allowed. Best performance is obtained using unbuffered DIMMs. Registered DIMMs stack memory devices on each DIMM for greater memory capacity, but they require additional time (1 clock) for memory accesses.

⚠ CAUTION, single-processor configurations

If you install only one processor in a system, it must go in the primary connector (closest to the DIMM sockets and the center of the server board). With a single-processor configuration, you must install a termination board and termination latch assembly in the empty secondary connector (closest to the edge of the server board) to ensure proper operation of your system. A termination board is provided with the N440BX server board.

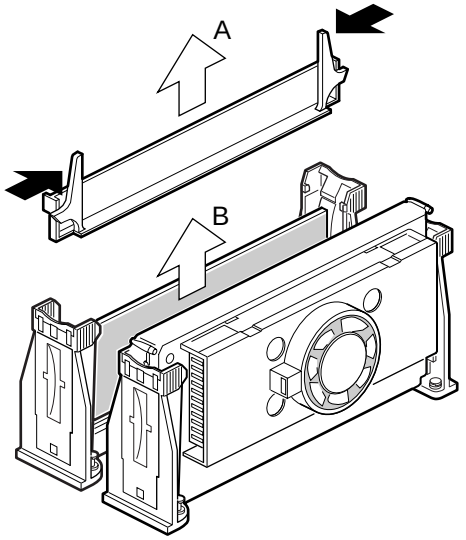

Figure 1.23 N440BX Server Baseboard Termination Card

1.23. APIC Bus

Interrupt notification and generation for the dual processors is done using an independent path between local APICs in each processor and the Intel I/O APIC located on the baseboard. This simple bus consists of 2 data signals and one clock line. PC-compatible interrupt handling is done by the PIIX4, with all interrupts delivered to the processor via the INTR line. However, reduced interrupt latency is possible when the APIC bus delivers interrupts in uni-processor operation (if supported by the OS).

1.24. Miscellaneous Processor/Memory Subsystem Circuitry

In addition to the circuitry described above, the processor subsystem contains the following:

- Processor core frequency configuration circuitry
- DIMM presence detection and auto-configuration logic
- Processor card presence detection circuitry
- ITP port for boundary scan support.

1.25. Processor Core Frequency and Memory Configuration Logic

The PIIX4 provides an independent IMB segment, the PIIX4 System Management Bus (PIIX4 SMB), supporting an IMB EEMUX device (PCF8550) for configuration of processor core speed. The PIIX4 IMB segment also provides access to information stored in IMB ROMs on installed DIMMs, and control of the SDRAM clock buffer that gates synchronous clocks to each DIMM. This feature allows a defective DIMM to be disabled, and total memory resized automatically. BIOS code controls these features using IMB operations performed by the PIIX4. Refer to “Server Management”, for a description of the other two IMB segments on N440BX Server, and information on how the PIIX4 SMB fits into the overall server management scheme.

1.26 Processor Card Presence Detection

Logic is provided on the baseboard to detect the presence and identity of installed processor or termination cards. A termination card *must* be installed in a vacant processor card slot to ensure reliable system operation. If the logic senses an empty connector, the system will not power up, preventing operation of the system with an improperly terminated GTL+ processor bus.

1.27. PCI I/O Subsystem

All I/O for N440BX Server, including PCI and PC-compatible, is directed through the PCI interface. On N440BX Server, the PCI bus supports the following embedded devices and connectors:

- Four 120-pin, 32-bit, 5 Volt, PCI expansion slot connectors, one is Intelligent I/O (I^2O) ready
- PIIX4 PCI-to-ISA bridge / IDE / USB / Power Management (and PIIX4 SMB) controller
- PCI video controller, Cirrus Logic CL-GD5480
- PCI Ultra SCSI Controller, Symbios Logic SYM53C876
- PCI Network Interface Controller, Intel 82558

Each device under the PCI host bridge has its IDSEL signal connected to one bit out of the PCI Address/Data lines AD[31::11], which acts as a device select on the PCI bus. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached, along with its corresponding device number.

Table 3-1. PCI Configuration IDs

IDSEL Value	Device
22	PCI Slot 1
23	PCI Slot 2
24	SCSI
25	PCI Slot 3
26	NIC
27	PCI Slot 4
29	PIIX4
31	Video

1.28. PCI Arbitration

The N440BX Server PCI bus supports 8 PCI masters: NIC, PCI slots 1 through 4, SCSI, PIIX4, and NBX (video is always a slave). All PCI masters must arbitrate for PCI access, using resources supplied by both NBX and custom arbitration logic. The NBX uses internal arbitration connections within its host interface, and the PCI interface on the NBX provides 5 REQ_L/GNT_L pairs for external devices or bridges. Logic in the BUD, which is attached to the REQ0_L/GNT0_L signals, provides support for an additional master on "Round Robin" basis.

One of the arbitration extensions goes to the SCSI controller, which contains an internal arbiter for bus master access to each SCSI interface (wide and narrow).

The PIIX4 operates with a private arbitration scheme using the NBX P_PHOLD_L / P_PHOLDA_L signals, so that access time capability for ISA masters is guaranteed.

The following table defines the arbitration connections on the N440BX Server:

Table 3-2. PCI Arbitration Connections

Baseboard Signals	Device
P_PHOLD_L/P_PHLDA_L	PIIX4
P_REQ1_L/P_GNT1_L	PCI Slot 2
P_REQ2_L/P_GNT2_L	PCI Slot 3
P_REQ3_L/P_GNT3_L	PCI Slot 4
P_REQ4_L/P_GNT4_L	NIC
S_REQ0A_L/S_GNT0A_L	PCI Slot 1
S_REQ0B_L/S_GNT0B_L	SCSI

1.28.1. PCI Connectors

Pins are numbered with respect to the module edge connector: B side signals appear on the front (component side) of the expansion board, A side on the back. Signals that are not connected are labeled with the signal mnemonic followed by "(nc)".

1.28.2. RAID-upgradeable PCI Slot

The N440BX Server provides support in PCI slot 3 for an I^2O RAID controller by AMI. This PCI add-in card utilizes the onboard SCSI controller chip along with its own built-in intelligence to provide a complete I^2O RAID controller subsystem onboard. N440BX Server interrupt structure is designed to allow the AMI RAID card to intercept PCI interrupts from the onboard SCSI chip when this card is installed in slot 3. If no RAID card is installed, the interrupts pass through the PCI interrupt swizzle on N440BX Server. Refer to

"Interrupts and I/O APIC" later in this chapter for more information on N440BX Server interrupt structure. Refer to the AMI Web site for details on the RAID card.

1.28.3. PCI Bus Termination

Certain PCI signals on N440BX Server have "functional" termination, i.e., either pull-up or pull-down resistors. In addition, certain PCI signals may require additional termination to meet signal quality requirements. These are driven through the board topology definition and simulation process, and are not specified in this document. The table in the appendix describes functional termination for PCI signals on N440BX Server. ACK64_L, PRSNT1_L, PRSNT2_L, REQ_L, REQ64_L, SBO_L, SDONE, and TRST_L are terminated at each PCI device and slot. All other signals listed in the table below are bussed, and require only a single pull-up or pull-down resistor. This also applies to the boundary scan signals TCK, TDI, and TMS which are unused in the system (TDO is unterminated).

The N440BX Server implementation of TRST_L does not follow the PCI guideline, but instead implements a more robust solution by providing individual pull-down resistors for each slot. This is done to compensate for numerous PCI components that violate the PCI input low leakage current (I_{il}) specification. If an add-in card directly connects the TRST_L pin on one of these components to the PCI connector, the system would not work with that card installed if the TRST_L signals were bussed and the standard pull-down guideline were used.

SBO_L and SDONE are unused on N440BX Server, but have separate pull-up resistors for each slot per the PCI specification. PRSNT1_L and PRSNT2_L are also not used, and are terminated on each connector with 0.1µF caps to ground on each slot. ACK64_L and REQ64_L have pull-up resistors since 64-bit PCI is not supported on N440BX Server. REQ_L for each slot also has a separate pull-up resistor since these signals are not bussed. Note that REQ_L from onboard PCI components do not require pull-up resistors since they are always driven.

1.29. PIIX4

The PIIX4 is a multi-function PCI device, providing four PCI functions in a single package: PCI-to-ISA bridge, PCI IDE interface, PCI USB controller, and power management controller. Each function within the PIIX4 has its own set of configuration registers and once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface. Refer to "Accessing Configuration Space" for more information on programming configuration space for multi-function devices.

The PIIX4 on N440BX Server primary role is to provide the gateway to all PC-compatible I/O devices and features. N440BX Server uses the following PIIX4 features:

- PCI interface
- ISA bus interface
- Dual IDE interfaces
- Power management control
- System reset control
- ISA-compatible interrupt control
- PC-compatible timer/counters and DMA controllers
- Baseboard plug-n-play support

- General purpose I/O
- Real-time Clock and CMOS configuration RAM.

Following are descriptions of each supported PIIX4 feature on the N440BX Server, and related connector pinouts.

1.29.1. PIIX4 PCI Interface

The PIIX4 fully implements a 32-bit PCI master/slave interface, in accordance with the *PCI Local Bus Specification, Rev. 2.1*. On the N440BX Server, the PCI interface operates at 33 MHz, using a 5V signaling environment.

1.29.2. ISA Interface

Function 0 in the PIIX4 provides an ISA bus interface, operating at 8.33 MHz, that supports two ISA expansion connectors, Flash memory, server management interface, and the SuperI/O chip (PC87309VLJ). Refer to “ISA I/O Subsystem”, later in this chapter, for more information.

1.29.3. PCI Bus Master IDE Interface

Function 1 in the PIIX4 provides a PCI bus master controller for dual IDE channels, each capable of programmed I/O (PIO) operation for transfer rates up to 14 MB/s, and Ultra DMA operation for transfer rates up to 33 MB/s. Each IDE channel supports two drives (0 and 1). Two IDE connectors, each featuring 40 pins (2 x 20), are provided on the baseboard, pinout is specified in the appendix. Unused signals are labeled with the signal mnemonic followed by the N440BX Server implementation in parentheses: “p/u” = pull-up resistor, “nc” = no connection.

1.29.4. Power Management Controller

One of the embedded functions in the PIIX4 is a power management controller. On N440BX Server, power management features are obtained using ACPI-compatible software control. For a complete discussion of power management architecture on N440BX Server, refer to “Power Management” later in this chapter.

1.29.5. Compatibility Interrupt Control

The PIIX4 provides the functionality of two 82C59 PIC devices, for ISA-compatible interrupt handling. For a complete discussion of interrupt handling on N440BX Server, refer to “Interrupts and I/O APIC” later in this chapter.

1.29.6. Real-time Clock

The PIIX4 contains an MC14681A compatible real-time clock with battery backup from an external battery. The device also contains 242 bytes of general purpose battery backed CMOS system configuration RAM. On N440BX Server, these functions are duplicated in the SuperI/O chip. However, the N440BX Server implementation uses the PIIX4 RTC and CMOS facilities.

1.29.7. General Purpose Input and Output Pins

The PIIX4 provides a number of general purpose input and output pins. Some of the pins are multiplexed with specific signals and are unavailable as GPIOs, and some perform dedicated GPIO functions on N440BX Server, as shown in the following table.

Table 3-3. PIIX4 General Purpose Input/Output Pin Assignments

Signal	Name	Description
GPI0	IOCHK_L	Monitors ISA IOCHK_L.
GPI1	PCI_PME_L	Pulled up to 3V_standby with 1KΩ. Connected to PCI conn. pin A19
GPI2	EEMUX_OVERRIDE_L	Jumper indicates whether processor core speed is set via the SMB (high) or fixed at 200MHz (low). Normally high via 10KΩ pullup to VCC3.
GPI3	PSWRD_CLR_L	State of password clear jumper.
GPI4	CMOS_CLR_L	State of CMOS clear jumper.
GPI5	APICREQ_L	Used as APICREQ_L.
GPI6	IRQ8_L	Used as IRQ8_L.
GPI7	CPU0_TTL_VID0	Monitors VID bit 0 for VRM attached to processor 0.
GPI8	PX4_THRM_L	Connects with BMC for thermal monitoring.
GPI9	Unused	Pulled up to 3V standby with 10KΩ. Available - battery low feature not used.
GPI10	ACPI_ACI_L	Monitors BMC output for server management.
GPI11	Unused	Pulled up to 3V standby with 10KΩ. Available - SMBALERT feature not used.
GPI12	PWR_CNTL_NIC	Monitors NIC power state.
GPI13	CPU0_TTL_VID1	Monitors VID bit 1 for VRM attached to processor 0.
GPI14	CPU0_TTL_VID2	Monitors VID bit 2 for VRM attached to processor 0.
GPI15	CPU0_TTL_VID3	Monitors VID bit 3 for VRM attached to processor 0.
GPI16	CPU0_TTL_VID4	Monitors VID bit 4 for VRM attached to processor 0.
GPI17	CPU1_TTL_VID0	Monitors VID bit 0 for VRM attached to processor 1.
GPI18	CPU1_TTL_VID1	Monitors VID bit 1 for VRM attached to processor 1.
GPI19	CPU1_TTL_VID2	Monitors VID bit 2 for VRM attached to processor 1.
GPI20	CPU1_TTL_VID3	Monitors VID bit 3 for VRM attached to processor 1.
GPI21	CPU1_TTL_VID4	Monitors VID bit 4 for VRM attached to processor 1.
GPO0	FRB_TIMER_HALT_L	Stops FRB timer.

Table 3-4. PIIX4 General Purpose (con't)

Signal	Name	Description
GPO1	LA17	Implements this signal. Not Available as GPO.
GPO2	LA18	Implements this signal. Not Available as GPO.
GPO3	LA19	Implements this signal. Not Available as GPO.
GPO4	LA20	Implements this signal. Not Available as GPO.
GPO5	LA21	Implements this signal. Not Available as GPO.
GPO6	LA22	Implements this signal. Not Available as GPO.
GPO7	LA23	Implements this signal. Not Available as GPO.
GPO8	F_SERR_L	Causes BUD to assert SERR_L.
GPO9	EN_SLOT_IRQ9	Selects source for IRQ9 assertion. High = PCI slot, low = PIIX4 GPO29.
GPO10	EEMUX_WP	Implements WP signal to IMB EEMUX for processor core speed control.
GPO11	Not connected	Available as GPO.
GPO12	APICACK_L	Implements this signal. Not Available as GPO.
GPO13	APICCS_L	Implements this signal. Not Available as GPO.
GPO14	IRQ0	Implements this signal. Not Available as GPO.
GPO15	Not connected	Available as GPO.
GPO16	PX4_RTC_PWRDN_L	Causes system to power down.
GPO17	EN_NMI_TO_SMI_L	Causes BUD to route all incoming NMIs to SMI.
GPO18	CLR_SMI	Clears latched SMI source in BUD.

GPO19	EN_NMI	Enables NMI assertion by BUD.
GPO20	Not connected	Available as GPO.
GPO21	SCW_PD_L	SCSI termination power down control.
GPO22	Not connected	Available as GPO.
GPO23	X_OE_L	Implements this signal. Not available as GPO.
GPO24	FLASH_PE_L	Indicates a Flash BIOS programming cycle to the BUD.
GPO25	DIS_NON_FLASH_SMI	Connects with BUD for secure Flash programming (see “Flash ROM BIOS” below).
GPO26	VM_EN_L	Voltage margining control signal.
GPO27	VM_UP_L	Voltage margining control signal.
GPO28	FD_DRATE0	Floppy connector signal.
GPO29	SCI_IRQ9_PIIX4	Generates IRQ9 from PIIX4 if selected by GPO9.
GPO30	SP_EN	Speaker override control.

1.30. SCSI Subsystem

N440BX Server provides an embedded dual-function, PCI SCSI host adapter: Symbios Logic SYM53C876. The SYM53C876 contains two independent SCSI controllers that share a single PCI bus master interface as a multi-function device. Internally, each controller is identical, capable of operations using either 8- or 16-bit SCSI providing 10 MB/s (Fast-10) or 20 MB/s (Fast-20) throughput, or 20 MB/s (Ultra) or 40 MB/s (Ultra-wide). In the N440BX Server implementation, controller (A) attaches to a 68-pin 16-bit (wide) SCSI connector interface, controller (B) attaches to a 50-pin 8-bit (narrow) SCSI connector interface. Each controller has its own set of PCI configuration registers and SCSI I/O registers. As a PCI 2.1 bus master, the SYM53C876 supports burst data transfers on PCI up to the maximum rate of 132 MB/sec using on-chip buffers. Refer to the SYM53C876 PCI-Dual Channel SCSI Multi-Function Controller Data Manual for more information on the internal operation of this device, and descriptions of SCSI I/O registers.

1.30.1. Symbios Logic SYM53C876 PCI Signals

The SYM53C876 supports all of the required 32-bit PCI signals including the PERR_L and SERR_L functions. Full PCI parity is maintained on the entire data path through the chip. The device also takes advantage of PCI interrupt signaling capability, using PCI_INTB_L (for controller A, wide SCSI) and PCI_INTC_L (for controller B, narrow) on the N440BX Server board. Please see the Interupt routing figure. The figure below shows the PCI signals supported by the SYM53C876.

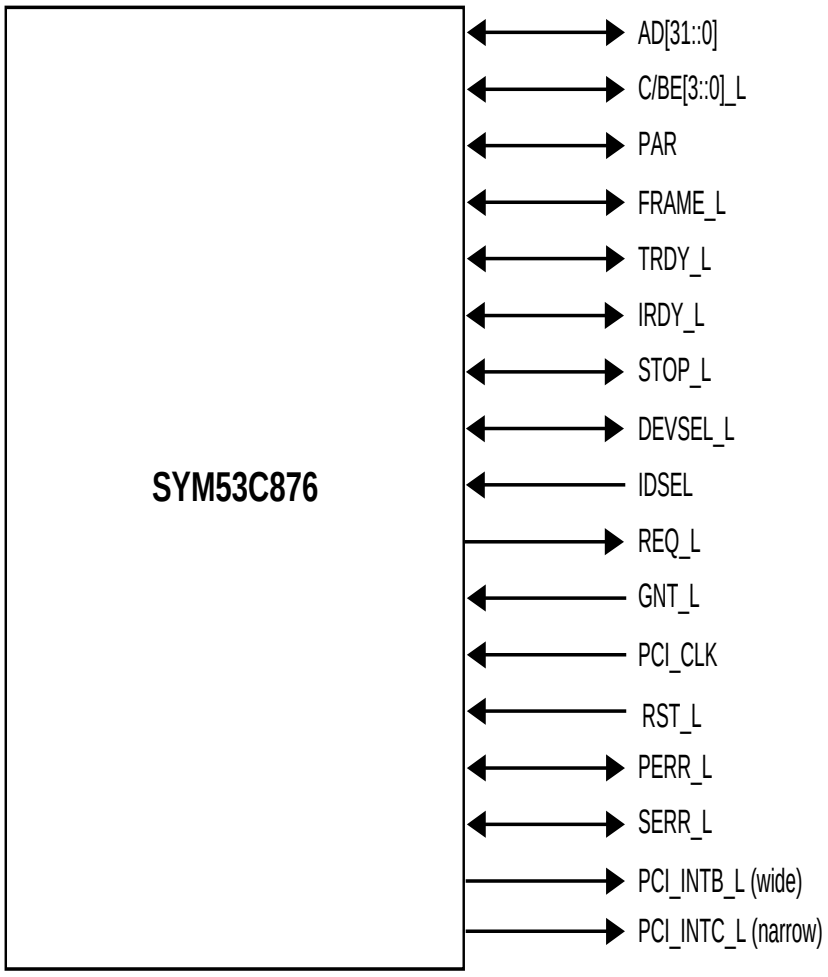

Figure 3-1. Embedded SCSI PCI Signals

1.30.2. SYM53C876 Supported PCI Commands

The SYM53C876 supports PCI commands as shown in the following table:

Table 3-5. Embedded SCSI Supported PCI Commands

C/BE [3::0] _L	Command	SYM53C876 Support	
		Target	Master
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	Yes	Yes
1101	Dual Address Cycle	No	No
1110	Memory Read Line	Yes*	Yes
1111	Memory Write and Invalidate	Yes**	Yes

* Defaults to Memory Read
** Defaults to Memory Write

The extensions to memory commands (memory read multiple, memory read line, and memory write and invalidate) work with the cache line size register to give the cache controller advance knowledge of the minimum amount of data to expect. The decision to use either the memory read line or memory read multiple commands is determined by a bit in the configuration space command register for this device.

1.30.3. SCSI Interfaces

The SYM53C876 contains two independent SCSI controllers: A for Wide SCSI, B for Narrow. Each controller supports 8-bit or 16-bit Fast-10 and Fast-20 SCSI operation at data transfer rates of 10, 20, or 40 MB/s. Each maintains its own set of configuration and run-time registers. On the N440BX Server board, the only difference between each controller is the connector to which it attaches.

Each SCSI interface on the N440BX Server offers active negation outputs, controls for external differential transceivers, a disk activity output, and a SCSI terminator power down control. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus, avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48 mA single-ended SCSI bus with no additional drivers (the SCSI segment can handle up to 15 devices). SCSI termination power is always on, regardless of the register settings for SYM53C876 SCSI termination power control features.

1.30.4. SCSI Bus

The SCSI data bus is 8- or 16-bits wide with odd parity generated per byte. SCSI control signals are the same for either bus width. To accommodate 8-bit devices on the 16-bit Wide SCSI connector, the SYM53C876 assigns the highest arbitration priority to the low byte of the 16-bit word. This way, 16-bit targets can be mixed with 8-bit if the 8-bit devices are placed on the low data byte. For 8-bit mode, the unused high data byte is self-terminated and need not be connected. During chip power down, all inputs are disabled to reduce power consumption. Please see the Appendix for pin outs of the narrow and wide SCSI connectors.

1.31. PCI Video

N440BX Server provides a Cirrus Logic CL-GD5480 video controller, along with video SGRAM and support circuitry for an embedded SVGA video subsystem. The CL-GD5480 64-bit VGA Graphics Accelerator chip contains an SVGA video controller, clock generator, BitBLT engine, and RAMDAC. 256K x 32 SGRAM chips provide 2 MB (factory build option, no socket) of 10ns video memory. The SVGA subsystem supports a variety of modes: up to 1600 x 1200 resolution, and up to 16.7 M colors. It also supports analog VGA monitors, single- and multi-frequency, interlaced and non-interlaced, up to 100 Hz vertical retrace frequency. The N440BX Server board also provides a standard 15 pin VGA connector, and external video blanking logic for server management console redirection support.

1.32. Video Chip PCI Signals

The CL-GD5480 supports a minimal set of 32-bit PCI signals since it never acts as a PCI master. As a PCI slave the device requires no arbitration or interrupt connections.

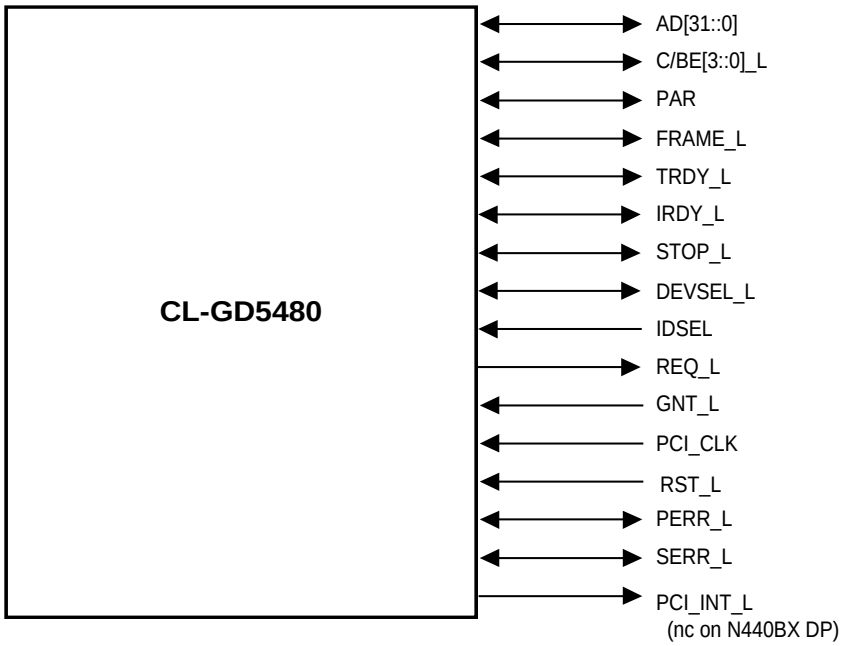

Figure 3-2. Video Controller PCI Signals

1.32.1. Video Controller PCI Commands

The CL-GD5480 supports the following PCI commands:

Table 3-6. Video Chip Supported PCI Commands

		CL-GD5480 Support	
C/BE[3::0]_L	**Command Type**	**Target**	**Master**
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	No
0111	Memory Write	Yes	No
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	No	No
1101	Dual Address Cycle	No	No
1110	Memory Read Line	No	No
1111	Memory Write and Invalidate	No	No

1.32.2. Video Modes

The CL-GD5480 supports all standard IBM VGA modes. Using 2MB (standard) of SGRAM, N440BX Server supports special Cirrus Logic extended modes. The following tables show the standard and extended modes that this implementation supports, including the number of colors and palette size (e.g., 16 colors out of 256 K colors), resolution, pixel frequency, and scan frequencies.

Table 3-7. Standard VGA Modes

Mode(s) in Hex	Colors (number /palette size)	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
0, 1	16/256K	360 X 400	14	31.5	70
2, 3	16/256K	720 X 400	28	31.5	70
4, 5	4/256K	320 X 200	12.5	31.5	70
6	2/256K	640 X 200	25	31.5	70
7	Mono	720 X 400	28	31.5	70
D	16/256K	320 X 200	12.5	31.5	70
E	16/256K	640 X 200	25	31.5	70
F	Mono	640 X 350	25	31.5	70
10	16/256K	640 X 350	25	31.5	70
11	2/256K	640 X 480	25	31.5	60
12	16/256K	640 X 480	25	31.5	60
12+	16/256K	640 X 480	31.5	37.5	75
13	256/256K	320 X 200	12.5	31.5	70

Table 3-8. Extended VGA Modes

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)	Memory Option
58, 6A	16/256K	800 X 600	36	35.2	56	1MB
58, 6A	16/256K	800 X 600	40	37.8	60	1MB
58, 6A	16/256K	800 X 600	50	48.1	72	1MB
58, 6A	16/256K	800 X 600	49.5	46.9	75	1MB
5C	256/256K	800 X 600	36	35.2	56	1MB
5C	256/256K	800 X 600	40	37.9	60	1MB
5C	256/256K	800 X 600	50	48.1	72	1MB
5C	256/256K	800 X 600	49.5	46.9	75	1MB
5C	256/256K	800 X 600	56.25	53.7	85	1MB
5C	256/256K	800 X 600	68.2	63.6	100	1MB
5D	16/256K (interlaced)	1024 X 768	44.9	35.5	43	1MB
5D	16/256K	1024 X 768	65	48.3	60	1MB
5D	16/256K	1024 X 768	75	56	70	1MB
5D	16/256K	1024 X 768	78.7	60	75	1MB
5E	256/256K	640 X 400	25	31.5	70	1MB
5F	256/256K	640 X 480	25	31.5	60	1MB
5F	256/256K	640 X 480	31.5	37.9	72	1MB
5F	256/256K	640 X 480	31.5	37.5	75	1MB
5F	256/256K	640 X 480	36	43.3	85	1MB
5F	256/256K	640 X 480	43.2	50.9	100	1MB
60	256/256K (interlaced)	1024 X 768	44.9	35.5	43	1MB
60	256/256K	1024 X 768	65	48.3	60	1MB
60	256/256K	1024 X 768	75	56	70	1MB
60	256/256K	1024 X 768	78.7	60	75	1MB
60	256/256K	1024 X 768	94.5	68.3	85	1MB
60	256/256K	1024 X 768	113.3	81.4	100	1MB
64	64K	640 X 480	25	31.5	60	1MB
64	64K	640 X 480	31.5	37.9	72	1MB
64	64K	640 X 480	31.5	37.5	75	1MB
64	64K	640 X 480	36	43.3	85	1MB
64	64K	640 X 480	43.2	50.9	100	1MB
65	64K	800 X 600	36	35.2	56	1MB
65	64K	800 X 600	40	37.8	60	1MB
65	64K	800 X 600	50	48.1	72	1MB
65	64K	800 X 600	49.5	46.9	75	1MB
65	64K	800 X 600	56.25	53.7	85	1MB
65	64K	800 X 600	68.2	63.6	100	1MB
66	32K	640 X 480	25	31.5	60	1MB
66	32K	640 X 480	31.5	37.9	72	1MB
66	32K	640 X 480	31.5	37.5	75	1MB
66	32K	640 X 480	36	43.3	85	1MB
66	32K	640 X 480	43.2	50.9	100	1MB
67	32K	800 X 600	36	35.2	56	1MB
67	32K	800 X 600	40	37.8	60	1MB
67	32K	800 X 600	50	48.1	72	1MB
67	32K	800 X 600	49.5	46.9	75	1MB

Table 3-8. Extended VGA Modes (cont.)

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)	Memory Option
67	32K	800 X 600	56.25	53.7	85	1MB
67	32K	800 X 600	68.2	63.6	100	1MB
68	32K (interlaced)	1024 X 768	44.9	35.5	43	2MB
68	32K	1024 X 768	65	48.3	60	2MB
68	32K	1024 X 768	75	56	70	2MB
68	32K	1024 X 768	78.7	60	75	2MB
68	32K	1024 X 768	94.5	68.3	85	2MB
68	32K	1024 X 768	113.3	81.4	100	2MB
6C	16/256K (interlaced)	1280 X 1024	75	48	43	1MB
6D	256/256K (interlaced)	1280 X 1024	75	48	43	2MB
6D	256/256K	1280 X 1024	108	65	60	2MB
6D	256/256K	1280 X 1024	135	80	75	2MB
6D	256/256K	1280 X 1024	157.5	91	85	2MB
6E	32K	1152 X 864	94.5	63.9	70	2MB
6E	32K	1152 X 864	108	67.5	75	2MB
6E	32K	1152 X 864	121.5	76.7	85	2MB
6E	32K	1152 X 864	143.5	91.5	100	2MB
71	16M	640 X 480	25	31.5	60	1MB
71	16M	640 X 480	31.5	37.9	72	1MB
71	16M	640 X 480	31.5	37.5	75	1MB
71	16M	640 X 480	36	43.3	85	1MB
71	16M	640 X 480	43.2	50.9	100	1MB
74	64K (interlaced)	1024 X 768	44.9	35.5	43	2MB
74	64K	1024 X 768	65	48.3	60	2MB
74	64K	1024 X 768	75	56	70	2MB
74	64K	1024 X 768	78.7	60	75	2MB
74	64K	1024 X 768	94.5	68.3	85	2MB
74	64K	1024 X 768	113.3	81.4	100	2MB
78	32K	800 X 600	36	35.2	56	1MB
78	16M	800 X 600	40	37.8	60	2MB
78	16M	800 X 600	50	48.1	72	2MB
78	16M	800 X 600	49.5	46.9	75	2MB
78	16M	800 X 600	56.25	53.7	85	2MB
78	16M	800 X 600	68.2	63.6	100	2MB
7B	256/256K (interlaced)	1600 X 1200	135	62.5	48	2MB
7B	256/256K	1600 X 1200	162	75	60	2MB
7C	256/256K	1152 X 864	94.5	63.9	70	1MB
7C	256/256K	1152 X 864	108	67.5	75	1MB
7C	256/256K	1152 X 864	121.5	76.7	85	1MB
7C	256/256K	1152 X 864	143.5	91.5	100	1MB
7D	64K	1152 X 864	94.5	63.9	70	2MB
7D	64K	1152 X 864	108	67.5	75	2MB
7D	64K	1152 X 864	121.5	76.7	85	2MB
7D	64K	1152 X 864	143.5	91.5	100	2MB

For more information refer to the *Cirrus Logic CL-GD5480 Technical Reference Manual*.

1.33. Network Interface Controller (NIC)

N440BX Server supports a 10BASE-T/100BASE-TX network subsystem based on the Intel 82558 Fast Ethernet PCI Bus Controller. This device is similar in architecture to its predecessor (Intel 82557), except with an integrated physical layer interface. The advantage of this controller is that no external devices are required to implement an embedded network subsystem, except TX/RX magnetics, 2 status LEDs**,** and a connector.

The 82558 is a highly integrated PCI LAN controller for 10 or 100 Mbps Fast Ethernet networks. As a PCI bus master, the 82558 can burst data at up to 132 MB/s. This high-performance bus master interface can eliminate the intermediate copy step in RX/TX frame copies, resulting in faster frame processing. The network OS communicates with the 82558 using a memory-mapped I/O interface, PCI interrupt connected directly to the BUD (Basic Utility Device), and two large receive and transmit FIFOs, which prevent data overruns or under runs while waiting for access to the PCI bus, as well as enabling back to back frame transmission within the minimum 960ns inter-frame spacing. The figure below shows the PCI signals supported by the 82558:

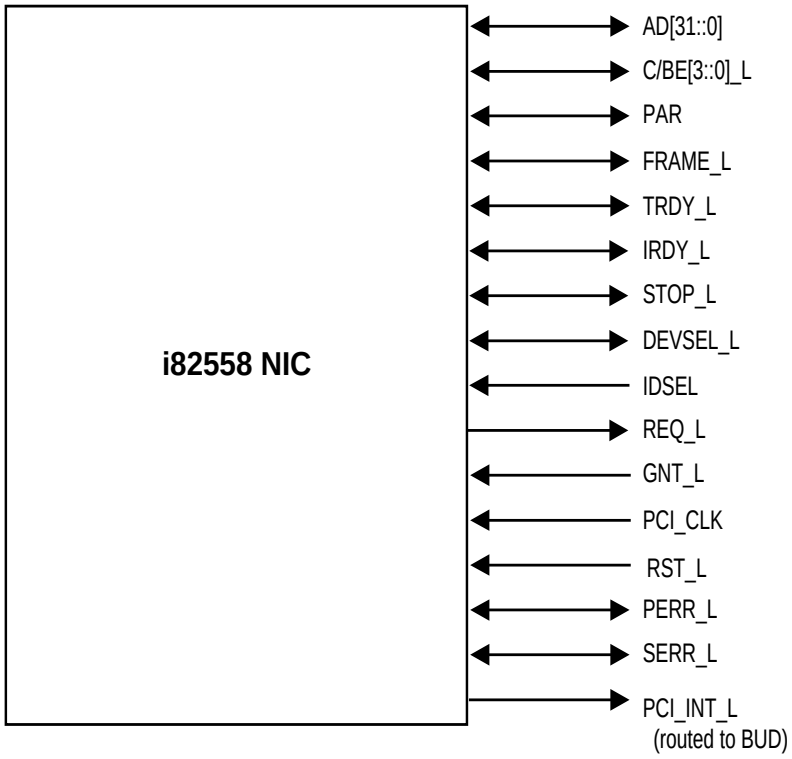

Figure 1-3. Embedded NIC PCI Signals

1.33.1. Supported Network Features

The 82558 contains an IEEE MII compliant interface to the components necessary to implement a IEEE 802.3 100BASE-TX network connection. N440BX Server supports the following features of the 82557 controller:

- Glueless 32-bit PCI Bus Master Interface (Direct Drive of Bus), compatible with PCI Bus Specification, revision 2.1
- 82596-like chained memory structure, with improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- On-chip counters for network management
- Autodetect and autoswitching for 10 or 100 Mbps network speeds
- Support for both 10 Mbps and 100 Mbps Networks, full or half duplex-capable, with back-to-back transmit at 100 Mbps
- Integrated physical interface to TX magnetics.

The magnetics component terminates the 100BASE-TX connector interface. A Flash device stores the network ID.

1.33.2. NIC Connector and Status LEDs

The 82558 drives LEDs on the network interface connector that indicate transmit/receive activity on the LAN, valid link to the LAN, and 10/100 Mbps operation.

1.34. ISA I/O Subsystem

On the N440BX Server, the PIIX4 provides a bridge to an ISA I/O subsystem that supports the following connectors and devices:

- Two ISA slots, one physically shared with PCI slot 1
- Flash memory for BIOS ROM and extensions
- National Semiconductor PC87309VLJ SuperI/O chip, which supports the following:
    - Two PC-compatible serial ports
    - Enhanced parallel port
    - Floppy controller
    - Keyboard/Mouse ports

The ISA I/O subsystem also connects with the Intel I/O APIC and BMC. The I/O APIC relays interrupts produced by ISA devices in dual processor operation (or in uni-processor operation for increased performance with certain OS implementations. The BUD, a programmable logic device performs rerouting of PCI interrupts as ISA interrupts for MP OS implementations that are not fully MPS 1.4 compatible, and management interrupt (NMI_L and SMI_L) control. Refer to “Interrupts and I/O APIC” later in this chapter for more information on these devices and how they are used in the N440BX Server interrupt structure. The BMC controls server management features on N440BX Server. Refer to “Server

Management" later in this chapter for details. For details on pin out and termination please refer to the Appendix.

1.35. Compatibility I/O Controller Subsystem

The National PC87309VLJ SuperI/O device is a plug and play (PnP) compatible standard I/O subsystem chip. This device contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. N440BX Server provides the connector interface for each. In addition, the SuperI/O contains a real-time clock, which is unused on N440BX Server.

Note:

Unlike it predecessor (87307), the PC87309VLJ provides no general purpose I/O bits or programmable chip selects. All GPIOs required by N440BX Server subsystems are supplied by the PIIX4 as specified above.

1.36.1. Serial Ports

Two connectors are provided, one 9-pin D-Sub in the stacked housing for Serial port A, and the second via 10-pin header for Serial port B. Both ports are compatible with 16550A and 16450 UARTs, supporting relocatable I/O addresses. Each serial port can be set to 1 of 4 different COM ports, and can be enabled separately. When enabled, each port can be programmed to generate edge or level sensitive interrupts. When disabled, serial port interrupts are available to add-in cards. The pinout for the two connectors are available in the appendix.

1.36.2. Parallel Port

The 25/15 pin high rise connector stacks the parallel port connector over the VGA and serial Port A connector. The 87309 provides an IEEE 1284-compliant 25-pin bi-directional parallel port. BIOS programming of the SuperI/O registers enable the parallel port, and determine the port address and interrupt. When disabled, the interrupt is available to add-in cards. Pin out of the Parallel port is available in the appendix.

1.36.3. Floppy Disk Controller

The FDC on the SuperI/O is functionally compatible with the PC8477, which contains a superset of the floppy disk controllers in the DP8473 and N82077. The baseboard provides the 24 MHz clock, termination resistors, and chip selects. All other FDC functions are integrated into the SuperI/O, including analog data separator and 16-byte FIFO. Pinout is available in the appendix.

1.36.4. Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single stacked housing. The mouse connector is stacked over the keyboard connector. External to the board they appear as two connectors. The keyboard and mouse controller are software compatible with the 8042AH and PC87911. The keyboard and mouse connectors are PS/2 compatible, with pinout available in the appendix.

1.36.5. Front Panel Header (AT, System)

An inline AT header is provided for AT-style front panel connections, e.g., power, LED indicators, and reset as well has a Front panel 2x16 post socket header. Both pin outs are available in the appendix.

1.36.6. Flash ROM BIOS

An 8Mbit flash memory (Intel 28F008S5) provides non-volatile storage space for BIOS and general purposes. The device is byte wide, of the Smart 5 FlashFile family and symmetrically blocked. The Flash device is directly addressed as 16 64-kbyte blocks of 8-bit ISA memory. Refer to the *Byte-Wide Smart 5 FlashFile Memory Family 4, 8, and 16 MB Data Book* for additional device information.

1.36.7. Secure Flash Programming Mechanism

On N440FX DP, the BUD detects any write operation to Flash and asserts SMI_L. The SMI_L handler (part of BIOS) then looks for a signature from the Flash Memory Update utility (FMUP) before allowing any writes to Flash. This prevents accidental loading of non-compatible BIOS code into Flash.

1.37. System Reset Control

Reset circuitry on the N440BX Server board monitors reset from the front panel, PIIX4, I/O controller, and processor subsystem to determine proper reset sequencing for all types of reset. The reset logic is designed to accommodate a variety of ways to reset the system, which can be divided into the following categories:

- Power-up reset
- Hard reset
- Soft (programmed) reset

1.37.1. Power-up Reset

Power-up reset occurs on the initial application of power to the system. The power supply asserts its "power good" signal within 400 to 2000ms of its output voltages being stable. The BMC monitors this signal, and asserts its power good output 30 to 40ms after detecting the power supply's power good signal asserted (the onboard VRMs are designed to provide stable processor power 30 to 40ms after the main power is stable).

1.37.2. Hard Reset

Hard reset may be initiated by software, or by the user resetting the system through the front panel. For software initiated hard reset, the PIIX4 Reset Control register should be used. The front panel reset is routed to the PIIX4 through the reset and power micro-controller. Both sources of hard reset cause the PIIX4 to assert ISA bus reset (RST_RSTDRV) and PCI reset (RST_P_RST_LB). RST_RSTDRV resets the ISA subsystem, while RST_P_RST_L resets the PCI bus. The NBX receives the PCI reset signal and propagates it to the processor subsystem

1.37.3. Soft Reset

Soft resets may be generated by the keyboard controller (RST_KB_L), or by the chip set in the processor subsection (RST_INIT_REQ_L). The two sources of soft reset are combined in the reset logic, and routed to the processor subsection via the RST_INIT_CPU_L signal. Soft reset causes the processors to begin execution in a known state without flushing caches or internal buffers.

A programmed reset may be initiated by software. Although reset control is provided by registers in the NBX, the chip's documentation recommends that the PIIX4 Reset Control register be used instead for programmed resets.

1.37.4. Reset Diagram

Reset flows throughout the N440BX Server board as shown in the following figure.

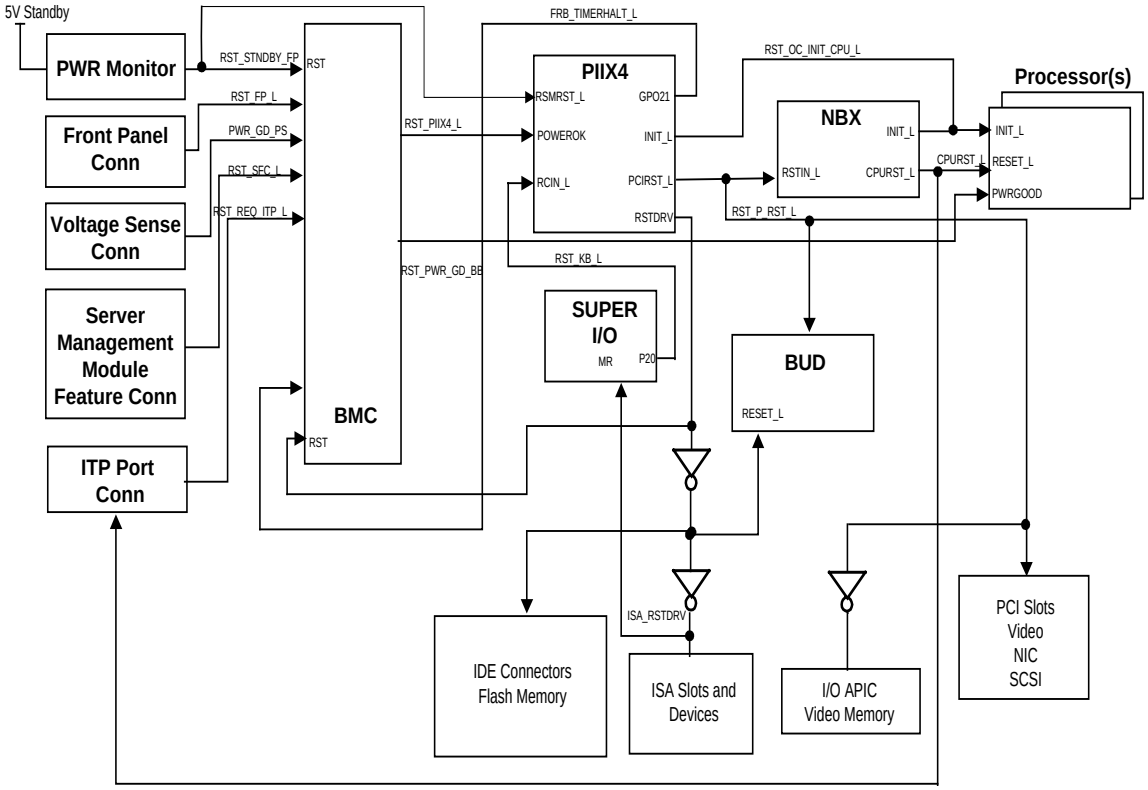

Figure 3-4. Reset Flow Diagram

1.38. Clock Generation and Distribution

All buses on N440BX Server operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 100 MHz at 2.5V logic levels - Both Slot 1 connectors, the NBX, the ITP port
- 100 MHz at 3.3V logic levels - SDRAM DIMMs
- 33.3 MHz at 3.3V logic levels - Reference clock for the PCI bus clock driver
- 14.31818 MHz at 2.5V logic levels - Processor and I/O APIC bus clock

There are 4 main synchronous clock sources on the N440BX Server board: 100MHz host clock generator for processors and SDRAM, 48 MHz clock for PIIX4 and SuperI/O chips, 33.3 MHz PCI reference clock, and 14.318 MHz APIC and ISA clocks. For information on processor/SDRAM clock generation, refer to the *Mixed Voltage Clock Synthesizer/Driver Specification with SDRAM Support*. In addition, N440BX Server provides asynchronous clock generators: 40 MHz clock for the embedded SCSI controller, 32 KHz clock for the PIIX4 RTC, 22.1 MHz clock for the BMC, and a 25 MHz clock for the NIC. The following figure illustrates clock generation and distribution on the N440BX Server board.

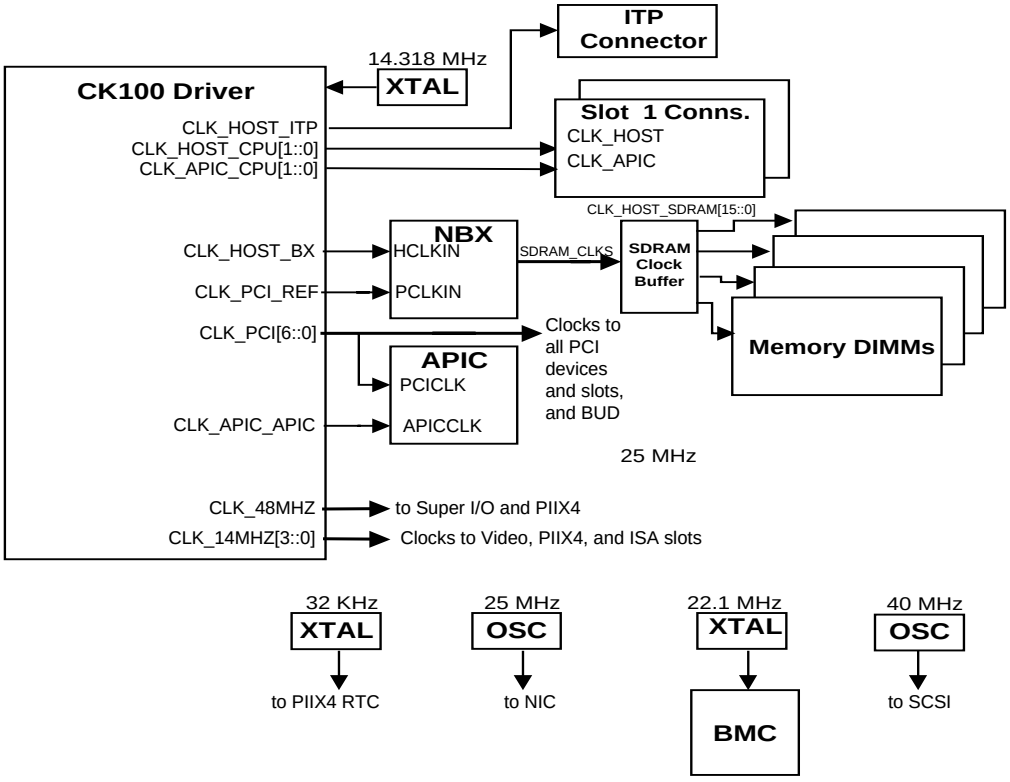

Figure 3-5. Clock Generation and Distribution

1.39. Interrupts and I/O APIC

N440BX Server interrupt architecture accommodates both PC-compatible PIC mode, and dual-processor APIC mode interrupts. In addition, N440BX Server provides a PCI to ISA interrupt rerouting mechanism for compatibility with some multiprocessor operating systems which do not fully support the APIC.

1.39.1. PIIX4 Compatibility Interrupt Controller

For PC-compatible mode, the PIIX4 provides two 82C59-compatible interrupt controllers embedded in the device. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The PIIX4 and SuperI/O contain configuration registers that define which interrupt source logically maps to I/O APIC INTx pins. In PIC mode, the PIIX4 provides a way to direct PCI interrupts onto one of the interrupt request levels 1-15. Note that this is only useful in compatibility mode since the redirected interrupts are not sourced on the outputs of the PIIX4.

1.39.2. Intel I/O APIC

For APIC mode, the N440BX Server interrupt architecture incorporates the Intel I/O APIC device, to manage and broadcast interrupts to local APICs in each processor. The I/O APIC monitors interrupt requests from devices, and on occurrence of an interrupt sends a message corresponding to the interrupt via the APIC bus to each local APIC. The APIC bus minimizes interrupt latency time for compatibility interrupt sources, in both single and dual processor operation. The I/O APIC can also supply greater than 16 interrupt levels to the processor(s). The APIC bus consists of an APIC clock, and two bi-directional data lines.

N440BX Server APIC structure consists of a single I/O APIC device with 24 input interrupt requests. Compatibility interrupt levels 0 through 15 appear on inputs 0 through 15. The I/O APIC also manages 8 interrupt levels associated with PCI interrupts: PCI interrupts A through D are routed to APIC inputs 16 through 19. This supports more efficient interrupt processing. The PIIX4 also contains I/O APIC features that are not used in the N440BX Server platform.

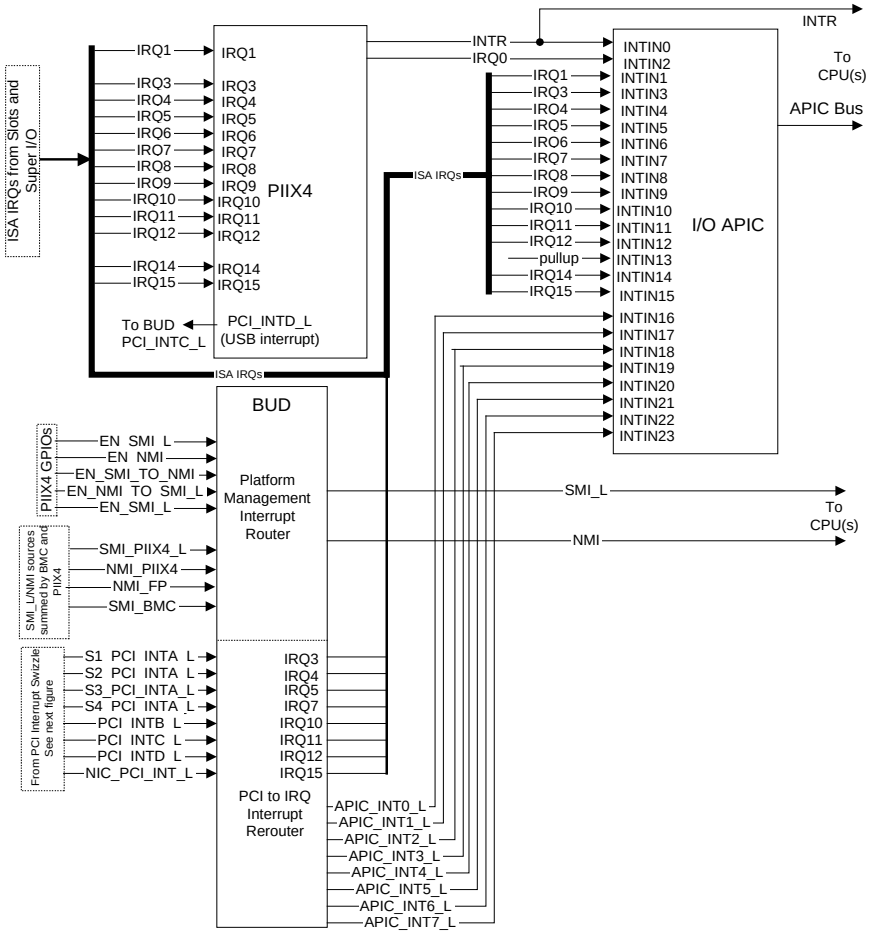

Figure 3-6. Interrupt Structure

1.40. Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on N440BX Server. The actual interrupt map is defined using configuration registers in the PIIX4 and the I/O controller, and PCI to IRQ interrupt rerouter in the BUD. I/O Redirection Registers in the I/O APIC are provided for each interrupt signal, which define hardware interrupt signal characteristics for APIC messages sent to local APIC(s). Use the information provided in this table to determine how to program each interrupt.

Table 3-9. Interrupt Definitions

Interrupt	I/O APIC level	Description
INTR	INT0	Processor interrupt
NMI		NMI from BUD to processor
IRQ0	INT2	Timer interrupt from PIIX4
IRQ1	INT1	Keyboard interrupt
IRQ2		Interrupt signal from second 8259 internal to PIIX4
IRQ3	INT3	Serial port A or B interrupts from 87309VLJ device, user-configurable.
IRQ4	INT4	Serial port A or B interrupts from 87309VLJ device, user-configurable.
IRQ5	INT5	
IRQ6	INT6	Floppy disk
IRQ7	INT7	Parallel port
IRQ8_L	INT8	RTC interrupt
IRQ9	INT9	
IRQ10	INT10	
IRQ11	INT11	
IRQ12	INT12	Mouse interrupt
	INT13	
IRQ14	INT14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1
IRQ15	INT15	Secondary IDE interrupt
PCI_INTA_L	INT16	PCI Interrupt signal A
PCI_INTB_L	INT17	PCI Interrupt signal B
PCI_INTC_L	INT18	PCI Interrupt signal C
PCI_INTD_L	INT19	PCI Interrupt signal D
SMI_L		System Management Interrupt. General-purpose error indicator from various sources. Controlled by BUD.

1.40.1. PCI Add-in Card Slot Interrupt Sharing

The following figure shows how PCI interrupts, shared between slots and embedded controllers, are routed to the BUD. The BUD manages each PCI_INT_A from each slot, cascaded PCI_INTs B through C from each slot, and PCI interrupts from SCSI and NIC devices, to avoid conflicts (since most PCI cards use PCI_INTA_L as their interrupt pin). The arrows indicate the direction of interrupt flow from slot to slot, with final destination at the BUD interrupt inputs. The BUD then delivers each interrupt to the appropriate PIIX4 compatibility IRQ and I/O APIC INTIN pins.

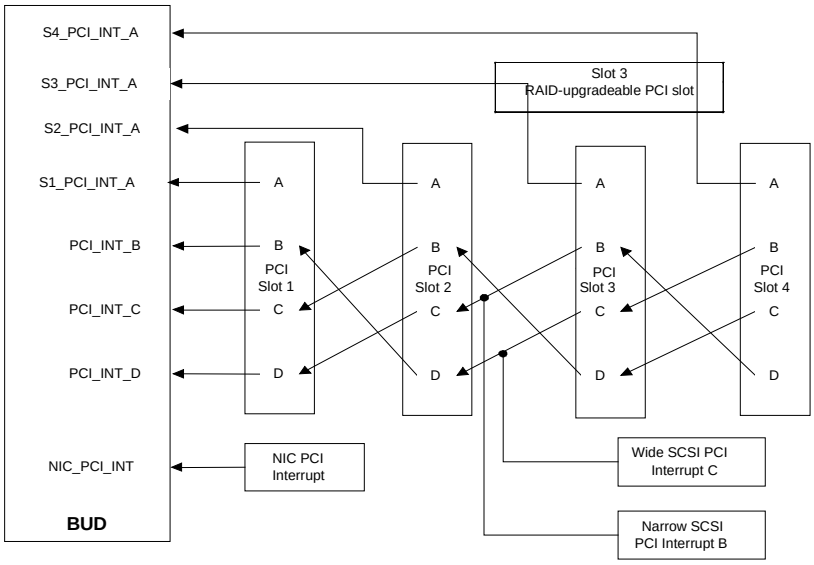

Figure 3-7. PCI Slot Interrupt Swizzle

1.40.2. PCI Interrupt Rerouting

Some multiprocessor operating systems are unable to handle interrupts from PCI slots and devices as pure PCI interrupts, via inputs 16-19 (allocated to PCI) of the I/O APIC. Rather, they expect PCI interrupts to be delivered as ISA IRQs. Multiprocessor operating systems may also expect some interrupts from the PC-compatible PIC in the PIIX4, and others from the I/O APIC (Mixed Mode). Some device drivers check whether the device uses one of the traditional IRQs, and if not (when the PCI interrupt is connected directly to the I/O APIC), the driver fails to install or run properly. The PIIX4 performs internal PCI to IRQ interrupt steering so that PCI interrupts can be delivered to the PIC. However, the PCI interrupt steering feature is unidirectional, which means that it cannot redirect PCI interrupts to the I/O APIC.

For these reasons, N440BX Server incorporates an external PCI to IRQ rerouter circuit in the BUD, that can be programmed to pass PCI interrupts through to inputs 16-19 of the I/O APIC, or deliver a specific PCI interrupt to an ISA IRQ. Under software control, a PCI interrupt can be individually rerouted to an ISA IRQ signal. This functionality is contained in the BUD.

Two 8-bit registers are provided in the rerouter circuit, with each nibble of a register controlling a specific PCI Interrupt line via PIO commands. The PIIX4 decodes the address of the PIO command and produces a chip select, which is controlled using the PIIX4 Programmable Chip Select Control register (78h - 79h). The rerouter uses only 2 bytes of the minimum 4 selectable, so aliases are provided. Refer to “PCI Interrupt to IRQ Routing Control” for run-time programming information. Refer to PIIX4 Programmable Chip Select Control register description for initialization-time requirements.

1.40.3. Working with PCI Interrupts

The N440BX DP Server baseboard shares PCI bus resources with onboard devices. The list below gives some guidelines to reduce the possibility of conflicts and performance restrictions.

1) Try to stay away from installing a LAN adapter in Slot 3. Either the configuration may not work or it may reduce the performance quality on the network. If the server needs an additional LAN adapter, install it in Slot 1 or 2 and this will allow for maximum throughput. Slot 4 could have the same results as Slot 3 and should not be used if possible

2) When configuring a RAID controller in the N440BX Server baseboard, Slots 1 and 2 are better for performance and configuration. This is due to the onboard resources that are being used. Another consideration is to have this RAID pack as the boot device. (Refer to Table 14 Boot Order.)

When integrating peripherals into a server system, taking into consideration the architecture of the PCI bus and the onboard resources can help in making the right choices and offering a reliable server.

1.41. Boot Order

The baseboard boot order for non-multi-boot cards is outlined in the following table. On the N440BX Server baseboard multi-boot cards will always sign-on ahead of all other cards and onboard SCSI.

Table 1 Boot Order

Order	Boot Device
1	Onboard IDE
2	Onboard SCSI
3	PCI Slot 1
4	PCI Slot 2
5	PCI Slot 3
6	PCI Slot 4

1.42. System Management Interrupt Handling

N440BX Server is designed to report these types of system errors: ISA bus, PCI bus, ECC memory, and System limit. Errors are reported by the BMC and PIIX4 using SMI_L. SMI is used for server management and advanced error processing. All errors can be intercepted by SMI for preprocessing (if SMI_L is enabled), or handled directly by NMI handlers. Some errors have to generate an NMI even if they are intercepted by the SMI, because the traditional way to handle errors in PC architecture is via the NMI. NMI/SMI handling logic in the BUD emulates non-ISA errors as ISA-compatible using NMI and SMI_L.

1.43. Basic Utility Device (BUD)

In addition to the PCI arbitration and interrupt rerouting functions described above, the BUD also gates and redirects SMI_L and NMI to generate SERR_L, and performs other miscellaneous logic

functions (e.g., PCI arbitration expansion). The BUD contains an I/O mapped ISA interface for control of PCI-to-IRQ interrupt rerouting. Functional specifications for BUD signal pins are given in the following table.

Table 3-10. BUD Signal Descriptions

Signal	Pin	Type *	Description
AD0	92	I	Driven by ISA address bit SA0.
AD1	93	I	Driven by ISA address bit SA1.
APIC_INT0_L	32	O	INT0 signal to I/O APIC via series 10Ω resistor.
APIC_INT1_L	30	O	INT1 signal to I/O APIC via series 10Ω resistor.
APIC_INT2_L	31	O	INT2 signal to I/O APIC via series 10Ω resistor.
APIC_INT3_L	7	O	INT3 signal to I/O APIC via series 10Ω resistor.
APIC_INT4_L	33	O	INT4 signal to I/O APIC via series 10Ω resistor.
APIC_INT5_L	40	O	INT5 signal to I/O APIC via series 10Ω resistor.
APIC_INT6_L	9	O	INT6 signal to I/O APIC via series 10Ω resistor.
APIC_INT7_L	5	O	INT7 signal to I/O APIC via series 10Ω resistor.
BMC_SUSCLK	85	O	BMC suspend clock. The BUD divides the 32KHz PX4_SUSCLK (pin 41) by 256 to generate BMC_SUSCLK for BMC timestamping of SM events.
CLK_APIC	29	I	APIC clock from CK100 driver
CLK_PCI_BUD	90	I	Synchronous PCI master clock from CK100 driver
CLR_SMI	61	I	Driven by a PIIX4 GPIO bit 18 to clear a latched SMI condition. On assertion, clears the latched SMI signal in the BUD.
CPU_NMI	69	O	NMI to the processor(s), asserted when EN_NMI (pin 46) and NMI_PIIX4 (pin 50) are asserted, or when the Front Panel NMI switch is pressed.
CPU_SMI_L	83	O	Generates an SMI_L to the processor(s). This signal is gated by EN_SMI_L (pin 35) assertion and pending NMI request.
D0	94	I/O	Connects to ISA bus data bit SD0.
D1	96	I/O	Connects to ISA bus data bit SD1.
D2	97	I/O	Connects to ISA bus data bit SD2.
D3	98	I/O	Connects to ISA bus data bit SD3.
D4	99	I/O	Connects to ISA bus data bit SD4.
D5	100	I/O	Connects to ISA bus data bit SD5.
D6	1	I/O	Connects to ISA bus data bit SD6.
D7	2	I/O	Connects to ISA bus data bit SD7.
DIS_NON_FLASH_ SMI	8	I	Driven by PIIX4 GPIO bit 25 as part of secure Flash programming mechanism.
EN_NMI	46	I	Driven by PIIX4 GPIO bit 19 to gate NMI generation (other than Front Panel NMI).
EN_NMI_TO_SMI_L	36	I	Driven by PIIX4 GPIO bit 17 to redirect NMI to SMI.
EN_SMI_L	35	I	Driven by PIIX4 GPIO bit 9, to enable the generation of SMI to the processor(s).
EN_SMI_TO_NMI	62	I	Driven by the BMC to redirect SMI_L to NMI, which is controlled from the ISA interface using BMC mailbox registers. SMI_L redirection occurs by default.
F_SERR	54	I	Driven by PIIX4 GPIO bit 8 to force assertion of SERR_L on PCI. The BUD converts the signal to a pulse synchronous with PCI, which generates SERR_L.

* I = Input, O = Output

Table 3-10. BUD Signal Descriptions (cont.)

Signal	Pin	Type*	Description
FLASH_PE_L	48	I	Driven by PIIX4 GPIO bit 24 to indicate a Flash BIOS programming cycle. The BUD generates SMI_L in response, which supports the secure Flash programming mechanism on N440BX DP (see “Flash ROM BIOS” above).
IORD_L	87, 14	I	I/O read command driven by the ISA IORD_L signal.
IOWR_L	10	I	I/O write command driven by the ISA IOWC_L signal.
IRQ3	12	O	ISA IRQ3 signal from PCI to IRQ re-router in the BUD.
IRQ4	68	O	ISA IRQ4 signal from PCI to IRQ re-router in the BUD.
IRQ5	13	O	ISA IRQ5 signal from PCI to IRQ re-router in the BUD.
IRQ7	44	O	ISA IRQ7 signal from PCI to IRQ re-router in the BUD.
IRQ10	65	O	ISA IRQ10 signal from PCI to IRQ re-router in the BUD.
IRQ11	67	O	ISA IRQ11 signal from PCI to IRQ re-router in the BUD.
IRQ12	49	O	ISA IRQ12 signal from PCI to IRQ re-router in the BUD.
IRQ15	64	O	ISA IRQ15 signal from PCI to IRQ re-router in the BUD.
ISA_BALE	72	I	Driven by ISA BALE signal.
ISA_RSTDRV_L	88	I	Reset to the BUD from ISA interface reset signal.
NMI_FP_L	42	I	Front Panel NMI directly from the momentary push button switch on the Front Panel (in parallel with BMC connection). Pressing of this switch is captured by NMI latch circuitry in the BUD.
NMI_PIIX4	50	I	NMI indication from the PIIX4, which causes the assertion of CPU_NMI (pin 69) to occur if EN_NMI (pin 46) is also asserted.
P_GNT0_L	25	I	GNT0_L signal from NBX for arbitration expansion logic in BUD
P_INT_B_L	19	I	Interrupt B from cascaded PCI_INTB,C,D_L PCI slot interrupt swizzle, and SCSI controller PCI_INTB_L (wide).
P_INT_C_L	18	I	Interrupt C from cascaded PCI_INTB,C,D_L PCI slot interrupt swizzle, and SCSI controller PCI_INTC_L (narrow).
P_INT_D_L	17	I	Interrupt D from cascaded PCI_INTB,C,D_L PCI slot swizzle.
P_INT_NIC_L	20	I	Interrupt from NIC PCI_INTA_L
P_INT_PCI1_L	24	I	Interrupt from PCI slot 1 PCI_INTA_L
P_INT_PCI2_L	23	I	Interrupt from PCI slot 2 PCI_INTA_L
P_INT_PCI3_L	22	I	Interrupt from PCI slot 3 PCI_INTA_L
P_INT_PCI4_L	21	I	Interrupt from PCI slot 4 PCI_INTA_L
P_REQ0_L	79	O	REQ_L signal to NBX from PCI arbitration logic expansion logic in BUD.
P_SERR_L	80	O	PCI SERR_L signal forced by the BUD.
PD_CS_L	57	I	Driven by PIIX4 PCS0 as part of ISA I/O interface to the BUD.
PS_FRAME_L	37	I	FRAME_L signal from PCI interface for arbitration expansion logic in BUD.
PS_IRDY_L	55	I	IRDY_L signal from PCI interface for arbitration expansion logic in BUD.
PS_STOP_L	6	I	STOP_L signal from PCI interface for arbitration expansion logic in BUD.
PS_TRDY_L	52	I	TRDY_L signal from PCI interface for arbitration expansion logic in BUD.
PX4_SUSCLK	41	I	PIIX4 suspend clock. 32KHz clock source for BMC suspend clock.
RST_P_RST_L	89	I	Reset to the BUD from PCI interface reset signal.
S_GNT0A_L	71	O	GNT_L signal to PCI slot 1
S_GNT0B_L	84	O	GNT_L signal to SCSI controller chip
S_REQ0A_L	45	I	REQ_L signal from PCI slot 1
S_REQ0B_L	47	I	REQ_L signal from SCSI controller chip
SMI_BMC_L	27	I	Driven by the BMC to indicate the occurrence of an SMI condition.
SMI_PIIX4_L	56	I	Asserted by the PIIX4 on occurrence of an SMI_L condition, to indicate a request for handler service.
TCK	62	I/O	

Signal	Pin	Type*	Description
TDI	4	I/O	IEEE 1149.1 Boundary Scan Signals
TDO	73	I/O	(for prototype only)
TMS	15	I/O	

* I = Input, O = Output

2. Server Management

2.1. Overview

On N440BX Server, three serial buses that follow IMB protocol provide independent pathways for server management functions. The PIIX4 system management bus mentioned above (PIIX4 SMB) connects with each DIMM, and controls SDRAM clocks and processor speed configuration. A single micro-controller referred to as the Baseboard Management Controller (BMC) manages the other two IMB segments:

- Server Management Bus supporting 8K SEEPROM and processor/baseboard temperature sensors.
- Intelligent Management Bus (IMB) supporting connectors to system-wide server management devices.

In addition, the BMC manages sensors directly using I/O and ADC lines, controls the Emergency Management Port (EMP), detects and reports system fan failures, and manages Fault Resilient Booting (FRB). The BMC provides the Host ISA and IMB interfaces to server management features on N440BX Server. The following diagram illustrates server management architecture on the N440BX Server baseboard.

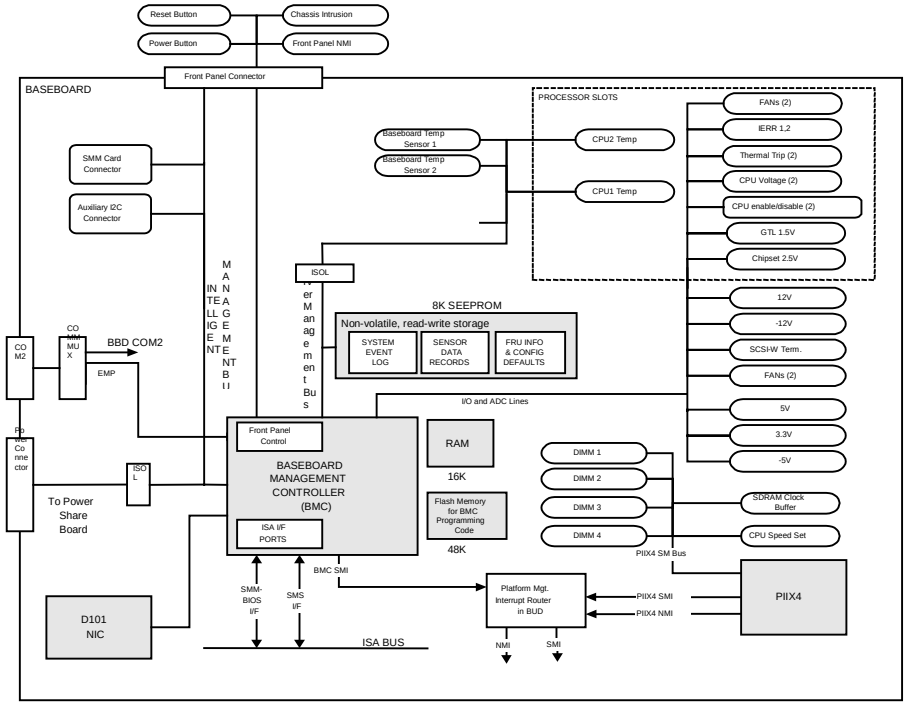

Figure 2-1. Server Management Block Diagram

2.2. Server Management Bus

The Server Management Bus (SMB) is a single master, open-drain, serial bus which is electrically and timing compatible with the 100 Kbps version of the IMB bus specification. The SMB extends throughout the baseboard providing an independent pathway for the BMC to communicate with 2 baseboard and 2 processor slot temperature sensors. In addition, the SMB supports an 8K SEEPROM device for non-volatile storage of the System Event Log (SEL), Sensor Data Record Repository (SDRR), FRU information, and configuration defaults. The BMC controls access to this device and manages the data structures within (refer to BMC description below).

Buffers are provided to isolate the baseboard and processor temperature sensors from the rest of the SMB. These buffers, running on 5V_Standby, keep the bus alive to the BMC even though main power is switched off. This allows the BMC to communicate with its SEEPROM at all times.

2.3. Intelligent Management Bus

The Intelligent Management Bus (IMB) is a multi-master, open-drain, serial bus which is also electrically and timing compatible with the 100 Kbps version of the IMB bus specification. The IMB attaches to connectors on the baseboard creating a server management network that extends throughout the baseboard and system chassis, providing an independent pathway for communications between the BMC and system-level server management devices (e.g., Hot-swap SCSI controller). In addition, the IMB provides inter-chassis communications extensions for a complete server management network solution.

The communication protocol for the IMB is defined in the *Intelligent Management Bus Communications Protocol Specification*. The protocol is designed to work with micro-controllers and other IMB masters, and slave devices such as IMB temperature sensors.

The IMB attaches to the following connector interfaces on the N440BX Server board:

- Auxiliary IMB connector
- Server Monitor Module (SMM) card feature connector
- Front panel connector
- Auxiliary power connector (via isolation buffer)

The N440BX Server board provides the main pull-ups on the clock (IMB_SCL) and data (IMB_SDA) lines of the IMB. This termination is sized to drive the full IMB, i.e., capacitive loading for not only the board, but for the chassis, SMM Card IMB, and auxiliary IMB connections. Sufficient pull-up capability is provided on the isolated side of the IMB for the BMC, SMM Card, SMM Card IMB, Front Panel IMB, and aux. IMB connections. These pull-ups are driven by 5V Standby. Since a full set of pull-ups is provided on the board, additional pull-ups are not necessary for external devices connecting to the IMB. Only the N440BX Server board should provide pull-ups for these connections.

Following are definitions of aux. IMB, SMM card, aux. power and main front panel connectors.

Auxiliary IMB Connector

The auxiliary IMB connector has the following pinout.

Table 2-3 Auxiliary IMB Connector Pinout

Pin	Signal
1	Local IMB SDA
2	GND
3	Local IMB SCL

Caution:

A shorted IMB connection at the auxiliary IMB connector will disrupt proper operation of the IMB.

2.3.1. SMM Card Feature Connector

The SMM card feature connector attaches to the IMB. In addition to IMB signals, the 26-pin connector provides the following signals as shown in the table below:

Table 2.3.1 SMM Card Feature Connector Pinout

Pin	Signal	Description
1	CPU_SMI_L	System Management Interrupt
2	LOCAL_IMB_SCL	IMB clock line
3	GND	Ground
4	Reserved	-
5	PWR_CNTRL_SFC_L	Host power supply on/off control
6	LOCAL_IMB_SDA	IMB serial data line
7	5VSTNDBY	+5V standby indication (power OK)
8	KEYLOCK_SFC_L	Keyboard lock signal
9	CPU_NMI	Non-maskable interrupt indication
10	VCC3	3.3V power supply status input
11	RST_SFC_L	Baseboard reset signal from Server Monitor Module
12	GND	Ground
13	GND	Ground
14	Reserved	-
15	SECURE_MODE_BMC	Secure mode indication
16	GND	Ground
17	SFC_CHASSIS_INSTRUSION_L	Chassis intrusion indication
18	Reserved	-
19	Reserved	-
20	GND	Ground
21	Reserved	-
22	Reserved	-
23	Reserved	unused
24	Reserved	-
25	Key pin (nc)	Connector key
26	Reserved	-

2.3.2. Auxiliary Power Connector

A 14-pin connector is provided for power supply status indication, as well as the IMB connection. Other power connector pin outs are specified in the ***Appendix***. The aux. power connector has the following pinout:

Table 2.3.2. Auxiliary Power Connector Pinout

Pin	Signal	Pin	Signal
1	+5V standby power mode sense Return	2	+5V standby power mode Sense
3	+3V Sense	4	+3V Sense Return
5	IMB Clock line	6	IMB Data line
7	GND	8	POWER_GOOD
9	PS_POWER_ON	10	GND
11	+5V standby power mode	12	nc (Key)
13	Reserved	14	VCC 24

2.4. Chassis Intrusion

The chassis intrusion header has been added to the baseboard of the N440BX Server. It is a 3-pin, shrouded and keyed connector located near the NIC indicator LEDs. Intrusion has occurred when the signal is open, chassis is secure when pulled to ground. The chassis intrusion header has the following pin out.

Table 2.4 Chassis Intrusion Pin-out

Pin	Signal
1	Chassis Intrusion
2	GND
3	Chassis Intrusion

2.4.1. Front Panel Connector

A 16-pin header is provided that attaches to the system front panel, which contains reset, NMI, and power control switches, LED indicators, as well as the IMB connection. The connector has the following pinout:

Table 2.4.1. Front Panel Connector Pinout

Pin	Signal	Pin	Signal
1	GND	2	Hard disk activity LED
3	Front panel reset switch	4	Front panel power switch
5	+5V standby mode	6	nc (key)
7	Front panel NMI switch	8	POWER_COL_FP_LED_L(Power LED/blink for ACPI Sleep)
9	Fan failure indicator LED	10	Chassis intrusion switch
11	Power fault LED	12	+5V standby power mode
13	IMB Data line	14	RJ45_ACTLED(LAN Active LED; supported on Astor chassis only
15	IMB Clock line	16	GND

2.5. Baseboard Management Controller (BMC)

On N440BX Server, all server management functionality formerly distributed between three controllers is concentrated in the BMC. The BMC and associated circuitry are powered from 5V_Standby, which remains active when system power is switched off. The BMC is implemented using a Dallas Semiconductor DS82CH10 micro-controller.

The primary function of the BMC is to autonomously monitor system platform management events, and log their occurrence in the non-volatile SEL. (Sensor Error Log). These events include such as over-temperature and over-voltage conditions, fan failure, or chassis intrusion. While monitoring, the BMC maintains the non-volatile SDRR (Sensor Data Record Repository), from which run-time information can be retrieved. The BMC provides an ISA host interface to SDRR information, so software running on the server can poll and retrieve the current status of the platform. A shared register interface is defined for this purpose.

SEL contents can be retrieved after system failure, for analysis by field service personnel using the System Setup Utility (SSU) and system management tools, such as Intel LANDesk® Server Manager. Since the BMC is powered by 5V_Standby, SEL (and SDRR) information is also available via the IMB. An Emergency Management Card, such as the Intel LANDesk SMM card, can obtain the SEL and make it remotely accessible using a LAN or telephone line connection. N440BX Server introduces the Emergency Management Port (EMP), which allows remote access to the SEL and other features using the COM2 port. During its watch, the BMC performs the following functions:

- Baseboard temperature and voltage monitoring
- VID Bit reading
- Processor presence monitoring and FRB control
- Baseboard fan failure detection and indicator control
- SEL interface management
- SDR Repository interface management
- SDR/SEL time stamp clock
- Baseboard Field Replaceable Unit (FRU) information interface
- System management watchdog timer
- Periodic SMI timer
- Front panel NMI handling
- Event receiver
- ISA host and IMB interface management
- Secure mode control, video blank and floppy write protect monitoring and control, front panel lock/unlock initiation.
- Sensor event initialization agent

- Wake-on LAN (WOL) via Magic Packet support
- ACPI Support

2.5.1. BMC Front Panel Control

The BMC performs all front panel controller functions on N440BX Server. These include control of system power, hard-resets, and the power failure LED. The BMC drives system power-on/off or hard reset from the following sources:

- Front panel push-button
- SMM card feature connector signal (controlled by secure mode)
- Transition of PIIX real-time clock alarm/suspend signal
- Command from IMB via front panel connector, aux. IMB, or SMM card
- Magic Packet signal from NIC
- Command from EMP
- Command from ISA interface
- BMC watchdog timer

2.5.2. Secure Mode

The BMC monitors the SECURE_MODE signal from the baseboard keyboard controller. When the system is powered up, and SECURE_MODE asserted, the BMC prevents power off or reset via the front panel power and reset push buttons. A 'Secure Mode Violation Attempt' event is flagged by the BMC whenever a front panel push button is pressed. The BMC also provides options for blanking the onboard video, and write-protecting the onboard floppy interface when Secure Mode is active.

2.5.3. Power Fault LED

The BMC controls the front panel Power Fault LED signal. The BMC asserts this signal whenever it attempts to power on the system without success, and when the BMC detects a power supply failure. The BMC can also be directed to assert this signal via an IMB 'Force Power Fault LED On' command.

2.6. Emergency Management Port (EMP)

The COM2 serial port on the N440BX Server can be configured for use as an Emergency Management Port (EMP). EMP provides a level of system management via RS-232 during powered-down, pre-boot, and post-boot situations. This allows System Management Software (SMS) interactions via point-to-point RS-232 connections, or external modem. EMP provides access to these basic management features:

- System power up
- System power down (Not available in restricted mode).
- System Reset (Not available in restricted mode).
- Access to the System Event Log, FRU, and Sensor Data Records.
- Access to BIOS Console Redirection.
- Password Protection

The EMP is intended for use in a secure environment. A simple password can be configured to provide a rudimentary level of security on the interface. System configuration options can be used to disable this interface.

The COM2 port can be used on N440BX Server for three different purposes: EMP, console redirection, or normal COM usage. If the BMC is using the port for EMP purposes, it is unavailable to the BIOS or SMS during this mode. If the System BIOS is using the port for console redirection, it is unavailable to the BMC or SMS (since the machine is still doing POST). Under normal usage COM2 appears to the OS as a normal serial port; in this case the BMC and System BIOS cannot use the port.

The N440BX Server EMP architecture supports several remote access modes, selectable using the F2 BIOS Setup Screen, as follows:

1. **Pre-boot only mode** - The EMP is only available while the machine is powered off and during POST. Just prior to booting the OS, the System BIOS disables the EMP by sending a command to the BMC. COM2 is then available as a normal serial port.
2. **SMS activated mode** - Essentially the same as Pre-boot only, except that SMS software may elect to take ownership or release control of COM2. This mode allows SMS to configure the system for remote access.
3. **Always active mode** - EMP and Console Redirect are available under the same conditions as listed in #1 above. However, the System BIOS leaves the port enabled for run-time EMP and SMS usage. The BIOS configures the hardware such that the O/S can not “see” the port.
4. **Always disabled mode** - EMP and Console Redirection are not available under any conditions.
5. **Restricted mode -** This option can be selected in conjunction with either the ‘Pre-boot Only’ or ‘Always Active’ modes listed above, using the BIOS setup interface. When activated, Power Down control, Front Panel NMI, and Reset Control via the EMP are disabled. Power On control, System Event Log access, FRU Inventory, and Sensor Data Repository access remain enabled. Console redirection operation is unaffected by Restricted Mode.

2.6.1. EMP Password

The BMC implements a simple password mechanism for the EMP, activated by BIOS setup. If the password is active, a correct password must be received on the EMP before any other commands are accepted. The password must be entered every time COM2 is switched over to EMP operation. It must also be re-entered if the EMP has been inactive for more than 30 seconds. Only BIOS setup can set or clear the password, it cannot be changed remotely.

2.7. Fault Resilient Booting

The BMC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If two processors are installed and the processor designated as the BSP fails to complete the boot process, FRB attempts to boot the system using the alternate processor.

- FRB level 1 is for recovery from a BIST failure detected during POST. This FRB recovery is fully handled by BIOS code.
- FRB level 2 is for recovery from a Watchdog time out during POST. The Watchdog timer for FRB level 2 detection is implemented in the BMC.
- FRB level 3 is for recovery from a Watchdog time out on Hard Reset / Power-up. Hardware functionality for this level of FRB is provided by the BMC on the processor subsystem.

FRB-3 is managed by the BMC, which controls the ability to boot using either processor in the event of a catastrophic processor failure. On power up, a timer starts that can only be stopped by a healthy processor using the GPIO bit, FRB_TMRHLT_L, on the PIIX4. If processor 0 fails to halt the FRB timer before time out, the controller asserts STOP_FLUSH to the processor and asserts FRB_RST_L for 10ms. When the system comes out of reset, processor 0 is prevented from acting as the BSP, allowing the other processor to take over the boot process.

2.8. System Fan Interface

N440BX Server provides four 3-pin, shrouded, and keyed fan connectors. Two of these connectors, located next to each Pentium® II/ Pentium® III processor card on the baseboard, are for a fansink. The remaining two connectors on the baseboard attach to chassis fans equipped with a sensor that indicates whether the fan is operating. The sensor pins for these fans are routed to the BMC for failure monitoring. The two connector types have the following pinout:

Table 2.8. Chassis Fan Connector Pinout

Pin	Signal
1	GND
2	Fan Sensor
3	+12V

Table 2.8.1. Fansink Connector Pinout

Pin	Signal
1	GND
2	+12V
3	Fan Sensor

The following table details the baseboard jumper functions.

Table 2.8.2 Board Jumper description

Function	Pins (default in bold)	What it does at system reset
CMOS clear	**1-2, Protect**	Preserves the contents of NVRAM.
	2-3, Erase	Replaces the contents of NVRAM with the Intel manufacturing default settings.
Password clear	**5-6, Protect**	Maintains the current system password.
	6-7, Erase	Clears the password.
Recovery Boot	**9-10, Normal**	System attempts to boot using the BIOS stored in flash memory.
	10-11, Recovery	BIOS attempts a recovery boot, loading BIOS code from a floppy diskette into the flash device. This is typically used when the BIOS code has been corrupted.
Boot Block Write Protect	**13-14, Protect**	BIOS boot block is write-protected
	14-15	BIOS boot block is erasable and programmable
		CAUTION: Programming the boot block incorrectly will prevent the system from booting.
Clock Enable	**1-2, Protect**	Processor speed configuration is protected.
	2-3, Enable	Processor speed configuration is enabled. Changes can be made in BIOS/SSU.
FRB Timer Enable	**5-6, Enable**	FRB operation is enabled (system boots from processor 1 if processor 0 fails)..
	6-7, Disable	FRB is disabled..
Chassis Intrusion Detection	**9-10, Enable**	Switch installed on chassis indicates when cover has been removed.
	10-11, Disable	Chassis intrusion switch is bypassed.

3. Memory and Other Resource Mappings

This chapter describes the initial programming environment including address maps for memory and I/O, techniques and considerations for programming ASIC registers, and hardware options configuration.

3.1. Memory Space

At the highest level, Pentium® II/ Pentium® III processor address space is divided into 4 regions, as shown in the following figure. Each region contains sub-regions, as described in the following sections. Attributes can be independently assigned to regions and sub-regions using PAC registers.

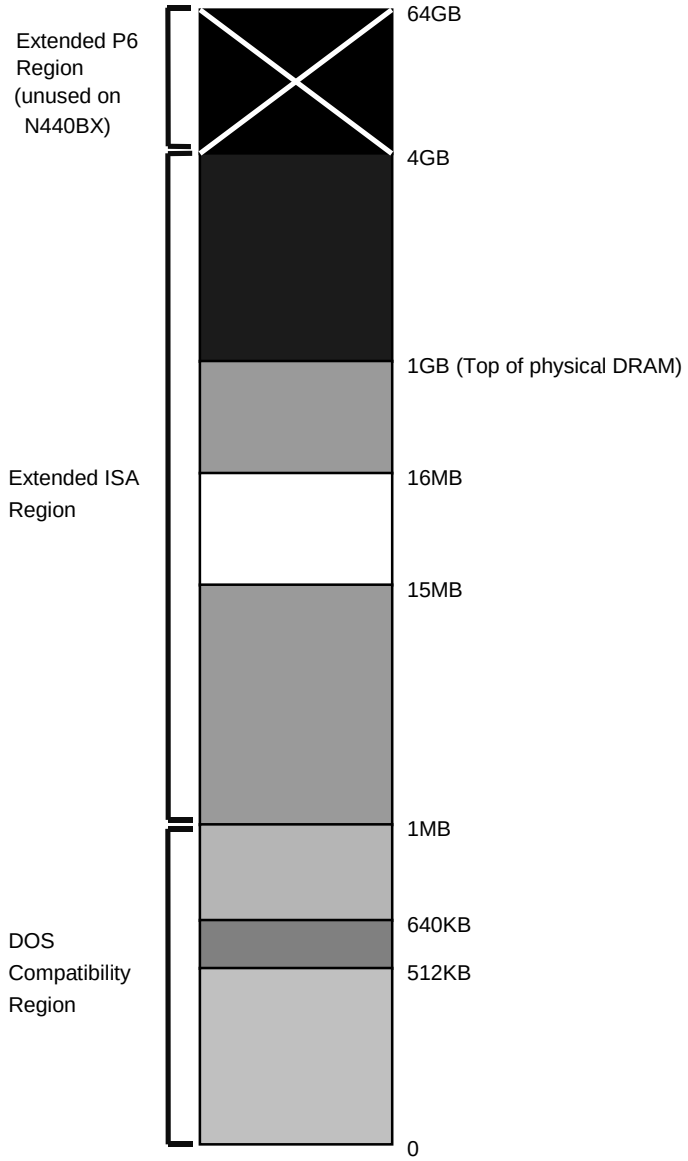

Figure 15. Pentium II/Pentium III processor memory address space

3.2. DOS Compatibility Region

The first region of memory below 1MB was defined for early PCs, and must be maintained for compatibility reasons. This region is divided into sub-regions as shown in the following figure.

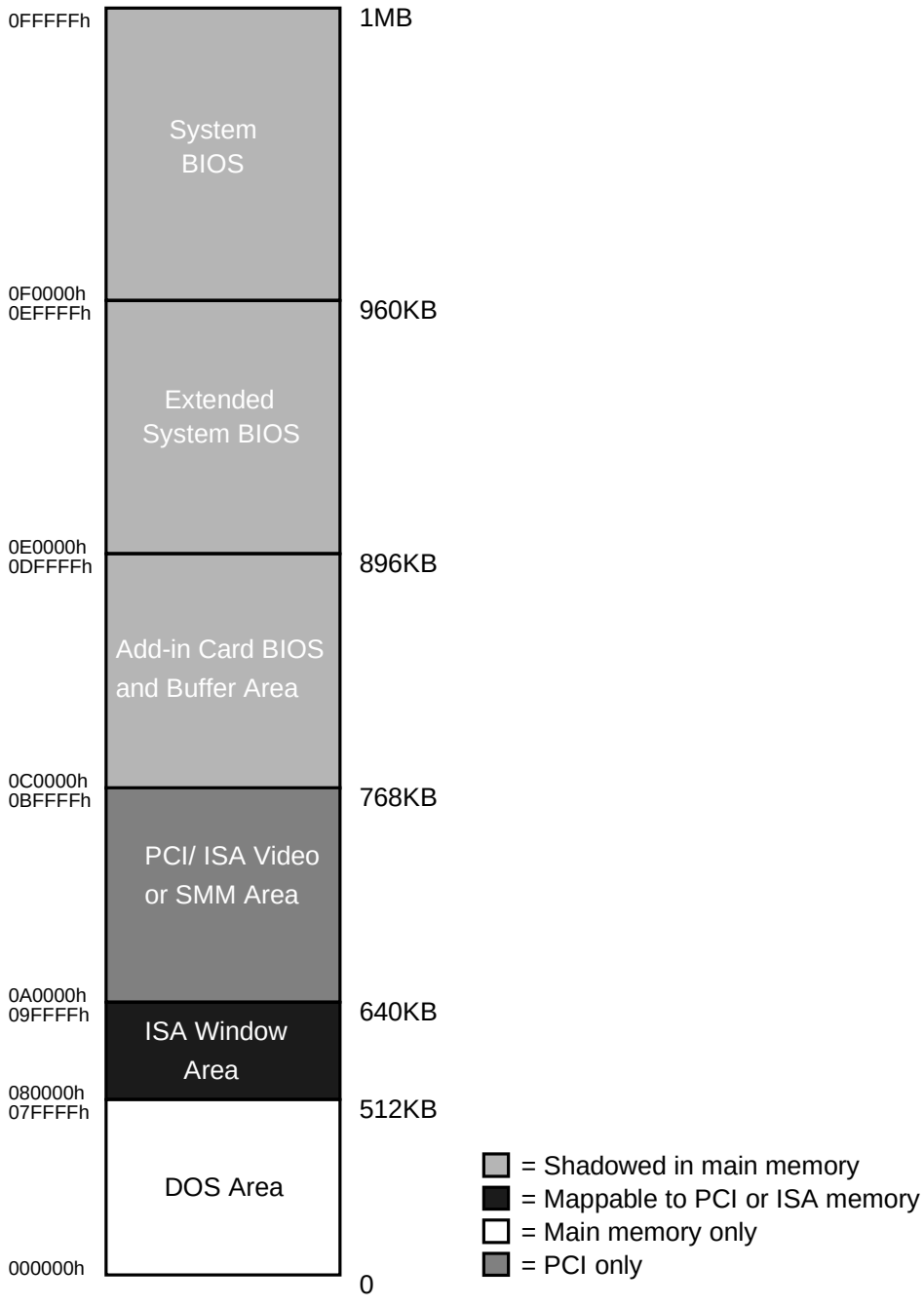

Figure 16. DOS Compatibility Region

3.3. DOS Area

The DOS region is 512KB in the address range 0 to 07FFFFh. This region is fixed and all accesses go to main memory.

3.4. ISA Window Memory

The ISA Window Memory is 128KB between the addresses of 080000h to 09FFFFh. This area can be mapped to the PCI bus or main memory.

3.5. Video or SMM Memory

The 128KB Graphics Adapter Memory region at 0A0000h to 0BFFFFh is normally mapped to the VGA controller on the PCI bus. This region is also the default region for SMM space. The SMM region can be remapped by programming the SMRAM Control Register in the PAC.

3.6. Add-in Card BIOS and Buffer Area

The 128KB region between addresses 0C0000h and 0DFFFFh is divided into eight segments of 16KB segments mapped to ISA memory space, each with programmable attributes, for expansion card buffers. Historically, the 32KB region from 0C0000h to 0C7FFFh has contained the video BIOS location on a video card. However, on N440BX Server, the video BIOS is located in the Extended BIOS or System BIOS areas.

3.7. Extended System BIOS

This 64KB region from 0E0000h to 0EFFFFh is divided into 4 blocks of 16KB each, and may be mapped with programmable attributes to map to either main memory or to the PCI bus. Typically, this area is used for RAM or ROM.

3.8. System BIOS

The 64KB region from 0F0000h to 0FFFFFh is treated as a single block. By default this area is normally Read/Write disabled with accesses forwarded to the PCI bus. Through manipulation of R/W attributes, this region can be shadowed into main memory.

3.9. Extended Memory

Extended memory on N440BX Server is defined as all address space greater than 1MB. The Extended Memory region covers 4GB of address space from addresses 0100000h to FFFFFFFFh, as shown in the following figure.

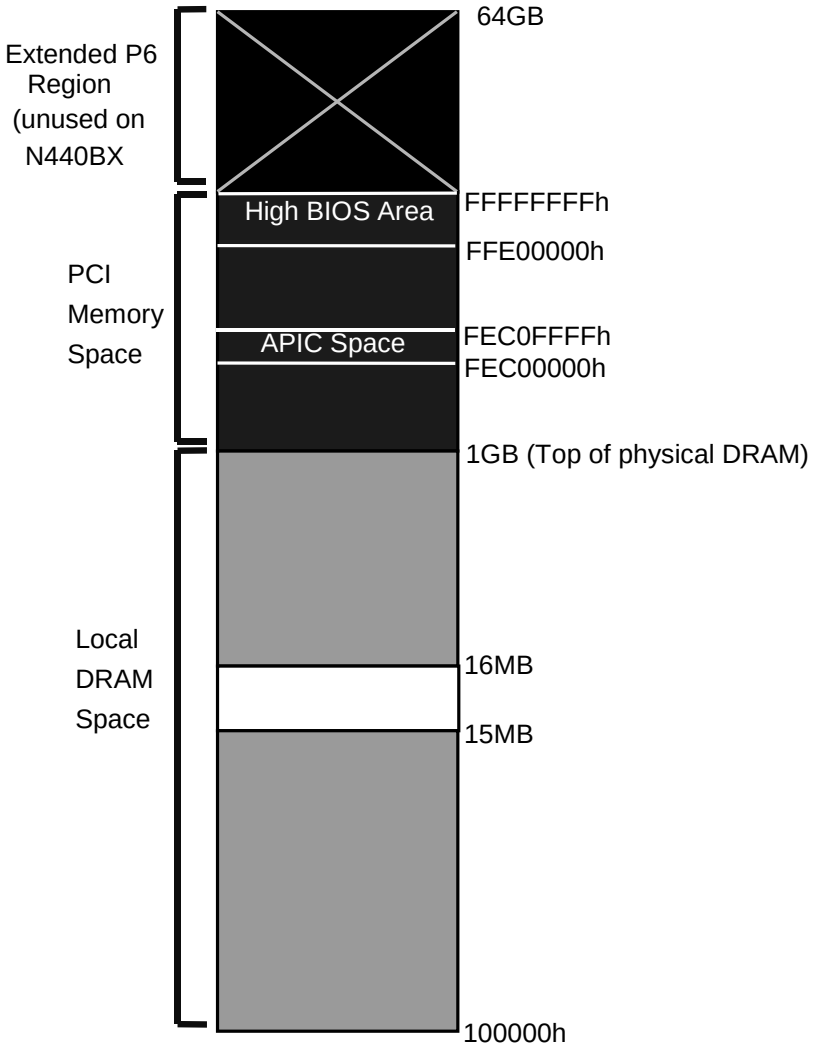

Figure 17 Extended Memory Map

3.10. Main Memory

All installed SDRAM greater than 1MB is mapped to local main memory, up to the top of physical memory that is located at 1GB. Memory between 1MB to 15MB is considered to be standard ISA extended memory. 1MB of memory starting at 15MB can be optionally mapped to the PCI bus memory space. The remainder of this space, up to 1GB, is always mapped to main memory.

3.11. PCI Memory Space

Memory addresses between 1GB and 4GB are mapped to the PCI bus. This region is divided into three sections: High BIOS, APIC Configuration Space, and General-purpose PCI Memory.

The General-purpose PCI Memory area is typically used for memory-mapped I/O to PCI devices. The memory address space for each device is set using PCI configuration registers

3.12. High BIOS

The top 2MB of Extended Memory is reserved for the system BIOS, extended BIOS is for PCI devices, and A20 aliasing by the system BIOS. The Pentium II/Pentium III processor begins executing from the High BIOS region after reset. Only 256KB of the high BIOS area is actually required by the BIOS, but 2MB is required by Pentium II/Pentium III processor MTRR programming.

3.13. I/O APIC Configuration Space

A 64KB block located 20MB below 4GB (0FEC00000h to 0FEC0FFFFh) is reserved for the I/O APIC configuration space.

I/O APIC units are located beginning at a base address determined by subtracting 013FFFF0h from the reset vector. The first I/O APIC is located at FEC00000h. Each I/O APIC unit is located at FEC0x000h where x is the I/O APIC unit (0 through F).

3.14. Extended Pentium II/Pentium III Processor Region (above 4GB)

A Pentium® II / Pentium® III processor-based system can have up to 64GB of addressable memory. However, the 82440BX PCIset only supports 32-bit addressing, with the BIOS operating in 4GB of address space (the memory DIMMs provide up to 512MB of main memory). All accesses to the region from 4GB to 64GB are claimed by the PAC and terminated. Write data is dropped and zeroes are returned on reads.

3.15. Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into memory located on the Pentium II/Pentium III processor bus. Typically, this is done to allow ROM code to execute more rapidly out of RAM. ROM is designated read-only during the copy process while RAM at the same address is designated write-only. After copying, the RAM is designated read-only and the ROM is designated write-only (shadowed). Processor bus transactions are routed accordingly. Transactions originating from the PCI bus or ISA masters and targeted at shadowed memory blocks will not appear on the processor's bus.

3.16. SMM Mode Handling

A Pentium II/Pentium III processor asserts SMMEM_L in its Request Phase if it is operating in System Management Mode (SMM). SM code resides in SMRAM. SMRAM can overlap with memory residing on the Pentium II/ Pentium III processor bus or memory normally residing on the PCI bus. The PAC determines where SMRAM space is located through the value of the SMM Range configuration space register.

The SMRAM Enable bit in the SMRAM Enable configuration register will determine how the SM accesses are handled by the PAC component. When the SMRAM Enable bit is zero (SMRAM disabled), accesses to the SMM Range with SMMEM_L asserted are ignored by the PAC. When the SMRAM Enable bit is one (SMRAM enabled), accesses to the SMM range with SMMEM_L asserted are claimed by the PAC.

If the SMMEM_L signal is not asserted, the SMM Range is not decoded regardless of the state of the SMRAM Enable bit (this allows SMRAM to overlap with memory normally residing on the processor bus).

In summary, when the SMMEM_L signal is asserted, the SMM Range is similar to a Memory Space Gap, where the SMM Enable bit either enables or disables the memory gap.

The SMI_L signal may be asserted in the Response Phase by a device in SMM power-down mode.

Refer to the System Management RAM Control Register (SMRAM 72h)

3.17. I/O Map

The PAC allows I/O addresses to be mapped to the processor bus or through designated bridges in a multi-bridge system. Other PCI devices, including PIIX4, have built-in features that support PC-compatible I/O devices and functions, which are mapped to specific addresses in I/O space. On N440BX Server, the PIIX4 provides the bridge to ISA functions. The I/O map in the following table shows the location in N440BX Server I/O space of all directly I/O-accessible registers. PCI configuration space registers for each device control mapping in I/O and memory spaces, and other features that may affect the global I/O map. All configuration space registers for PCI devices are described in Chapter 5. The SuperI/O controller contains configuration registers that are accessed through an index and data port mechanism.

Table 3 N440BX I/O Map

Address(es)	Resource	Notes
0000h - 000Fh	DMA Controller 1	
0010h - 001Fh	DMA Controller 1	aliased from 0000h - 000Fh
0020h - 0021h	Interrupt Controller 1	
0022h - 0023h		
0024h - 0025h	Interrupt Controller 1	aliased from 0020h - 0021h
0026h - 0027h		
0028h - 0029h	Interrupt Controller 1	aliased from 0020h - 0021h
002Ah - 002Bh		
002Ch - 002Dh	Interrupt Controller 1	aliased from 0020h - 0021h
002Eh - 002Fh	SuperI/O Index and Data Ports	
0030h - 0031h	Interrupt Controller 1	aliased from 0020h - 0021h
0032h - 0033h		
0034h - 0035h	Interrupt Controller 1	aliased from 0020h - 0021h
0036h - 0037h		
0038h - 0039h	Interrupt Controller 1	aliased from 0020h - 0021h
003Ah - 003Bh		
003Ch - 003Dh	Interrupt Controller 1	aliased from 0020h - 0021h
003Eh - 003Fh		
0040h - 0043h	Programmable Timers	
0044h - 004Fh		
0050h - 0053h	Programmable Timers	aliased from 0040h - 0043h
0054h - 005Fh		
0060h, 0064h	Keyboard Controller	Keyboard chip select from 87309
0061h	NMI Status & Control Register	
0063h	NMI Status & Control Register	aliased
0065h	NMI Status & Control Register	aliased
0067h	NMI Status & Control Register	aliased

0070h	NMI Mask (bit 7) & RTC Address (bits 6::0)	
0072h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0074h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0076h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0071h	RTC Data	
0073h	RTC Data	aliased from 0071h
0075h	RTC Data	aliased from 0071h
0077h	RTC Data	aliased from 0071h

Table 4 N440BX I/O Map (cont.)

Address(es)	Resource	Notes
0080h - 0081h	BIOS Timer	
0080h - 008Fh	DMA Low Page Register	PIIX4
0090h - 0091h	DMA Low Page Register (aliased)	PIIX4
0092h	System Control Port A (PC-AT control Port) (this port not aliased in DMA range)	PIIX4
0093h - 009Fh	DMA Low Page Register (aliased)	PIIX4
0094h	Video Display Controller	
00A0h - 00A1h	Interrupt Controller 2	PIIX4
00A4h - 00A15	Interrupt Controller 2 (aliased)	PIIX4
00A8h - 00A19	Interrupt Controller 2 (aliased)	PIIX4
00ACh - 00ADh	Interrupt Controller 2 (aliased)	PIIX4
00B0h - 00B1h	Interrupt Controller 2 (aliased)	PIIX4
00B2h	Advanced Power Management Control	PIIX4
00B3h	Advanced Power Management Status	PIIX4
00B4h - 00B5h	Interrupt Controller 2 (aliased)	PIIX4
00B8h - 00B9h	Interrupt Controller 2 (aliased)	PIIX4
00BCh - 00BDh	Interrupt Controller 2 (aliased)	PIIX4
00C0h - 00DFh	DMA Controller 2	PIIX4
00F0h	Clear NPX error	Resets IRQ13
00F8h - 00FFh	x87 Numeric Coprocessor	
0102h	Video Display Controller	
0170h - 0177h	Secondary Fixed Disk Controller (IDE)	PIIX4 (not used)
01F0h - 01F7h	Primary Fixed Disk Controller (IDE)	PIIX4
0200h - 0207h	Game I/O Port	Not used
0220h - 022Fh	Serial Port A	
0238h - 023Fh	Serial Port B	
0278h - 027Fh	Parallel Port 3	
02E8h - 02EFh	Serial Port B	
02F8h - 02FFh	Serial Port B	
0338h - 033Fh	Serial Port B	
0370h - 0375h	Secondary Floppy	
0376h	Secondary IDE	
0377h	Secondary IDE/Floppy	
0378h - 037Fh	Parallel Port 2	
03B4h - 03BAh	Monochrome Display Port	
03BCh - 03BFh	Parallel Port 1 (Primary)	
03C0h - 03CFh	Video Display Controller	

03D4h - 03DAh	Color Graphics Controller	
03E8h - 03EFh	Serial Port A	
03F0h - 03F5h	Floppy Disk Controller	
03F6h - 03F7h	Primary IDE - Sec. Floppy	
03F8h - 03FFh	Serial Port A (Primary)	
0400h - 043Fh	DMA Controller 1, Extended Mode Registers.	PIIX4

Table 22 N440BX I/O Map (cont.)

Address(es)	Resource	Notes
0461h	Extended NMI / Reset Control	PIIX4
0462h	Software NMI	PIIX4
0480h - 048Fh	DMA High Page Register.	PIIX4
04C0h - 04CFh	DMA Controller 2, High Base Register.	
04D0h - 04D1h	Interrupt Controllers 1 and 2 Control Register.	
04D4h - 04D7h	DMA Controller 2, Extended Mode Register.	
04D8h - 04DFh	Reserved	
04E0h - 04FFh	DMA Channel Stop Registers	
0678h - 067Ah	Parallel Port (ECP)	
0778h - 077Ah	Parallel Port (ECP)	
07BCh - 07BEh	Parallel Port (ECP)	
0800h - 08FFh	NVRAM	
0C80h - 0C83h	EISA System Identifier Registers	PIIX4
0C84h	Board Revision Register	
0C85h - 0C86h	BIOS Function Control	
0CA9h	DISMIC Data Register	Server management mailbox registers.
0CAAh	DISMIC Control/Status Register	
0CABh	DISMIC Flags Register	
0CF8h	PCI CONFIG_ADDRESS Register	Located in PAC
0CF9h	PAC Turbo and Reset control	PIIX4
0CFCh	PCI CONFIG_DATA Register	Located in PAC
46E8h	Video Display Controller	
xx00 - xx1F*	SCSI registers	Refer to SCSI chip doc.

*SCSI I/O base address is set using configuration registers.

3.18. Accessing Configuration Space

All PCI devices contain PCI configuration space, accessed using mechanism #1 defined in the *PCI 2.1 Local Bus Specification*. The PIIX4 is accessed as a multi-function PCI device, with 3 sets of configuration registers.

If dual processors are used, only the processor designated as the BSP should perform PCI configuration space accesses. Precautions should be taken to guarantee that only one processor is accessing configuration space at a time.

Two Dword I/O registers in the PAC are used for the configuration space register access:

- CONFIG_ADDRESS (I/O address 0CF8h)
- CONFIG_DATA (I/O address 0CFCh)

When CONFIG_ADDRESS is written to with a 32-bit value selecting the bus number, device on the bus, and specific configuration register in the device, a subsequent read or write of CONFIG_DATA initiates the data transfer to/from the selected configuration register. Byte enables are valid during accesses to CONFIG_DATA; they determine whether the configuration register is being accessed or not. Only full Dword reads and writes to CONFIG_ADDRESS are recognized as a configuration access by the PAC. All other I/O accesses to CONFIG_ADDRESS are treated as normal I/O transactions.

3.18.1. CONFIG_ADDRESS Register

CONFIG_ADDRESS is 32 bits wide and contains the field format shown in the following figure. Bits [23::16] choose a specific bus in the system. Bits [15::11] choose a specific device on the selected bus. Bits [10::8] choose a specific function in a multi-function device. Bits [7::2] select a specific register in the configuration space of the selected device or function on the bus.

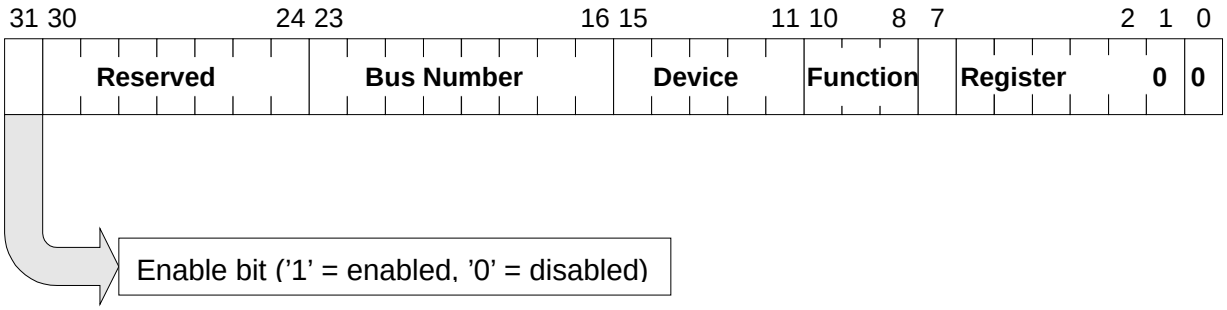

Figure 18 CONFIG_ADDRESS Register

3.18.2. Device Number and IDSEL Mapping

Each device under a PCI bridge has its IDSEL input connected to one bit out of the PCI bus address/data signals AD[31::11] for the PCI bus. Each IDSEL-mapped AD bit acts as a chip select for each device on PCI. The host bridge responds to a unique PCI device ID value, that along with the bus number, cause the assertion of IDSEL for a particular device during configuration cycles. The following table shows the correspondence between IDSEL values and PCI device numbers for the PCI bus. The lower 5-bits of the device number are used in CONFIG_ADDRESS bits [15::11].

Table 23 PCI Configuration IDs and Device Numbers

	PCI Bus	
IDSEL	**Device #**	**Device**
31	10100b	PIIX4
30	10011b	
29	10010b	CL-GD5480 video chip
28	10001b	
27	10000b	82558 NIC
26	01111b	PCI Slot 4
25	01110b	
24	01101b	
23	01100b	PCI Slot 3
22	01011b	Symbios 53C876
21	01010b	PCI Slot 2

20	01001b	PCI Slot 1
19	01000b	
18	00111b	
17	00110b	
16	00101b	
15	00100b	
14	00011b	
13	00010b	
IDSEL	**Device #**	**Device**
12	00001b	
11	00000b	Hardwired to host bridge

3.19. Error Handling

The N440BX Server is designed to report the following types of system errors: ISA bus, PCI bus, ECC memory, and System limit. Errors are reported using SMI_L. SMI is used for server management and advanced error processing. All errors can be intercepted by SMI for preprocessing (if SMI_L is enabled), or handled directly by NMI handlers. Some errors have to generate an NMI even if they are intercepted by the SMI, because the traditional way to handle errors in PC architecture is via the NMI. The N440BX emulates non-ISA errors as ISA-compatible using NMI and SMI_L.

Three error handlers are required: BIOS NMI handler, OS NMI handler, and SMI handler. The SMI has the highest priority to process the errors and is OS-transparent. The OS NMI handler can process all errors as well, even when the SMI is disabled. In this case, some errors are SMI resources that can be routed to the NMI. The BIOS NMI handler processes the ISA-compatible errors and disables the NMI only.

3.20. Hardware Initialization and Configuration

This section describes the following:

- System initialization
- Programming considerations for various portions of the I/O system

3.21. System Initialization Sequence

A Pentium® II / Pentium® II processor system based on the 82440BX PCIset is initialized and configured in the following manner.

System power is applied. The power-supply provides resets using the RST_PWR_GD_BB signal. PCI reset (RST_P_RST_L) is driven to tri-state the PCI bus in order to prevent PCI output buffers from short circuiting when the PCI power rails are not within the specified tolerances. The PAC asserts G_CPURST_L to reset the processor(s).

The PAC is initialized, with its internal registers set to default values.

Before G_CPURST_L is deasserted, the PAC asserts BREQ0_L. Processor(s) in the system determine which host bus agents they are, Agent 0 or Agent 1, according whether their BREQ0_L or BREQ1_L is asserted. This determines bus arbitration priority and order.

The processor(s) in the system determines which processor will be the BSP by issuing Bootstrap Inter-Processor Interrupts (BIPI) on the APIC data bus. The non-BSP processor becomes an application processor and idles, waiting for a Startup Inter-Processor Interrupt (SIPI).

The BSP begins by fetching the first instruction from the reset vector.

PAC registers are updated to reflect memory configuration. SDRAM is sized and initialized.

All PCI and ISA I/O subsystems are initialized and prepared for booting.

3.22. Server Management Programming Interface

DISMIC mailbox registers provide a mechanism for communications between IMB server management bus agents, and SMS or SMI handler code running on the server. DISMIC mailbox register space, physically located in the device, is mapped to BMC external data memory and ISA I/O space. This shared register space consists of three byte-wide registers:

- Flags Register - provides semaphores for use in various defined operations
- Control/Status Register - accepts commands and returns completion codes
- Data Register - provides a port for transactions that exchange data

In addition to the ports described above, the DISMIC contains a port 070h snoop register. See the section titled "Port 70h Snoop Register" below for further information.

SMS and SMI handler code interacts with the register interface using a variety of read and write commands encapsulated in messages. The origin of a message is specified during a particular transaction using Control Codes that are unique to the transaction, allowing the interface to allocate priority to various sources, and control SMI handler and SMS precedence (the SMI handler can always abort or temporarily interrupt any transaction).

3.22.1. Port 70h Snoop Register

The Port 70h Snoop Register reads back the state of bit 7 of I/O port 70h (RTC NMI enable bit) to the BMC. This register shadows any ISA write to port 70h. Due to architectural constraints in the DISMIC, the contents of this register cannot be made available for direct I/O read access at an alternate address location on the ISA bus. Access to the register's contents is provided only through the BMC using a command defined for this purpose.

3.23. PCI Interrupt to IRQ Routing Control

Embedded in a separate programmable logic device is logic for rerouting of PCI interrupts to ISA IRQs. Two I/O locations are reserved by the BIOS using the PIIX4 Programmable Chip Select Control register, for control of the PCI to IRQ re-router feature: CA4h and CA5h. Writes to the upper and lower nibble of each byte determine whether the interrupt is passed through to the I/O APIC, or rerouted to an ISA IRQ input on the PIIX4. The following figure shows the PCI interrupt line associated with each nibble. The following table defines the encoding of each nibble.

A0 = 1		A0 = 0	
PCI_INTD_L	PCI_INTC_L	PCI_INTB_L	PCI_INTA_L

Bit 0

Figure 19 PCI to IRQ Rerouter Control Bytes

The following table reviews PCI to IRQ nibble encoding.

Table 24 PCI to IRQ Rerouter Nibble Encoding

Value	Meaning
0000b	Pass interrupt through to I/O APIC (default)
0001b	Reserved
0010b	Reserved
0011b	Reroute PCI_INTn_L to IRQ3
0100b	Reserved
0101b	Reroute PCI_INTn_L to IRQ5
0110b	Reserved
0111b	Reroute PCI_INTn_L to IRQ7
1000b	Reserved
1001b	Reroute PCI_INTn_L to IRQ9
1010b	Reroute PCI_INTn_L to IRQ10
1011b	Reroute PCI_INTn_L to IRQ11
1100b	Reserved
1101b	Reserved
1110b	Reserved
1111b	Reroute PCI_INTn_L to IRQ15

4. BIOS

4.1. BIOS

4.1.1 BIOS Overview

The term “BIOS," as used in the context of this document, refers to the following:

- System BIOS, that controls basic system functionality using stored configuration values.
- Configuration Utilities (CU) consisting of Flash ROM-resident Setup utility and system memory-resident Server Setup Utility (SSU), that provides user control of configuration values stored in NVRAM and battery-backed CMOS configuration RAM.
- Flash Memory Update utility (IFLASH), that loads predefined areas of Flash ROM with Setup, BIOS, and other code/data.

Each of these are introduced here, with references to the appropriate chapter for details. A summary of memory maps for Flash, and CMOS configuration RAM and NVRAM register spaces, which provide the operating environment for BIOS code, is also presented. The following figure shows the relationship between BIOS components and register spaces. The unshaded areas are loaded into Flash using the Flash Memory Update Utility (IFLASH).

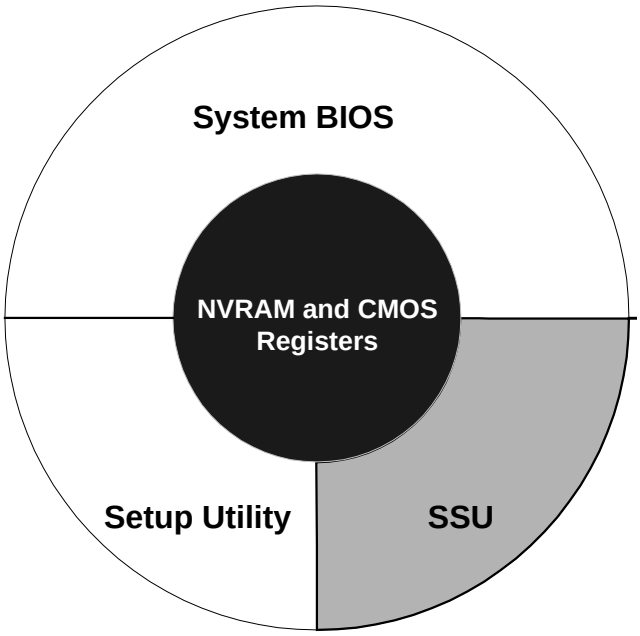

Figure 4-1. N440BX BIOS Architecture

4.1.1. System BIOS over view

The system BIOS is the core of the Flash ROM-resident portion of the BIOS. The system BIOS provides standard PC-BIOS services and some new industry standards, such as I_2O, Plug and Play, DMI and ACPI. In addition, the system BIOS provides support for these N440BX specific features: security features, multiple-speed processor support, SMP support, fault resilient booting (FRB), logging of critical events, server management features, CMOS configuration RAM defaults, multiple language support, defective DIMM detection and remapping, automatic detection of video adapters, PCI BIOS interface, option ROM shadowing, system information reporting, ECC support, SMI support, user-supplied BIOS support, L2 cache support, memory sizing, boot drive sequencing, and resource allocation support.

4.1.2. Configuration Utilities

The SSU provides the means to configure on board hardware devices and add-in cards. The SSU consists of the following:

- Standard PC-AT Setup utility, embedded in Flash ROM, for configuration of on board resources.
- SSU, for configuration of add-in cards as well as on board resources, which must be run from a boot diskette or CD-ROM shipped with the system.

4.1.3. Flash Update Utility

The system BIOS and the setup utility is resident in partitioned Flash ROM. The device is in-circuit re-programmable, except for the recovery boot block, which is electrically protected from erasure. A jumper on the baseboard can enable writing to boot block.

To reload Flash memory from a floppy disk (or from CD-ROM), use a Flash update utility. The file to be loaded contains a new copy of BIOS code. The utility must match the board ID with the one in the load file to protect against reprogramming the Flash with BIOS for another platform. Baseboard revisions may share a common SSU but may require different BIOS code.

4.1.3.1. System Flash ROM layout

The Flash ROM contains system initialization routines, Setup utility, and runtime support routines. The exact layout is subject to change, as determined by Intel. All areas are 64KB in size (symmetric flash). 64KB is reserved for diagnostic boot loader and an 8KB User block is available for user ROM code or custom logos. 64KB area is used to store the string database. The complete ROM is visible, starting at physical address 4GB less 512KB. The Flash Memory Update utility loads BIOS components to blocks of specified length and location, as summarized in *Table 4-1: Flash Map Summary*. This is a typical example of a Flash block table.

Table 4-1. Flash ROM Map Summary

Length	Base Address	Usage
1000h	0FFF80000h	ESCD (4k) see below
9000h	0FFF81000h	DMI , SCSI NVRAM, Multiboot data
10000h	0FFF90000h	Console Redirection
2000h	0FFF98000h	User Binary
4000h	0FFF9C000h	Diagnostic Boot Area
10000h	0FFFA0000h	BIOS block
10000h	0FFFB0000h	BIOS block (smm handler)
10000h	0FFFC0000h	BIOS block (strings, SCSI BIOS)
10000h	0FFFD0000h	BIOS block (video BIOS, setup)
C000h	0FFFE0000h	BIOS block
4000h	0FFFEC000h	Recovery Block
10000h	0FFFF0000h	BIOS block

None of the above blocks are visible at the aliased addresses below 1 MB due to shadowing. The above table is representative only of the information contained in the Flash ROM. The BIOS alone needs to know the exact map. Intel reserves the right to change the Flash map without notice. All block in this flash part are 64k (10000h) in length. The BIOS will adjust the size of each component to fit in a given block. Only the Recovery block, ESCD and DMI are fixed at a given location.

Offset	Length	Description
0	1000h	Plug-n-Play ESCD
1000h	0180h	DMI information
1180h	0080h	Mfg.
1200h	0100h	Custom CMOS
1300h	0200h	Multiboot
1500h	0020h	Hard Drive
1520h	0080h	SCSI B
1700h	01F4h	Scratch
18f4h	070ch	SCSI A
2000h	2810h	Processor Patch BIOS Update
4810h	0040h	System ID
4850h	0020h	OEM Throttle Register

4.2. System BIOS

This chapter describes those features of the system BIOS that are unique to N440BX. The N440BX platform does not provide legacy support USB. Legacy mode of USB keyboard emulating a PS/2 keyboard via SMM is not supported on N440BX. While devices such as USB keyboards will work with OS drivers, these keyboards will not respond during BIOS POST. The following groups of system BIOS features are described here:

- Security features
- Auto-configuration features
- Performance features
- Reliability features
- System services
- OEM customization hooks
- Console redirection
- I_2O support
- DMI support
- POST Memory Manager Support
- ACPI support

4.3. Security Features

The BIOS provides a number of security features. This section describes the security features and operating model.

4.3.1. Operating Model

The following table summarizes the operation of security features supported by the BIOS.

Table 4-2. Security Features Operating Model

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Secure mode	Keyboard Inactivity Timer, Runtime activation of KBC Hotkey	User Password enabled in SSU	• Screen goes blank (if enabled in SSU). • Floppy writes are disabled (if selected in SSU). • Power and Reset switches on the front panel are disabled(if enabled in Setup). • No mouse or keyboard input is accepted.	User Password	• Video is restored. • Floppy writes are enabled. • Power and Reset switches are enabled. • Keyboard and mouse inputs are accepted.

Table 4-3. Security Features Operating Model

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Secure boot	Power On/Reset	User Password and Secure Boot Enabled in SSU	• Enter secure mode. • Prompts for Password, if booting from drive A. • Video is blanked (if enabled in Setup). • Floppy writes are disabled (if programmed in SSU). • Power and Reset switches on the front panel are disabled(if programmed in SSU). • No mouse or keyboard input is accepted; however, the Mouse driver will be allowed to load before a password is required. • If booting from drive A, and the user enters correct password, the system boots normally.	User Password	• Floppy writes are enabled. • Power and Reset switches are enabled. • Keyboard and mouse inputs are accepted. • System attempts to boot from drive A. If the user enters correct password, and drive A is bootable, the system boots normally
Password on boot User Password boot (AT style)	Power On/Reset	User Password set and password on boot enabled and Secure Boot Disabled in SSU	• System halts for User Password before booting. The system is not in secure mode. • Video is blanked (if enabled in SSU). • Floppy writes are disabled (if programmed so by SSU). • No mouse or keyboard input is accepted.	User Password	• Keyboard and mouse inputs are accepted. • The system boots normally. Boot sequence is determined by SSUoptions.
Diskette Access	Power On/Reset	Set feature to Admin in SSU	User is prevented from accessing the floppy drive. Administrator is always prevented from accessing the floppy drive.	Set feature to User in SSU	User is allowed to access the floppy drive.
Fixed disk boot sector	Power On/Reset	Set feature to Write Protect in SSU	Will write protect the boot sector of the hard drive to prevent viruses from corrupting the drive.	Set feature to Normal in SSU	Hard drive will behave normally.

4.3.2. Password Protection

Through the use of passwords, the BIOS prevents unauthorized tampering with the system. Once secure mode is enacted, access to the system is allowed only after you have entered the correct password(s). Each of two passwords, for User and Administrator, can be created during system configuration using the SSU .

Once secure mode is enacted, access to the system is allowed only after you have entered the correct password. Each password, User and Administrator, can be created during system configuration using the SSU . Once set, a password can be disabled by changing it to a null string. The Administrator password

can still modify the time and date, but other fields can only be modified if the user password is entered. For example, system hardware configuration can be controlled by the User password, while Administrator control access to the machine's file system. If only an administrator password is set (no User password), this password is requested when entering Setup and must be entered before the majority of the fields can be modified. If only the User password is set (no administrator password), the User password must be entered to access Setup, but all fields can be modified once entered.

Once set, a password can be disabled by changing it to a null string.

4.3.2.1. Inactivity timer

If the inactivity timer function is enabled, and no keyboard or mouse actions have occurred for the specified time-out period, the following occurs until the User password is entered:

- Keyboard and mouse input is disabled
- Video is blanked (if programmed in SSU)
- Floppy drive is write protected (if enabled)
- Front panel reset and power switches are locked (if enabled)
- A time-out period may be specified with the SSU .

4.3.2.2. Hot key activation

A Hotkey combination can activate secure mode immediately, rather than having to wait for the inactivity time-out to expire. The Hotkey combination is set using the SSU . The following keys are valid hot keys : A-Z, 0-9.

4.3.2.3. Password clear switch

The BIOS determines if the password clear jumper is set. If set, any passwords are cleared from CMOS and password protection is disabled.

4.3.3. Floppy Write Protection

If enabled by the SSU , floppy disk writes are blocked when the system is in secure mode. Floppy write protection is only in effect while the system is in secure mode. Otherwise, write protection is disabled.

4.3.4. Power Switch and Reset Button Lock

If enabled by the SSU , the power switch and reset button are disabled when in secure mode.

4.3.5. Secure Boot (Unattended Start)

Secure Boot allows the system to boot and run the OS. However, until the User password is entered, mouse and keyboard input is not accepted and the front panel reset/power switches are disabled. The SSUis used to place the system into secure boot mode. In secure boot mode, if the BIOS detects a floppy disk in the A drive at boot time, it prompts the User for a password. When the password is entered, the system can boot from the floppy and secure mode is disabled. Any one of the secure mode triggers cause the system to go back into secure mode. If there is no disk in drive A, the system boots from the next boot device and is placed in secure mode automatically. All of the enabled secure mode features go into effect at boot time.

4.3.6. Interaction with External Utilities

External utilities that need to perform password validation, such as SSU, can call the appropriate BIOS interface. The BIOS performs the password validation and returns the status. The interface is not described here for security reasons.

4.4. Auto-Configuration Features

The BIOS provides support for auto-configuration of the following:

- Plug and Play
- Processor speed
- SMP initialization
- Memory sizing
- Boot drive selection
- Mouse and keyboard swapping
- Pentium® II/ Pentium® III processor BIOS update
- LCD support

4.4.1. Plug and Play

The BIOS supports the following industry standards for full Plug and Play capabilities:

- Plug and Play (PnP) ISA specification
- Desktop Management Interface (DMI) BIOS specification
- Extended System Configuration Data Specification (EISA is not supported).
- PCI local Bus specification

4.4.1.1. Resource allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with other Intel servers. The BIOS scans for the following, in order:

1. ISA devices: If an ISA device is found, it is initialized and given resource priority over other devices of the same type plugged into the system.
2. Off board PCI devices: If found, the BIOS initializes and allocates resources to these devices.
3. On board Video, IDE, and SCSI devices: If equivalent functionality is not found off board, the BIOS allocates resources according to the parameters set up by the SSU.

4.4.1.2. PnP ISA auto-configuration

The BIOS:

- Fully supports the PnP ISA protocol
- Reads the PnP ISA configuration port
- Assigns the system I/O, memory, DMA channels, and IRQs from the resource pool
- The Super I/O* chip is an example of a PnP ISA device.

4.4.1.3. PCI auto-configuration

The BIOS supports the INT 1Ah, AH = B1h functions, in conformance with the PCI specification, Rev. 2.1. BIOS also supports the 16 and 32-bit protected mode interfaces as required by the PCI BIOS specification. System POST performs auto-detection and auto-configuration of ISA, ISA Plug-N-Play, and

PCI devices. This process maps each device into memory and/or I/O space, and assigns IRQs and DMA channels as required, so that there are no conflicts prior to booting the system. BIOS scans the PCI devices on each PCI bus in low to high sequence. The PCI busses are also scanned in the same order. The BIOS programs the PCI-ISA interrupt routing logic in MISSMIC to steer PCI interrupts to compatible ISA IRQs.

The BIOS detects the presence of I_2O compliant intelligent controllers, such as i960 RD and configures them as documented in the I_2O BIOS specification. The BIOS queries each I_2O IOP to find out if a PCI device is controlled by IOP and does not enable the devices under IOP control and does not allocate IRQ resources to such devices.

Drivers and OS programs can determine the installed devices and their assigned resources using the BIOS interface functions. The BIOS does not support devices behind PCI-to-PCI bridges that require mapping to the first 1 MB of memory space due to architectural limitation. (Refer *to PCI-to-PCI Architecture Specifications*). The User can override the IRQ assigned to a PCI card by using SSU.

4.4.1.4. Legacy ISA configuration

Unlike Plug-N-Play cards, legacy ISA cards do not provide any mechanism by which the BIOS can find out their resource requirements. Further, legacy ISA cards cannot be configured and require fixed resources. The SSU utility helps the user configure the Legacy ISA devices. The SSU utility allows the end user to reserve the Legacy ISA system resource and save the information into NVRAM. The POST resource management will not allocate the resources that are reserved for legacy ISA cards to PnP devices.

4.4.1.5. On board device auto-configuration

The BIOS detects all on board devices and assigns appropriate resources. The BIOS dispatches the option ROM code for the on board devices to DOS compatibility hole (C0000h to E7FFFh) and transfers control to the entry point. User may disable scanning of the on-board Symbios SCSI ROM using the SSU .

4.4.1.6. Automatic detection of video adapters

The BIOS looks for video adapters in the following order:

1. ISA
2. PCI
3. Baseboard

The on board (or off board) video BIOS is shadowed, starting at address C0000h, and is initialized before memory tests begin in POST. Precedence is always given to off board devices.

4.4.2. Multiple Processor Support

The BIOS supports one or two Pentium® II/ Pentium® III processors. The processors and IO APIC IRQ routing are described in a table specified in the next section. If only one processor is installed the other slot must be populated with a terminator. In a single processor system the APIC table and ACPI tables are dynamically updated to reflect the actual status of good processors in the system.

4.4.2.1. Multiprocessor specification support

The BIOS complies with all requirements of the Intel Multi-Processor Specification (MPS) version 1.4 for Symmetric Multi-Processor (SMP) support, as well as MPS version 1.1, for backward compatibility. The version number can be configured using the SSU . The base MP Configuration Table contains the following entries:

- MP table header
- Processor entries
- PCI bus entries
- I/O APIC entries
- I/O interrupt entries
- Local interrupt entries

The extended MP table is constructed if MPS version 1.4 is selected. It contains these entries:

- System address space mapping entries
- Bus hierarchy descriptor
- Compatibility bus address space modifier entries
- Note: The MP APIC table and ACPI table are the only places where the number of processors are dynamically reported from boot to boot.

4.4.2.2. Multiple processor support

On reset, the Primary Processor is selected by the BMC to become the BootStrap Processor (BSP). The slot labeled Primary CPU will always be examined first. If a serious error is detected during Built-In Self Tests (BIST), that processor does not participate in the initialization protocol and the Secondary processor then becomes the BSP and the Primary is halted and removed from the MP table. Whichever processor successfully passes BIST is automatically selected by the hardware as the BSP and starts executing from the reset vector (F000:FFF0h). A processor that does not perform the role of BSP is referred to as an Application Processor (AP).

The BSP is responsible for executing POST and preparing the machine to boot the OS. BIOS performs several other tasks in addition to those required for MPS support. These tasks are part of the fault resilient booting algorithm. At the time of booting, the system is in virtual wire mode and the BSP alone is programmed to accept local interrupts (INTR driven by the PIC and NMI). As a part of the boot process, the BSP wakes up the APs. When woken up, the AP programs its memory type range registers (MTRRs) so that they are identical to those of the BSP. All APs execute a halt instruction with their local interrupts disabled.

4.4.2.3. Multiple Processor speed support

The BIOS supports different steppings of Pentium® II/Pentium® III processors as long as they are within 1 release of each other. Both processors must be of the same cache size. Two processor modules of different operating frequency are allowed within a single system configuration however the system will only operate reliably at the slower of the two. All installed processors must run at the same frequency (for example, the bus and core frequencies of all processors must be identical). Also, for best performance, all processors must be of the same CPU ID.

The type and speed of all detected processors are also reported by the SSU .

4.4.3. Memory Sizing

During POST the BIOS:

- Tests and sizes memory
- Configures the memory controller

Nightshade supports various size and configurations of ECC SDRAM DIMMS. Memory sizing and configuration are only guaranteed for qualified DIMMs approved by Intel. The BIOS gathers all type, size, speed and memory attributes from the on-board EEPROM or SPD on the memory DIMM. It is required that the memory be stuffed from the lowest DIMM socket to the highest for the memory to work in all configurations over the full environmental range of the server.

The memory sizing algorithm determines the size of each row of DIMMs. The BIOS reads the DIMM speed information and programs the PAC accordingly. BIOS does not perform the extended memory test if instructed by the user via SSU . Disabling the extended memory test reduces the boot time. In any case, the BIOS always initializes ECC memory. The BIOS is capable of detecting, sizing, and testing any amount of RAM, up to the physical maximum of 1 GB. The BIOS is capable of reporting up to 64 MB using INT 15h, AH = 88h, or INT 15h, function E801h, which can report up to 4,096 MB. INT 15h, function E820h supports reporting of the system memory regions.

4.4.4. Boot Device Selection

The BIOS conforms to the Phoenix BIOS boot specification 1.01. The BIOS boot specification describes a method where the BIOS identifies all Initial Program Load (IPL) devices in the system, prioritizes them in the order the user selects, and then sequentially goes through each device and attempts to boot. It is possible to use the SSUto change the boot order of devices connected to the system. In the case where the order has been changed by a user, the system boots in the order chosen, with the exception of legacy devices. Legacy devices are those devices that tend to take control of the boot process altogether by hooking boot vector (interrupt 19h). Further, they provide no means for identifying themselves as an IPL device. Therefore, the BIOS cannot selectively boot from one of several Legacy IPL devices in a system. The user can choose whether the first boot device is a floppy, a CDROM, a hard drive, an I_2O device through SSU . The system BIOS will try and boot from devices in the order specified by the user. Further, the user can reorder the hard drives and choose the C: drive to be any IDE drive or any drive that is controlled by a Boot BIOS Specification compliant option ROM BIOS, such as the on-board Symbios BIOS. Hard drives that are controlled by all other controllers will appear as ‘Other bootable cards” in the setup menu, and the user cannot control the order on drive by drive basis for such controllers. Some boot BIOS compliant option ROM BIOS’s may present all the drives as a single device, and may not allow the user to manipulate the order on a drive by drive basis. The user is responsible for making sure that the C: drive has a bootable image, if booting from a hard drive.

4.4.5. Mouse and Keyboard Swapping

The BIOS allows users to swap the keyboard and PS/2 mouse connectors before system the is powered on. It detects the combination during POST and initializes the KBC accordingly. Hot plugging of the mouse and keyboard is not supported by Nightshade and may have unpredictable results.

4.4.6. Pentium® II/Pentium® III Processor BIOS Update API

The Pentium® II/Pentium® III processor has the capability to correct specific errata through the loading of an Intel supplied data block. The Pentium Pro processor BIOS update specification defines a way of incorporating future releases of such data block (also called the “update”) into a system BIOS. The BIOS is responsible for storing the update in a non-volatile memory block and loading it into each Pentium II/ Pentium III processor during POST sequence. The Pentium Pro processor BIOS update specification requires the system BIOS to implement function calls to read the update and overwrite the existing update with a new release. These functions can be accessed from real mode by executing INT 15 with AX=0xD042. The corresponding 16-bit protected mode interface is not implemented. BIOS performs all the recommended security checks before validating an update.

4.4.7. Boot Without Keyboard

The system can boot with or without a keyboard. There is no entry in the SSU for keyboard enable/disable. The presence of the keyboard is detected automatically during POST, and the keyboard is tested if present. The BIOS will not detect or use USB keyboards.

4.5. Performance Features

For enhanced performance, the BIOS sets up the L2 cache controller for the Pentium® II/ Pentium® III processor and performs option ROM shadowing.

4.5.1. L2 cache initialization

There are differences between the Pentium® II/Pentium® III processor cache implementation and previous Intel processor architectures. To boost system performance, the Pentium II/Pentium III processor contains an L2 cache and cache controller; which previously had been handled by external devices. BIOS programs L2 cache controllers of each processor in a manner that is consistent with the other processor and the PCIset.

L2 cache is tested as a part of the Pentium II/Pentium III processor BIST. If L2 cache is bad, the Pentium II/ Pentium III processor indicates the error in the BIST and the BIOS disables the Processor. The BIOS detects the cache size and cache type (ECC or non-ECC), and programs the cache controller accordingly before performing any cache operations. The BIOS displays a warning message on the screen if the two processors have different cache sizes. Not all bus to core ratio settings support L2 cache being on. Some bus to core ratios are not allowed by the processor and the BIOS will disable the cache accordingly with the registers in the processor.

4.5.1.1. Cache state on boot

The BIOS looks at a bit in CMOS to determine if the system caches should be enabled or disabled. The user can modify the bit in the Boot Options of the Setup Main menu. If the cache is enabled, cache controllers in all Pentium II/ Pentium III processors are initialized in a consistent manner with each other and the 82440BX PCI Set.

4.5.2. Option ROM Shadowing

All on board adapter ROMs (stored in compressed form in the system Flash ROM), and PCI adapter ROMs are shadowed into RAM in the ISA-compatible ROM adapter memory space between C0000h to E7FFFh. The BIOS ROM found on ISA devices are shadowed (if capable) into adapter memory space in the same range after initialization. Shadowing for ISA devices can be disabled for various regions using the SSU . PCI BIOS ROMs are always shadowed. Typically the onboard video bios is shadowed at C0000h.

4.5.3. Memory speed optimization

The BIOS detects the system memory speed and bus speed and optimizes the memory controller for the best performance.

The system bus speed can be detected by the processor internal speed and the bus ratio. The memory DIMM speed can be detected by its ID. Using this information the BIOS can set up the memory controller register for the best performance.

4.5.4. PCIset performance optimization

The BIOS detects the system configuration, such as board ID, PCIset stepping, processor stepping, and optimizes the PCIset for the best performance. Most of the PCIset registers are automatically. The bios no longer supports 1 Megabyte holes at 15-16 Megabyte memory regions. The user may be allowed to control a limited number of performance features. It is not recommended for the user to change any of the default PCI timing settings.

4.6. Reliability Features

The BIOS supports several features to create a robust computing environment including the following:

- ECC memory and defective DIMM handling
- Fault resilient booting
- Logging of critical events
- I^2C system management bus
- CMOS default override
- Emergency Management port

4.6.1. Defective DIMM detection and remapping

The ECC memory subsystem on N440BX is able to detect single-bit errors (SBE) and certain multi-bit errors (MBE) during reads from and writes to system DRAM. Single-bit errors can be detected and corrected. Certain patterns of MBEs can be detected but cannot be corrected, whereas other types of MBEs cannot be detected.

During POST memory testing, detection of single-bit and multi-bit errors in DRAM banks is enabled. Any error is avoided by reducing the usable memory in that bank so that the byte containing the hard error is no longer accessible. This is done automatically by the BIOS during POST and does not require any user intervention. The BIOS logs the errors in the nonvolatile system event log. The BIOS detects the speed of individual DIMMs. The BIOS disables a DIMM that is slower than what the hardware requires and displays a warning message.

4.6.1.1. Memory configuration algorithm

The algorithm for determining memory configuration is as follows:

If there is no DIMM population, or the DIMMs are all bad, or have the wrong speed, the BIOS sounds a beep code error and POST is terminated. The BIOS requires at least 4 MB of good memory for POST to start up. The BIOS individually probes each bank for the size of installed DIMMs. The BIOS detects the speed and type of the DIMM SDRAM and programs the PCIset accordingly. If the bank does not match one of the allowable configurations, the BIOS reports the error with an error message. EDO memory is not physically supported due to the memory socket used on the baseboard. Non ECC memory will be supported but not tested or validated by Intel. The BIOS will automatically shut off all ECC capability for the system if detected. All configuration data for the memory DIMMs is gathered by the BIOS from the SPD or EEPROM on the DIMM. This is done via the SMBUS interface on the PIIX4.

In the event that the BIOS disables or resizes a bank, an error message displays with the DIMM number of the failing memory. Another message informs the user that the amount of usable memory in that bank is being reduced to eliminate the failing location. Eliminating hard errors in this way during POST is done as a precaution to prevent an SBE from becoming an MBE after the system has booted and to prevent SBEs from being detected and logged each time the failed location(s) are accessed. This is recorded in the SEL (System Event Log) at both post time as well as runtime with an SMI. See the Server management specification for the format of the memory errors in the SEL. This is implemented as an EEPROM that the BMC can access directly with the server on or off.

If the error is an SBE, the 440BX automatically corrects the data before it is returned to memory. The 440BX memory controller scrubs the memory location where the error occurred to correct the SBE and

the BIOS will record the SBE via an SMI to the SEL. If the error is an MBE, this condition is considered fatal, and after the error is logged, an NMI is generated, telling the OS to handle this fatal error.

4.6.1.2. ECC Memory Initialization

The system BIOS handles ECC memory initialization. All memory locations, including System Management RAM and shadow memory region, are unconditionally initialized during POST (set to 0). Error detection is disabled while ECC memory is initialized to prevent false alarms caused by un-initialized memory bytes. If hard errors are detected during the memory test, the memory partition containing the errors is resized to eliminate the failing locations.

4.6.1.3. ECC and SMI support

During normal operation, any SBEs (single bit errors) are detected and are handled by the SMI support code. The SMI code logs the SBE, keeping up to 3 records of the last SBE logs in the system event log. The 440BX memory controller cannot locate the exact address of the error, but can only point to the row that contains the error location. Scrubbing is always automatically enabled when ECC memory is detected. The row containing the failing location is scrubbed by reading the corrected data and writing back the correct data automatically by the memory controller. If read from shadow memory results in an SBE, the BIOS must enable writes to that area, scrub the locations and disable writes. Scrubbing helps to prevent a single-bit correctable error from turning into multiple-bit errors in the future. Scrubbing an entire row is a time consuming operation and might affect correct functioning of certain operating systems. If MBEs are detected, the BIOS SMI handler will log an event into the SEL (System Event Log) and then generate an NMI to the OS. This is part of the server management control functions which the BMC provides with its non-volatile storage device (available out of band).

The ECC memory feature may be disabled if significant performance increase is measured in the Platform. The BIOS setup will provide a switch to disable ECC memory. The default will be for ECC to be enabled. This switch will disappear in the shipping release if the performance is not deemed significant.

4.6.2. Fault Resilient Booting (FRB)

The BIOS and firmware provides a feature to guarantee that the system will boot even if one processor fails during POST or hangs while booting to the O/S. The BMC contains 2 watchdog timers that if they trip will reset the system. The first timer(FRB-3) starts counting down whenever the system comes out of hard reset and usually is about 5 seconds. If the BSP successfully resets and starts executing the BIOS will disable the FRB-3 timer in the BMC and system will continue on with POST. If the timer expires because of the BSP's failure to fetch or execute BIOS code, the BMC resets the system and disables the failed processor. The system will continue to reset alternating BSP's between the primary and secondary processor socket until the BIOS POST gets past disabling the FRB-3 timer in the BMC.

The second watchdog timer(FRB-2) in the BMC is set to 5-6 minutes and is designed to guarantee that the system will complete BIOS POST. Near the end of POST, before the options ROMs are initialized, the BIOS will disable the FRB-2 timer in the BMC. If the system hangs during POST, the BIOS will fail to disable the timer in the BMC which generates an ASR (Asynchronous System Reset).

In a dual processor system the BIOS will register the AP in the MP table. When started by the BSP, if an AP fails to complete initialization within a certain time, it is assumed to be non-functional. This AP is not listed in the MP table (refer to the *MP Specifications, Rev. 1.4*) and is invisible to the OS. If either processor fails the BIST (Built-In Self Test) it is marked bad and removed from the MP table. The BIOS will disable the processor and reset the system to make sure the failed processor will be electrically disabled on the next boot.

The BMC maintains a flag bit in non-volatile ROM for each processor. This bit is used to store a processor's track record. It is set whenever a processor fails and remains so until the user forces the system to retest the processor and it successfully makes it past both FRB timers. The BIOS reminds the user about a previous processor failure during each boot cycle and keeps that processor disabled until the status flag is cleared by the user. Processors that have failed in the past are not allowed to become the BSP[3], and are not listed in the MP table. It might happen that all the processors in the system are marked bad. An example is a uniprocessor system where the processor has failed in the past. If all the processors are bad, the BIOS does not alter the BSP and attempts to boot from the original BSP. It also informs the user that it is trying to boot from a failed processor if the POST gets executed. Error messages are displayed on the console, errors are logged in the event log if a processor fails. The failed processor is identified by its number.

If the user replaces a processor marked bad by the BIOS, the system BIOS must be informed about this change by running BIOS setup and selecting that processor to be re-tested. If a bad processor is removed from the system, the BMC automatically detects this condition and clears the status flag for that processor.

There will be 4 choices for each slot that the user is presented in BIOS setup for processor status:

1.) processor installed (user may not select this, indicates processor has passed BIOS POST)

2.) processor failed (user can force this to disable for a questionable processor or the processor may have failed FRB-2, FRB-3 or BIST and the BIOS is removing it from the system).

3.) processor not installed (user selects this option in the BIOS setup to notify the system that the processor is not present in that slot and a terminator has been placed in it).

4.) force retest (used to add a new processor to the system. Next reboot BIOS will test the processor and will go to state "processor installed" if it passes FRB-3,FRB-2 and BIST. Also used to force re-testing of processors marked as failed.)

Conditions BIOS will automatically force a retest on a processor.

1.) if a processor was added to the system that was previously marked as not installed

(replacing a terminator card with a processor).

2.) CMOS was cleared.

3.) FRB-3 or FRB-2 timer tripped and the system rebooted.

4.) failed BIST on a processor

The BIOS will not automatically re-test a processor that was previously marked as failed. It cannot tell that a new processor has been added since it will not re-test the processor until the user has marked it so. The BIOS will report to the screen that a processor has failed and will continue to do so until the user either marks it as failed or marks it as not installed and removes it.

Removing a processor and replacing it with a terminator module when it previously was marked as installed will cause the BIOS to indicate that it is no longer installed.

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[3] Since BSP selection is done in hardware by Pentium® II/ Pentium® III processors, it may be possible for a processor that has failed in the past, or one that has failed BIST to become the BSP. The BIOS can detect such conditions and transfer BSP ownership to another "good" processor, if available.

Any one of the failures (FRB-3, FRB-2 and BIST) are recorded to the BMC server event log. The processor (s) that failed are recorded as well.

If the FRB jumper on the baseboard is set to disable the frb-3 and frb-2 timer shall never time-out. This effectively disables all FRB time-out features on the baseboard.

4.6.3. Logging System events

If enabled by the configuration utility or BIOS setup, the BIOS can log critical and informational events to nonvolatile memory. This area is managed by BMC and can be accessed by sending commands to BMC. A Critical event is one that might result in the system being shut down to prevent catastrophic side effects from propagating to other parts of the system. Multi-bit and parity errors in the memory subsystem are considered critical errors, as are most errors that generate a Non-Maskable-Interrupt (NMI), which might subsequently generate a System Management Interrupt (SMI). These errors include I/O channel check, software generated NMI, and PCI SERR events.

During POST, the BIOS initializes System Management RAM (SMRAM) with error handling and logging code. Each processor has a private area of SMRAM dedicated to it for SMI processing. The DRAM controller and PIIX4 are programmed to generate an SMI for PCI SERR, software generated NMI, I/O channel check, and ISA watchdog time-out and NMIs generated by the PAC. The PAC generates an SERR if parity/ECC errors are observed in the memory subsystem. The PAC generates an interrupt if a single-bit correctable error is observed in the memory subsystem. The PIIX4 can be programmed to generate an SMI on this interrupt. When these errors are detected, the SMI routines log the error or event in a manner that is transparent to the OS and then causes an NMI to be generated for certain events, so that the OS can respond appropriately. The BIOS also logs an event on another type of memory error called Single Bit Error (SBE). For this error, the BIOS will not generate an NMI to the OS. BMC may independently log events and is responsible for serializing accesses to the area.

If the OS device driver is using the watchdog timer to detect software or hardware failures and that timer expires, an Asynchronous Reset (ASR) is generated, which is equivalent to a hard reset. The POST portion of the BIOS can query BMC for watchdog reset event as the system reboots, and logs this event to the logging area. Failure of a processor during POST will also be logged in the Flash during POST.

4.6.3.1. I^2C Diagnostic Bus (Intelligent Management Bus)

The I^2C interface on the baseboard provides an independent interconnect between various devices in the system (for example, memory subsystem, processor subsystem, etc.), for diagnostic or other purposes normally unavailable to the system. The I^2C bus acts as system management bus and carries information about system events. The BIOS must go through the BUD interface of BMC in order to send messages to I^2C devices and receive messages. The BMC is accessible to the processor at I/O addresses 0CA0-0CA3 on the ISA bus. The BMC acts as a gateway to other I^2C devices.

4.6.4. Emergency Management Port (EMP)

Nightshade provides a communication serial port with the BMC. A multiplexer which is controlled by the BMC determines if the COM2 external connector is attached to the BMC or the standard serial port in the Super I/O*. The following features are available over this port:

- System power control (on/off remotely)
- Access to the event log, system serial no. and model no. and sensor data logs in the BMC
- System reset

- NMI control
- Allows BIOS console redirection through the BMC serial port
- Password security protection for EMP serial port
- Access to status of real time events in BMC

Multiplexer configuration on COM2 connector

The BIOS supports 4 different modes which the EMP can be configured for in F1 BIOS setup:

Disabled:

COM2 is connected to the Super I/O* and never is connected to the BMC. COM2 acts like a serial port on a normal system.

Pre-boot only:

Only available when the machine is powered down and during post. If the BIOS is setup in this mode the multiplexed for COM2 is connected to the BMC during post and when the machine is off and on standby power. This requires that AC power be connected to the system. Just before boot to O/S (Int 18,19) the BIOS will switch the multiplexer via BMC command on its ISA interface over to the standard Super I/O* COM2 port. The O/S or server management drivers may at anytime submit commands to the BMC to switch the multiplexer back.

Always Active:

COM2 is dedicated to the serial port on the BMC. COM2 is removed from the system resources available to the O/S and BIOS. Baud rate is fixed by the BMC at 19200 baud. The BIOS does not send any commands to the BMC for this mode regarding EMP.

Security:

The EMP allows password security similar to the BIOS password security. In the F1 BIOS setup, the user may select a password which will be downloaded to the BMC during setup. The BMC will wait until the password is submitted to the serial port. System power down, reset and NMI control are unavailable until this password is submitted. The EMP security only effects security to the BMC services and does not impact any other BIOS or O/S services in the system.

BIOS will download all configuration information such as password and operation mode on saving of the BIOS setup screen (F10) to the BMC via the ISA interface.

BIOS console redirection

If the option in the BIOS for console redirection is turned on for COM2 there are some added functions allowed if the BMC EMP is setup for “Always active” or “Pre-boot” mode.

Escape characters for multiplexer control of COM2 port. The BIOS console redirection will support an extra control escape sequence to force COM2 port over to the BMC. Once this command is sent, the COM2 port will be attached to the BMC EMP serial port and the Super I/O* COM2 data will be ignored. This feature is available to the remote user to allow them to monitor the status of POST as the BIOS comes up over COM2 and then take control of the system reset or power from the BMC. If the system does not come up a watchdog time-out feature in the BMC will automatically switch the port over in case the system does not make it through POST.

The character sequence will be "**ESC O 9**"(also denoted as ^[O9) to switch the multiplexer to the BMC serial port. This key sequence is above the normal ANSI function keys and will never be used by an ANSI terminal.

A restriction of using COM2 for both EMP with BIOS console redirection is that the baud rate is fixed to 19200 baud and the port is setup for N,8,1 Xon/Xoff.

See the section on Console Redirection for further details on how it works.

Modem support on EMP

BIOS setup will also provide a field for modem setup to the BMC. The BMC will be responsible for controlling the modem if it is attached to COM2 since the BMC will always have control of COM2 before system reset .

4.7. Console Redirection

The BIOS supports redirection of both video and keyboard via a serial link (COM 1 or COM 2). When console redirection is enabled, local (Host Server) keyboard input and video output is passed both to the local keyboard and video connections, and to the remote console via the serial link. Keyboard inputs from both sources are considered valid and video is displayed to both outputs. Optionally, the system can be operated without a host keyboard or monitor attached to the system and run entirely via the remote console. Both Setup and the SSU can be accessed via console redirection. This feature is only designed to work with BIOS POST and DOS in standard text mode since most operating systems today no longer use real mode BIOS calls to communicate to the keyboard and video. This feature was intended to allow remote operation of the server for BIOS setup and the SSU. It is not tested or maintained under any other software.

4.7.1. Operation

When redirecting through a modem (as opposed to a Null modem cable), the modem needs to be configured with the following:

1. Auto-answer (for example, ATS0=2, to answer after 2 rings)
2. Modem reaction to DTR set to return to command state (for example, AT&D1)
3. Failure to provide #2 above causes the modem to either drop the link when the Server reboots (as in AT&D0), or make the modem unresponsive to Server baud rate changes (as in AT&D2).

The BIOS Setup/SSU option for handshaking must be set to CTS/RTS + CD. The CD refers to Carrier Detect. In selecting this form of handshaking, the Server is prevented from sending video updates to a modem that is not connected to a remote modem. If this is not selected, video update data being sent to the modem disables many modems from answering an incoming call.

Once Console Redirection is selected via BIOS Setup or SSU, redirection is loaded into memory and activated during POST. While redirection cannot be "removed" without rebooting, it can be disabled and restarted. When disabled, the serial port is released by redirection and might be used by another application. Restarting reclaims the serial port and continues redirection. Disabling/restarting is accomplished through the following INT 16h mechanism. The standard INT 16h (Keyboard handler) function ah=05h places a keystroke in the key buffer, just as if an actual key had been pressed. Keystrokes so buffered are examined by redirection, and if a valid command string has been sent, it is executed. The following commands are supported in this fashion:

Esc-CDZ0 - Disable Console Redirection.

Esc-CDZ1 - Restart Console Redirection.

In order to disable redirection, the software must call INT 16h, function ah=05h five times to place the five keys in the key buffer. Keystrokes sent to the INT 16h buffers for purposes of invoking a command are buffered, and should be removed via the normal INT 16h calls to prevent these keystrokes from being passed on to another application. This feature was intended to allow downloading of files via Zmodem or Xmodem to the host server system from the remote target. BIOS iFlash update or the SSU could be downloaded to the host system in this manner and run remotely. This allows remote upgrade of the system software.

4.7.2. Limitations

Console redirection is a Real Mode BIOS extension, and does not operate outside of Real Mode. Console redirection does not work once the OS or a driver like EMM386 takes the processor into protected mode. If an application takes the processor in and out of protected mode, it should disable redirection before entering protected mode and restart it once back into real mode. Video is redirected by scanning and sending changes in text video memory. Thus, console redirection is unable to redirect video in graphics mode. Keyboard redirection functions via the BIOS INT 16h handler. Software bypassing this handler does not receive redirected keystrokes.

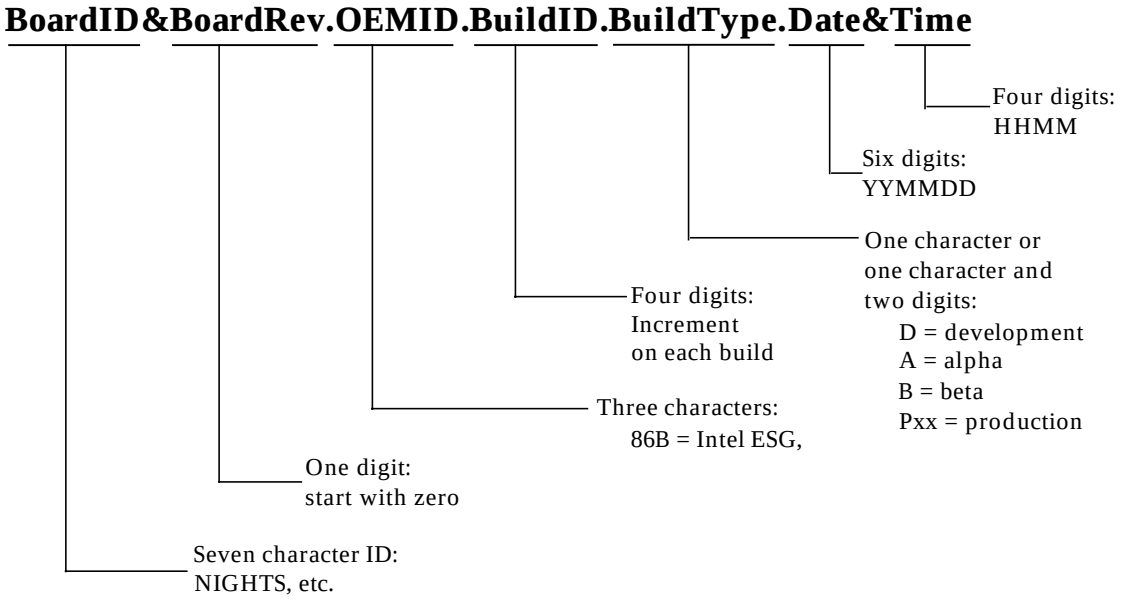
4.8. BIOS Revision History Format

The BIOS Revision Identification is used to track board, OEM, and build revision information for any given BIOS. This identifier can be a maximum of 32 characters. The first 28 characters have been defined using the following format:

The figure below illustrates a standard 32-byte BIOS ID.

EXAMPLE:

NIGHTS0.86B.0057.P06.9809040810



5. System Setup Utility / Configuration Utility

This chapter describes the Configuration Utilities that provide the means to configure on board resources and add-in cards. The utilities are provided in two forms: the diskette-loadable SSU and the ROM-resident BIOS Setup utility. The following topics are covered here:

- Configuration utilities overview
- Configurable options
- BIOS Setup utility operation
- Configuration CMOS RAM definition

5.1 Configuration Utilities Overview

Configuration of on board devices is done using the BIOS Setup utility embedded in Flash ROM. Setup provides enough configuration functionality to boot a system diskette, shipped with the hardware, that contains the SSU. The booted SSU is required for configuration of PCI and ISA add-in cards. The SSU is released on diskette or CDROM. Setup is always provided in Flash for basic system configuration.

The SSU is PCI-aware and conforms to the ISA Plug and Play Specification version 1.1. The SSU works with any compliant CFG or OVL files supplied by the peripheral device manufacturer. Intel supplies only the OVL and CFG files for the system baseboard.

The configuration utilities modify the CMOS RAM and NVRAM, under direction of the user. The actual hardware configuration is accomplished by the BIOS POST routines and the BIOS Plug-N-Play Auto-Configuration Manager. The configuration utilities always update a checksum for both areas, so that any potential data corruption is detectable by the BIOS, before actual hardware configuration takes place. If the data is corrupted, the BIOS requests that you configure the system before the system is rebooted.

If the disk-based SSU is used, a logo is automatically displayed before the SSU is executed. The logo can be customized by the OEM.

5.2 Configurable Options

The following table defines most of the configurable options available in the SSU. More options may also be supported.

Note that the BIOS detects the state of the “CMOS default” jumper (on the baseboard). If set prior to power-on or hard reset, the BIOS changes CMOS and NVRAM settings to their default state. This guarantees the system’s ability to boot from floppy (CMOS clear) to execute the SSU. The default values are **highlighted**.

Table 5-1 Configurable SSU Options (Part 1)

Group	Configuration Feature	Selection Options	Notes
System Identification and Version Information			
	Config and Overlay Version	N/A	Display only
	BIOS Version	N/A	Display only
	MP Spec. Version	**1.1**/1.4	
System Processor Modules	Display Processor Type(s) and Speed(s) based on position	N/A	Display only
System Processor Status	Processor Status for each processor based on position	**Pass**/Failed	The status automatically changes to "failed" if the BIOS detects a processor failure. The user can change the status either way by SSU. A "failed" processor remains disabled in next boots until the user changes the status to "Pass" or the system is booted with the processor removed.
Memory Shadowing	Shadowing ISA ROM	**Enable** /disable	Independent controls for each 16KB block between C0000 and E7FFF
Extended Memory options (cache/1MB ISA hole)	Extended Memory size /Cache Size	N/A	Display only Press enter to enable/disable cache and extended memory hole
On board Disk	On board Floppy Controller	**Enable** / Disable	
Controllers	On board IDE Controller	**Enable** / Disable	
On board Communications	Serial Port 1 Configuration	Serial port 1 Address and IRQ	
Devices	Serial Port 2 Configuration	Serial Port 2 Address and IRQ	
	Serial Port 2 mode	**Normal / EMP mode**	
	Parallel Port Configuration	Parallel Port Address and IRQ	
	Parallel Port Mode	Output Only parallel port / Bi-directional parallel port / Enhanced Parallel printer port / **Extended capabilities parallel port, DMA 1** / Extended capabilities parallel port, DMA 3	Select parallel port mode
Floppy Subsystem	Floppy drive A Options	Disabled/360K/720K/**1.44M**/2.88M	Default is 1.44 MB
	Floppy drive B Options	**Disabled**/360K/720K/1.44M/2.88M	

Table 5-2. Configurable SSU Options (Part 2)

IDE Subsystem			
IDE configuration - Primary master	Configuration selection	None/User/**Auto**/CD	For slave device on IDE channel
	Multi-sector transfer selection	2 sectors per Block / 4 sectors per block / 8 sectors per block / 16 sectors per block / **None** ,	
	Translation Mode	Standard CHS/ **Logical Block Addressing**	
	Transfer mode	**Standard**/PIO 1/ PIO 2/ PIO 3 / PIO 4	
IDE configuration - Primary slave	Configuration selection	None/User/**Auto**/CD	For slave device on IDE channel
	Multi-sector transfer selection	2 sectors per Block / 4 sectors per block / 8 sectors per block / 16 sectors per block / **None** Drives Primary Master/Slave,	
	Translation Mode	Standard CHS/ **Logical Block Addressing** Drives Primary Master/Slave, C:, D:	
	Transfer mode Fast Programmed I/O modes	**Standard**/PIO 1/ PIO 2/ PIO 3 / PIO 4 Drives Primary Master/Slave, C:, D:	
Multiboot Group menu			
	IPL devices	Diskette drive Hard Drive ATAPI CDROM drive I2O devices Diagnostic boot	Press plus/minus keys to change the boot order
	BCV devices	List of up to 8 BCV devices	Choose the ordering of hard drives (refer to 0)
Console Redirection	Serial port	**Disable** / Port 1/Port 2	
	Baud rate	2400/ **9600**/ 19.2k/ 115.2k	
	Hardware flow control	**None** / CTS-RTS / Xoff-Xon	
	Terminal Type	PC ANSI/VT 00	
Security Subsystem	Administrative Password	Press enter to change the password	Not prompted for a password since administrative password is already validated before entering this menu
(Refer to “Security Features” in section 0)	User Password	Press enter to change the password	Requires that the current password be entered before it is changed

	Secure Mode Hotkey	Ctrl-Alt-key or None	This is the key to press with Ctrl-Alt keys to enter secure mode immediately. Valid keys are A-Z, 0-9
	Secure Boot Mode	Enable / **Disable**	
	Video Blanking	Enable / **Disable**	
	Reset Button and Power Switch Locking	Enable / **Disable**	Firmware/bios only supports enable.
	Keyboard Inactivity Timer	**2 min**/ 5 min. / 10 min / 20 min / 1 hr / 2 hr	
	Floppy Writes During Secure Mode	Enable / **Disable**	
	Password on boot	**Disabled**/Enabled	
On board SCSI Subsystem	On board SCSI ROM Scan	**Enable** / Disable	All on board SCSI fully configured, but ROM scan skipped if disabled
Language Support	Language Support options	**English**/Italian/Spanish/ French/German	OEM may replace any of these languages with another
Keyboard/Mouse	NumLock State at Boot	**On** / Off	
Subsystem	Typematic Speed	Slow / **Medium** / Fast	
	Mouse Control	**Enabled**/Disabled	

Table 5-3 Configurable SSU Options (Part 3)

Server Management			
System Management Options	SMM Enable	Enable / **Disable**	
	Event Logging	Enable / **Disable**	Controls on board event logging.

5.3. Setup Utility Operation

The ROM-resident Setup utility configures only on board devices. Configuration of added PCI or ISA cards requires the use of the diskette-loadable SSU.

The Setup utility screen is divided into four functional areas:

Keyboard Command Bar — Located at the bottom of the screen. This bar displays the keyboard commands supported by the Setup utility.

Menu Selection Bar — Located at the top of the screen. Displays the various major menu selections available to the user. The Server Setup utility major menus are: Main Menu, Advanced Menu, Security Menu, Server Menu, Boot Menu, and the Exit Menu.

Options Menu — Each Options menu occupies the left and center sections of the screen. Each menu contains a set of features. Selecting certain features within a major Options menu drops you into sub-menus.

Item Specific Help Screen — Located at the right side of the screen is an item-specific Help screen.

5.3.1. Entering Setup Utility

During POST operation, the user is prompted to enter Setup using the F2 function key as follows:

```
Press <F2> to enter Setup
```

Note that a few seconds might pass before Setup is entered. This is the result of POST completing test and initialization functions that must be completed before Setup can be entered. When Setup is entered, the Main Menu options page is displayed.

5.3.2 Keyboard Command Bar

The bottom portion of the Setup screen provides a list of commands that are used for navigating the Setup Utility. These commands are displayed at all times, for every menu and sub-menu.

Each Setup menu page contains a number of features. Except those used for informative purposes, each feature is associated with a value field. This field contains user-selectable parameters. Depending on the security option chosen and in effect via password, a menu feature's value can be changeable or not. If a

value is non-changeable due to insufficient security privilege (or other reasons), the feature's value field is inaccessible. The Keyboard Command Bar supports the following:

F1 Help

Pressing F1 on any menu invokes the general Help window. This window describes the Setup key legend. The up arrow, down arrow, Page Up, Page Down, Home, and End keys scrolls the text in this window.

Enter Execute Command

The Enter key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected feature has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the Enter key will undo the pick list, and allow another selection in the parent menu.

ESC Exit

The ESC key provides a mechanism for backing out of any field. This key will undo the pressing of the Enter key. When the ESC key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered. When the ESC key is pressed in any sub-menu, the parent menu is re-entered. When the ESC key is pressed in any major menu, the Exit menu page displays.

↑ Select Item

The up arrow is used to select the previous value in a pick list, or the previous feature in a menu item's option list. The selected item must then be activated by pressing the Enter key.

↓ Select Item

The down arrow is used to select the next value in a menu item's option list, or a value field's pick list. The selected item must then be activated by pressing the Enter key.

↔ Select Menu

The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed.

- Change Value

The minus key is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list.

+ Change Value

The plus key is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list.

F9 Setup Defaults

Pressing F9 causes the following to appear:

Setup Confirmation
Load default configuration now? [Yes] [No]

If the “Yes” is selected and the Enter key is pressed, all Setup fields are set to their default values. If “No” is selected and the Enter key is pressed, or if the ESC key is pressed, then you are returned to where you were before F9 was pressed without affecting any existing field values.

F10 Save and Exit

Pressing F10 causes the following message to appear:

Setup Confirmation
Save Configuration changes and exit now? [Yes] [NO]

If “Yes” is selected and the Enter key is pressed, all changes are saved and Setup is exited. If “No” is selected and the Enter key is pressed, or the ESC key is pressed, you are returned to where you were before F10 was pressed without affecting any existing values.

5.3.3 Menu Selection Bar

The Menu Selection Bar is located at the top of the screen. It displays the various major menu selections available to the user:

- Main Menu
- Advanced Menu
- Security Menu
- Server Menu
- Boot Menu
- Exit Menu

These and associated sub-menus are described below.

5.3.3.1 Main Menu Selections

The following tables describe the available functions on the Main Menu, and associated sub-menus. Default values are highlighted.

Table 5-11. Main Menu Selections

Feature	Option	Description
System Time	HH:MM:SS	Set the System Time.
System Date	MM/DD/YYYY	Set the System Date.
Legacy Diskette A: Legacy Diskette B:	Disabled,360KB, 720KB, 1.44 MB, 2.88 MB	Select the floppy diskette type.
Primary IDE Master	N/A	Selects sub-menu.
Primary IDE Slave	N/A	Selects sub-menu.
Secondary IDE Master	N/A	Selects sub-menu.
Secondary IDE Slave	N/A	Selects sub-menu.
Keyboard Features	N/A	Selects sub-menu.
Memory Cache	**Enabled**, Disabled	Enables Pentium® II/ Pentium® III Processor Cache
CPU speed	200/250/300/350 /400/450/500	Selects processor speed when the processor speed jumper is in program position. Display only field, when the processor speed jumper is in protect position.
Language	**English (US)**, Spanish, Italian, French, German	Selects which language BIOS displays.

Table 5-12. Primary IDE Master and Slave Adapters Sub-menu Selections

Feature	Option	Description
Type	**Auto** None CDROM User	Auto allows the system to attempt auto-detection of the drive type. None informs the system to ignore this drive. CDROM allows the manual entry of fields described below. User allows the manual entry of all fields described below.
Cylinders	1 to 9999	Number of Cylinders on Drive. This field is only changeable for Type User. This field is informational only, for Type Auto.*
Heads	1 to 16	Number of read/write heads on Drive. This field is only available for Type User. This field is informational only, for Type Auto.*
Sectors	0 to 63	Number of Sectors per Track. This field only available for Type User. This field is informational only, for Type Auto.*
Maximum Capacity	see description	Computed size of Drive from Cylinders, Heads, and Sectors entered. This field is only available for Type User. This field is informational only, for Type Auto.*
LBA Format		information only
Total Sectors		information only
Maximum Capacity		information only
Multi-Sector Transfer	**Disabled** 2, 4, 8, or 16 Sectors	Determines the number of sectors per block for multiple sector transfers. This field is informational only, for Type Auto.
LBA Mode Control	**Disabled** Enabled	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors. This field is informational only, for Type Auto.
32 Bit I/O	**Disabled** Enabled	Enabling allows 32 bit IDE data transfers. This field is informational only, for Type Auto.
Transfer Mode	**Standard** Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4	Select the method for moving data to/from the drive. This field is informational only, for Type Auto.
Ultra DMA	**Disabled** Enabled	For use with Ultra DMA drives. This field is informational only, for Type Auto.

* These fields appear only for Type Auto if a drive is detected.

Table 5-13. Keyboard Sub-menu Selections

Feature	Option	Description
Numlock	Auto On **Off**	Selects the power-on state of Numlock.
Key Click	**Disabled** Enabled	Enables key click.
Keyboard auto-repeat rate	**30/sec** 26.7/sec 21.8/sec 18.5/sec 13.3/sec 10/sec 6/sec 2/sec	Selects key repeat rate.
Keyboard auto-repeat delay	¼ sec **½ sec** ¾ sec 1 sec	Selects delay before key repeat.

5.3.3.2 Advanced Menu Selections

The following tables describe the menu options and associated sub-menus available on the Advanced Menu.

Table 5-7. Advanced Menu Selections

Feature	Option	Description
Plug & Play OS	**No** Yes	Select 'Yes' if you are booting a Plug and Play capable OS (i.e. Win 95)
Reset Configuration Data	**No** Yes	Select 'Yes' if you want to clear the System Configuration Data during next boot. Automatically reset to 'No' in next boot.
PCI Configuration	N/A	Selects sub-menu.
Integrated Peripherals Configuration	N/A	Selects sub-menu.
Advanced Chipset Configuration	N/A	Selects sub-menu.
Use Multiprocessor Specification	**1.1** 1.4	Selects the version of MP spec to use. Some OS require version 1.1 for compatibility reasons.
Large Disk Access Mode	**DOS** Other	DOS - select 'DOS'. UNIX, Novell Netware, or other OS - select 'Other'.
Delay on option ROM	**Disabled** Enabled	If enabled, the BIOS pauses for 2 seconds after the option ROMs are scanned, and before option ROM screen is cleared.

Table 5-8. PCI Configuration Sub-menu Selections

Feature	Option	Description
PCI Device, Embedded SCSI	N/A	Selects sub-menu
PCI Device, Slot #1	N/A	Selects sub-menu
PCI Device, Slot #2	N/A	Selects sub-menu
PCI Device, Slot #3	N/A	Selects sub-menu
PCI Device, Slot #4	N/A	Selects sub-menu

Table 5-9. PCI Device, Embedded SCSI Sub-menu Selections

Feature	Option	Description
Option ROM Scan	**Enabled** Disabled	Enable option ROM scan of the selected device.
Wide SCSI Enable Master	**Enabled**	Enable selected device as a PCI bus master. Always enabled.
Latency Timer	Default 000h 020h **040h** 060h 080h 0A0h 0C0h 0E0h	Minimum guaranteed time, in units of PCI bus clocks, that a device may be master on a PCI bus.

Table 5-10. PCI Device, Slot #1 - Slot #4 Sub-menus Selections

Feature	Option	Description
Enable Master	**Enabled** Disabled	Enable selected device as a PCI bus master.
Latency Timer	Default 000h 020h **040h** 060h 080h 0A0h 0C0h 0E0h	Minimum guaranteed time, in units of PCI bus clocks, that a device may be master on a PCI bus.

Table 5-11. Integrated Peripheral Configuration Sub-menu Selections

Feature	Option	Description
COM 1	Disabled **Enabled** Auto PnP OS	If set to “Auto”, BIOS configures the port. If set to “PnP OS”, OS configures the port.
Base I/O Address	**3F8h** 2F8h 3E8h 2E8h	Selects the base I/O address for COM port A
Interrupt	**4** 3	Selects the IRQ for COM port A
COM 2	Disabled **Enabled** Auto PnP OS	If set to “Auto”, BIOS configures the port. If set to “PnP OS”, OS configures the port.
Base I/O Address	3F8h **2F8h** 3E8h 2E8h	Selects the base I/O address for COM port B
Interrupt	4 **3**	Selects the IRQ for COM port B
Parallel Port	Disabled **Enabled** Auto PnP OS	If set to “Auto”, BIOS configures the port. If set to “PnP OS”, OS configures the port.
Mode	Output only Bi-Directional EPP **ECP**	Selects Parallel Port Mode
Base I/O Address	**378h** 278h	Selects the base I/O address for LPT port.
Interrupt	5 **7**	Selects the IRQ for LPT port
DMA channel	**1** 3	Selects the DMA for LPT port
Floppy disk controller	Disabled **Enabled**	Enables on board floppy disk controller.

Table 5-12 Advanced Chipset Configuration Sub-Menu Selections

Feature	Option	Description
640-768K Memory Region	640 768	If enabled ISA MASTER and DMA cycles are forwarded to PCI
Delayed Transaction	Enable **Disable**	Enable the delayed transaction mechanism when PIIX4 is target of a PCI transaction.
Passive Release	Enable **Disable**	Enable the Passive Release Mechanism PHOLD# signal when PIIX4 is a PCI Master.

5.3.3.3 Security Menu Selections

The following options are available on the Security Menu.

Table 3-13. Security Menu Selections

Feature	Option	Description
User Password is	**Clear** Set	Status only; user cannot modify. Once set, it can be disabled by setting to a null string, or clearing via the clear password jumper on board.
Administrator Password is	**Clear** Set	Status only; user cannot modify. Once set, it can be disabled by setting to a null string, or clearing via the clear password jumper on board.
Set User Password is	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clearing via the clear password jumper on board
Set Administrator Password is	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clearing via the clear password jumper on board
Password on boot	**Disabled** Enabled	If enabled, and the user password is set, the system will prompt the user for a password before system boots.
Diskette Access	User **Admin**	User is prevented from accessing the floppy drive if set to Admin. Administrator is always prevented from accessing the floppy drive.
Fixed disk boot sector	**Normal** Write protect	Will write protect the boot sector of the hard drive to prevent viruses from corrupting the drive under DOS if set to write protect.
Secure Mode Timer	**Disabled** 2 min, 5 min, 10 min, 20 min, 1 hr, 2 hr	Period of keyboard and PS/2 mouse inactivity specified for Secure Mode to activate. A password is required for Secure Mode to function. Cannot be enabled unless at least one password is enabled.
Secure Mode Hot Key (Ctrl-Alt-)	[ ] [A, B, ..., Z] [0-9]	Key assigned to invoke the secure mode feature. Cannot be enabled unless at least one password is enabled. Can be disabled by entering a new key followed by a backspace.
Secure Mode Boot	**Disabled** Enabled	System boots in Secure Mode. The user must enter a password to unlock the system. Cannot be enabled unless at least one password is enabled.
Video Blanking	**Disabled** Enabled	Blank video when Secure mode is activated. A password is required to unlock the system. Cannot be enabled unless at least one password is enabled.
Floppy Write Protect	**Disabled** Enabled	When Secure mode is activated, the floppy drive is write protected. A password is required to re-enable floppy writes. Cannot be enabled unless at least one password is enabled.
Reset and Power Switch Lock	**Disabled** Enabled	When Secure Mode is activated, the Reset and Power switches are locked. A password is required to unlock the system. Cannot be enabled unless at least one password is enabled.
System backup reminder	**Disabled** Daily Weekly Monthly	Before booting the BIOS, the gives the user a reminder to perform system backup if set.
Virus check reminder	**Disabled** Daily Weekly Monthly	Before booting the BIOS, this gives the user a reminder to perform a virus check if set.

5.3.3.4 Server menu selections

The following menu and sub-menu options are available on the Server Menu.

Table 5-14. Server Menu Selections

Feature	Option	Description
System Management	N/A	Selects sub-menu.
Console Redirection	N/A	Selects sub-menu.
PCI IRQs to IO-APIC mapping	**Disabled** Enabled	If Enabled, the BIOS describes direct PCI interrupt connections to the I/O APIC in the MP table. Do not enable if OS does not support this feature.
Processor Retest	Yes **No**	Select 'Yes', BIOS will clear historical processor status and retest all processors on next boot.

Table 5-15. System Management Sub-menu Selections

Feature	Option	Description
System Management Mode	Disabled **Enabled**	If enabled, the Server Management Handler will be loaded.
System Event Logging	**Disabled** Enabled	When enabled, system events will be logged by BIOS and the BMC.
Clear Event Log	**No** Yes	If Yes, the System Event log will be cleared.
SMM Debug Mode	**Disabled** Enabled	If enabled the SMM will output to the video and Port 80
Server Management Info	N/A	Selects sub-menu
Set EMP Password is	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string. The valid characters are a-z, A-Z, 0-9 .
EMP Escape string	4 byte string	When EMP is used with a modem, BMC will use this string to inform the modem that the next bytes are to be interpreted as command. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default string is "+++".
EMP Hang up string	8 byte string	When EMP is used with a modem, BMC will use this string to terminate a connection. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default is "ATH".
EMP Modem Initialization String	16 byte string	When EMP is used with a modem, BMC will use this strings to configure the modem every time EMP initializes. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default is "AT&F0S0=1S14=0&D".
EMP High modem Initialization String	4 byte string	When EMP is used with a modem, BMC will use this strings to configure the modem every time EMP initializes. This string is stored in BMC, and not in BIOS CMOS, but clear CMOS jumper sets this string to default. The default is "0".
EMP Access Mode	PreBoot Active **Disabled**	Pre-boot : EMP Enable during POWER DOWN or POST. Always Active : EMP always enabled. Disabled : EMP Disabled
EMP Restricted Mode Access	Enable **Disabled**	Restricted Mode : Power Down, Front Panel NMI , Reset Control via EMP are disabled. Can be selected with Pre-boot, or Always Active mode.
EMP Direct Connect/Modem Mode	**Direct Connect** / Modem Mode	Upon selection USER can connect DIRECTLY to port or using a MODEM.

Table 5-16. Server Management Info Sub-menu Selections

Feature	Option	Description
Board Part Number	N/A	(DMI) Intel motherboard part no. (pba)
Board Serial Number	N/A	(DMI) Intel motherboard serial no.
System Part Number	N/A	(DMI) Integrated system part no.
System Serial Number	N/A	(DMI) Integrated system serial no.
Chassis Part Number	N/A	(DMI) Chassis part no.
Chassis Serial Number	N/A	(DMI) Chassis serial no.
BMC Revision	N/A	BMC revision ID. Revision of firmware for baseboard micro controller
HSBP Revision	N/A	HSBP revision ID. Revision of firmware on Hot Swap SCSI Backplane. Only shown if a Hot Swap BackPlane microcontroller exists in the system.

Table 5-17. Console Redirection Sub-menu Selections

Feature	Option	Description
COM Port Address	**Disabled** 3F8 2F8 3E8	When enabled, Console Redirection uses the I/O port specified. Choosing “Disabled” completely disables Console Redirection.
IRQ #	3 or 4	When Console Redirection is enabled, this shows the IRQ assigned per the COM Port Address chosen above.
Baud Rate	9600 **19.2k** 38.4k 115.2k	When Console Redirection is enabled, it will use the baud rate specified.
Console Type	**ANSI** VT100	Enables the specified Console type.
Flow Control	None CTS/RTS XON/XOFF **CTS/RTS + CD**	None = No flow control CTS/RTS = Hardware based flow control XON/XOFF = Software flow control CTS/RTS +CD = Hardware based + Carrier Detect flow control

5.3.3.5 Boot menu selections

Boot Menu options allow the user to select the boot device. The following table is an example of a list of devices ordered in priority of the boot invocation. Items can be re-prioritized by using the up and down arrow keys to select the device. Once the device is selected, use the plus (+) key to move the device higher in the boot priority list. Use the minus (-) key to move the device lower in the boot priority list.

Table 5-18. Boot Menu Selections

Feature	Option	Description
Floppy Check	**Disabled** Enabled	If Enabled, the system verifies Floppy type on boot. Disable results in a faster boot.
Boot Device Priority	N/A	Selects sub-menu
Hard Drive	N/A	Selects sub-menu
Removable Devices	N/A	Selects sub-menu

Table 5-19. Boot Device Priority Selections

Boot Priority	Device	Description
1.	Removable Devices	Attempt to boot from a removable media device.
2.	Hard Drive	Attempt to boot from a hard drive device.
3.	ATAPI CD-ROM Drive	Attempt to boot from an ATAPI CD-ROM drive.
4.	LANDesk ® Service agent II	Attempt to boot from LANDesk ®.
4.	Diagnostic boot	Attempt to boot from diagnostic boot partition of the Flash. For details, refer to *Section 2.4.5: Diagnostic Boot* in *Chapter 2: System BIOS*.

Table 5-20. Hard Drive Selections

Option	Description
1. Drive #1 (or actual drive string) 2. Other bootable Cards Additional entries for each drive that has a PNP header.	To select the boot drive, use the up and down arrows to highlight a device, then press the plus key (+) to move it to the top of the list (or the minus key (-) to move it down). Other bootable cards cover all the boot devices that are not reported to the system BIOS through BIOS Boot specification mechanism. It may or may not be bootable, and may not correspond to any device. Press ESC to exit this menu.

Table 5-21. Removable Device Menu

Option	Description
1. Device #1 2. Other bootable devices such as Legacy Devices like floppy drives.	To select the device, use the up and down arrows to highlight a device, then press the plus key (+) to move it to the top of the list (or the minus key (-) to move it down). Press ESC to exit this menu. The operating system assigns drive letters to these devices in the order displayed. Change

5.3.3.6 Exit menu selections

The following menu options are available on the Server menu. Select an option using the up or down arrow key. Then press Enter to execute the option.

Table 5-22. Exit Menu Selections

Option	Description
Exit Saving Changes	Exit after writing all modified Setup item values to NVRAM
Exit Discarding Changes	Exit leaving NVRAM unmodified
Load Custom Defaults	Load values of all Setup items from previously saved Custom Defaults
Save Custom Defaults	Save present Setup values to Custom Defaults
Load Default Values	Load default values for all Setup items.
Discard Changes	Read previous values of all Setup items from NVRAM
Save Changes	Write all Setup item values to NVRAM

6. Flash Update Utility

The Flash Memory Update utility (IFLASH) loads a fresh copy of the BIOS into Flash ROM. The loaded code and data include the following:

- On board Video BIOS and SCSI BIOS
- BIOS Setup utility
- User-definable Flash area (User Binary Area)
- Diagnostic boot loader binary
- Language file

When running IFLASH in interactive mode, you may choose to update a particular Flash area. Updating a Flash area takes a file or series of files from a hard or floppy disk, and loads it in the specified area of Flash ROM. In interactive mode, IFLASH can display the header information of the selected files.

NOTE

The utility iFLASH must be run without the presence of a Protected mode control program, such as Windows or EMM386 (Do not run in a DOS window under NT, Win95 or Win98. IFLASH uses the processor's flat addressing mode to update the Flash part.

Other platforms have shown interactions between system sensor event logging, and the IFLASH. With the Nightshade, Sensor event logging is not performed via SMI, thus there are no potential interactions to effect/corrupt FLASH.

6.1 Loading the System BIOS

A new BIOS is contained in .BIx files. The number of .BIx files is determined by the size of the BIOS area in the Flash part. For further information on logical area 1 - System BIOS, see *Table 4-1: Flash Table*. As of this writing, the system BIOS area is 8 files (512KB). They are named as follows:

xxxxxxxx.BIO

xxxxxxxx.BI1

xxxxxxxx.BI2

etc til xxxxxx.BI7

The first 8 letters of each filename on the release diskette can be any value, but cannot be renamed. Each file contains a link to the next file in the sequence. IFLASH does a link check before updating to ensure that the process is successful. However, the first file in the list can be renamed, but all subsequent filenames must remain unchanged. (See *Section 6.5: Recovery Mode* in *Chapter 6: Flash Update Utility*.)

Once an update of the system BIOS is complete, you are prompted for a reboot. Language files are overwritten by updating the system BIOS. If a custom language file has been created, it must be Flashed in after the system BIOS has been updated. The user binary area and diagnostic loader binary image is also updated during a system BIOS update. User binary can be updated independent of the system BIOS.

6.2 User Binary Area

Nightshade includes an 8KB area in Flash for implementation-specific OEM add-ons. The User Binary area can be saved and updated exactly as described above in the *System BIOS* section. Only one file is needed. The valid extension for user files is USR.

6.3 Diagnostic Boot Loader Partition

Nightshade supports 32KB of diagnostic boot loader, which can be saved and updated like the User Binary area, without having to update the rest of the BIOS. The valid extension for the diagnostic boot loader partition is .DBL.

6.4 Language Area

The system BIOS language area can be updated without having to update the entire BIOS. Nightshade supports English, Spanish, French, German, and Italian (from Intel). These languages are selectable using the SSU . When additional language files (*.LNG) are made available, they can be loaded into the system BIOS using IFLASH (in interactive mode, as described above), in the same manner as updating the system BIOS and the user binaries.

6.5 Recovery Mode

In the case of a corrupt .BIx image or an unsuccessful update of the system BIOS, Nightshade can boot in recovery mode. To place Nightshade into recovery mode, move the boot option jumper to recovery position. The jumper connects pins 1 and 2 (normal BIOS) by default.

Recovery mode requires at least 8 MB of RAM in the first DIMM socket, and drive **A:** must be set up to support a 3.5” 1.44 MB floppy drive. This is the mode of last resort, used only when the main system BIOS will not come up. In recovery mode operation, IFLASH (in non-interactive mode only) automatically updates only the main system BIOS. IFLASH senses that N440BX is in recovery mode and automatically attempts to update the system BIOS. It is recommended to turn off FRB by setting the jumper to disable while doing recovery.

Before powering up Nightshade, obtain a bootable MS DOS diskette that contains a copy of the BIOS release. Boot the system from drive **A:** using this diskette, which executes a special AUTOEXEC.BAT file from the BIOS release. The batch file invokes IFLASH, which updates the Flash ROM with the BIOS found on the diskette.

NOTE

During recovery mode, video will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes two to four minutes. A successful update ends with two high-pitched beeps. Failure is indicated by a long series of short beeps.

If a failure occurs, it is most likely that one or more of the system BIOS IFLASH files is corrupt or missing. After a successful update, power down the system and move the recovery jumper back to pins 1 and 2. Power up the system and verify that the BIOS version number matches the version of the entire BIOS that you originally attempted to update. CMOS is not cleared when the system BIOS is updated. Configuration information like ESCD is not overwritten during BIOS flash update. Remember that any

additional or different languages or User Binaries or diagnostic binaries that were present before updating need to be reloaded to Flash.

7. Error Handling

This chapter defines how errors are handled by system BIOS on the Nightshade platform. This chapter provides the role of BIOS in error handling and the interaction between the BIOS, platform hardware and server management firmware as far as error handling is concerned. In addition, error logging techniques are described, and beep codes for errors are defined.

7.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors on Nightshade, which can be disabled and enabled individually or as a group, can be categorized as follows:

- ISA bus
- PCI bus
- Memory single and multi-bit errors
- Sensors
- processor internal error, thermal trip error, temperatures and voltages, GTL voltage levels

The BIOS cannot detect errors on the Pentium® II/ Pentium® III processor bus because PAC does not monitor these.

ISA and PCI bus errors can be further classified as ‘standard bus’ errors, which have a standard register interface across all platforms. All other errors, such as Pentium II/ Pentium III processor and ECC errors, are referred to as ‘product-specific’ errors, which require special consideration depending upon the system configuration. Product-specific errors can be emulated as standard bus errors, if specific routing of certain hardware signals, as documented in this chapter, are followed. This emulation is important to both OS and BIOS NMI handlers, which have no knowledge of product-specific errors, but need to recover and shut down the system gracefully. In Nightshade, sensors are managed by the BMC. The BMC is capable of receiving event messages from individual sensors and log system events. The BIOS programs the BMC not to generate a SMI on a sensor events such as fan failure.

7.2 Error Handlers

The BIOS has an NMI handler that gets invoked when an NMI occurs in POST. Generally, the OS traps the NMI and does not pass it onto the BIOS NMI handler. Therefore, the BIOS NMI handler is rarely invoked in real operating environment. The SMI handler cannot be bypassed by the OS, and is used to handle and log system level events that are not visible to the server management firmware.

7.2.1 BIOS NMI handler

To maintain DOS compatibility, the BIOS NMI handler only processes enabled standard bus errors, such as ISA Parity check or IOCHK# errors. It displays an error message, issues a beep signal, and halts. It disables NMI using bit 7 of I/O port 70h (RTC Index Port) on the occurrence of an unknown or spurious NMI. This can cause unusual side effects because it allows a spurious NMI to block a subsequent valid NMI.

7.2.2 OS NMI handler

The OS NMI handler processes standard bus errors at the OS level. When SMI is disabled, hardware must ensure that these errors are routed to NMI. Most OS NMI handler implementations are not product specific and behave in a manner similar to a BIOS NMI handler. It is the responsibility of the BIOS SMI handler to present platform specific errors, such as multi-bit ECC error, as one of the standard bus errors, like parity error, to the OS NMI handler. If the SMI handler is disabled via SSU , the OS will not know about platform-specific critical errors.

7.2.3 SMI handler

If the SMI handler control bit in Setup is disabled, no SMI signals are generated, and no SMI handler is required. If enabled, all system errors are preprocessed by the SMI handler, even those that are normally considered to generate an NMI. The SMI handler sends a command to the BMC to log the event and provides the data to be logged.

7.3 Handling and logging System Errors

This section describes the register bits associated with the various categories of system errors, and actions taken by error handlers. It covers the events logged by the BIOS and the format of data bytes associated. The BIOS is responsible for monitoring and logging certain system events. BIOS sends an event request message to BMC to log the event. Some of the errors, such as processor failure, are logged during early POST and not by SMI handler.

7.3.1 Logging format conventions

BIOS complies with the Platform Sensor and Event Interface EPS, Revision 1.0. The BIOS always uses a software ID of 0 to log POST errors. SMM handler uses software ID of 10h. OEM user binary should use software IDs of 1 and SMM User Binary should use an ID of 11h. The Software ID allows external software to find the origin of the event message.

The BIOS uses the following sensor numbers while logging events. Application software can examine the sensor number field in the log record to determine the source of error. The *Platform Sensor and Event Interface EPS* requires that distinct sensor numbers are used for different error sources.

Table 7-1. System Event Logging Format

Event Types	***Sensor Type/Sensor #/ Type Code/Data bytes 1,2,3.***
Single bit memory error	**0C *EF E7 20 DIMM# FF**
Multi bit memory error	**0C *EF E7 21 DIMM# FF**
Memory parity error	**0C *EF E7 02 FF FF**
Front panel NMI	**13 28 E7 00 FF FF**
Bus timeout	**13 *EF E7 01 FF FF**
I/O chk	**13 *EF E7 02 FF FF**
Software NMI	**13 *EF E7 03 FF FF**
PCI PERR	**13 *EF E7 04 FF FF**
PCI SERR	**13 *EF E7 05 FF FF**

Note:

* Sensor # = 0EFh (not applicable). Other fields are sufficient enough to identify type of errors.

The BIOS treats all the above sensors as discrete sensors. The 4 bit offset field in the first event data byte indicates the exact cause of the error. In all the events logged by the BIOS, up to 2 OEM data bytes are used to indicate the physical location of the error, such as the DIMM row number. Application software must examine these bytes to point to the exact source of error within a 'virtual sensor'. *Table 7-2, Event Request Message Event Data Field Contents* describes the various fields in the event request message, as sent by the BIOS.

Table 7-2. Event Request Message Event Data Field Contents

Event Trigger Class	**Event Data**
discrete	Event Data 1 7 0 = OEM code in byte 2 6:5 00 = unspecified byte 3 10 = OEM code in byte 3 4 reserved. Set to 0 when sending event. 3:0 Offset from Event Trigger for discrete event state Event Data 2 OEM code byte 1 Event Data 3 Optional OEM code byte 2. FFh or not present if unspecified.

7.3.2 ISA Bus Error

ISA bus errors generate an NMI, triggered by a memory error or IOCHK# assertion on the ISA bus. Nightshade always uses ECC memory, so it emulates the ISA Memory parity error as an uncorrectable ECC memory error. For other system fatal errors generated by PCI or Pentium® II processor bus, the SMI handler can emulate a memory parity error to pass control to the NMI handler. An I/O register at 61h (System Control port B) is defined that controls and indicates the errors. The NMI can be disabled using the RTC Index port bit 7 (I/O port 70h). The following tables show the action taken by each error handler, and control bits associated with this error.

Table 7-3. Error Handler Action on ISA Bus Error

Handler	Action
BIOS NMI	Displays an error message, and halts the system.
OS NMI	Logging of error and graceful system shutdown.
BIOS SMI	The SMI handler logs the event(s). The sensor number is 4 as defined in *Section 0.: Logging Format Conventions*. There is only one OEM data byte that indicates the slot number. The slot number is set to 0ffh if it cannot be determined.

Table 7-4. ISA Bus Error Control Bits

Location	Function	Bit(s)	Description	Value
I/O 61h	System Control	7	Memory parity check error flag (RO)	1 = error, 0 = OK
	Port B	6	Channel check (IOCHK#) error flag (RO)	
		5::4	Reserved	
		3	Channel check enable (RW)	1 = enable, 0 = disable
		2	Parity check enable (RW) (system board error enable)	
		1::0	Reserved	

7.3.3 PCI Bus Error

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. The BIOS can be instructed to enable or disable reporting PERR# and SERR# through NMI. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported directly by SERR#. SERR# can be routed to NMI. In the Nightshade platform, PAC is the device that reports errors on PCI #1 using SERR#. All the PCI-to-PCI bridges are configured so that it generates SERR# on the primary interface whenever there is SERR# on the secondary side, if SERR# is enabled through SSU . The same is true for PERR#. The sensor number is 4, as defined in *Section 0.: Logging Format Conventions*. Two OEM data bytes are present. The first OEM byte indicates the PCI bus number. The second OEM byte encodes the PCI device number and the PCI function number in a standard manner. The most significant 5 bits have the device number and the other 3 bits indicate the function number. The offset from the event trigger field determines whether it was a PERR or SERR. The following tables show the action taken by each error handler, and control bits associated with this error.

Table 7-5. Error Handler Action on PCI Bus Error

Handler	Action
BIOS NMI	Halt the system, Disable NMI
OS NMI	Logging, shutdown
BIOS SMI	Logging PCI errors.

Table 7-6. PCI Bus Error Control Bits

Location	Function	Bit(s)	Description	Value
PAC 04h	Command	6	PERR# enable	1 = enable, 0 = disable
PAC 05h	Command	1	SERR# enable	1 = enable, 0 = disable
PAC 90h	Error	4	Enable SERR# on receiving Target abort	1 = enable, 0 = disable
	Command	3	Enable SERR# on PCI parity Error	
	Register	1	Enable SERR# on Multi-Bit ECC/Parity error	
		0	Enable SERR# on Single-Bit ECC/Parity error	
PAC 91h	Error	4	Multi-Bit ECC/Parity error	1 = error, 0 = OK
	Status Reg.	0	Single-Bit ECC/Parity error	

7.3.4 Pentium® II Processor Bus Error

Neither PAC nor the I^2C controller reports Pentium® II/ Pentium® III processor bus AERR# and BERR# error signals to the system. (AERR# indicates an address parity error and BERR# indicates an unrecoverable Pentium II/Pentium III processor bus error.) Therefore, the system SMM handler does not log and report these type of errors to the OS.

7.3.5 Memory Bus Error

PAC generates SERR# on single and double-bit errors. Generation of NMI on SBE is disabled when SMI is disabled. The following register bits control and log the errors. The following tables show the action taken by each error handler, and control bits associated with this error. The message contains one OEM data byte. The row number (zero-based enumeration) is used as the OEM data byte in this record. For EDO and SDRAM modules, row number 0 is the bottom row.

Table 7-7. Error Handler Action on Memory Bus Error

Handler	Action
BIOS NMI	Emulation or Disable NMI
OS NMI	Logging, shutdown
BIOS SMI	Logging. Note: The SMI handler might emulate processor bus fatal errors (only), and pass control to the BIOS NMI handler.

Table 7-8. Memory Bus Error Control Bits

Location	Function	Bit(s)	Description	Value
PAC 90h	Command	1	Enable multi-bit memory Error Reporting	1-enabled, 0-disabled
		0	Enable single-bit memory Error Reporting	
PAC 91h	Memory Error	7-5	DRAM row where the last multi-bit error occurred valid only if bit 4 is set	0 to 7
		4	Multi-bit ECC error flag	1 = error, 0 = OK
		3-1	DRAM row where the last SBE occurred valid only if bit 0 is set	0 to 7
	Status	0	Single-Bit ECC error flag,	1 = error, 0 = OK

7.3.6 System Limit Error

The Nightshade I^2C microcontroller monitors system operational limits. It manages the A/D converter, defining voltage and temperature limits, and fan senses and chassis intrusion. Any sensor values outside of specified limits are fully handled by BMC and there is no need to generate an SMI to the host processor.

7.3.7 Processor Failure

The BIOS detects BIST failure and watchdog timer reset events. The failed processor can be identified by the first OEM data byte field in the log. For example, if processor 0 fails, the first OEM data byte will be 0.

7.3.8 Boot event

The BIOS downloads the system date and time to the BMC during POST and logs a boot event.

7.4 Error Messages and Error Codes

The system BIOS displays error messages on the video screen. Prior to video initialization, beep codes inform you of errors. POST error codes are logged in the event log, as well as the EBDA.

The BIOS displays POST error codes on the video monitor. The error codes are defined by Intel and whenever possible are backward-compatible with error codes used in the XXpress platform.

Following are definitions of POST error codes, POST beep codes, and system error messages.

7.4.1 POST Codes

The BIOS indicates the current testing phase during POST after the video adapter has been successfully initialized by writing a 2-digit hex code to I/O location 80h. If a Port-80h card (Post card*) is installed, it displays this 2-digit code on a pair of hex display LEDs.

Table 7-9. Port-80h Code Definition

Code	Meaning
CP	Phoenix check point (port-80) code

The following table contains the port-80 codes displayed during the boot process. A beep code is a series of individual beeps on the PC speaker, each of equal length. The following table describes the error conditions associated with each beep code and the corresponding POST check point code as seen by a ‘port 80h’ card (for example, if an error occurs at check point 22h, a beep code of 1-3-1-1 is generated). The - means there s a pause between the sequence that delimits the sequence.

Table 7-10. Standard BIOS Port-80 Codes in execution sequence during post

CP	Beeps	Reason
02		Verify Real Mode
12		Restore processor control word during warm boot (only occurs on warm reboot)
24		Set ES segment register to 4GB
04		Get processor type
06		Initialize system hardware
18		8254 timer initialization
08		Initialize PCIset registers with initial POST values
C4		Initialize system flags in cmos
11		Load alternate registers with initial POST values
0E		Initialize I/O
0C		Initialize caches to initial POST values
16	1-2-2-3	BIOS ROM checksum
17		turn cache off
28		Autosize DRAM
2A		Clear 512K base RAM
2C	1-3-4-1	RAM failure on address line xxxx*
2E	1-3-4-3	RAM failure on data bits xxxx* of low byte of memory bus (1st 4 meg)
2F		Initialize L2 cache if enabled in cmos
38		Shadow system BIOS ROM
20	1-3-1-1	Test DRAM refresh
29		Post Memory Manager Initialization (PMM)
33		Post Dispatch manager Initialization
34		Test CMOS
C1		Post error manager Intialization
09		Set in POST flag
0A		Initialize processor registers and cpu microcode
3A		Autosize cache
0B		Enable processor cache
0F		Initialize the local bus IDE (not used anymore but here for phx std)
10		Initialize Power Management (APM not used in Nightshade)
14		Initialize keyboard controller
1A		8237 DMA controller initialization
1C		Reset Programmable Interrupt Controller
22	1-3-1-3	Test 8742 Keyboard Controller
32		read processor bus-clock frequency and compute boot processor speed
67		Initialize and register other cpu via SMM through apic bus
69		Initialize SMI handler for all processors
00		wait for secondary processor to execute init smi handler
F4		exit Smi handler (secondary processor executed halt in smi)
3C		Configure advanced PCIset registers and reset coprocessor
3D		Load alternate registers with CMOS values
42		Initialize interrupt vectors
46	2-1-2-3	Check ROM copyright notice
45		Initialize all pre-pnp devices
49		Initialize PCI bus and devices (also read escd and allocate resources)
48		Check video configuration against CMOS (vga or mda)
4A		Initialize all video adapters in system
4C		Shadow video BIOS ROM
24		put cpu in big real mode (flat mode memory addressing - up to 4 Gb)

Table 7-10. Standard BIOS Port-80 Codes (cont.)

CP	Beeps	Reason
59		Post display manager initialization (video screen error codes now visible)
22		reset and test keyboard first try (only warm reset)
52		reset and test keyboard controller (both warm and cold reset)
54		Set key click if enabled
76		Enable keyboard
58	2-2-3-1	Test for unexpected interrupts
4B		Quietboot start (not used in N440BX)
4E		Display copyright notice
50		Display cpu(s) type and speed
51		Eisa Init (Not used in N440BX)
5A		Display prompt “Press F2 to enter SETUP”
5B		Disable cpu L1 cache for memory test
5C		Test RAM between 512 and 640k
60		Test extended memory (4Mb to top of memory)
62		Test extended memory address lines
64		Jump to UserPatch1
66		Configure advanced cache registers
68		Enable external and processor caches
6A		Display external cache size
6C		Display shadow message
6E		Display non-disposable segments
70		Display error messages to video
72		Check for configuration errors
74		Test real-time clock
7C		Set up hardware interrupt vectors
7E		Test coprocessor if present
80		not used
88		Initialize BIOS Data Area , timeouts for detecting parallel, serial and hdd controller clear cmos shutdown flag
8A		Initialize Extended BIOS Data Area
81		late post core initialization of devices
87		configure mcd devices
85		Initialize and detect PC-compatible PnP ISA devices (serial, parallel etc)
82		not used
84		clear intrerrupts from com port detection
86		console redirection initialized
83		configure onboard hard disk controller
89		Enable NMI

8C		Initialize floppy controller
90		Initialize and detect hard disks
8B		Detect and test for Mouse or Auxillary device on keyboard controller
95		Install CD-ROM for boot
92		Jump to UserPatch2
C5		Initialize GPNV areas of DMI
98	1-2	Search for option ROMs. One long, two short beeps on checksum failure of an option rom
93		Scan for User flash roms MP table initialization (wake up secondary processor and halt it)
9C		Set up Power Management (not used)
9D		enable security
9E		Enable hardware interrupts
A0		Set time of day
A2		Check key lock
A4		Initialize typematic rate
C2		Initialize DMI tables
C3		Log post errors with Post error manager and to SEL in BMC also update VID bits and memory presence to BMC display and FRB errors (watchdog timeouts, bist or CPU failures)
A8		Erase F2 prompt
AA		Scan for F2 key stroke
AC		Initialize EMP port if selected. Remove com2 from BDA if EMP is enabled. Enter SETUP
AE		Clear in-POST flag
B0		Turn on secure boot if enabled(secure front panel, blank video, floppy write protect) Check for errors
B2		POST done – prepare to boot Operating System
B4	1	One short beep before boot
B5		Display Quietboot (not used)
BE		Clear screen
B6		Check password (optional)
BC		Clear parity checkers
BA		not used
B7		ACPI configuration (table configuration in memory and BDA)
BD		Display multiboot menu if esc is hit
BF		Display system config summary(if enabled in cmos)
8F		get total # of hard drives and put in BDA
91		Program IDE hard drives (timing, pio modes etc)

9F		save Total # of hard drives (scsi and ATA) in BDA
97		Fixup MP table (checksum)
99		check smart harddrive
C7		Prepare to boot to OS, clean up graphics and pmm areas.
C0		Try to boot with INT 19 return to video mode 3 disable pmm return to real mode disable gate A20 clears system memory reset stack Invokes Int19
		Error handling Post codes (may occur at anytime during post)
DO		Interrupt handler error
D2		Unknown interrupt error
D4		Pending interrupt error
D6		Initialize option ROM error
D8		Shutdown error
DA		Extended Block Move
DC		Shutdown 10 error

7.4.2 POST Error Codes and Messages

The following table defines POST error codes and associated messages. The BIOS will prompt the user to press a key in case of serious errors. Some of the error messages are preceded by the string ‘Error” to highlight the fact that these indicate a possibly malfunctioning systems.

Table 7-11. POST Error Messages and Codes

Code	Error message	Pause on error
0162	BIOS unable to apply BIOS update to processor 1	Yes
0163	BIOS unable to apply BIOS update to processor 2	Yes
0164	BIOS does not support current stepping for processor 1	Yes
0165	BIOS does not support current stepping for processor 2	Yes
0200	Failure Fixed Disk	No
0210	Stuck Key	No
0211	Keyboard error	No
0212	Keyboard Controller Failed	Yes
0213	Keyboard locked - Unlock key switch	Yes
0220	Monitor type does not match CMOS - Run SETUP	No
0230	System RAM Failed at offset:	No
0231	Shadow Ram Failed at offset:	No
0232	Extended RAM Failed at offset:	No
0250	System battery is dead - Replace and run SETUP	Yes
0251	System CMOS checksum bad - Default configuration used	Yes
0260	System timer error	No
0270	Real time clock error	No
0297	ECC Memory error in base (extended) memory test in Bank xx	Yes
02B2	Incorrect Drive A type - run SETUP	No
02B3	Incorrect Drive B type - run SETUP	No
02D0	System cache error - Cache disabled	No
02F5	DMA Test Failed	Yes
02F6	Software NMI Failed	No
0401	Invalid System Configuration Data - run configuration utility	No
None	System Configuration Data Read Error	No
0403	Resource Conflict	No
0404	Resource Conflict	No
0405	Expansion ROM not initialized	No
0406	Warning: IRQ not configured	No
0504	Resource Conflict	Error
0505	Expansion ROM not initialized	No
0506	Warning: IRQ not configured	No
0601	Device configuration changed	No
0602	Configuration error - device disabled	No
8100	processor 0 failed BIST	Yes
8101	processor 1 failed BIST	Yes
8104	processor 0 Internal Error (IERR) failure	Yes
8105	processor 1 Internal Error (IERR) failure	Yes
8106	processor 0 Thermal Trip failure	Yes
8107	processor 1 Thermal Trip failure	Yes
8108	Watchdog Timer failed on last boot, BSP switched.	Yes
810A	processor 1 failed initialization on last boot.	Yes
810B	processor 0 failed initialization on last boot.	Yes
810C	processor 0 disabled, system in Uni-processor mode	Yes
810D	processor 1 disabled, system in Uni-processor mode	Yes
810E	processor 0 failed FRB Level 3 timer	Yes
810F	processor 1 failed FRB Level 3 timer	Yes
8110	Server Management Interface failed to function	Yes
8120	IOP sub-system is not functional	Yes

8150	NVRAM Cleared by Jumper	Yes
8151	NVRAM Checksum Error, NVRAM cleared	Yes
8152	NVRAM Data Invalid, NVRAM cleared	Yes

8. Board Set Specifications

This chapter specifies the operational parameters and physical characteristics for the N440BX Server. This is a board-level specification only. System specifications are beyond the scope of this document.

8.1. Absolute Maximum Ratings

Operation of the N440BX Server at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 8-1. Absolute Maximum Ratings

Operating Temperature	0°C to +55°C *
Storage Temperature	-40°C to +70°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V **
3.3V Supply Voltage with Respect to ground	-0.3 to +3.63V
5V Supply Voltage with Respect to ground	-0.3 to +5.5V

- Chassis design must provide proper airflow to avoid exceeding Pentium® II/Pentium® III maximum case temperature.
- ** V_{DD} means supply voltage for the device.

Further topics in this chapter specify normal operating conditions for N440BX Server.

8.2. Electrical Specifications

DC specifications for N440BX Server power connectors and module power budgets, are summarized here. Electrical characteristics for major connector interfaces (including DC and AC specifications), can be obtained from other documents:

- PCI Connectors -- PCI Local Bus Specification Rev. 2.1
- ISA slots -- EISA Bus Specification

8.3. Power Connection

Main power supply connection is obtained using either the 20-pin ATX-style connector or the 24-pin Columbus II-style connector. A third connector is provided for power supply control in the Columbus II chassis. The following tables define the pin outs and wire gauge/color for each of these connectors.

Table 8-2. 20-pin ATX-style Main Power Connector Pin out

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	+3.3 VDC	Orange	11	+3.3 VDC 3.3 V sense	Orange Brown
2	+3.3 VDC	Orange	12	-12 VDC	Blue
3	COM	Black	13	COM	Black
4	+5 VDC	Red	14	PS-ON*	Green
5	COM	Black	15	COM	Black
6	+5 VDC	Red	16	COM	Black
7	COM	Black	17	COM	Black
8	PWR-OK	Gray	18	-5 VDC	White
9	5 V Standby	Purple	19	+5 VDC	Red
10	+12 VDC	Yellow	20	+5 VDC	Red

Warning: Do not attempt to plug the ATX 20-pin connector into the 24-pin Columbus II chassis-style connector. Damage to the baseboard will occur.

Table 8-3. 24-pin Columbus II chassis-style Power Connector Pin out

Pin	Signal	Pin	Signal
1	GND	2	Hard disk activity LED
3	Front panel reset switch	4	Front panel power switch
5	+5V standby mode	6	nc (key)
7	Front panel NMI switch	8	POWER_COL_FP_LED_L(Power LED/blink for ACPI Sleep)
9	Fan failure indicator LED	10	Chassis intrusion switch
11	Power fault LED	12	+5V standby power mode
13	IMB Data line	14	RJ45_ACTLED(LAN Active LED; supported on Astor chassis only
15	IMB Clock line	16	GND

Table 8-4. 14-pin Auxiliary Power Connector Pin out

Pin	Signal	Pin	Signal
1	+5V standby power mode sense Return	2	+5V standby power mode Sense
3	+3V Sense	4	+3V Sense Return
5	IMB Clock line	6	IMB Data line
7	GND	8	POWER_GOOD
9	PS_POWER_ON	10	GND
11	+5V standby power mode	12	nc (Key)
13	Reserved	14	VCC 24

8.4. Power Consumption

The following table shows the power consumed on each supply line for a N440BX Server baseboard with 2 processors, 4 DIMMs, 4 PCI slot loads (2A @ 5V per slot), and 1 ISA slot load (Server Monitor Module board).

NOTE:

The following numbers are provided as an example. Actual power consumption will vary depending on the exact N440BX Server configuration. Refer to the appropriate system chassis document for more information.

Table 8-5. Power Consumption

Device(s)	3.3V	+5V	+12V	-12V	5V Standby	
Processors	3.04A	8.17A	3.41A			
Memory DIMMs	3.58A					
GTL Termination	2.91A					
NBX	1.20A					
Baseboard	.32A	2.56A	.2A	.15A	.8A	
Fans			1.0A			
Keyboard/Mouse		.5A				
PCI slots		8A				
ISA slot		.1A	1.0A			
Total Current	**11.05 A**	**19.33 A**	**5.61**	**.15A**	**.8A**	**Total**
Total Power	**36.47 W**	**96.65 W**	**67.32W**	**1.8W**	**.4W**	**202.74W**

8.5. Power Supply Specifications

This section provides power supply design guidelines for a N440BX Server-based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 8-6. Power Supply Voltage Specification

Item	Min	Nom	Max	Units	Tolerance
VOLTAGE TOLERANCE:					
3.3 Volts	3.14	3.30	3.46	V	+5%
5 Volts	4.80	5.00	5.25	V	+5%
+12 Volts	11.40	12.00	12.60	V	+5%
-12 Volts	-11.40	-12.00	-12.60	V	+5%
-5 Volts	-4.75	-5.00	-5.25	V	+5%
5 Volts Standby	+4.75	+5.00	+5.25	V	+5%

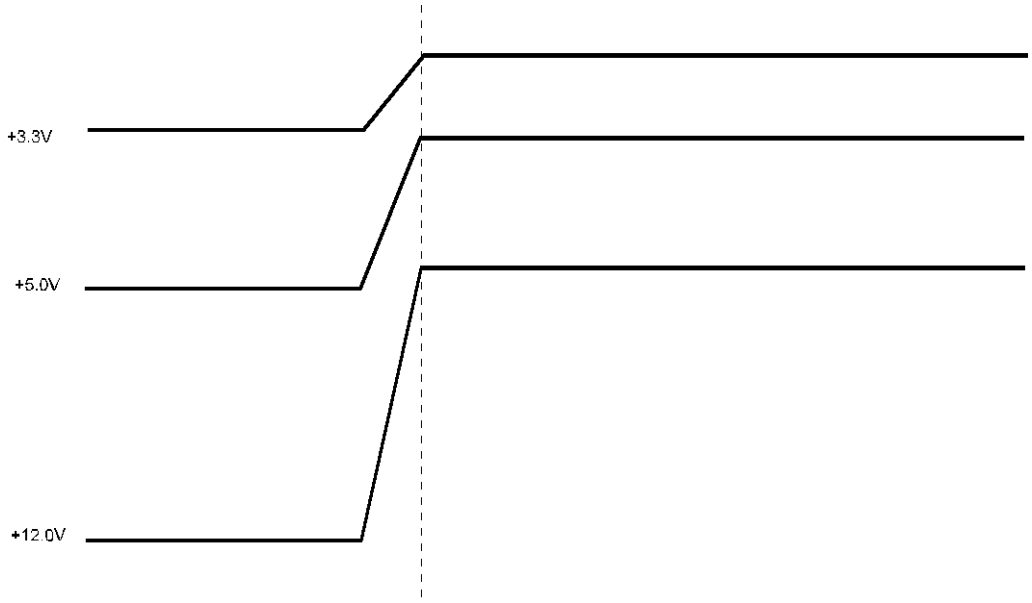
Table 8-7. Transient and Remote Sense/Sink Currents

Item	Min	Nom	Max	Units
TRANSIENT CURRENTS:				
Max dI/dt:				
5 Volts			0.5	A/µs
3.3 Volts			TBD	A/µs
+12 Volts			TBD	A/µs
-12 Volts			0.3	A/µs
-5 Volts			0.3	A/µs
5 Volts Standby			0.5	A/µs
Amplitude:				
5 Volts			7.0	A
3.3 Volts			0.5	A
+12 Volts			3.0	A
-12 Volts			0.5	A
-5 Volts			0.5	A
5 Volts Standby			0.01	A
REMOTE SENSE:				
Fuse Rating:		N/A		A
Sense Trace Resistance:			0.05	Ω
SINK CURRENT (While Voltage Form Off):				
Off Voltage:				
Item	**Min**	**Nom**	**Max**	**Units**
5 Volts			0.2	V
3.3 Volts			0.1	V
+12 Volts			0.1	V
-12 Volts			0.1	V
-5 Volts			0.1	V

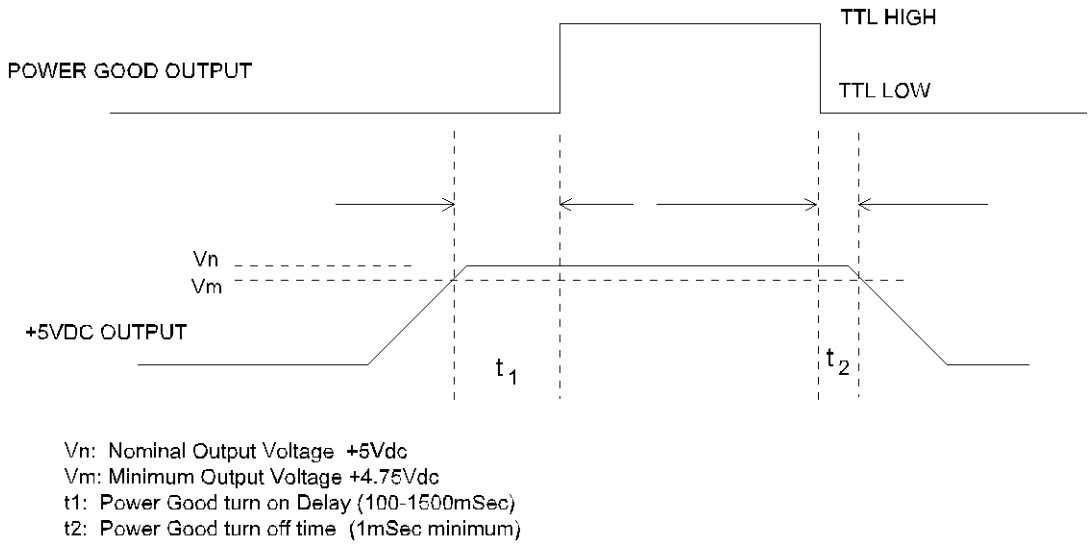
Table 8-8. Ramp Rate/ Ramp Shape/ Sequencing/ Power Good & Power On Signals

Item	Min	Nom	Max	Units	Comments
Ramp Rate(On):					
5 Volts	5		70	ms	From 10% to within regulation
3.3 Volts	5		70	ms	From 10% to within regulation
+12 Volts	5		70	ms	From 10% to within regulation
-12 Volts	5		70	ms	From 10% to within regulation
-5 Volts	5		70*	ms	From 10% to within regulation
5 Volts Standby	5		70	ms	From 10% to within regulation
Ramp "Shape"(On & Off):					Monotonic
Sequencing: **(with respect to 5 Volts)**					See Figure 6-1
3.3 Volts					
+12 Volts					
-12 Volts					
-5 Volts					
5 Volts Standby					
Power Good Signal					See Figure 6-2
Vil			0.4	V	
Vih	3.5			V	
Iil	4.0			mA	
Iih			0.2	mA	
Timing requirements				TBD	
Power On Signal				TBD	
Vol			0.4	V	
Voh	3.5			V	
Iol	4.0			mA	
Ioh			0.2	mA	
Timing requirements				TBD	
Etc.					

***-5V must not ramp up before +12V**



0Figure 6-1. DC Voltage Sequencing



Vn: Nominal Output Voltage +5Vdc
Vm: Minimum Output Voltage +4.75Vdc
t1: Power Good turn on Delay (100-1500mSec)
t2: Power Good turn off time (1mSec minimum)

Note: +5Vdc Standby must have a minimum of .8A.

Figure 8-2. Power Good Signal Characteristics

9. Errata Listing

9.1. Summary Errata Table

The following tables indicate the Errata and the Document Changes that apply to the NL440BX & T440BX UP Server system. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Table

Doc:	Intel intends to update the appropriate documentation in a future revision.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	Plans	ERRATA
1	NoFix	Full length PCI card interference.
2	NoFix	Some mouse configurations are incompatible with N440BX Server.
3	NoFix	Systems may automatically power up if a PCI card is inserted without removing AC power. Not a bug.
4	Fixed	The ESCD PnP records are not fully compliant with either V2.0 or V2.1 of the ESCD specification.
5	Fixed	The BIOS does not honor PCI disable bit in ESCD.
6	NoFix	When selecting BIOS Boot Order, it is impossible to determine boot drive if models are identical.
7	NoFix	Microsoft* Windows NT* 4.0 installs boot files to wide SCSI channel by default.
8	NoFix	If PS/2 mouse is not connected Windows NT 4.0, install fails.
9	Fixed	N440BX Server freezes with Windows NT 4.0 display drivers and some hardware RAID cards on the production Country Kit.
10	NoFix	BIOS setup indicates processor cache enabled when disabled.
11	NoFix	Response to power button takes approximately four seconds before reaching video on boot-up using the front panel.
12	NoFix	NA440BX Server system event log entries do not record drive insertion events when swap occurs in less than three seconds.
13	NoFix	Option ROM space is limited with N440BX DP Server.
14	NoFix	Sensor data records cannot be read when N440BX Server is in +5V standby power mode.
15	NoFix	FRB 3 errors are logged multiple times in the system event log.
16	NoFix	System event log - Multi-bit Memory Errors indicated as voltage events in system event log viewer.
17	Fix	Cannot clear system event log when in +5V standby power mode.
18	NoFix	Watch Dog timer fails to count down properly.
19	NoFix	Events that take place before the BIOS sets the time will have a Pre-Init time stamp.
20	Fixed	Intel® EtherExpress™ PRO/100B Speedo IV 82558 driver will not load in Microsoft* Windows* 95
21	NoFix	Intelligent I/O PCI add-in cards fail when configured in Slot 4.
22	Fixed	Version 3.49 of TestView does not contain a VGA or hotswap backplane test package.
23	Fixed	Front Panel Drive Light Remains on when First Symbios SCSI channel is disabled.
24	NoFix	The system will not boot to a 2nd or 3rd fixed disk when primary disk is not bootable.
25	Fix	Fixed disk boot sector write protect CMOS option does not protect against viruses

9.2. ERRATA

1. Full length PCI card interference

PROBLEM: If there is a cable in the narrow SCSI connector, some full-length PCI add-in cards that are installed into the slot closest to processors (PCI 4) will not seat fully. The bracket hinders the add-in card from seating fully.

IMPLICATION: The user will be restricted from using some full-length add-in cards in PCI slot 4.

WORKAROUND: None identified.

STATUS: NoFix.

2. Some mouse configurations are incompatible with the N440BX DP Server

PROBLEM: The N440BX baseboard will not recognize some PS/2 mouse configurations. Specifically when a PS/2 mouse is attached to a 25' extension, the mouse often fails to be recognized by most operating systems. When using a switch box the user is limited to an extension cable that is no longer than 6'.

IMPLICATION: With certain operating systems, when using a long mouse extension cable the mouse will not be recognized and not be functional.

WORKAROUND: None identified.

STATUS: NoFix.

3. Systems may automatically power up if a PCI card is inserted without removing AC power. Not a bug.

PROBLEM*:* If the system has been powered down via the front panel power switch, some devices are still in a powered up mode due to the N440BX's system management features.

IMPLICATION*:* Inserting a card in the PCI slots without unplugging the system may short some PCI pins together, causing the PCI_PME_L signal to bring the system into a fully powered mode. Due to the hazard this poses we recommend users unplug the system before opening the system.

The following is called out in our user guide documentation:

WARNINGS

System power on/off: The DC push-button on/off switch (a convex button) on the front panel DOES NOT turn off the system AC power. To remove power from system, you must unplug the AC power cord from the wall outlet.

WORKAROUND: None

STATUS: NoFix.

4. The Extended System Configuration Data (ESCD) Plug-n-Play records are not fully compliant with either V2.0 or V2.1 of the ESCD specification

PROBLEM: The Plug-n-Play ESCD records indicate compliance with v2.0 of the ESCD specification.

IMPLICATION: The Plug-n-Play ESCD records are not completely compliant with either v2.0 or v2.1 of the Plug-n-Play specification.

WORKAROUND: None identified.

STATUS: Fixed. All records have been updated to V2.1 of the ESCD spec in BIOS 9 and newer.

5. BIOS does not honor PCI disable bit in Extended System Configuration Data (ESCD)

PROBLEM: The ESCD free-form record for PCI devices contains a field that indicates if a PCI function should be enabled or disabled. The Server Setup Utility (SSU) will set this bit if the user requests to disable a PCI device. On the next boot, the BIOS should turn off the command register in the PCI device, ignore its option ROM, and ignore any resource requirements found in the function's Base Address Registers or Interrupt Pin.

IMPLICATION: If the onboard devices are disabled through the SSU, their resources will be reallocated on the next system boot.

WORKAROUND: None

STATUS: Fixed. This issue is resolved with SSU3 and BIOS release 9 or newer.

6. When selecting BIOS boot order it is impossible to determine the boot drive if models are identical

PROBLEM: Using identical drives, it is impossible to determine which drive corresponds to which logical unit number (LUN).

IMPLICATION: If two identical drives are installed, the user will not be able to determine which drive corresponds to which LUN in BIOS setup.

WORKAROUND: None identified.

STATUS: Fix - in a future SCSI BIOS revision.

7. Microsoft* Windows NT* 4.0 installs boot files to the wide SCSI channel by default

PROBLEM: Microsoft Windows NT always installs its boot loader files to the first hard drive it finds in the scan order of the SCSI controller regardless of BIOS configuration. The scan order of the Symbios SCSI controllers are wide (hba 0) then narrow (hba 1) channels.

IMPLICATION: To install Microsoft Windows NT to a Narrow SCSI drive while a wide SCSI drive is present, Microsoft Windows NT will place the boot files on hba 0, id=0, which is the drive connected to the wide controller and the rest of the install on the narrow device.

WORKAROUND: In the Symbios configuration utility, change the default boot order from dev 68 = 0, dev 69 = 1 to dev 69 = 0, dev 68 = 1.

STATUS: NoFix.

8. If PS/2 mouse is not connected, Microsoft* Windows NT* 4.0 install fails

PROBLEM: When the Microsoft Windows NT 4.0 install process tries to load the kernel and drivers it hangs after displaying OS version and kernel type if the PS/2 mouse is not connected.

IMPLICATION: Microsoft Windows NT 4.0 cannot install without a pointing device on a N440BX DP Server.

WORKAROUND: None identified.

STATUS: NoFix.

9. Microsoft* Windows NT* 4.0 freezes with production Country Kit video drivers and some hardware RAID cards

PROBLEM: Microsoft Windows NT 4.0 freezes and produces an “orange” or “blank” screen when using some hardware RAID solutions and production Country Kit display drivers.

IMPLICATION: The N440BX Server system must boot with the standard VGA option displayed on the NT Boot loader.

WORKAROUND:

STATUS: Fixed-- Version 1.22 of the Cirrus 5480 display drivers for Microsoft Windows NT 4.0 available at the Intel web site www.intel.com/support.

10. BIOS setup reports processor cache enabled when disabled

PROBLEM: The Pentium® II processor algorithm dictates that the processor cache is disabled if processor speed is less than 3 times the front side bus speed. This occurs when the CMOS is cleared and the user immediately enters BIOS setup before setting the CMOS clear jumper back to normal operation. BIOS setup will indicate that the cache is enabled when it is really disabled.

IMPLICATION: Cache is disabled despite setup reporting that it is enabled during CMOS clear.

WORKAROUND: Setting the clear CMOS jumper back to normal will set the default processor speed to 3 times the front side bus speed and enable the cache.

STATUS: NoFix.

11. Response to power button takes approximately four seconds before video display occurs on boot-up

PROBLEM: If the N440BX is turned off using the front panel switch before video is reached during POST there will be a four second delay in the system shutting down.

IMPLICATION: The PIIX4 does not get initialized until POST 52 (video). If the power button is depressed before this time the baseboard management controller (BMC) senses the change in state and will wait for a message from the PIIX4 until its time-out period has reached about four seconds. If there is no message, the BMC will then force the system to power down.

WORKAROUND: None identified.

STATUS: NoFix - this is normal operation.

12. N440BX Server system event log entries do not record drive insertion events when drive swap occurs in less than three seconds

PROBLEM: In an Astor chassis hot-swap drive bay, insertion events will not be logged if the drive is removed and reinserted in a time span of less than three seconds.

IMPLICATION: The drive may not get an ID or power and will not function correctly.

WORKAROUND: Wait more than 3 seconds before inserting a drive after removing a drive.

STATUS: NoFix.

13. Option ROM space limited on the N440BX DP Server

PROBLEM: When configuring a N440BX with multiple add-in cards using option ROMs, the system may hang or skip an option ROM while scanning, if there is not enough space to load all ROMs.

IMPLICATION: Every device requires a certain amount of option ROM space to function. The N440BX has c800 to e000h available for high memory. However, certain configurations will not fit inside of this space causing the system to hang or leave out one or more add-in cards.

WORKAROUND: None identified at this time.

STATUS: NoFix.

14. Sensor data records cannot be read when server is in +5V standby power mode

PROBLEM: With the power off and the N440BX Server system in +5V standby power mode, the sensor data records cannot be read using the emergency management console or server management software.

IMPLICATION: When querying the baseboard management controller for sensor data records, no error is given and zero SDR records are reported even when SDR records are present.

WORKAROUND: None identified at this time.

STATUS: NoFix.

15. FRB3 errors are logged multiple times in the system event log

PROBLEM: Once the baseboard management controller has marked a processor as having a FRB 3 error, it is logged into the system event log on every boot. The FRB 3 error should only be logged on the first boot-up. This causes the error to appear as if an FRB 3 error is occurring on each and every boot, this is not the case.

IMPLICATION: The number of errors in the system event log is artificially inflated.

WORKAROUND: In order to clear the FRB 3 error enter BIOS setup and enable Processor Retest Option.

STATUS: NoFix.

16. Multi-bit memory errors indicated as voltage events in system event log viewer

PROBLEM: A multi-bit memory error is misreported as a voltage event in the system event log.

IMPLICATION: By injecting many multi-bit memory errors while the BIOS is trying to service the original error a voltage event is entered into the system event log. The BIOS handles the event normally and writes the event out to the BMC when it gets a single occurrence of a multi-bit memory error. The event is reported correctly.

WORKAROUND: None identified at this time.

STATUS: NoFix – This is normal operation.

17. Cannot clear the system event log in +5V standby power mode

PROBLEM: In +5V standby power mode with the baseboard management controller and system event log buffer either full or partially filled, a user can issue the "clear system event log" command. It will appear to execute normally but a "*Get System Event Log"* information command indicates the same system event log entry count reported just before the clear. Powering the BMC up completely (booting the system) and re-sending the "*Get System Event Log"* command will indicate that the only two events were power down and power up.

IMPLICATION: It will be necessary to power the system up and re-issue the "*Get System Event Log"* command to get the accurate system event log entry count after clearing the event log.

WORKAROUND: None identified at this time.

STATUS: Fix.

18. Watch Dog Timer failing to count down properly

PROBLEM: If the count down value is set to 12h or below, the timer counts down to zero very rapidly or instantaneously. On rare occasions it will count properly and count down to 08h in second intervals.

IMPLICATION: Processor test will fail and system will halt.

WORKAROUND: If the timer is set to 15h which is equivalent to 2 seconds it reliably counts down to 0 in 1 second intervals.

STATUS: NoFix.

19. Timing issues when N440BX Server system is in +5V stand-by power mode

PROBLEM: When the server is in +5V stand by power mode, the system event log and sensor data records time is zero. If the time is reset, it does not begin to increment while in +5V stand-by power mode.

IMPLICATION: Events that take place before the BIOS sets the time will have a Pre-Init time stamp.

WORKAROUND: None identified at this time.

STATUS: NoFix.

20. Intel EtherExpress™ PRO/100B 82558 driver will not load in Microsoft* Windows* 95

PROBLEM: The driver for the integrated 82558 network component on the N440BX DP Server baseboard will not load in Windows 95.

IMPLICATION: The integrated network component is inoperable upon installation of this driver.

WORKAROUND:

STATUS: Fixed. Enable PnP OS in the BIOS setup. Install Windows 95 with, or without, network support. In Control Panel, System, remove the network adapter under other bus, under PCI. Reboot the system, after which the system will find the NIC and request the driver. Insert the 2.0 82558 driver and choose the 82558 integrated controller with wired for management (wfm) support. Insert the Windows 95 CD and reboot. The network is now installed and it is possible to load other network support packages, such as TCP/IP.

21. PCI add-in card failure when configured in Slot 4 of the N440BX DP Server

PROBLEM: PCI add-in cards designed with the Intel i960® or Intelligent I/O cards may fail on the N440BX DP Server when configured in Slot 4 of the baseboard as a result of bus contention.

IMPLICATION: The system may hang if an Intelligent I/O card such as an Intel i960® is used in Slot 4. This only affects slot 4. Slot 4 my be used with any PCI card that does not use more than 1 interrupt line.

WORKAROUND: NONE

STATUS: NoFix:

22. Intel™ TestView Version 3.49 does not contain a VGA or hotswap backplane test package

PROBLEM: Cannot test the VGA or hotswap backplane with TestView V3.49

IMPLICATION:

WORKAROUND:

STATUS: Fixed. Update to the latest version of TestView. Version 4.03S.

23. Front Panel Drive Light Remains on when First Symbios SCSI channel is disabled.

PROBLEM: When the first Symbios channel is disabled and there are no devices attached, the hard drive activity light remains on after booting to the operating system.

IMPLICATION: HD indicator light is inaccurate.

WORKAROUND: This is fixed by installing the current Symbios driver under the operating system. This does not correct the activity light between the scan of the SCSI bus in POST to the point in which the operating system loads the driver.

STATUS: Fix.

24. The system will not boot to a 2nd or 3rd fixed disk when primary disk is not bootable.

PROBLEM: The N440BX will not boot to a drive that has a lower boot priority than a non-bootable drive that has #1 priority, as set in CMOS setup.

IMPLICATION: Explanation:

Each hard drive in the system is numbered sequentially in ascending order starting from 80. The number assigned to the drive is determined by one of the following methods:

1) For non-PnP compliant option ROMs or devices, the scan option ROM execution order determines the drive number. When the option ROM is invoked, it claims a range of drive numbers corresponding to the number of logical drives it possesses (0, 1, or more). Exact drive numbering can not be controlled by the BIOS when using non-PnP compliant option ROMs or devices.

2) For PnP compliant option ROMs or devices, the multi-boot component of the BIOS controls the order that drives are assigned by selectively invoking connection vectors in the option ROMs. Calling a connection vector signals the option ROM to claim a drive number. By controlling the order of the connection vector execution, the drive numbers may be assigned in a specific order. In general, once a drive number has been claimed/assigned, it can not be reclaimed or reassigned. The boot drive will always be drive 80 because the OS boot loader specifically requests data from drive 80. Since a drive number can not be reassigned if the drive fails to boot and the boot drive must be drive 80, no other hard drive may be booted from. The order of the drives in the multi-boot menus will determine how drives attached to the PnP-compliant option ROMs will be numbered.

WORKAROUND: None.

STATUS: NO Fix – This is normal operation.

25. Fixed disk boot sector write protect CMOS option does not protect against viruses.

PROBLEM: BIOS Setup option "Fixed Disk Drive Boot Sector- Write Protect" does not prevent viruses from writing to the master boot record MBR.

IMPLICATION: The system is susceptible to Virus infections.

WORKAROUND: None

STATUS: Fix.