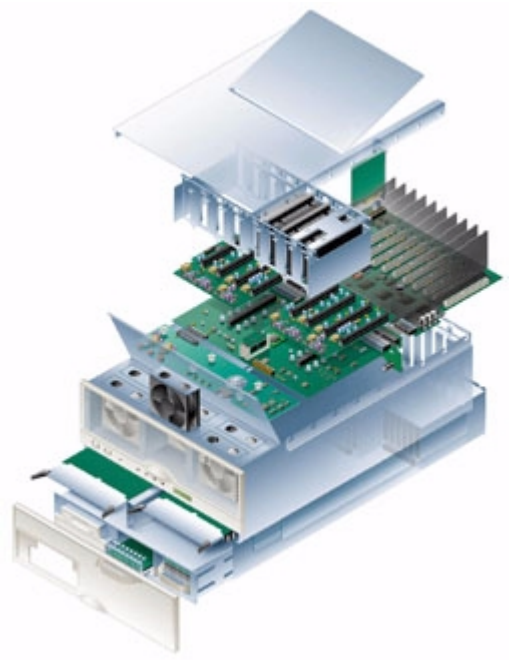

OPRF100 MP Board Set

Supporting Up To Eight Intel® Pentium® III Xeon™ Processors

Technical Product Specification

Intel Order #753673-001
Revision 1.0

Revision History

Date	Rev.	Modifications
August, 1999	1.0	Initial release.

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Conventions and Terminology

This document uses the following terms and abbreviations:

Term	Definition
ACPI	Advanced Configuration and Power Interface.
ASIC	Application Specific Integrated Circuit.
Asserted	Logic “Truth.” The “1” or active state. Active LOW signals end with “_L”.
ATE	Automated Test Equipment.
BIOS	Basic Input-Output System.
BitBLT	Bit Boundary Block Transfer.
BMC	Bus Management Controller, interfaces to SMIC and IPMB.
De-asserted	Logic “False.” The “0” or non-active state.
DFM	Design For Manufacturability.
DFT	Design For Testability.
DIB	Data Interface Buffer.
DIMM	Dual Inline Memory Module.
DWORD	Double Word. A 32-bit quantity.
ECC	Error Checking and Correcting.
EEPROM	Electrically Erasable Programmable Read-Only Memory.
EMP	Emergency Management Port.
FPC	Front Panel Controller.
FRU	Field Replaceable Unit.
FSB	Front Side Bus.
GTL+	Gunther Transceiver Logic.
HDM	High Density Metric.
I^2C* Bus	Two wire bi-directional serial bus, used as the carrier for IPMB.
ICMB	Intelligent Chassis Management Bus.
IDE	Integrated Drive Electronics, an interface to drives and storage devices.
IPMB	Intelligent Platform Management Bus.
IPMI	Intelligent Platform Management Interface.
IRQ	Interrupt Request.
ISA	Industry Standard Architecture.

ISP	In-System Programming.
ITP	In Target Probe.
JTAG	Joint Test Action Group. Defined the IEEE standard test access port and boundary scan architecture: IEEE Std 1149.1.
KB	Kilobyte. 1024 bytes.
LFM	Linear Feet per Minute.
LSB	Least Significant Bit.
LVDS	Low Voltage Differential SCSI.
MAC	Memory Access Controller.
MB	Megabyte.
MB/s	Megabytes per second.
MTBF	Mean Time Between Failures.
NIC	Network Interface Card.
NMI	Non-Maskable Interrupt.
OC	Open Collector.
OCP	Over Current Protection.
OEM	Original Equipment Manufacturer.
OVP	Over Voltage Protection.
PAL	Programmable Array Logic.
PCC	Power Control Circuitry.
PCI	Peripheral Component Interconnect. The I/O expansion bus.
PID	Programmable Interrupt Device.
PLD	Programmable Logic Device.
PMM	Processor Memory Module.
PS	Power Supply.
RAS	Reliability, Availability, Serviceability.
RTC	Real Time Clock.
RXD	Received.
SCI	System Control Interrupt.
SCSI	Small Computer Systems Interface, typically used for storage devices.
SECC	Single Edge Connector Cartridge.
SEL	System Event Log.
SMBus	System Management Bus.
SMI	Server Management Interrupt.

SMIC	Server Management Interface Controller.
SMM	Server Management Module or System Management Mode.
SMUX	SDRAM Multiplexer.
SPD	Serial Presence Detect.
SPI	Serial Parallel Interface.
TTL	Transistor-Transistor Logic.
TXD	Transmitted.
USB	Universal Serial Bus.
VID	Voltage ID.
VMC	Voltage Management Controller.
WOL	Wake-On-LAN*.

References

Refer to the following documents for additional information:

- *Advanced Configuration And Power Interface Specification*, Revision 1.0, 22 December 1996, http://www.teleport.com/~acpi.
- *Errata to the Advanced Configuration and Power Interface Specification*, Revision 1.0, http://www.teleport.com/~acpi.
- *ACPI Implementor's Guide*, v. 0.50, http://www.teleport.com/~acpi.
- *PC Registered DIMM Specification*, Revision 1.0, http://developer.intel.com/design/pcisets/memory/index.htm.
- *Pentium® Pro Family Developer's Manual*, Volume 1: Specifications. http://developer.intel.com/design/pro/manuals/index.htm.
- *82371AB PCI-TO-ISA/IDE Xcelerator (PIIX4) Data Sheet*, April, 1997, Intel Corporation, number 290562-001, ftp://download.intel.com/design/pcisets/datashts/29056201.pdf.
- *PC Serial Presence Detect Specification*, http://developer.intel.com/design/pcisets/memory/index.htm.

Table of Contents

1. Introduction

This document describes the architecture, functionality, and interfaces of the OPRF100 MP board set. This board set consists of several boards including the OPRF100 Profusion* carrier, processor mezzanine board, memory carrier, and midplane board. This board set is designed to be used in a high density rack mountable chassis and as such is designed to minimize the overall mechanical dimensions of the board set.

The OPRF100 MP board set is based on the Intel® Pentium® III Xeon™ processor and the Profusion PCIset. Both the processor and the chip set have been optimized for eight-way server applications.

Features:

- One to eight Pentium® III Xeon™ processors.
- Profusion* PCIset.
- Support for up to 32 GB of 3.3 V SDRAM (PC-100 registered DIMMs).
- Four peer 64-bit PCI buses (two 66-MHz and two 33-MHz buses, *PCI Local Bus Specification*, Rev. 2.1 [PCI, Rev. 2.1] compliant).
- Ten full-length, hot-plug PCI slots—four 66 MHz and six 33 MHz.
- Onboard dual channel Symbios* LVD SCSI controller for high performance mass storage devices.
- Onboard PCI video controller with 2-MB memory for standard server video requirements.
- IDE controller (integrated in PIIX4E).
- PIIX4E PCI to ISA bridge.
- Universal Serial Bus (USB) (integrated in PIIX4E).
- SMC* Super I/O component to handle all PC legacy functions (keyboard, mouse, serial, parallel).
- Programmable Interrupt Device (PID), a custom Intel ASIC which provides interrupt steering and I/O APIC facilities.
- Complete built-in server management capabilities.
- Intelligent Platform Management Interface (IPMI) compliant for communicating information between all boards in the chassis and between chassis.
- Field replaceable unit (FRU) information and temperature sensors stored on all boards (part number, serial number, board name).

Document Structure and Outline

The information contained in this document is organized into eight chapters. Each board in the OPRF100 MP board set is described in detail within its own chapter.

- **Chapter 1:Introduction**
  Provides an architectural overview of the OPRF100 MP board set.
- **Chapter 2:OPRF100 I/O Carrier**
  Details the I/O section of the OPRF100 MP board set.
- **Chapter 3:OPRF100 Profusion* Carrier**
  Details the processor section of the OPRF100 MP board set and the interface to the memory carrier and front panel.
- **Chapter 4:OPRF100 Processor Mezzanine Board**
  Details the processor mezzanine boards that hold up to four Pentium III® Xeon™ processors each.
- **Chapter 5:OPRF100 Memory Carrier**
  Details the memory section of the OPRF100 MP board set.
- **Chapter 6:OPRF100 Midplane**
  Details the interface between the Profusion* carrier and the I/O carriers.
- **Chapter 7:OPRF100 Cache Coherency Board**
  Provides information about the cache coherency board for the OPRF100 MP board set.
- **Chapter 8:OPRF100 Board Set Specifications**
  Provides information about board set power, thermal, and environmental specifications.
- **Chapter 9:OPRF100 BIOS Specifications**
  Provides information about the features and functionality of the BIOS.

1.1 Architecture Overview

A block diagram of the OPRF100 MP board set is shown below. The following sections describe aspects of the architecture in more detail.

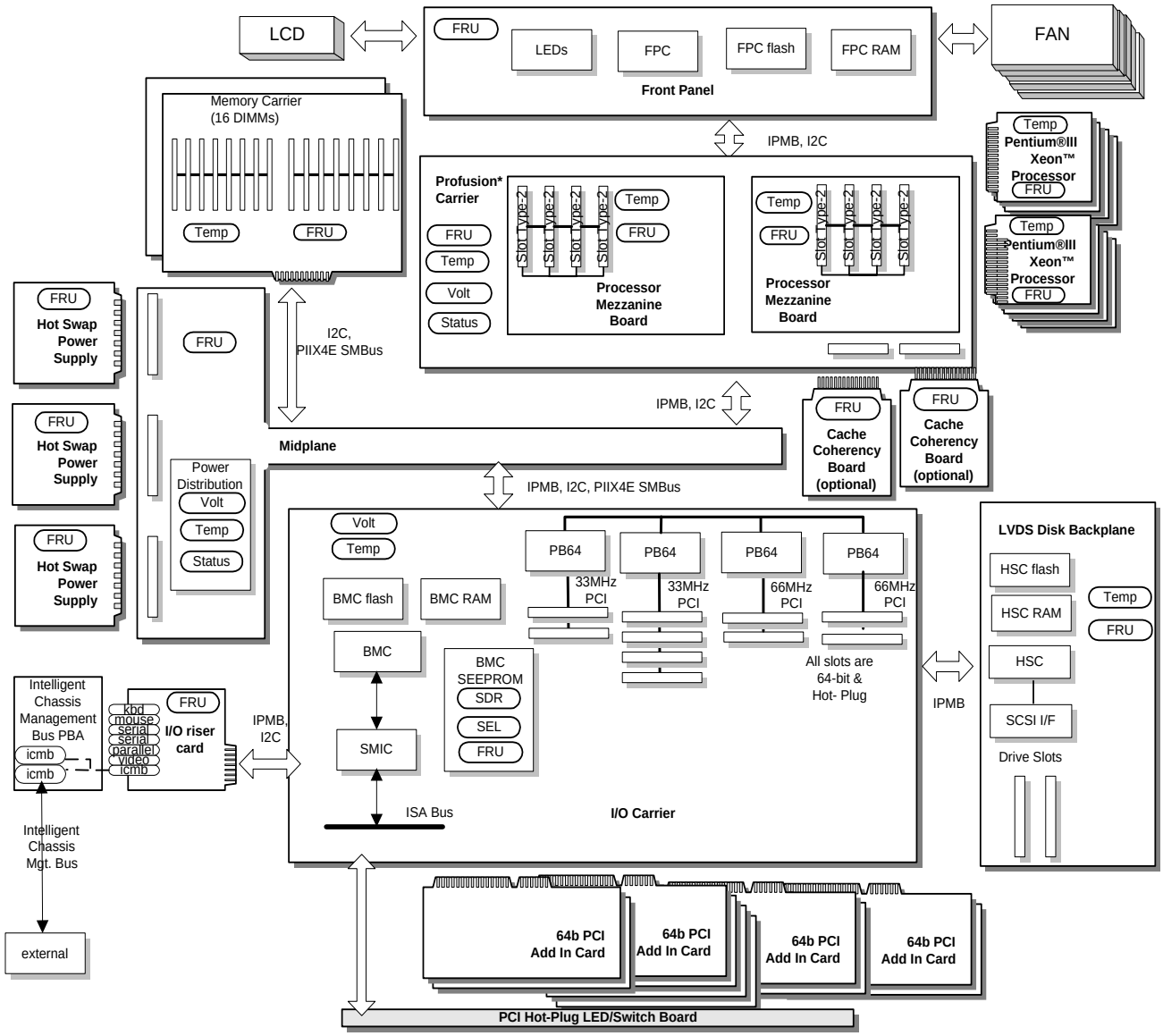

Figure 1-1: Block Diagram

1.1.1 Board Set Overview

The OPRF100 MP board set is a dual baseboard design that contains a total of seven individual board designs.

- Profusion* carrier (contains the Profusion chip set components).
- Processor mezzanine board (contains four Pentium® III Xeon™ processor slots and voltage regulators). There are up to two processor mezzanine boards per system.
- I/O carrier (contains all I/O functions including PCI slots).

- I/O riser card (plugs into the I/O carrier and contains all legacy connectors: video connector, parallel port, two serial ports, keyboard and mouse connectors, and USB connectors).
- Memory carrier (16-DIMM connectors; two carriers are supported for a total of 32 GB).
- Midplane (provides connection between the I/O carrier, memory carrier, and Profusion carrier and also provides the power interface for the board set).
- Cache coherency board (maintains coherency information used by the Profusion PCIset).

The baseboards, when installed into a chassis, are connected to each other by the midplane. A 100-MHz Pentium® Pro type I/O bus of the Profusion PCIset electrically connects the two baseboards together. Power to the board set is supplied through the midplane.

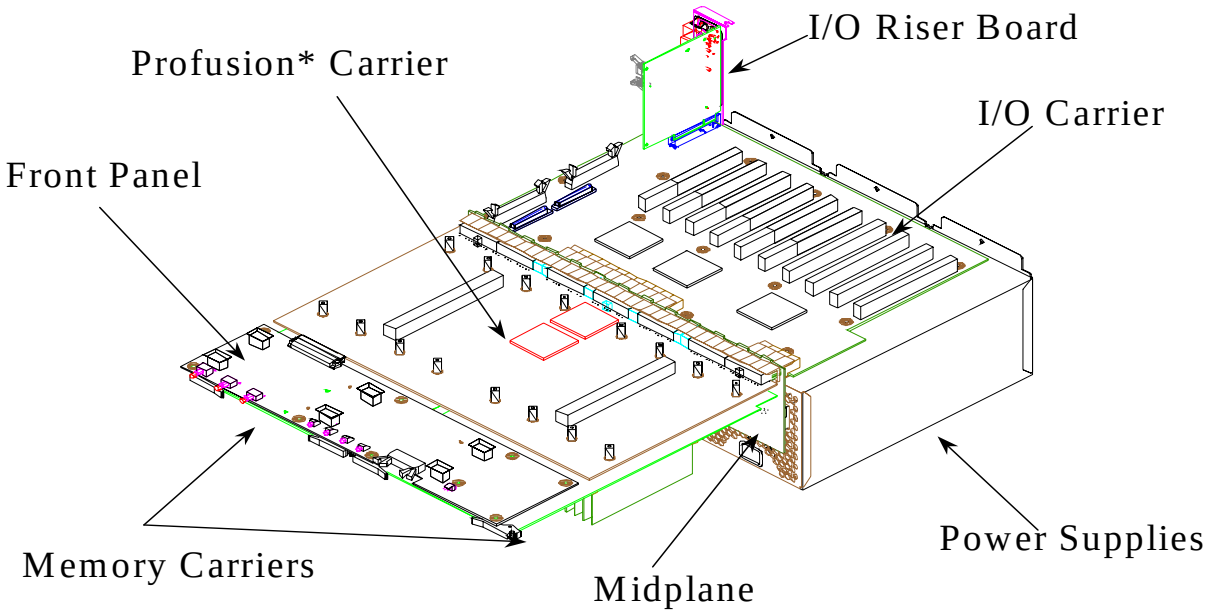

Figure 1-2: OPRF100 Board Set

1.1.1.1 OPRF100 Profusion* Carrier

The OPRF100 Profusion carrier supports one to two OPRF100 processor mezzanine boards. Each processor mezzanine board accepts one to four processors. Each processor is packaged in a single-edge connector cartridge (SECC), which includes a 100-MHz front-side bus (FSB) interface, a processor core, and a back-side bus which operates at the frequency of the processor core and supports 512KB, 1 MB, or 2 MB of L2 cache. See the appendices of this document for more information on mixed processor steppings. Hardware support for processor fault resilient boot (FRB) is provided. A450NX processor termination modules are required for any unoccupied processor slot. The only time A450NX processor termination modules are not required is when the mezzanine is not populated with processors. Whenever a processor is installed on either mezzanine, A450NX processor termination modules are required for the unpopulated slots.

The final load on each of the two front-side buses (one from each processor mezzanine board) is the Memory Access Controller (MAC) and Data Interface Buffer (DIB) components of the Profusion PCIset. This pair of chips interfaces to the memory subsystem and I/O bus, in addition to the

front-side bus. The memory subsystem interface is equipped with connectors for two OPRF100 memory carriers. Note that the I/O bus of the Profusion PCIset is intended for connection to PB64 (PCI bus 64-bit expander bridge component of the Profusion chip set) devices. It is not designed for other uses such as connection for other processor buses or cluster connections.

Power is supplied to the processors via integrated voltage regulators. There are a total of six voltage regulators on each processor mezzanine board. Four are used to supply the processor core voltages, and two supply the L2 cache voltages.

In addition to the facilities described above, the Profusion carrier also supports the OPRF100 server management architecture by providing nonvolatile storage of baseboard and server management data, digital and analog data monitoring hardware, defective processor monitoring and disabling controls, and access to memory carrier management data. See Chapter 3 for more details on the Profusion carrier and Chapter 4 for more details on the processor mezzanine board.

1.1.1.2 OPRF100 I/O Carrier

The OPRF100 I/O carrier provides the basis for a scaleable, high performance, high slot count I/O subsystem. Four 64-bit PCI bus segments are supported (all are peer buses) via four PB64s. Two 33-MHz (33-MHz/64-bit) segments host six PCI slots while the other two 66-MHz segments (66-MHz/64-bit) host four PCI slots for a total of 10 PCI slots in the system. All slots have hot-plug capability. Note that there is no ISA slot available.

The compatibility bus is the primary 33-MHz PCI segment that hosts the PIIX4E ISA south bridge (with one IDE interface and two USB ports), the Cirrus Logic* 5446 VGA controller (with 2 MB of onboard video memory), the Symbios 53C896* dual channel LVDS SCSI controller for storage device support (i.e., disks, CD-ROM, tape drive, etc.), and two 33-MHz/64-bit PCI slots. Also behind the PIIX4E is the SMC FDC37C937APM* Super I/O component, which provides two serial ports, a parallel port, a keyboard controller and PS/2 keyboard and mouse ports, a floppy disk interface, a real time clock, and GPIOs. Note that the connectors for the serial ports, the parallel port, the video, and the PS/2 keyboard and mouse ports are provided on a separate I/O riser card (which is part of the OPRF100 MP board set). The I/O riser card plugs vertically into the I/O carrier via a card edge connector.

The secondary 33-MHz PCI segment hosts four 33-MHz/64-bit PCI slots and the PID ASIC. The PID is a custom designed ASIC that provides interrupt steering functions (including support logic for use with the 8259A* interrupt controllers in the PIIX4E) and I/O APIC facilities. In addition to the standard IRQs, the PID supports a large number of PCI and onboard interrupt sources; a total of 64 interrupt routing table entries are available. Separate interrupt inputs will be provided for the four PCI interrupts of each PCI slot.

Each of the two 66-MHz PCI segments hosts two 66-MHz/64-bit PCI expansion slots.

In addition to the facilities described above, the I/O baseboard also implements the core of the OCPRF100 MP server system’s server management architecture.

The intelligent I/O node hardware will be provided only via add-in cards with embedded I/O processors; this provides a flexible and scaleable intelligent I/O solution appropriate for a high-end server product. See Chapter 2 for more details on the I/O carrier.

1.1.1.3 A450NX I/O Riser Board

The A450NX I/O riser board plugs vertically into the I/O carrier and provides all of the necessary legacy connectors for video, parallel, serial, keyboard, and mouse. The Intelligent Chassis Management Bus (ICMB) connects through the I/O riser card as well. All of the connectors are located on the riser card instead of the I/O carrier because of space constraints on the I/O carrier.

1.1.1.4 OPRF100 Memory Carrier

The OPRF100 MP board set supports up to two memory carriers. Each carrier provides 16 sites for PC-100 registered DIMMs, supporting up to a total of 32 GB of 100-MHz 3.3 V registered SDRAM; 64-Mbit, 128-Mbit and 256-Mbit SDRAMs may be used.[1] The minimum configuration is 128 MB of memory as implemented through installation of a single 128-MB PC-100 DIMM. The supported memory sizes range from 128 MB to 32 GB. Supported memory configurations are:

- 128, 256, 512, and 1024-MB PC-100 Registered DIMMs.
- 100 MHz SDRAM.
- Up to 32 DIMMs supported (using a total of 32 1024-MB DIMMs on both memory carriers).
- DIMMs may differ in size on a carrier but should be populated in pairs across carriers for interleaving.

The memory carrier contains a high speed SMX component to buffer and synchronize data between the SDRAMs and the Profusion PCIset. Each memory carrier can provide peak bandwidth of 800 MB/s. In order to achieve the maximum system memory bandwidth (1.6 GB/s peak), both memory carriers must be installed, and contain matched DIMMs.

The memory carrier also supports the IPMI server management architecture by providing FRU information via nonvolatile storage on the carrier. The DIMM Serial Presence Detect (SPD) EEPROM is read by BIOS via the SMBus in the PIIX4E for determination of the installed DIMM types and sizes. See Chapter 5 for more details about the memory carrier.

1.1.1.5 A450NX Processor Termination Module

The A450NX processor termination module provides the necessary electrical termination for the processor’s front-side gunning transceiver logic+ (GTL+) bus. A450NX processor termination modules are required for any unoccupied processor slot. The only time A450NX processor termination modules are not required is when the mezzanine is not populated with processors. Whenever a processor is installed on either mezzanine, A450NX processor termination modules are required for the unpopulated slots.

1.1.1.6 OPRF100 Midplane

The OPRF100 midplane provides bus interconnection between the Profusion, memory, and I/O carriers. This board also provides power distribution to the Profusion, memory, and I/O carriers

1. Contact your Intel sales representative for a listing of supported memory part numbers.

and to the peripheral bay from the three system power supply connectors. See Chapter 6 for more information on the midplane.

1.1.1.7 OPRF100 Cache Coherency Board

The OPRF100 cache coherency board is a high-capacity SSRAM memory board based on the Profusion PCIset. It maintains coherency information used by the chip set. The cache coherency board has been designed for use with the Profusion carrier, which has two cache coherency board connectors.

1.1.2 I/O Bus Support

1.1.2.1 PCI Bus

The OPRF100 MP board set provides four 64-bit PCI peer buses; two are 66 MHz and two are 33 MHz. There are a total of 10 PCI slots: four 66-MHz slots and six 33-MHz slots. All four PCI buses are compliant to the *PCI Local Bus Specification, Rev. 2.1*. The PCI buses are operated synchronously with the processor bus, using the processor bus clock as a master clock. The input clock, received over the midplane interface, is multiplied by two-thirds to support the 66-MHz PCI bus. The board set will support PCI adapters which draw power from both 3.3 V and 5 V, although the power allocation from 3.3 V may be limited. Note, the 64-bit slots will accept both 32 and 64-bit adapters. *PCI 2.1* peer to peer transfers are also supported.

1.1.2.2 ISA Bus

The Intel® 82371AB PCI to ISA/IDE Accelerator (PIIX4E) component provides the bridge interconnect from the primary PCI bus to an ISA bus. As implemented, the PIIX4E also provides one IDE channel as well as two USB interfaces. The ISA bus contains no slots, it is only used for communication to integrated devices such as the BIOS flash component, the SMC Super I/O component and the main OPRF100 MP board set's server management controller. The SMC Super I/O component provides all legacy connections including keyboard, mouse, floppy disk controller, one parallel port, and two serial ports. The server management interface chip (SMIC) and baseboard management controller (BMC) are the heart of the OPRF100 MP board set's server management functionality. The SMIC is implemented with a programmable logic device (PLD), while the BMC is implemented with an 80C652* microcontroller. The SMIC actually resides on the ISA bus, while the BMC is located behind the SMIC.

1.2 Component Details

1.2.1 Microprocessor

The OPRF100 MP board set supports the Pentium III Xeon processor. It is packaged in a 330-pin SECC, and contains a processor core, L2 cache components, and miscellaneous other components mounted to a fiberglass substrate. The substrate is then mounted to a cartridge, which includes a heat plate to which a heat sink is attached for heat dissipation.

The Profusion carrier has jumpers to support the ratio of processor core frequency to system bus frequency ranging from 2 to 7 in 1/2-step increments. This allows for selection of future proces-

sors up to 750 MHz. See Chapter 3 for more details on how to select the ratio. All processors in the system must be running at the same frequency. Also, mixed processor steppings will be supported on a limited basis. Refer to the appendices in this document for information on supported mixed stepping configurations. Refer to the *100-MHz Slot 2 Processor EMTS*, *Version 1.5*, for more information on the Pentium III Xeon processor.

1.2.2 Profusion* PCIset

The OPRF100 MP board set is based on the Profusion PCIset. The Profusion PCIset is optimized for server platforms and offers the following features not found on previous Intel® chip sets.

- Support for greater than 8 GB of memory addressing.
- Support for up to eight processors.
- 64-bit 66-MHz PCI bus support.

In addition, the I/O performance of the Profusion PCIset has been increased from previous chip sets.

- Dual 100-MHz front-side processor buses with a combined peak bandwidth of 1.6 GB/s.
- Dual dedicated 100-MHz memory buses with a combined peak bandwidth of 1.6 GB/s.
- Dedicated I/O bus with a peak bandwidth of 800 MB/s.

The Profusion PCIset is comprised of six components, consisting of three unique components:

- One MAC located on the Profusion carrier.
- One DIB located on the Profusion carrier.
- Four PB64s located on the I/O carrier.

1.2.2.1 Memory Access Controller (MAC)

The Memory Access Controller (MAC) is packaged in a ceramic ball grid array (CBGA) package. It provides the interface between both processor buses, both memory buses, and the I/O bus. The MAC dissipates 5-6 W and will be shipped without a heat sink.

1.2.2.2 Data Interface Buffer (DIB)

The Data Interface Buffer (DIB) is packaged in a 655-pin ball grid array (BGA) package. It provides the interface between both processor buses, both memory buses, and the I/O bus. The DIB dissipates 5-6 W and will be shipped without a heat sink.

1.2.2.3 PB64 (PCI bus 64-bit expander bridge component of the Profusion chip set)

The PB64 is packaged in a 456-pin BGA package. It provides the interface between the I/O bus and the PCI buses. Four PB64s are located on the I/O carrier. Each PB64 dissipates 7-8 W and the I/O carrier is planned to be shipped with a heat sink on each PB64.

1.2.3 Programmable Interrupt Device (PID)

The Programmable Interrupt Device (PID) is an ESG/Intel developed ASIC, which provides interrupt steering functions (including support logic for use with the 8259A interrupt controllers in the PIIX4E) and I/O APIC facilities. In addition to the standard IRQs, the PID supports a large number of PCI and onboard interrupt sources; a total of 64 interrupt routing table entries are available. A separate interrupt input will be provided for each of the four interrupts from every 64-bit PCI slot on the I/O carrier.

The PID is packaged in a 256-pin BGA package.

1.3 Performance

The core of the OPRF100 MP board set is the Pentium III Xeon processor and the Profusion PCIset. Below are the capabilities of each of the major buses on the OPRF100 MP board set. The values shown are peak bandwidth capable on the bus. Actual sustained bandwidth will be lower and will vary with the configuration of the server (i.e., adapter cards, O/S, etc.) and the application(s) being run.

Table 1-1: Peak Bus Bandwidth

Bus	Frequency	Bus Width	Peak Band Width	Signaling Technology
Processor	100 MHz	72-bits (64-data + 8 ECC)	800 MB/s	GTL+
Memory	100 MHz	72-bits (64-data + 8 ECC)	800 MB/s	GTL+
IO bus	100 MHz	72-bits (64-data + 8 ECC)	800 MB/s	GTL+
PCI-64	66 MHz	64-bits (64-data + 2 parity)	532 MB/s	TTL/LV-TTL

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2. OPRF100 I/O Carrier

This chapter describes the architecture of the OPRF100 I/O carrier. The I/O carrier mates with the Profusion* carrier and other boards of the OPRF100 MP board set through the midplane board. The I/O carrier contains all I/O interfaces for the server board set.

Features

The I/O carrier has the following features:

- Four functionally independent PCI buses.
- Integrated dual channel LVDS controller.
- Integrated Disk Electronics (IDE) controller supporting one IDE bus.
- Onboard video, serial, parallel, Universal Serial Bus (USB).
- Six hot-plug 33-MHz, 64-bit PCI slots.
- Four hot-plug 66-MHz, 64-bit PCI slots.
- Wake On LAN* hardware interface.
- I^2C* server management interface.

2.1 Architectural Overview

This section provides an overview of the I/O carrier, showing functional blocks and the component placement diagrams of the I/O carrier and I/O riser board.

The following figure illustrates the general architecture of the I/O carrier.

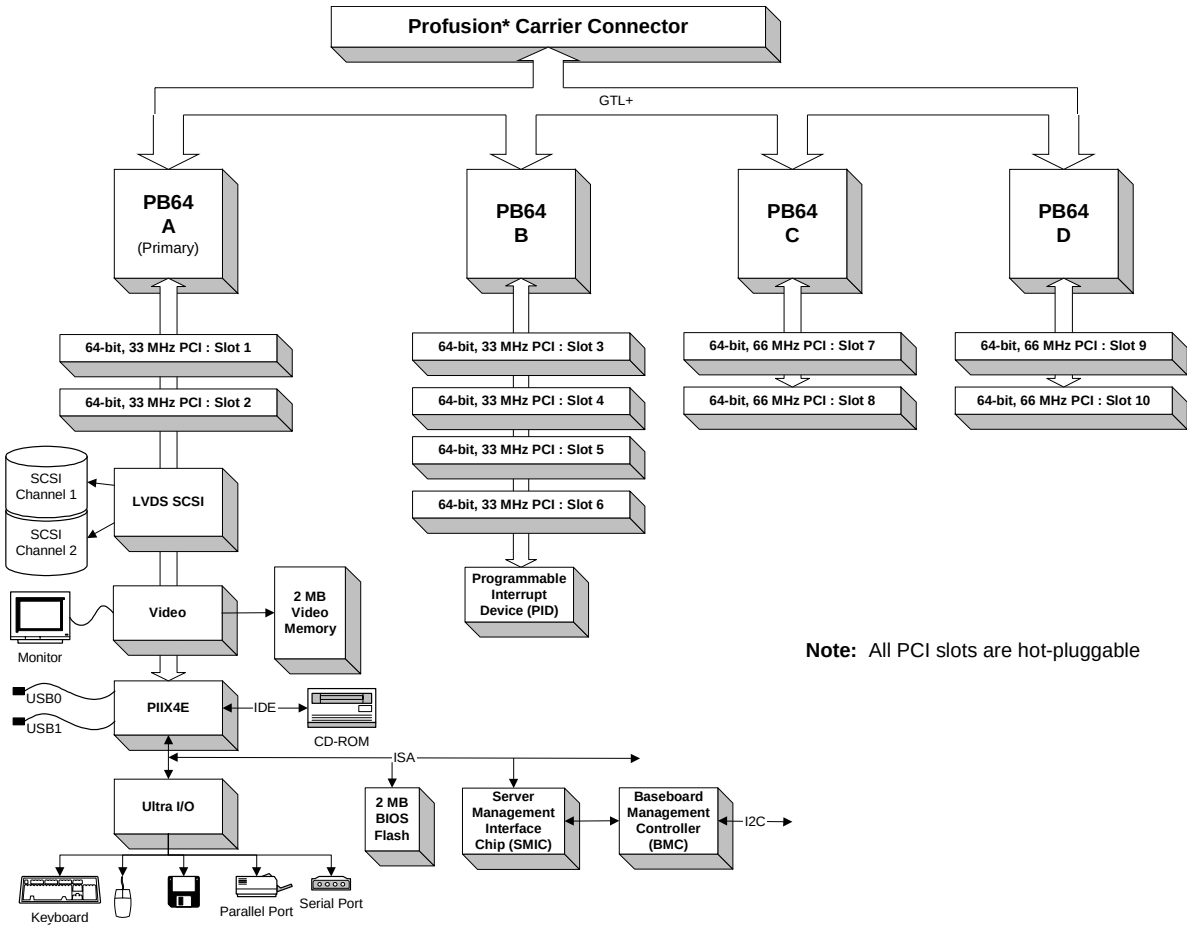


Figure 2-1: I/O Carrier Placement Plot

The I/O carrier provides the primary input/output interface of the OPRF100 MP board set. The carrier interfaces with the OPRF100 Profusion carrier through the midplane board.

2.1.1 I/O Bus Interface

The four PB64 components interface the MAC and DIB components through the midplane board with an I/O bus operating at 100 MHz. This I/O bus is a 64-bit wide bus and provides a peak bandwidth of 800 MB/s. For reliability, the address bus is parity protected and the data bus is ECC protected.

2.1.2 PCI Bus A

PCI Bus A operates at 64 bits, 33 MHz and fully adheres to the *PCI Specification, Revision 2.1*. PCI Bus A provides a peak bandwidth of 264 MB/s. This PCI bus is configured on the I/O carrier with the necessary devices to boot the operating system. The Intel® 82371AB PCI to ISA/IDE Accelerator (PIIX4E) component provides the bridge to Industry Standard Architecture (ISA) devices, IDE devices, and the USB interface. The boot flash ROM is directly connected to the ISA bus and under control of the PIIX4E. The arbiter for PCI Bus A resides in the PB64 component controlling this bus.

A Symbios* 53C896 Ultra2 SCSI chip provides two 16-bit high speed SCSI channels. This high performance SCSI chip is capable of providing data rates up to 80 MB/s per channel in 16-bit operations to insure maximum data throughput while minimizing PCI bus overhead.

Onboard video is supplied by a Cirrus Logic* GD5446 PCI video controller with 2 MB of onboard video EDO DRAM. The CL-GD5446 VisualMedia* accelerator is a 64-bit DRAM-based SVGA controller with hardware-accelerated BitBLT (bit boundary block transfer), video playback, and video capture to the frame buffer. It combines the Cirrus Logic V-Port* with a multiformat frame buffer for cost effective video playback. The onboard video also features a 64-bit GUI BitBLT engine with double-buffered, memory-mapped control registers.

Two 64-bit user accessible expansion slots are provided on this bus. Both PCI slots are hot-pluggable, adhering to the *PCI Hot Plug Specification, Revision 1.0*.

PCI Bus A is *PCI Specification, Revision 2.1* compliant and provides the user with two expansion slots for high bandwidth applications. Both PCI slots are hot-pluggable, adhering to the *PCI Hot Plug Specification, Revision 1.0*. PCI Bus A provides a peak bandwidth of 264 MB/s. Additional information is available in Section PCI Bus A.

Server management logic is also connected to this bus indirectly through the ISA bus. Additional information on the server management logic is available in Section Server Management Logic.

2.1.3 PCI Bus B

The 64-bit, 33-MHz PCI Bus B is also *PCI Specification, Revision 2.1* compliant. PCI Bus B provides a peak bandwidth of 264 MB/s. The Programmable Interrupt Device (PID), an Intel® designed Application Specific Integrated Circuit (ASIC), resides on the PCI bus for system interrupt steering. The PID contains the logic required to provide 8259A mode, APIC mode and Advanced Configuration and Power Interface (ACPI) functionality. The PID includes PCI, APIC, and PIIX4E interfaces. Refer to Section Programmable Interrupt Device for more information on the PID. The arbiter for PCI Bus B resides in the PB64 component controlling this bus.

Four 64-bit PCI expansion slots are provided on this bus. All four PCI slots are hot-pluggable, adhering to the *PCI Hot Plug Specification, Revision 1.0*. Additional information is available in Section PCI Bus B.

2.1.4 PCI Bus C

The 64-bit, 66-MHz PCI Bus C is *PCI Specification, Revision 2.1* compliant and provides the user with two expansion slots for high bandwidth adapters. Both PCI slots are hot-pluggable, adhering to the *PCI Hot Plug Specification, Revision 1.0*. PCI Bus C provides a peak bandwidth of 528 MB/s. Additional information is available in Section PCI Bus C.

2.1.5 PCI Bus D

The 64-bit, 66-MHz PCI Bus D is *PCI Specification, Revision 2.1* compliant and provides the user with two expansion slots for high bandwidth applications. Both PCI slots are hot-pluggable, adhering to the *PCI Hot Plug Specification, Revision 1.0*. PCI Bus D provides a peak bandwidth of 528 MB/s. Additional information is available in Section PCI Bus D.

2.1.6 Server Management Logic

The heart of server management is the Baseboard Management Controller (BMC). External communication can be established with the BMC through the Server Management Interface Controller (SMIC). For detailed information on the SMIC, see the Server Management Interface Controller (SMIC) section. The server management logic maintains a system event log (SEL) to store important system information. System voltage levels are monitored by the server management logic.

OPRF100 server management includes hardware to perform in-system programming (ISP) of the system programmable logic.

The server management logic also provides monitoring and control of other system devices including: video, floppy disk, chassis fans, and BIOS flash. See the Server Management section for details on server management logic.

2.1.7 A450NX I/O Riser Board

To conserve space on the I/O carrier, many legacy connections have been placed on a riser board attached to the I/O carrier. Connections to video, keyboard, mouse, two COM ports, one parallel port, and the Intelligent Chassis Management Bus (ICMB) interface are all provided through the A450NX I/O riser board.

2.1.8 Major Component Reference Tables

The following tables identify the major components and their reference designators.

Table 2-1: I/O Carrier Component Reference

Reference Designator	Name and Description	Reference Designator	Name and Description
J1A1	USB Connector.	U1C1	Cirrus Logic* GD5446 VGA Controller.
J1B1	A450NX I/O Riser Board Connector.	U2G1	Symbios* 53C896 LVDS.
J3B1, J3B2, J4B1, J5B1, J5B2, J6B1	33 MHz PCI Slots.	U1D1	SMC* Ultra I/O Component.
J7B1, J8B1, J8B2, J9B1	66 MHz PCI Slots.	U2D3	PIIX4E, PCI to ISA Bridge Device.
J2F1	In System Programming. (Used to program the SIMC and BMC PAL)	U2F2	SMIC (Server Management Interface Controller).
J1G1	IDE Connector: Primary Channel.	U4F2	BMC PAL

Table 2-1: I/O Carrier Component Reference (Continued)

J1E3	Floppy Disk Drive Connector.	U3H1	BMC (Baseboard Management Controller).
J3H1	Server Management Feature Connector.	U4H1	Flash to hold the BMC code. 32Kx8 (or 64Kx8), socketed device.
J1G2, J1E4	SCSI Connector (for peripheral devices).	U3G3	32Kx8 RAM for BMC.
J1F1, J1E2	Auxiliary I^2C* Connectors.	U5F2	PID.
J1E1	Wake On Lan*	U5H1	PB64-0 (PCI Bus Expander 0).
J2D1	Manufacturing Mode	U6H1	PB64-1 (PCI Bus Expander 1).
J2C1	PHP Header(Interface to Slot LED's and Switches)	U7H1	PB64-2 (PCI Bus Expander 2).
SW4G1	Configuration Switches.	U9H1	PB64-3 (PCI Bus Expander 3).
U2C3	2 MB BIOS Flash Device.	B6G1	Battery.
U2A2, U2A3, U2B1, U2B2	2 MB Video DRAM.		

Table 2-2: A450NX I/O Riser Board Component References

Reference Designator	Name and Description
J1	ICMB Connector.
J4	Combined Mouse and Serial Connector.
J5	COM 1 and COM 2 Serial Port Connectors.
J6	Combined Parallel and Video Connector.
J7	Edge Connector. Plugs into connector J3 on the I/O carrier.

2.2 Connector Signal Descriptions

This section defines the function of signal pins on all user accessible I/O carrier connector interfaces. The signal mnemonics defined here may appear in descriptive text throughout this document. An "_L" following a signal name indicates that the signal is active-low. (Note: this is the same convention used on schematics for active-low signals). One colon between numbers in square brackets indicates a range of signals (e.g., the notation [13:0] is a range of 14 unique sig-

nals). Refer to the Mechanical Specifications section for the connector pinout and mechanical information.

2.2.1 I/O Connector Signals

Most signals appearing on the I/O connector interfacing with the Profusion carrier are driven by the Profusion MAC and DIB components. These signals follow the GTL+ specification and use a Pentium® Pro bus protocol.

The following tables define the signals according to functional groups: I/O, Clock and Reset, Server Management, Legacy, JTAG, ISP, Front Panel, and Power Signals. Each PB64 on the I/O carrier is connected to the I/O bus on the Profusion carrier.

Table 2-3: I/O Bus Interface Signals

Signal(s)	Name and Description
IO_A[35:3]	**I/O Bus Address**. Address signals are the upper address bits issued with the current request.
IO_ADS_L	**I/O Bus Address Strobe**. Address Strobe indicates that the current cycle is the first of two cycles of a request.
IO_AERR_L	**I/O Bus Address Parity Error**. Address Parity Check is asserted when either an address or request parity error occurs.
IO_AP[1:0]_L	**I/O Bus Address Parity**. Address Parity is the parity computed over the address; IO_AP[1] covers IO_A[35:24], and IO_AP[0] covers IO_A[23:3].
IO_BERR_L	**I/O Bus Data Error**. Bus Error indicates an unrecoverable data error.
IO_BINIT_L	**I/O Bus Initialization**.
IO_BNR_L	**I/O Bus Block Next Request**. Block Next Request blocks the current request bus owner from issuing new requests.
IO_BPRI_L	**I/O Bus Priority Request**. Priority Agent Bus Request is issued by the high-priority bus agent to acquire the request bus. The high-priority agent is always the next bus owner. (This is an input on the Pentium® Pro I/O bus.)
IO_D[63:0]	**I/O Bus Data**. Each set of 72 data signals moves data to/from an SDRAM array. Sixty-four signals are used for the actual data and the other eight signals carry ECC information.
IO_DBSY_L	**I/O Bus Data Bus Busy**. Data Bus Busy is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
IO_DEFER_L	**I/O Bus Defer**. IO_DEFER is driven by the addressed agent to indicate that bus completion cannot be guaranteed for the transaction.
IO_DEP_L[7:0]	**I/O Bus ECC**. Each set of 72 data signals moves data to/from an SDRAM array. Sixty-four signals are used for the actual data and the other eight signals carry ECC information.

Table 2-3: I/O Bus Interface Signals

IO_DRDY_L	**I/O Bus Data Ready**. Data Ready is asserted for each cycle in which data is transferred.
IO_HIT_L	**I/O Bus Hit**. Hit indicates that a caching agent holds an unmodified version of the requested line. Hit is also driven in conjunction with IO_HITM to extend the snoop window.
IO_HITM_L	**I/O Bus Hit Modified**. Hit Modified indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Hit Modified is also driven in conjunction with IO_HIT to extend the snoop window.
IO_LOCK_L	**I/O Bus Lock**. Lock is asserted for an indivisible sequence of transactions.
IO_REQ[4:0]_L	**I/O Bus Request**. In the first cycle of a request, these signals carry the request type. In the second cycle, they carry the data size and transfer length.
IO_RESET_L	**I/O Bus Reset**. (This signal is an input on the Pentium Pro I/O bus.)
IO_RP_L	**I/O Bus Request Parity**. Request Parity is the parity computed over IO_ADS and IO_REQ[3:0].
IO_RS[2:0]_L	**I/O Bus Response**. Response indicates the type of response.
IO_RSP_L	**I/O Bus Response Parity**. Response Parity is parity computed over IO_RS[2:0].
IO_TRDY_L	**I/O Bus Target Ready**. Target Ready indicates a valid response cycle.

The I/O Connector Clock and Reset Signals table is a summary of I/O connector clock and reset signal pins, including the signal mnemonic, name, and brief description.

Table 2-4: I/O Connector Clock and Reset Signals

Signal(s)	Name and Description
IO_PWRGD	**I/O Power Good**. Inactive state resets the Profusion* carrier. Note that this power good signal transitions when the front panel resets the system.
IO_RESET_L	**I/O Bus Reset**. This signal is driven from the primary PB64 and is an input on the Pentium® Pro I/O bus.
PB64_A_CRESET_L	**Delayed CPU Reset**. This reset is asserted eight clocks after IO_RESET_L for devices that use IO_RESET_L for logic.
PB64_A_CLK	**Pentium Pro Bus Clock**. All Pentium Pro bus timings are referenced to the rising edge of this clock. This clock is driven to the PB64 on PCI Bus A.
PB64_B_CLK	**Pentium Pro Bus Clock**. All Pentium Pro bus timings are referenced to the rising edge of this clock. This clock is driven to the PB64 on PCI Bus B.

Table 2-4: I/O Connector Clock and Reset Signals (Continued)

PB64_C_CLK	**Pentium Pro Bus Clock**. All Pentium Pro bus timings are referenced to the rising edge of this clock. This clock is driven to the PB64 on PCI Bus C.
PB64_D_CLK	**Pentium Pro Bus Clock**. All Pentium Pro bus timings are referenced to the rising edge of this clock. This clock is driven to the PB64 on PCI Bus D.
PWR_GOOD	**Power Good**. This signal provides a power-on reset to the MAC and DIB. The signal is a 3.3 V tolerant signal and indicates that the clocks and power supplies are within their specifications. The signal remains low (capable of sinking leakage current) without glitches from the time that the power supplies are turned on until they become valid. The signal then transitions monotonically to a high (3.3 V) state within 100 ns.
PWRGDB	**Buffered Power Good**. Buffered version of Profusion carrier power good input to PB64. This signal indicates when power is good throughout the entire system.

The I/O Connector Server Management Signals table is a summary of server management signal pins, including the signal mnemonic, name, and brief description.

Table 2-5: I/O Connector Server Management Signals

Signal(s)	Name and Description
CPU_SPI_RESET_L	**CPU SPI Reset**. Driven by SMIC to reset CPU SPI chain.
I2C_BMC_SCL	**BMC I^2C Clock**. Clock reference for the local BMC I^2C* bus. This bus is controlled by the BMC.
I2C_BMC_SDA	**BMC I^2C Data**. Serial data transfer for the local BMC I^2C bus. This bus is controlled by the BMC.
I2C_DS2P0_SCL	**CPU0 I^2C Clock**. Clock reference for the I^2C bus to the first processor mezzanine board. This bus is controlled by the BMC.
I2C_DS2P0_SDA	**CPU0 I^2C Data**. Serial data transfer for the I^2C bus to the first processor mezzanine board. This bus is controlled by the BMC.
I2C_DS2P1_SCL	**CPU1 I^2C Clock**. Clock reference for the I^2C bus to the second processor mezzanine board. This bus is controlled by the BMC.
I2C_DS2P1_SDA	**CPU1 I^2C Data**. Serial data transfer for the I^2C bus to the second processor mezzanine board. This bus is controlled by the BMC.
I2C_GLOBAL_SCL	**Global I^2C Clock.** Main I^2C clock connecting all microcontrollers on all system boards.
I2C_GLOBAL_SDA	**Global I^2C Data**. Main I^2C data connecting all microcontrollers on all system boards.

Table 2-5: I/O Connector Server Management Signals (Continued)

SPI_CLK	**SPI Clock**. Clock used for the Serial-Parallel Interface chains.
SPI_CPU_SEL_L	**SPI CPU Chain Select**. Selects one of the CPU SPI chains for reading or writing. The subselects are used to select exactly which chain.
SPI_MISO	**SPI Chain Serial Input**. This is the data input for the serial SPI chain.
SPI_MOSI	**SPI Chain Serial Output**. This is the data output for the serial SPI chain.
SPI_SEL0_L	**SPI Chain Subselect 0**. Selects the appropriate CPU SPI chain for reading or writing.
SPI_SEL1_L	**SPI Chain Subselect 1**. Selects the appropriate CPU SPI chain for reading or writing.
SPI_SEL2_L	**SPI Chain Subselect 2**. Selects the appropriate CPU SPI chain for reading or writing.

The I/O Connector Legacy Signals table is a summary of legacy signal pins, including the signal mnemonic, name, and brief description.

Table 2-6: I/O Connector Legacy Signals

Signal(s)	**Name and Description**
A20M_L	**Address 20 Mask**. PIIX4E asserts A20M# to the CPU based on combination of port 92 register, bit 1 (FAST_A20), and A20GATE input signal.
ADC_OSC_RESET	**Initialize A/D clock**. This signal initializes the A/D oscillator to a reliable value.
CPU_SLP_L	**CPU Sleep**. This pin is driven by the PIIX4E to the processor and puts it into the sleep state.
FERR_L	**Numeric Coprocessor Error**. This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the CPU. If FERR# is asserted, PIIX4E generates an internal IRQ13 to its interrupt controller unit. PIIX4E then asserts the INT output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active.
IGNNE_L	**Ignore Numeric Exception**. This signal is connected to the ignore numeric exception pin on the CPU. Used only if the PIIX4E coprocessor error reporting function is enabled. If FERR# is active, indicating a coprocessor error, a write to the coprocessor error register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the coprocessor error register is written, the IGNNE# signal is not asserted.

Table 2-6: I/O Connector Legacy Signals (Continued)

INIT_L	**Initialization**. Asserted in response to any one of the following conditions. When the system reset bit in the reset control register is reset to 0 and the reset CPU bit toggles from 0 to 1, PIIX4E initiates a soft reset by asserting INIT. PIIX4E also asserts INIT if a shut down special cycle is decoded on the PCI bus, if the RCIN# signal is asserted, or if a write occurs to port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated.
INTR	**CPU Interrupt**. INTR is driven by PIIX4E to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state.
MEM_SBCERR_L	**Single-Bit Corrected Memory Error and Performance Counter overflow**. This is an input to the PID.
PIC_CLK	**APIC Clock**. PIC_CLK is used to determine when valid data is being sent over the APIC bus (PICD[1:0]).
PICD[1:0]	**APIC data**. PICD[1:0] are bidirectional signals used to send and receive data over the APIC bus.
PIIX_SMB_SCL	**SM Bus Clock**. System management bus clock used to synchronize transfer of data on SMBus.
PIIX_SMB_SDA	**SM Bus Data**. Serial data line used to transfer data on SMBus.
PIIX_SMB_SEL0	**SM Bus Select 0**. The SM Bus was split into four separate SM buses in order the support the large number of DIMMs in main memory. This pin is select 0 for the multiplexer on the Profusion* carrier.
PIIX_SMB_SEL1	**SM Bus Select 1**. The SM Bus was split into four separate SM buses in order the support the large number of DIMMs in main memory. This pin is select 1 for the multiplexer on the Profusion carrier.
STOP_CLK_L	**Stop Clock**. This signal is output from the PIIX4E and connects directly to the CPU. STOP_CLK_L is synchronous to the PCI clock on PCI Bus A.

The I/O connector JTAG Signals table is a summary of JTAG signal pins, including the signal mnemonic, name, and brief description. The I/O carrier boundary scan chain is connected to the chain on the Profusion carrier. The chain is accessible via the ITP connector on the Profusion carrier. See Section Boundary Scan for additional information.

Table 2-7: I/O Connector JTAG Signals

Signal(s)	Name and Description
IO_TCK	**Test Clock**. Test clock is used to clock state information and data into and out of the device during boundary scan.

Table 2-7: I/O Connector JTAG Signals (Continued)

IO_TDI	**Test Data Input**. Test input is used to serially shift data and instructions into the TAP.
IO_TDO	**Test Data Output**. Test output is used to shift data out of the device.
IO_TMS	**Test Mode Select**. Test mode select is used to control the state of the TAP controller.
IO_TRST_L	**Test Reset**. Test Reset is used to reset the TAP controller logic. For normal operation, TRST_L must be asserted low after PWRGD is asserted.

The following tables describe the signals used to program various devices inside the chassis.

Table 2-8: I/O Connector In-system Programming Signals

Signal(s)	Name and Description
GLOBAL_MODE	**Global ISP Mode**. This is the mode pin required for Lattice* In-system-Programming and allows the BMC to program all Lattice parts throughout the system.
GLOBAL_SCLK	**Global ISP Clock**. This is the clock pin required for Lattice In-system-Programming and allows the BMC to program all Lattice parts throughout the system.
GLOBAL_SDI	**Global ISP SDI**. This is the serial data-in pin required for Lattice In-system-Programming and allows the BMC to program all Lattice parts throughout the system.
ISP_CPU_EN_L	**CPU ISP Enable**. This pin enables the Lattice parts on the Profusion* carrier for In-system Programming.

Table 2-9: I/O Connector Front Panel Signal Descriptions

Signal(s)	Description
COM2_TO_FP_EN	**COM2 Front Panel Redirect**. Connects the COM2 transceiver to the front panel for front panel redirection.
COM2_TO_SIO_EN_A	**COM2 SuperIO Redirect**. Connects the COM2 transceiver to the Super I/O chip and the XIMB transceiver to the front panel.
FAN_FAILED_L	**Fan Failure**. Signal from the power distribution board indicating a fan failure.
FP_NMI_SWT_L	**System-NMI Switch**. This is debounced by the BMC.

Table 2-9: I/O Connector Front Panel Signal Descriptions (Continued)

FP_TO_PIIX_PWRBTN	**Front Panel Power Button**. This pin is driven to the PIIX4E to indicate that the power button was pressed on the front panel. The PIIX4E performs a 16-ms debounce of this signal.
HARD_RESET	**Hard Reset**. Overall system reset from FP asserted >500 ms. Deassert >=0 ms.
I2C_BACKUP_SCL	**Backup I^2C* Bus Clock**. This bus operates under standby voltage and allows the front panel access to the SEL on the I/O carrier.
I2C_BACKUP_SDA	**Backup I^2C Bus Data**. This bus operates under standby voltage and allows the front panel access to the SEL on the I/O carrier.
I2C_CEL_CONNECT_BMC_A	**SEL to BMC Connect**. Connects SEL serial EEPROM to the I/O Carrier's BMC.
I2C_CEL_CONNECT_FPC	**SEL to FPC Connect**. Connects SEL serial EEPROM to front panel's FPC.
I2C_FPC_SCL	**Front Panel Private I^2C Bus Clock**.
I2C_FPC_SDA	**Front Panel Private I^2C Bus Data**.
INTRUSION_L	**Intrusion**. Indicates disk door has been opened. Driven from SCSI hot-swap backplane.
NMI_5V	**Non-Maskable Interrupt**. Driven to CPU.
PROC_RESET_L	**Processor Reset Status**. This signal indicates that The CPU is actively being held in reset state.
PWR_CNTRL_RTC_L	**RTC Power Control**. Power control signal from Super I/O. High time >5 ms. Low time 5 ms.
PWR_CNTRL_SFC_L	**SFC Power Control**. Power control signal from the server monitor module. High time >=5 ms. Low 5-100 ms.
RI_TTL_FP	**COM2 redirection signal**. This signal remains active at the front panel connector even when COM2 has been connected to the I/O carrier's Super I/O component.
SECURE_MODE_BMC	**BMC Secure Mode**. Signal from the BMC PAL indicating a system-secure state.
SIN_TTL_COM2	**COM2 redirection signal**. This signal remains active at the front panel connector even when COM2 has been connected to the I/O carrier's Super I/O component.
SIN_TTL_XIMB	**ICMB receive**.
SMI_L	**System Management Interrupt**.
SOUT_TTL_COM2	COM2 redirection signal.
SOUT_TTL_XIMB	**ICMB transmit**.
SPEAKER_DATA	**Speaker**. An amplified version of this signal drives the front panel's speaker.

Table 2-9: I/O Connector Front Panel Signal Descriptions (Continued)

XIMB_SOUT_EN	**Open collector signal**. Output enables the ICMB transceivers TXD RS485 output.

The following table is a summary of power pins, including the signal mnemonic, name, and brief description.

Table 2-10: I/O Connector Power Pins

Signals(s)	Type	Name and Description
GND	PWR	**Ground**. Power supply ground.
-12V	PWR	**-12 V power supply**.
3.3V	PWR	**3.3 V power supply**.
5V	PWR	**5 V power supply**.
12V	PWR	**12 V power supply**.
VCC_STDBY	PWR	**5 V standby.** Standby power from power supply.

2.2.2 PCI Signal Descriptions

The following table is a summary of PCI signal pins, including the signal mnemonic, electrical type, full name, and brief description. The PCI implementation on the I/O carrier supports 33- and 66-MHz, 64-bit PCI bus operation. The signals supported are listed in the table. The electrical types are as follows:

Table 2-11: PCI Electrical Levels

Type	Description
in	Input is a standard input-only signal.
o/d	Open Drain allows multiple devices to share signals as a wired-OR.
out	Totem Pole Output is a standard active driver.
s/t/s	Sustained Tri-State is an active low tri-state signal owned and driven by one and only one agent at a time, subject to specific timing restrictions.

Table 2-11: PCI Electrical Levels (Continued)

t/s	Tri-State is a bi-directional, tri-state input/output pin.

Table 2-12: PCI Signal Descriptions

Signal(s)	Type	Name and Description
ACK64_L	s/t/s	**Acknowledge 64-bit Transfer** indicates that the PCI target is willing to transfer data using 64 bits.
AD[63:00]	t/s	**Address and Data** are multiplexed; during the first clock of a transaction (address phase) they contain a 32-bit physical address; during subsequent clocks, data. As address bits, AD0 and AD1 have no significance; instead, they are encoded to indicate the burst type.
C/BE[7:0]_L	t/s	**Bus Command and Byte Enable** are multiplexed; during the address phase of a transaction, C/BE[3:0]_L defines the bus command; during the data phase C/BE[3:0]_L determines which byte lanes carry valid data.
DEVSEL_L	s/t/s	**Device Select**, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, it indicates whether any device on the bus has been selected.
FRAME_L	s/t/s	**Cycle Frame** is driven by the current master to indicate the beginning and duration of an access.
GNT_L	in	**Grant** indicates to the agent that the arbiter has granted access to the bus. This is a point-to-point signal. Every master has its own GNT_L.
IDSEL	in	**Initialization Device Select** is used as a chip select instead of the upper 20 address lines during configuration read and write transactions.
INT[A:D]_L	in	**PCI interrupt** signals from add-in card. Onboard devices may also generate these signals, which are managed by the PID.
IRDY_L	s/t/s	**Initiator Ready** indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. During a write, IRDY_L indicates that valid data is present. During a read, it indicates the master is prepared to accept data.
LOCK_L	s/t/s	**Lock** indicates an atomic operation that may require multiple transactions to complete.
M66EN	In	**66MHZ_Enable** indicates to a device if the bus segment is operating at 66 or 33 MHz.
PAR	t/s	**Parity** indicates even parity across AD[31:00] and C/BE[3:0]_L. Parity generation is required by all PCI agents.
PAR64	t/s	**Parity64** indicates even parity for the upper 32 bits of data on AD[63:32].
PCICLK		**Bus Clock** for this PCI segment, synchronous with processor local bus. May be either 33 MHz or 30 MHz, depending on processor frequency. Default is 33 MHz.
PERR_L	s/t/s	**Parity Error** reports a data parity error on all commands except Special Cycle.
REQ_L	out	**Request** indicates to the arbiter that this agent desires use of the bus. This is a point-to-point signal. Every master has its own REQ_L.

Table 2-12: PCI Signal Descriptions (Continued)

REQ64_L	s/t/s	**Request 64-bit Transfer**, when actively driven by the current bus master, indicates it desires to transfer data using 64 bits.
PCIRST_L	in	**Reset** forces the PCI sequencer of each device to a known state.
SERR_L	o/d	**System Error** reports address parity errors, data parity errors on Special Cycle commands, or any other system error where the result will be catastrophic.
STOP_L	s/t/s	**Stop** indicates the current target is requesting the Master to stop the current transaction.
TRDY_L	s/t/s	**Target Ready** indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. During a read, TRDY_L indicates that valid data is present. During a write, it indicates the target is prepared to accept data.

2.2.3 SCSI Signal Descriptions

The following table is a summary of the SCSI connector signal pins, including the signal mnemonic, name, and brief description.

Table 2-13: SCSI Signal Descriptions

Signal Name	Type	Description
-ACK[P,M]	LVDS	**Transfer Acknowledge**.
-ATN[P,M]	LVDS	**Attention**.
-BSY[P,M]	LVDS	**Bus Busy**.
-C/D[P,M]	LVDS	**Control/Data**. If true (logic 0) = Control Phase. If false (logic 1) = Data Phase.
-DB(0:15)[P,M]	LVDS	**Data Bus**.
-DBP(0:1)[P,M]	LVDS	**Parity**. DBP0: DB(15:8). DBP1: DB(7:0).
-I/O[P,M]	LVDS	**Direction**. If true (logic 0) I = Input to initiator. If false (logic 1) O = Output from initiator.
-MSG[P,M]	LVDS	**Message Phase**.
-REQ[P,M]	LVDS	**Transfer Request**.
-RST[P,M]	LVDS	**Bus Reset**. All devices on bus will reset.

Table 2-13: SCSI Signal Descriptions (Continued)

-SEL[P,M]	LVDS	**Arbitration**.
DIFFSENSE	Analog	**SCSI Mode Sense**.
GROUND	Power	**Electrical Ground**.
TERMPWR	Power	**Terminator Power**. Static 5 volts.

2.2.4 ISA Signal Descriptions

The following table is a summary of ISA signal pins, including the signal mnemonic, name, and brief description. An ISA “bus master” can be either the Super I/O chip or the SMIC.

Table 2-14: ISA Signal Descriptions

Signal(s)	Name and Description
AEN	**Address Enable**. When negated, an I/O slave responds to addresses and I/O commands.
BALE	**Bus Address Latch Enable**. At the falling edge, indicates a valid address on LA[23:17].
BCLK	**Bus Clock**. Synchronizes events on the ISA bus (at 8.33 MHz nominal).
SD[15:8]	**Data Bus High**. High-order 8-bits of 16-bit data bus (byte lane 1) on ISA connector.
SD[7:0]	**Data Bus Low**. Low-order 8-bits of 16-bit data bus (byte lane 0) on ISA connector.
DACK[7:0]_L	**DMA Acknowledge**.
DRQ[7:0]	**DMA Request**.
IOCS16_L	**16-bit I/O Capable**. Indicates that this is a 16-bit I/O slave.
IOCHK_L	Signals a serious error.
IORC_L	**Slot I/O read command**.
IOWC_L	**Slot I/O write command**.
IRQx	**Interrupt Request**. x = interrupt number.
LA[23:17]	**Latchable Address**.
MASTER16_L	**16-bit ISA Master Indicator**.
MEMCS16_L	**16-bit Memory Capable**. Only ISA memory slaves generate this signal.
MRDC_L	**Slot Memory Read Command**.
MWTC_L	**Slot Memory Write Command**.

Table 2-14: ISA Signal Descriptions (Continued)

NOWS_L	**No Wait State**. An ISA slave asserts NOWS_L to indicate that no more clock cycles are required to complete this transaction.
OSC	**Oscillator**. 14.31818 MHz clock for timer loops.
REFRESH_L	**Refresh**. When asserted, indicates that a memory refresh cycle is in progress. An ISA master can also assert this signal to request that the platform execute a refresh cycle.
RESDRV	**ISA Reset**. When asserted, causes a hard reset of ISA expansion boards.
SA[19:0]	**System Address**. This address is valid throughout the entire bus command cycle.
SBHE_L	**System Bus High Enable**. When asserted, indicates that the expansion board should drive data on the high-order byte of SD[15:0].
SMRDC_L	**System Memory Read Command**. When asserted by the system board, indicates that the addressed memory slave may drive data. Only asserted during ISA read accesses from 00000000H through 000FFFFFH.
SMWTC_L	**System Memory Write Command**. When asserted by the system board, indicates that the addressed memory slave may latch data. Only asserted during ISA write accesses to 00000000H through 000FFFFFH.
TC	**Terminal Count**. As an output, indicates that the DMA word count rolls over from 0 to 0FFFFFFH. As an input, indicates that the DMA slave wants to terminate the transfer.

2.2.5 IDE Signal Descriptions

The following table is a summary of the IDE interface connector signal pins, including the signal mnemonic, name, and brief description.

Table 2-15: IDE Signal Descriptions

Signal	Name and Description
CS1P_L	**Select Command Register Block**.
CS3P_L	**Select Control Register Block**.
CSEL	**Cable Select**. Tells who is master drive (drive 0). This is also SPSYNC (Spindle Sync).
DA[2:0]	**Register Select Address.** (from ISA address bus).
DACK_L	**Direct Memory Access (DMA) Acknowledge**.
DD[15:0]	**ISA Data**.
DIOR_L	**Read Request**. Handshake request for read operations.
DIOW_L	**Write Request**. Handshake request for write operations.

Table 2-15: IDE Signal Descriptions (Continued)

DRQ	**Direct Memory Access (DMA) Request**.
HDACT_L	**Disk Drive Present** (power up) or active.
IORDY	**Ready**. Optional. Device ready for operation (high).
IRQ14	**Interrupt Request**.
RSTDRV_L	**Reset**. Forces drivers on the ISA bus to initialize.

2.2.6 Server Monitor Module Feature Connector (SFC)

The feature connector is provided for use by an IPMI compliant server monitor module. The signals provided by this connector allow the server monitor module to take full control of the system.

Table 2-16: SMM Feature Connector

Name	Description	Type	V/I Characteristics[1]
+3.3V	**3.3V Power**.	PWR	
+5V	**5 V Power**.	PWR	
GND	**Electrical Ground**.	PWR	
I2C_BACKUP_SCL	**Backup I^2C* Bus Clock**. This bus operates under standby voltage and allows the front panel access to the SEL on the I/O carrier.	I/O	$V_{OL} \leq 0.6V$ @ 8.5mA (open-drain) $V_{IL} \leq 0.6V$ @ ± 1.0µA $V_{IH} \geq 1.4V$ @ ± 1.0µA
I2C_BACKUP_SDA	**Backup I^2C Bus Data**. This bus operates under standby voltage and allows the front panel access to the SEL on the I/O carrier.	I/O	$V_{OL} \leq 0.6V$ @ 8.5mA (open-drain) $V_{IL} \leq 0.6V$ @ ± 1.0µA $V_{IH} \geq 1.4V$ @ ± 1.0µA

Table 2-16: SMM Feature Connector (Continued)

INIT_L	**Initialization**. Asserted in response to any one of the following conditions. When the system reset bit in the reset control register is reset to 0 and the reset CPU bit toggles from 0 to 1, PIIX4E initiates a soft reset by asserting INIT. PIIX4E also asserts INIT if a shut down special cycle is decoded on the PCI bus, if the RCIN# signal is asserted, or if a write occurs to port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated.	OD	
INTRUSION_L	**Intrusion**. Indicates disk door has been opened. Driven from SCSI hot-swap backplane.	OUT	$V_{IL} \leq 0.8V$ @ ±1.0µA $V_{IH} \geq 2.0V$ @ ±1.0µA
KB_CLK	**Keyboard Clock**.	I/O	
KB_DATA	**Keyboard Data**.	I/O	
KEYLOCK_FROM_SFC_L	**Keyboard Unlock/lock Indicator**.	IN	$V_{OL} \leq 0.33V$ @ 4mA (open-drain)
MS_CLK	**Mouse Clock**.		
MS_DATA	**Mouse Data**.	I/O	
PWR_CNTRL_SFC_L	**Power Up/Down Indicator** from SMM connector.	IN	$V_{OL} \leq 0.33V$ @ 4mA (open-drain)
RESET_BMC_OC_L	**BMC Reset**. Places into, or monitors, the reset condition of the BMC component.	I/O	
RST_SFC_L	**Reset Request**. SMM connector requests baseboard to reset.	IN	$V_{OL} \leq 0.33V$ @ 4mA (open-drain)
SECURE_MODE_BMC	**Secure Mode**. Host in secure mode.	OUT	$V_{IL} \leq 0.8V$ @ ±1.0µA $V_{IH} \geq 2.0V$ @ ±1.0µA
SMI_L	**Server Management Interrupt**.	I/O	$V_{IL} \leq 0.8V$ @ ± 1.0µA $V_{IH} \geq 2.0V$ @ ± 1.0µA
SMMCPU_NMI	**Non-Maskable Interrupt**.	OUT	$V_{IL} \leq 0.8V$ @ ±11.0µA $V_{IH} \geq 2.0V$ @ ±11.0µA
SMMCPU_NMI_L	**CPU Non-maskable Interrupt**.	I/O	$V_{IL} \leq 0.8V$ @ ±1.0µA $V_{IH} \leq 3.3V$ @ ±1.0µA
VCC_STDBY	**Standby +5 V Power**.	PWR	

Notes:

1. V/I characteristics at device inputs not including load resistors.

2.2.7 Auxiliary I²C* Connectors

These connectors allow external devices to connect to the OPRF100 MP board set's Intelligent Platform Management Bus (IPMB). Two of these connectors are provided on the I/O carrier: one for the server monitor module and another for an auxiliary IPMB.

Table 2-17: Auxiliary I²C Connector*

Name	Description	Type	V/I Characteristics
I2C_BACKUP_SCL	**I²C* Serial Clock**.	I/O	$V_{OL} \leq 0.6V$ @ 8.5mA (open-drain) $V_{IL} \leq 0.6V$ @ ± 1.0µA $V_{IH} \geq 1.4V$ @ ± 1.0µA
I2C_BACKUP_SDA	**I²C Serial Data Line**.	I/O	$V_{OL} \leq 0.6V$ @ 8.5mA (open-drain) $V_{IL} \leq 0.6V$ @ ± 1.0µA $V_{IH} \geq 1.4V$ @ ± 1.0µA
GND	**Electrical Ground** (slave). For an I²C bus master, this is a sense pin, and should be pulled up to VCC with a resistor.	PWR	

2.2.8 Wake-On-LAN* Connector

This three-pin connector allows a network adapter card built to the Wake-On-LAN* specification to "wake up" the system. This connector provides standby power, and a functioning interrupt line.

Table 2-18: Wake On LAN Connector*

Name	Description	Type	V/I Characteristics
MP_WAKEUP	**Wakeup**. This pin wakes up the system. One example implementation is if a "magic packet" was detected by the network interface card (NIC).	I	
VCC_STDBY	**Standby Voltage**. + 5 V.	PWR	
GND	**Electrical Ground** (slave). For an I²C* bus master, this is a sense pin, and should be pulled up to VCC with a resistor.	PWR	

2.3 Functional Architecture

The following figure is the functional block diagram for the I/O carrier. This section provides operational details of each functional block. The I/O carrier block diagram is replicated here for convenience.

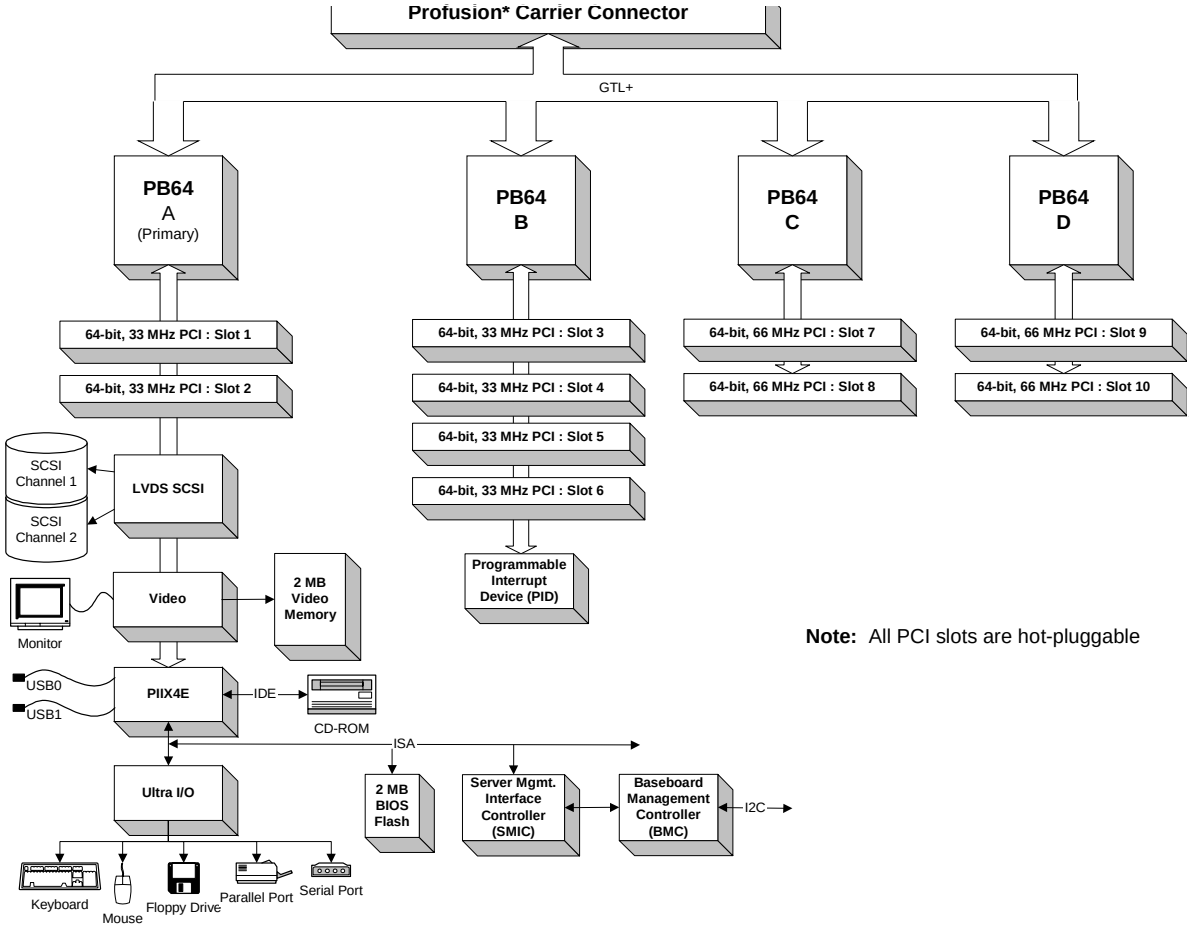


Figure 2-2: Server Management I²C* Private Bus Structure

2.3.1 I/O Connector

The connector supporting the I/O bus in addition to many sideband signals required to pass between the I/O carrier and the other OPRF100 boards is a 1008-pin HDM connector. The mating connector resides on the midplane which then distributes the signals to the remaining boards of the OPRF100 MP board set.

2.3.2 GTL+ I/O Bus Interface

The four PB64 components interface the midplane board with an I/O bus operating at 100 MHz. This I/O bus uses GTL+ technology and follows the same protocol as the Pentium Pro bus (see the *Pentium® Pro Family Developer's Manual, Volume 1: Specifications*, http://developer.intel.com/design/pro/manuals/index.htm). The I/O bus is capable of transfers at a peak data rate of 800 MB/s.

For additional information see the *Pentium® Pro Family Developer's Manual, Volume 1: Specifications*, http://developer.intel.com/design/pro/manuals/index.htm.

2.3.3 PCI Bridge (PB64)

Four PB64 components reside on the I/O carrier. All four PB64 components support 64-bit interfaces in compliance with *PCI Specification, Revision 2.1.* Two PB64 components support 5-V, 33-MHz PCI while the other two components support 3.3-V, 66-MHz PCI. The PCI buses are operated synchronously with the processor bus, using the processor bus clock as a master clock. The input clock received over the I/O bus is divided by three to support the 33-MHz PCI buses and is divided by 1.5 to support the 66-MHz buses.

The first PB64 component controls PCI Bus A and is the primary PCI bridge. The remaining three PB64 components are secondary PCI bridges. The primary PCI bridge is responsible for I/O bus arbitration.

2.3.4 PCI Bus A

PCI Bus A is the primary 64-bit, 33-MHz PCI bus and is configured with the necessary devices to boot the operating system. This bus provides two full length, 64-bit expansion slots (identified as J3B1 and J3B2). A brief overview of the primary components connected to PCI Bus A is provided in the following sections.

2.3.4.1 Symbios* 53C896 SCSI Controller

A single Symbios 53C896 LVDS controller provides embedded SCSI on the primary 64-bit PCI bus. The controller communicates as a 64-bit PCI device for optimum performance. The configuration registers define PCI-related parameters for the 53C896 device. The 53C896 supports all mandatory registers in the PCI configuration space header, including the vendor ID, device ID, class code, revision ID, header type, and command and status fields.

The 53C896 supports two LVDS channels: one is intended for control of internal drives and the other is intended for high speed connection to an external disk array. Refer to the Symbios 53C896 data sheets at http://www.symbios.com for details.

2.3.4.2 Cirrus Logic* GD5446 PCI Video Controller

The Cirrus Logic GD5446 PCI video controller is connected to the primary 64-bit PCI bus and is used to provide onboard VGA capability to the I/O carrier. The CL-GD5446 includes a glueless 32-bit PCI bus interface. This interface features full *PCI Specification, Revision 2.1* compliance,

including optimized PCI burst writes which support PCI writes to the frame buffer at greater than 55 MB/s. The I/O carrier implements 2 MB of EDO video RAM for this controller.

The frame buffer is addressable through a 16-MB window consisting of three 4-MB byte-swapping apertures, and a special video aperture. The VGA control registers are relocatable anywhere in the 64-KB space (allowing multiple devices in a single system).

The GD5446 is automatically disabled by BIOS if a video adapter is detected on any of the PCI AT expansion slots. Complete information for this device can be found in the Cirrus Logic GD5446 data sheet at http://www.cirrus.com.

For configuration purposes, the I/O carrier places a 10 KΩ pull-down resistor on the following pins: MD62 (IRQ Enable), MD58 (Dual CAS), MD57 (Extended RAS for EDO), MD49 (PCI Bus) and MD48 (PCI Bus).

External PCI video adapters must be added to the primary 64-bit PCI bus. When detected, the BIOS automatically disables the onboard GD5446 video controller.

2.3.4.3 Intel® 82371AB PCI to ISA/IDE Accelerator (PIIX4E)

The PIIX4E component provides:

- Bridge for ISA devices.
- Two IDE channels.
- Two USB 1.0 compliant ports.
- Power management logic including full support of the *Advanced Configuration and Power Interface Specification, Revision 1.0,* http://www.teleport.com/~acpi.
- Two fast DMA controllers.
- Real-time clock.
- System Management Bus (SMBus) interface.

Complete information for this device can be found in the *82371AB PCI-TO-ISA/IDE Xcelerator (PIIX4E) Data Sheet.*

The following table lists the current GPIO usage for the PIIX4E.

Table 2-19: PIIX GPIO List

GPI#	Mux Function	Usage	GPO#	Mux Function	Usage
GPI0	IOCHK#	ISA_IOCHK_L	GPO0		FRB_TIMER_HALT_L
GPI1#		PCI_PME_L	GPO1	LA17	LA17
GPI2	REQA#	Reserved	GPO2	LA18	LA18

Table 2-19: PIIX GPIO List (Continued)

GPI3	REQB#	Reserved	GPO3	LA19	LA19
GPI4	REQC#	BOOT_STAT	GPO4	LA20	LA20
GPI5	APICREQ#	APIC_REQ_L	GPO5	LA21	LA21
GPI6	IRQ8#	IRQ8_L	GPO6	LA22	LA22
GPI7	SERIRQ	+3.3V	GPO7	LA23	LA23
GPI8	THRM#	PIIX_THRM_L	GPO8		NOT USED
GPI9	BATLOW#	BATTERY	GPO9	GNTA#	PIIX_SMB_SEL0
GPI10	LID#	PCI_IRQ_L	GPO10	GNTB#	PIIX_SMB_SEL1
GPI11	SMBALERT#	BATTERY	GPO11	GNTC#	NOT USED
GPI12	RI#	WAKEUP_L	GPO12	APICACK#	APIC_ACK0_L
GPI13		+3.3V	GPO13	APICCS#	NOT USED
GPI14		+3.3V	GPO14	IRQ0	IRQ0
GPI15		+3.3V	GPO15	SUSB#	NOT USED
GPI16		SCWB_HIPD	GPO16	SUSC#	PWR_CNTRL_RTC_L
GPI17		SCWB_SE	GPO17	CPU_STP#	NOT USED
GPI18		SCWB_LVD	GPO18	PCI_STP#	NOT USED
GPI19		SCWA_HIPD	GPO19	ZZ	NOT USED
GPI20		SCWA_SE	GPO20	SUS_STAT1#	SUS_STAT1_L
GPI21		SCWA_LVD	GPO21	SUS_STAT2#	NOT USED
			GPO22	XDIR#	SCWA_TERM_EN_L
			GPO23	XOE#	SCWB_TERM_EN_L
			GPO24	RTCCS#	NOT USED
			GPO25	RTCALE	NOT USED
			GPO26	KBCCS#	NOT USED
			GPO27		FLASH_WP_L
			GPO28		FLASH_A20_387
			GPO29	IRQ9OUT#	IRQ9
			GPO30		SPEAKER CONTROL

2.3.4.4 Expansion Slots

Two standard 33-MHz, 64-bit PCI expansion slots are user accessible on the primary PCI bus. These slots compete for access to the bus along with the other components mounted to the bus. Both slots conform to the *PCI Hot Plug Specification Revision 1.0*.

2.3.4.5 IDSEL# Routing

The IDSEL# routing for PCI Bus A is identified in the following table. All attempts were made to minimize BIOS impact by keeping the IDSEL# routing as similar as possible to the A450NX board set.

Table 2-20: IDSEL# Mapping for PCI Bus A

AD Signal	Component/ PCI Slot Number
20	J3B1
21	J3B2
26	Onboard SCSI
28	Video
31	PIIX4E

2.3.5 PCI Bus B

PCI Bus B is also a 64-bit wide bus running at a frequency of 33 MHz. This bus provides four full length, 64-bit expansion slots (identified as J4B1, J5B1, J5B2 and J6B1). A brief overview of the primary components connected to PCI Bus B is provided in the following sections.

2.3.5.1 Programmable Interrupt Device

The I/O carrier incorporates an ASIC referred to as the PID. The PID is an Intel-designed interrupt controller that provides interrupt steering functions including ISA 8259A, and I/O APIC mode controller operations. The PID provides up to 15 ISA IRQs and 49 PCI and miscellaneous interrupt inputs.

The PID contains logic to direct system critical error interrupts to the Server Management Interrupt (SMI) and Non-Maskable Interrupt (NMI) signals to the processors. The following critical interrupts can be routed to SMI:

- PIIX NMIs (these include ISA parity, IOCHK, and port 92h software NMIs).

- PCI SERR and PERR.
- Correctable ECC errors.
- Uncorrectable ECC errors.
- PIIX SMI.

In addition, the PID allows the following to generate an NMI via an SMI-to-NMI mapping option. This allows fatal NMIs to be produced even when the SMI handler is disabled.

- PCI SERR and PERR.
- Uncorrectable ECC errors.
- BMC SMI.

The SMI handler has an option to generate a fatal NMI after it has logged an event, whereupon the OS will typically execute an NMI handler that will display an error status and halt the system. This is an appropriate action to avoid continuing OS operation with a potential unlocated data corruption.

To minimize the possibility of interrupt conflicts, especially with increased use of multi-ported adapter cards, the PID provides four dedicated interrupts per 64-bit PCI slot. The following table summarizes the interrupt mappings.

Table 2-21: PCI and Miscellaneous Interrupt Mappings

PID Interrupt	PCI Interrupt	Component/ PCI Slot Number	PCI Bus
0	D	J9B1	PCI-D
1	C	J9B1	PCI-D
2	B	Onboard SCSI channel B	PCI-A
3	B	J9B1	PCI-D
4	A	J9B1	PCI-D
5	D	J8B2	PCI-D
6	C	J8B2	PCI-D
7	B	J8B2	PCI-D
8	A	J8B2	PCI-D
9	D	J8B1	PCI-C
10	C	J8B1	PCI-C
11	B	J8B1	PCI-C
12	A	J8B1	PCI-C

Table 2-21: PCI and Miscellaneous Interrupt Mappings (Continued)

13	D	J7B1	PCI-C
14	C	J7B1	PCI-C
15	B	J7B1	PCI-C
16	A	J7B1	PCI-C
17	D	J6B1	PCI-B
18	C	J6B1	PCI-B
19	B	J6B1	PCI-B
20	A	J6B1	PCI-B
21	D	J5B2	PCI-B
22	C	J5B2	PCI-B
23	B	J5B2	PCI-B
24	A	J5B2	PCI-B
25	D	J5B1	PCI-B
26	C	J5B1	PCI-B
27	B	J5B1	PCI-B
28	A	J5B1	PCI-B
29	D	J4B1	PCI-B
30	C	J4B1	PCI-B
31	B	J4B1	PCI-B
32	A	Video	PCI-A
33	D	PIIX4E	PCI-A
34	A	J4B1	PCI-B
35	D	J3B2	PCI-A
36	C	J3B2	PCI-A
37	B	J3B2	PCI-A
38	A	J3B2	PCI-A
39	D	J3B1	PCI-A
40	C	J3B1	PCI-A
41	B	J3B1	PCI-A
42	A	Onboard SCSI channel A	PCI-A
43	PCI Hot Plug Interrupt		All

Table 2-21: PCI and Miscellaneous Interrupt Mappings (Continued)

44	SCBERR#	MAC	---
45	A	J3B1	PCI-A
46	NMI	PIIX4E	---
47	Unused	---	---

Table 2-22: ISA & Miscellaneous Interrupt Mappings

PID Interrupt	ISA Interrupt
0	INTR
1	IRQ1
2	IRQ0
3	IRQ3
4	IRQ4
5	IRQ5
6	IRQ6
7	IRQ7
8	IRQ8#
9	IRQ9
10	IRQ10
11	IRQ11
12	IRQ12
13	IRQ13
14	IRQ14
15	IRQ15

2.3.5.2 Expansion Slots

Four standard 33-MHz, 64-bit PCI expansion slots are user accessible on the PCI Bus B. These slots compete for access to the bus with the PID. All four slots conform to the *PCI Hot Plug Specification Revision 1.0*.

2.3.5.3 IDSEL# Routing

The IDSEL# routing for PCI Bus B is identified in the following table.

Table 2-23: IDSEL# Mapping for PCI Bus B

AD Signal	Component/ PCI Slot Number
20	J4B1
21	J5B1
22	J5B2
23	J6B1
25	PID

2.3.6 PCI Bus C

PCI Bus C provides the highest performance available with *PCI Specification, Revision 2.1* compliance. PCI Bus C is 64 bits running at a frequency of 66 MHz interfacing two full length, 64-bit expansion slots (identified as J7B1 and J8B1). Both slots conform to the *PCI Hot Plug Specification Revision 1.0*. A BIOS setup option is available to set the default frequency of these slots and also the slots associated with PCI Bus segment D.

2.3.6.1 IDSEL# Routing

The IDSEL# routing for PCI Bus C is identified in the following table.

Table 2-24: IDSEL# Mapping for PCI Bus C

AD Signal	Component/ PCI Slot Number
20	J7B1

Table 2-24: IDSEL# Mapping for PCI Bus C (Continued)

21	J8B1

2.3.7 PCI Bus D

Similar to PCI Bus C, PCI Bus D also provides the highest performance available with *PCI Specification, Revision 2.1* compliance. PCI Bus D is 64 bits running at a frequency of 66 MHz interfacing two full length, 64-bit expansion slots (identified as J8B2 and J9B1). Both slots conform to the *PCI Hot Plug Specification Revision 1.0*. A BIOS setup option is available to set the default frequency of these slots and also the slots associated with PCI Bus segment C.

2.3.7.1 IDSEL# Routing

The IDSEL# routing for PCI Bus D is identified in Table 2-25:.

Figure 2-3: Table 2-25:

Table 2-25: IDSEL# Mapping for PCI Bus D

AD Signal	Component/ PCI Slot Number
20	J8B2
21	J9B1

2.3.8 ISA Bus

The BIOS device, SMC* Ultra I/O controller and the SMIC are the only devices located on the ISA bus. An ISA connector is not supported.

2.3.8.1 SMC* FDC37C937APM Ultra I/O Controller

The FDC37C937APM* incorporates the following:

- Keyboard interface.
- Real-time clock (RTC).
- SMC's true CMOS 765B floppy disk controller.

- Advanced digital data separator.
- 16-byte data FIFO.
- Two 16C550 compatible UARTs.
- One Multi-Mode* parallel port, which includes ChiProtect* circuitry plus EPP and ECP support.
- On-chip 24 mA AT bus drivers.
- Game port chip select and two floppy direct drive support.
- ACCESS bus.
- Soft power management.
- SMI support.

The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMC advanced digital data separator incorporates SMC's patented data separator technology, allowing for ease of testing and use. Both on-chip UARTs are compatible with the NS16C550*. The parallel port, the IDE interface, and the game port select logic are compatible with IBM PC/AT architecture, as well as with EPP and ECP. The FDC37C937APM incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C937APM provides features for compliance with the ACPI. These features include support of both legacy and ACPI power management models through the selection of SMI or SCI. It implements a 24-bit power management timer, power button override event (four-second button hold to turn off the system) and either edge triggered interrupts.

The I/O address, DMA channel, and IRQ channel on each FDC37C937APM logical device may be programmed through internal configuration registers. There are 480 I/O address location options, 13 IRQ options, and three DMA channel options for each logical device. The FDC37C937APM does not require any external filter components and is, therefore, easy to use and offers lower system cost and reduced board area. The FDC37C937APM is software and register compatible with SMC's proprietary 82077AA core.

For more details about the functions of the FDC37C937APM, refer to the data sheet at http://www.smsc.com.

Table 2-26 lists the current GPIO usage for the SMC* FDC37C937APM Ultra I/O Controller.

Table 2-26: SMC* Super I/O GPIO List

GPI#	Usage
GPIO10	MFG MODE_L
GPIO11	NOT USED

Table 2-26: SMC Super I/O GPIO List (Continued)*

GPIO12	WDO_307_L
GPIO13	RST_BMC_CMD_L
GPIO14	BMC_FRC_UPDATE_L
GPIO15	FW_BOOT_BLOCK_PGM_EN_L
GPIO16	NOT USED
GPIO17	NOT USED
GPIO20	RST_KB_L
GPIO21	PASWD_CLR_L
GPIO22	PHP SWITCH BYPASS
GPIO23	NOT USED
GPIO24	CMOS_CLR_L
GPIO25	A20GATE

2.3.8.2 BIOS Flash Device

The onboard BIOS is located in an onboard 2 MB flash device attached directly to the ISA bus. The device is enabled under the control of the PIIX4E. The device is accessed in byte wide mode. The BIOS can be updated by an update utility at boot time by inserting a bootable floppy into the drive that contains the updated BIOS image and the update utility software. The BIOS contains a recovery boot option, which is enabled by positioning switch 2 to the open position. This switch configuration forces the BIOS to update without user intervention. A series of beeps indicates the beginning and end of the programming process.

2.3.8.3 Server Management Interface Controller (SMIC)

The SMIC is a programmable logic device (Lattice* ispLSI* 2096) which implements a bridge from the ISA bus to the BMC's local bus. The SMIC is described in more detail in Section ISA to BMC Bridge (SMIC).

2.3.9 Wake-On-LAN*

Wake-On-LAN* (WOL) is defined as the ability of a management application to remotely power up a computer which is powered off. For the I/O carrier, WOL is implemented as a three-pin connector designed to be used in conjunction with a network interface card (NIC). A cable will connect the WOL connector with the PCI NIC. The three-pin connector is defined in Section Wake-On-LAN* Connector and consists of standby power, ground, and an interrupt pin (WAKEUP_L). The I/O carrier routes the interrupt to GPI12 of the PIIX4E.

2.3.10 Server Management

The heart of server management is the BMC. External communication can be established with the BMC through the SMIC. The Server Management Logic maintains a SEL to store important system information. System voltage levels are monitored by the server management logic.

Included in the OPRF100 MP board set's server management are hardware hooks to perform in-system programming of the system programmable logic. This capability allows the BMC to program specific programmable logic devices.

The server management logic also provides monitoring and control of other system devices including video, floppy disk, chassis fans, and BIOS flash.

2.3.10.1 Device Maps

The following table shows the address mapping of the various server management devices as seen by the BMC.

Table 2-27: Server Management Device Maps

Function	Address Range	Access Type	Width	Enable Signal
SMIC	0xFF00 – 0xFFFF	See Section .	Byte	smic_decode
Output Latch 2	0xFEC0 – 0xFEFF	Write (Read RAM Shadow).	Byte	Internal to PLD
Output Latch 1	0xFE80 – 0xFEBF	Write (Read RAM Shadow).	Byte	Internal to PLD
Output Latch 0	0xFE40 – 0xFE7F	Write (Read RAM Shadow).	Byte	Internal to PLD
Input Latch 0	0xFE00 – 0xFE3F	Read.	Byte	Internal to PLD
(reserved for future use)	0xFD00 – 0xFCFF	--	--	--
PCI Hot Plug Latch 2	0xFC80 – 0xFCBF	Read.	Byte	Internal to PLD
PCI Hot Plug Latch 1	0xFC40 – 0xFC7F	Read.	Byte	Internal to PLD
PCI Hot Plug Latch 0	0xFC00 – 0xFC3F	Read.	Byte	Internal to PLD
RAM	0xC000 – 0xFBFF	Read, Write, Execute.	15 KB	bmc_ram1_cs_l
FLASH, OPS	0x1000 – 0xBFFF	Read, Write, Execute.	44 KB	bmc_flash_cs_l
FLASH, BOOT	0x0000 – 0x0FFF	Read, Execute.	4 KB	bmc_flash_cs_l

Each of the devices represented in the following table is enabled with the server management decode programmable logic device (PLD). See the Server Management Decode section for more details.

The SMIC is implemented as a Lattice ispLSI 2096 Programmable Array Logic (PAL). Refer to Section ISA to BMC Bridge (SMIC) for SMIC details. All of the latches are implemented in a separate server management decode PAL (ispLSI 2096). Refer to Section Server Management Decode for details on the server management decode PAL.

2.3.10.2 I/O Memory Maps

The following table provides a cross reference between the I/O signals and the individual devices. These can be referenced against the device map section (see the Server Management Device Maps table) to resolve the absolute address.

Table 2-28: Server Management I/O Map

Device	Topic	Signal	Access	Offset	Bit
Micro Port 0	Not Applicable	Not Applicable (BMC Address/Data Bus)	-	-	7:0
Micro Port 1	SPI Bus	SPI_CLK	RW		0
		SPI_MISO			1
		SPI_MOSI			2
	MVRM1 I^2C* Bus	I2C_DS2P1_ SCL			3
		I2C_DS2P1 _SDA			4
	Memory	BMC_OP_CLR_L			5
	Global I^2C Bus	I2C_GLOBAL_SCL			6
		I2C_GLOBAL_SDA			7
Micro Port 2	Not Applicable	Not Applicable (BMC Address Bus 15:12, 10:8)	-		7:0
Micro Port 3	BMC's Private I^2C Bus	I2C_BMC_SCL	-		0
		I2C_BMC_SDA	-		1
	Host processor to BMC Interrupt	INTR0_SMIC_L	R		2
	Secure Mode	SECURE_MODE_KB_L	R		3
	MVRM0 I^2C Bus	I2C_DS2P0 _SCL	-		4
		I2C_DS2P0 _SDA	-		5
	Reserved	BMC_WR_L	-		6
		BMC_RD_L	-		7
Input Latch #0	Interrupts	FP_NMI_SWT_L	R		0

Table 2-28: Server Management I/O Map (Continued)

	Not Used	Not Used			1
					2
	PIIX4E	SUS_STAT1_L			3
	Memory	BMC_FRC_UPDATE_L			4
	Keylock	KEYLOCK_FROM_SFC_L			5
	Bios Flash	FLASH_WP_L			6
	PIIX4E	FRB_TIMER_HALT_L			7
Output Latch #0	Keylock	KEYLOCK_SFC_L	RW		0
	Fans	FAN_FAILED_L			1
	Interrupts	PX4_EXTSMI_L			2
	Secure Mode	SECURE_MODE_BMC			3
	Floppy Drive	FD_READ_ONLY_L			4
	Video	BLANK_VID			5
	Not Used	Not Used			6
	Output Latches	LATCH_2_EN_L			7
Output Latch #1	In Circuit Logic Programming	ISP_SCLK	RW		0
		ISP_MODE			1
		ISP_CPU_EN_L			2
		ISP_IO_EN0_L			3
		Not Used			4
					5
					6
		BMC_RESET_DIS			7
Output Latch #2	SPI Chain Select	SPI_SEL0_L	RW		0
		SPI_SEL1_L			1
		SPI_SEL2_L			2
		SPI_IO_SEL_L			3
		SPI_CPU_SEL_L			4
		Not Used			7:5
PHP Input Latch #0	PCI Hot Plug Monitoring	HP_AMBER[0]	R		0

Table 2-28: Server Management I/O Map (Continued)

		HP_PWR[0]			1
		HP_AMBER[1]			2
		HP_PWR[1]			3
		HP_AMBER[2]			4
		HP_PWR[2]			5
		HP_AMBER[3]			6
		HP_PWR[3]			7
PHP Input Latch #1		HP_AMBER[4]			0
		HP_PWR[4]			1
		HP_AMBER[5]			2
		HP_PWR[5]			3
		HP_AMBER[6]			4
		HP_PWR[6]			5
		HP_AMBER[7]			6
		HP_PWR[7]			7
PHP Input Latch #2		HP_AMBER[8]			0
		HP_PWR[8]			1
		HP_AMBER[9]			2
		HP_PWR[9]			3
		Not Used			7:4
SMIC	ISA to BMC Bridge	ISA_BMC_DATA_REG	-	0xFF01	7:0
		ISA_BMC_CTRL_REG	-	0xFF02	7:0
		ISA_BMC_FLAG_REG	-	0xFF03	7:0
	Reset	PROC_RESET_NOW	R	0xFF04	7
		PROC_RESET_HI_LO	RW		6
		PROC_RESET_LO_HI	RW		5
		PWR_GOOD_LAST_RESET	RW		4
	Memory	BMC_A16_PAGE	RW		3
	Reset	FW_FORCE_RST_LATCH			2
		RESET_HSBP_L	RW		1
	Reset/Interrupt	BMC_SERR_L	RW		0

Table 2-28: Server Management I/O Map (Continued)

	Memory	Not Used	-	0xFF05	7
					6
					5
					4
		FW_BOOT_BLOCK_PGM_EN (from jumper block)	R		3
		FW_BOOT_BLOCK_PGM_EN_L (from processors)			2
	Watchdog	SW_WATCHDOG_EN			1
		WDO_307_L			0
	Not Used	Not Used [REAL_TIME_CLOCK_SYNCH]	RW	0xFF06	7:0

2.3.10.3 BMC Program Memory (Flash)

The I/O carrier contains a 64Kx8 Atmel* 29C512 for storing program memory and initialized variables. Note that while the flash device is 64Kx8, only 44 KB is used with the existing memory map (see the Server Management Device Maps table). Field Replaceable Unit (FRU) information will not be stored in this device, but will be stored in the serial EEPROM. See the FRU Information section for FRU details.

The program flash cannot normally overwrite pages associated with the boot block. The boot block is the lower 4 KB of program space. The FW_BOOT_BLOCK_PGM_EN signal is associated with a Host processor controlled enable of writes to the lower 4 KB block. With this signal asserted, firmware may overwrite pages associated with the entire device including this lower 4 KB. The BMC PAL code monitors the state of FW_BOOT_BLOCK_PGM_EN _L and thereby determines whether the boot block can be reprogrammed.

The 29C512 also supports the “device clear” function. This function should not be used because it effectively overrides the boot block protection by clearing the lower 4 KB of the device.

The BMC_FRC_UPDATE_L signal provides a mechanism for the Host processor to signal the firmware to go into firmware update mode.

2.3.10.3.1 Onboard Flash Programming

To program the flash on board in production, the Automated Test Equipment (ATE) can drive the FLASH_PROGRAM signal using a bed of nails. The SMIC outputs also must be tri-stated in

order to prevent contention on the FLASH_PROGRAM signal. After production, an update utility can be used to update flash code when needed.

2.3.10.4 RAM

BMC program data is supported with a 32Kx8 RAM. It should be noted that while the RAM device is 32 KB, only 15 KB is used with the existing memory map (see the Server Management Device Maps table).

2.3.10.5 System Event Log (SEL) Serial EEPROM

The serial EEPROM is provided on the I/O carrier to provide FRU information, system event logging and other non-volatile storage capabilities. The EEPROM device is an Atmel 24C128. It is a 2.7 V part allowing it to be switched between the 5 V and the 3.3 V power domains. This switching is under the control of the Front Panel Controller (FPC). The FPC controls whether the SEL is connected to either the BMC's private I^2C bus or the FPC's I^2C bus.

When switching the SEL between the 3.3 V and 5 V buses, it is recommended that both the BMC private I^2C bus and the FPC private I^2C bus are tri-stated. Tri-stating the bus avoids potential problems including switching glitches, and entering parts into unknown states.

When the I2C_CEL_CONNECT_FPC signal is asserted, the serial EEPROM is electrically connected to the FPC's private I^2C bus and is powered from the backup +5 V supply. When the I2C_CEL_CONNECT_BMC signal is asserted, the serial EEPROM is electrically connected to the I/O carrier's private I^2C bus and is powered from the +3.3 V supply.

Note:I2C_CEL_CONNECT_FPC and I2C_CEL_CONNECT_BMC **must** be mutually exclusive. Otherwise the 3.3 V and 5 V power planes will be shorted together. The current FPC software ensures this mutual exclusion.

An additional consideration is the BMC on power up. A firmware mechanism is required to tell the BMC when the SEL device is available. It is required that the BMC's I^2C bus be static between 0 and 20 ms after the rising edge of I2C_CEL_CONNECT_BMC.

2.3.10.6 I^2C* Buses

The I/O carrier is the driver and receiver of many I^2C buses for server management purposes. The primary reason for these buses is to allow the various server management controllers (the BMC for the I/O carrier) to communicate to slave devices throughout the system. The I^2C slave devices comprise temperature sensors and EEPROMs, which contain FRU information. See the I/O Carrier section for the I/O carrier FRU components.

2.3.10.6.1 Global I^2C Bus (IPMB)*

The BMC's I^2C pins, SDA and SCL, are connected to the global I^2C bus. The global bus connects the BMC to microcontrollers on the front panel board and the LVDS backplane board. No

slave I^2C devices (devices that do not support multi-master) are connected to this bus. This bus consists of I2C_GLOBAL_SDA and I2C_GLOBAL_SCL.

2.3.10.6.2 Private Management Bus

The following table is a list of all I^2C devices located on the BMC's private bus. Some of these devices reside on the I/O carrier and are described elsewhere in this document. Devices that reside on boards other than the I/O carrier are described further in their respective product specifications. The private I^2C bus is formed by the I2C_BMC_SCL and I2C_BMC_SDA signals. The Server Management I^2C Private Bus Structure diagram shows a listing of the BMC private I^2C buses that communicate through the I/O carrier.

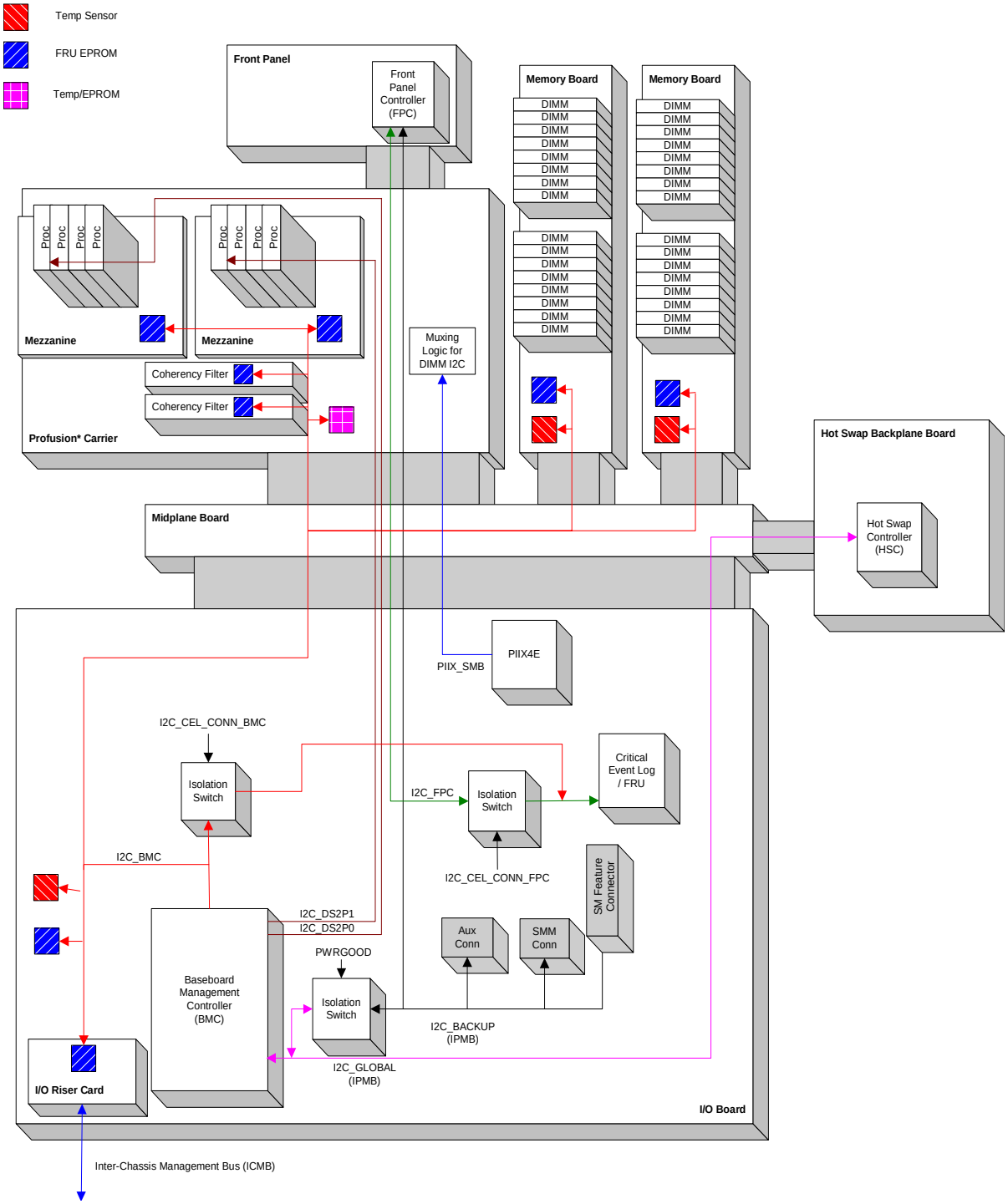


Figure 2-4: Server Management I²C Buses

BMC I2C Private Bus Structure

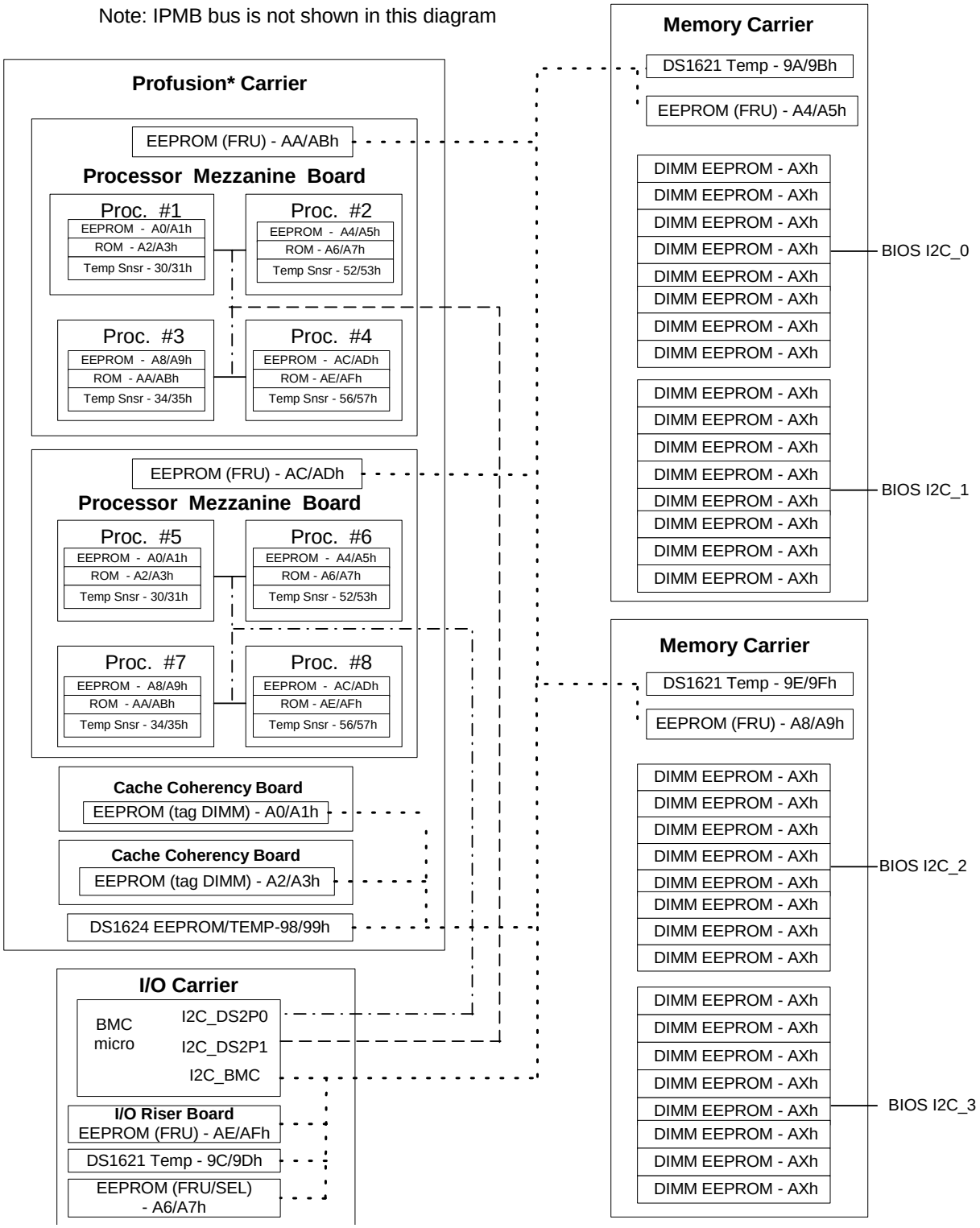


Figure 2-5: Server Management I²C* Private Bus Structure

Table 2-29: BMC's Private Management Bus Devices

Name	Device	Address	Board
Serial EEPROM (FRU/SEL)	AT24C128*	A6/A7h	I/O Carrier
Temp Sensor	DS1621*	9C/9Dh	
Serial EEPROM (FRU)	AT24C02*	AE/AFh	IO Riser Board
Temp Sensor	DS1621	9A/9Bh	Memory Carrier 0
Serial EEPROM (FRU)	AT24C02	A4/A5h	
Temp Sensor	DS1621	9E/9Fh	Memory Carrier 1
Serial EEPROM (FRU)	AT24C02	A8/A9h	
Serial EEPROM (FRU)/Temp Sensor	DS1624*	98/99h	Profusion* Carrier
Serial EEPROM (tag DIMM)	AT24C02	A0/A1h	
Serial EEPROM (tag DIMM)	AT24C02	A2/A3h	
Serial EEPROM (FRU)	AT24C02	AA/ABh	Processor Mezzanine 0
Serial EEPROM (FRU)	AT24C02	AC/ADh	Processor Mezzanine 1

2.3.10.6.3 Processor Mezzanine Board I²C* Buses

The BMC drives two I²C buses, one for each processor mezzanine board. Each I²C bus connects to FRU and temperature sensing devices for each board. The first bus comprises I2C_DS2P0_SDA and I2C_DS2P0_SCL, and the second comprises I2C_DS2P1_SDA and I2C_DS2P1_SCL. See the following tables for the logical address of these signals.

The following tables list the I²C addresses for the devices on each I²C bus.

Table 2-30: BMC Mezzanine Private Bus 0 (I2C_DS2P0) Devices

Name	Device	Address
Temp Sensor (CPU 1)	Pentium® II Xeon™ processor internal	30/31h
Serial EEPROM (CPU 1)		A0/A1h
Serial ROM (CPU 1)		A2/A3h

Table 2-30: BMC Mezzanine Private Bus 0 (I2C_DS2P0) Devices (Continued)

Temp Sensor (CPU 2)		52/53h
Serial EEPROM (CPU 2)		A4/A5h
Serial ROM (CPU 2)		A6/A7h
Temp Sensor (CPU 3)		34/35h
Serial EEPROM (CPU 3)		A8/A9h
Serial ROM (CPU 3)		AA/ABh
Temp Sensor (CPU 4)		56/57h
Serial EEPROM (CPU 4)		AC/ADh
Serial ROM (CPU 4)		AE/AFh

Table 2-31: BMC Mezzanine Private Bus 1 (I2C_DS2P1) Devices

Name	Device	Address
Temp Sensor (CPU 5)	Pentium® II Xeon™ processor internal	30/31h
Serial EEPROM (CPU 5)		A0/A1h
Serial ROM (CPU 5)		A2/A3h
Temp Sensor (CPU 6)		52/53h
Serial EEPROM (CPU 6)		A4/A5h
Serial ROM (CPU 6)		A6/A7h
Temp Sensor (CPU 7)		34/35h
Serial EEPROM (CPU 7)		A8/A9h
Serial ROM (CPU 7)		AA/ABh
Temp Sensor (CPU 8)		56/57h
Serial EEPROM (CPU 8)		AC/ADh
Serial ROM (CPU 8)		AE/AFh

2.3.10.6.4 Front Panel I²C Bus*

The front panel controller drives an I²C bus to the I/O carrier to allow the controller to read the I/O carrier SEL even if power is not applied to the I/O carrier. A multiplexer is implemented on the I/O

carrier that switches between the front panel I^{2}C bus and the private management bus. The front panel I^{2}C bus comprises I2C_FPC_SDA and I2C_FPC_SCL.

2.3.10.6.5 Backup I^{2}C Bus*

A backup I^{2}C bus is implemented on the I/O carrier. This bus operates on standby power which permits the front panel board to access the SEL while power is off. The front panel operates on standby power only. The backup I^{2}C bus comprises I2C_BACKUP_SDA and I2C_BACKUP_SCL.

2.3.10.7 FRU Information

The I/O carrier and A450NX I/O riser board contain the following I^{2}C accessible devices which contain FRU information:

- AT24C128 – I/O carrier FRU information.
- AT24C02 – 256-byte SEEPROM containing A450NX I/O riser board FRU information.

FRU information for both the I/O carrier and A450NX I/O riser board are stored in SEEPROM devices located on each board. The devices are accessed via the BMC. The SEEPROM devices are accessible at the addresses shown in the following table.

Table 2-32: I/O Carrier and A450NX I/O Riser Board I^{2}C* Address Map (FRU Data)

Device	Function	I^{2}C* Address
AT24C128	I/O carrier FRU information.	A6h,A7h
AT24C02	A450NX I/O riser board FRU information.	AEh,Afh

Both the AT24C128 and AT24C02 will provide board FRU information. The FRU information is read by Intel® Server Control (ISC) software or equivalent.

2.3.10.7.1 I/O Carrier

Of the 128 KB SEEPROM located on the I/O carrier, 256 bytes are dedicated to storage of FRU information. The programmable space (256 bytes) is broken into four areas. Table 2-33 shows the areas, a description, and the space allocated to each area.

Table 2-33: SEEPROM Programming Areas (I/O Carrier)

Area	Size	Description
Common Header	8 bytes	Programming offsets to the other areas below.
Internal Use	48 bytes	This area is reserved for general purpose use by Intel®'s server management firmware/controllers.
Board Information	80 bytes	Contains the board FRU information listed in .
Product Information	120 bytes	Programmed as shown below when the I/O carrier is installed into Intel's OCPRF100 chassis. Otherwise this area is not programmed by Intel and is available for OEM use.†

The following table lists the board-specific FRU information that will be programmed into the board information area.

Table 2-34: I/O Board FRU Information

Board Information			
Information	**Description**	**Example**	**Notes**
Mfg. Date/Time	Time and date of board manufacture. (Value programmed (in hex) is teh number of minutes after 0:00 hrs. 1/1/96.)	000f593h (Translated to a date and time. Example: f593h=62867 min, = 43 days and 947 min, = Feb. 12, 1996, 3:47 p.m.)	2
Manufacturer	Board manufacturer.	Intel	1
Board Product Name	Board name/description.	'OPRF100 I/O Carrier'	1
Board Serial Number	Intel® board serial number.	N42385906	2
Board Part Number	Intel board part number.	702647-001	2

Notes:

1. Actual value programmed into the board.
2. Example value. Actual value will vary from board to board and/or from fab to fab.

The table below lists the board-specific FRU information that will be programmed into the product information area. Note that this information is only programmed when the I/O carrier is installed in

to the OCPRF100 MP Server System chassis. This area will be left blank if the I/O carrier is purchased as a board level product.

Table 2-35: Product FRU Information (I/O Carrier)

Product Information			
Information	**Description**	**Example**	**Notes**
Manufacturer Name	System manufacturer name.	Intel	1
Product Name	System name/description.	'OPRF100 Server System'	1
Part Number/Model Number	Intel® system top assembly part number.	702647-001	2
Product Version	Not used. 0 bytes allocated.	---	1
Product Serial Number	Intel system serial number.	N42385906	2
Asset Tag	Not used. 0 bytes allocated.	---	1

Notes:

1. Actual value programmed into the board.
2. Example value. Actual value will vary from board to board and/or from fab to fab.

The table below identified exactly how the FRU information (256 bytes) is allocated within the AT24C128 SEEPROM. This information is useful for those who will be accessing the hardware directly for information (i.e., BIOS developers and server management software developers). Note: For clarity, the information programmed for board level products is shown. The additional information that would be programmed in the product information area for system level products is not provided.

Table 2-36: SEEPROM Content Location (I/O Carrier)

Address	Length	Description	Default Value
0x00	1	Common Header Format Version.	0x01
0x01	1	Internal Use Area Offset (8-byte multiples).	0x01
0x02	1	Chassis Information Area Offset (8-byte multiples).	0x00 (area not present)
0x03	1	Board information Area Offset (8-byte multiples).	0x05
0x04	1	Product Information Area Offset (8-byte multiples).	0x11
0x05	2	Zero Padding.	

Table 2-36: SEEPROM Content Location (I/O Carrier) (Continued)

Address	Length	Description	Default Value
0x07	1	Common Header Checksum.	0xE8
0x08	72	Internal Use Area.	
0x38	1	Board Information Area Format Version.	0x01
0x39	1	Board Information Area Length (8-byte multiples).	0x0A
0x3A	1	Unicode Country Base.	0x00
0x3B	3	Manufacture Date/Time.	
0x3E	1	Board Manufacturer Type/Length Byte.	0xC5
0x3F	5	Board Manufacturer (ASCII).	'Intel'
0x44	1	Product Name Type/Length Byte.	0xDC
0x45	20	Product Name.	'OPRF100 Server System'
0x59	1	Board Serial Number Type/Length Byte.	0xC9
0x5A	9	Board Serial Number.	
0x63	1	Board Part Number Type/Length Byte.	0xCA
0x64	10	Board Part Number.	
0x6E	1	No More Fields Flag.	0xC1
0x6F	24	Zero Padding.	
0x87	1	Board Information Area Checksum.	
0x88	120	Product Information Area.	

2.3.10.7.2 A450NX I/O Riser Board

The A450NX I/O riser board is used for the I/O carrier. The FRU information is contained in an AT24C02 SEEPROM which has 256 bytes of programmable space. The following table shows a list of the four areas, a description, and the space allocated to each area.

Table 2-37: SEEPROM Programming Areas (A450NX I/O Riser Board)

Area	Size	Description
Common Header	8 bytes	Programming offsets to the other areas below.

Table 2-37: SEEPROM Programming Areas (A450NX I/O Riser Board) (Continued)

Internal Use	48 bytes	This area is reserved for general purpose use by Intel®'s server management firmware/controllers.
Board Information	80 bytes	Contains the board FRU information listed in .
Product Information	120 bytes	Available for OEM use.†

Notes:

† Documentation on how to program this area will be available at a later date.

The following table lists the board-specific FRU information that will be programmed into the board information area.

Table 2-38: FRU Information (A450NX I/O Riser Board)

Board Information			
Information	**Description**	**Example**	**Notes**
Mfg. Date/Time	Time and date of board manufacture. (Value programmed (in hex) is the number of minutes after 0:00 hrs. 1/1/96.)	000f593h (Translated to a date and time. Example: f593h = 62867 min, = 43 Days & 947 min, = Feb 12, 1996, 3:47 p.m.)	2
Manufacturer	Board manufacturer.	Intel	1
Board Product Name	Board name/description.	A450NX I/O Riser Board	1
Board Serial Number	Intel® board serial number.	N42385906	2
Board Part Number	Intel board part number.	679267-001	2

Notes:

1. Actual value programmed into the board.
2. Example value. Actual value will vary from board to board and/or from fab to fab.

The following table identifies exactly which bytes are allocated for what within the AT24C02 SEEPROM. This information is useful for those who will be accessing the hardware directly for information (i.e., BIOS developers and server management software developers).

Table 2-39: SEEPROM Content Location (A450NX I/O Riser Board)

Address	Length	Description	Default Value
0x00	1	Common Header Format Version.	0x01
0x01	1	Internal Use Area Offset (8-byte multiples).	0x01
0x02	1	Chassis Information Area Offset (8-byte multiples).	0x00 (area not present)
0x03	1	Board Information Area Offset (8-byte multiples).	0x05
0x04	1	Product Information Area Offset (8-byte multiples).	0x11
0x05	2	Zero Padding.	
0x07	1	Common Header Checksum.	0xE8
0x08	72	Internal Use Area.	
0x38	1	Board Information Area Format Version.	0x01
0x39	1	Board Information Area Length (8-byte multiples).	0x0A
0x3A	1	Unicode Country Base.	0x00
0x3B	3	Manufacture Date/Time.	
0x3E	1	Board Manufacturer Type/Length Byte.	0xC5
0x3F	5	Board Manufacturer (ASCII).	‘Intel’
0x44	1	Product Name Type/Length Byte.	0xDC
0x45	21	Product Name.	‘A450NX I/O Riser Card’
0x5A	1	Board Serial Number Type/Length Byte.	0xC9
0x5B	9	Board Serial Number.	
0x64	1	Board Part Number Type/Length Byte.	0xCA
0x65	10	Board Part Number.	
0x6F	1	No More Fields Flag.	0xC1
0x70	23	Zero Padding.	
0x87	1	Board Information Area Checksum.	
0x88	120	Product Information Area.	

2.3.10.8 Analog Inputs

An A/D converter, part number ADC0819 made by National Semiconductor*, is located on the I/O carrier. This device monitors all voltages on the I/O carrier and provides the measured voltages to the BMC where server management software can monitor them. The V_{REF} inputs to the A/D are connected to +5 V and GND.

To convert conversion counts to input voltage the following formula is used:

$$V_i = 5V \times \frac{A/D_{counts}}{256}$$

Table 2-40: Server Management A/D Converter Values

Voltage	Channel
3.3 V Power Bus	0
+12 V Power Bus	1
+5 V Power Bus	2
Vcc Standby Bus	3
-12 V Power Bus	4
Not Used	5 - 7
3.3 V1 Power Bus	8
SCWA_VREF 1.0 [DA]	9
SCWA_VREF 2.0 [DA]	10
SCWA_VREF 3.0 [DA]	11
SCWB_VREF 1.0	12
SCWB_VREF 2.0	13
SCWB_VREF 3.0	14
Not Used	15 - 18

The following example shows how to calculate the bus voltage from an A/D converter reading.

The A/D converter's channel 4 input, which monitors the -12 V supply, is at 1.9 V. The following formula is used to derive the actual supply voltage:

$$V_m = V_I \times 5.525 - 22.62V$$

$$V_m = 1.9 \times 5.525 - 22.62V$$

$$V_m = -12.6V$$

Therefore the -12 V power bus is at 12.6 V ± measurement error of approximately 1%.

2.3.10.9 Serial Parallel Interface (SPI) Chain Signals

The I/O carrier controls multiple SPI chains with two select signals and three subselects. Only one SPI chain is used on the I/O board so the subselects are currently unused on the I/O carrier. For specifics regarding the Profusion carrier board chains, refer to the *OPRF100 Profusion* Carrier* chapter of this document.

The SPI chain which resides on the I/O carrier is responsible for reading the status of the A/D device explained in Section Analog Inputs. The following table lists all of the signals associated with the SPI chains. All of the SPI chains are controlled through Output Latch #2 (see the Server Management Decode section for details).

Table 2-41: Serial Parallel Interface Bus

Function	Signal
Clock	SPI CLK
Master Out Slave In	SPI_MOSI
Master In Slave Out	SPI_MISO
Enable IO Baseboard SPI Chain	SPI_IO_SEL_L
Enable CPU Baseboard SPI Chains	SPI_CPU_SEL_L
Sub Address Selects	SPI_SEL_0_L
Sub Address Selects	SPI_SEL_1_L
Sub Address Selects	SPI_SEL_2_L

To select the I/O carrier SPI chain, assert the SPI_IO_SEL_L signal. To enable the Profusion carrier SPI chain, assert the SPI_CPU_SEL_L signal. Note that there must be a “dead” period between chain assertions in which both chains are deasserted. All toggling of subaddress selects should occur while the chains are deasserted. The SPI chain on the I/O carrier interfaces the National Semiconductor ADC0819*.

- The BMC drives A/D converter’s address on SPI bus and asserts CS#.
- Six microseconds after the CS# goes active, the MSB of the PREVIOUS conversion becomes valid on MISO.
- At least 400 ns before the CLK line goes high, the MUX address bit must be driven on MISO.
- On the rising CLK edges the address bits driven on the MISO line are latched into the A/D converter.
- A/D results are shifted unto the bus on the CLK falling edge. 250 ns after CLK goes low, the MSB of the PREVIOUS conversion becomes valid on MISO.

- Next A/D conversion begins on the falling CLK edge.
- A/D conversion is complete 64 µsec after the A/D conversion began. If A/D converters CLK is held low, then the MSB data bit appears on MISO.
- Next A/D conversion begins again on last falling CLK edge. In this case the CS# goes inactive between conversions.
- A/D conversion is complete 64 µsec, maximum, after A/D conversion began. CS# should not go active until after the previous A/D conversion is complete.

The Profusion carrier SPI chain and associated signals are described in the *OPRF100 Profusion Carrier* chapter of this document.

2.3.10.9.1 SPI Chain Compatibility

This section describes how to design SPI interface firmware that is compatible with all SPI chains.

The A/D converters and the CPU's serial digital I/O are similar but not identical. All MOSI is clocked into all devices on the rising clock edge. Unfortunately, MISO is not clocked out on the same edge; the A/D converter shifts on the falling clock edge while the CPU's serial digital I/O is clocked on the rising edge. See the following table for SPI chain compatibility.

Table 2-42: SPI Chain Compatibility

	A/D Clock Cycle	Digital I/O Clock Cycle
MOSI clocked in	¦	¦
MISO clocked out	Ø	¦

Although these two serial streams are not identical, they are compatible, and can be driven using the following approach.

- Activate the device(s) by bringing the SELECT low with CLK low.
- Read MOSI. Write MISO.
- Drive Clock High.
- Drive Clock Low.
- Repeat steps 2 through 4 for each byte transferred.
- When finished with all bytes, bring CS high. Keep CLK low.

A note on driving the CS line low: the CS for each SPI bus is derived from a 138 (one of eight decoder) or 139 (one of four decoder). The decoder's address should not be changed while it is active as this could cause glitches on other select lines. Therefore, the address should be changed in the following sequence.

- Disable decoder by bringing SEL# line high.
- Change to new address.
- Enable decoder by bringing the SEL# line low.

2.3.10.10 Server Management Reset

Server management can reset many different components in the system through firmware. The following sections explain how to reset each subsystem.

2.3.10.10.1Resetting the Processors

The processors and chip set are forced to reset via deassertion of the SMIC's IO_PWRGD_CTRL signal. This signal is deasserted by the SMIC whenever any one of the following conditions occur:

- FW_FORCE_RST_LATCH latch is asserted.
- POWER_GOOD signal is deasserted.
- Front panel asserts a reset by asserting the HARD_RESET signal.

Three bits are available within the SMIC to determine the processor reset state. See the following table for the exact logical location of these bits. These bits give the current processor reset state, an indication of the processor entering a reset state, and an indication of the processor leaving the reset state.

The PROC_RESET_NOW bit returns the current state of processor reset (1 is in reset, 0 is not in reset). This bit is **not** latched. In other words, a firmware read of this bit indicates the actual current state of processor reset.

The PROC_RESET_HI_LO bit is asserted when the processors exit the reset state. The bit is deasserted whenever it is read by the BMC. This bit is reset to zero whenever POWER_GOOD is deasserted.

The PROC_RESET_LO_HI bit is asserted when the processors enter the reset state. The bit is deasserted whenever it is read by the BMC. This bit is also reset to zero whenever POWER_GOOD is deasserted.

Multiple bits are required because a processor reset can be as short as approximately 80 ns. Without latching transitions, the firmware would be unable to determine if such a momentary processor reset had occurred.

The PROC_RESET_L signal is inverted and becomes the SYS_RESET_STATE signal. This signal comes from the SMIC and goes to the front panel.

2.3.10.10.2Resetting the System from the BMC

The BMC can force the system into reset by asserting the FW_FORCE_RST_LATCH latch. This is asserted and deasserted per the memory map in Section I/O Memory Maps. This latch is reset whenever POWER_GOOD is deasserted.

2.3.10.10.3Resetting the BMC

The BMC is reset via the RESET_BMC signal from the SMIC. This signal is asserted (high) whenever one of the following two conditions occur:

- POWER_GOOD is deasserted.
- RESET_BMC_CMD_L signal is asserted.

In all other conditions, the RESET_BMC signal is deasserted. See the Server Management Decode section for details about how the RESET_BMC signal can be masked by firmware.

The PWR_GOOD_LAST_RESET bit can be used to determine the source of the last BMC reset. See the following table for the exact logical location of this bit.

Whenever PWR_GOOD signal is deasserted, the PWR_GOOD_LAST_RESET latch is cleared. Whenever the RST_BMC_CMD_L signal is asserted, this latch is set (assuming the PWR_GOOD signal is not deasserted). The state of the latch can be monitored per the memory map. Software can read this signal but cannot write this signal.

2.3.10.11 Video

The video is blanked through assertion of the BLANK_VID signal. This signal is driven by Output Latch 0 in the server management decode PAL (see the Server Management Decode section).

2.3.10.12 Floppy Drive

The floppy drive is put into read-only state by asserting FD_READ_ONLY_L signal. This signal is driven by Output Latch 0 in the server management decode PAL (see the Server Management Decode section).

2.3.10.13 Secure Mode

The SECURE_MODE_BMC signal indicates the secure mode state of the system to the server monitor module and the front panel. This signal is driven by Output Latch 0 in the server management decode PAL (see the Server Management Decode section).

2.3.10.14 Fans

The fan failed LED is illuminated by asserting the FAN_FAILED_L signal. This signal is driven by Output Latch 0 in the server management decode PAL (see the Server Management Decode section). There are no fans to be directly monitored by the BMC. Instead, fan failure state is determined via the Intelligent Platform Management Bus (IPMB).

2.3.10.15 BIOS Flash

The BIOS flash may be write-protected by the SMC chip by asserting the FLASH_WP_L signal. This FLASH_WP_L signal may be monitored by the firmware through Input Latch 0 of the server management decode PAL (see the Server Management Decode section).

2.3.10.16 Keylock

The KEYLOCK_FROM_SFC_L signal is the keylock command output from the server monitor module. This signal is buffered by the BMC. The output signal is KEYLOCK_SFC_L. The BMC firmware should set the KEYLOCK_SFC_L output equal to the KEYLOCK_FROM_SFC_L input signal. This signal is driven by Output Latch 0 in the server management decode PAL (see the Server Management Decode section).

2.3.10.17 Keyboard Secure Mode

The keyboard secure mode state can be determined by reading the SECURE_MODE_KB_L input signal. This signal originates on the Ultra I/O component and is driven to the BMC's port 3 (see the Server Management Decode section).

2.3.10.18 Temperature Sensing

A Dallas Semiconductor* DS1621 digital temperature sensor is located on the I/O carrier. This device can be used to judge the ambient temperature of the I/O carrier. Server management software can read this data and take preventative measures if the temperature is too hot.

2.3.10.19 Real Time Clock Interface

The real time clock (RTC) interface is available to retain synchronization between the real time clock and the server management. Synchronization is required because the RTC and server management have separate clocks which, over time, will drift, one relative to the other.

The synchronization scheme consists of an 8-bit counter clocked by the RTC's clock. This counter can be read directly by the BMC. When the counter is read it is reset to zero. The counter stops counting at FFH. If the BMC reads FFH, that means that an overflow condition has occurred and that synchronization has been lost.

The RTC clock "ticks" 2^{15} times per second which goes through a 3-bit prescaler before it clocks the 8-bit counter. Therefore, the 8-bit counter "ticks" 2^{12} times per second. One least significant bit (LSB) of the 8-bit counter corresponds to roughly 0.244 ms. The current time is calculated based on the initial time plus the elapsed time as follows. Note that the hardware does not provide a mechanism for determining the initial time.

$$\text{CURRENT\_TIME} = \text{INTITIAL\_TIME} + \text{ELAPSED\_TIME}$$

It is best to calculate elapsed time in seconds as there is no round off error using this scheme. It is calculated as follows:

$$\text{ELAPSED\_TIME (seconds)} = \text{COUNTER\_\_LSBS} >> 12$$

In this scheme the BMC must maintain a running accumulation of COUNTER_LSBS. Since the counter is reset each time it is read, the reading must be buffered. The following scheme would work

```
BUFFERED_COUNT = RTC_COUNTER;  // Buffer the counter value
if(BUFFERED_COUNT==0xFF)       // Check for overflow
 error_handler();
COUNTER_LSBS += BUFFERED_COUNT;
```

2.3.11 Programmable Logic Devices

The I/O carrier employs two Lattice ispLSI 2096 programmable logic devices to control various functions for server management. The first PLD is responsible for address decode and latching control bits for the different server management devices. The second PLD operates as the SMIC. Both PLDs provide in-system programming to ease functionality changes required late in the design.

2.3.11.1 Server Management Decode

The server management decode PLD comprises five primary functions:

- Address decode for the BMC I/O space.
- Input latch implementation.
- Output latch implementation.
- PIIX4E SERR# implementation.
- NMI implementation.

The PLD decodes the address for each of the devices in the following table. Since the input and output latches are implemented within the PLD, the latch enables are not observable from outside the PLD.

There are four 8-bit input latches implemented within the PLD: one for various inputs for server management (Input Latch 0) and three for PCI hot plug (PCI Hot Plug Latch 0, 1, and 2). Input Latch 0 allows the BMC to read the status of signals driven by the SMIC, Ultra I/O, and PIIX4E. PCI Hot Plug Latch 0, 1, and 2 read the power and amber LED status of the hot-pluggable PCI slots. These inputs give PCI hot plug error visibility to the server management architecture.

There are three 8-bit output latches implemented within the PLD. The output latch states are mirrored in RAM such that any value written to the latch can also be read back from the exact same address at the RAM. This permits read-modify-write operations. Note that the RAM-mirroring only works if a single address is used for both read and write by firmware.

Output Latch 0 controls many of the functions listed above. Bit 8 of Output Latch 0 enables Output Latch 1. Output Latch 1 controls the in-system programming chains on the I/O carrier (the SMIC) and the Profusion carrier.

Note that when the SMIC is programmed, all of its outputs will tri-state. One of the outputs of the SMIC is the BMC's reset signal (reset_bmc). Therefore, the scenario exists where the BMC attempts to program the SMIC device and gets reset while it is attempting to download the program. Bit 8 of Output Latch 1 disables the reset line to the BMC allowing software to disable this reset condition.

The third output latch controls the SPI chains. Output Latch 2 drives five enables for the different SPI chains.

The server management decode PLD also drives SERR# to the PIIX4E. PCI-A and PCI-B SERR# signals are driven at 33 MHz. PCI-C and PCI-D are driven at 66 MHz. BMC_SERR is driven by the SMIC at 8 MHz. All five SERR# signals need to be ORed together and sent to the PIIX4E at 33 MHz. Similarly, NMI is driven to the I/O carrier connector. The PLD ORs each of the NMI sources together (CPU_NMI, SMM_NMI, and FP_NMI) before driving it to the connector.

2.3.11.2 ISA to BMC Bridge (SMIC)

The ISA to BMC bridge, also known as the SMIC, allows system software, often referred to as "ISA side software," to communicate with the server management firmware. The three registers associated with this functionality are listed in the following table.

Table 2-43: SMIC Register Map

ISA I/O Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	BMC xdata Address
0x0CA9	Data register									0xFF01
0x0CAA	Ctrl/Sts register									0xFF02
0x0CAB	Flags register	RX Data Ready	TX Data Ready	0	SMI	SMS	SMS Avail	0	Busy	0xFF00, 0xFF03, 0xFF07

The three SMIC registers (Data, Ctrl/Sts, Flags) are readable by both ISA and BMC at any time. Bits 1 and 5 of the Flags register will always be zero. The state of the Busy bit in the Flags register determines which side (ISA or BMC) can write to the Ctrl/Sts and Flags registers.

When the Busy bit is a 0 (default power-on state):

- An ISA agent (namely the PIIX4E) can write to the Data register.
- An ISA agent can write to the Ctrl/Sts register.
- An ISA agent can write to the Busy bit in the Flags register.
- An ISA agent cannot write to any other bits in the Flags register.
- An ISA agent can read from any of the three registers.
- The BMC cannot write to any of these three registers.
- The BMC can read from any register.

When the Busy bit is a 1 (a state only possible writing from the ISA side):

- The BMC's INTR0_SMIC_L interrupt input is asserted (low).
- The BMC can write to the Data register.
- The BMC can write to the Ctrl/Sts register.
- The BMC can write to the Flags register (bit 5 and 1 will always remain zero).
- BMC can read from any register.
- An ISA agent (namely the PIIX4E) can read from any of the three registers.

Proper usage of the registers is described in the *Saber Server Management External Product Specification.*

The SMIC is reset by deasserting POWER_GOOD or asserting the RST_DRV_L signal. The RST_DRV_L signal is an output from the Ultra I/O chip.

The following table describes the SMIC signals. 3S output means the pin can be tri-stated. OC means the pin is an open-collector output. BIDI means the pin is bi-directional (input and output).

Table 2-44: SMIC Signal Description

Signal Name	Pin Number	Type	Description
ISP_IO_EN_L	18	INPUT	I/O carrier In-system programming (ISP) chain enable signal. A low on this signal puts the SMIC in programming mode, tri-states all I/O pins, and changes ISP_SDO from a high impedance state to a driven state. It is used when the SMIC and all other devices in the system (except the BMC's address decoder) are reprogrammed. It is driven either by the BMC or the ISP connector.
ISP_SPARE_SDO	20	INPUT	ISP chain serial data input. This signal carries the serial data used to program the SMIC.
ISP_MODE	46	INPUT	ISP chain mode input. This signal is also used to set the programming state for the SMIC and all other ISP programmable devices in the system (except the BMC's address decoder). It is driven either by the BMC or the ISP connector.
ISP_SCLK	78	INPUT	ISP chain serial clock. This signal is used to clock the serial programming data into and out of all the ISP devices in the system (except the BMC's address decoder). It is driven either by the BMC or the ISP connector.

Table 2-44: SMIC Signal Description (Continued)

ISP_SDO	50	3S, OUT-PUT	ISP chain serial data output. This signal carries the serial programming data out of the SMIC. It is shared with other ISP outputs in the system (except the BMC's address decoder) and returns to both the BMC and the ISP connector. It is in a high impedance state when none of the chains are being programmed.
SD(0)	21	3S, BIDI	ISA bus data bit 0.
SD(1)	22	3S, BIDI	ISA bus data bit 1.
SD(2)	23	3S, BIDI	ISA bus data bit 2.
SD(3)	24	3S, BIDI	ISA bus data bit 3.
SD(4)	25	3S, BIDI	ISA bus data bit 4.
SD(5)	26	3S, BIDI	ISA bus data bit 5.
SD(6)	27	3S, BIDI	ISA bus data bit 6.
SD(7)	28	3S, BIDI	ISA bus data bit 7.
SA(0)	29	INPUT	ISA bus address bit 0.
SA(1)	30	INPUT	ISA bus address bit 1.
SA(2)	31	INPUT	ISA bus address bit 2.
ISA_IOR_L	32	INPUT	ISA bus I/O read.
ISA_IOW_L	34	INPUT	ISA bus I/O write.
ISA_BALE	35	INPUT	ISA bus buffered address latch enable.
ISA_AEN	36	INPUT	ISA bus address enable.
IN_CIRCUIT_FLASH_PGM_EN_L	37	INPUT	Not used.
RST_DRV_L	38	INPUT	This signal is driven by the PIIX4E to devices on the ISA bus. The SMIC resets its registers when this signal is asserted.
RESET_SW_JMP	39	INPUT	Not used.
RESET_FW_JMP	40	INPUT	Not used.
RESET_BMC_OC_L	41	OC output	Not used.
RESET_FPC_JMP	42	INPUT	Not used.
RESET_HSBP_JMP	43	INPUT	Not used.
RESET_SPARE1_JMP	45	INPUT	Not used.
RESET_SPARE2_JMP	52	INPUT	Not used.
FW_WATCHDOG_EN	54	INPUT	Not used.

Table 2-44: SMIC Signal Description (Continued)

SW_WATCHDOG_EN	55	INPUT	GPIO bit from the SMC used by firmware to determine whether to take action when a software watchdog time-out occurs.
HARD_RESET	57	INPUT	A 1 on this pin will cause the SMIC to hold the system in reset.
FP_NMI_SWT_L	59	INPUT	Not used.
BOOT_BLOCK_PGM_EN_JMP	60	INPUT	Firmware boot block program enable jumper.
BOOT_BLOCK_PGM_EN_L	61	INPUT	Firmware boot block program enable (L). This signal comes from a SMC GPIO pin and is used by the BMC's address decoder to protect flash from being reprogrammed accidentally.
32KHZ_RTC_CLK	62	INPUT	Clock input from real-time clock.
RST_SFC_L	69	INPUT	Not used.
PWR_CNTRL_SFC_L	70	INPUT	Not used.
RST_BMC_CMD_L	72	INPUT	An SMC output signal that resets the BMC.
SMIC_CSB_L	73	INPUT	This signal is used as an ISA chip-select from the SMC. Either it or PLD_CS1 can be used to select the SMIC from the ISA side. Note that after this signal is active the SMIC only looks at ISA address bits 0-2 to determine which register is being accessed.
WD0_307_L	76	INPUT	This is the watchdog output signal from the SMC.
SECURE_MODE_BMC	77	INPUT	Not used.
PWR_GOOD	19, 58	INPUT	This signal is a 1 when the power to the system is stable and valid. When this signal is 0, all the registers in the SMIC return 0 and the system, including the BMC, is held in reset through the IO_PWRGD_CTRL and RESET_BMC_OC_L signals, respectively. All the registers that are latched (i.e., writeable) will remain 0 even after PWR_GOOD returns to a 1, but the registers which simply return the state of the SMIC's input pins will return those states properly when PWR_GOOD returns to a 1.
CLK_ISASYS	15, 83	INPUT	Not used.
OSCILLATOR	67, 80	INPUT	Not used.
BMC_D(0)	85	3S, BIDI	BMC microcontroller data bus bit 0.
BMC_D(1)	86	3S, BIDI	BMC microcontroller data bus bit 1.
BMC_D(2)	87	3S, BIDI	BMC microcontroller data bus bit 2.
BMC_D(3)	88	3S, BIDI	BMC microcontroller data bus bit 3.
BMC_D(4)	89	3S, BIDI	BMC microcontroller data bus bit 4.

Table 2-44: SMIC Signal Description (Continued)

BMC_D(5)	90	3S, BIDI	BMC microcontroller data bus bit 5.
BMC_D(6)	91	3S, BIDI	BMC microcontroller data bus bit 6.
BMC_D(7)	92	3S, BIDI	BMC microcontroller data bus bit 7.
BMC_A(0)	93	INPUT	BMC microcontroller address bus bit 0.
BMC_A(1)	94	INPUT	BMC microcontroller address bus bit 1.
BMC_A(2)	95	INPUT	BMC microcontroller address bus bit 2.
BMC_A(3)	96	INPUT	BMC microcontroller address bus bit 3.
BMC_A(4)	98	INPUT	BMC microcontroller address bus bit 4.
BMC_A(5)	99	INPUT	BMC microcontroller address bus bit 5.
BMC_A(6)	100	INPUT	BMC microcontroller address bus bit 6.
BMC_A(7)	101	INPUT	BMC microcontroller address bus bit 7.
BMC_A(8)	102	INPUT	BMC microcontroller address bus bit 8.
BMC_A(9)	103	INPUT	BMC microcontroller address bus bit 9.
BMC_A(10)	104	INPUT	BMC microcontroller address bus bit 10.
BMC_A(11)	105	INPUT	BMC microcontroller address bus bit 11.
BMC_A(12)	106	INPUT	BMC microcontroller address bus bit 12.
BMC_A(13)	107	INPUT	BMC microcontroller address bus bit 13.
BMC_A(14)	108	INPUT	BMC microcontroller address bus bit 14.
BMC_A(15)	109	INPUT	BMC microcontroller address bus bit 15.
BMC_A(16)	117	INPUT	BMC microcontroller flash address page bit.
BMC_RD_L	118	INPUT	BMC microcontroller data read line. It is activated when the BMC performs a read from its XDATA address space.
BMC_WR_L	119	INPUT	BMC microcontroller data write line. It is activated when the BMC performs a write to its XDATA address space.
BMC_PSEN_L	120	INPUT	BMC microcontroller code read line. It is activated when the BMC performs an instruction fetch (from its CODE address space).
SMIC_DECODE	121	INPUT	Reserved.
PROC_RESET_L	128	INPUT	A 1 on this signal indicates the system processor(s) is in a reset state. A 0 indicates the system processor(s) is not in a reset state.

Table 2-44: SMIC Signal Description (Continued)

RESET_HSBP_L	2	OUTPUT	The SMIC drives this line low to reset the hot swap backplane or other mass storage array, if such mass storage array supports an external reset. The state of this bit can be written-to and read-from.
RESET_PWR_DIST_L	3	OUTPUT	The SMIC drives this line low to reset the power distribution system, if such power distribution system supports an external reset.
SYS_RESET_STATE	5	OUTPUT	This signal is the inverse of PROC_RESET_L.
BMC_SERR_L	6	OUTPUT	The SMIC drives this line low to signal an internal BMC “soft error.”
CPU_SPI_RESET_L	7	OUTPUT	This signal oscillates with 32KHZ_RTC_CLK when either PWR_GOOD is low or HARD_RESET is high. It is used to reset the SPI bus.
INTR0_SMIC_L	8	OUTPUT	This signal is the inverse of the Busy bit in the Flags register. It causes an interrupt of the BMC microcontroller. Its electrical state is the inverse of the bit for firmware backward compatibility.
FLASH_PROGRAM	9	OUTPUT	Not used by the SMIC.
BMC_TO_FPC_RST_CMD	11	OUTPUT	Not used.
IO_PWRGD_CTRL	12	OUTPUT	The SMIC writes a 0 to this signal to hold the system in reset. A 1 on this signal does not guarantee that the system is not being held in reset by another signal elsewhere.
PLD_CS1_L	13, 114	INPUT	A 0 on this signal indicates the PIIX4E is selecting the SMIC from the ISA side based on the ISA bus’ I/O address, i.e., this signal goes low (active) when any of the ISA addresses in the table above is present on the ISA bus. At present there are only three of these addresses.

2.3.11.3 Remote PLD Logic Download

The OPRF100 MP board set server management provides the hardware hooks required to perform in-system programming of programmable logic in the field. It is required that the signals associated with ISP get put into their default states as soon as possible after power up.

Before enabling Output Latch 1, bit 8 of Output Latch 0 must be written to a 1. Doing this places all associated signals in their proper states.

All ISP signals are tri-stated (pulled up actually) with the BMC_OP_CLR_L signal driven high. This signal is driven through port 1 of the BMC.

There are two ISP chains supported on the OPRF100 MP board set. The first chain consists of a Lattice ispLSI 2096 device representing the server management decode PLD. The second chain is also a Lattice ispLSI 2096 device representing the SMIC. The two devices **must** reside on separate chains. The server management decode PLD must be functional while the SMIC is programmed. The server management decode PLD contains logic that prevents the BMC from resetting while programming the SMIC.

Table 2-45: ISP Chain Signal List

Signal Name	Function
ISP_MODE	In-system Program Mode Bit. This signal is common to all chains.
ISP_CLK	In-system Program Clock. This signal is driven by a dedicated pin from the BMC. This pin is High Z when the BMC is in reset. During normal operation (when not in programming mode) this signal will not toggle.
ISP_SDI	In-system Program Serial Data In. This signal is an output from the BMC and is a common input to the first device in each of the four programming chains. It is tied through a zero ohm resistor to the BMC's SPI_MISO and therefore may toggle during normal operation of the BMC.
ISP_SDO	In-system Programming Serial Data Out. This signal is a common output from the CPU and I/O boards programming chains and also the SPI_MOSI pin through a zero ohm resistor. These ISP chains do not drive this signal during normal operation because their ISP_EN_L inputs are not asserted. This signal may be toggled by other devices from the SPI bus during normal (non programming) operations. The HSBP and FP ISP serial data out pins were not connected to this signal because they do not become High Z when not selected.
ISP_CPU_EN_L	In-system Programming Enable Number Two. This signal selects the CPU's ISP chain.
ISP_IO_EN0_L	In-system Programming Enable Number Two. This signal selects the I/O carrier's ISP chain.

2.3.11.3.1 Using Onboard Programming Connectors

Each OPRF100 board has an ISP connector to allow programming all of the PLDs. The I/O carrier has such a connector and allows programming of the two onboard Lattice PLDs. The two devices are connected together in a serial chain: first the BMC PAL followed by the SMIC.

An additional feature was added to allow the BMC to program the PLDs. Therefore, a software program could be shipped to customers that would allow them to update the PLD devices easily with minimal impact. Therefore, a second ISP chain originates from the BMC and connects to the SMIC and the other Lattice devices on the other boards.

The BMC PAL is not permitted to be programmed by the BMC. This PAL drives BMC critical signals that must be reliable during programming (BMC_RESET for example). When a PAL is programmed, it's signal pins are tri-stated. The BMC's reset cannot tri-state while the BMC is attempting to program a device.

The BMC's ISP signals should only be activated when a PLD download is being performed. The firmware should disable the chains by driving Output Latch 1 (see the I/O Memory Maps). Note that the ISP chains may also be disabled by driving BMC_OP_CLR_L high (Output Latch 0).

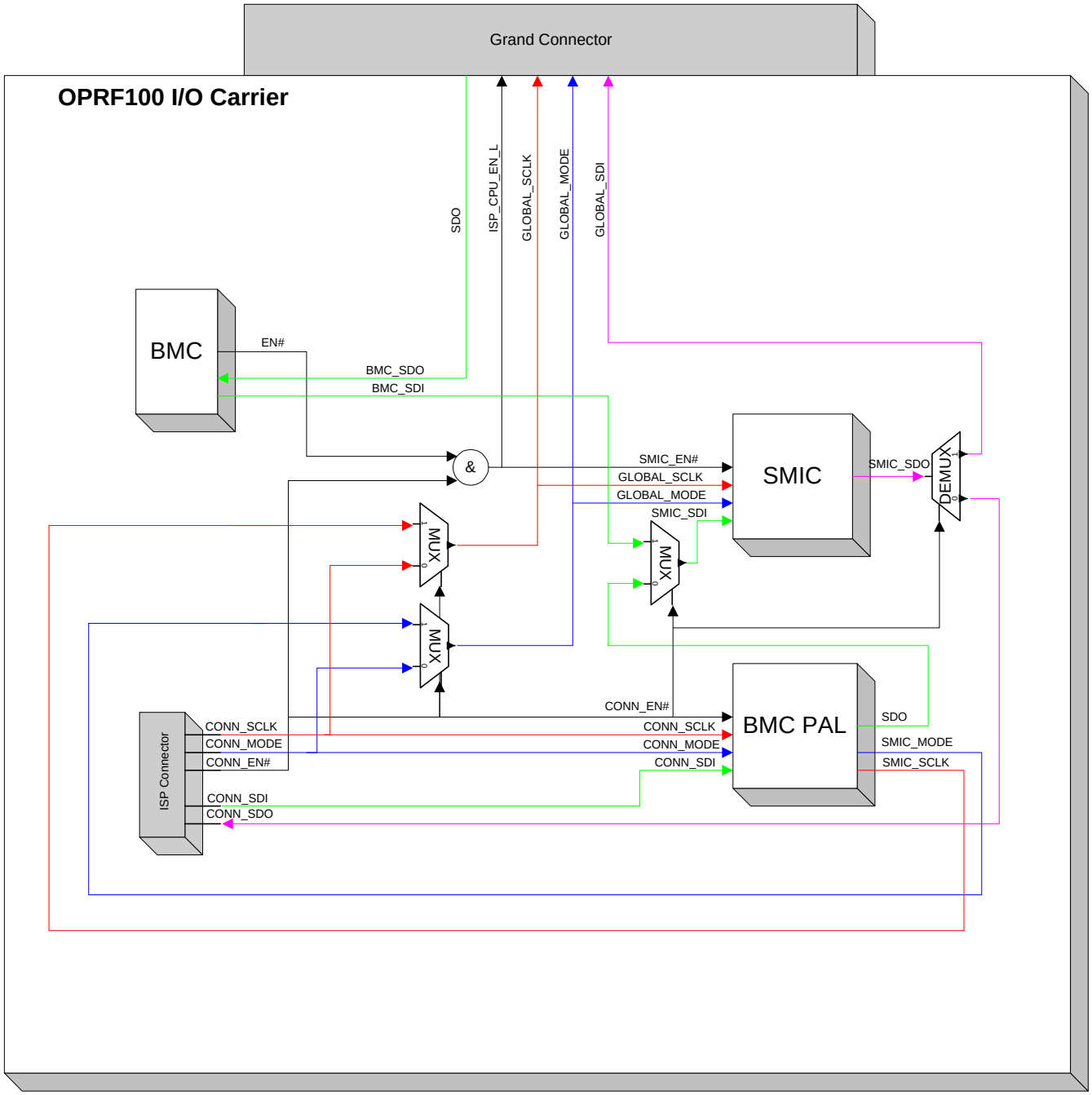


Figure 2-6: In-system-Programming of Onboard PLDs

2.3.11.3.2 Processor NMI Interrupt

The FP_NMI_SWT_L signal is an input from the NMI switch on the front panel. This signal is read through Input Latch 0. This signal is debounced by the BMC. During both transitions the switch will normally bounce. The following table defines the worst case switch characteristics.

Table 2-46: Worst Case Switch Characteristics

Switching Case	Min (Milliseconds)	Typical	Max
Switch Press Ramp (High-Low).	0	20	200
Switch Release Ramp (Low-High).	0	12	150
Required switch cycle duration detection by firmware.	50	20	n/a
Potential Switch Cycle characteristics (press to release). [No firmware requirements derived from this row.]	0	200	n/a

After being debounced, the BMC can pass on this NMI to the system by asserting the BMC_FP_NMI_L signal. This signal is initialized by hardware to its deasserted state only when PWR_GOOD is deasserted.

2.3.11.3.3 Server Management Interrupts

An SMI interrupt is signaled by asserting the PX4_EXTSMI_L signal through Output Latch 0. This signal requires proper initialization to a 1.

The firmware can produce a soft error interrupt to the server management software by asserting the BMC_SERR_L signal. This signal is initialized by hardware to its deasserted state only when PWR_GOOD is deasserted.

The processors can interrupt the BMC via the INTR0_SMIC_L signal. This signal is initialized by hardware to its deasserted state only when PWR_GOOD is deasserted. This signal is the inverse of the Busy bit in the Flags register of the SMIC and causes an interrupt of the BMC microcontroller. An ISA agent (PIIX4E) can only set this bit, and the BMC can only clear this bit.

2.3.12 Boundary Scan

Boundary scan is accessible through the In Target Probe (ITP) when the I/O carrier is in a system environment. The Scan Header connector is located on the Profusion carrier board. This port is used primarily to test the connectivity of the various board components.

2.3.13 Board Configuration Switches

Configuration switches exist on the I/O carrier to enable the user to recover a BIOS, clear a CMOS password, or clear all CMOS settings. Switches labeled ‘reserved’ should not be changed from their shipping configurations.

Table 2-47: GPIO Assignments

Function	Device:GPIO#
Normal/Recovery Boot	PIIX:GPI04
CMOS ClearCMOS Clear	SuperIO:GP24
Password ClearPassword Clear	SuperIO:GP21
PHP Switch OverridePHP Switch override	SuperIO:GP22

Table 2-48: GPIO Assignments

Switch	Function
1(Open)	Reserved†
1(Closed)	
2(Open)	Normal boot.†
2(Closed)	Recovery boot.
3(Open)	Reserved†
3(Closed)	
4(Open)	Reserved†
4(Closed)	
5(Open)	Do not clear CMOS†
5(Closed)	Clear CMOS.
6(Open)	Do not clear password†
6(Closed)	Clear password.
7(Open)	PCI Hot-plug Mechanical Switches Enabled†
7(Closed)	PCI Hot-plug Mechanical Switches Disabled.
8(Open)	Reserved†
8(Closed)	

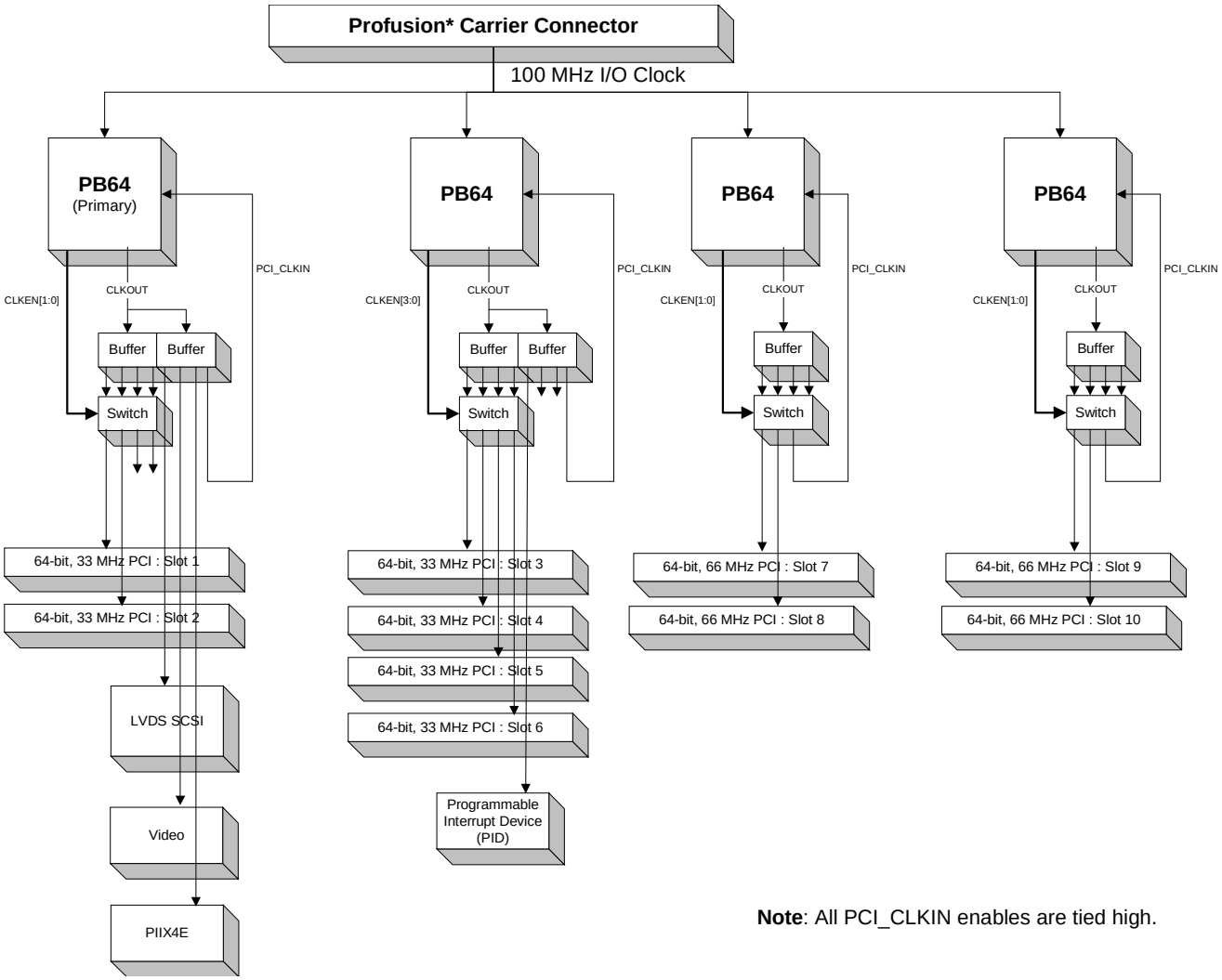
Notes:

† Indicates the default jumper position.

2.3.14 Clock Distribution

Clocks on the I/O carrier are derived from two sources: a derivative of the host clock passed on the I/O bus and onboard oscillators. Clocks are unitary loaded and length matched for minimum skew. PCI slot clocks are 2.5 inches shorter than onboard clocks to allow for the loading and trace length induced by add-in cards.

All of the PCI connector clocks pass through a switch in order to provide PCI hot-plug capability.



Note: All PCI_CLKIN enables are tied high.

Figure 2-7: I/O Carrier Clocking Architecture

2.3.15 Reset Sequence

Refer to Reset Diagram for the sequence of events during reset.

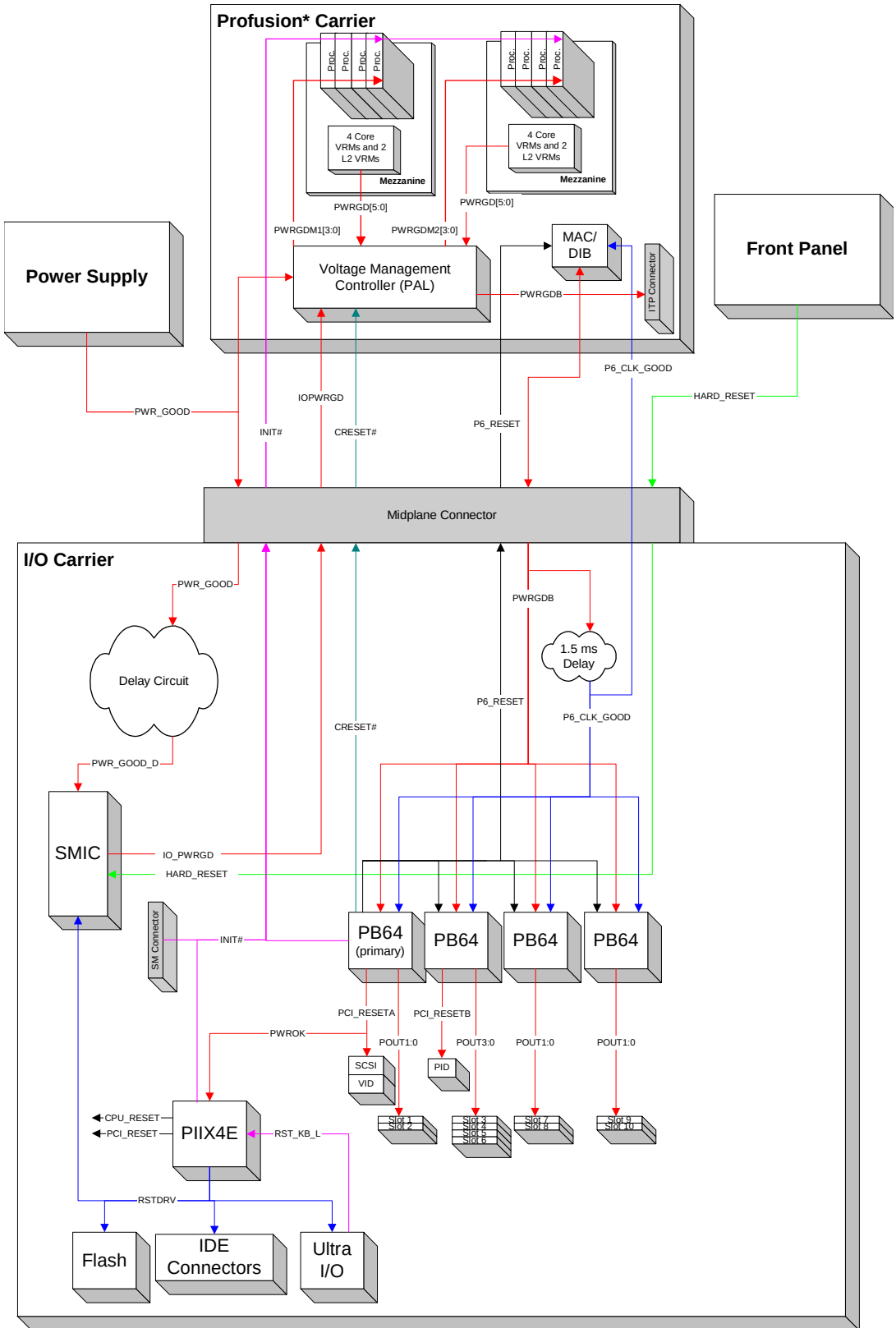


Figure 2-8: Reset Diagram

The following sequence of events occurs when power is applied to the I/O carrier:

The 5 V standby power is assumed active which applies power to the signal PS_PWR_ON. This signal is not shown in Reset Diagram. Agents that drive this signal (front panel and midplane) may hold this signal false to prohibit the main supplies from applying power to the board. When the signal PS_PWR_ON transitions true, it is an indicator to activate the power supplies and apply full power to the system.

When the power supplies are within their specified limits, the signal PWR_GOOD is asserted from a source external to the I/O carrier. The I/O carrier delays PWR_GOOD for insurance resulting in PWR_GOOD_D. The SMIC monitors the status of PWR_GOOD_D, RSTDRV and HARD_RESET which is driven by the front panel controller. When HARD_RESET is deasserted, and PWR_GOOD remains asserted, the SMIC asserts IO_PWRGD.

The signal IO_PWRGD is an output from the I/O carrier to the Profusion carrier. IO_PWRGOOD indicates that the I/O carrier can complete reset sequencing. In response to the assertion of IO_PWRGD, the Profusion carrier will assert PWRGDB. Until PWRGDB is asserted, the I/O carrier PB64 components remain in a reset state. When PWRGDB is asserted, each PB64 releases its corresponding PCI reset signals.

While in reset, each PB64 holds its corresponding PCI bus in reset. When the primary PCI bus is held in reset, it removes the power good indicator to the PIIX4E component. This condition causes the PIIX4E to issue RSTDRV to the ISA bus. RSTDRV is released after PCI reset is released.

To ensure that all I/O devices are ready to accept the first code fetch, the PIIX4E PCI reset output is used to hold the I/O bus BNR# signal asserted. This ensures that the PIIX4E is ready to process the first address decoded located in the flash located on the ISA bus.

2.3.16 Boot Order

The I/O carrier provides the system a variety of methods of detecting and booting an operating system. The BIOS scans devices and user configurable option slots in a specific sequence. The default boot order is listed in the following table, although there are many factors, including user changes to the BIOS setup, which may affect the actual boot order of a particular configuration.

Table 2-49: Boot Order

I/O Device	Bus
Floppy	--
Primary IDE	
P1	PCI-A
P2	
Onboard SCSI	
P3	PCI-B

Table 2-49: Boot Order (Continued)

P4	
P5	
P6	
P7	PCI-C
P8	
P9	PCI-D
P10	

The IDSEL assignments are shown in the following tables to help determine the actual boot order.

2.4 Mechanical Specifications

The following diagrams show the mechanical specifications for the I/O carrier and the A450NX I/O riser board. All dimensions are given in inches. Connectors are dimensioned to pin 1.

Table 2-50: A450NX I/O Riser Board Connector Definitions

Description	Connector Type	Intel® Part	Quantity	Location
Multifunction mouse connector/ keyboard connector.	FOXCONN/Hon Hai* MH11063-D0	201377-001	1	J4
Multifunction dual serial port connector.	FOXCONN/Hon Hai DM10156-73	201004-013	1	J5
Multifunction located nearest the connectors. VGA connector/interface with each serial port. Parallel port connection.	AMP* 750433-2	201325-001	1	J6
ICMB cable interface connector.	AMP 111988-1	661966-001	1	J1

2.4.1 I/O Bus Connector

Table 2-51: I/O Bus Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A5	NO CONNECT	B1	+12V	C5	PB64_D_CLK	D1	+5V	E5	GROUND	F1	+12V
A6	NO CONNECT	B2	+12V	C6	GROUND	D2	+5V	E6	GROUND	F2	+12V
A7	NO CONNECT	B3	+12V	C7	PB64_C_CLK	D3	+5V	E7	GROUND	F3	+12V
A8	NO CONNECT	B4	+12V	C8	GROUND	D4	+5V	E8	GROUND	F4	+12V
A9	NO CONNECT	B5	GROUND	C9	PB64_B_CLK	D5	GROUND	E9	GROUND	F5	NO CONNECT
A10	NO CONNECT	B6	GROUND	C10	GROUND	D6	NO CONNECT	E10	GROUND	F6	GROUND
A11	NO CONNECT	B7	GROUND	C11	PB64_A_CLK	D7	GROUND	E11	GROUND	F7	P64_D_TCLK
A12	NO CONNECT	B8	GROUND	C12	GROUND	D8	P64_C_TCLK	E12	GROUND	F8	GROUND
A13	PC_CLKGOOD	B9	GROUND	C13	-12V	D9	GROUND	E13	GROUND	F9	PID_TCLK
A14	-12V	B10	GROUND	C14	-12V	D10	P64_B_TCLK	E14	GROUND	F10	GROUND
A15	-12V	B11	GROUND	C15	NO CONNECT	D11	GROUND	E15	GROUND	F11	NO CONNECT
A16	RESERVED	B12	GROUND	C16	NO CONNECT	D12	P64_A_TCLK	E16	GROUND	F12	PG4_D_GTL_VREF
A69	NO CONNECT	B13	GROUND	C69	NO CONNECT	D13	PG4_D_GTL_VREF	E69	GROUND	F13	PG4_D_GTL_VREF
A70	NO CONNECT	B14	GROUND	C70	NO CONNECT	D14	PG4_D_GTL_VREF	E70	GROUND	F14	RESERVED
A71	NO CONNECT	B15	GROUND	C71	IO_RESET_L	D15	RESERVED	E71	GROUND	F15	RESERVED
A72	NO CONNECT	B16	GROUND	C72	IO_BERR_L	D16	RESERVED	E72	GROUND	F16	RESERVED
A73	NO CONNECT	B17	+12V	C73	IO_RS1_L	D17	+5V	E73	GROUND	F17	+3.3V
A74	NO CONNECT	B18	+12V	C74	IO_REQ3_L	D18	+5V	E74	GROUND	F18	+3.3V
A75	IO_RS0_L	B19	+12V	C75	IO_REQ0_L	D19	+5V	E75	GROUND	F19	+3.3V
A76	IO_REQ2_L	B20	+12V	C76	IO_BPRI_L	D20	+5V	E76	GROUND	F20	+3.3V

Table 2-51: I/O Bus Connector Pinout (Continued)

A77	IO_HIT_L	B69	GROUND	C77	IO_DEFER_L	D69	PWR_GOOD	E77	GROUND	F69	IO_PWRGD
A78	IO_AP1_L	B70	GROUND	C78	IO_ADS_L	D70	PWRGDB	E78	GROUND	F70	NO CONNECT
A79	IO_A(35)	B71	GROUND	C79	IO_A(29)	D71	IO_BINIT_L	E79	GROUND	F71	IO_RSP_L
A80	IO_AP0_L	B72	GROUND	C80	IO_A(24)	D72	IO_TRDY_L	E80	GROUND	F72	IO_RS2_L
A81	IO_A(20)	B73	GROUND	C81	IO_A(17)	D73	IO_DRDY_L	E81	GROUND	F73	IO_AERR_L
A82	IO_A(23)	B74	GROUND	C82	IO_A(21)	D74	IO_REQ4_L	E82	GROUND	F74	IO_REQ1_L
A83	NO CONNECT	B75	GROUND	C83	IO_A(14)	D75	IO_LOCK_L	E83	GROUND	F75	IO_HITM_L
A84	NO CONNECT	B76	GROUND	C84	IO_A(5)	D76	IO_RP_L	E84	GROUND	F76	IO_DBSY_L
A85	IO_A(7)	B77	GROUND	C85	IO_A(12)	D77	IO_BNR_L	E85	GROUND	F77	IO_A(34)
A86	NO CONNECT	B78	GROUND	C86	NO CONNECT	D78	IO_A(33)	E86	GROUND	F78	IO_A(32)
A87	NO CONNECT	B79	GROUND	C87	IO_A(6)	D79	IO_A(31)	E87	GROUND	F79	IO_A(30)
A88	NO CONNECT	B80	GROUND	C88	NO CONNECT	D80	IO_A(28)	E88	GROUND	F80	IO_A(27)
A89	NO CONNECT	B81	GROUND	C89	IO_D(60)	D81	IO_A(26)	E89	GROUND	F81	IO_A(25)
A90	IO_D(56)	B82	GROUND	C90	IO_D(61)	D82	IO_A(22)	E90	GROUND	F82	IO_A(19)
A91	NO CONNECT	B83	GROUND	C91	IO_D(50)	D83	IO_A(18)	E91	GROUND	F83	IO_A(16)
A92	NO CONNECT	B84	GROUND	C92	IO_D(43)	D84	IO_A(15)	E92	GROUND	F84	IO_A(13)
A93	IO_D(45)	B85	GROUND	C93	IO_D(52)	D85	IO_A(10)	E93	GROUND	F85	IO_A(11)
A94	IO_D(39)	B86	GROUND	C94	IO_D(49)	D86	IO_A(8)	E94	GROUND	F86	IO_A(9)
A95	IO_D(31)	B87	GROUND	C95	IO_D(37)	D87	IO_A(3)	E95	GROUND	F87	IO_A(4)
A96	IO_D(33)	B88	GROUND	C96	IO_D(36)	D88	PG4_A_CRESET_L	E96	GROUND	F88	IO_D(63)
A97	NO CONNECT	B89	GROUND	C97	IO_D(35)	D89	IO_D(62)	E97	GROUND	F89	IO_D(58)
A98	IO_D(32)	B90	GROUND	C98	IO_D(29)	D90	IO_D(57)	E98	GROUND	F90	IO_D(59)
A99	IO_D(26)	B91	GROUND	C99	IO_D(30)	D91	IO_D(55)	E99	GROUND	F91	IO_D(54)
A100	IO_D(22)	B92	GROUND	C100	IO_D(19)	D92	IO_D(51)	E100	GROUND	F92	IO_D(53)
A101	NO CONNECT	B93	GROUND	C101	IO_D(18)	D93	IO_D(46)	E101	GROUND	F93	IO_D(48)

Table 2-51: I/O Bus Connector Pinout (Continued)

A102	IO_D(15)	B94	GROUND	C102	IO_D(7)	D94	IO_D(47)	E102	GROUND	F94	IO_D(44)
A103	NO CONNECT	B95	GROUND	C103	IO_D(9)	D95	IO_D(42)	E103	GROUND	F95	IO_D(38)
A104	IO_D(16)	B96	GROUND	C104	IO_D(5)	D96	IO_D(41)	E104	GROUND	F96	IO_D(40)
A105	NO CONNECT	B97	GROUND	C105	IO_D(1)	D97	IO_D(27)	E105	GROUND	F97	IO_D(34)
A106	IO_DEP_L(7)	B98	GROUND	C106	IO_D(3)	D98	IO_D(24)	E106	GROUND	F98	IO_D(28)
A107	IO_DEP_L(2)	B99	GROUND	C107	IO_DEP_L(6)	D99	IO_D(25)	E107	GROUND	F99	IO_D(21)
A108		B100	GROUND	C108	IO_DEP_L(1)	D100	IO_D(12)	E108	GROUND	F100	IO_D(17)
A109	CPU_SPI_RESET_L	B101	GROUND	C109	SPI_CPU_SEL_L	D101	IO_D(23)	E109	GROUND	F101	IO_D(14)
A110	SPI_SEL2_L	B102	GROUND	C110	SPI_SEL1_L	D102	IO_D(20)	E110	GROUND	F102	IO_D(13)
A111	SPI_SEL0_L	B103	GROUND	C111	SPI_MOSI	D103	IO_D(10)	E111	GROUND	F103	IO_D(8)
A112	SPI_MISO	B104	GROUND	C112	SPI_CLK	D104	IO_D(6)	E112	GROUND	F104	IO_D(11)
A113	I2C_BMC_SDA	B105	GROUND	C113	I2C_BMC_SCL	D105	IO_DEP_L(5)	E113	GROUND	F105	IO_D(4)
A114	I2C_GLOBAL_SDA	B106	GROUND	C114	I2C_GLOBAL_SCL	D106	IO_D(0)	E114	GROUND	F106	IO_D(2)
A115	I2C_DS2P1_SDA	B107	GROUND	C115	I2C_DS2P1_SCL	D107	IO_DEP_L(3)	E115	GROUND	F107	IO_DEP_L(4)
A116	I2C_DS2P0_SDA	B108	GROUND	C116	I2C_DS2P0_SCL	D108	NO CONNECT	E116	GROUND	F108	IO_DEP_L(0)
A169	GLOBAL_SCLK	B109	GROUND	C169	GLOBAL_MODE	D109	ADC_OSC_RESET	E169	GROUND	F109	INIT_L
A170	ISP_CPU_EN_L	B110	GROUND	C170	GLOBAL_SDI	D110	A20M_L	E170	GROUND	F110	INTR
A171	RESERVED	B111	GROUND	C171	VCC_STDBY	D111	CPU_SLP_L	E171	GROUND	F111	FERR_L
A172	RESERVED	B112	GROUND	C172	I2C_CEL_CONNECT_BMC_A	D112	STOP_CLK_L	E172	GROUND	F112	IGNNE_L
A173	FAN_FAILED_L	B113	GROUND	C173	PROC_RESET_L	D113	MEM_SBCERR_L	E173	GROUND	F113	PICD(1)
A174	SECURE_MODE_BMC	B114	GROUND	C174	FP_TO_PIIX_PWRBTN	D114	PICD(0)	E174	GROUND	F114	PIIX_SMB_SCL
A175	NO CONNECT	B115	GROUND	C175	INTRUSION_L	D115	PIIX_SMB_SDA	E175	GROUND	F115	PIC_CLK

Table 2-51: I/O Bus Connector Pinout (Continued)

A176	SPEAKER_DATA	B116	GROUND	C176	I2C_CEL_CONNECT_FPC	D116	PIIX_SMB_SEL1	E176	GROUND	F116	PIIX_SMB_SEL0
A177	PWR_CNTRL_RTC_L	B165	+12V	C177	PWR_CNTRL_SFC_L	D165	+5V	E177	GROUND	F165	+3.3V
A178	FP_NMI_SWT_L	B166	+12V	C178	HARD_RESET	D166	+5V	E178	GROUND	F166	+3.3V
A179	COM2_TO_FP_EN	B167	+12V	C179	COM2_TO_SIO_EN_A	D167	+5V	E179	GROUND	F167	+3.3V
A180	SMI_L	B168	+12V	C180	NMI_5V	D168	+5V	E180	GROUND	F168	+3.3V
		B169	GROUND			D169	IO_TDO			F169	IO_TDI
		B170	GROUND			D170	IO_TMS			F170	SCSI_TCLK
		B171	GROUND			D171	IO_TRST_L			F171	VCC_STDBY
		B172	GROUND			D172	VCC_STDBY			F172	VCC_STDBY
		B173	GROUND			D173	VCC_STDBY			F173	I2C_BACKUP_SDA
		B174	GROUND			D174	I2C_BACKUP_SCL			F174	I2C_FPC_SDA
		B175	GROUND			D175	I2C_FPC_SCL			F175	DTR_TTL_FP
		B176	GROUND			D176	RTS_TTL_FP			F176	RI_TTL_FP
		B177	GROUND			D177	CTS_TTL_FP			F177	DSR_TTL_FP
		B178	GROUND			D178	DCD_TTL_FP			F178	SOUT_TTL_XIMB
		B179	GROUND			D179	SOUT_TTL_COM2			F179	SIN_TTL_XIMB
		B180	GROUND			D180	SIN_TTL_COM2			F180	XIMB_SOUT_EN
		B181	+12V			D181	+5V			F181	+5V
		B182	+12V			D182	+5V			F182	+5V
		B183	+12V			D183	+5V			F183	+5V
		B184	+12V			D184	+5V			F184	+5V

The I/O carrier uses a connector equivalent to BERG* 73956-9003 to interface with the Profusion carrier.

2.4.2 PCI Connectors (64-bit)

Table 2-52: 33-MHz, 64-bit PCI Connectors (Slots A and B)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	TRST_L	A48	GND	B1	-12V	B48	AD10
A2	+12V	A49	AD9	B2	TCK	B49	M66EN
A3	TMS	A50	5V KEYWAY	B3	GND	B50	5V KEYWAY
A4	TDI	A51		B4	TDO	B51	
A5	+5V	A52	C/BEO_L	B5	+5V	B52	AD8
A6	INTA_L	A53	+3.3V	B6	+5V	B53	AD7
A7	INTC_L	A54	AD6	B7	INTB_L	B54	+3.3V
A8	+5V	A55	AD4	B8	INTD_L	B55	AD5
A9	RESERVED	A56	GND	B9	PRSNT1_L	B56	AD3
A10	+5V	A57	AD2	B10	RESERVED	B57	GND
A11	RESERVED	A58	AD0	B11	PRSNT2_L	B58	AD1
A12	GND	A59	+5V	B12	GND	B59	+5V
A13	GND	A60	REQ64_L	B13	GND	B60	ACK64_L
A14	RESERVED	A61	+5V	B14	RESERVED	B61	+5V
A15	RESET_L	A62	+5V	B15	GND	B62	+5V
A16	+5V	A63	GND	B16	CLK	B63	RESERVED
A17	GRANT_L	A64	C/BE7_L	B17	GND	B64	GND
A18	GND	A65	C/BE5_L	B18	REQ_L	B65	C/BE6_L
A19	RESERVED	A66	+5V	B19	+5V	B66	C/BE4_L

Table 2-52: 33-MHz, 64-bit PCI Connectors (Slots A and B) (Continued)

A20	AD30	A67	PAR64	B20	AD31	B67	GND
A21	+3.3V	A68	AD62	B21	AD29	B68	AD63
A22	AD28	A69	GND	B22	GND	B69	AD61
A23	AD26	A70	AD60	B23	AD27	B70	+5V
A24	GND	A71	AD58	B24	AD25	B71	AD59
A25	AD24	A72	GND	B25	+3.3V	B72	AD57
A26	IDSEL	A73	AD56	B26	C/BE3_L	B73	GND
A27	+3.3V	A74	AD54	B27	AD23	B74	AD55
A28	AD22	A75	+5V	B28	GND	B75	AD53
A29	AD20	A76	AD52	B29	AD21	B76	GND
A30	GND	A77	AD50	B30	AD19	B77	AD51
A31	AD18	A78	GND	B31	+3.3V	B78	AD49
A32	AD16	A79	AD48	B32	AD17	B79	+5V
A33	+3.3V	A80	AD46	B33	C/BE2_L	B80	AD47
A34	FRAME_L	A81	GND	B34	GND	B81	AD45
A35	GND	A82	AD44	B35	IRDY_L	B82	GND
A36	TRDY_L	A83	AD42	B36	+3.3V	B83	AD43
A37	GND	A84	+5V	B37	DEVSEL_L	B84	AD41
A38	STOP_L	A85	AD40	B38	GND	B85	+5V
A39	+3.3V	A86	AD38	B39	LOCK_L	B86	AD39

Table 2-52: 33-MHz, 64-bit PCI Connectors (Slots A and B) (Continued)

A40	SDONE	A87	GND	B40	PERR_L	B87	AD37
A41	SB0_L	A88	AD36	B41	+3.3V	B88	+5V
A42	GND	A89	AD34	B42	SERR_L	B89	AD35
A43	PAR	A90	GND	B43	+3.3V	B90	AD33
A44	AD15	A91	AD32	B44	C/BE1_L	B91	GND
A45	+3.3V	A92	RESERVED	B45	AD14	B92	RESERVED
A46	AD13	A93	GND	B46	GND	B93	RESERVED
A47	AD11	A94	RESERVED	B47	AD12	B94	GND

Table 2-53: 66-MHz, 64-bit PCI Connectors (Slots C and D)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	TRST_L	A48	GND	B1	-12V	B48	AD10
A2	+12V	A49	AD9	B2	TCK	B49	M66EN
A3	TMS	A50	GND	B3	GND	B50	GND
A4	TDI	A51	GND	B4	TDO	B51	GND
A5	+5V	A52	C/BEO_L	B5	+5V	B52	AD8
A6	INTA_L	A53	+3.3V	B6	+5V	B53	AD7
A7	INTC_L	A54	AD6	B7	INTB_L	B54	+3.3V
A8	+5V	A55	AD4	B8	INTD_L	B55	AD5
A9	RESERVED	A56	GND	B9	PRSNT1_L	B56	AD3
A10	+3.3V	A57	AD2	B10	RESERVED	B57	GND
A11	RESERVED	A58	AD0	B11	PRSNT2_L	B58	AD1
A12	3.3V KEYWAY	A59	+3.3V	B12	3.3V KEYWAY	B59	+3.3V
A13		A60	REQ64_L	B13		B60	ACK64_L
A14	RESERVED	A61	+5V	B14	RESERVED	B61	+5V
A15	RESET_L	A62	+5V	B15	GND	B62	+5V

Table 2-53: 66-MHz, 64-bit PCI Connectors (Slots C and D) (Continued)

A16	+3.3V	A63	GND	B16	CLK	B63	RESERVED
A17	GRANT_L	A64	C/BE7_L	B17	GND	B64	GND
A18	GND	A65	C/BE5_L	B18	REQ_L	B65	C/BE6_L
A19	RESERVED	A66	+3.3V	B19	+3.3V	B66	C/BE4_L
A20	AD30	A67	PAR64	B20	AD31	B67	GND
A21	+3.3V	A68	AD62	B21	AD29	B68	AD63
A22	AD28	A69	GND	B22	GND	B69	AD61
A23	AD26	A70	AD60	B23	AD27	B70	+3.3V
A24	GND	A71	AD58	B24	AD25	B71	AD59
A25	AD24	A72	GND	B25	+3.3V	B72	AD57
A26	IDSEL	A73	AD56	B26	C/BE3_L	B73	GND
A27	+3.3V	A74	AD54	B27	AD23	B74	AD55
A28	AD22	A75	+3.3V	B28	GND	B75	AD53
A29	AD20	A76	AD52	B29	AD21	B76	GND
A30	GND	A77	AD50	B30	AD19	B77	AD51
A31	AD18	A78	GND	B31	+3.3V	B78	AD49
A32	AD16	A79	AD48	B32	AD17	B79	+3.3V
A33	+3.3V	A80	AD46	B33	C/BE2_L	B80	AD47
A34	FRAME_L	A81	GND	B34	GND	B81	AD45
A35	GND	A82	AD44	B35	IRDY_L	B82	GND
A36	TRDY_L	A83	AD42	B36	+3.3V	B83	AD43
A37	GND	A84	+3.3V	B37	DEVSEL_L	B84	AD41
A38	STOP_L	A85	AD40	B38	GND	B85	+5V
A39	+3.3V	A86	AD38	B39	LOCK_L	B86	AD39
A40	SDONE	A87	GND	B40	PERR_L	B87	AD37
A41	SB0_L	A88	AD36	B41	+3.3V	B88	+3.3V
A42	GND	A89	AD34	B42	SERR_L	B89	AD35
A43	PAR	A90	GND	B43	+3.3V	B90	AD33
A44	AD15	A91	AD32	B44	C/BE1_L	B91	GND
A45	+3.3V	A92	RESERVED	B45	AD14	B92	RESERVED
A46	AD13	A93	GND	B46	GND	B93	RESERVED
A47	AD11	A94	RESERVED	B47	AD12	B94	GND

Notes:

The M66EN pin will be tied to GND for all PCI slots on PCI-A and PCI-B. M66EN will be tied to +3.3 V for all PCI slots on PCI-C and PCI-D.

The I/O carrier uses a connector equivalent to AMP* 145034-1 to interface with the 64-bit PCI bus.

2.4.3 SCSI Connector

Table 2-54: SCSI Connector/Single Ended Mode

Signal Name	Conn. Pin	Cable Pin	Cable Pin	Conn. Pin	Signal Name
GROUND	1	1	2	35	DB(12)#
GROUND	2	3	4	36	DB(13)#
GROUND	3	5	6	37	DB(14)#
GROUND	4	7	8	38	DB(15)#
GROUND	5	9	10	39	DB(P1)#
GROUND	6	11	12	40	DB(0)#
GROUND	7	13	14	41	DB(1)#
GROUND	8	15	16	42	DB(2)#
GROUND	9	17	18	43	DB(3)#
GROUND	10	19	20	44	DB(4)#
GROUND	11	21	22	45	DB(5)#
GROUND	12	23	24	46	DB(6)#
GROUND	13	25	26	47	DB(7)#
GROUND	14	27	28	48	DB(P)#
GROUND	15	29	30	49	GROUND
DIFSENSE	16	31	32	50	GROUND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED (NC)	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
GROUND	21	41	42	55	ATN#
GROUND	22	43	44	56	GROUND
GROUND	23	45	46	57	BSY#

Table 2-54: SCSI Connector/Single Ended Mode (Continued)

GROUND	24	47	48	58	ACK#
GROUND	25	49	50	59	RST#
GROUND	26	51	52	60	MSG#
GROUND	27	53	54	61	SEL#
GROUND	28	55	56	62	C/D#
GROUND	29	57	58	63	REQ#
GROUND	30	59	60	64	I/O#
GROUND	31	61	62	65	DB(8)#
GROUND	32	63	64	66	DB(9)#
GROUND	33	65	66	67	DB(10)#
GROUND	34	67	68	68	DB(11)#

The I/O carrier uses a FOXCONN* QA01343-P4 connector or equivalent to interface to the SCSI bus.

Table 2-55: SCSI Connector/LVDS Mode

Signal Name	Conn. Pin	Cable Pin	Cable Pin	Conn. Pin	Signal Name
+DB(12)	1	1	2	35	-DB(12)
+DB(13)	2	3	4	36	-DB(13)
+DB(14)	3	5	6	37	-DB(14)
+DB(15)	4	7	8	38	-DB(15)
+DB(P1)	5	9	10	39	-DB(P1)
+DB(0)	6	11	12	40	-DB(0)
+DB(1)	7	13	14	41	-DB(1)
+DB(2)	8	15	16	42	-DB(2)
+DB(3)	9	17	18	43	-DB(3)
+DB(4)	10	19	20	44	-DB(4)
+DB(5)	11	21	22	45	-DB(5)
+DB(6)	12	23	24	46	-DB(6)
+DB(7)	13	25	26	47	-DB(7)

Table 2-55: SCSI Connector/LVDS Mode (Continued)

+DB(P0)	14	27	28	48	-DB(P0)
GROUND	15	29	30	49	GROUND
DIFSENSE	16	31	32	50	GROUND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED (NC)	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
+ATN	21	41	42	55	-ATN
GROUND	22	43	44	56	GROUND
+BSY	23	45	46	57	-BSY
+ACK	24	47	48	58	-ACK
+RST	25	49	50	59	-RST
+MSG	26	51	52	60	-MSG
+SEL	27	53	54	61	-SEL
+C/D	28	55	56	62	-C/D
+REQ	29	57	58	63	-REQ
+I/O	30	59	60	64	-I/O
+DB(8)	31	61	62	65	-DB(8)
+DB(9)	32	63	64	66	-DB(9)
+DB(10)	33	65	66	67	-DB(10)
+DB(11)	34	67	68	68	-DB(11)

2.4.4 IDE Connector

Table 2-56: IDE Connector

Pin	Signal	Pin	Signal
1	RSTDRV	2	GROUND
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD1

Table 2-56: IDE Connector (Continued)

11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GROUND	20	KEY PIN
21	DRQ	22	GROUND
23	DIOW	24	GROUND
25	DIOR	26	GROUND
27	IORDY	28	CSEL
29	DACK	30	GROUND
31	IRQ	32	No Connection
33	DA1	34	No Connection
35	DA0	36	DA2
37	CS1P_L	38	DS3P_L
39	DHACT_L	40	GROUND

The I/O carrier uses a connector equivalent to an AMP 111945-8 40-pin header or equivalent to interface to both the primary and secondary IDE buses.

2.4.5 Floppy Disk Port Connection

Table 2-57: Floppy Disk Connector

Pin	Name	Pin	Name
1	GND	2	FD_DENSEL
3	GND	4	n/c
5	Key	6	FD_DRATE0
7	GND	8	FD_INDEX_L
9	GND	10	FD_MTR0_L
11	GND	12	FD_DR1_L
13	GND	14	FD_DR0_L
15	GND	16	FD_MTR1_L

Table 2-57: Floppy Disk Connector (Continued)

17	FD_MSEN1	18	FD_DIR_L
19	GND	20	FD_STEP_L
21	GND	22	FD_WDATA_L
23	GND	24	FD_WGATE_L
25	GND	26	FD_TRK0_L
27	FD_MSEN0	28	FD_WPROT_L
29	GND	30	FD_RDATA_L
31	GND	32	FD_HDSEL_L
33	GND	34	FD_DSKCHG_L

The I/O carrier uses a connector equivalent to AMP 111944-7 or equivalent to interface to the floppy port.

2.4.6 USB Connector

Table 2-58: USB Connector

Pin	Signal	Description
A1	VCC	Over Current Monitor Line Port 0.
A2	DATAL0	Differential Data Line Paired with DATAH0.
A3	DATAH0	Differential Data Line Paired with DATAL0.
A4	GND	Ground Potential.
B1	VCC	Over Current Monitor Line Port 1.
B2	DATAL1	Differential Data Line Paired with DATAH1.
B3	DATAH1	Differential Data Line Paired with DATAL1.
B4	GND	Ground Potential.

The I/O carrier uses a FOXCONN/Hon Hai* DM10156-73 connector or equivalent to interface to the USB.

2.4.7 I²C* Feature Connector Pin Assignments

Table 2-59: I²C Feature Connector Pin Assignments*

Pin	Name	Pin	Name
1	SMI#	2	I2CCLK
3	CONP	4	key
5	PWROFF#	6	I2CDATA
7	LPOK	8	KEYUNLK
9	NMI	10	HostAUX
11	RESET#	12	GND
13	GND	14	key
15	SECURE	16	GND
17	INTRUD#	18	NMI_L
19	INIT_L	20	GND
21	KB_DATA	22	MS_DATA
23	KB_CLK	24	MS_CLK
25	Key	26	RESET_BMC_L

2.4.8 I²C* Connector

Table 2-60: I²C Connector*

Name	Pin
CLK	1
GND	2
DATA	3

2.4.9 Legacy Connections

The I/O carrier provides connection to VGA, serial, parallel, mouse and keyboard functions by means of the A450NX I/O riser board mounted to the baseboard. The A450NX I/O riser board provides the direct user interface. Section I/O Bus Connector provides the pinout of the connector on the I/O carrier, whereas following sections provide the pinout of the user level interfaces of the A450NX I/O riser board.

Table 2-61: Legacy Connections

Pin	Signal	Pin	Signal
A1	VCC_STDBY	B1	+5V
A2	KB_DATA	B2	MS_DATA
A3	KB_CLK	B3	MS_CLK
A4	+5V	B4	SIN_TTL_XIMB
A5	SOUT_TTL_XIMB	B5	SIN_TTL_COM2
A6	PP_SLCT	B6	SP0_DCD_L
A7	PP_PE	B7	SP1_DCD_L
A8	PP_BUSY	B8	SP0_SIN
A9	PP_ACK_L	B9	Ground
A10	Ground	B10	SP1_SIN
A11	PP_DR7	B11	SP0_RI_L
A12	PP_DR6	B12	SP1_RI_L
A13	PP_DR5	B13	Ground
A14	PP_DR4	B14	SP0_DTR_L
A15	Ground	B15	SP1_DTR_L
A16	PP_DR3	B16	SP0_SOUT
A17	PP_DR2	B17	SP1_SOUT
A18	PP_DR1	B18	No Connection
A19	PP_DR0	B19	SP0_DSR_L
A20	Ground	B20	SP1_DSR_L
A21	PP_STB_L	B21	SP0_RTS_L
A22	PP_SLIN_L	B22	Ground
A23	PP_INIT_L	B23	SP1_RTS_L
A24	PP_ERR_L	B24	SP0_CTS_L

Table 2-61: Legacy Connections (Continued)

A25	PP_AFD_L	B25	SP1_CTS_L
A26	I2C_BMC_SCL	B26	RTL_TTL_FP_L
A27	DSR_TTL_FP	B27	DTR_TTL_FP_L
A28	CTS_TTL_FP	B28	DCD_TTL_FP_L
A29	RT_TTL_FP	B29	I2C_BMC_SDA
A30	COM2_TO_STD_EN	B30	XIMB_SOUT_EN
A31	COM2_TO_FP_EN	B31	SOUT_TTL_COM2
A32	Ground	B32	PWR_GOOD
A33	Ground	B33	Ground
A34	Ground	B34	Ground
A35	V_BLUE	B35	V_VSYNC
A36	Ground	B36	Ground
A37	V_GREEN	B37	V_HSYNC
A38	Ground	B38	Ground
A39	V_RED	B39	VR_DDCDAT
A40	Ground	B40	VR_DDCCLK

The I/O carrier uses a connector equivalent to an AMP 650090-3 connector to connect the A450NX I/O riser board to the I/O carrier. The “B” signals listed above are located on the primary side of the A450NX I/O riser board (the primary side is the USB connector side, if you are looking at the I/O carrier). The “A” signals are located on the secondary side of the A450NX I/O riser board (the secondary side is the ISA slot side, if you are looking at the I/O carrier). Pin 1 is located toward the front of the board (away from the connectors on the A450NX I/O riser board and toward the PB64 heat sinks). Pin 40 is located nearest the connectors.

2.4.9.1 VGA Connector

Table 2-62: Video Port Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	RED	Analog color signal R.	2	GREEN	Analog color signal G.
3	BLUE	Analog color signal B.	4	n/c	No connect.
5	GND	Video ground (shield).	6	GND	Video ground (shield).

Table 2-62: Video Port Connector Pinout (Continued)

7	GND	Video ground (shield).	8	GND	Video ground (shield).
9	n/c	No connect.	10	GND	Video ground.
11	n/c	No connect.	12	n/c	No connect.
13	HSYNC	Horizontal sync.	14	VSYNC	Vertical sync.
15	n/c	No connect.			

2.4.9.2 Serial Port Connector

Table 2-63: Serial Port Connector

Pin	Name	Description	Pin	Name	Description
1	DCD	Data Carrier Detected	2	RXD	Receive Data
3	TXD	Transmit Data	4	DTR	Data Terminal Ready
5	GND	Ground	6	DSR	Data Set Ready
7	RTS	Return to Send	8	CTS	Clear to Send
9	RIA	Ring Indication Active			

The I/O carrier uses a FOXCONN/Hon Hai DM10156-73 connector or equivalent to interface with each serial port.

2.4.9.3 Parallel Port Connection

Table 2-64: Parallel Port Connection

Pin	Name	Pin	Name
1	STROBE_L	14	AUFDXT_L
2	D0	15	ERROR_L
3	D1	16	INIT_L
4	D2	17	SLCTIN_L
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND

Table 2-64: Parallel Port Connection (Continued)

8	D6	21	GND
9	D7	22	GND
10	ACK_L	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

2.4.9.4 Mouse Connector

Table 2-65: Mouse Connector

Pin	Signal	Description
7	MSEDAT	Mouse data.
8	(NC)	
9	GND	
10	FUSED_VCC	
11	MSECLK	Mouse clock.
12	(NC)	

2.4.9.5 Keyboard Connector

Table 2-66: Keyboard Connector

Pin	Signal	Description
1	KEYDAT	Keyboard data.
2	(NC)	
3	GND	
4	FUSED_VCC	
5	KEYCLK	Keyboard clock.
6	(NC)	

2.4.10 PHP LED/Switch Connector

Table 2-67: PHP LED/Switch Connector

Pin	Signal	Description
1	S1_A_SWITCH	Slot 1, Bus A, Intrusion switch signal
2	S2_A_SWITCH	Slot 2, Bus A, Intrusion switch signal
3	S1_A_GREEN	Slot 1, Bus A, Green LED control signal
4	S2_A_GREEN	Slot 2, Bus A, Green LED control signal
5	S1_A_AMBER	Slot 1, Bus A, Amber LED control signal
6	S2_A_AMBER	Slot 2, Bus A, Amber LED control signal
7	S1_B_SWITCH	Slot 1, Bus B, Intrusion switch signal
8	S2_B_SWITCH	Slot 2, Bus B, Intrusion switch signal
9	S1_B_GREEN	Slot 1, Bus B, Green LED control signal
10	S2_B_GREEN	Slot 2, Bus B, Green LED control signal
11	S1_B_AMBER	Slot 1, Bus B, Amber LED control signal
12	S2_B_AMBER	Slot 2, Bus B, Amber LED control signal
13	S3_B_SWITCH	Slot 3, Bus B, Intrusion switch signal
14	S4_B_SWITCH	Slot 4, Bus B, Intrusion switch signal
15	S3_B_GREEN	Slot 3, Bus B, Green LED control signal
16	S4_B_GREEN	Slot 4, Bus B, Green LED control signal
17	S3_B_AMBER	Slot 3, Bus B, Amber LED control signal
18	S4_B_AMBER	Slot 4, Bus B, Amber LED control signal
19	S1_C_SWITCH	Slot 1, Bus C, Intrusion switch signal
20	S2_C_SWITCH	Slot 2, Bus C, Intrusion switch signal
21	S1_C_GREEN	Slot 1, Bus C, Green LED control signal
22	S2_C_GREEN	Slot 2, Bus C, Green LED control signal
23	S1_C_AMBER	Slot 1, Bus C, Amber LED control signal
24	S2_C_AMBER	Slot 2, Bus C, Amber LED control signal
25	S1_D_SWITCH	Slot 1, Bus D, Intrusion switch signal
26	S2_D_SWITCH	Slot 2, Bus D, Intrusion switch signal
27	S1_D_GREEN	Slot 1, Bus D, Green LED control signal
28	S2_D_GREEN	Slot 2, Bus D, Green LED control signal

Table 2-67: PHP LED/Switch Connector (Continued)

29	S1_D_AMBER	Slot 1, Bus D, Amber LED control signal
30	S2_D_AMBER	Slot 2, Bus D, Amber LED control signal
31	3.3V	VCC
32	GROUND	GND
33	3.3V	VCC
34	GROUND	GND
35	3.3V	VCC
36	GROUND	GND
37	3.3V	VCC
38	GROUND	GND
39	3.3V	VCC
40	GROUND	GND

2.4.11 Voltage Tolerances

Table 2-68: Voltage Tolerances

DC Voltage	Acceptable Tolerance
3.3 V	± 5%
5 V	± 5%
5 V standby	± 5%
12 V	± 5%

3. OPRF100 Profusion* Carrier

This chapter describes the architecture of the Profusion* carrier which is part of the OPRF100 MP board set. The Profusion carrier interfaces to the midplane board through a 1008-pin connector.

Features

The Profusion carrier has the following features:

- Two processor mezzanine connectors to accommodate one to eight Pentium® II Xeon™ processors.
- Two 72-pin SO-DIMM connectors for two cache coherency filters.
- One Profusion memory controller (memory access controller (MAC) and data interface buffer (DIB)).
- System clock generator.
- System boundary scan interface.
- Onboard DC-DC converters for the CPU bus and I/O bus Vtt power.
- Onboard DC-DC converter for 2.5 V power.
- I^2C, serial peripheral interface (SPI) and in-system programming (ISP) server management interfaces.

3.1 Introduction

This section provides an overview of the Profusion carrier, showing functional blocks and board layout.

3.1.1 Block Diagram

Figure 3-1: Profusion* Carrier Block Diagram illustrates the high level architecture of the Profusion carrier and Profusion PCIset.

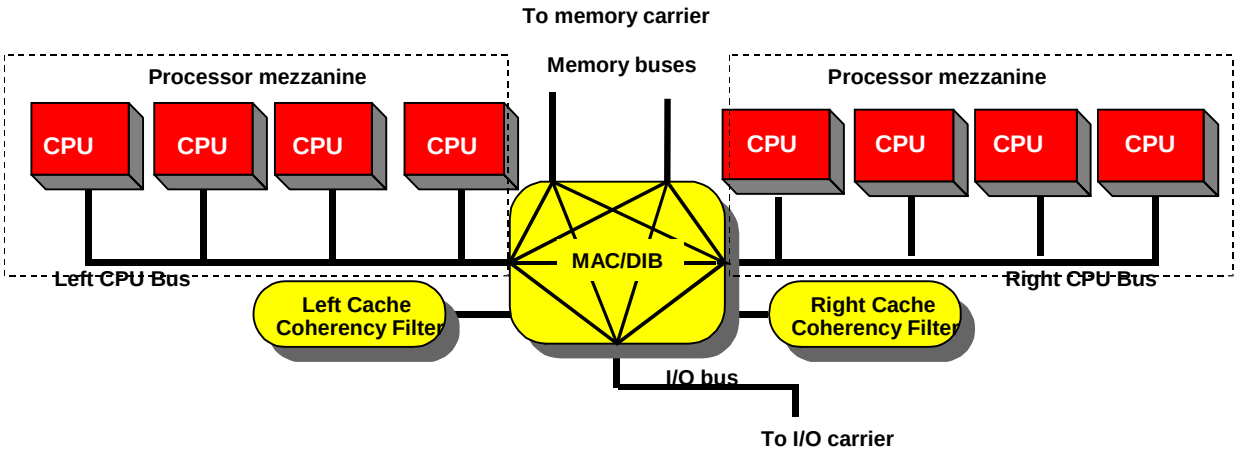


Figure 3-1: Profusion Carrier Block Diagram*

3.1.2 Architectural Overview

The Profusion carrier provides connectors for the processor mezzanine boards. It contains a modular grand connector, which connects to the midplane; it also contains a connector for the front panel. The Profusion carrier design is partitioned according to the following functional blocks:

- Two front-side buses (processor buses) with a processor mezzanine connector per bus.
- Two memory buses which interface to two memory carriers through connectors on the midplane.
- I/O carrier interface through a 100-MHz I/O bus connection through the grand connector.
- Clock generation.
- System management logic.
- Voltage regulators.
- Configuration jumpers.

The Profusion PCIset components (MAC and DIB) reside on the Profusion carrier and provide an interface to the main processor, memory, and I/O buses. The primary front-side bus (FSB) is used to connect the four processors on the primary processor mezzanine board. A secondary FSB is used to connect the four processors on the secondary processor mezzanine board. The I/O bus is used to provide an interface to four PB64s (PCI 64-bit bridges) and subsequently the onboard video, LVD SCSI, and other I/O expansion devices. The memory subsystem buses provide an interface to two separate memory carriers. One bus is used to connect to the primary memory carrier, and the other bus connects to the secondary memory carrier. The Profusion PCIset provides one last interface bus used to interface to the primary and secondary coherency filter tag static RAM (SRAM) DIMMs.

3.1.3 Placement Diagram

The following diagram shows the placement of the major components and connectors on the Profusion carrier.

Note, the connectors described below are clockwise from bottom.

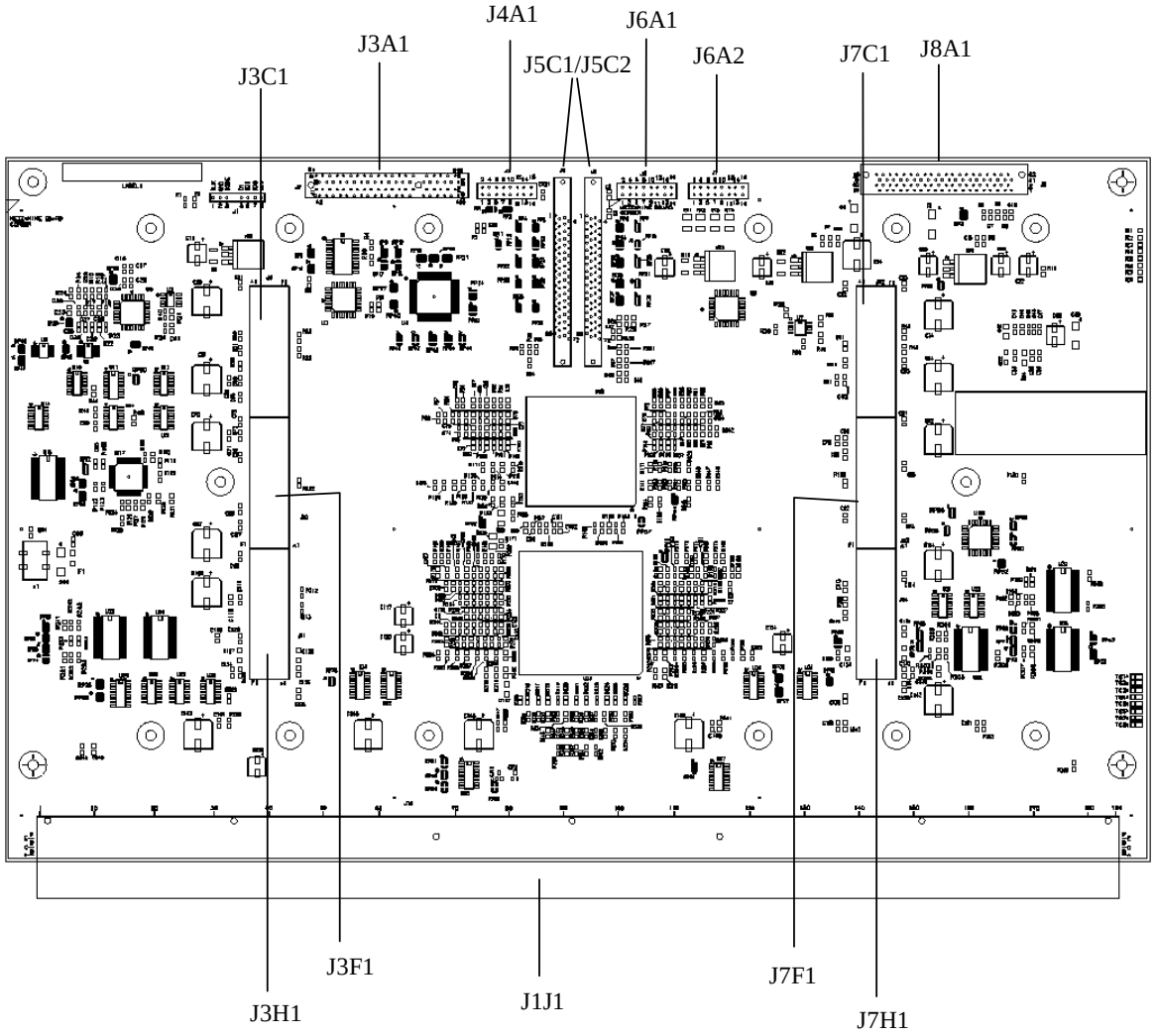


Figure 3-2: Profusion* Carrier Layout

- J1J1: Midplane connector (grand connector).
- J7C1/J7F1/J7H1:Processor mezzanine board #1 connector (primary).
- J3A1: System JTAG connector.
- J6A1: Board configuration jumper block.
- J5C1/J5C2: Tag DIMM sockets.
- J3C1/J3F1/J3H1:Processor mezzanine board #2 connector (secondary).
- J8A1: Front panel connector.
- J4A1/J6A2Depopulated configuration jumper blocks.

3.2 Functional Architecture

This section provides a more detailed architectural description of the Profusion carrier functional blocks.

3.2.1 Front-side Bus (FSB)

The FSB is an ECC protected 64-bit bus using GTL+ technology and running at 100 MHz. It is functionally compatible with the Pentium® Pro processor bus. Instead of the daisy chain routing of the Pentium Pro processor bus with one set of termination resistors on each end of the bus, the FSB uses a stubbed topology with distributed termination resistors (150 ohm) at the end of each of its six stubs. The FSB requires special GTL+ buffers employing active termination through a p-channel pull-up device at each output buffer.

Because each stub of the FSB must be terminated, the FSB requires termination modules to be installed in each unused processor slot. In systems with more than four processors, both mezzanine connectors will contain processor mezzanine boards while any unused processor connectors on the mezzanine will contain processor termination modules. In systems with four or fewer processors, only one mezzanine connector need be populated with a processor mezzanine board. At the user's option, the second mezzanine board can be installed or left unpopulated. No termination of an empty processor mezzanine connector is required. Additionally, if the second processor mezzanine board is installed and no processors are populated in it, then no processor termination modules are necessary for the second board.

3.2.2 Memory Interface

The memory subsystem consists of two memory carriers, each containing sixteen 72-bit wide DIMM sockets, providing up to 16 GB of SDRAM memory per carrier. Separate memory address, control, and data buses are routed from the MAC and DIB components on the Profusion carrier to the two memory carriers. In addition, there are dedicated buffer control signals for each of the memory carrier connectors.

A set of control signals connects the MAC to the DIB component in order to allow the MAC to control the operation of the DIB. The MAC connects to the control signals of the primary front-side bus, the secondary front-side bus, and the I/O bus. This allows for the interchange of information between the two processor buses and the PB64 PCI host bridges on the I/O carrier. Thus, a processor on either processor bus (right or left) or an I/O device can access the memory arrays connected to the DIB.

The MAC has two separate interfaces to the custom coherency filter tag SRAM DIMMs. The two SRAM DIMMs hold cache coherency data used to filter traffic traveling from one CPU bus to the other. The SRAM modules are installed into the 72-pin DIMM sockets defined in Section Coherency DIMM Interface Signals. The coherency filter tag SRAM DIMMs are based on 256K x 18 cache RAM components, and they are powered from +3.3 V power.

The DIB connects to the data bus signals of the primary front-side bus, the secondary front-side bus, and the I/O bus. The DIB interfaces to the two memory arrays, each of which contains six-

teen 168-pin Synchronous DRAM (SDRAM) DIMM sockets. Therefore, the DIB can access a total of 32 DIMMs.

3.2.3 I/O Bus Interface

Like the processor bus, the I/O bus also uses GTL+ signaling technology. Instead of the stub or star topology of the FSB, the I/O bus uses the daisy chain routing of the Pentium Pro processor bus with one set of termination resistors on each end of the bus. The I/O bus, system management signals, system clock and reset signals, and legacy signals, connect to the Profusion carrier through a 1008-pin, 2 mm pin and socket connector. For connector numbering conventions, refer to Section Mechanical Specifications.

The I/O bus is a high-speed (100-MHz clocked on rising edge) bi-directional multisource link between the Profusion carrier and the I/O carrier. The I/O bus has enough bandwidth for two 64-bit, 33-MHz PCI buses and two 64-bit, 66-MHz PCI buses.

3.2.4 Clock Generation

Figure 3-3: Profusion* Carrier Clock Distribution shows the clock distribution architecture for the Profusion carrier. The clock frequency of the onboard clock oscillator is 100 MHz. The main clock buffer contains a multiplexer circuit that selects between the onboard 100-MHz clock (default) and an external test clock. Both are low-voltage TTL (LVTTL) levels. An active low CLK_MARGIN_L signal selects the external clock.

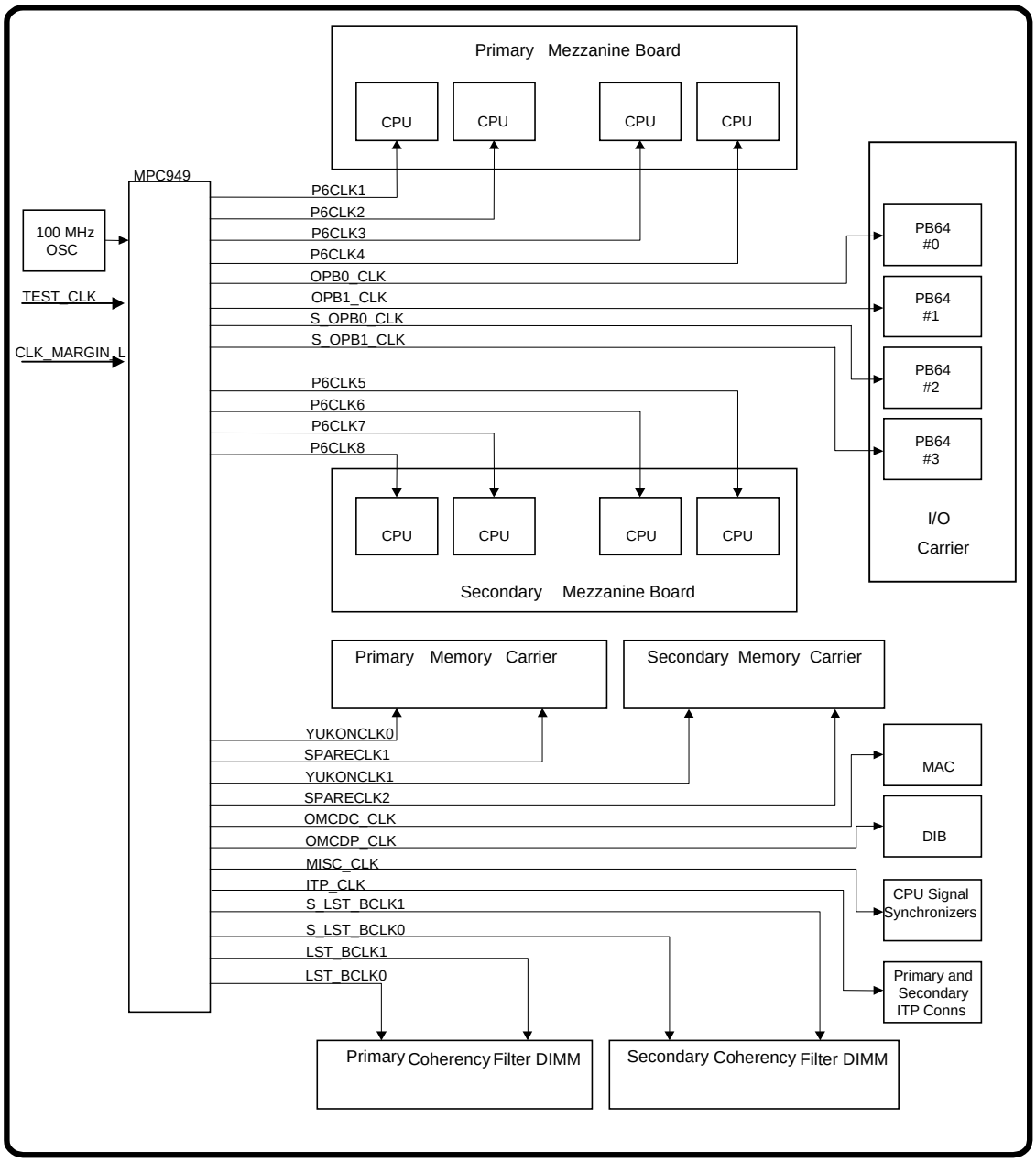


Figure 3-3: Profusion* Carrier Clock Distribution

3.2.5 System Management Interface

Figure 3-4: Profusion* Carrier System Management Logic shows the system management logic implemented on the Profusion carrier. The Profusion carrier contains five management buses:

- A private 3.3 V I^2C bus that connects all field replaceable unit (FRU) EEPROM I^2C devices on the Profusion carrier, memory carriers, and processor mezzanine boards.
- An SPI bus.

- A processor I^2C bus for the primary processor mezzanine board.
- A processor I^2C bus for the secondary processor mezzanine board.
- A switched System Management Bus (SMBus) interface to the Serial Presence Detect (SPD) EEPROMs on each memory carrier DIMM.

Each is used to gather different types of information. The first four buses are accessed through the baseboard management controller (BMC) via server management software like Intel®'s LANDesk® Server Manager. The fifth bus is accessed through the PIIX4E.

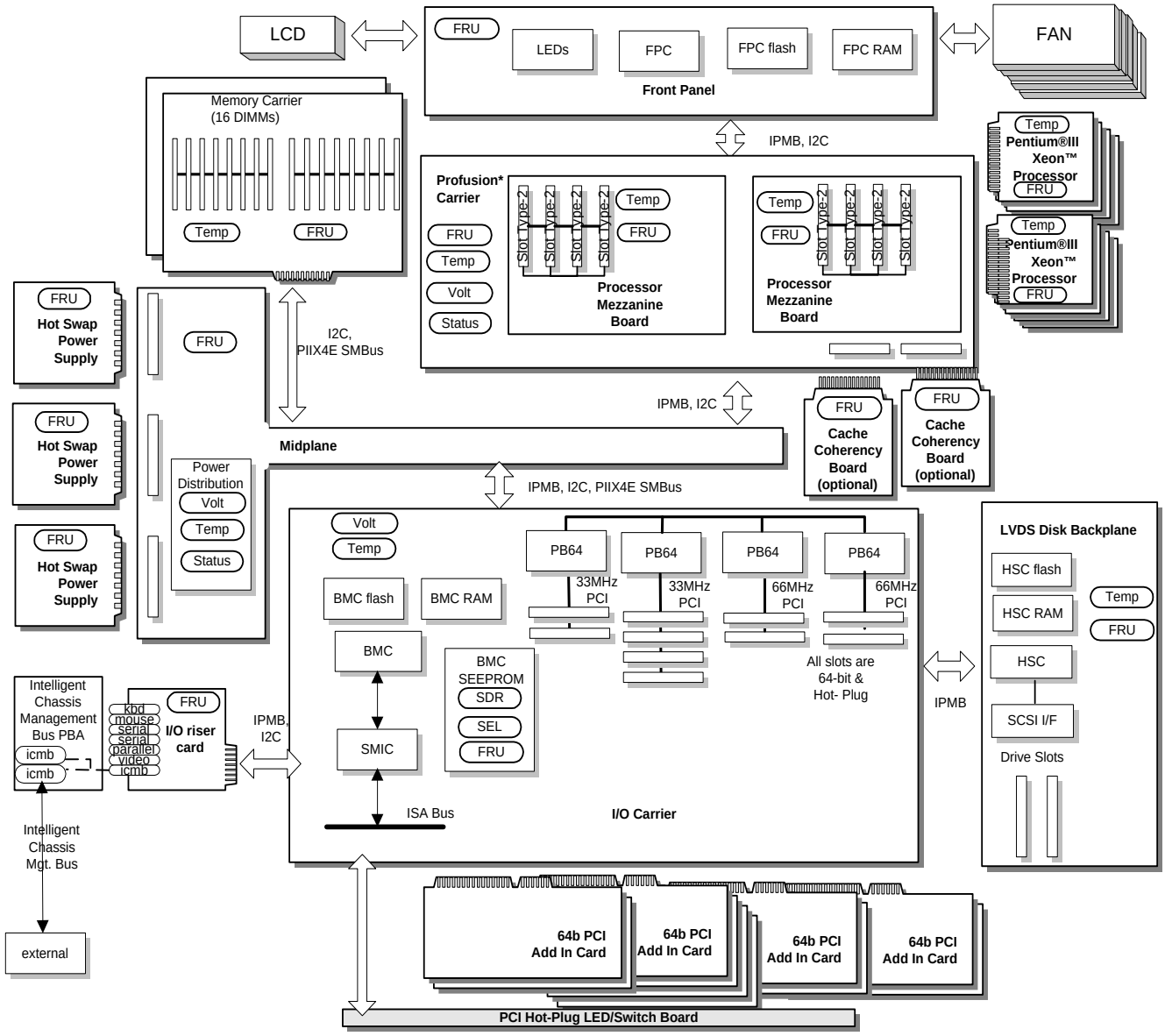


Figure 3-4: Profusion* Carrier System Management Logic

3.2.5.1 I²C* Accessed Features

The private I²C bus provides access to basic temperature, configuration, and inventory information. The Profusion carrier contains the following I²C accessible devices:

- Baseboard FRU/temp information (Dallas* DS1624).
- Coherency filter FRU information (Atmel* 24C02).

These are accessed via the BMC on the I/O carrier. The I²C devices are accessible at the following addresses:

Table 3-1: Profusion* Carrier I²C* Address Map

Device	I²C Address
Profusion* carrier FRU/temp information	98h,99h
Coherency filter 1 FRU information	A0h, A1h
Coherency filter 2 FRU information.	A2h, A3h

3.2.5.1.1 FRU SEEPROM

Serial EEPROMs, accessed via the I²C bus, provide non-volatile storage for the following FRU information. The FRU information is made available to higher level server management software through the Intel® Server Console (ISC) software.

Each SEEPROM has 256 bytes of programmable space that is broken into four areas. The SEPROM Programming Areas table lists the areas, a description of each area, and the amount of space allocated to each area.

Table 3-2: SEEPROM Programming Areas

Area	Size	Description
Common Header	8 bytes	Programming offsets to the other areas below.
Internal Use	48 bytes	This area is reserved for general purpose use by Intel®'s server management firmware/controllers. The only publicly defined region of this area is that for the format version number.

Table 3-2: SEEPROM Programming Areas (Continued)

Board Information	80 bytes	Contains the board FRU information listed in the table below.
Product Information	80 bytes	Available for OEM use.

FRU Information lists the board specific FRU information that will be programmed into the board information area.

Table 3-3: FRU Information

Board Information			
Information	**Description**	**Example**	**Notes**
Format Version	Specifies the version of the format definition for this area.	01h	1
Board Area Length	Defines the size of this area in multiples of 8 bytes.	0Ah = 80 bytes	1
Language Code	Specifies the language that the information is in.	00 = 8-bit Latin 1 ASCII	1
Mfg. Date/Time	Time and Date of Board Manufacture. (Value programmed (in hex) is the number of minutes after 0:00 hrs. 1/1/96.)	000f593h (Example: f593h = 62867 min., = 43 days and 947 min., = Feb 12, 1996, 3:47 p.m.)	2
Manufacturer Type/ Length byte	Specifies what type and how big the following field is.	C5h = 8 bit ASCII, 5 bytes	1
Manufacturer	Board manufacturer.	Intel	1
Board Product Name Type/Length byte	Specifies what type and how big the following field is.	DDh = 8 bit ASCII, 29 bytes	1
Board Product Name	Board name/description.	OPRF100 Profusion* carrier	1
Board Serial Number Type/Length byte	Specifies what type and how big the following field is.	CCh = 8 bit ASCII, 12 bytes	1
Board Serial Number	Intel® board serial number.	INSJ42385906	2
Board Part Number Type/Length byte	Specifies what type and how big the following field is.	CAh = 8 bit ASCII, 10 bytes	1
Board Part Number	Intel board part number.	704129-302	2
End of Information byte	Indicates no more info. Fields.	C1h	1

Notes:

1. Actual value programmed into the board.
2. Example value. Actual value will vary from board to board and/or from fab to fab. Last byte in Board Information Area is checksum (required).

Temperature and EEPROM data may be accessed via I^2C commands to the DS1624 device. The EEPROM Command Set table is taken from the DS1624 data sheet.

Table 3-4: EEPROM Command Set

Instruction	Description	Protocol	2-Wire Bus Data After Issuing Protocol	Notes
Temperature Conversion Commands				
Read Temperature	Read last converted temperature value from temperature register.	Aah	<read 2 bytes data>	
Start Convert T	Initiates temperature conversion.	Eeh	idle	
Stop Convert T	Halts temperature conversion.	22h	idle	
Memory Commands				
Access Memory	Reads or writes to 256-byte EEPROM memory.	17h	<write data>	
Access Config	Reads or writes configuration data to configuration register.	Ach	<write data>	

3.2.5.2 SPI Accessed Features

The SPI bus provides information about the processor slots, the processors installed in those slots and A/D converters on the Profusion carrier. The SPI bus is accessed through the BMC. The following types of information are accessible via the SPI bus on the Profusion carrier:

- Error and status inputs, including processor ID bits, and control outputs.
- Nineteen-channel A/D converter for monitoring Profusion carrier voltages.

The SPI bus is composed of four separate serial chains to minimize the length of each chain, thus keeping the access latency short. The first chain provides access to processor stop control, the second chain provides error and status information, the third chain provides access to the A/D converter on the Profusion carrier, and the fourth chain provides access to more error and status information. Details of each chain are listed below.

Note that the “type” reference is identified with respect to the BMC.

The First SPI Chain Bit Map table shows the control outputs accessible via the first SPI serial chain:

Table 3-5: First SPI Chain Bit Map

Bit(s)	Signal Name	Type	Description
0	STOP1	Output	Disable processor 1.
1	STOP2	Output	Disable processor 2.
2	STOP3	Output	Disable processor 3.
3	STOP4	Output	Disable processor 4.
4	STOP5	Output	Disable processor 5.
5	STOP6	Output	Disable processor 6.
6	STOP7	Output	Disable processor 7.
7	STOP8	Output	Disable processor 8.
8	TM_0_WRITE	Output	Set/clear TM0 configuration bit in MAC
9	TM_1_WRITE	Output	Set/clear TM1 configuration bit in MAC
10	TM_2_WRITE	Output	Set/clear TM2 configuration bit in MAC
11	TM_3_WRITE	Output	Set/clear TM3 configuration bit in MAC
12	TM_4_WRITE	Output	Set/clear TM4 configuration bit in MAC
13	TM_5_WRITE	Output	Set/clear TM5 configuration bit in MAC
14	PIPELINE_WRITE	Output	Set/clear PIPELINE configuration pin on DIB
15	OVERRIDE_EN	Output	Enable the configuration data in bits 8:14 to be driven into the MAC and DIB.

The next section shows the error and status inputs accessible via the second SPI serial chain:

Table 3-6: Second SPI Chain Bit Map

Bit(s)	Signal Name	Type	Description
1	THERMTRIP1_L	error input	Thermal error on first processor.
2	IERR1_L	error input	Internal error in first processor.

Table 3-6: Second SPI Chain Bit Map

3	THERMTRIP2_L	error input	Thermal error on second processor.
4	IERR2_L	error input	Internal error in second processor.
5	CPU_RATIO3	status input	Core to bus frequency ratio bit 3.
6	CPU_RATIO2	status input	Core to bus frequency ratio bit 2.
7	CPU_RATIO1	status input	Core to bus frequency ratio bit 1.
8	CPU_RATIO0	status input	Core to bus frequency ratio bit 0.
9	THERMTRIP3_L	error input	Thermal error on third processor.
10	IERR3_L	error input	Internal error in third processor.
11	THERMTRIP4_L	error input	Thermal error on fourth processor.
12	IERR4_L	error input	Internal error in fourth processor.
13	S_MEMPRES_L	status input	Second memory carrier present.
14	MEMPRES_L	status input	Primary memory carrier present.
15	Reserved	spare	Always ‘1’.
16	Reserved	spare	Always ‘1’.
17	THERMTRIP5_L	error input	Thermal error on fifth processor.
18	IERR5_L	error input	Internal error in fifth processor.
19	THERMTRIP6_L	error input	Thermal error on sixth processor.
20	IERR6_L	error input	Internal error in sixth processor.
21	THERMTRIP7_L	error input	Thermal error on seventh processor.
22	IERR7_L	error input	Internal error in seventh processor.
23	THERMTRIP8_L	error input	Thermal error on eighth processor.
24	IERR8_L	error input	Internal error in eighth processor.
25	PRES_DET1	status input	CPU present in slot 1.
26	PRES_DET2	status input	CPU present in slot 2.
27	PRES_DET3	status input	CPU present in slot 3.
28	PRES_DET4	status input	CPU present in slot 4.
29	PRES_DET5	status input	CPU present in slot 5.
30	PRES_DET6	status input	CPU present in slot 6.

Table 3-6: Second SPI Chain Bit Map

31	PRES_DET7	status input	CPU present in slot 7.
32	PRES_DET8	status input	CPU present in slot 8.

The Profusion Carrier A/D Converter Channel Map table shows the A/D converter accessible via the third SPI serial chain:

Table 3-7: Profusion Carrier A/D Converter Channel Map*

Channel	Voltage	Description
0	VCCP1	Processor 1 core voltage.
1	VCCP2	Processor 2 core voltage.
2	VCCP3	Processor 3 core voltage.
3	VCCP4	Processor 4 core voltage.
4	VTT	Primary processor bus GTL+ termination voltage (1.5 V).
5	+2.5 V	+2.5 V supply voltage.
6	+3.3 V	+3.3 V supply voltage.
7	+5 V	+5 V supply voltage.
8	VCCP5	Processor 5 core voltage.
9	VCCP6	Processor 6 core voltage.
10	+12 V	+12 V supply voltage.
11	VCCP7	Processor 7 core voltage.
12	VCCP8	Processor 8 core voltage.
13	VCC_L2_12	Processor 1 and 2 cache voltage.
14	VCC_L2_34	Processor 3 and 4 cache voltage.
15	VCC_L2_56	Processor 5 and 6 cache voltage.
16	VCC_L2_78	Processor 7 and 8 cache voltage.
17	VTT	Secondary processor bus GTL+ termination voltage (1.5 V).
18	VTT	I/O bus GTL+ termination voltage (1.5 V).

The Fourth SPI Serial Chain Bit Map table shows the error and status signals accessible via the fourth SPI serial chain:

Table 3-8: Fourth SPI Serial Chain Bit Map

Bit(s)	Signal name	Type	Description
1	L2CONFLICT1_L	error input	L2 cache VIDs for processor pair 1-2 do not match.
2	L2CONFLICT2_L	error input	L2 cache VIDs for processor pair 3-4 do not match.
3	L2CONFLICT3_L	error input	L2 cache VIDs for processor pair 5-6 do not match.
4	L2CONFLICT4_L	error input	L2 cache VIDs for processor pair 7-8 do not match.
5	TM_0_READ	Status input	Read TM0 configuration data which was driven to MAC.
6	TM_1_READ	Status input	Read TM1 configuration data which was driven to MAC.
7	TM_2_READ	Status input	Read TM2 configuration data which was driven to MAC.
8	TM_3_READ	Status input	Read TM3 configuration data which was driven to MAC.
9	TM_4_READ	Status input	Read TM4 configuration data which was driven to MAC.
10	TM_5_READ	Status input	Read TM5 configuration data which was driven to MAC.
11	PIPELINE_READ	Status input	Read PIPELINE configuration data which was driven to DIB.
12	LST1_PRES_L	Status input	Primary coherency filter present
13	LST2_PRES_L	Status input	Secondary coherency filter present

The BMC uses the BMC_SPI_BUS to access the SPI serial chains on the Profusion carrier. Four select signals are decoded to select the four SPI serial chains.

The SELECT bits in the BMC_SPI_BUS (see I/O connector pinout) are defined as follows:

Table 3-9: Profusion Carrier SPI Serial Chain Select*

SPI(4:1)	SEL(2)	SEL(1)	SEL(0)	Description
0001	0	0	1	First Profusion* carrier serial chain (control).
0000	0	0	0	Second Profusion carrier serial chain (error and status).
0010	0	1	0	Third Profusion carrier serial chain (19-channel ADC).

Table 3-9: Profusion Carrier SPI Serial Chain Select (Continued)*

0011	0	1	1	Fourth Profusion carrier serial chain (error and status).
1xxx	X	X	X	Used on I/O carrier (refer to the *I/O Carrier* chapter for more details).

3.2.5.3 ISP Bus

A voltage management controller (VMC) and a reset GAL are connected to the ISP bus. These parts can be programmed through the ISP bus which is accessed from the BMC on the I/O carrier. The ISP bus is intended for access only during debug or field upgrade in order to reprogram programmable logic devices (PLDs) in the system.

3.2.6 Voltage Regulators

The Profusion carrier has two small linear regulators for the GTL+ termination voltage (1.5 V) required to terminate the processor buses and I/O bus. The primary voltage input for these regulators is the +3.3 V supply rail. A small +2.5 V linear regulator is also present for the 2.5 V logic on the Profusion carrier (MAC). This regulator converts off the +5 V supply rail.

3.2.6.1 VTT (1.5v) Converter

The following list shows the features of the onboard VTT voltage regulator.

- 3.3 V input voltage.
- 4.6 A maximum output current.
- 1.5 V nominal output voltage.
- 500,000h Mean Time Between Failures (MTBF).
- 50% efficiency at maximum load.
- Over voltage protection.
- Short circuit protection.
- No heat sink required.
- Margining supported.

This 1.5 V supply is used for the termination of all the GTL+ signals for the two processor front-side buses and the I/O bus. The termination voltage for the I/O bus on the other end is generated on the I/O carrier.

The GTL+ receiver reference voltage (VREF =2/3 of VTT) is also derived separately from each VTT. These VREFs are tied together among all regulators generating VTT for a common bus. However, VREF and VTT are kept separate between buses.

The margining is controlled by the following resistors.

Table 3-10: 1.5 V Termination Voltage Margining

Voltage	Resistor Value	Resistor Value	Resistor Value
VTT	R3M1=110 R8B1=22	R8B1 = 8.8	R3M1 = 69
VTT	R9M4=110 R2B1=22	R2B1=8.8	R9M4=69
Vtt	1.5 V	-10% (1.35 V)	+10% (1.65 V)

3.2.6.2 +2.5 V Regulator

The following list shows the features of the onboard 2.5 V linear regulator.

- 5 V input voltage.
- 2.9 A output current.
- ± 5% margining.

This 2.5 V regulator is used to supply the correct voltage for operation of the MAC component of the Profusion chip set.

The margining is controlled by the following resistors.

Table 3-11: +2.5 V Regulator Voltage Margining

Voltage	Resistor Value	Resistor Value	Resistor Value
+2.5 V	R7B1=R7A3=22	R7A3=19.6	R7B1 = 20
	+2.5 V	-5% (2.38 V)	+5% (2.62 V)

3.2.7 Board Configuration Jumpers

The J6A1 jumper block serves two functions:

Enables test/validation modes of operation (see the J6A1 Board Configuration Jumper Block (Oscillator, Server Management) table).

Determines core to bus ratio (see the J6A1 Board Configuration Jumper Block (Bus Ratio) table.

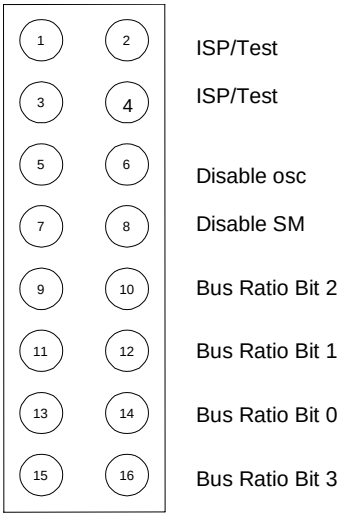


Figure 3-5: J6A1 Jumper Connector Pinout

Table 3-12: J6A1 Board Configuration Jumper Block (Oscillator, Server Management)

J6A1	OPEN	CLOSED
Pins 1-2	DEFAULT	Connects MVRM2 PLD program data out pin to boundary scan connector MVRM2 TDO pin (for in-system programming use only).
Pins 3-4	DEFAULT	Connects MVRM2 PLD program data in pin to boundary scan connector MVRM2 TDI pin (for in-system programming use only).
Pins 5-6	DEFAULT	Disables onboard clock oscillator. Clocks must be supplied by external test clock generator.
Pins 7-8	DEFAULT	Disables first SPI chain processor stop outputs.

Note that jumpers across the pins in the J6A1 Board Configuration Jumper Block (Oscillator, Server Management) table are for internal Intel validation only and in normal operation these jumpers would be open. The jumpers are not readable by and cannot be overwritten by SPI or I2C.

Jumpers across the pins of J6A1 as shown in the J6A1 Board Configuration Jumper Block (Bus Ratio) table determine the processor core to (front-side) bus frequency ratio. Currently defined ratios are shown in the J6A1 Board Configuration Jumper Block (Bus Ratio) table. Core frequen-

cies shown in the J6A1 Board Configuration Jumper Block (Bus Ratio) table are based on 100 MHz bus frequency. These jumpers are readable via SPI chain 2 bits 5:8 (corresponding to pins 15/16, 9/10, 11/12 and 13/14, respectively).

Table 3-13: J6A1 Board Configuration Jumper Block (Bus Ratio)

Jumper Configuration	Bus Ratio	Core Frequency (MHz)
J13-14	3:1	300
J9-10, J13-14	7:2	350
J11-12	4:1	400
J9-10, J11-12	9:2	450
J11-12, J13-14	5:1	500
J9-10, J11-12, J13-14	11:2	550
J15-16	6:1	600
J9-10, J15-16	13:2	650
J13-14, J15-16	7:1	700
J9-10, J13-14, J15-16	15:2	750
(no jumpers)	Reserved	
J9-10	Reserved	
J11-12, J15-16	Reserved	
J9-10, J11-12, J15-16	Reserved	
J11-12, J13-14, J15-16	Reserved	
J9-10, J11-12, J13-14, J15-16	Reserved	

3.3 Signal Descriptions

This section defines the function of signal pins on the Profusion carrier connector interfaces. The signal mnemonics defined here may appear in descriptive text throughout this chapter. An “_L” following the signal name indicates that the signal is active-low (note that this is the same convention used on schematics for active-low signals). A colon between numbers in parenthesis indicates a range of signals (e.g., A(13:0)). Refer to Section Mechanical Specifications for exact connector pinouts.

In most of the signal description tables, a signal type is presented for each of the signal names. This is used to describe the signaling technology, voltage, or otherwise of the given signal. The electrical types are as follows:

Table 3-14: Electrical Signal Types

Type	Description
GTL+	Signal uses GTL+ signaling scheme.
LVTTL	Signal uses low voltage TTL compatible signaling scheme (Vil max=0.8 V, Vih min=2.0 V, Voh max = 3.6 V).
TTL	Signal uses TTL compatible signaling scheme (Vil max=0.8 V, Vih min=2.0 V, Voh max = 5.5 V).
2.5 V	Signal uses ultra low voltage signaling scheme (Vil max = 0.8 V, Vih min = 1.7 V, Voh max = 3.0 V).
in	Input is a standard input-only signal from the Profusion* carrier viewpoint.
Out	Totem pole output is a standard active driver from the Profusion carrier viewpoint.
t/s	Tri-state is a bi-directional, tri-state input/output pin.
s/t/s	Sustained tri-state is an active low tri-state signal owned and driven by one and only one agent at a time, subject to specific timing restrictions.
o/d	Open drain allows multiple devices to share signals as a wired-OR.
PWR	Voltage supplies and sense lines.

3.3.1 Memory Interface Signals

Most of the memory control signals appearing on the grand connector are driven by the MAC chip, which supports SDRAM DIMMs. The DIB chip drives most of the memory data signals. Refer to the chip set documentation for complete signal descriptions. The chip set provides two copies of all signals: one for the primary memory carrier and one for the secondary memory carrier.

The following tables define the signals according to these functional groups: Address/Control, System Management and Scan Signals. The connector specification is extensible to future versions of the memory carrier.

Table 3-15: Memory Carrier Address/Control Signals

Signal(s)	Type	Name and Description
LBA[1:0], RBA[1:0]	LVTTL output	Multiplexed row and column bank address bits. The two address lines support two or four banks of memory per SDRAM device.
LMA[12:0], RMA[12:0]	LVTTL output	Multiplexed row and column address bits. The bank address and 13 address lines are sufficient to support 64Mx4 SDRAMs with asymmetric addressing.
LMCS_L [7:0], RMCS_L [7:0]	LVTTL output	Memory chip selects. Each chip select is connected to four DIMMs of SDRAMs. Only one each of the RAS_L [3:0] and CAS_L [3:0] signals is active to further qualify which DIMM is selected. This two-dimensional decode supports 32 DIMMs on each memory port.
LMRAS_L [3:0], RMRAS_L [3:0]	LVTTL output	Row address strobes. These active-low signals strobe in the bank and row address issued on the BA[1:0] and MA[12:0] signals. There is one RAS_L signal for each group of eight DIMMs. The MCS_L [7:0] signals further qualify which of the eight DIMMs is selected.
LMCAS_L [3:0], RMCAS_L[3:0]	LVTTL output	Column address strobes. These active-low signals strobe in the bank and column address issued on the BA[1:0] and MA[12:0] signals. There is one CAS_L signal for each group of eight DIMMs. The MCS_L [7:0] signals further qualify which of the eight DIMMs is selected.
LMWE_L [3:0], RMWE_L [3:0]	LVTTL output	Write enable signals. These active-low signals specify whether the current operation is a write or a read from the SDRAM. There is one MWE_L signal for each group of eight DIMMs. The MCS_L [7:0] signals further qualify which of the eight DIMMs is written.
LMD_L[63:0], LMDEP_L[7:0], RMD_L[63:0], RMDEP_L[7:0]	LVTTL bidirectional	Memory data bits. Each set of 72 data signals moves data to/from an SDRAM array. Sixty-four signals are used for the actual data and the other eight signals carry ECC information.
PWRGDB	LVTTL out	Buffered Power Good. A buffered version of the PWRGD signal, provided by the VMC to all other components in the Profusion* PCIset.
YUKONCLK	LVTTL out	Host Clock In. This is the buffered version of the host clock.

The Memory Carrier System Management Signals table is a summary of system management signal pins, including the signal mnemonic, name, and brief description.

Table 3-16: Memory Carrier System Management Signals

Signal(s)	Type	Name and Description
I2C_SCL	TTL out	I^2C Clock. Clock reference for the I^2C interface. Three buses per memory carrier (1) I2C_BMC bus accesses FRU EEPROM and temp. sensor; (2) MEMA bus accesses first 8 DIMM slot serial presence detect (SPD) EEPROMs; (3) MEMB bus accesses second 8 DIMM slot SPD EEPROMs.
I2C_SDA	TTL o/d	I^2C Data. Serial data transfer for the I^2C interface. Three buses per memory carrier as detailed above.

The Memory Carrier SCAN Signals table is a summary of SCAN signal pins, including the signal mnemonic, name, and brief description. All SCAN signals are controlled from the system JTAG connector, J3A1.

Table 3-17: Memory Carrier SCAN Signals

Signal(s)	Type	Name and Description
TCK	LVTTL out	Test Clock. Test clock is used to clock state information and data into and out of the board during system boundary scan.
TDI	o/d out	Test Data Input. Test input is used to serially shift data and instructions into the board.
TDO	LVTTL in	Test Output. Test output is used to shift data out of the board.
TMS	LVTTL out	Test Mode Select. Test mode select is used to control the state of the TAP controller.
TRST_L	LVTTL out	Test Reset. Test reset is used to reset the TAP controller logic. For normal operation, TRST_L is held low.

3.3.2 I/O Connector Signals

Most of the I/O control signals appearing on the grand connector are driven by the MAC chip while most of the data signals are driven by the DIB chip. Refer to the chip set documentation for complete signal descriptions.

The following tables define the signals according to these functional groups: I/O Bus, Resets, Clocks, System Management, Miscellaneous, and Power Signals. The I/O bus on the Profusion carrier connects to four separate PB64 components on the I/O carrier.

Table 3-18: I/O Connector I/O Bus Signals

Signal(s)	Type		Name and Description
IO_BPRI_L	GTL+	I	Priority Agent Bus Request is issued by the high-priority bus agent to acquire the request bus. The high-priority agent is always the next bus owner. (This is an input on the I/O bus.)
IO_BNR_L	GTL+	I/O	Block Next Request blocks the current request bus owner from issuing new requests.
IO_LOCK_L	GTL+	I/O	Lock is asserted for an indivisible sequence of transactions.
IO_ADS_L	GTL+	I/O	Address Strobe indicates that the current cycle is the first of two cycles of a request.
IO_REQ_L[4:0]	GTL+	I/O	Request. In the first cycle of a request, these signals carry the request type. In the second cycle, they carry the data size and transfer length.
IO_RP_L	GTL+	I/O	Request Parity is the parity computed over IO_ADS_L and IO_REQ_L[3:0].
IO_A_L[35:3]	GTL+	I/O	Address signals are the upper address bits issued with the current request.
IO_AP_L[1,0]	GTL+	I/O	Address Parity is the parity computed over the address; IO_AP_L[1] covers IO_A_L[35:24], and IO_AP_L[0] covers IO_A_L[23:3].
IO_AERR_L	GTL+	I/O	Address Parity Check is asserted when either an address or request parity error occurs.
IO_HIT_L	GTL+	I/O	Hit indicates that a caching agent holds an unmodified version of the requested line. Hit is also driven in conjunction with IO_HITM_L to extend the snoop window.
IO_HITM_L	GTL+	I/O	Hit Modified indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Hit Modified is also driven in conjunction with IO_HIT_L to extend the snoop window.
IO_DEFER_L	GTL+	I/O	IO_DEFER_L is driven by the addressed agent to indicate that bus completion cannot be guaranteed for the transaction.
IO_RS_L[2:0]	GTL+	I/O	Response indicates the type of response.
IO_RSP_L	GTL+	I/O	Response Parity is parity computed over IO_RS_L[2:0].
IO_TRDY_L	GTL+	I/O	Target Ready indicates a valid response cycle.
IO_D_L[63:0]	GTL+	I/O	Data signals
IO_DEP_L[7:0]	GTL+	I/O	Data Parity; one parity bit per byte.
IO_DBSY_L	GTL+	I/O	Data Bus Busy is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
IO_BINIT_L	GTL+	I/O	Bus Initialization.
IO_BERR_L	GTL+	I/O	Bus Error indicates an unrecoverable data error.

Table 3-18: I/O Connector I/O Bus Signals (Continued)

IO_RESET_L	GTL+	I	Reset. (This signal is an input on the I/O bus.)

The I/O Connector Clock and Reset Signals table is a summary of clock and reset signal pins, including the signal mnemonic, name, and brief description.

Table 3-19: I/O Connector Clock and Reset Signals

Signal(s)	Type	Name and Description
PB64_[A:D]_CLK	LVTTL out	Clocks to PCI host bridges; one load per clock signal.
CRESET_L	LVTTL in	Configuration mux reset; trails IO_RESET_L by at least four clocks; used to switch configuration data mux to processors.
IO_PWRGD	TTL in	System hard reset from SMIC
PWRGDB	LVTTL out	IO_PWRGD conditioned by Profusion* carrier.
PWR_GOOD	TTL in	Power good from power supplies.
TOGGLE_OSC	TTL in	Resets local oscillators to ADC and VMC.
P6_CLK_GOOD	LVTTL_in	Delayed version of PWRGDB used to initialize the PLLs in the chip set.

The I/O Connector System Management Signals table is a summary of system management signal pins, including the signal mnemonic, name, and brief description.

Table 3-20: I/O Connector System Management Signals

Signal(s)	Type	Name and Description
I2C_BMC_SCL	LVTTL in	BMC private I^2C Clock. Clock reference for the I^2C interface. Pulled up to +3.3 V.
I2C_BMC_SDA	LVTTL o/d	BMC private I^2C Data. Serial data transfer for the I^2C interface. Pulled up to +3.3 V.
I2C_FPC_SCL	TTL in	Front Panel Controller (FPC) private I^2C Clock. Clock reference for the I^2C interface. Pulled up to +5 V.
I2C_FPC_SDA	TTL o/d	FPC private I^2C Data. Serial data transfer for the I^2C interface. Pulled up to +5 V.

Table 3-20: I/O Connector System Management Signals (Continued)

I2C_BACKUP_SCL	TTL in	Private I^2C Clock for an I^2C bus powered by 5VSTNDBY. Pulled up to 5 V STNDBY.
I2C_BACKUP_SDA	TTL o/d	Private I^2C Data for an I^2C bus powered by 5VSTNDBY. Pulled up to 5 V STNDBY.
I2C_DS2P[1:0]_SCL	LVTTL in	Private I^2C Clock for an I^2C bus to the processors. One bus per processor mezzanine board. Pulled up to 3.3 V.
I2C_DS2P[1:0]_SDA	LVTTL o/d	Private I^2C Data for an I^2C bus to the processors. One bus per processor mezzanine board. Pulled up to 3.3 V.
BMC_SPI_BUS(6)	TTL in	SPI MOSI (data in).
BMC_SPI_BUS(5)	TTL out	SPI MISO (data out).
BMC_SPI_BUS(4)	TTL in	SPI SEL3.
BMC_SPI_BUS(3)	TTL in	SPI SEL2.
BMC_SPI_BUS(2)	TTL in	SPI SEL1.
BMC_SPI_BUS(1)	TTL in	SPI SEL0.
BMC_SPI_BUS(0)	TTL in	SPI CLK.
CPU_SPI_RESET_L	TTL in	System management logic reset.
PIIX_SMB_SCL	LVTTL in	PIIX4 SMB clock. Clock reference for the SPD EEPROMs. Pulled up to +3.3 V.
PIIX_SMB_SDA	LVTTL o/d	PIIX4 SMB data. Switched among four banks of SPD EEPROMs on memory carrier. Pulled up to +3.3 V
PIIX_SMB_SEL[1:0]	LVTTL in	PIIX4 SMB select. Controls to which bank of SPD EEPROMs the PIIX_SMB_CLK and PIIX_SMB_SDA are connected.

The I/O Connector Legacy Signals table is a summary of legacy signal pins, including the signal mnemonic, name, and brief description.

Table 3-21: I/O Connector Legacy Signals

Signal(s)	Type	Name and Description
INTR	LVTTL in	Interrupt.
NMI	TTL in	Nonmaskable Interrupt.
A20M_L	LVTTL in	A20 Mask.
IGNNE_L	LVTTL in	Ignore Numerical Error.

Table 3-21: I/O Connector Legacy Signals (Continued)

INIT_L	LVTTL in	Processor Soft Error Request.
SMI_L	LVTTL in	System Management Interrupt.
FERR_L	TTL out	Floating Point Error.

The I/O Connector Miscellaneous Signals table is a summary of miscellaneous signal pins, including the signal mnemonic, name, and brief description.

Table 3-22: I/O Connector Miscellaneous Signals

Signal(s)	Type	Name and Description
PIC_CLK	LVTTL out	APIC clock. Runs at HCLK/4 (25 MHz).
PICD(1:0)	2.5V o/d	APIC data. Pulled up with 100 ohm to 2.5 V on I/O carrier.
SBCERR_L	LVTTL out	MAC interrupt request.
ISP_SDI	TTL in	In-System Programming Data In.
ISP_SDO	TTL out	In-System Programming Data Out.
ISP_EN_L	TTL in	In-System Programming Enable.
ISP_MODE	TTL in	In-System Programming Mode.
ISP_SCLK	TTL in	In-System Programming Clock.
CPU_SLP_L	TTL in	Puts processors in Sleep state (not connected on Profusion* carrier).
STOP_CLK_L	TTL in	Puts processors in Stop Grant state.
B-GTLREF	GTL+	GTL+ reference voltage to all chips in the chip set.

The I/O Connector SCAN Signals table is a summary of SCAN signal pins, including the signal mnemonic, name, and brief description.

Table 3-23: I/O Connector SCAN Signals

Signal(s)	Type	Name and Description
IO_TCK{5:0]	LVTTL out	Test Clock. Test clock is used to clock state information and data into and out of the I/O carrier during boundary scan. Six copies for point-to-point routing.

Table 3-23: I/O Connector SCAN Signals (Continued)

IO_TDI	o/d out	Test Data Input. Test input is used to serially shift data and instructions into the board.
IO_TDO	LVTTL in	Test Output. Test output is used to shift data out of the board.
IO_TMS	LVTTL out	Test Mode Select. Test mode select is used to control the state of the TAP controller.
IO_TRST_L	LVTTL out	Test Reset. Test reset is used to reset the TAP controller logic. For normal operation, TRST_L must be asserted low after PWRGD is asserted.

The I/O Connector Power Pins table is a summary of power pins, including the signal mnemonic, name, and brief description.

Table 3-24: I/O Connector Power Pins

Signals(s)	Type	Name and Description
GND	PWR	Ground. Power supply ground.
+3.3V	PWR	3.3 V power supply.
+5V	PWR	5 V power supply.
+12V	PWR	Positive 12 V power supply.
5VSTNDBY	PWR	5 V standby power, always active as long as AC present at input to system.
N12V	PWR	Negative 12 V power supply.
12VSENSE	PWR	12 V power supply remote sense

3.3.3 Front Panel Interface Signals

The Front Panel Connector table is a summary of power pins, including the signal mnemonic, name, and brief description.

Table 3-25: Front Panel Connector

Signal(s)	Description
COM2_TO_FP_EN	**COM2 Front Panel Redirect**. Connects the COM2 transceiver to the front panel for front panel redirection.
COM2_TO_SIO_EN_A	**COM2 Super I/O Redirect**. Connects the COM2 transceiver to the I/O carrier's Super I/O* chip and the XIMB transceiver to the front panel.
FAN_FAILED_L	**Fan Failure**. Signal from the power distribution board indicating a fan failure.
FP_NMI_SWT_L	**System-NMI Switch**. This is debounced by the BMC.
FP_TO_PIIX_PWRBTN	**Front Panel Power Button**. This pin is driven to the I/O carrier to indicate that the power button was pressed on the front panel.
HARD_RESET	**Hard Reset**. Overall system reset from the front panel asserted >500 ms. De-assert >=0 ms.
I2C_BACKUP_SCL	**Backup I^2C Bus Clock**. This bus operates under standby voltage and allows the front panel access to the CEL on the I/O carrier.
I2C_BACKUP_SDA	**Backup I^2C Bus Data**. This bus operates under standby voltage and allows the front panel access to the CEL on the I/O carrier.
I2C_CEL_CONNECT_BMC_A	**CEL to BMC Connect**. Connects CEL serial EEPROM to the I/O carrier's BMC.
I2C_CEL_CONNECT_FPC	**CEL to FPC Connect**. Connects CEL serial EEPROM to the FPC.
I2C_FPC_SCL	**Front Panel Private I^2C Bus Clock**.
I2C_FPC_SDA	**Front Panel Private I^2C Bus Data**.
INTRUSION_L	**Intrusion**. Indicates disk door has been opened. From SCSI hot-swap back-plane.
NMI_5V	**Nonmaskable Interrupt**. Driven to CPU.
PROC_RESET_L	**Processor Reset Status**. This signal indicates that the processor is actively being held in reset state.
PWR_CNTRL_RTC_L	**RTC Power Control**. Power control signal from Super I/O. High time >5 ms. Low time 5 ms.
PWR_CNTRL_SFC_L	**SFC Power Control**. Power control signal from the Server Monitor Module. High time >=5 ms. Low 5-100 ms.
RI_TTL_FP	**COM2 redirection signal**. This signal remains active at the front panel connector even when COM2 has been connected to the I/O carrier's Super I/O chip.
SECURE_MODE_BMC	**BMC Secure Mode**. Signal from the I/O carrier indicating a system-secure state.
SIN_TTL_COM2	**COM2 redirection signal**. This signal remains active at the front panel connector even when COM2 has been connected to the I/O carrier's Super I/O chip.
SIN_TTL_XIMB	**ICMB receive**.
SMI_L	**System Management Interrupt**.

Table 3-25: Front Panel Connector (Continued)

SOUT_TTL_COM2	**COM2 redirection signal**.
SOUT_TTL_XIMB	**ICMB transmit**.
SPEAKER_DATA	**Speaker**. An amplified version of this signal drives the front panel's speaker.
XIMB_SOUT_EN	**Open collector signal.** Output enables the ICMB transceivers TXD RS485 output.

3.3.4 JTAG Scan Interface Signals

The following diagram shows the JTAG scan chain for the Profusion carrier and how it is connected to the processor slots, memory carriers, and I/O carrier.

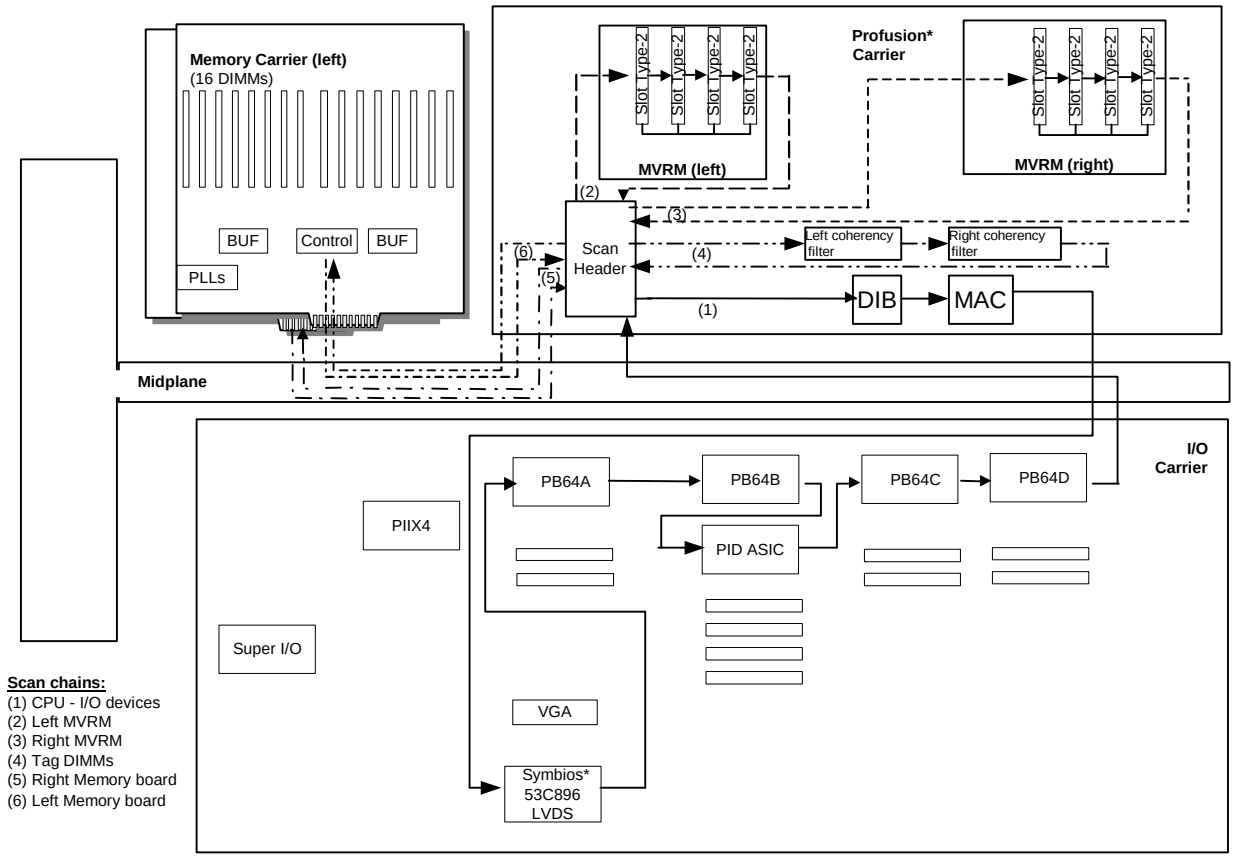


Figure 3-6: Profusion Carrier Scan Chains*

The maximum operating frequency for the primary OPRF100 board set scan chain is 1 MHz. Note that the JTAG signals are open-drain signals pulled up to 3.3 V, except on the processor mezzanine boards and CPU-I/O devices where they are pulled up to 2.5 V.

When a JTAG boundary scan controller is plugged into the system JTAG connector, six separate JTAG data chains are accessible. The JTAG data chains provide boundary scan access to the LSI components that make up an OPRF100 system assembly. It is possible that one of the processor mezzanine boards and/or one of the memory carriers is not installed, or that one or both of the coherency filter tag DIMMs are not installed. Hardware on the scan controller board should be configurable in such a way that the data chain is maintained regardless of whether these boards are installed or not. It is possible to interconnect the six chains into one or more chains depending on installed components and length of test vectors desired. Processor slots without processors will maintain the integrity of the chain as long as A450NX processor termination modules are installed in these slots.

3.3.5 Coherency DIMM Interface Signals

The Coherency Filter Tag SRAM DIMM Connector Pinout table gives the pinout of the 72-pin coherency filter tag SRAM DIMM connector. This connector is a Berg* SO-DIMM connector. Each pin on these connectors can carry 0.3 amps of current, and the pinout provides the following number of power, ground, and reserved pins.

- +3.3 Vdc - 8 pins.
- Ground - 13 pins.
- Reserved - 0 pins.

Table 3-26: Coherency Filter Tag SRAM DIMM Connector Pinout

Pin	Signal Name	Function	Pin	Signal Name	Function
1	vcc3	3.3 V power	2	vcc3	3.3 V power
3	vcc3	3.3 V power	4	vcc3	3.3 V power
5	a[17]	Address bus bit 17 input	6	a[16]	Address bus bit 16 input
7	a[15]	Address bus bit 15 input	8	a[14]	Address bus bit 14 input
9	a[13]	Address bus bit 13 input	10	a[12]	Address bus bit 12 input
11	a[11]	Address bus bit 11 input	12	a[10]	Address bus bit 10 input
13	a[9]	Address bus bit 9 input	14	a[8]	Address bus bit 8 input
15	gnd	Ground	16	gnd	Ground
17	d[17]	Data bus bit 17	18	d[16]	Data bus bit 16
19	d[15]	Data bus bit 15	20	d[14]	Data bus bit 14
21	ce[0]#	Chip enable #0 input	22	ce[2]#	Chip enable #2 input
23	d[13]	Data bus bit 13	24	d[12]	Data bus bit 12
25	d[11]	Data bus bit 11	26	d[10]	Data bus bit 10

Table 3-26: Coherency Filter Tag SRAM DIMM Connector Pinout (Continued)

27	d[9]	Data bus bit 9	28	d[8]	Data bus bit 8
29	gnd	Ground	30	gnd	Ground
31	CLK[0]	Clock line 0	32	CLK[1]	Clock line 1
33	gnd	Ground	34	gnd	Ground
35	d[7]	Data bus bit 7	36	d[6]	Data bus bit 6
37	d[5]	Data bus bit 5	38	d[4]	Data bus bit 4
39	d[3]	Data bus bit 3	40	d[2]	Data bus bit 2
41	d[1]	Data bus bit 1	42	d[0]	Data bus bit 0
43	gnd	Ground	44	GND	Ground
45	a[7]	Address bus bit 7 input	46	a[6]	Address bus bit 6 input
47	a[5]	Address bus bit 5 input	48	a[4]	Address bus bit 4 input
49	a[3]	Address bus bit 3 input	50	a[2]	Address bus bit 2 input
51	a[1]	Address bus bit 1 input	52	a[0]	Address bus bit 0 input
53	gnd	Ground	54	gnd	Ground
55	ce[1]#	Chip enable #1 input	56	ce[3]#	Chip enable #3 input
57	gnd	Ground	58	gnd	Ground
59	SCL	I^2C* clock line	60	sda	I^2C data line
61	sa[0]	I^2C address line bit 0	62	inst#	DIMM Installed
63	tdi	JTAG Test Data In	64	we#	Write enable input
65	tms	JTAG Test Mode Select	66	tDO	JTAG Test Data Out
67	VSTBY	3.3 V power [1]	68	TCK	JTAG Test Clock
69	vcc3	3.3 V power	70	vcc3	3.3 V power
71	vcc3	3.3 V power	72	vcc3	3.3 V power

NOTES:

1. Pin 67 on the tag DIMM connector is connected to 3.3 V on the Profusion carrier but connected to an isolated power trace (VSTBY) on the DIMM. VSTBY is connected to the I^2C serial EEPROM's Vcc pin, which allows applications to power the EEPROM from standby power. Powering the I^2C EEPROM from standby voltage is not required on the Profusion carrier.

3.4 Mechanical Specifications

This section specifies the physical characteristics for the Profusion carrier. This is a board-level specification only.

3.4.1 Connector Specifications

The Baseboard Connector Specifications table shows reference designators, quantity, manufacturer, and part number for connectors on the baseboard. Item numbers reference the circled numbers on the baseboard mechanical drawing. Refer to manufacturer's documentation for more information.

Table 3-27: Baseboard Connector Specifications

Item	Ref. Designator(s)	Qty.	Mfr. And Part #	Description
1	J1J1	1	MOLEX* 73670-0115	Grand connector 1008 signal pins + 12 power blades + 2 guide pins.
2	J3C1/J3F1/J3H1/ J7C1/ J7F1/J7H1	6	MOLEX 73780-3143	Mezzanine connector.
3	J8A1	1	AMP* 2-557101-1	Front panel connector.
4	J3A1	1	AMP 650181-2	JTAG connector.
6	J6A1	1	AMP 104351-8	Configuration header.
7	J5C1/J5C2	2	Berg* 93764-418722	Coherency filter sockets.

3.4.1.1 Grand Connector Pinout

The grand connector uses a high density metric (HDM) pin-and-socket connector for interfacing with the memory carriers and the I/O carrier. This connector consists of two signal modules with 72 pins apiece, six signal modules with 144 pins apiece, and four power modules with 12 pins (four per contact) each. To achieve a 3:2 signal/ground ratio, two-fifths of the pins on the signal module are connected to ground. The next two subsections give the pinouts for both the memory carriers and the I/O carrier. A 1:1 signal/ground ratio for all high-speed signals is maintained while lower speed signals use a 2:1 signal/ground ratio. The next two subsections give the pinouts for both the power modules and the signal modules.

3.4.1.1.1 Memory Bus Connector Signals (within the Grand Connector)

Each signal pin is rated at 1A. Each memory carrier uses two 144-pin sections. One section is given in the Profusion Carrier Memory Signal Connector Pinout table.

Table 3-28: Profusion Carrier Memory Signal Connector Pinout*

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
PWR_GD	F24	GND	B21	SPARECLK0	D21	GND	E21	TDI	C21
GND	F22	GND	B22	GND	D22	GND	A22	GND	B23
GND	E23	BMC_SCL	F21	TCK	C22	BMC_SDA	C23	TMS	C25
TDO	D24	DIMM0_SDA	A26	GND	D26	GND	D22	CAS_L(1)	A23
RAS_L(0)	F23	CAS_L(0)	C24	RAS_L(1)	D23	DIMM0_SCL	A21	CS_L(2)	A25
WE_L(1)	F25	GND	E25	CS_L(1)	D25	WE_L(0)	A24	GND	B26
CS_L(3)	F27	CS_L(0)	F26	GND	E26	GND	B25	D(3)	A27
GND	E28	GND	E27	D(1)	D27	D(0)	C26	D(8)	A29
D(4)	F29	D(2)	C28	GND	B28	GND	B27	GND	B30
D(9)	F31	GND	E29	D(6)	D29	D(5)	A28	D(13)	A31
GND	E32	D(7)	F30	GND	E30	GND	B29	CB(2)	A33
D(14)	F33	GND	E31	D(11)	C31	D(10)	C30	GND	B34
CB(3)	F35	D(12)	D32	GND	B32	GND	B31	D(19)	A35
GND	E36	GND	E33	CB(0)	D33	D(15)	A32	D(24)	A37
D(20)	F37	CB(1)	F34	GND	E34	GND	B33	GND	B38
GND	E38	GND	E35	D(17)	D35	D(16)	C34	D(29)	A39
D(25)	F39	D(18)	D36	GND	B36	GND	B35	GND	B40
D(30)	F41	GND	E37	D(22)	C37	D(21)	A36	A(1)	A41
GND	E42	D(23)	D38	D(27)	D39	GND	B37	BA(0)	A44
A(4)	F43	GND	E39	GND	E40	D(26)	C38	A(6)	A46
BA(1)	F44	D(28)	F40	A(0)	D41	GND	B39	A(11)	A49
A(7)	F46	GND	E41	GND	B42	D(31)	C40	D(36)	A51
A(8)	F47	A(2)	A42	A(5)	D43	GND	B41	GND	B52
GND	E48	GND	E43	GND	D44	A(3)	C42	D(41)	A53
A(13)	F49	GND	E44	CLK	D45	GND	B43	GND	B54
GND	E50	GND	E45	GND	D46	GND	B44	D(46)	A55
D(35)	F51	GND	E46	A(10)	D47	GND	B45	CB(7)	A57
D(40)	F53	GND	E47	GND	B48	GND	B46	GND	B58
D(45)	F55	A(12)	D48	D(32)	C49	GND	B47	D(52)	A59
GND	E56	GND	E49	GND	B50	A(9)	A48	D(57)	A61
CB(6)	F57	D(34)	D50	D(37)	C51	GND	B49	GND	B62
D(51)	F59	GND	E51	GND	E52	D(33)	A50	D(62)	A63

Table 3-28: Profusion Carrier Memory Signal Connector Pinout (Continued)*

GND	E60	D(39)	F52	D(42)	D53	GND	B51	CS_L(7)	A65
D(56)	F61	GND	E53	GND	E54	D(38)	C52	BD_ID	A66
D(61)	F63	D(44)	F54	D(47)	C55	GND	B53	WE_L(3)	A67
GND	E64	GND	E55	GND	B56	D(43)	C54	DIMM1_SDA	A68
CS_L(6)	F65	CB(5)	D56	D(48)	C57	GND	B55		
RAS_L(2)	F67	GND	E57	GND	E58	CB(4)	A56		
PRES_DET_L	F68	D(50)	F58	D(53)	C59	GND	B57		
DIMM1_SCL	C68	GND	E59	GND	B60	D(49)	D58		
		D(55)	D60	D(58)	C61	GND	B59		
		GND	E61	GND	E62	D(54)	A60		
		D(60)	F62	D(63)	D63	GND	B61		
		GND	E63	GND	B64	D(59)	C62		
		CS_L(5)	C64	CAS_L(3)	D65	GND	B63		
		GND	E65	GND	E66	CS_L(4)	A64		
		RAS_L(3)	F66	WE_L(2)	D67	GND	B65		
		GND	E67	TM(4)	D68	CAS_L(2)	C66		
		GND	E68			GND	B67		
						GND	B68		

3.4.1.1.2 I/O Connector Signals (within the Grand Connector)

Table 3-29: Profusion Carrier I/O Signal Connector Pinout*

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
C5	PB64_D_CLK	B1	+12V	A5	NO CON-NECT	D1	+5V	E5	GROUND	F1	+12V
C7	PB64_C_CLK	B2	+12V	A6	NO CON-NECT	D2	+5V	E6	GROUND	F2	+12V
C9	PB64_B_CLK	B3	+12V	A7	NO CON-NECT	D3	+5V	E7	GROUND	F3	+12V
C11	PB64_A_CLK	B4	+12V	A8	NO CON-NECT	D4	+5V	E8	GROUND	F4	+12V

Table 3-29: Profusion Carrier I/O Signal Connector Pinout (Continued)*

A9	NO CONNECT	B5	GROUND	C6	GROUND	D5	GROUND	E9	GROUND	F5	NO CONNECT
A10	NO CONNECT	B6	GROUND	C8	GROUND	D6	ITP_BCLK	E10	GROUND	F6	GROUND
A11	NO CONNECT	B7	GROUND	C10	GROUND	D7	GROUND	E11	GROUND	F7	TCK3
A12	NO CONNECT	B8	GROUND	C12	GROUND	D8	TCK4	E12	GROUND	F8	GROUND
A13	P6_CLK_GOOD	B9	GROUND	C13	-12V	D9	GROUND	E13	GROUND	F9	TCK5
A14	-12V	B10	GROUND	C14	-12V	D10	TCK6	E14	GROUND	F10	GROUND
A15	-12V	B11	GROUND	C15	NO CONNECT	D11	GROUND	E15	GROUND	F11	NO CONNECT
A16	NO CONNECT	B12	GROUND	C16	ISP_SDO	D12	TCK7	E16	GROUND	F12	PG4_D_GTL_VREF
A69	NO CONNECT	B13	GROUND	C69	NO CONNECT	D13	PG4_D_GTL_VREF	E69	GROUND	F13	PG4_D_GTL_VREF
A70	NO CONNECT	B14	GROUND	C70	NO CONNECT	D14	PG4_D_GTL_VREF	E70	GROUND	F14	NO CONNECT
A71	NO CONNECT	B15	GROUND	C71	IO_RESET_L	D15	NO CONNECT	E71	GROUND	F15	NO CONNECT
A72	NO CONNECT	B16	GROUND	C72	IO_BERR_L	D16	NO CONNECT	E72	GROUND	F16	NO CONNECT
A73	NO CONNECT	B17	+12V	C73	IO_RS1_L	D17	+5V	E73	GROUND	F17	+3.3V
A74	NO CONNECT	B18	+12V	C74	IO_REQ3_L	D18	+5V	E74	GROUND	F18	+3.3V
A75	IO_RS0_L	B19	+12V	C75	IO_REQ0_L	D19	+5V	E75	GROUND	F19	+3.3V
A76	IO_REQ2_L	B20	+12V	C76	IO_BPRI_L	D20	+5V	E76	GROUND	F20	+3.3V
A77	IO_HIT_L	B69	GROUND	C77	IO_DEFER_L	D69	PWR_GOOD	E77	GROUND	F69	IO_PWRGD
A78	IO_AP1_L	B70	GROUND	C78	IO_ADS_L	D70	PWRGDB	E78	GROUND	F70	NO CONNECT
A79	IO_A(35)	B71	GROUND	C79	IO_A(29)	D71	IO_BINIT_L	E79	GROUND	F71	IO_RSP_L
A80	IO_AP0_L	B72	GROUND	C80	IO_A(24)	D72	IO_TRDY_L	E80	GROUND	F72	IO_RS2_L
A81	IO_A(20)	B73	GROUND	C81	IO_A(17)	D73	IO_DRDY_L	E81	GROUND	F73	IO_AERR_L
A82	IO_A(23)	B74	GROUND	C82	IO_A(21)	D74	IO_REQ4_L	E82	GROUND	F74	IO_REQ1_L
A83	NO CONNECT	B75	GROUND	C83	IO_A(14)	D75	IO_LOCK_L	E83	GROUND	F75	IO_HITM_L
A84	NO CONNECT	B76	GROUND	C84	IO_A(5)	D76	IO_RP_L	E84	GROUND	F76	IO_DBSY_L

Table 3-29: Profusion Carrier I/O Signal Connector Pinout (Continued)*

A85	IO_A(7)	B77	GROUND	C85	IO_A(12)	D77	IO_BNR_L	E85	GROUND	F77	IO_A(34)
A86	NO CONNECT	B78	GROUND	C86	NO CON-NECT	D78	IO_A(33)	E86	GROUND	F78	IO_A(32)
A87	NO CONNECT	B79	GROUND	C87	IO_A(6)	D79	IO_A(31)	E87	GROUND	F79	IO_A(30)
A88	NO CONNECT	B80	GROUND	C88	NO CON-NECT	D80	IO_A(28)	E88	GROUND	F80	IO_A(27)
A89	12V SENSE	B81	GROUND	C89	IO_D(60)	D81	IO_A(26)	E89	GROUND	F81	IO_A(25)
A90	IO_D(56)	B82	GROUND	C90	IO_D(61)	D82	IO_A(22)	E90	GROUND	F82	IO_A(19)
A91	NO CONNECT	B83	GROUND	C91	IO_D(50)	D83	IO_A(18)	E91	GROUND	F83	IO_A(16)
A92	NO CONNECT	B84	GROUND	C92	IO_D(43)	D84	IO_A(15)	E92	GROUND	F84	IO_A(13)
A93	IO_D(45)	B85	GROUND	C93	IO_D(52)	D85	IO_A(10)	E93	GROUND	F85	IO_A(11)
A94	IO_D(39)	B86	GROUND	C94	IO_D(49)	D86	IO_A(8)	E94	GROUND	F86	IO_A(9)
A95	IO_D(31)	B87	GROUND	C95	IO_D(37)	D87	IO_A(3)	E95	GROUND	F87	IO_A(4)
A96	IO_D(33)	B88	GROUND	C96	IO_D(36)	D88	PG4_A_CR ESET_L	E96	GROUND	F88	IO_D(63)
A97	NO CONNECT	B89	GROUND	C97	IO_D(35)	D89	IO_D(62)	E97	GROUND	F89	IO_D(58)
A98	IO_D(32)	B90	GROUND	C98	IO_D(29)	D90	IO_D(57)	E98	GROUND	F90	IO_D(59)
A99	IO_D(26)	B91	GROUND	C99	IO_D(30)	D91	IO_D(55)	E99	GROUND	F91	IO_D(54)
A10 0	IO_D(22)	B92	GROUND	C10 0	IO_D(19)	D92	IO_D(51)	E10 0	GROUND	F92	IO_D(53)
A10 1	NO CONNECT	B93	GROUND	C10 1	IO_D(18)	D93	IO_D(46)	E10 1	GROUND	F93	IO_D(48)
A10 2	IO_D(15)	B94	GROUND	C10 2	IO_D(7)	D94	IO_D(47)	E10 2	GROUND	F94	IO_D(44)
A10 3	NO CONNECT	B95	GROUND	C10 3	IO_D(9)	D95	IO_D(42)	E10 3	GROUND	F95	IO_D(38)
A10 4	IO_D(16)	B96	GROUND	C10 4	IO_D(5)	D96	IO_D(41)	E10 4	GROUND	F96	IO_D(40)
A10 5	NO CONNECT	B97	GROUND	C10 5	IO_D(1)	D97	IO_D(27)	E10 5	GROUND	F97	IO_D(34)
A10 6	IO_DEP_L(7)	B98	GROUND	C10 6	IO_D(3)	D98	IO_D(24)	E10 6	GROUND	F98	IO_D(28)
A10 7	IO_DEP_L(2)	B99	GROUND	C10 7	IO_DEP_L(6)	D99	IO_D(25)	E10 7	GROUND	F99	IO_D(21)
A10 8	NO CONNECT	B10 0	GROUND	C10 8	IO_DEP_L(1)	D10 0	IO_D(12)	E10 8	GROUND	F10 0	IO_D(17)
A10 9	CPU_SPI_RE SET_L	B10 1	GROUND	C10 9	SPI_CPU_ SEL_L	D10 1	IO_D(23)	E10 9	GROUND	F10 1	IO_D(14)
A11 0	SPI_SEL2_L	B10 2	GROUND	C11 0	SPI_SEL1_ L	D10 2	IO_D(20)	E11 0	GROUND	F10 2	IO_D(13)

Table 3-29: Profusion Carrier I/O Signal Connector Pinout (Continued)*

A111	SPI_SEL0_L	B103	GROUND	C111	SPI_MOSI	D103	IO_D(10)	E111	GROUND	F103	IO_D(8)
A112	SPI_MISO	B104	GROUND	C112	SPI_CLK	D104	IO_D(6)	E112	GROUND	F104	IO_D(11)
A113	I2C_BMC_SDA	B105	GROUND	C113	I2C_BMC_SCL	D105	IO_DEP_L(5)	E113	GROUND	F105	IO_D(4)
A114	I2C_GLOBAL_SDA	B106	GROUND	C114	I2C_GLOBAL_SCL	D106	IO_D(0)	E114	GROUND	F106	IO_D(2)
A115	I2C_DS2P1_SDA	B107	GROUND	C115	I2C_DS2P1_SCL	D107	IO_DEP_L(3)	E115	GROUND	F107	IO_DEP_L(4)
A116	I2C_DS2P0_SDA	B108	GROUND	C116	I2C_DS2P0_SCL	D108	NO CONNECT	E116	GROUND	F108	IO_DEP_L(0)
A169	IOC_SCLK	B109	GROUND	C169	IOC_MODE	D109	TOGGLE_OSC	E169	GROUND	F109	INIT_L
A170	ISP_CPU_EN_L	B110	GROUND	C170	IOC_SDI	D110	A20M_L	E170	GROUND	F110	INTR
A171	NO CONNECT	B111	GROUND	C171	5VSTNDBY	D111	CPU_SLP_L	E171	GROUND	F111	FERR_L
A172	NO CONNECT	B112	GROUND	C172	I2C_CEL_CONNECT_BMC_A	D112	STOP_CLK_L	E172	GROUND	F112	IGNNE_L
A173	FAN_FAILED_L	B113	GROUND	C173	PROC_RESET_L	D113	MEM_SBCERR_L	E173	GROUND	F113	PICD(1)
A174	SECURE_MODE_BMC	B114	GROUND	C174	FP_TO_PIIX_PWRBTN	D114	PICD(0)	E174	GROUND	F114	PIIX_SMB_SCL
A175	PS_PWR_ON	B115	GROUND	C175	INTRUSION_L	D115	PIIX_SMB_SDA	E175	GROUND	F115	PIC_CLK
A176	SPEAKER_DATA	B116	GROUND	C176	I2C_CEL_CONNECT_FPC	D116	PIIX_SMB_SEL1	E176	GROUND	F116	PIIX_SMB_SEL0
A177	PWR_CNTRL_RTC_L	B165	+12V	C177	PWR_CNTRL_SFC_L	D165	+5V	E177	GROUND	F165	+3.3V
A178	FP_NMI_SWT_L	B166	+12V	C178	HARD_RESET	D166	+5V	E178	GROUND	F166	+3.3V
A179	COM2_TO_FP_EN	B167	+12V	C179	COM2_TO_SIO_EN_A	D167	+5V	E179	GROUND	F167	+3.3V
A180	SMI_L	B168	+12V	C180	NMI_5V	D168	+5V	E180	GROUND	F168	+3.3V
		B169	GROUND			D169	IO_TDO			F169	IO_TDI
		B170	GROUND			D170	IO_TMS			F170	IO_TCK

Table 3-29: Profusion Carrier I/O Signal Connector Pinout (Continued)*

		B171	GROUND			D171	IO_TRST_L			F171	5VSTNDBY
		B172	GROUND			D172	5VSTNDBY			F172	5VSTNDBY
		B173	GROUND			D173	5VSTNDBY			F173	I2C_BACKUP_SDA
		B174	GROUND			D174	I2C_BACKUP_SCL			F174	I2C_FPC_SDA
		B175	GROUND			D175	I2C_FPC_SCL			F175	DTR_TTL_FP
		B176	GROUND			D176	RTS_TTL_FP			F176	RI_TTL_FP
		B177	GROUND			D177	CTS_TTL_FP			F177	DSR_TTL_FP
		B178	GROUND			D178	DCD_TTL_FP			F178	SOUT_TTL_XIMB
		B179	GROUND			D179	SOUT_TTL_COM2			F179	SIN_TTL_XIMB
		B180	GROUND			D180	SIN_TTL_COM2			F180	XIMB_SOUT_EN
		B181	+12V			D181	+5V			F181	+5V
		B182	+12V			D182	+5V			F182	+5V
		B183	+12V			D183	+5V			F183	+5V
		B184	+12V			D184	+5V			F184	+5V

3.4.2 Mechanical Specifications

Figure 3-7: Profusion* Carrier Mechanical Drawing shows the mechanical specifications for the Profusion carrier and the connector positions. All dimensions are given in inches

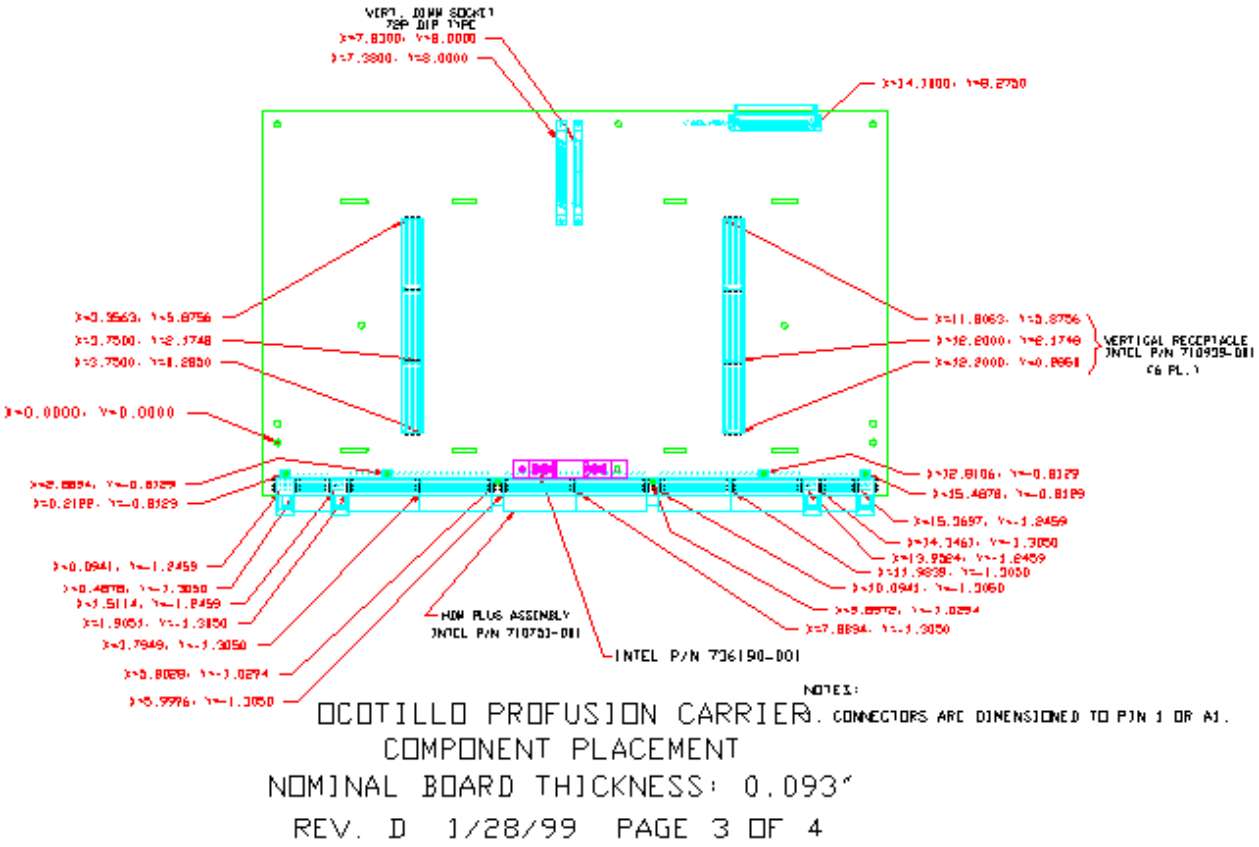


Figure 3-7: Profusion Carrier Mechanical Drawing*

3.4.2.1 Voltage Tolerances

Table 3-30: Voltage Tolerances

DC Voltage	Acceptable Tolerance
5 V	± 5%
3.3 V	± 5%
12 V	± 5%

4. OPRF100 Processor Mezzanine Board

This chapter describes the architecture and external interfaces of the OPRF100 processor mezzanine board. The processor mezzanine board has been designed for use with the OPRF100 MP board set.

Features

- Each module accommodates one to four Intel® Pentium® III Xeon™ processors.
- Six integrated voltage regulators.
- System may have one or two processor mezzanine boards.
- EEPROM with FRU information.
- Complete JTAG scan chain.

4.1 Introduction

The OPRF100 processor mezzanine board is used for the installation of and power delivery to the Pentium III Xeon processors. Each mezzanine board can accommodate up to four processors. Two mezzanine boards can be used to support up to eight processors in the board set. The board partitioning of the mezzanine allows for flexibility by requiring that only one mezzanine be installed. The second mezzanine is needed only when using five or more processors, and its mating connector on the OPRF100 Profusion* carrier can be left unpopulated when not in use.

The diagram below provides an overview of the processor mezzanine board, showing primary components and their relationships, and physical board layout diagrams.

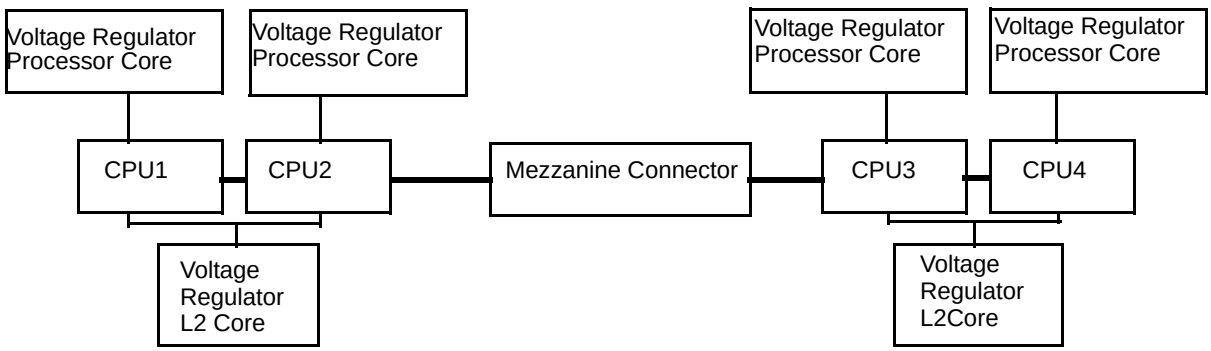


Figure 4-1: Block Diagram of the OPRF100 Processor Mezzanine Board

4.1.1 Architectural Overview

The mezzanine provides the connectors with which to install the Pentium III Xeon processors. It uses integrated voltage regulators to correctly power the processors from the main system power

distribution system. It also provides the function of handling all of the JTAG scan signals. As with all other boards of the OPRF100 MP board set, the mezzanine board also includes a SEEPROM component for storage of FRU data including part number, serial number, board ID, etc. Each of these functional components of the mezzanine is described in further detail in the following sections.

4.1.1.1 Four Pentium® III Xeon™ Processor Slots

The OPRF100 processor mezzanine board can accept up to four Pentium III Xeon processors. Any unpopulated slot requires an A450NX processor termination module. For example, if two processors are used, then two termination modules are needed. The processor and/or termination modules may be populated in any order. If a mezzanine is not populated with processors, then no termination modules are required.

Termination modules must provide proper termination on the GTL+ signals and connect TDI to TDO on the JTAG bus.

4.1.1.2 Voltage Regulators and L2 VID Compare

The Profusion carrier provides enough current to power two processor mezzanine boards. Six voltage regulators powered from +12 V reside on each processor mezzanine. Each processor slot has an individual voltage regulator for the processor core logic, and a voltage regulator that is shared between two processor slots for the L2 cache logic, for a total of six voltage regulators on the board.

Each processor core and L2 cache outputs a unique 5-bit VID (Voltage ID) signal. If the VIDs on shared L2 caches do not match, then the power is disabled to both processor cores and L2 caches to prevent damage. Slots 1 and 2 share a L2 cache, as do slots 3 and 4.

4.1.1.3 I^2C* Accessed Features

The processor mezzanine board contains the following I^2C* accessible devices on two unique buses.

- 24C02* – SEEPROM containing FRU information.
- Processor SMB bus – a common bus for all four slots.

These devices are accessed via the baseboard management controller (BMC) on the OPRF100 I/O carrier. See in the *Saber Server Management External Architecture Specification* for information on addressing these devices.

The 24C02, when accessed via the I^2C bus, will provide FRU information. The FRU information is read by Intel®'s LANDesk® Server Manager software, or equivalent, and available via the LANDesk Server Manager console.

The 24C02 SEEPROM has 256 bytes of programmable space, which is broken into four areas. The table below shows a list of the areas, a description, and the space allocated.

Table 4-1: 24C02 SEEPROM Programming Areas

Area	Size	Description
Common Header	8 Bytes	Programming offsets to the other areas below.
Internal Use	48 Bytes	This area is reserved for general purpose use by Intel®'s server management firmware/controllers.
Board Info.	80 Bytes	Contains the board FRU information listed in the table below.
Product Info.	80 Bytes	Available for OEM use.

The table below lists the board specific FRU information that will be programmed into the board info. area.

Table 4-2: FRU Information

Board Information			
Information	**Description**	**Example**	**Notes**
Format Version	Specifies the version of the format definition for this area.	01h	1
Board Area Length	Defines the size of this area in multiples of 8 bytes.	0Ah = 80 bytes	1
Language Code	Specifies the language that the information is in.	00 = 8-bit Latin 1 ASCII	1
Mfg. Date/Time	Time and date of board manufacture (value programmed (in hex) is the number of minutes after 0:00 hrs. 1/1/96).	000f593h (Date and time translation shown below.) f593h = 62867 min. = 43 days and 947 min. = Feb 12, 1996, 3:47p.m.	2
Manufacturer Type/ Length byte	Specifies what type and how big the following field is.	C5h = 8 bit ASCII, 5 bytes	1
Manufacturer	Board Manufacturer	Intel	1
Board Product Name Type/Length byte	Specifies what type and how big the following field is.	DBh = 8 bit ASCII, 27 bytes	1
Board Product Name	Board Name/Description	OPRF100 processor mezzanine	1
Board Serial Number	Intel® Board Serial Number	N42385906	2
Board Part Number Type/Length byte	Specifies what type and how big the following field is.	CAh = 8 bit ASCII, 10 bytes	1

Table 4-2: FRU Information (Continued)

Board Part Number	Intel Board Part Number	714520-001	2

Notes:
1. Actual value programmed into the board.
2. Example value. Actual value will vary from board to board and/or from fab to fab

The table below identifies the byte allocation and purpose within the 24C02 SEEPROM. This information is useful for those who will be accessing the hardware directly for information (i.e., BIOS developers and server management software developers).

Table 4-3: SEEPROM Content Location

Address	Length	Description	Default Value
0x00	1	Common Header Format Version	0x01
0x01	1	Internal Use Area Offset (8-byte multiples)	0x01
0x02	1	Chassis Information Area Offset (8-byte multiples)	0x00 (area not present)
0x03	1	Board Information Area Offset (8-byte multiples)	0x07
0x04	1	Product Information Area Offset (8-byte multiples)	0x00
0x05	2	Zero Padding	
0x07	1	Common Header Checksum	0xE8
0x08	48	Internal Use Area	
0x38	1	Board Information Area Format Version	0x01
0x39	1	Board Information Area Length (8-byte multiples)	0x0A
0x3A	1	Unicode Country Base	0x00
0x3B	3	Manufacture Date/Time	
0x3E	1	Board Manufacturer Type/Length Byte	0xC5
0x3F	5	Board Manufacturer (ASCII)	‘Intel’
0x44	1	Product Name Type/Length Byte	0xDB
0x45	28	Product Name	‘OPRF100 processor mezzanine’
0x61	1	Board Serial Number Type/Length Byte	0xCC
0x62	9	Board Serial Number	
0x6B	1	Board Part Number Type/Length Byte	0xCA
0x6D	10	Board Part Number	

Table 4-3: SEEPROM Content Location (Continued)

0x76	1	No More Fields Flag	0xC1
0x77	16	Zero Padding	
0x87	1	Board Information Area Checksum	
0x88	120	Product Information Area	

EEPROM data may be accessed via I^2C commands to the 24C02 device.

4.1.1.4 JTAG and ITP Connector

The module provides a complete JTAG interface via the mezzanine connector or ITP connector. In order for the JTAG bus to function, an A450NX processor termination module is required for any unoccupied processor slot to complete the scan chain. The scan chain order is slot 1, slot 2, slot 3, then slot 4.

4.1.2 Placement Diagram

Figure 4-2: Placement Diagram shows the primary components of the processor mezzanine board and their positions on the printed circuit board.

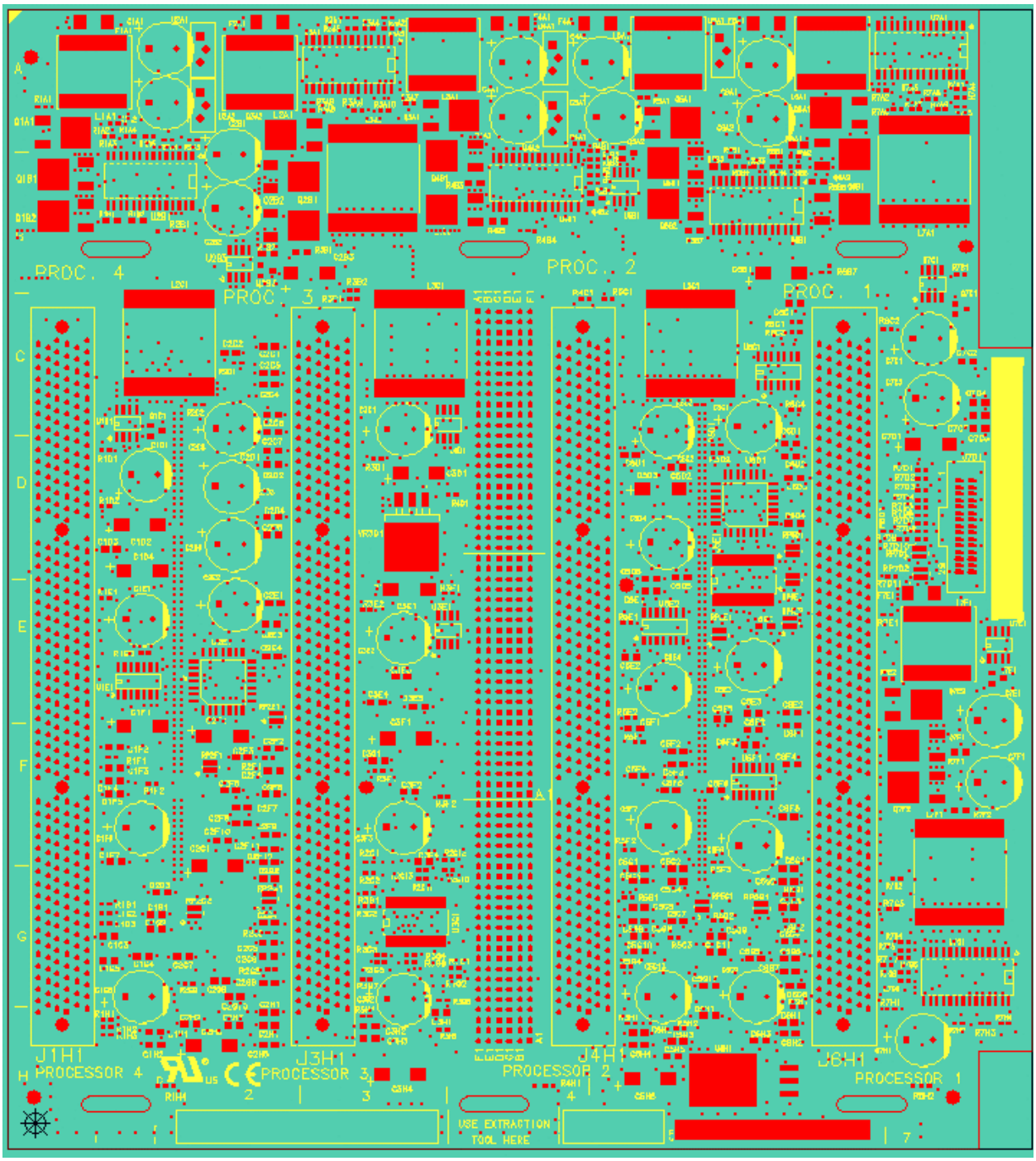


Figure 4-2: Placement Diagram

Table 4-4: Reference Designator Descriptions

Reference Designator	Description
J6H1	Processor slot 1
J4H1	Processor slot 2
J3H1	Processor slot 3
J1H1	Processor slot 4
J4T1,J4P1,J4L1	Mezzanine connector
VR3D1	LT1585* VTT regulator
U3E1	24C02*
J7D1	ITP connector

4.2 Signal Descriptions

This section provides a reference to signal pins used on the mezzanine connector. The signal mnemonics defined here may appear in descriptive text in the document. For complete signal descriptions, refer to the *100-MHz Slot 2 Processor EMTS, Version 1.5* document. An "_L" suffix on the signal name indicates that the signal is active-low. (**Note:** "_L" is the same convention used in schematics and simulation). A colon between numbers indicates a range of signals (e.g., A [31:0]).

4.2.1 Mezzanine Connector Interface Bus Signals

Following is a summary of the mezzanine bus signal pins, including the signal mnemonic, electrical type, full name, and brief description. The electrical types are shown in the table below.

Table 4-5: Electrical Types

Type	Description
in	Input is a standard input-only signal.
out	Totem Pole Output is a standard active driver.
o/d	Open Drain allows multiple devices to share signals as a wired-OR.

The supported mezzanine interface signals are listed in the table below.

Table 4-6: Processor Mezzanine Interface Connector Signal Summary

Signal(s)	Type	Name and Description
L12_PWRGD	out	Power Good status from shared L2 voltage regulators for processors 1 and 2.
L34_PWRGD	out	Power Good status from shared L2 voltage regulators for processors 3 and 4.
P12_L2_VRM_OUTEN	out	Pentium® III Xeon™ processors 1 and 2 L2 VIDs match and voltage regulator enabled.
P34_L2_VRM_OUTEN	out	Pentium III Xeon processors 3 and 4 L2 VIDs match and voltage regulator enabled.
P6_A[35:3]	in/out	Address Bus.
P6_A20M_L	in/out	Address-20 Mask.
P6_ADS_L	in/out	Address Strobe.
P6_AERR_L	in/out	Address Parity Error.
P6_APICCLK	in	APIC Clock.
P6_BERR_L	in/out	Bus Error.
P6_BINIT_L	in/out	Bus Initialization.
P6_BNR_L	in/out	Block Next Request.
P6_BPRI_L	in/out	Priority Agent Bus Request.
P6_D[63:0]_L	in/out	Data.
P6_DBSY_L	in/out	Data Bus Ready.
P6_DEFER_L	in/out	Defer.
P6_DRDY_L	in/out	Data Ready.
P6_FRCERR12	In/out	Functional Redundancy Checking Error processors 1 and 2.
P6_FRCERR34	In/out	Functional Redundancy Checking Error processors 3 and 4.
P6_HIT_L	in/out	Hit.
P6_HITM_L	in/out	Hit Modified.
P6_IGNNE_L	In	Ignore Numeric Error.
P6_LOCK_L	in/out	Lock.
P6_RESET_L	in/out	Reset.
P6_RP_L	in/out	Request Parity.
P6_RSP_L	in/out	Response Parity Signal.

Table 4-6: Processor Mezzanine Interface Connector Signal Summary (Continued)

P6_SBRK_L	in/out	System Break.
P6_SMI_L	in	System Management Interrupt.
P6_TRDY_L	in/out	Target Ready.
SM_SCL	in	I^2C* Clock. Clock reference for the I^2C interface to Pentium III Xeon processors.
ISM_SDA	in/out	I^2C Data. Serial data transfer for the I^2C interface to Pentium III Xeon processor.
I2C_SCL	in	I^2C Clock. Clock reference for the I^2C interface to 24C02*.
I2C_SDA	in/out	I^2C Data. Serial data transfer for the I^2C interface to 24C02.
TDI	in	JTAG Input.
TDO	o/d	JTAG Output.
TRST_L	in	JTAG Reset.
P6_APICD[0:1]	in/out	APIC Data.
P6_AP[1:0]_L	in/out	Address Parity.
P6_RS[2:0]_L	in/out	Response Signals.
P6_BREQ[3:0]_L	in/out	Symmetric Agent Bus Request.
P6_REQ[4:0]_L	in/out	Request Command.
P[4:1]_BCLK	in	100-MHz Clock to each slot.
P[4:1]_FERR_L	out	Floating-point Error.
P[4:1]_FLUSH_L	in	Flush.
P[4:1]_IERR_L	out	Internal Error.
P[4:1]_PWRGD	out	Power Good status from each processor core voltage regulator.
P[4:1]_PWREN	out	Pentium III Xeon processor populated and voltage regulator enabled.
P[4:1]_STPCLK_L	in	Stop Clock.
P[4:1]_SLP_L	in	Sleep.
P[4:1]_THERMTRIP_L	out	Thermal Trip.
P6_DEP[7:0]_L	in/out	Data Bus ECC/Parity.

4.3 Specifications

This section specifies the operational parameters and physical characteristics for the processor mezzanine board. This is a board-level specification only.

4.3.1 Mechanical Specifications

Figure 4-4: Mechanical Specifications shows the mechanical specifications of the processor mezzanine board. All dimensions are given in inches.

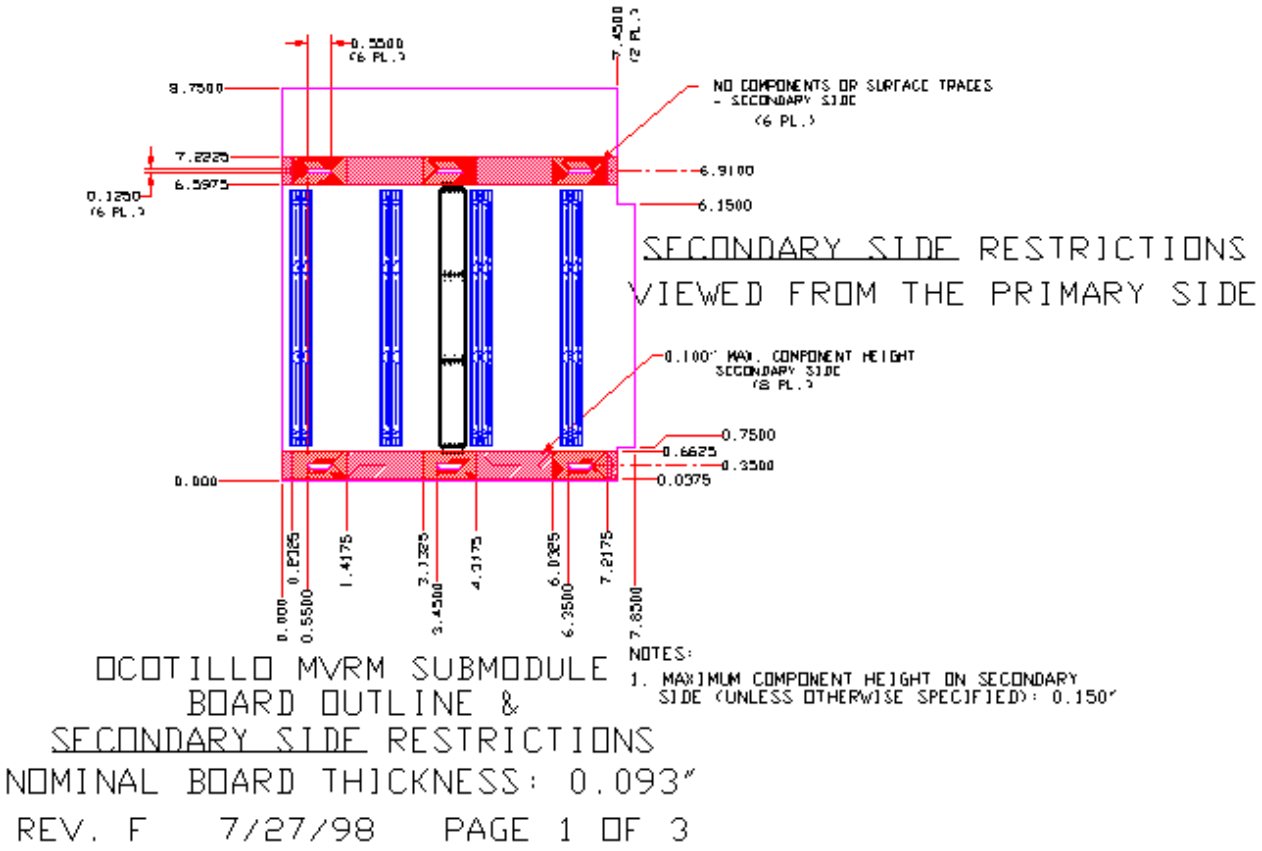


Figure 4-4: Mechanical Specifications

4.3.1.1 Voltage Tolerances

The Profusion carrier must supply 12.0 V, 5.0 V, 3.3 V, and 2.5 V power to the processor mezzanine board. shows the acceptable tolerance range for these voltage levels.

Table 4-7: DC Voltage

DC Voltage	Acceptable Tolerance
+ 12.0 V	± 5 %
+ 5.0 V	± 5 %
+ 3.3 V	± 5 %
+ 2.5 V	± 5 %

4.3.1.2 Mezzanine Interface Connector

The processor mezzanine board uses three 144-pin connector sections to form a single large connector. See the table below for the pin assignments. Note that sections 1 and 3 are the same physical part with an endcap, hence section 3 is rotated 180 degrees.

Table 4-8: Mezzanine Interface Connector Pinout (Section 1)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	+12V	B1	+12V	C1	+12V	D1	+12V	E1	+12V	F1	+12V
A2	+12V	B2	+12V	C2	+12V	D2	+12V	E2	+12V	F2	+12V
A3	+12V	B3	+12V	C3	+12V	D3	+12V	E3	+12V	F3	+12V
A4	+12V	B4	+12V	C4	+12V	D4	+12V	E4	+12V	F4	+12V
A5	P2_PWRGD	B5	P1_PWRGD	C5	N/C	D5	N/C	E5	P3_PWRGD	F5	P4_PWRGD
A6	P2_PWREN	B6	P1_PWREN	C6	+2.5V	D6	+2.5V	E6	P3_PWREN	F6	P4_PWREN
A7	P2_FERR_L	B7	P1_FERR_L	C7	P6_SMI_L	D7	GROUND	E7	P3_FERR_L	F7	P4_FERR_L
A8	TDI	B8	TDO	C8	TRST_L	D8	GROUND	E8	TCK	F8	TMS
A9	P2_IERR_L	B9	P2_IERR_L	C9	P6_INIT_L	D9	N/C	E9	P3_IERR_L	F9	P4_IERR_L
A10	P6_A20_L	B10	P6_IGNNE_L	C10	N/C	D10	N/C	E10		F10	N/C
A11	P2_SLP_L	B11	P1_SLP_L	C11	GROUND	D11	N/C	E11	P4_SLP_L	F11	P3_SLP_L
A12	P2_THERMTRIP_L	B12	P2_THERMTRIP_L	C12	GROUND	D12	N/C	E12	P2_THERMTRIP_L	F12	P2_THERMTRIP_L

Table 4-8: Mezzanine Interface Connector Pinout (Section 1) (Continued)

A13	N/C	B13	P6_APICD0	C13	IO_PWRGD	D13	N/C	E13	N/C	F13	N/C
A14	P6_APICCLK	B14	P6_APICD1	C14	P6_PWRGD_DC	D14	P6_NMI	E14	P6_INTR	F14	N/C
A15	P2_STPCLK_L	B15	P1_STPCLK_L	C15	N/C	D15	N/C	E15	P3_STPCLK_L	F15	P4_STPCLK_L
A16	P2_FLUSH_L	B16	P1_FLUSH_L	C16	N/C	D16	N/C	E16	P3_FLUSH_L	F16	P4_FLUSH_L
A17	N/C	B17	N/C	C17	N/C	D17	N/C	E17	GROUND	F17	N/C
A18	GROUND	B18	N/C	C18	N/C	D18	GROUND	E18	P6_BINIT_L	F18	N/C
A19	P6_DEP_L(4)	B19	P6_DEP_L(2)	C19	GROUND	D19	P6_DEP_L(0)	E19	P6_DEP_L(1)	F19	GROUND
A20	P6_D_L(62)	B20	GROUND	C20	P6_DEP_L(7)	D20	P6_DEP_L(3)	E20	GROUND	F20	VCCP1
A21	GROUND	B21	P6_D_L(58)	C21	P6_DEP_L(6)	D21	GROUND	E21	P6_DEP_L(5)	F21	VCCP2
A22	P6_D_L(63)	B22	P6_D_L(56)	C22	GROUND	D22	P6_D_L(55)	E22	P6_D_L(61)	F22	GROUND
A23	P6_D_L(50)	B23	GROUND	C23	P6_D_L(60)	D23	P6_D_L(53)	E23	GROUND	F23	VCCP3
A24	GROUND	B24	P6_D_L(59)	C24	P6_D_L(54)	D24	GROUND	E24	P6_D_L(57)	F24	VCCP4

Table 4-9: Mezzanine Interface Connector Pinout (Section 2)

Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
A1	P6_D_L(48)	B1	N/C	C1	GROUND	D1	P6_D_L(46)	E1	N/C	F1	GROUND
A2	P6_D_L(52)	B2	GROUND	C2	P6_D_L(51)	D2	P6_D_L(49)	E2	GROUND	F2	RESERVED
A3	GROUND	B3	N/C	C3	N/C	D3	GROUND	E3	P6_D_L(39)	F3	RESERVED
A4	P6_D_L(47)	B4	P6_D_L(41)	C4	GROUND	D4	P6_D_L(42)	E4	P6_D_L(45)	F4	GROUND
A5	P6_D_L(40)	B5	GROUND	C5	P6_D_L(44)	D5	P6_D_L(36)	E5	GROUND	F5	RESERVED
A6	GROUND	B6	P6_D_L(34)	C6	P6_D_L(37)	D6	GROUND	E6	P6_D_L(43)	F6	RESERVED
A7	P6_D_L(32)	B7	P6_D_L(38)	C7	GROUND	D7	P6_D_L(35)	E7	P6_D_L(33)	F7	GROUND
A8	P6_D_L(29)	B8	GROUND	C8	P6_D_L(28)	D8	P6_D_L(31)	E8	GROUND	F8	RESERVED

Table 4-9: Mezzanine Interface Connector Pinout (Section 2) (Continued)

A9	GROUND	B9	P6_D_L(25)	C9	P6_D_L(26)	D9	GROUND	E9	P6_D_L(30)	F9	RESERVED
A10	P6_D_L(22)	B10	P6_D_L(19)	C10	GROUND	D10	N/C	E10	N/C	F10	GROUND
A11	P6_D_L(27)	B11	GROUND	C11	P6_D_L(24)	D11	P6_D_L(23)	E11	GROUND	F11	RESERVED
A12	GROUND	B12	P6_D_L(20)	C12	P6_D_L(18)	D12	GROUND	E12	P6_D_L(21)	F12	N/C
A13	N/C	B13	N/C	C13	GROUND	D13	P6_D_L(16)	E13	P6_D_L(13)	F13	GROUND
A14	P6_D_L(17)	B14	GROUND	C14	P6_D_L(15)	D14	P6_D_L(11)	E14	GROUND	F14	N/C
A15	GROUND	B15	P6_D_L(7)	C15	P6_D_L(12)	D15	GROUND	E15	P6_D_L(10)	F15	N/C
A16	P6_D_L(4)	B16	P6_D_L(6)	C16	GROUND	D16	P6_D_L(9)	E16	P6_D_L(14)	F16	GROUND
A17	P6_D_L(2)	B17	GROUND	C17	P6_D_L(5)	D17	P6_D_L(8)	E17	GROUND	F17	N/C
A18	GROUND	B18	P6_D_L(0)	C18	P6_D_L(1)	D18	GROUND	E18	P6_D_L(3)	F18	P6_FRCERR34
A19	P6_FRCERR12	B19	P6_RESET_L	C19	GROUND	D19	VREF	E19	VREF	F19	GROUND
A20	P6_A_L(35)	B20	GROUND	C20	P6_A_L(32)	D20	N/C	E20	GROUND	F20	N/C
A21	GROUND	B21	N/C	C21	P6_A_L(33)	D21	GROUND	E21	P6_BERR_L	F21	N/C
A22	P6_D_L(26)	B22	P6_A_L(29)	C22	GROUND	D22	P6_A_L(30)	E22	P6_A_L(34)	F22	GROUND
A23	P6_D_L(31)	B23	GROUND	C23	N/C	D23	N/C	E23	GROUND	F23	+5V
A24	GROUND	B24	P6_A_L(28)	C24	P6_A_L(24)	D24	GROUND	E24	P6_A_L(27)	F24	+5V

Table 4-10: Mezzanine Interface Connector Pinout (Section 3)

Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
A1	+12V	B1	+12V	C1	+12V	D1	+12V	E1	+12V	F1	+12V
A2	+12V	B2	+12V	C2	+12V	D2	+12V	E2	+12V	F2	+12V

Table 4-10: Mezzanine Interface Connector Pinout (Section 3) (Continued)

A3	+12V	B3	+12V	C3	+12V	D3	+12V	E3	+12V	F3	+12V
A4	SM_SCL	B4	SM_SDA	C4	+12V	D4	+12V	E4	GROUND	F4	ITP_BCLK
A5	GROUND	B5	GROUND	C5	I2C_SDA	D5	I2C_SCL	E5	GROUND	F5	GROUND
A6	P4_BCLK	B6	GROUND	C6	+3.3V	D6	L34_PWRGD	E6	GROUND	F6	P2_BCLK
A7	GROUND	B7	GROUND	C7	+3.3V	D7	+3.3V	E7	GROUND	F7	GROUND
A8	P3_BCLK	B8	GROUND	C8	+3.3V	D8	L12_PWRGD	E8	GROUND	F8	P1_BLCK
A9	GROUND	B9	GROUND	C9	+3.3V	D9	+3.3V	E9	N/C	F9	GROUND
A10	P6_ADS_L	B10	P6_AP_L(0)	C10	GROUND	D10	P6_RSP_L	E10	P6_AP_L(1)	F10	GROUND
A11	P6_BREQ_L(2)	B11	GROUND	C11	P6_BREQ_L(0)	D11	P6_BREQ_L(3)	E11	GROUND	F11	P6_BREQ_L(1)
A12	GROUND	B12	N/C	C12	P6_DBSY_L	D12	GROUND	E12	P6_RS_L(1)	F12	P6_RP_L
A13	N/C	B13	P6_REQ_L(3)	C13	GROUND	D13	P6_HITM_L	E13	P6_RS_L(2)	F13	GROUND
A14	VCCL2_1	B14	GROUND	C14	P6_REQ_L(2)	D14	P6_RS_L(0)	E14	GROUND	F14	P6_HIT_L
A15	GROUND	B15	P6_DEFER_L	C15	P6_TRDY_L	D15	GROUND	E15	P6_LOCK_L	F15	P6_DRDY_L
A16	N/C	B16	P6_BPRI_L	C16	GROUND	D16	P6_REQ_L(1)	E16	P6_REQ_L(4)	F16	GROUND
A17	VCCL2_2	B17	GROUND	C17	P6_BNR_L	D17	N/C	E17	GROUND	F17	P6_REQ_L(0)
A18	GROUND	B18	P6_A_L(9)	C18	P6_A_L(4)	D18	GROUND	E18	P6_A_L(3)	F18	P6_A_L(6)
A19	N/C	B19	P6_AERR_L	C19	GROUND	D19	P6_A_L(8)	E19	P6_A_L(7)	F19	GROUND
A20	N/C	B20	GROUND	C20	P6_A_L(5)	D20	P6_A_L(10)	E20	GROUND	F20	P6_A_L(12)
A21	GROUND	B21	P6_A_L(14)	C21	N/C	D21	GROUND	E21	P6_A_L(17)	F21	P6_A_L(11)
A22	N/C	B22	P6_A_L(16)	C22	GROUND	D22	P6_A_L(13)	E22	P6_A_L(18)	F22	GROUND
A23	N/C	B23	GROUND	C23	P6_A_L(19)	D23	P6_A_L(25)	E23	GROUND	F23	P6_A_L(15)
A24	GROUND	B24	P6_A_L(22)	C24	P6_A_L(23)	D24	GROUND	E24	P6_A_L(20)	F24	P6_A_L(21)

5. OPRF100 Memory Carrier

This chapter describes the architecture and external interfaces of the OPRF100 memory carrier. The OPRF100 memory carrier is a high-capacity SDRAM memory board based on the Profusion* PCIset. The memory carrier has been designed for use with the OPRF100 MP board set.

Features

- Up to 16 GB of ECC memory per carrier using 16 72-bit dual inline memory modules (DIMMs), for a total of up to 32 GB using two carriers.
- PC-100 compatible 3.3 V registered SDRAM modules (in compliance with the *PC-100 Registered DIMM Specification*, Version 1.2).
- SDRAM burst access and two-way interleaving (when two memory boards are installed).
- Minimum configuration of 128 MB using one 128-MB DIMM.
- Supports PC-100 registered DIMMs with capacity of 128 MB, 256 MB, 512 MB, and 1024 MB. See your Intel sales representative for a list of supported DIMM part numbers.
- Provides server management data, including thermal monitoring, FRU information, and presence detect bit access.
- High reliability HDM right-angle mating connector for interfacing with the OPRF100 midplane.

5.1 Introduction

This section provides an overview of the OPRF100 memory carrier, showing primary components and their relationships, and physical board layout diagrams.

5.1.1 Block Diagram

Figure 5-1: OPRF100 Memory Carrier Block Diagram shows the main architectural features of the memory carrier.

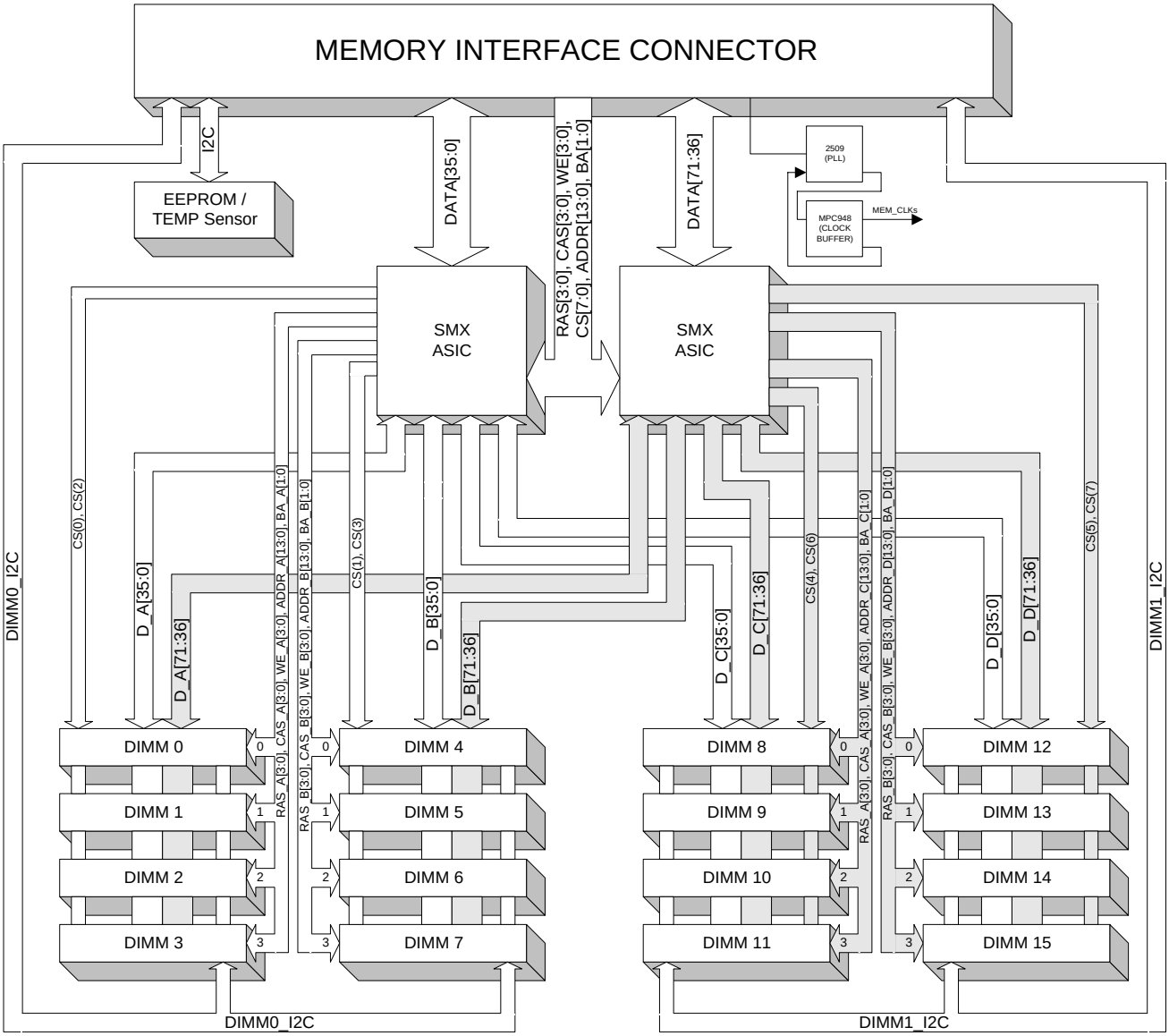


Figure 5-1: OPRF100 Memory Carrier Block Diagram

5.1.2 Memory Carrier Clock Distribution Diagram

Figure 5-2: OPRF100 Memory Carrier Clock Distribution Diagram shows the clock distribution scheme for the OPRF100 memory carrier.

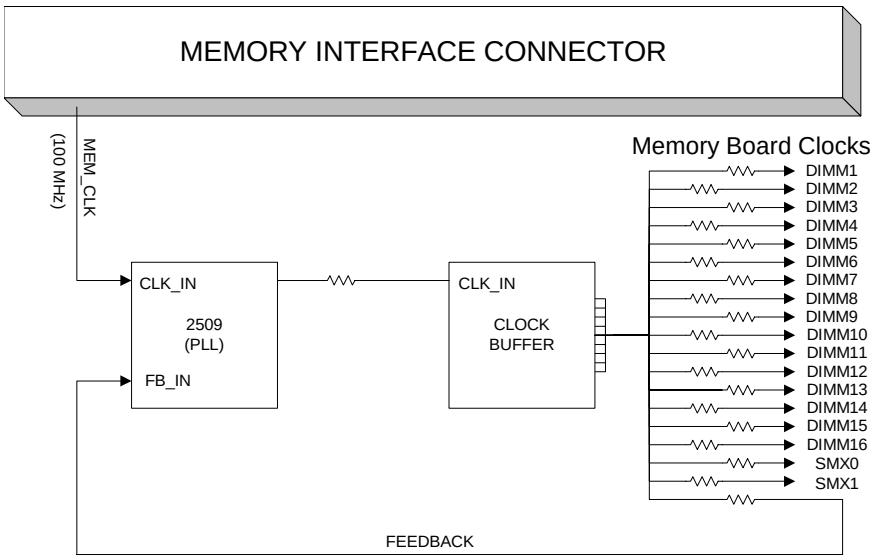


Figure 5-2: OPRF100 Memory Carrier Clock Distribution Diagram

5.1.3 Architectural Overview

The OPRF100 memory carrier is based on the Profusion PCIset. The carrier's main components are as follows:

- DRAM array consisting of 16 DIMM sockets, which accept 3.3 V PC-100 (Rev 1.2) registered SDRAM ECC DIMMs.
- Two SMX memory pipeline ASICs. These ASICs provide registered fanout of the SDRAM control signals (RAS, CAS, WE, Address, and Chip Select) to the SDRAM array. The SMX devices also function as a 1:4 bidirectional registered pipeline multiplexor for the data signals to/from the SDRAM array.
- Server management support with onboard EEPROM and temperature sensors plus accessibility of EEPROM data from all DIMMs.

5.1.4 Placement Diagram

Figure 5-3: Memory Carrier Placement Diagram was generated from the actual layout database and shows the primary components of the memory carrier and their position on the printed circuit board. The table below maps reference designator to device name.

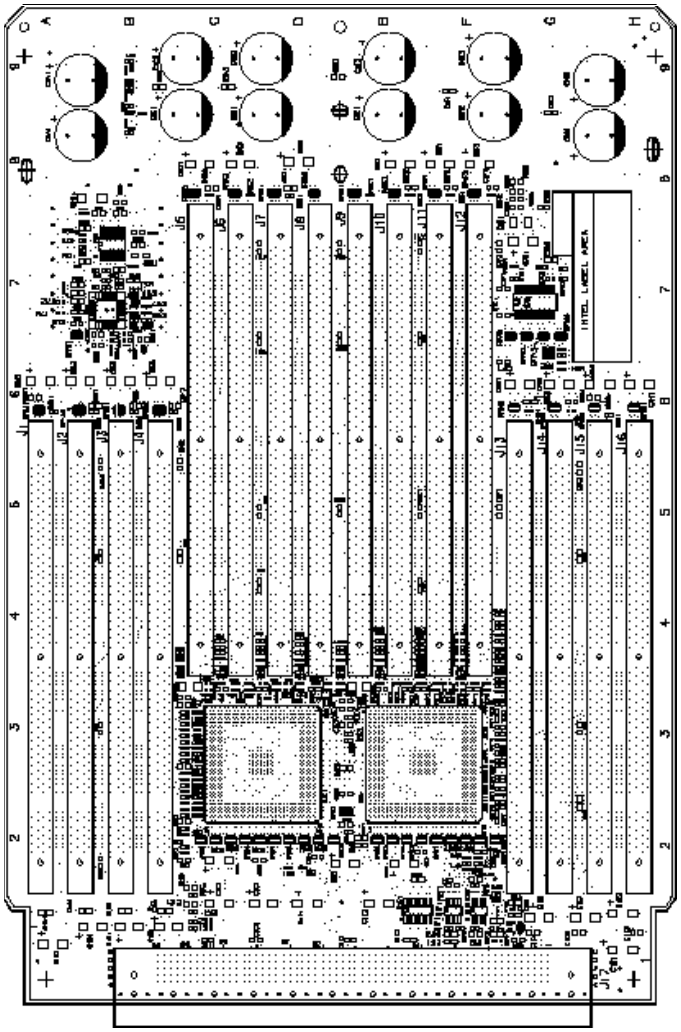


Figure 5-3: Memory Carrier Placement Diagram

Table 5-1: Placement Diagram Reference Designators

Reference Designator	Description
J17	Memory interface connector.
J1-J16	168-pin SDRAM DIMM sockets.

Table 5-1: Placement Diagram Reference Designators (Continued)

U3C1	SMX0, Memory board controller for DIMMs 0-7. (388 pin BGA)
U3E1	SMX1, Memory board controller for DIMMs 8-16. (388 pin BGA)
U7B1	Clock driver (PLL).
U7B2	MPC948, 1:12 Clock distribution chip (buffer).
U7G1	74ALVCH16244*, 16-bit buffer/driver.
U1F2	DS1621*, I^2C* Temperature sensor.
U1F1	AT24C02*, I^2C EEPROM.
U1E1	74LVC04*, Hex inverter.

5.2 Functional Description

This section provides a more detailed description of the memory carrier functional blocks.

5.2.1 SDRAM Array

The memory array on the memory carrier consists of 16 72-bit (64-bit data plus eight ECC bits) DIMM sockets. Each of the SDRAM DIMMs operates with a burst length of four, thus providing a full 288-bit (32-byte) cache line per transaction.

There are several types of DIMMs available; the table below shows which permutations of normal DIMM options can be used in the memory carrier. This is subject to change, and inclusion in this table does not imply that a particular DIMM type will be validated.

Table 5-2: Memory Carrier DIMM Support

Category	**Supported DIMM Variety**
Speed	100 MHz, PC-100 compatible SDRAM (refer to the *PC Registered DIMM Specification Revision 1.2*)
Capacity/ Organization/ Refresh	128 MB: 64 Mbit, 4MBx4bankx4 SDRAM 256 MB: (double-high; 64 Mbit, 4MBx4bankx4 SDRAM or 128 MB, 8MBx4bankx4 SDRAM) 512 MB: (double-high; 128 Mbit, 8MBx4bankx4 SDRAM or 256 MB, 16MBx4bankx4 SDRAM) 1GB DIMM: double-high; 256 Mbit, 16Mx4bankx4 SDRAM
Voltage	3.3 V

Table 5-2: Memory Carrier DIMM Support (Continued)

Data Width	X72 (ECC)
Page Mode	SDRAM
Buffered/Registered	Registered
Maximum Overall Height	43.18 mm (1.7 inches) (refer to the *PC Registered DIMM Specification Revision 1.2*)
Maximum Overall DIMM Thickness	8.13 mm (0.32 inches) (refer to the *PC Registered DIMM Specification Revision 1.2*)

- 128, 256, 512, and 1024-MB DIMMs.
- From 1 to 32 DIMMs (total number of DIMMs for two memory carriers).
- Equal number of DIMMs should be placed on each memory carrier (except when only one DIMM is used, then the single DIMM should be placed in the primary memory carrier).
- DIMM sizes on a single carrier may vary, but when both memory carriers are installed, the DIMM configuration on each memory carrier should be identical to support memory interleaving for performance gains. This rule also applies to mixing SDRAM technologies. For example: 256-MB DIMMs can be built with either stacked 64-MB SDRAMs or with 128-MB SDRAMs. These two different 256-MB DIMMs are interchangeable and can be mixed in any configuration on a single memory carrier. However, two DIMMs of equal size, but built with different SDRAM density should not be mixed in the same DIMM connector location across memory ports.

During Power-on Self Test (POST), the BIOS will scan the EEPROM of all DIMMs.

Depending on how the memory carriers are installed, the memory subsystem can operate in two different modes. See the descriptions below for each population option.

Interleaved: (Two memory carriers installed): In this configuration, the memory subsystem operates in interleaved mode such that the memory carriers share a common address range. One memory carrier will respond to even-numbered cache lines, while the other memory carrier will respond to odd-numbered cache lines. This configuration will offer the highest performance because it allows the two memory carriers to be used in a balanced fashion, reducing address conflicts.

In the two-memory carrier configuration, the DIMMs must be installed in pairs (one on each carrier) and in the same location on each memory carrier.

Single Port Mode: (One memory carrier installed.) In this configuration, the memory subsystem operates in a single-port mode such that the one installed memory carrier responds to all memory addresses. The DIMMs on this single memory carrier are not required to be installed in pairs and can be installed one DIMM at a time.

Although a single memory carrier will support DIMM population in various configurations (empty sockets included), when fewer than 16 DIMMs are installed on a memory carrier, there is a preferred order for populating the DIMM sites.

5.2.2 Profusion* PCIset

5.2.2.1 Memory Carrier SDRAM Interface MUX (SMX)

The SDRAM interface multiplexor (SMX) interfaces between the SDRAM controller and the SDRAM memory to provide a pipelined registered multiplexor. It is used in a high speed SDRAM memory application in which four separate DATA ports must be multiplexed onto, or demultiplexed from, a single memory port. It performs two major functions for the memory interface: a registered fanout of the control and address signals and registered, multiplexed data flow between the memory controller and the four data ports. Two SMXs together make up a complete memory interface supporting up to 32 GB of memory across two memory carriers.

The control and address signals are registered and provide two copies for greater fanout. The control block functions as a simple 1:2 registered driver. It drives two registered copies of each control signal out to the memory interface. The control signals are also used internally to generate the steering logic for the data path block. The address block is similar to the data path block in functionality.

The data path block functions as a registered 4:1 multiplexor during read operations and as a 1:4 decoded registered driver during write operations. It supports up to four burst reads and writes. Each data path direction has its own output enable signal (generated internally). During a read operation, data is stored in the internal B port registers on the low-to-high transition of the clock (CLK) input. The internally generated select (SEL0,SEL1) signals provide switching ability between the four data ports onto the memory controller data bus. The register on the memory controller output permits the fastest possible data transfer, thus extending the period for which data is valid on the bus. During write operations the input data from the memory controller is stored on the four B port registers and output enable is used to switch the data out onto one of the four data ports. The output enable signal is generated internally using the control signal inputs.

The control terminals are registered so that all transactions are synchronous with CLK.

5.2.2.2 Error Detection and Correction

The Profusion PCIset provides automatic correction of single bit errors and detection of double bit errors. All failures can be reported by the BIOS into the system event log (SEL). Single bit errors will be reported in the SEL to identify the specific failing DIMM. See the *OCPRF100 BIOS External Product Specification* for additional information about the format in which the memory errors are logged.

5.2.3 System Management Interface

The memory carrier provides system management software with information about board operating temperature and DIMM configuration in addition to FRU information about the memory carrier itself.

The temperature and FRU data comes from two devices that reside on the SM BMC private I^{2}C* bus. Temperature data is provided by a Dallas Semiconductor* DS1621 temperature sensor, while the FRU data is provided by an Atmel* AT24C02 EEPROM. DIMM configuration data (presence, organization, size, speed, etc.) can be accessed via EEPROMs located on each DIMM. The DIMM ID and configuration data is read by BIOS via the PIIX4E SMBus. The I^{2}C addresses of these devices are listed in the table below. Note that the address of a device depends on which of the two memory connectors forms the interface between the Profusion carrier and the memory carrier.

5.2.3.1 I^{2}C* Accessed Features

The memory carrier contains the following I^{2}C accessible devices:

- DS1621 – Temperature sensor.
- AT24C02 – 2K EEPROM device containing FRU information.
- 2048-bit EEPROM device – DIMM configuration SEEPROM located on each DIMM installed in the system.

The DS1621 and AT24C02 devices are accessed via the BMC on the OPRF100 I/O carrier. The DIMM ID devices are read by BIOS via the PIIX4E SMBus. The I^{2}C devices are accessible at the following addresses:

Table 5-3: Memory Carrier I^{2}C* Address Map

		I^{2}C* Address	
Device	**Function**	**Mem. Slot #1 (Primary)**	**Mem. Slot #2 (Secondary)**
DS1621	Memory carrier temperature sensor.	9Ah	9Eh
AT24C02	Memory carrier FRU info.	A4h	A8h

Notes:
The device addresses are different depending on which slot the memory carrier is plugged into. The I^{2}C addresses are hard coded by the Profusion carrier.

5.2.3.1.1 DS1621 Temperature Sensor

The DS1621, when accessed via the I^{2}C bus, will provide the temperature of the carrier, as measured at the DS1621. Temperature data may be accessed via I^{2}C commands to the DS1621 device. The table below is taken from the DS1621 data sheet.

Table 5-4: Temperature Sensor Command Set

Instruction	Description	Protocol	2-Wire Bus Data After Issuing Protocol	Notes
Temperature Conversion Commands				
Read Temperature	Read last converted temperature value from temperature register.	Aah	<read 2 bytes data>	
Start Convert T	Initiates temperature conversion.	Eeh	Idle	
Stop Convert T	Halts temperature conversion.	22h	Idle	

5.2.3.1.2 AT24C02 Serial EEPROM*

The AT24C02, when accessed via the I^2C bus, will provide the following FRU information. The FRU information is read by Intel® LANDesk® Server Manager or equivalent software and is available via the LANDesk Server Manager console.

The AT24C02 SEEPROM has 256 Bytes of programmable space which is broken into four areas. The table below is a list of the areas, a description ,and the space allocated to each area.

Table 5-5: AT24C02 SEEPROM Programming Areas*

Area	Size	Description
Common Header	8 Bytes	Programming offsets to the other areas below.
Internal Use	48 Bytes	This area is reserved for general purpose use by Intel®'s server management firmware/controllers.
Board Info.	80 Bytes	Contains the board FRU information listed in the following table.
Product Info.	120 Bytes	Available for OEM use.

The table below lists the board specific FRU information that will be programmed into the board info. area.

Table 5-6: FRU Information

Board Information			
Information	**Description**	**Example**	**Notes**
Mfg. Date/Time	Time and date of board manufacture (value programmed (in hex) is the number of minutes after 0:00 hrs. 1/1/96).	000f593h (Translation shown below.) f593h = 62867 min. = 43 Days and 947 min. = Feb 12, 1996, 3:47p.m.	2
Manufacturer	Board Manufacturer	Intel	1
Board Product Name	Board Name/Description	'OPRF100 Memory Carrier'	1
Board Serial Number	Intel® Board Serial Number	N42385906	2
Board Part Number	Intel Board Part Number	714518-001	2

Notes:
1. Actual value programmed into the board.
2. Example value. Actual value will vary from board to board and/or from fab to fab.

The table below identifies the byte allocation for the AT24C02 SEEPROM. This information is useful for those who will be accessing the hardware directly for information (i.e., BIOS developers and server management software developers).

Table 5-7: SEEPROM Byte Map

Address	Length	Description	Default Value
0x00	1	Common Header Format Version	0x01
0x01	1	Internal Use Area Offset (8-byte multiples)	0x01
0x02	1	Chassis Information Area Offset (8-byte multiples)	0x00 (area not present)
0x03	1	Board Information Area Offset (8-byte multiples)	0x07
0x04	1	Product Information Area Offset (8-byte multiples)	0x00
0x05	2	Zero Padding	
0x07	1	Common Header Checksum	0xF7
0x08	48	Internal Use Area	
0x38	1	Board Information Area Format Version	0x01
0x39	1	Board Information Area Length (8-byte multiples)	0x0A
0x3A	1	Unicode Country Base	0x00

Table 5-7: SEEPROM Byte Map (Continued)

0x3B	3	Manufacture Date/Time	
0x3E	1	Board Manufacturer Type/Length Byte	0xC5
0x3F	5	Board Manufacturer (ASCII)	'Intel'
0x44	1	Product Name Type/Length Byte	0xD6
0x45	22	Product Name	'OPRF100 Memory Carrier'
0x5C	1	Board Serial Number Type/Length Byte	0xCC
0x5D	12	Board Serial Number	
0x69	1	Board Part Number Type/Length Byte	0xCA
0x6A	10	Board Part Number	
0x74	1	No More Fields Flag	0xC1
0x75	11	Zero Padding	
0x87	1	Board Information Area Checksum	
0x88	120	Product Information Area	

The AT24C02, when accessed via the I^2C bus, will provide the FRU information for the memory carrier. The following access commands are taken from the AT24C02 data sheet.

Table 5-8: AT24C02 EEPROM Command Set

Instruction	Description	Protocol	2-Wire Bus Data After Issuing Protocol	Notes
Memory Commands				
Access Memory	Reads or writes to 256-byte EEPROM memory.	17h	<write data>	
Access Config	Reads or writes configuration data to configuration register.	ACh	<write data>	

5.2.3.1.3 PC-100 Registered DIMM SEEPROM

The SDRAM configuration data is provided by a 2048-bit EEPROM device located on each DIMM in the system. These EEPROM devices allow for the reading of the SDRAM DIMM module

configuration, speed, organization, etc. This information is generally only useful to the BIOS. The individual bytes of these parts are defined as follows: (See the *PC Serial Presence Detect Specification* for individual bit information.)

Table 5-9: PC-100 DIMM SEEPROM Byte Map

Byte Number	Description
0	Defines number of bytes written into serial memory.
1	Total number of bytes of SPD memory device.
2	Fundamental memory type (FPM, EDO, SDRAM, etc).
3	Number of row addresses on this assembly.
4	Number of column addresses on this assembly.
5	Number of module rows on this assembly.
6	Data width of this assembly.
7	Data width continuation.
8	Voltage interface standard.
9	SDRAM cycle time, CL=X (highest CAS latency).
10	SDRAM access from clock (highest CAS latency).
11	DIMM configuration type (non-parity, ECC).
12	Refresh rate/type.
13	Primary SDRAM width.
14	Error checking SDRAM width.
15	Minimum clock delay back to back random column addresses.
16	Burst lengths supported.
17	Number of banks on each SDRAM device.
18	CAS latencies supported.
19	CS latency.
20	Write latency.
21	SDRAM module attributes.
22	SDRAM device attributes: general.
23	Min. SDRAM cycle time at CL X-1 (second highest CAS latency).
24	SDRAM access from clock at CL X-1 (second highest CAS latency).
25	Min SDRAM cycle time at CL X-2 (third highest CAS latency).
26	Max SDRAM access from clock at CL X-2 (third highest CAS latency).

Table 5-9: PC-100 DIMM SEEPROM Byte Map (Continued)

27	Min. row precharge time (Trp).
28	Min. row active to row active (Trrd).
29	Min. RAS to CAS delay (Trcd).
30	Min. RAS pulse width (Tras).
31	Density of each row on carrier (mixed, non-mixed sizes).
32-61	Superset information (future use).
62	SPD data revision code.
63	Checksum for bytes 0-62.
64-71	Manufacturer's JEDEC ID code per JEP-108E.
72	Manufacturing location.
73-90	Manufacturer's part number.
91-92	Revision code.
93-94	Manufacturing date.
95-98	Assembly serial number.
99-125	Manufacturer specific data.
126	Intel® specification frequency.
127	Intel specification CAS latency support.
128+	Unused storage locations.

DIMM Serial Presence Detect definitions are available in the *PC Serial Presence Detect Specification*.

Table 5-10: DIMM Address Map

DIMM	Address	DIMM	Address
Bank A, DIMM1 (J1)	0xA0	Bank C, DIMM9 (J9)	0xA0
Bank A, DIMM2 (J2)	0xA1	Bank C, DIMM10 (J10)	0xA1
Bank A, DIMM3 (J3)	0xA2	Bank C, DIMM11 (J11)	0xA2
Bank A, DIMM4 (J4)	0xA3	Bank C, DIMM12 (J12)	0xA3
Bank B, DIMM5 (J5)	0xA4	Bank D, DIMM13 (J13)	0xA4
Bank B, DIMM6 (J6)	0xA5	Bank D, DIMM14 (J14)	0xA5

Table 5-10: DIMM Address Map (Continued)

Bank B, DIMM7 (J7)	0xA6	Bank D, DIMM15 (J15)	0xA6
Bank B, DIMM8 (J8)	0xA7	Bank D, DIMM16 (J16)	0xA7

5.2.4 JTAG Scan

The OPRF100 memory carrier supports JTAG scanning of its memory board controllers. Figure 5-4: JTAG Scan Chain illustrates the scan chain on the memory carrier.

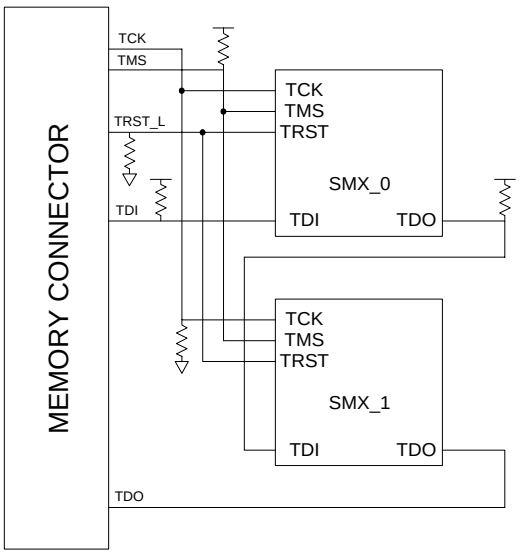


Figure 5-4: JTAG Scan Chain

5.3 Signal Descriptions

This section provides a reference to signal pins used on the memory bus connector and other signals on the memory carrier. The signal mnemonics defined here may appear in descriptive text in the document. An "_L" suffix on the signal name indicates that the signal is active-low. (Note: "_L" is the same convention used in schematics and simulation). A colon between numbers indicates a range of signals (e.g., AD[31:0]).

5.3.1 Memory Interface Bus Signals

The following tables are a summary of memory signal pins, including the signal mnemonic, electrical type, full name, and brief description. The table below shows signal electrical types:

Table 5-11: Electrical Types

Type	Description
in	Input is a standard input-only signal.
out	Totem Pole Output is a standard active driver.
o/d	Open Drain allows multiple devices to share signals as a wired-OR.

The memory interface signals supported are listed in the table below.

Table 5-12: Memory Interface Connector Signal Summary

Signal(s)	Type	Name and Description
ADDR[13:0]#	in	Memory Address Bus. These signals define the address of the location to be accessed in the DRAM. The signals are driven on two successive clock cycles to provide up to 28 bits of effective memory address.
BADDR[1:0]	In	SDRAM Bank Address. These signals indicate which of the four internal SDRAM banks is to be addressed.
RAS_L[3:0]	in	Row Address Strobe.
CAS_L[3:0]	In	Column Address Strobe.
WE_L[3:0]	In	Write Enable.
CS_L[7:0]	In	Chip Select.
BD_ID	in	Board ID. This signal is used by I^2C* devices on the memory carrier to properly decode their addresses. The Profusion* carrier should connect this pin to ground for carrier 0 and to 3.3 V for carrier 1.
MDE_L[71:0]	in/out	Memory Data and memory data check bits (ECC).
PWR_GD	In	Buffered Power Good. A buffered version of the PWRGD signal.
CLK	In	Host Clock in for the memory carrier. This is used to supply clocks to the various components on the carrier.
SYS_SCL	in/out	I^2C Clock. Clock reference for the memory carrier SM BMC I^2C interface.
SYS_SDA	in/out	I^2C Data. Serial data transfer for the memory carrier SM BMC I^2C interface.
DIMM0_SCL	in/out	DIMM0 I^2C Clock: Clock reference for the PIIX4E SMBus I^2C interface for DIMMs 0-7.
DIMM0_SDA	in/out	DIMM0 I^2C Data: Serial data transfer for the PIIX4E SMBus I^2C interface for DIMMs 0-7.
DIMM1_SCL	in/out	DIMM1 I^2C Clock: Clock reference for the PIIX4E SMBus I^2C interface for DIMMs 8-15.

Table 5-12: Memory Interface Connector Signal Summary (Continued)

DIMM1_SDA	in/out	DIMM1 I^2C Data: Serial data transfer for the PIIX4E SMBus I^2C interface for DIMMs 8-15.
TCK	in	Test Clock. Test Clock is used to clock state information and data into and out of the device during boundary scan.
TDI	in	Test Data Input. Test Input is used to serially shift data and instructions into the TAP. This signal is pulled up to 3.3 V through a 150 ohm resistor on the memory carrier.
TDO	o/d	Test Output. Test Output is used to shift data out of the device. This signal is not pulled up on the memory carrier.
TMS	in	Test Mode Select. Test Mode Select is used to control the state of the TAP controller.
TRST_L	in	Test Reset. Test Reset is used to reset the TAP controller logic.
MEM_PRES_L	Out	Memory Board Present. Used to indicate when the memory board is installed in the system.
3V_SENSE	Out	3 V Sense Line.

5.3.2 DRAM Interface Signals

The table below is a summary of DRAM interface signal pins, including the signal mnemonic and name.

Table 5-13: DRAM Interface Signal Summary

Signal(s)	Name and Description
RAS_L[3:0]	Row Address Strobe.
CAS_L[3:0]	Column Address Strobe.
WE_L[3:0]	Write Enable.
CS_L[7:0]	Chip Select.
ADDR[13:0]	Address.
BA[1:0]	SDRAM Bank Address.
MD_L[63:0]	Data Bus.
MCB_L[7:0]	Data Bus Check Bits (ECC)
DQM[7:0]	Data Mask Bits
CKE[1:0]	Clock Enable

5.3.3 Other Signals

The table below is a summary of other signal pins, including the signal mnemonic, name, and brief description.

Table 5-14: Other Signal Summary

Signal(s)	Name and Description
REG_ENA	DIMM Register Enable.
DIMM_WP	DIMM EEPROM Write Protect. Enables (or disables) DIMM EEPROM write protection.

5.4 Electrical and Environmental Specifications

This section specifies the operational parameters and physical characteristics for the memory carrier. This is a board-level specification only.

5.4.1 Electrical Specifications

This section documents the power budget for the memory carrier and pinout of both the power and signal sections of the memory interface connector.

5.4.1.1 Voltage Tolerances

The OPRF100 Profusion carrier must supply 3.3 V power to the memory carrier. The table below shows the acceptable tolerance range for these voltage levels.

Table 5-15: DC Voltage Tolerances

DC Voltage	Acceptable Tolerance
+ 3.3 V	± 5 %

5.4.2 SDRAM DIMM Connector

The table below provides the pinout for the 168-pin 72-bit registered DIMM module connector.

Table 5-16: DIMM Connector Pinout

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	/S3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vcc	48	DU	90	Vcc	132	A13
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	Vref, NC	104	DQ47	146	Vref, NC
21	CB0	63	CKE1	105	CB4	147	REGE
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE	69	DQ24	111	/CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58

Table 5-16: DIMM Connector Pinout (Continued)

30	/S0	72	DQ27	114	/S1	156	DQ59
31	DU	73	Vcc	115	/RAS	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10 (AP)	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	CK1	167	SA2
42	CK0	84	Vcc	126	A12	168	Vcc

5.4.3 Memory Interface Connector

The memory carrier uses a pin-and-socket connector for interfacing with the Profusion carrier. This connector consists of 300 pins (composed of two signal modules, with 150 pins each). The next section gives the pinouts for the signal modules. Figure 5-5: Memory Interface Connector Pin Diagram represents a top view of the connector pins. Each pin is rated at 1A.

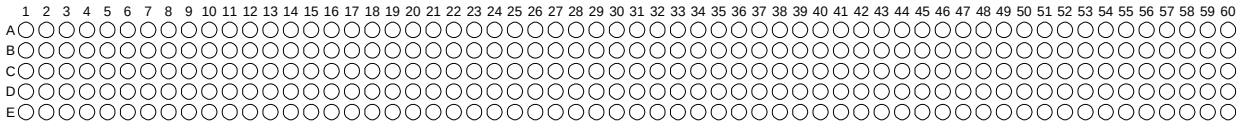


Figure 5-5: Memory Interface Connector Pin Diagram

5.4.3.1 Memory Interface Connector Pinout: Signal Section

Table 5-17: Memory Interface Connector Pinout

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
+12V (Not used)	A1	GND	B1	+12V (Not used)	C1	GND	D1	+12V (Not used)	E1

Table 5-17: Memory Interface Connector Pinout (Continued)

GND	A2	+5V (not used)	B2	GND	C2	+5V (not used)	D2	GND	E2
GND	A3	GND	B3	GND	C3	GND	D3	GND	E3
PWR_GD	A4	GND	B4	SPARECLK0	C4	GND	D4	MEM_SPARE1	E4
TRST_L	A5	GND	B5	GND	C5	GND	D5	SMX0_TDI	E5
GND	A6	SYS_SCL	B6	+3.3V	C6	SYS_SDA	D6	GND	E6
SMX1_TDO	A7	+3.3V	B7	TCK	C7	GND	D7	TMS	E7
GND	A8	DIMM0_SDA	B8	GND	C8	DIMM0_SCL	D8	+3.3V	E8
RAS_L(0)	A9	+3.3V	B9	RAS_L(1)	C9	GND	D9	CAS_L(1)	E9
GND	A10	CAS_L(0)	B10	GND	C10	WE_L(0)	D10	+3.3V	E10
WE_L(1)	A11	+3.3V	B11	CS_L(1)	C11	GND	D11	CS_L(2)	E11
GND	A12	CS_L(0)	B12	GND	C12	MDE_L(0)	D12	+3.3V	E12
CS_L(3)	A13	+3.3V	B13	MDE_L(1)	C13	GND	D13	MDE_L(3)	E13
GND	A14	MDE_L(2)	B14	GND	C14	MDE_L(5)	D14	+3.3V	E14
MDE_L(4)	A15	+3.3V	B15	MDE_L(6)	C15	GND	D15	MDE_L(8)	E15
GND	A16	MDE_L(7)	B16	GND	C16	MDE_L(10)	D16	+3.3V	E16
MDE_L(9)	A17	+3.3V	B17	MDE_L(11)	C17	GND	D17	MDE_L(13)	E17
GND	A18	MDE_L(12)	B18	GND	C18	MDE_L(15)	D18	+3.3V	E18
MDE_L(14)	A19	+3.3V	B19	MDE_L(64)	C19	GND	D19	MDE_L(66)	E19
GND	A20	MDE_L(65)	B20	GND	C20	MDE_L(16)	D20	+3.3V	E20
MDE_L(67)	A21	+3.3V	B21	MDE_L(17)	C21	GND	D21	MDE_L(19)	E21
GND	A22	MDE_L(18)	B22	GND	C22	MDE_L(21)	D22	+3.3V	E22
MDE_L(20)	A23	+3.3V	B23	MDE_L(22)	C23	GND	D23	MDE_L(24)	E23
GND	A24	MDE_L(23)	B24	GND	C24	MDE_L(26)	D24	+3.3V	E24
MDE_L(25)	A25	+3.3V	B25	MDE_L(27)	C25	GND	D25	MDE_L(29)	E25
GND	A26	MDE_L(28)	B26	GND	C26	MDE_L(31)	D26	GND	E26
MDE_L(30)	A27	GND	B27	ADDR (0)	C27	GND	D27	ADDR (1)	E27
GND	A28	ADDR (2)	B28	GND	C28	ADDR (3)	D28	+3.3V	E28
ADDR(4)	A29	+3.3V	B29	ADDR (5)	C29	GND	D29	MEM_SPARE2	E29
BADDR (1)	A30	GND	B30	GND	C30	GND	D30	BADDR (0)	E30
GND	A31	GND	B31	CLK	C31	GND	D31	GND	E31
ADDR (7)	A32	GND	B32	GND	C32	GND	D32	ADDR (6)	E32
ADDR (8)	A33	+3.3V	B33	ADDR (10)	C33	GND	D33	MEM_SPARE3	E33
GND	A34	ADDR (12)	B34	GND	C34	ADDR (9)	D34	+3.3V	E34
ADDR (13)	A35	GND	B35	MDE_L(32)	C35	GND	D35	ADDR (11)	E35

Table 5-17: Memory Interface Connector Pinout (Continued)

GND	A36	MDE_L(34)	B36	GND	C36	MDE_L(33)	D36	GND	E36
MDE_L(35)	A37	+3.3V	B37	MDE_L(37)	C37	GND	D37	MDE_L(36)	E37
GND	A38	MDE_L(39)	B38	GND	C38	MDE_L(38)	D38	+3.3V	E38
MDE_L(40)	A39	+3.3V	B39	MDE_L(42)	C39	GND	D39	MDE_L(41)	E39
GND	A40	MDE_L(44)	B40	GND	C40	MDE_L(43)	D40	+3.3V	E40
MDE_L(45)	A41	+3.3V	B41	MDE_L(47)	C41	GND	D41	MDE_L (46)	E41
GND	A42	MDE_L(69)	B42	GND	C42	MDE_L(68)	D42	+3.3V	E42
MDE_L(70)	A43	+3.3V	B43	MDE_L(48)	C43	GND	D43	MDE_L(71)	E43
GND	A44	MDE_L(50)	B44	GND	C44	MDE_L(49)	D44	+3.3V	E44
MDE_L(51)	A45	+3.3V	B45	MDE_L(53)	C45	GND	D45	MDE_L(52)	E45
GND	A46	MDE_L(55)	B46	GND	C46	MDE_L(54)	D46	+3.3V	E46
MDE_L(56)	A47	+3.3V	B47	MDE_L(58)	C47	GND	D47	MDE_L(57)	E47
GND	A48	MDE_L(60)	B48	GND	C48	MDE_L (59)	D48	+3.3V	E48
MDE_L(61)	A49	+3.3V	B49	MDE_L(63)	C49	GND	D49	MDE_L(62)	E49
GND	A50	CS_L(5)	B50	GND	C50	CS_L(4)	D50	+3.3V	E50
CS_L(6)	A51	+3.3V	B51	CAS_L(3)	C51	GND	D51	CS_L(7)	E51
GND	A52	RAS_L(3)	B52	GND	C52	CAS_L(2)	D52	+3.3V	E52
RAS_L(2)	A53	GND	B53	WE_L(2)	C53	GND	D53	WE_L(3)	E53
MEM_SPARE4	A54	RESV	B54	GND	C54	RESV	D54	+3.3V	E54
GND	A55	GND	B55	TM(4)	C55	BD_ID	D55	GND	E55
RESV	A56	GND	B56	3V_SENSE	C56	GND	D56	RESV	E56
DIMM1_SCL	A57	RESV	B57	GND	C57	RESV	D57	DIMM1_SDA	E57
GND	A58	GND	B58	MEM_PRES_L	C58	GND	D58	GND	E58
GND	A59	+5V (not used)	B59	GND	C59	+5V (not used)	D59	GND	E59
+12V (Not used)	A60	GND	B60	+12V (Not used)	C60	GND	D60	+12V (Not used)	E60

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6. Midplane

This chapter discusses the architecture and external interfaces of the OPRF100 midplane. The midplane is used as part of the OPRF100 MP board set to provide power distribution from two to three power supplies, and to perform data and control signal distribution between the various boards of the board set.

Features

Power Distribution Subsystem Features:

- Power supply connectors (for 2+1 power supply, hot swap)
- CPU, I/O, and memory signal interconnections
- Bulk decoupling capacitors for 5 VDC loads and 12 VDC loads
- 3.3 VDC and 5 VDC margining circuit
- Peripheral power connector
- PS_ON – controlled by front panel controller (FPC)
- AC_OK (disables PS_ON when AC voltage to power supplies is less than 180 VAC)

Non-power Sub-system Features:

- I^2C* bus for PS_Fault, Predictive_Fail, AC_OK, and PS_Present indicators
- I^2C signal connections to LVDS backplane (included in peripheral power connector)
- 3-pin I^2C connector

6.1 Functional Description

6.1.1 Placement Diagrams

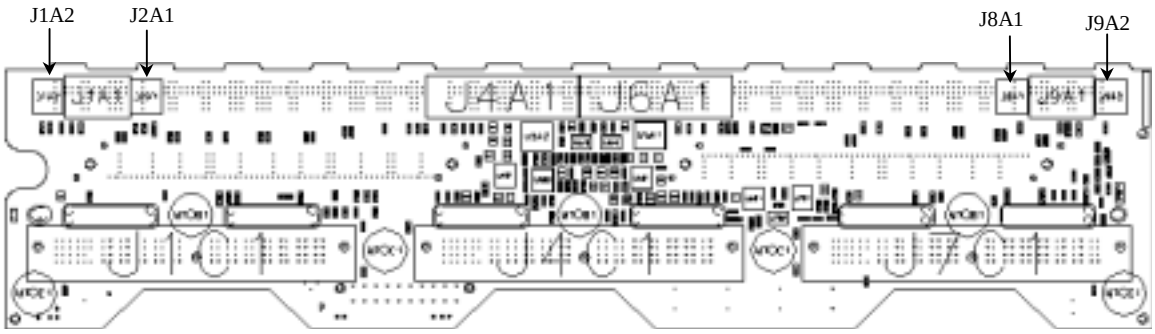

Figure 6-1: Placement Diagram (primary side)

Table 6-1: Reference Designators (primary side)

Reference Designator	Name and Description
J1A2, J2A1, J8A1, J9A2	Power from midplane to I/O carrier
J1A1, J4A1, J6A1, J9A1	Grand connector from Profusion* carrier to I/O carrier
J1C1	Power supply connector #1
J4C1	Power supply connector #2
J7C1	Power supply connector #3

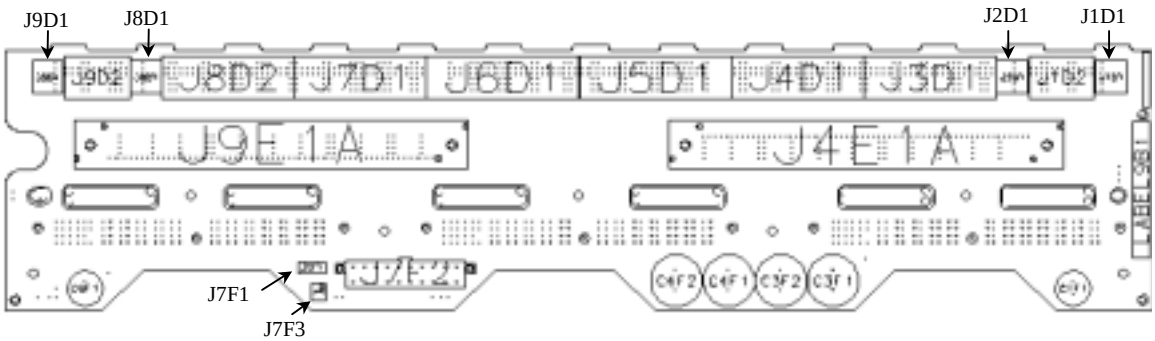

Figure 6-2: Placement Diagram (secondary side)

Table 6-2: Reference Designators (secondary side)

Reference Designator	Name and Description
J9E1A (J9E1A/B), J4E1A (J4E1A/B)	Memory Module Connectors
J7F2	Peripheral Bay Power/I^2C* Connector
J1D1, J2D1, JAD1, J9D1	Power from midplane to Profusion* Carrier

Table 6-2: Reference Designators (secondary side) (Continued)

J1D2, J3D1, J4D1, J5D1, J6D1, J7D1, J8D2, J9D2	Grand connector from I/O Carrier To Profusion Carrier
J7F3	Force AC_OK Signal Jumper
J7F1	External I^2C Connector

6.1.2 DC Output Power Supply Voltages

The table below lists power supply voltages that are distributed by the midplane to the rest of the system, in a 2+1 power supply redundant configuration:

Table 6-3: Available Power Supply Voltages

DC Voltage	Regulation	Ripple/ Noise pk-pk	Max. Continuous Load	OCP Limits	OVP Limits	Midplane BP Bulk Cap.
+3.3 V VCC3	3.25 V min 3.35 V max	1.5%	61.0 A	70.4 A min 82.8 A max	4.0 V min 4.5 V max	None
+5 V VCC5	4.9 V min 5.1 V max	1%	68.0 A	79.2 A min 93.6 A max	6.2 V min 6.5 V max	13.6 mF ±20%
+12 V[1] VCC12	11.76 V min 12.24 V max	1%	56.0 A (67.0 A pk)	78 A min 90 A max	14.5 V min 15.5 V max	13.8 mF±20%
-12 V (12VCC)[1]	-12.6 V min - 11.4 V max	1%	1.0 A	1.1 A min 1.3 A max	NA	NA
+5 V Standby 5VSTNDBY	4.75 V min 5.25 V max	2%	1.75 A	NA	NA	1 µF ±20%
+15 V Bias VBIAS	12 V min. 18 V max.	5%	200 mA	NA	NA	1 µF ±20%

Notes:

1. The regulation of –12 V to the front panel connector is +/- 10%.

6.1.3 5 V Standby

The power supplies provide a 5 V standby power source (5VSTNDBY). 5VSTNDBY is a low power 5 VDC supply, which is active whenever the system is plugged into AC power. 5VSTNDBY is used in several places on the midplane as follows: 5 V Quick Discharge circuit, I/O Connector Header, Power Good Circuit, and I²C Bus Circuits.

6.1.4 Power Supply Enable/Disable

This signal, PS_ON, is also known as Power_ON or PWR_ON_Supplies. It is a control signal that originates from the front panel, goes to the midplane, and then to the power supply. It is directly connected to pin 44 (Power_ON) of each power supply. A special case exists when the AC_OK bypass jumper is installed, in which case PS_ON directly follows PS_PWR_ON.

PS_ON is asserted (logic high) when:

- Signal *PS_PWR_ON* is asserted,
- and/or AC_OK signal is asserted.

PS_ON is deasserted (logic low) when:

- Signal *PS_PWR_ON* is deasserted,
- and/or AC_OK signal is deasserted.

Table 6-4: PS_ON Signal Logic Levels

PS_ON Signal	Voltage	Current
Asserted, Logic High, Power Supply Enabled	4 V min.	1.5 mA min source to the power supplies.
Deasserted, Logic Low, Power Supply Disabled	2 V max. or open circuit	0 mA (series ORing diode and pull-down resistor, internal to power supplies).

6.1.5 Remote Sense and Margining Circuit Connections

To maintain the power supply load regulation, voltage remote sensing is provided for the +3.3 VDC, +5 VDC, +12 VDC, and Common Ground Return. The 5 V remote sense is located on the I/O baseboard near the PCI slots. The 3.3 V remote sense is located on the memory carrier and wired OR on the midplane. The +12 V remote sense is located on the Profusion* carrier. Each remote sense line has a 100-ohm sense resistor located on the midplane so power can be applied safely in the absence of any of the above boards, which contain a remote sense resistor.

Table 6-5: Remote Sense Connections

Voltage	Remote Sense Connection	Power Supply Connector Pin (power supply signal)	Board Under Sensing
3.3 V	Buffered individual for each power supply	+3.3 V SENSE (Pin 3B)	Memory Carrier
5 V	Buffered individual for each power supply	+5 V SENSE (Pin 4B)	I/O Carrier
12 V	Direct common for all three power supplies	+12 V SENSE (Pin 5C)	Profusion* Carrier
GND	Direct common for all three power supplies	REMOTE SENSE RETURN (Pin 5D)	Midplane

The margining circuit is provided to give the FPC, through the I^2C bus, the capabilities to adjust the +3.3 V and +5 V supply by ±5% if needed. The margining circuit is coupled with the remote sense circuit as shown in Figure 6-3: 3.3 V and 5 V Remote Sense and Margining Circuit.

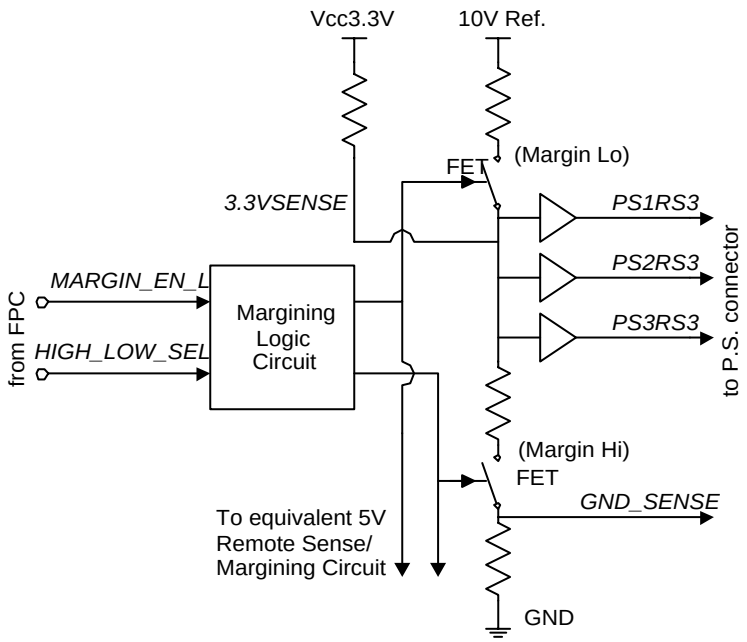

Figure 6-3: 3.3 V and 5 V Remote Sense and Margining Circuit

Table 6-6: Margining Control Input Signals Truth Table

MARGIN_EN_L	HIGH_LOW_SEL	3.3 V AND 5 V MARGIN
low (0)	low (0)	high (+5%)
low (0)	high (1)	low (-5%)
high (1) or open	low (0)	NONE (Nominal)
high (1) or open	high(1)	NONE (Nominal)

6.1.6 Load Share Connections

The power share functions are internal to the 750 W power supplies, which are designed to work in a 2+1 redundant, hot-swap configuration. The only load share outside connections on the mid-plane are as follows:

For 3.3 V, pin 1A (+3.3V_LS) of each power supply connector are connected together.

For 5 V, pin 4A (+5V_LS) of each power supply connector are connected together.

For 12 V, pin 1D (+12V_LS) of each power supply connector are connected together.

6.1.7 Power Good Circuit

The power good function originates on the midplane. The PGOODs of each power supply (pin 2D) are ORed together and that signal inputs a control circuit that generates a PWR_GOOD signal after an approximately 500 ms fixed delay. This delay is provided to ensure a secure PWR_GOOD even in case of a quick turn off/on of the front panel power switch. The PWR_GOOD is asserted when at least one power supply's PGOOD is asserted. The logic levels for the system PWR_GOOD signal are shown in the table below.

Table 6-7: System PWR_GOOD Logic Levels

PWR_GOOD SIGNAL	VOLTAGE	CURRENT
LOW STATE, DEASSERTED	0.4 V max.	4 mA min sink current
HIGH STATE, ASSERTED	3.5 V min.	200 µA max source current

When no PGOOD is asserted from any power supply, the PWR_GOOD will be deasserted.

6.1.8 5 V Quick Discharge Circuit

The 5 V quick discharge circuit is provided to speed up the discharge time of the +5 V supply voltage at power off. The circuit is sensing VCC5 and at power off it intrudes a 5Ω resistor across VCC5. This is needed because the large quantity of decoupling capacitors on VCC5 requires too long to discharge in case of a quick off and on situation. During normal operation, this 5Ω resistor is disconnected.

6.1.9 Power Supply Present

Each power supply output signal PSx_PRESENT (pin 2A) is used by the FPC to sense the number of power supplies present in the system (whether operational or not). Inside each power supply this pin is grounded. On the midplane, each of the three signals PS1_PRESENT, PS2_PRESENT, and PS3_PRESENT has a pull-up resistor which, leads to the FPC through the I²C bus. A logic low (0) indicates the power supply is present, while logic high (1) indicates the power supply is not present.

6.1.10 Power Supply Predictive Failure

Each power supply output signal PRED_FAIL_PSx (pin 4C) is used to alert the FPC in case the power supply is likely to fail soon due to its poorly performing fan (having slower RPMs than nominal). Logic high (1) indicates upcoming failure, while logic low (0) indicates a normal fan situation. On the midplane, each of the signals PRED_FAIL_PS1, PRED_FAIL_PS2 and PRED_FAIL_PS3 are connected to the FPC through the I²C bus. The signal going high will not cause the power supply to shut down, but will cause the FPC to warn the user about upcoming power supply failure. In addition, the power supply's yellow LED will blink.

6.1.11 AC OK Circuit

Each power supply output signal AC_OK_PSx (pin 3D) is used to disable the power supplies if the AC voltage drops below 180 VAC. Logic high (1) indicates AC is below 180 VAC, while logic low (0) indicates AC above 180 VAC. At least two power supplies in the system have to assert AC_OK_PSx in order for PS_ON to become asserted. On the midplane each of the signals AC_OK_PS1, AC_OK_PS2 and AC_OK_PS3 are inverted (to AC_OKx_L), and then connected to the FPC through the I²C bus.

The installation of a jumper on J9B1 disables the function of the AC_OK circuit. This will allow one power supply to assert PS_ON and power up the board set.

Table 6-8: Power Enable Override by AC OK Circuit

Number of Supplies Present	Number of AC_OK Asserted	POWER_ON_SUPPLIES
1	0	FORCED LOW
1	1	FORCED LOW

Table 6-8: Power Enable Override by AC OK Circuit (Continued)

2	1	FORCED LOW
2	2	Unaffected
3	1	FORCED LOW
3	2	Unaffected
3	3	Unaffected

6.1.12 Power Supply Fault

PS_FAULT is an output signal from each power supply (connector pin 3C). When it is high (1), it indicates that the power supply is operating normally and when it goes low (0) it indicates power supply failure. These signals are connected to the FPC through the I²C bus.

Table 6-9: PS_FAULT Signal Logic Levels

PS_FAULT SIGNAL	VOLTAGE/TTL LEVEL	CURRENT
DEASSERTED STATE (FAULT)	0.4 V max.	4 mA min sink current
ASSERTED STATE (NO FAULT)	3.5 V min.	200 µA max source current

The logical relationship between the signals PWR_GOOD, PRED_FAIL_PS, PS_FAULT, and POWER_ON are outlined in the table below.

Table 6-10: PWR_GOOD, PRED_FAIL_PS, PS_FAULT, AC_OK, and POWER_ON Relationships

CONDITIONS	PWR_GOOD Output H = power good	PRED_FAIL_PSx Output H = pred. failure	PSx_FAULT Output H = power supply OK	AC_OK_L Output L= AC >180V (from supply)	PS_ON Power Supply Input (pin 44) H = power supply enabled
No AC Power	L	L	L		L or H
AC In/Stdby On	L	L	H	L	L
DC Outputs OK	H	L	H	L	H

Table 6-10: PWR_GOOD, PRED_FAIL_PS, PS_FAULT, AC_OK, and POWER_ON Relationships

Power Supply Failure	L	L	L	L	H
Current Limit	L	L	H	L	H
Predictive Failure	H	H	H	L	H

6.1.13 I²C* Communication Circuit

The midplane provides an I²C data link to support each power supply's field replacement unit (FRU) signals: PS_SCL (serial clock, pin 23) and PS_SDA (serial data, pin 41). This data link is designed to enable the FPC to keep track of each power supply.

6.2 I²C* Interface

6.2.1 Power Management

The I²C bus is a part of the server management system. The part of the system located on the midplane was designed to perform the following tasks:

- Link the power supply power management circuit to the FPC.
- Report (read) power supply x fault (PSx_FAULT).
- Report (read) power supply x presence (PSx_PRESENT).
- Reports (read) power supply x predictive failure (PRED_FAIL_PSx).
- Reports (read) power supply x AC input status (AC_OKx_L).
- Asserts (write) to the margining circuit, MARGIN_EN_L, and to HIGH_LOW_SEL to change the current status.
- Read data from the EEPROM FRU located within the power supplies (part number, model, revision and specification information).

6.2.2 Other Functions

- Link the EEPROM circuit to the FPC, located in the front panel, via the I²C bus.
- Store the midplane's serial and model numbers, revision level, and specification on the EEPROM FRU.
- Retrieve data via the I²C bus to the microcontroller.

6.3 Power Management Communication

6.3.1 Power Supply Management Indication Circuit

The I²C two-wire communication is initiated at the microcontroller, located on the front panel board, and is connected to the midplane via the grand connector (J1D2 pins #D7 (clock and F6 (data)). This serial link employs I/O expanders (PCF8574) to convert the serial data to logic states. Each time the microcontroller initiates the communication with the PCF8574, it sends a start condition bit followed by its family address, and the last bit is the read/write bit. The following string is the expander's unique address: S01000000 (S stands for starting condition), or 40H in hex. Since the last bit is "0" the microcontroller will "write" out of the ports. See the table below.

Table 6-11: Power Management, Hex Address 40

	Port Hex Address	Signal		Description	OK/No Fault Condition	Fault Condition	Power Supply Present	Power Supply Not Present
P0	01H	PS1_FAULT	I	Power supply 1 fault signal	High	Low		
P1	02H	PSI_PRESENT_L	I	Power supply 1 present			Low	High
P2	04H	PS2_FAULT	I	Power supply 2 fault signal	High	Low		
P3	08H	PS2_PRESENT_L	I	Power supply 2 present			Low	High
P4	10H	PS3_FAULT	I	Power supply 3 fault signal	High	Low		
P5	20H	PS3_PRESENT_L	I	Power supply 3 present			Low	High
P6	40H	NOT USED						
P7	80H	NOT USED						

An additional I/O expander is used to carry out the power supply management circuit. See the table below for further details.

Table 6-12: Power Management, Hex Address 42

Port	Port Hex Address	Signal	I/O	Function	Logic State for OK Condition	Logic State for Fault/Upcoming Failure
P0	01H	PRED_FAIL_PS3	I	Alerts Upcoming Failure	Low	High
P1	02H	PRED_FAIL_PS2	I	Alerts Upcoming Failure	Low	High
P2	04H	PRED_FAIL_PS1	I	Alerts Upcoming Failure	Low	High
P3	08H	AC_OK1_L	I	Indicates valid AC voltage level	High	Low
P4	10H	AC_OK2_L	I	Indicates valid AC voltage level	High	Low
P5	20H	AC_OK3_L	I	Indicates valid AC voltage level	High	Low
P6	40H	MARGIN_EN_L	O		See	
P7	80H	HIGH_LOW_SF1	O		See	

6.4 Connector Description

6.4.1 Grand Connector Description

The grand connector is the junction of the midplane with both the I/O carrier and the Profusion carrier. The I/O and Profusion carriers meet the midplane in the same plane relative to each other, at 90 degrees to the midplane. Midplane HDM connectors provide the interconnection.

The grand connector consists of two segments of 288 pins for memory interconnection, one 432-pin midplane connection to the I/O carrier for I/O bus and front panel signals, and midplane power modules.

6.4.1.1 Grand Connector Pinout

Inserted from the primary side of the board, pins extend through to make contact with the I/O baseboard on the secondary side.

Table 6-13: CPU and I/O (J1D2)

	A	B	C	D	E	F
1	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
2	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
3	PASS_THROUGH	GND	VCC5STBY	PASS_THROUGH	GND	VCC5STBY
4	PASS_THROUGH	GND	PASS_THROUGH	VCC5STBY	GND	VCC5STBY
5	PASS_THROUGH	GND	PASS_THROUGH	VCC5STBY	GND	PASS_THROUGH
6	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	I2C_FPC_SDA
7	PS_PWR_ON	GND	PASS_THROUGH	I2C_FPC_SCL	GND	PASS_THROUGH
8	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
9	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
10	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
11	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
12	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH

Table 6-14: CPU and I/O (J9D2)

	A	B	C	D	E	F
1	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
2	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
3	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
4	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
5	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
6	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
7	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
8	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
9	PASS_THROUGH	GND	-12VCC	PASS_THROUGH	GND	PASS_THROUGH
10	-12VCC	GND	-12VCC	PASS_THROUGH	GND	PASS_THROUGH
11	-12VCC	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
12	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH

Table 6-15: CPU and I/O (J6D1)

	A	B	C	D	E	F
1	PASS_THROUGH	GND	PASS_THROUGH	PWR_GOOD	GND	PASS_THROUGH
2	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
3	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
4	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
5	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
6	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
7	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
8	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
9	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
10	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
11	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
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15	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
16	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
17	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
18	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
19	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
20	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
21	12V_RS	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
22	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
23	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
24	5V_SENSE	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH

Table 6-16: CPU and I/O (J5D1)

	A	B	C	D	E	F
1	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH

Table 6-16: CPU and I/O (J5D1) (Continued)

2	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
3	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
4	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
5	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
6	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
7	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
8	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
9	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
10	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
11	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
12	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
13	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
14	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
15	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
16	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
17	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
18	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
19	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
20	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
21	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
22	I2C_GLOBAL_SDA	GND	I2C_GLOBAL_SCL	PASS_THROUGH	GND	PASS_THROUGH
23	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH
24	PASS_THROUGH	GND	PASS_THROUGH	PASS_THROUGH	GND	PASS_THROUGH

Table 6-17: Grand Connector to Mem 1 (J4D1)

	A	**B**	**C**	**D**	**E**	**F**
1	SYS_SCL	GND	JTAG_TDI	SPARECLK0	GND	DIMM0_SCL
2	GND	GND	JTAG_TCK	GND	GND	GND
3	CAS_L1	GND	SYS_SDA	RAS_L1	GND	RAS_L0
4	WE_L0	GND	CAS_L0	JTAG_TDO	GND	MEM_PWR_GD

Table 6-17: Grand Connector to Mem 1 (J4D1) (Continued)

	A	B	C	D	E	F
5	CS_L2	GND	JTAG_TMS	CS_L1	GND	WE_L1
6	DIMM0_SDA	GND	MDE_L0	TRST_L	GND	CS_L0
7	MDE_L3	GND	N/C	MDE_L1	GND	CS_L3
8	MDE_L5	GND	MDE_L2	GND	GND	MEM_SPARE1
9	MDE_L8	GND	N/C	MDE_L6	GND	MDE_L4
10	N/C	GND	MDE_L10	N/C	GND	MDE_L7
11	MDE_L13	GND	MDE_L11	N/C	GND	MDE_L9
12	MDE_L15	GND	N/C	MDE_L12	GND	N/C
13	CB_L2	GND	N/C	CB_L0	GND	MDE_L14
14	N/C	GND	MDE_L16	N/C	GND	CB_L1
15	MDE_L19	GND	N/C	MDE_L17	GND	CB_L3
16	MDE_L21	GND	N/C	MDE_L18	GND	N/C
17	MDE_L24	GND	MDE_L22	N/C	GND	MDE_L20
18	N/C	GND	MDE_L26	MDE_L23	GND	N/C
19	MDE_L29	GND	N/C	MDE_L27	GND	MDE_L25
20	N/C	GND	MDE_L31	N/C	GND	MDE_L28
21	MA0(1)	GND	N/C	MA0(0)	GND	MDE_L30
22	MA0(2)	GND	MA0(3)	N/C	GND	N/C
23	N/C	GND	N/C	MA0(5)	GND	MA0(4)
24	MBA0	GND	MEM_SPARE3	GND	GND	MBA1

Table 6-18: Grand Connector to Mem 1 (J3D1)

	A	B	C	D	E	F
1	N/C	GND	GND	CLK0	GND	MEM_SPARE2
2	MA0(6)	GND	N/C	GND	GND	MA0(7)
3	GND	GND	N/C	MA0(10)	GND	MA0(8)
4	MA0(9)	GND	N/C	MA0(12)	GND	N/C
5	MA0(11)	GND	MDE_L32	N/C	GND	MA0(13)
6	MDE_L33	GND	N/C	MDE_L34	GND	N/C

Table 6-18: Grand Connector to Mem 1 (J3D1) (Continued)

7	MDE_L36	GND	MDE_L37	N/C	GND	MDE_L35
8	GND	GND	MDE_L38	N/C	GND	MDE_L39
9	MDE_L41	GND	N/C	MDE_L42	GND	MDE_L40
10	N/C	GND	MDE_L43	N/C	GND	MDE_L44
11	MDE_L46	GND	MDE_L47	N/C	GND	MDE_L45
12	CB_L4	GND	N/C	CB_L5	GND	N/C
13	CB_L7	GND	MDE_L48	N/C	GND	CB_L6
14	N/C	GND	GND	MDE_L49	GND	MDE_L50
15	MDE_L52	GND	MDE_L53	N/C	GND	MDE_L51
16	MDE_L54	GND	N/C	MDE_L55	GND	N/C
17	MDE_L57	GND	MDE_L58	N/C	GND	MDE_L56
18	N/C	GND	MDE_L59	N/C	GND	MDE_L60
19	MDE_L62	GND	N/C	MDE_L63	GND	MDE_L61
20	CS_L4	GND	CS_L5	N/C	GND	N/C
21	CS_L7	GND	MEM_SPARE4(Used for MEM_PRES)	CAS_L3	GND	CS_L6
22	BD_ID	GND	CAS_L2	N/C	GND	RAS_L3
23	WE_L3	GND	GND	WE_L2	GND	RAS_L2
24	DIMM1_SDA	GND	DIMM1_SCL	TM4	GND	N/C

Table 6-19: Grand Connector to Mem 2 (J8D2)

	A	**B**	**C**	**D**	**E**	**F**
1	S_SYS_SCL	GND	S_JTAG_TDI	S_SPARECLK0	GND	S_DIMM0_SCL
2	GND	GND	S_JTAG_TCK	GND	GND	GND
3	S_CAS_L1	GND	S_SYS_SDA	S_RAS_L1	GND	S_RAS_L0
4	S_WE_L0	GND	S_CAS_L0	S_JTAG_TDO	GND	S_MEM_PWR_GD
5	S_CS_L2	GND	S_JTAG_TMS	S_CS_L1	GND	S_WE_L1
6	S_DIMM0_SDA	GND	S_MDE_L0	S_TRST_L	GND	S_CS_L0
7	S_MDE_L3	GND	N/C	S_MDE_L1	GND	S_CS_L3
8	S_MDE_L5	GND	S_MDE_L2	GND	GND	S_MEM_SPARE1

Table 6-19: Grand Connector to Mem 2 (J8D2) (Continued)

9	S_MDE_L8	GND	N/C	S_MDE_L6	GND	S_MDE_L4
10	N/C	GND	S_MDE_L10	N/C	GND	S_MDE_L7
11	S_MDE_L13	GND	S_MDE_L11	N/C	GND	S_MDE_L9
12	S_MDE_L15	GND	N/C	S_MDE_L12	GND	N/C
13	S_CB_L2	GND	N/C	S_CB_L0	GND	S_MDE_L14
14	N/C	GND	S_MDE_L16	N/C	GND	S_CB_L1
15	S_MDE_L19	GND	N/C	S_MDE_L17	GND	S_CB_L3
16	S_MDE_L21	GND	N/C	S_MDE_L18	GND	N/C
17	S_MDE_L24	GND	S_MDE_L22	N/C	GND	S_MDE_L20
18	N/C	GND	S_MDE_L26	S_MDE_L23	GND	N/C
19	S_MDE_L29	GND	N/C	S_MDE_L27	GND	S_MDE_L25
20	N/C	GND	S_MDE_L31	N/C	GND	S_MDE_L28
21	MA1(1)	GND	N/C	MA1(0)	GND	S_MDE_L30
22	MA1(2)	GND	MA1(3)	N/C	GND	N/C
23	N/C	GND	N/C	MA1(5)	GND	MA1(4)
24	S_MBA0	GND	S_MEM_SPARE3	GND	GND	S_MBA1

Table 6-20: Grand Connector to Mem 2 (J7D1)

	A	**B**	**C**	**D**	**E**	**F**
1	N/C	GND	GND	CLK0	GND	S_MEM_SPARE2
2	MA1(6)	GND	N/C	GND	GND	MA1(7)
3	GND	GND	N/C	MA1(10)	GND	MA1(8)
4	MA1(9)	GND	N/C	MA1(12)	GND	N/C
5	MA1(11)	GND	S_MDE_L32	N/C	GND	MA1(13)
6	S_MDE_L33	GND	N/C	S_MDE_L34	GND	N/C
7	S_MDE_L36	GND	S_MDE_L37	N/C	GND	S_MDE_L35
8	GND	GND	S_MDE_L38	N/C	GND	S_MDE_L39
9	S_MDE_L41	GND	N/C	S_MDE_L42	GND	S_MDE_L40
10	N/C	GND	S_MDE_L43	N/C	GND	S_MDE_L44
11	S_MDE_L46	GND	S_MDE_L47	N/C	GND	S_MDE_L45

Table 6-20: Grand Connector to Mem 2 (J7D1) (Continued)

12	S_CB_L4	GND	N/C	S_CB_L5	GND	N/C
13	S_CB_L7	GND	S_MDE_L48	N/C	GND	S_CB_L6
14	N/C	GND	GND	S_MDE_L49	GND	S_MDE_L50
15	S_MDE_L52	GND	S_MDE_L53	N/C	GND	S_MDE_L51
16	S_MDE_L54	GND	N/C	S_MDE_L55	GND	N/C
17	S_MDE_L57	GND	S_MDE_L58	N/C	GND	S_MDE_L56
18	N/C	GND	S_MDE_L59	N/C	GND	S_MDE_L60
19	S_MDE_L62	GND	N/C	S_MDE_L63	GND	S_MDE_L61
20	S_CS_L4	GND	S_CS_L5	N/C	GND	N/C
21	S_CS_L7	GND	S_MEM_SPARE4	S_CAS_L3	GND	S_CS_L6
22	S_BD_ID	GND	S_CAS_L2	N/C	GND	S_RAS_L3
23	S_WE_L3	GND	GND	S_WE_L2	GND	S_RAS_L2
24	S_DIMM1_SDA	GND	S_DIMM1_SCL	S_TM4	GND	S_MEM_PRES

6.4.1.1.1 Grand Connector Power Modules

Table 6-21: Primary Side (J1A2)

	A	C	E
1	VCC12V	VCC5	VCC12V
2	VCC12V	VCC5	VCC12V
3	VCC12V	VCC5	VCC12V
4	VCC12V	VCC5	VCC12V

Table 6-22: Primary Side (J2A1)

	A	C	E
1	VCC12V	VCC5	VCC3V
2	VCC12V	VCC5	VCC3V
3	VCC12V	VCC5	VCC3V
4	VCC12V	VCC5	VCC3V

Table 6-23: Primary Side (J8A1)

	A	C	E
1	VCC12V	VCC5	VCC3V
2	VCC12V	VCC5	VCC3V
3	VCC12V	VCC5	VCC3V
4	VCC12V	VCC5	VCC3V

Table 6-24: Primary Side (J9A2)

	A	C	E
1	VCC12V	VCC5	VCC5
2	VCC12V	VCC5	VCC5
3	VCC12V	VCC5	VCC5
4	VCC12V	VCC5	VCC5

Table 6-25: Secondary Side (J9D1)

	A	C	E
1	VCC12V	VCC5	VCC12V
2	VCC12V	VCC5	VCC12V
3	VCC12V	VCC5	VCC12V
4	VCC12V	VCC5	VCC12V

Table 6-26: Secondary Side (J8D1)

	A	C	E
1	VCC3V	VCC5	VCC12V
2	VCC3V	VCC5	VCC12V
3	VCC3V	VCC5	VCC12V

Table 6-26: Secondary Side (J8D1) (Continued)

4	VCC3V	VCC5	VCC12V

Table 6-27: Secondary Side (J2D1)

	A	C	E
1	VCC3V	VCC5	VCC12V
2	VCC3V	VCC5	VCC12V
3	VCC3V	VCC5	VCC12V
4	VCC3V	VCC5	VCC12V

Table 6-28: Secondary Side (J1D1)

	A	C	E
1	VCC5V	VCC5	VCC12V
2	VCC5V	VCC5	VCC12V
3	VCC5V	VCC5	VCC12V
4	VCC5V	VCC5	VCC12V

6.4.1.2 Memory Board Connector

Table 6-29: Memory Board 1 Interface Connector (J4E1)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
+12V	A1	GND	B1	+12V	C1	GND	D1	+12V	E1
GND	A2	+5V	B2	GND	C2	+5V	D2	GND	E2
GND	A3	GND	B3	GND	C3	GND	D3	GND	E3
MEM_PWR_GD	A4	GND	B4	SPARECLK0	C4	GND	D4	MEM_SPARE1	E4
TRST_L	A5	GND	B5	GND	C5	GND	D5	JTAG_TDI	E5

Table 6-29: Memory Board 1 Interface Connector (J4E1) (Continued)

GND	A6	SYS_SCL	B6	+3.3V	C6	SYS_SDA	D6	GND	E6
JTAG_TDO	A7	+3.3V	B7	JTAG_TCK	C7	GND	D7	JTAG_TMS	E7
GND	A8	DIMM0_SDA	B8	GND	C8	DIMM0_SCL	D8	+3.3V	E8
RAS_L(0)	A9	+3.3V	B9	RAS_L(1)	C9	GND	D9	CAS_L(1)	E9
GND	A10	CAS_L(0)	B10	GND	C10	WE_L(0)	D10	+3.3V	E10
WE_L(1)	A11	+3.3V	B11	CS_L(1)	C11	GND	D11	CS_L(2)	E11
GND	A12	CS_L(0)	B12	GND	C12	MDE_L(0)	D12	+3.3V	E12
CS_L(3)	A13	+3.3V	B13	MDE_L(1)	C13	GND	D13	MDE_L(3)	E13
GND	A14	MDE_L(2)	B14	GND	C14	MDE_L(5)	D14	+3.3V	E14
MDE_L(4)	A15	+3.3V	B15	MDE_L(6)	C15	GND	D15	MDE_L(8)	E15
GND	A16	MDE_L(7)	B16	GND	C16	MDE_L(10)	D16	+3.3V	E16
MDE_L(9)	A17	+3.3V	B17	MDE_L(11)	C17	GND	D17	MDE_L(13)	E17
GND	A18	MDE_L(12)	B18	GND	C18	MDE_L(15)	D18	+3.3V	E18
MDE_L(14)	A19	+3.3V	B19	CB_L(0)	C19	GND	D19	CB_L(2)	E19
GND	A20	CB_L(1)	B20	GND	C20	MDE_L(16)	D20	+3.3V	E20
CB_L(3)	A21	+3.3V	B21	MDE_L(17)	C21	GND	D21	MDE_L(19)	E21
GND	A22	MDE_L(18)	B22	GND	C22	MDE_L(21)	D22	+3.3V	E22
MDE_L(20)	A23	+3.3V	B23	MDE_L(22)	C23	GND	D23	MDE_L(24)	E23
GND	A24	MDE_L(23)	B24	GND	C24	MDE_L(26)	D24	+3.3V	E24
MDE_L(25)	A25	+3.3V	B25	MDE_L(27)	C25	GND	D25	MDE_L(29)	E25
GND	A26	MDE_L(28)	B26	GND	C26	MDE_L(31)	D26	GND	E26
MDE_L(30)	A27	GND	B27	MA0(0)	C27	GND	D27	MA0(1)	E27
GND	A28	MA0(2)	B28	GND	C28	MA0(3)	D28	+3.3V	E28
MA0(4)	A29	+3.3V	B29	MA0(5)	C29	GND	D29	MEM_SPARE2	E29
MBA(1)	A30	GND	B30	GND	C30	GND	D30	MBA(0)	E30
GND	A31	GND	B31	CLK0	C31	GND	D31	GND	E31
MA0(7)	A32	GND	B32	GND	C32	GND	D32	MA0(6)	E32
MA0(8)	A33	+3.3V	B33	MA0(10)	C33	GND	D33	MEM_SPARE3	E33
GND	A34	MA0(12)	B34	GND	C34	MA0(9)	D34	+3.3V	E34
MA0(13)	A35	GND	B35	MDE_L(32)	C35	GND	D35	MA0(11)	E35
GND	A36	MDE_L(34)	B36	GND	C36	MDE_L(33)	D36	GND	E36
MDE_L(35)	A37	+3.3V	B37	MDE_L(37)	C37	GND	D37	MDE_L(36)	E37
GND	A38	MDE_L(39)	B38	GND	C38	MDE_L(38)	D38	+3.3V	E38
MDE_L(40)	A39	+3.3V	B39	MDE_L(42)	C39	GND	D39	MDE_L(41)	E39

Table 6-29: Memory Board 1 Interface Connector (J4E1) (Continued)

GND	A40	MDE_L(44)	B40	GND	C40	MDE_L(43)	D40	+3.3V	E40
MDE_L(45)	A41	+3.3V	B41	MDE_L(47)	C41	GND	D41	MDE_L(46)	E41
GND	A42	CB_L(5)	B42	GND	C42	CB_L(4)	D42	+3.3V	E42
CB_L(6)	A43	+3.3V	B43	MDE_L(48)	C43	GND	D43	CB_L(7)	E43
GND	A44	MDE_L(50)	B44	GND	C44	MDE_L(49)	D44	+3.3V	E44
MDE_L(51)	A45	+3.3V	B45	MDE_L(53)	C45	GND	D45	MDE_L(52)	E45
GND	A46	MDE_L(55)	B46	GND	C46	MDE_L(54)	D46	+3.3V	E46
MDE_L(56)	A47	+3.3V	B47	MDE_L(58)	C47	GND	D47	MDE_L(57)	E47
GND	A48	MDE_L(60)	B48	GND	C48	MDE_L(59)	D48	+3.3V	E48
MDE_L(61)	A49	+3.3V	B49	MDE_L(63)	C49	GND	D49	MDE_L(62)	E49
GND	A50	CS_L(5)	B50	GND	C50	CS_L(4)	D50	+3.3V	E50
CS_L(6)	A51	+3.3V	B51	CAS_L(3)	C51	GND	D51	CS_L(7)	E51
GND	A52	RAS_L(3)	B52	GND	C52	CAS_L(2)	D52	+3.3V	E52
RAS_L(2)	A53	GND	B53	WE_L(2)	C53	GND	D53	WE_L(3)	E53
MEM_SPARE4 Used for MEM_PRES	A54	RESV	B54	GND	C54	RESV	D54	+3.3V	E54
GND	A55	GND	B55	TM(4)	C55	BD_ID	D55	GND	E55
RESV	A56	GND	B56	3V_SENSE	C56	GND	D56	RESV	E56
DIMM1_SCL	A57	RESV	B57	GND	C57	RESV	D57	DIMM1_SDA	E57
GND	A58	GND	B58	MEM_PRES	C58	GND	D58	GND	E58
GND	A59	+5V	B59	GND	C59	+5V	D59	GND	E59
+12V	A60	GND	B60	+12V	C60	GND	D60	+12V	E60

Table 6-30: Memory Board 2 Interface Connector (J9E1)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
+12V	A1	GND	B1	+12V	C1	GND	D1	+12V	E1
GND	A2	+5V	B2	GND	C2	+5V	D2	GND	E2
GND	A3	GND	B3	GND	C3	GND	D3	GND	E3
S_MEM_PWR_GD	A4	GND	B4	S_SPARECLK0	C4	GND	D4	S_MEM_SPARE1	E4
S_TRST_L	A5	GND	B5	GND	C5	GND	D5	S_JTAG_TDI	E5
GND	A6	S_SYS_SCL	B6	+3.3V	C6	S_SYS_SDA	D6	GND	E6
S_JTAG_TDO	A7	+3.3V	B7	S_JTAG_TCK	C7	GND	D7	S_JTAG_TMS	E7

Table 6-30: Memory Board 2 Interface Connector (J9E1) (Continued)

GND	A8	S_DIMM0_SDA	B8	GND	C8	S_DIMM0_SCL	D8	+3.3V	E8
S_RAS_L(0)	A9	+3.3V	B9	S_RAS_L(1)	C9	GND	D9	S_CAS_L(1)	E9
GND	A10	S_CAS_L(0)	B10	GND	C10	S_WE_L(0)	D10	+3.3V	E10
S_WE_L(1)	A11	+3.3V	B11	S_CS_L(1)	C11	GND	D11	S_CS_L(2)	E11
GND	A12	S_CS_L(0)	B12	GND	C12	S_MDE_L(0)	D12	+3.3V	E12
S_CS_L(3)	A13	+3.3V	B13	S_MDE_L(1)	C13	GND	D13	S_MDE_L(3)	E13
GND	A14	S_MDE_L(2)	B14	GND	C14	S_MDE_L(5)	D14	+3.3V	E14
S_MDE_L(4)	A15	+3.3V	B15	S_MDE_L(6)	C15	GND	D15	S_MDE_L(8)	E15
GND	A16	S_MDE_L(7)	B16	GND	C16	S_MDE_L(10)	D16	+3.3V	E16
S_MDE_L(9)	A17	+3.3V	B17	S_MDE_L(11)	C17	GND	D17	S_MDE_L(13)	E17
GND	A18	S_MDE_L(12)	B18	GND	C18	S_MDE_L(15)	D18	+3.3V	E18
S_MDE_L(14)	A19	+3.3V	B19	S_CB_L(0)	C19	GND	D19	S_CB_L(2)	E19
GND	A20	S_CB_L(1)	B20	GND	C20	S_MDE_L(16)	D20	+3.3V	E20
S_CB_L(3)	A21	+3.3V	B21	S_MDE_L(17)	C21	GND	D21	S_MDE_L(19)	E21
GND	A22	S_MDE_L(18)	B22	GND	C22	S_MDE_L(21)	D22	+3.3V	E22
S_MDE_L(20)	A23	+3.3V	B23	S_MDE_L(22)	C23	GND	D23	S_MDE_L(24)	E23
GND	A24	S_MDE_L(23)	B24	GND	C24	S_MDE_L(26)	D24	+3.3V	E24
S_MDE_L(25)	A25	+3.3V	B25	S_MDE_L(27)	C25	GND	D25	S_MDE_L(29)	E25
GND	A26	S_MDE_L(28)	B26	GND	C26	S_MDE_L(31)	D26	GND	E26
S_MDE_L(30)	A27	GND	B27	MA1(0)	C27	GND	D27	MA1(1)	E27
GND	A28	MA1(2)	B28	GND	C28	MA1(3)	D28	+3.3V	E28
MA1(4)	A29	+3.3V	B29	MA1(5)	C29	GND	D29	S_MEM_SPARE2	E29
S_MBA(1)	A30	GND	B30	GND	C30	GND	D30	S_MBA(0)	E30
GND	A31	GND	B31	S_CLK0	C31	GND	D31	GND	E31
MA1(7)	A32	GND	B32	GND	C32	GND	D32	MA1(6)	E32
MA1(8)	A33	+3.3V	B33	MA1(10)	C33	GND	D33	S_MEM_SPARE3	E33
GND	A34	MA1(12)	B34	GND	C34	MA1(9)	D34	+3.3V	E34
MA1(13)	A35	GND	B35	S_MDE_L(32)	C35	GND	D35	MA1(11)	E35
GND	A36	S_MDE_L(34)	B36	GND	C36	S_MDE_L(33)	D36	GND	E36
S_MDE_L(35)	A37	+3.3V	B37	S_MDE_L(37)	C37	GND	D37	S_MDE_L(36)	E37
GND	A38	S_MDE_L(39)	B38	GND	C38	S_MDE_L(38)	D38	+3.3V	E38
S_MDE_L(40)	A39	+3.3V	B39	S_MDE_L(42)	C39	GND	D39	S_MDE_L(41)	E39
GND	A40	S_MDE_L(44)	B40	GND	C40	S_MDE_L(43)	D40	+3.3V	E40
S_MDE_L(45)	A41	+3.3V	B41	S_MDE_L(47)	C41	GND	D41	S_MDE_L(46)	E41

Table 6-30: Memory Board 2 Interface Connector (J9E1) (Continued)

GND	A42	S_CB_L(5)	B42	GND	C42	S_CB_L(4)	D42	+3.3V	E42
S_CB_L(6)	A43	+3.3V	B43	S_MDE_L(48)	C43	GND	D43	S_CB_L(7)	E43
GND	A44	S_MDE_L(50)	B44	GND	C44	S_MDE_L(49)	D44	+3.3V	E44
S_MDE_L(51)	A45	+3.3V	B45	S_MDE_L(53)	C45	GND	D45	S_MDE_L(52)	E45
GND	A46	S_MDE_L(55)	B46	GND	C46	S_MDE_L(54)	D46	+3.3V	E46
S_MDE_L(56)	A47	+3.3V	B47	S_MDE_L(58)	C47	GND	D47	S_MDE_L(57)	E47
GND	A48	S_MDE_L(60)	B48	GND	C48	S_MDE_L(59)	D48	+3.3V	E48
S_MDE_L(61)	A49	+3.3V	B49	S_MDE_L(63)	C49	GND	D49	S_MDE_L(62)	E49
GND	A50	S_CS_L(5)	B50	GND	C50	S_CS_L(4)	D50	+3.3V	E50
S_CS_L(6)	A51	+3.3V	B51	S_CAS_L(3)	C51	GND	D51	S_CS_L(7)	E51
GND	A52	S_RAS_L(3)	B52	GND	C52	S_CAS_L(2)	D52	+3.3V	E52
S_RAS_L(2)	A53	GND	B53	S_WE_L(2)	C53	GND	D53	S_WE_L(3)	E53
S_MEM_SPARE4	A54	RESV	B54	GND	C54	RESV	D54	+3.3V	E54
GND	A55	GND	B55	S_TM(4)	C55	S_BD_ID	D55	GND	E55
RESV	A56	GND	B56	S_3V_SENSE	C56	GND	D56	RESV	E56
S_DIMM1_SCL	A57	RESV	B57	GND	C57	RESV	D57	S_DIMM1_SDA	E57
GND	A58	GND	B58	S_MEM_PRES	C58	GND	D58	GND	E58
GND	A59	+5V	B59	GND	C59	+5V	D59	GND	E59
+12V	A60	GND	B60	+12V	C60	GND	D60	+12V	E60

6.4.1.3 I²C* Connector

Table 6-31: 3-Pin I²C Connector Pinout (J7F1)*

Pin #	Signal:
1	I2C_GLOBAL_SDA
2	GND
3	I2C_GLOBAL_SCL

6.4.1.4 Power Supply Connector

Table 6-32: 36-Pin Power Supply Connector Pinouts (J1C1, J4C1, J7C1)

Signal Pins						
	1	**2**	**3**	**4**	**5**	**6**
D	+ 12 V LS	PGOOD	AC_OK	Spare	Remote SEN RTN	- 12 V
C	A0	SCL	FAULT	PRED FAIL	+12 V SENSE	KEY
B	A1	SDA	+3.3 V SENSE	+5 V SENSE	+ 24 V	+5 V Stdby
A	+ 3.3 V LS	Power Present	Spare	+5 V LS	PS_ON	PS_KILL

Table 6-33: Power Blades

Power Blades											
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
+12 V	+12 V	GND	GND	GND	GND	GND	GND	+5 V	+5 V	3.3 V	3.3 V

Figure 6-5: DC Connector

6.4.1.5 Peripheral Bay Power and I²C* Connector

Table 6-34: 20-Pin Peripheral Power Connector Pinout (J7F2)

Pin #	Signal:	Pin #	Signal:
1	VCC12	11	VCC12

Table 6-34: 20-Pin Peripheral Power Connector Pinout (J7F2) (Continued)

2	GND	12	GND
3	VCC12	13	VCC12
4	VCC5	14	VCC5
5	GND	15	GND
6	VCC5	16	VCC5
7	GND	17	GND
8	I2C_GloBAL_SCL	18	I2C_GloBAL_SDA
9	GND	19	GND
10	PWR_GOOD	20	VCC12

6.5 Performance Requirements

The power share function is performed inside the power supplies in a 2+1 redundant configuration. The midplane function is to distribute the power to the loads and provide some additional decoupling capacitance to aid the power supplies step load dynamic response. Change in output voltage is to remain within regulation limits. Required power supplies are not to be affected when a redundant supply fails or is disconnected. Output current is to be redistributed among the remaining two supplies and meet system requirements.

6.6 Mechanical and Environmental Specifications

6.6.1 Mechanical

The midplane has dimensions of 16.5" x 4.15" and 0.093" thick. The current densities on the board are kept low enough to allow no more than a 20°C rise on the printed circuit board traces.

7. OPRF100 Cache Coherency Board

This section describes the architecture and external interfaces of the OPRF100 cache coherency board. The OPRF100 cache coherency board is a high-capacity SSRAM memory board based on the Profusion* PCIset. Its purpose is to maintain coherency information that the Profusion PCIset uses. The cache coherency board has been designed for use with the OPRF100 Profusion carrier, which has two cache coherency board connectors.

Features

- Utilizes fast synchronous SRAMs (SSRAMs).
- Two configurations utilizing a common printed circuit board.
- Mates with 72-pin SO DIMM socket with nonstandard keying to prevent misapplication.
- Provides server management field replaceable unit (FRU) data.
- Provides a JTAG interface to the SSRAM devices.
- Supports 4.5 Mbit (256K lines), 9 Mbit (512K lines), or 18 Mbit (1-MB lines) cache coherency filter sizes using one, two, or four 256K x 18 SSRAM modules.

7.1 Introduction

This section provides an overview of the cache coherency board, showing primary components and their relationships, and physical board layout diagrams.

7.1.1 Block Diagram

Figure 7-1: Cache Coherency Board Block Diagram shows the main architectural features of the cache coherency board.

Cache Coherency Block Diagram

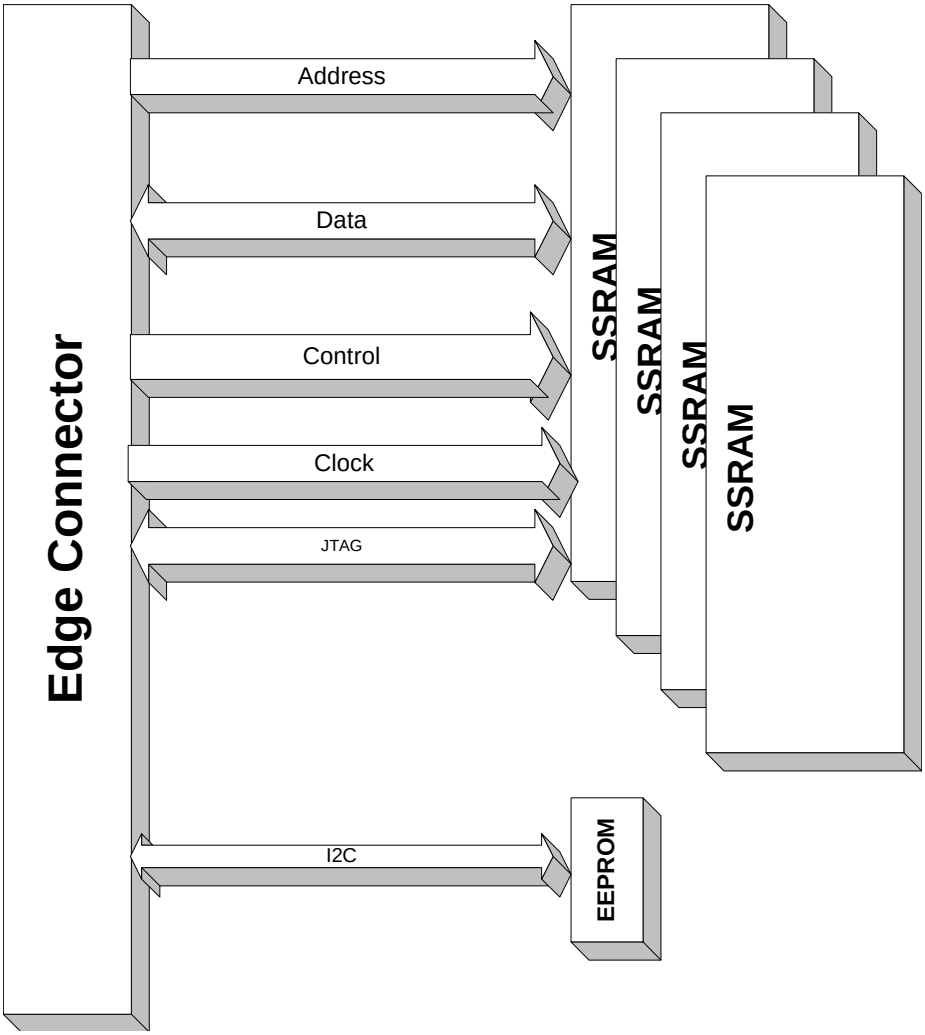

Figure 7-1: Cache Coherency Board Block Diagram

7.1.2 Architectural Overview

The cache coherency board is based on the Profusion PCIset. The module's main components are as follows:

- One or four SSRAM memory devices (119 pin BGA package).
- Server management support with on board EEPROM.

7.1.3 Placement Diagram

Figure 7-3: Cache Coherency Board shows the primary components of the cache coherency board and their positions on the printed circuit board. The table below maps the reference designators to device name.

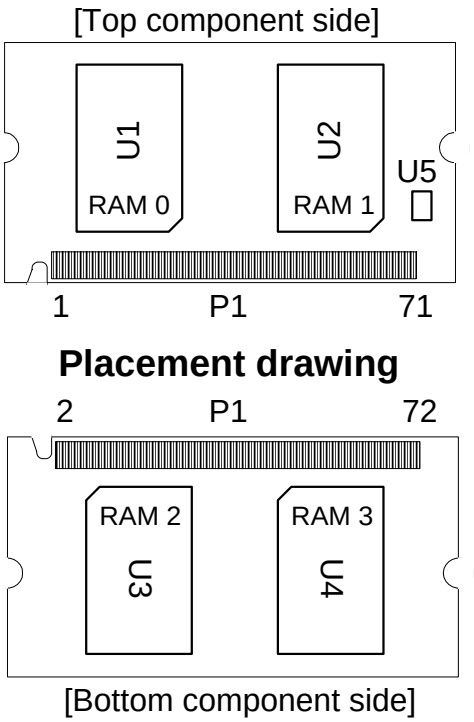

Figure 7-3: Cache Coherency Board

Table 7-1: Placement Diagram Reference Designators

Reference Designator	Description
U1-4	SSRAM
U5	EEPROM
P1	Edge finger connector

7.2 Functional Description

This section provides a more detailed description of the cache coherency board functionality.

7.2.1 SSRAM Array

The SSRAM array consists of four devices. One or four devices can be populated. The device's address, data and control signals are bused together to each device with the exception of individual chip enables (CE#) and the daisy chained JTAG data signals. These signals are present on

the module's edge-finger connector for interfacing to the external chip set controller. No additional decoding or buffering is provided. The table below lists the two different configurations.

Table 7-2: Cache Coherency Board Configurations

Configuration	SSRAM Population	Cache Coherency Board Size
1 SRAM	U1	256K of 18 bit entries
4 SRAM	U1, U2, U3, U4	1 MB of 18 bit entries

The SSRAMs are packaged in 7 x 17 (119) bump ball grid array package with SRAM JEDEC standard pinout and boundary scan order. This packaging allows for a pair of components to be mounted top and bottom side and share a common via per pin (for most signals). This is accomplished by mapping the signal to SSRAM pins on the bottom side component to the mirrored equivalent pin of the top side component. Ram 0 and Ram 2 are mirrored pairs and Ram 1 and Ram 3 are mirrored pairs. Note the re-mapping of the signals between Ram 0/Ram 1 and Ram 2/ Ram 3 in the logic diagrams.

The coherency filter uses 3.3 V as its voltage source to power the EEPROM, SSRAM core and output drivers (VDDq).

The SSRAM devices normally use a differential clocking scheme. In this design, however, only single ended clocks are provided from the host board. Two identical clocks are provided [CLK(0) and CLK(1)] with each clock driving two SSRAMs (necessary to reduce loading). The inverse clocks required by the SSRAMs are static signals terminated to 2/3 Vdd +/- 80 mV. This is done by a resistor divider on the module, thus creating a reference level in the SSRAM that determines the switching threshold for the actual clock inputs.

7.2.2 SSRAM Mode Bit Settings

Two mode bits are available to set the read mode of the SSRAM. These bits (M1 and M2) are set high or low depending on resistor populations. The particular SSRAM used defines these bits. The expected value for this design is register/latch mode (M1 = high, M2 = low). The table below lists the mode bit configuration options and default setting.

Table 7-3: Mode Bit Settings

Mode Bits	Populate Resistors	Depopulate Resistors	Mode Description
M2=LOW, M1=LOW	R8, R4	R7, R6	
M2=LOW, M1=HIGH	R8, R6	R7, R4	Default

Table 7-3: Mode Bit Settings (Continued)

M2=HIGH, M1=LOW	R7, R4	R8, R6	
M2=HIGH, M1=HIGH	R7, R6	R8, R4	

Note: Resistors are zero ohm. Some implementations of the module may replace the populated resistors with board etch for the default case. Changing the settings would require cutting the etch to depopulate the resistor.

In addition to the M1/M2 bits, the following SSRAM pins are tied low (resistor to GND): SB0, SB1 (byte write enables), G (asynchronous output enable), ZZ (asynchronous sleep mode). In this configuration, the global write enable (SW) is used, the output enable is always on, and sleep mode is not used.

7.2.3 System Management Interface

The cache coherency board provides system management software with information about the configuration in addition to FRU information about the cache coherency board itself. This data comes from a 24C02-3* EEPROM device that resides on the I^2C* bus. The I^2C address of this device is set by populating configuration resistors for A2 and A1. Address A0 is set by the level of signal SA0. This signal connects to the coherency filter's edge connector and allows for the host board to set a unique address for two different coherency filters. The table below lists the address configuration options and default setting.

Table 7-4: I^2C Address Configurations*

I^2C* Address	**Populate Resistors**	**Depopulate Resistors**	**Default Configuration**
A2=LOW, A1=LOW	R22, R23	R24, R25	Default
A2=LOW, A1=HIGH	R22, R25	R24, R23	
A2=HIGH, A1=LOW	R24, R23	R22, R25	
A2=HIGH, A1=HIGH	R24, R25	R22, R23	

Note: Resistors R22 and R23 are zero ohm. Some implementations of the module may replace these resistors with board etch for the default case. Changing the settings would require cutting the etch to depopulate the resistor.

Table 7-5: SA0 Signal Levels/I²C Addresses*

SA0	I2C* Address
LOW	A0, A1
HIGH	A2, A3

The design sets the write protection for the EEPROM to always enable writes. This is accomplished by pulling down the WC pin on the EEPROM to ground by a zero ohm resistor, R1. Some implementations of the module may replace this resistor with board etch.

7.2.4 JTAG Scan Chain

The cache coherency board supports JTAG scanning of its SSRAM devices. Figure 7-5: JTAG Scan Chain illustrates the scan chain on the module.

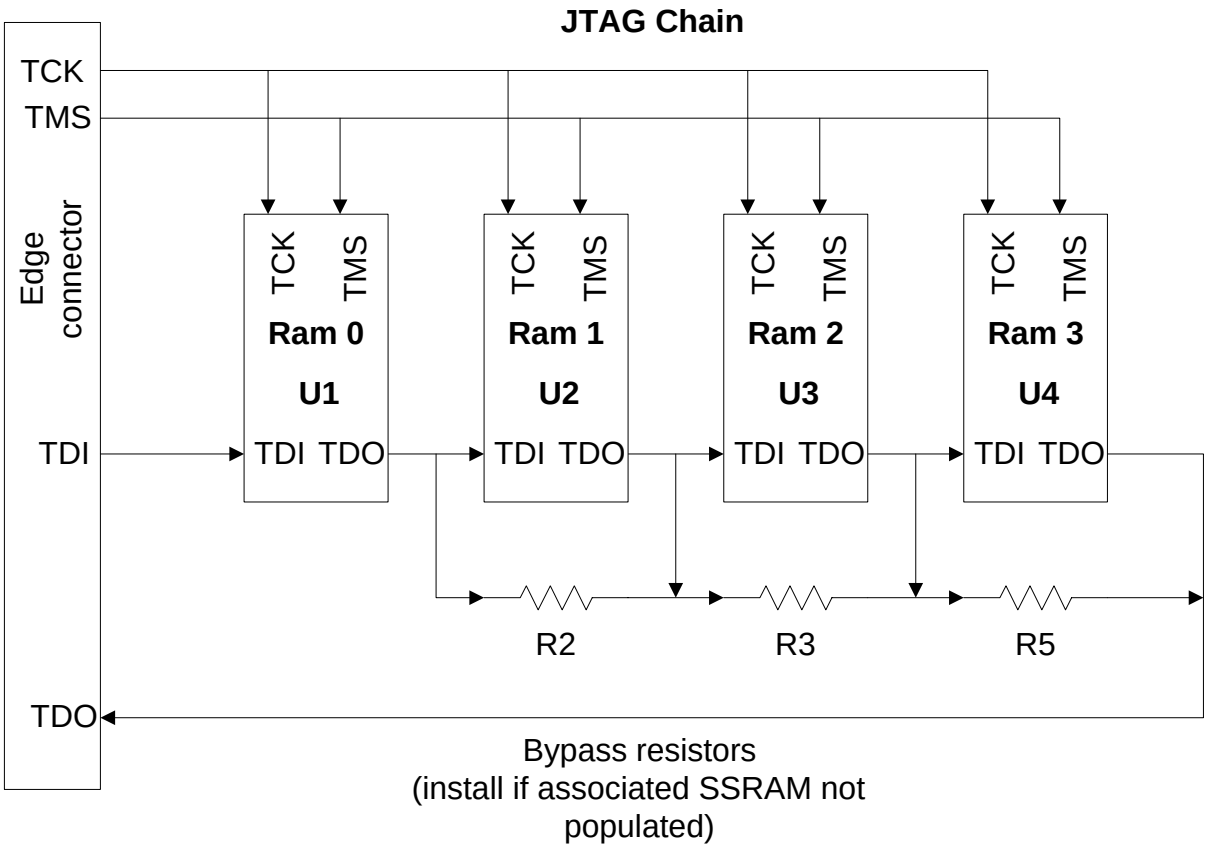

Figure 7-5: JTAG Scan Chain

Since the design allows for configurations of one, two, or four SSRAMs, bypass resistors are included to provide continuity to the JTAG data chain when less than four SSRAMs are populated. The table below lists the resistor populations by configuration.

Table 7-6: JTAG Resistor Configurations

Configuration	Populate Resistors (zero ohm)	Depopulate Resistors
1 SSRAM (U1)	R2, R3, R5	-
4 SSRAMs (U1-4)	-	R2, R3, R5

7.3 Signal Descriptions

This section provides a quick reference to signal pins used on the cache coherency board connector and other signals on the board. The signal mnemonics defined here may appear in descriptive text in the document. A “#” as suffix on the signal name indicates that the signal is active-low. A colon between numbers indicates a range of signals (e.g., AD[31:0]).

7.3.1 Memory Interface Bus Signals

The following tables are a summary of signal pins, including the signal mnemonic, electrical type and brief description. The table below lists the electrical types for the signals and The table below lists the interface connector signal summary.

Table 7-7: Electrical Types

Type	Description
in	Input is a standard input-only signal.
out	Totem Pole Output is a standard active driver.
o/d	Open Drain allows multiple devices to share signals as a wired-OR.
power	Power.

Table 7-8: Memory Interface Connector Signal Summary

Signal(s)	Type	Name and Description
A[17:0]	in	Coherency Address Bus. These signals define the address of the location to be accessed in the SSRAM. Common to all SSRAMs.
WE#	in	Write Enable for all SSRAMs.
CE[3:0]#	in	Chip enables. One chip enable is attached to each SSRAM device.
D[17:0]	in/out	Memory Data. Common to all SSRAMs.
CLK(1:0)	in	Clocks to the SSRAM devices. CLK(0) connects to U1 and U3. CLK(1) connects to U2 and U4.
SCL	in/out	I^2C* Clock. Clock reference for the cache coherency board I^2C interface.
SDA	in/out	I^2C Data. Serial data transfer for the cache coherency board I^2C interface.
SA0	in	Externally selectable address to the EEPROM. This signal is normally set HIGH or LOW by the host board to allow two coherency modules to connect into the same I^2C bus. This connects to the least significant address bit.
TCK	in	JTAG Test Clock. Test clock is used to clock state information and data into and out of the device during boundary scan.
RAM0_TDI	in	JTAG Test Data Input. Test Input is used to serially shift data and instructions into the TAP. This signal is connected to the TDI input of RAM 0.
RAM3_TDO	o/d	JTAG Test Output. Test Output is used to shift data out of the device. This signal is connected to the TDO output of RAM 3 and its associated bypass resistor.
TMS	in	JTAG Test Mode Select. Test Mode Select is used to control the state of the TAP controller.
INST#	out	Indicates to the host that the module is installed. The host would pull this signal up with a resistor. Connects to GND on the coherency module.
VSTBY	power	3.3 V power signal that powers the EEPROM. May be connected to a special 3.3 V source on the host board (i.e., standby voltage) or normal 3.3 V depending on the application. In Saber system, this pin is connected to the main 3.3 V.
3.3V	power	Main 3.3 V power rail. Connects to the SSRAM core and output power pins.
GND	power	Ground reference.

7.3.2 Other Signals

The table below lists the summary of other signals, including the signal mnemonic and a brief description.

Table 7-9: Other Signal Summary

Signal(s)	Name and Description
M1, M2	Mode bits to the SSRAMs. The particular SSRAMs used define these static values. See , which describes these bit settings.
CLK(1:0)#	Static level signal connecting to the SSRAMs' CLK# pin. The level on these signals is set 2/3 the 3.3 V power rail. This provides the threshold reference for the CLK input to the SSRAM.

7.4 Electrical and Mechanical Specifications

This section specifies the operational parameters and physical characteristics for the cache coherency board.

7.4.1 Mechanical Specifications

Figure 7-7: Cache Coherency Board Outline Drawing shows the mechanical specifications of the cache coherency board. All dimensions are given in inches. The board outline drawing (part of the fab package) contains the complete dimensions and is given precedence over this drawing.

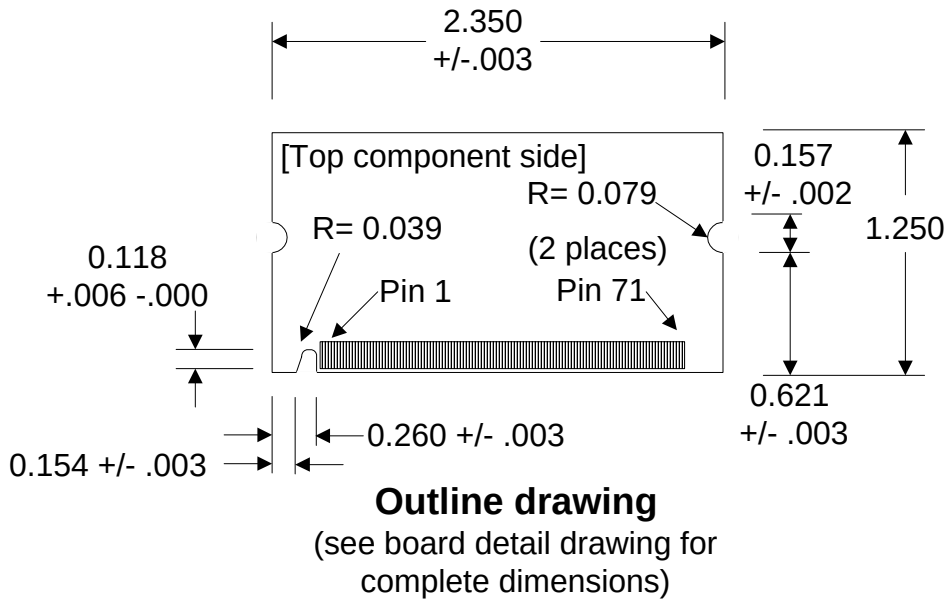

Figure 7-7: Cache Coherency Board Outline Drawing

Note that the key notch (next to pin 1) is unique from either the industry standard 3.3 V DRAM or 5 V DRAM 72 pin SODIMM. This was done to prevent the accidental insertion of a standard DIMM into the host board. Doing so could result in severe damage to the host board.

The table below below lists additional mechanical specifications for the cache coherency board. Note: The board fab drawings take precedence over this specification.

Table 7-10: Mechanical Specifications

Number of layers	6
Number of planes	2
Copper weight	1/2 oz. outer layers 1 oz. inner layers
Dielectric material	FR4
Finished thickness	.040 +/- .003
Finish	Solder mask over bare copper
Impedance	75 ohms +/- 10% on all .004 lines
Edge fingers	Hard gold (min.00005) over nickel (.0001 to .0003) Bevel edges both sides to 45 x .008

7.4.2 Electrical Specifications

This section documents the pinout of the DIMM's edge connector.

7.4.2.1 Memory Interface Connector

The cache coherency board uses an industry standard 72-pin small outline DIMM (SODIMM) edge finger connector. Odd numbered pins (1-71) are located on the top component side with pin 1 located next to the key (notch on the bottom edge of the board). Even numbered pins (2-72) are located on the bottom component side with pin 2 located opposite pin 1. See Figure 7-3: Cache Coherency Board for the location of pin 1.

7.4.2.2 Memory Interface Connector Pinout: Signal Section

Table 7-11: Coherency Filter SRAM DIMM Connector Pinout

Pin	Signal Name	Function	Pin	Signal Name	Function
1	vcc3	3.3 V power	2	vcc3	3.3 V power
3	vcc3	3.3 V power	4	vcc3	3.3 V power
5	a[17]	Address bus bit 17 input	6	a[16]	Address bus bit 16 input
7	a[15]	Address bus bit 15 input	8	a[14]	Address bus bit 14 input
9	a[13]	Address bus bit 13 input	10	a[12]	Address bus bit 12 input
11	a[11]	Address bus bit 11 input	12	a[10]	Address bus bit 10 input
13	a[9]	Address bus bit 9 input	14	a[8]	Address bus bit 8 input
15	gnd	Ground	16	gnd	Ground
17	d[17]	Data bus bit 17	18	d[16]	Data bus bit 16
19	d[15]	Data bus bit 15	20	d[14]	Data bus bit 14
21	ce[0]#	Chip enable #0 input	22	ce[2]#	Chip enable #2 input
23	d[13]	Data bus bit 13	24	d[12]	Data bus bit 12
25	d[11]	Data bus bit 11	26	d[10]	Data bus bit 10
27	d[9]	Data bus bit 9	28	d[8]	Data bus bit 8
29	gnd	Ground	30	gnd	Ground
31	CLK[0]	Clock line 0	32	CLK[1]	Clock line 1
33	gnd	Ground	34	gnd	Ground
35	d[7]	Data bus bit 7	36	d[6]	Data bus bit 6
37	d[5]	Data bus bit 5	38	d[4]	Data bus bit 4
39	d[3]	Data bus bit 3	40	d[2]	Data bus bit 2
41	d[1]	Data bus bit 1	42	d[0]	Data bus bit 0
43	gnd	Ground	44	GND	Ground
45	a[7]	Address bus bit 7 input	46	a[6]	Address bus bit 6 input
47	a[5]	Address bus bit 5 input	48	a[4]	Address bus bit 4 input
49	a[3]	Address bus bit 3 input	50	a[2]	Address bus bit 2 input
51	a[1]	Address bus bit 1 input	52	a[0]	Address bus bit 0 input
53	gnd	Ground	54	gnd	Ground
55	ce[1]#	Chip enable #1 input	56	ce[3]#	Chip enable #3 input

Table 7-11: Coherency Filter SRAM DIMM Connector Pinout (Continued)

57	gnd	Ground	58	gnd	Ground
59	SCL	I^2C* clock line	60	sda	I^2C data line
61	sa[0]	I^2C address line bit 0	62	inst#	DIMM installed
63	tdi	JTAG Test Data In	64	we#	Write enable input
65	tms	JTAG Test Mode Select	66	tDO	JTAG Test Data Out
67	VSTBY	3.3 V power	68	TCK	JTAG Test Clock
69	vcc3	3.3 V power	70	vcc3	3.3 V power
71	vcc3	3.3 V power	72	vcc3	3.3 V power

7.5 Voltage Tolerances

Table 7-12: Voltage Tolerances

DC Voltage	Acceptable Tolerances
3.3 V	± 5%

8. Board Set Specifications

This section describes the specification for the entire OPRF100 MP board set. While previous sections may provide information for the individual boards, an OEM who is integrating the OPRF100 MP board set into their own chassis must design to the specifications in this section. The board set as a whole will also be tested to the environmental and regulatory specifications listed in this section.

8.1 Power Requirements

8.1.1 Min/Max Current Ratings

The table below shows the tolerances and minimum and maximum currents for +3.3 V, +5 V, +12 V, -12 V, +5 VSB and 15 VSB for the complete OPRF100 MP board set: the OPRF100 Profusion* carrier, OPRF100 I/O carrier (with A450NX I/O riser), OPRF100 memory carriers, OPRF100 processor mezzanine boards, OPRF100 cache coherency boards, OPRF100 midplane. The table also includes boards which are typically used with the OPRF100 MP board set while integrated into a completed system assembly. The system boards used as examples in this table are the AC450NX server system front panel, A450NX processor termination modules, and peripheral LVDS backplane. These are the requirements that the power supply system must meet at the input to the midplane to ensure complete board set functionality. All the values are specified at the remote sense points in the system.

Table 8-1: Minimum/Maximum Current Ratings

Board	Spec	Units	+3.3 V	+5 V	+12 V	-12 V	+5 VSB	+15 VSB	Power
I/O carrier	**Min Load (no PCI cards, no WOL)**	Adc	0.20	0.70	0.01	0.20	0.005		**6.7 W**
Including:	**Max Load (no PCI cards, no WOL)**	Adc	4.50	7.20	0.01	0.20	0.15	0.0	**54.1 W**
I/O Riser Bd.	**Max Step Load (no PCI cards, no WOL)**	Adc	2.00	2.00	0.00	0.00	0.10		
WOL ckt	**Max Slew rate (no PCI cards, no WOL)**	A/µs	0.10	0.10	0.00	0.00	0.01		
	Max Load (w/all PCI cards+WOL)	Adc	8.00	45.20	5.00	1.20	0.75		**330.6 W**
Plugs into	**Max Step Load (w/all PCI cards+WOL)**	Adc	2.00	12.17	4.50	0.25	0.10		
Mid-Plane	**Max Slew rate (w/all PCI cards+WOL)**	A/µs	1.00	1.00	0.10	0.01	0.01		
	Existing Bulk Caps	µF	1,890.0	31,662.0	0.0	0.0	10.0		

Table 8-1: Minimum/Maximum Current Ratings (Continued)

	Add. Bulk caps required	µF	0.0	0.0	0.0	0.0	37.0		
	w/ max ESR	mÙ							
	Max resist. drop allowed	mÙ	9.79	5.84	30.74	45.00	45.00		
	Volt. regul. spec required @load	±%	5.0	5.0	5.0	10.0	5.0		
Profusion	**Min Load**	Adc	0.49	0.40	0.00				**3.6 W**
Carrier	**Max Load**	Adc	6.14	3.86	0.00	0.00	0.00	0.0	**39.6 W**
Plugs into	**Max Step Load**	Adc	2.00	0.75	0.00				
Mid-Plane	**Max Slew rate**	A/us	0.05	0.05	0.00				
	Existing Bulk Caps	µF	200.0	200.0	9,400.0	22.0	22.0		
	Add. Bulk caps required	µF	0.0	0.0	0.0	0.0	25.0		
	w/ max ESR	mÙ							
	Max resist. drop allowed	mÙ	7.29	22.74	6.74	605.0	15.00		
	Volt. regul. spec required @load	±%	5.0	5.0	5.0	10.0	5.0		
Mezzanine 1	**Min Load**	Adc	1.84	0.28	5.70		0.0001		**75.9 W**
Card	**Max Load**	Adc	1.90	0.33	24.97	0.0	0.001	0.0	**307.6 W**
Plugs into	**Max Step Load**	Adc	0.10	0.10	18.00		0.001		
Profusion c.	**Max Slew rate**	A/us	0.05	0.05	0.18		0.001		
	Existing Bulk Caps	µF	366.0	22.0	3,240.0		0.0		
	Add. Bulk cap required	µF	0.0	0.0					
	w/ max ESR	mÙ							
	Max resist. drop allowed	mÙ	4.625	37.625	2.545				
	Volt. regul. spec required @load	±%	5.0	5.0	5.0		5.0		
Mezzanine 2	**Min Load**	Adc	0.0	0.0	0.0		0.0		**0.0 W**
Card	**Max Load**	Adc	1.90	0.33	24.97	0.0	0.001	0.0	**307.6 W**

Table 8-1: Minimum/Maximum Current Ratings (Continued)

Plugs into Profusion c.	**Max Step Load**	Adc	0.05	0.05	18.00		0.001		
	Max Slew rate	A/us	0.05	0.05	0.18		0.001		
	Existing Bulk Caps	uF	366.0	22.0	3,240.0		0.0		
	Add. Bulk cap required w/ max ESR	uF mÙ	0.0	0.0					
	Max resist. drop allowed	mÙ	4.625	37.625	2.545				
	Volt. regul. spec required @load	±%	5.0	5.0	5.0		5.0		
Front Panel	**Min Load**	Adc		0.05	3.10	0.001	0.10		**38.0 W**
	Max Load	Adc	0.0	0.23	4.00	0.010	1.00	0.0	**54.3 W**
Plugs into Profusion c.	**Max Step Load**	Adc		0.18	0.10	0.001	0.04		
	Max Slew rate	A/us		0.075	0.001	0.001	0.055		
	Existing Bulk Caps	µF		22.0	150.0	0.100	22.0		
	Add. Bulk cap required w/ max ESR	µF mÙ		0.0	0.0	0.0	0.0		
	Max resist. drop allowed	mÙ		230.75	20.0	1100.0	12.0		
	Volt. regul. spec required @load	±%		5.0	5.0	10.0	5.0		
Mem. Bd.1	**Min Load**	Adc	1.20						**4.0 W**
Plugs into	**Max Load**	Adc	23.00	0.0	0.0	0.0	0.0	0.0	**75.9 W**
Mid-Plane	**Max Step Load**	Adc	6.00						
	Max Slew rate	A/us	290.00						
	Existing Bulk Caps	µF	81,600.0						
	Add. Bulk cap w/ max ESR	µF mÙ	0.0						
	Max resist. drop allowed	mÙ	8.18						
	Volt. regul. spec required @load	±%	5.0						

Table 8-1: Minimum/Maximum Current Ratings (Continued)

Mem. Bd.2	**Min Load**	Adc	0.00						**0.0 W**
Plugs into	**Max Load**	Adc	23.00	0.0	0.0	0.0	0.0	0.0	**75.9 W**
Mid-Plane	**Max Step Load**	Adc	6.00						
	Max Slew rate	A/us	290.00						
	Existing Bulk Caps	µF	81,600.0						
	Add. Bulk cap	µF	0.0						
	w/ max ESR	mÙ							
	Max resist. drop allowed	mÙ	8.18						
Peripheral	**Min Load**	Adc	0.0	0.70	0.25	0.0	0.0		**6.5 W**
LVDS Bp.	**Max Load**	Adc	0.0	4.44	5.65	0.0	0.0		**90.0 W**
Plugs into	**Max Step Load**	Adc		0.90	5.40				
Mid-Plane	**Max Slew rate**	A/us		0.28	0.16				
Through P.Bay BP	**Existing Bulk Caps**	µF		13,600.0	4,700.0				
	Add. Bulk cap	µF		0.0	0.0				
	w/ max ESR	mÙ							
	Max resist. drop allowed	mÙ		2.0	2.0				
	Volt. regul. spec required	±%							
Mid-Plane	**Min Load**	Adc	0.1	0.1	0.1	0.0	0.05	0.15	**4.5 W**
	Max Load	Adc	0.1	0.1	0.1	0.0	0.05	0.15	**4.5 W**
	Existing Bulk Caps	µF	3.0	13,600.0	13,800.0	0.0	0.5	0.0	
	Add. Bulk cap	#	0.0	0.0	0.0	0.0	0.0		
	w/ max ESR	mÙ							
	Max resist. drop allowed	mÙ	1.53	1.53	1.53	60.13	25.0		
	Volt. regul. spec required	±%	5.0	5.0	5.0	10.0	5.0	10.0	
Tot min load =		Adc	**3.83**	**2.23**	**9.16**	**0.20**	**0.16**	**0.15**	**139.1 W**

Table 8-1: Minimum/Maximum Current Ratings (Continued)

Tot max step load		Adc	**16.15**	**14.15**	**46.00**	**0.25**	**0.14**	**0.00**	
	Total max load (w/o rem s. losses)	Adc	**64.04**	**54.49**	**64.69**	**1.21**	**1.80**	**0.15**	**1285.8 W**
Total Bulk Caps=		µF	**166,025.0**	**59,128.0**	**34,530.0**	**22.1**	**54.5**	**0.0**	
Total pwr =	**1285.8**	W	**211.33**	**272.45**	**776.28**	**14.52**	**9.01**	**2.25**	**1285.8 W**

Table 8-2: Minimum/Maximum Current Ratings

Peripheral Loads

	5V load						**12V load**						
	Max	**Min**	**Max Step**	**Max di/dt**	**Tol.**	**Max Rip-ple**	**Max Avg**	**Max Pk**	**Min**	**Max Step**	**Max di/dt**	**Tol.**	**Max Rip-ple**
Peripheral Load	**Adc**	**Adc**	**Adc**	**A/µs**	**±%**	**mV**	**Adc**	**Adc**	**Adc**	**Adc**	**A/µs**	**±%**	**mV**
1 of Floppy Drive	0.65	0.01	0.40	0.033	n/a	100.0	0.00	0.00					
1 of CDROM Drive	0.55	0.17	0.10	0.050	5.0	100.0	0.60	0.60	0.20	0.40	0.001	10.0	200.0
1 of 10k LVDS HDD	1.36	0.85	0.20	0.050	5.0	100.0	2.50	3.20	0.06	2.50	0.040	5.0	150.0
SCSI Back-Plane	0.52	0.52	0.00	0.000	5.0	100.0	0.05	0.05	0.05	0.00	0.000	5.0	100.0
Totals for:													
1FD+1CDROM+SCSI Bp	1.72	0.70	0.50	0.08	5.0	100.0	0.65	0.65	0.25	0.40	0.001	5.0	100.0
1FD+1CDROM+2HDD+SCSI Bp	4.44	2.40	0.90	0.183	5.0	100.0	5.65	7.05	0.37	5.40	0.081	5.0	100.0
1FD+1CDROM+4HDD+SCSI Bp	7.16	4.10	1.30	0.283	5.0	100.0	10.65	13.45	0.49	10.40	0.161	5.0	100.0

Actual worst case slew rate measurements of Cabot Front Panel at the input connector:

5 V bus = 0.0721 A/µs

Table 8-2: Minimum/Maximum Current Ratings (Continued)

+12 V bus = 82.4 µA/µs

5 VSB bus = 0.0525 A/µs

-12 V bus = not measurable

WOL pwr requirements:

S4 state (sleep mode): I/O bd.+ Net card + FP = 0.91A@5VSB

S1 state: see min. pwr requirements on pwr budget sheet

Periph. Min load configuration: 1FD + 1CDROM

Table 8-3: Configurations for Min/Max Current Ratings

Board	Minimum Configuration	Maximum Configuration
I/O Carrier	I/O carrier, I/O riser	Core PCI power = 5V for all 10 PCI slots: The first 6 HS PCI slots (slot#1-6): 5V signaling only @33MHz w/ 3A max@5V each slot, sub-total = 6x 3A=18A. The last 4 HS PCI slots (slot#7-10): 3.3V signaling only @66MHz w/ 5A max@5V each slot, sub-total = 4x 5A=20A, Therefore, the total 5V PCI load allocation = 38A max for all 10 slots.
Profusion* Carrier	Profusion carrier, processor mezzanine board (1), Pentium® II Xeon™ processor (1), A450NX processor termination modules (3)	Profusion carrier, processor mezzanine board(2), Pentium III Xeon processors (8 at FMB maximum load), cache coherency boards (2 at 4 Tag configuration)
Memory Carrier (each)	Memory carrier, 128MB DIMM (1) [1 memory carrier only]	Max load per card: 16 DIMMs x 512MB per DIMM Actual estim. Max load is 22.37A per card. Assumes ~650MB/s sustained bandwidth.
Front Panel	Front panel with 6 system fans	Front panel with 6 system fans
Midplane	Midplane	Midplane
Peripheral LVDS Backplane	1FD + 1CDROM	Floppy drive (1), CDROM (1), hard disk drive (2), SCSI Backplane

Table 8-4: Sense Point Locations

Voltage	Sense Point Location
3.3 V	On each memory board, connects together on the midplane

Table 8-4: Sense Point Locations

5.0 V	On I/O carrier
12 V	On Profusion* carrier, two points each located near the mezzanine connector and connected together
Ground	On midplane near the center of the carrier (grand) connector

8.1.2 Absolute Maximum Ratings

Operation of the OPRF100 MP board set at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect reliability. Sufficient airflow must be provided to the board set to maintain all components within their specifications to ensure proper board component functionality.

Table 8-5: Absolute Maximum Ratings

Storage Temperature	-55°C to +70°C
Operating Temperature	5°C to 55°C
Voltage of any signal with respect to ground	-0.3V to Vdd + 0.3V
+3.3V supply with respect to ground	-0.3V to +4.3V
+5V supply with respect to ground	-0.3V to +6.5V
+12V supply with respect to ground	-0.3V to 14V

Notes:
Vdd means supply voltage for the device

8.1.3 Voltage Timing and Sequencing

The table below describes the power-up and power-down timing requirements for the OPRF100 MP board set.

Table 8-6: OPRF100 Board Set Voltage Timing and Sequencing Requirements

Parameter	Description	Specification
T_{rise}	Voltage Rise Time. This is the time it takes for all voltages (+3.3V, +5V, +12V, -12V) to rise from 10% to within regulation limits for each voltage	$T_{rise-min}$ 5ms $T_{rise-max}$ 350ms
T_{off}	Minimum Voltage Off Time. This is the time the power supplies must be powered down before being powered back up again.	100 ms.
$T_{sequence-on}$	Voltage sequencing during power on and off.	None. All voltages can come up or down in any order as long as they meet the above timing requirements and reach specified values within 100ms of each other. For example, the 3.3V output shall not be delayed from the +5V output. The rise time of the +3.3 V output and that of +5V output shall track such that the ?V between +5 V and +3.3 V does not exceed 2.25V at any time during turn on.

Note: all parameters measured at the sense points of the system.

8.1.4 Interfacing Requirements

In addition to the power supplies' maximum and minimum currents, voltages, etc., there are also requirements for the logic-level control signals which interface the I/O carrier to the power distribution system:

The PWR_GOOD signal originates on the power distribution system. It is the culmination of all the midplane power supply connnectors and is used for indication of valid and stable power from each supply. This signal is delayed from the power good signals coming from each supply. When this signal is low the system is either receiving some sort of (invalid) power from the power supplies and is being held in the reset state, or the power supplies are off. Note that in Intel's OCPRF100 Server System with the Cabot chassis, it only takes two (out of a total of three) power supplies to be turned off or otherwise be invalid for the PWR_GOOD signal to become deasserted (low). The OCPRF100 Cabot chassis can function with only one power supply turned on. In the case in which an OEM would be supplying a custom power distribution system and power supplies, the number of valid supplies which will assert the PWR_GOOD signal is not defined. It is up to the system integrator to be sure that the power distribution system can meet the power requirements of the OPRF100 MP board set. The PWR_GOOD signal must meet the following requirements.

Table 8-7: PWR_GOOD Electrical Requirements

Parameter	Description	Value
V_{oh} minimum	Minimum digital output high voltage	+4.0V into High Speed CMOS inputs @1.5mA
V_{ol} maximum	Maximum digital output low voltage	+0.7V into High Speed CMOS inputs @-3.5mA
$T_{rise\ min}$	PWR_GOOD rise time from V_{ol} to $V_{oh.}$	2µs into 2000pF

8.1.5 Power Sub-System Timing Specifications

The following figure is the power-up sequence. The sequence is initiated by assertion of PS_ON or AC applied. PGOOD is the ORing of the power good signals from each supply. PWR_GOOD is a delayed version of PGOOD. This signal is the power good indication to the system.

8.1.5.1 Turn-On Timing Specifications

Table 8-9: Turn-on Timing Specifications

Table 8-8:

Turn-On	+3.3VDC	+5VDC	+12VDC
TCMD_ON (ms)	1500 max	1500 max	1500 max
TRISE (ms)	350 max 5 min	350 max 5 min	350 max 5 min
TON-GD (ms)	100-1500	100-1500	100-1500
TOFF_MIN (ms)	350-500	350-500	350-500
Overshoot (VDC)	None	None	None

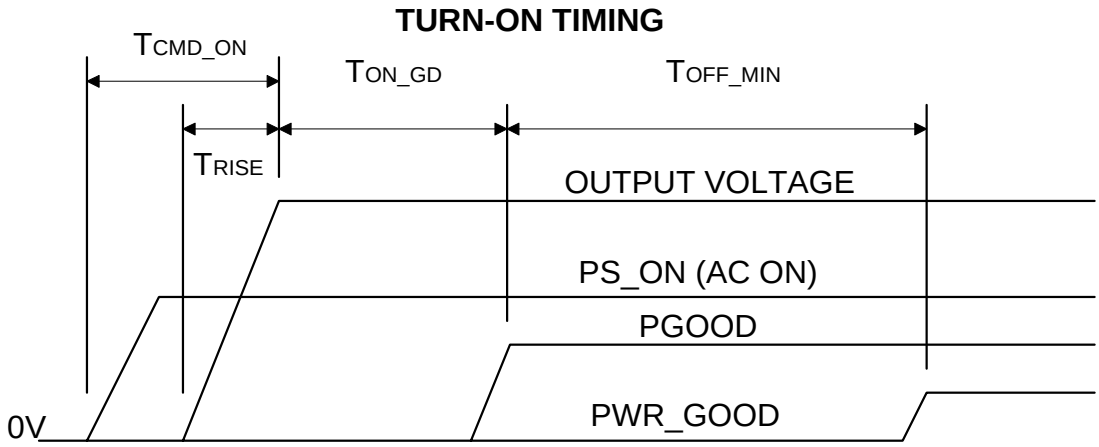

Figure 8-1: Power-Up Sequence

The following figure is the power-down sequence. The sequence is initiated by the front panel or other source such as interlock de-asserting PS_ON or loss of AC. At time T_{CMD_NGD} later PWR_GOOD is de-asserted. This is followed at T_{NGD_DROP} time by power supplies going out of specification.

Table 8-9: Turn-off Timing Specifications

Turn-Off time	**+3.3VDC**	**+5VDC**	**+12VDC**
TCMD_NGD(ms)	0-13.5	0-13.5	0-13.5
TNDG_DROP(ms)	1 (min)	1 (min)	1 (min)
TCMD_DROP(s)	10 (max)	10 (max)	10 (max)

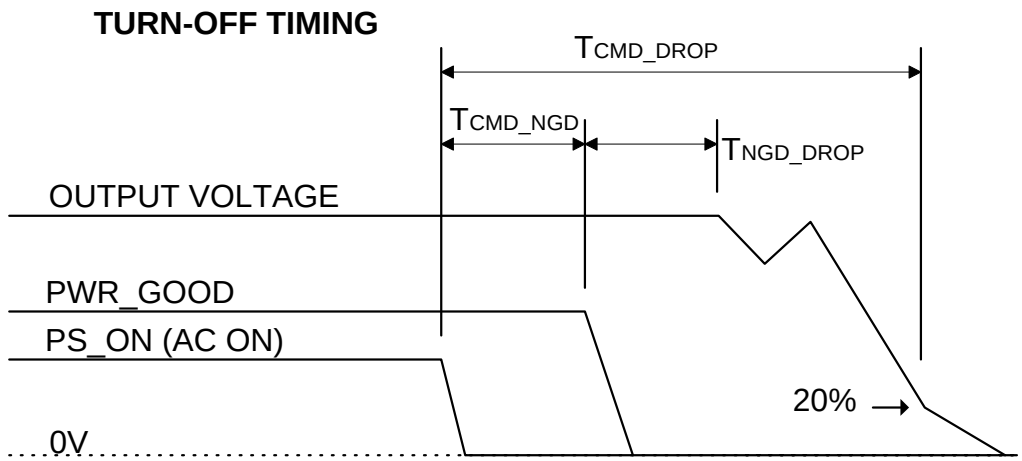

Figure 8-2: Power-Down Sequence

8.2 Thermal Requirements

The Profusion carrier requires an approximate air velocity of 300 LFM @ 40°C as measured at the edge of the processor heatsink closest to the front panel connector edge. Airflow is suggested to be from front to back of the board (front panel toward midplane connector).

The I/O carrier requires approximately 200 LFM average velocity with a 45 °C ambient temperature and the memory carriers require approximately 300 LFM with a 40°C ambient temperature to operate within specifications.

The air velocity specifications are approximate and should only be used for preliminary sizing of system cooling requirements. In a system the airflow must be sufficient to cool all board components to their specifications.

8.3 Board Level Environmental Specifications

The boards meet the Intel Board Environmental Specification 112000 Rev. G with the following exception:

The minimum operating temperature is specified at +5°C (instead of 0°C).

Table 8-10: Board Level Environmental Specifications

Temperature	
Operating	+5° to 40°C (41° to 95°F) C † (See altitude exception.)
Nonoperating	-40°C to 70°C (-104° to 158°F)

Table 8-10: Board Level Environmental Specifications

Temperature, thermal map	Must not exceed maximum IC junction temperature as specified in the component data sheets
Thermal Shock	
Nonoperating	-40° to 70°C (-40° to 158°F)
Shock	
Unpackaged	Trapezoidal, 50g, 170in/sec.
Packaged	Half sine, 2msec / Simulated Free Fall Product Weight — Height < 20-lbs. — 42” 21-40 — 36” 41-80 — 30” 81-100 — 24”
Vibration	
Unpackaged	5 Hz to 500 Hz, Sine sweep 0.5 G, 15 minutes at each of 3 resonant points
	5 Hz to 500 Hz, 3.1gRMS random
Packaged	10 Hz to 500 Hz, 1.0gRMS random
Humidity	
Operating	85% relative humidity (noncondensing) at 40°C (104°F)
Nonoperating	95% relative humidity (noncondensing) at 55°C (131°F)
Altitude	
Operating	Up to 3048 m (0 to 10000 ft) Note: Maximum ambient temperature is linearly derated between 1520 m (5000 ft) and 3048 m (10000 ft) by 1°C per 305 m (1000 ft)
Nonoperating	To 15240 m (50000 ft)
Electrostatic Discharge (ESD)	
Operating	Tested as part of system to 20 kV; no component damage
EMI	
Operating	Certified to FCC Class A; tested to CISPR 22B, EN 55022, and registered with VCCI

Notes:
† Chassis design must provide proper airflow.

8.4 Regulatory Compliance

The OPRF100 MP board set meets the European community's EMC directive and carries the CE mark.

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9. OPRF100 BIOS Specifications

This chapter describes three software components of the OCPRF100 MP server system product:

- System BIOS
- BIOS Setup
- iFLASH

Drawing from previous Intel® products, the OCPRF100 MP server system BIOS provides standard PC-compatible features, plus routines that support the extended hardware features of the system's OPRF100 board set and the OCPRF100 MP server system chassis. These extended features include:

- Eight symmetric processors
- 32 GB of shared memory using PC-100 registered DIMMs
- Four peer PCI buses
- 10 hot-plug PCI slots (with four 66-MHz/64-bit slots and six 33-MHz/64-bit slots)

The OCPRF100 MP server system BIOS configures the Profusion* PCIset including the memory controller and PCI host bridges. It also supports the server management capabilities of the Intelligent Platform Management Bus (IPMB). Section System Hardware discusses the hardware resources supported by the BIOS.

Adherence to industry standards enables a wide range of "shrink wrapped" operating systems and adapter choices. Intel has participated in industry initiatives to develop standards that address highly scalable machines. Section Industry Standards shows the industry standards supported by the BIOS.

A system vendor can customize the OCPRF100 MP server system product through the "user binary" facility. This facility provides for "splash screens" and other custom code that can differentiate a product offering. In addition to the space reserved for user binaries, over 1 MB of the system flash ROM is reserved for use by system vendors.

The OCPRF100 MP server system BIOS includes features that enhance the reliability, availability, and serviceability (RAS) of the product. The BIOS Power-on self test (POST) contains routines that check the integrity of processors, memory DIMMs, memory ports, and coherency filters. If these routines detect a failure, BIOS deconfigures the failing device and attempts to boot using the healthy hardware that remains. Like previous Intel® platforms, the BIOS provides a consistent way to handle, display, and record system errors that occur during POST or during run time. Errors are recorded in a system event log (SEL) which is available in-band from a system processor and out-of-band over the IPMB. Section System BIOS explains the features supported by the system BIOS.

Because the system BIOS automatically configures system resources, many users never need to execute a configuration utility. Nevertheless, the system provides a flash-resident setup utility

that allows users to set preferences about system operation. This utility, called BIOS Setup, is entered by pressing F2 during POST. BIOS Setup is further described in Section BIOS Setup Utility.[1]

The iFLASH utility updates the system flash ROM. It provides security features that reduce the risk of tampering. A recovery boot block allows recovery from catastrophic problems. The recovery boot block is electrically protected from erasure by a jumper on the OPRF100 I/O carrier. Section Flash Utility further describes iFLASH.

POST codes, memory maps, data formats, and other reference material are located in appendices at the end of this document.

9.1 System Hardware

The OCPRF100 MP server system supports eight Pentium® II Xeon™ processors. The Profusion PCIset connects these processors in a symmetric, cache-coherent configuration. The system supports a wide range of memory configurations from a minimum of 128 MB to a maximum of 32 GB.[2] Four peer PCI buses provide high-speed access to resources in 10 hot-plug, 64-bit PCI slots.

9.1.1 Processors

The BIOS supports eight-way symmetric multiprocessing (SMP) using the Pentium III Xeon processor and the Profusion PCIset. It automatically detects and initializes each processor. The BIOS supports mixed steppings of the processor. The flash ROM contains space for eight updates.[3]

The BIOS supports the following processor features:

- Power-on Built-in Self-test (BIST).
- Processor bus error checking and correcting (ECC).
- Processor BIOS updates.
- Lowest-feature processor selection.
- System management mode (SMM).
- Memory type range registers (MTRRs).
- Model specific registers (MSRs).

1. BIOS Setup should not be confused with the System Setup Utility (SSU), a DOS-based program that provides the means to specially configure adapter cards and various embedded devices. See the *System Setup Utility External Product Specification* for more information.
2. Support for 32 GB depends upon the commercial availability of the required DIMMs and validation in the platform.
3. Although BIOS supports mixed steppings, uncharacterized errata may exist. The OCPRF100 MP server system BIOS does not support combinations that have known errata. Refer to the appendices at the end of this document for details on supported mixed stepping configurations.

If the bootstrap processor (BSP) fails during POST, BIOS will attempt to boot the system using another processor. This feature, called fault resilient rooting (FRB), is described in Section Fault Resilient Booting (FRB).

9.1.2 Profusion* Chip Set

The Profusion PCIset connects the processors, memory, and four peer PCI buses. It consists of the memory access controller (MAC), data interface buffer (DIB), and PCI host bridge (PB64).

The BIOS supports the following features of the chip set:

- Memory port interleaving
- Coherency filters
- Coherency rules SRAM
- Routing of memory cycles for PCI, VGA, APICs, and ROM space
- Routing of I/O cycles
- System management RAM (SMRAM)
- Bus ECC
- Memory ECC

Memory gaps from 512KB to 640KB and from 15 MB to 16 MB are not supported. The memory in these regions is treated as normal system memory; memory-mapped I/O resources cannot be placed there.

The BIOS automatically initializes system memory, the coherency filters, and the rules SRAM. It examines the PC-100 serial presence detect (SPD) EEPROMs on the PC-100 DIMMs and adjusts the memory timings accordingly. Three levels of memory tests accommodate different preferences about test time versus thoroughness. For higher availability, BIOS can deconfigure a failing memory DIMM, memory port, and coherency filter as described in Section Defective Memory Remapping.

9.1.3 I/O Subsystem

The OPRF100 I/O carrier provides a PC-AT compatible I/O subsystem with PCI slots instead of ISA/EISA slots. It provides 10 PCI slots, an embedded PCI VGA, and an embedded dual-channel low voltage differential SCSI (LVDS) controller. It also supports the standard compatibility devices: two serial ports, one parallel port, two Universal Serial Bus (USB) ports, an IDE port, a floppy controller, and a PS/2 keyboard and mouse.

The PIIX4E provides the bridge to ISA-compatible resources on the I/O carrier. It also provides an IDE controller and a USB controller. BIOS uses its SMBus to access the SPD EEPROMs on the PC-100 DIMMs. BIOS uses the 256 bytes of CMOS configuration RAM for nonvolatile storage of BIOS Setup options and other BIOS parameters.

The SMC* Ultra I/O chip (FDC37C937APM) provides a floppy controller, parallel port, two serial ports, a keyboard port, and a mouse port. The BIOS supports four modes of the parallel port: out-

put-only, bidirectional, enhanced parallel port (EPP), and extended capabilities port (ECP). The Ultra I/O chip also provides a keyboard controller containing Phoenix* microcode. The BIOS downloads commands to the keyboard controller to provide various security features as described in Section Security.

The I/O carrier contains 10 hot-plug PCI slots, plus a PCI SVGA controller (Cirrus Logic* CL-GD5446) and a dual-channel low voltage differential SCSI controller (Symbios* SYM53C896). The flash ROM contains the option ROM (OPROM) for both of these components.

The BIOS uses the programmable interrupt device (PID) to route PCI interrupts to the AT-compatible PICs. The PID also contains an I/O APIC, which can handle interrupts when enabled by the operating system (OS). The BIOS provides the standard Plug and Play interfaces for PCI interrupt routing.

The system flash ROM contains 2 MB of field programmable memory. The upper 1 MB contains BIOS and other regions reserved for Intel. The lower 1 MB is available for use by system vendors. The BIOS implements a security mechanism that reduces the risk of unauthorized modification of the system flash ROM.

9.1.4 Intelligent Platform Management Bus (IPMB)

The BIOS communicates with the IPMB to update the SEL through the baseboard management controller (BMC), display messages on the liquid crystal display (LCD), and implement FRB. By passing messages over the IPMB to the BMC, server management cards can access the log, even if the system processors are not running.

The server management interface controller (SMIC) provides the gateway to the IPMB. The BMC accesses many of the system components.

The BIOS provides interface functions that allow real-mode software to send messages over the IPMB as described in the appendices at the end of this document.

9.2 Industry Standards

The system BIOS supports industry standards wherever possible. These standards expand the range of operating systems, software, adapters, and peripheral devices supported by the OCPRF100 MP server system.

System vendors who develop software to differentiate their server products also benefit because standards provide a consistent programming interface, regardless of the underlying hardware.

The system BIOS is governed by the industry standards discussed in the following sections.

9.2.1 ACPI

The system BIOS supports the *Advanced Configuration and Power Interface (ACPI) Specification*, Revision 1.0. ACPI is the key element in operating system directed power management. It supports an orderly transition from existing (legacy) hardware to ACPI-compliant hardware. With ACPI, the operating system can take direct control over the power management and Plug and

Play functions of the system. ACPI makes the MPS table and the Plug and Play BIOS run-time interfaces obsolete.

The system supports the S1, S4 OS, and S5 sleep states. It also supports Wake on LAN* from the S1 and S4 states.

After the operating system sends the command to switch to ACPI mode, the power button acts as a sleep button and a power button. If the button is pressed for less than four seconds, the system enters a sleep state determined by the operating system. If it is pressed for more than four seconds, the system powers down to the S5 state.

S1 Sleep State. The system enters the S1 sleep state when the power button is pressed momentarily or when the operating system directs it to enter S1. The S1 sleep state retains the system context; all processors' caches, memory, and chip set devices retain their state information. Only the power button and power management events (Wake on LAN) can wake the system from S1.

S4 Sleep State. The system enters the S4 state when the power button is pressed (if configured for hibernation) or when the hibernate option is chosen in the shutdown menu. If the operating system supports save-to-disk, it stores the system context to hard disk before powering down. When the system powers on, the operating system restores all processes from the disk. When the system awakens, BIOS performs a normal boot; BIOS does not participate in saving and restoring the system context.

S5 Sleep State. The system powers down without saving context.

The hot-plug controller in the PB64 contains memory-mapped resources which cannot be described by ACPI. This deviates from the *Hardware Design Guide for Microsoft Windows NT Server*. Intel has reached an agreement with Microsoft on this matter. Microsoft has agreed not to fail any OEM server presented to Microsoft Windows Hardware Quality Lab (WHQL) that incorporates the PCI hot plug technology, if the system complies with a documented list of guidelines.

9.2.2 Boot Devices and Peripherals

The system BIOS supports a wide range of peripherals and boot devices. It can boot an operating system from a floppy, an IDE device, a SCSI device, a network card, or an I_2O device. Bootable CD-ROMs are supported in emulation and nonemulation modes.

The OCPRF100 MP server system BIOS supports the following specifications:

- *BIOS Boot Specification*, Version 1.01.
- *El Torito CD-ROM Boot Specification*, Version 1.0.
- *Intelligent I/O (I_2O) Architecture Specification*, Revision 1.0.
- *Universal Serial Bus (USB) Specification*, Revision 1.0.

Legacy USB devices are not supported by the BIOS, but nothing in BIOS precludes support by an operating system. A USB-aware operating system can enable the USB functionality.

Ordinarily, the system BIOS boots from the first device detected in its scan order. If adapters conform to the *BIOS Boot Specification*, the boot device can be selected without changing the placement of the adapter cards. This feature is described in Section Boot Device Selection.

I_2O defines a standard architecture for intelligent I/O, an approach to I/O in which low-level interrupts are handled by specially designed I/O processors, which communicate by passing messages. Although the system does not include any built-in I_2O devices, the BIOS provides the runtime functions necessary to boot from an I_2O mass-storage adapter card. I_2O devices are added to the interrupt 13h chain and booted using these calls.

9.2.3 Management

Management of clients and servers is a major issue for end users. The system BIOS supports server management applications through the following specifications:

- *Desktop Management Interface (DMI) Specification*, Version 2.00.
- *System Management BIOS (SMBIOS) Reference Specification*, Version 2.1.
- *Wired for Management Baseline Specification*, Version 1.1a.

The OCPRF100 MP server system BIOS provides the data and interfaces required by the DMI specification. In addition, the BIOS provides a memory image of DMI data to allow operating systems to read DMI structures from protected mode. This interface is described in Section DMI/ SMBIOS Support.

9.2.4 Configuration

Plug and Play compatibility allows most devices to be added to the system with no manual configuration at all. The system BIOS supports the following industry standards for full Plug and Play compatibility:

- *Multiprocessor Specification (MPS)*, Versions 1.1 and 1.4.
- *Extended System Configuration Data Specification*, Version 1.02a.
- *Plug and Play BIOS Specification*, Version 1.0a.
- *Plug and Play ISA Specification*, Version 1.0a.
- *PCI Specification*, Revision 2.1.
- *PCI BIOS Specification*, Revision 2.1.
- *PCI to PCI Bridge Specification*, Revision 1.0.
- *PCI Power Management Specification*, Revision 1.0.
- *PCI Hot-plug Specification*, Revision 1.0.
- *POST Memory Manager (PMM) Specification*, Version 1.01.

Although the system contains no ISA slots, the *Plug and Play ISA Specification* is supported because of the embedded peripherals.

The system BIOS can support either version of the *Multiprocessor Specification*. If version 1.1 is selected, BIOS simply includes entries for the processors, buses, APICs, and interrupts. If version 1.4 is selected, BIOS also creates entries describing the bus, memory, and I/O topology of the system. BIOS Setup allows the user to specify which version of tables should be generated.

The system BIOS allows users to use the SSU to specify PIC-mode interrupt assignments. This configuration step is completely optional unless required by higher level software.

9.3 System BIOS

The OCPRF100 MP server system BIOS provides features that make the product easier to use, easier to manage, and easier to service. It contains features to reduce downtime and enhance diagnosis of failures. Security features reduce the risk of tampering. Customization features allow system vendors to add splash screens and custom code to the product.

The features of the BIOS can be divided into several areas:

Ease of Use

- Automatic configuration
- Boot device selection
- Mouse and keyboard port swapping
- LCD messages

Reliability, Availability, and Serviceability (RAS)

- Hot-plug replacement of PCI devices
- Fault resilient booting
- Defective memory remapping
- Critical event logging
- CMOS default override
- BIOS recovery

Manageability

- Console redirection
- DMI and SMBIOS
- IPMB interface
- Emergency management port

Security

- Password protection
- Boot without keyboard

- Floppy write protection
- Front panel lock
- Keyboard lock
- Secure boot mode
- Video blanking

Customization

- User binary
- Language block

9.3.1 Ease of Use

BIOS automatically detects and configures processors, memory, embedded devices, and plug-in devices. It numbers the PCI buses and assigns system resources to devices as required. BIOS conflict detection and resolution logic ensures that the system boots with no conflicts.

With no ISA slots to support, most of the traditional resource conflicts have been eliminated. Although some embedded devices connect to the internal ISA bus, the requirements for these devices are well understood and do not conflict with resources required by PCI. Users who wish to specify explicit resource assignments can invoke BIOS Setup or the SSU. Both utilities allow users to change many of the resources assigned to the compatibility devices. In addition, the SSU allows users to specify PIC-mode interrupt assignments for PCI devices.

BIOS detects and enables add-in VGA controllers on PCI bus segment A. If an add-in VGA controller is present, BIOS disables the embedded controller. Add-in VGA controllers are not supported on other PCI bus segments or behind PCI-to-PCI bridges.

The system BIOS does not support auto-detection of floppy drive type, but IDE drives and floppy media are automatically detected.

9.3.1.1 Memory Detection and Initialization

The system BIOS automatically detects, configures, initializes, and tests memory. Section Supported Configurations lists the supported configurations. Section Memory Configuration Algorithms describes the configuration algorithms employed.

9.3.1.1.1 Supported Configurations

The system BIOS supports memory sizes from 128 MB to 32 GB across two OPRF100 memory carriers. Each memory carrier provides 16 sites for PC-100 registered DIMMs. Single and double stacked DIMMs in sizes of 128 MB, 256 MB, and 512 MB are supported; 1-GB DIMMs will be validated later. DIMM sizes can be mixed on the same memory carrier. Open slots are permitted.

One or two memory carriers can be installed. If only one memory carrier is installed, it can be placed in either memory slot. Better performance is achieved by installing two memory carriers,

although the degree of performance improvement depends on the number of processors and their workloads.

If two memory carriers are installed, the size and placement of DIMMs on both carriers must be identical for optimum performance. For example, if a 128 MB single-stacked DIMM is placed in a particular slot in the left memory carrier, a 128 MB single-stacked DIMM must be placed in the same slot on the right memory carrier. If this rule is violated, BIOS configures the memory controller for the smaller of the two DIMM sizes.

9.3.1.1.2 Memory Configuration Algorithms

This section presents an overview of the configuration process. The subsections explain each step in more detail.

Configuration Sequence. After a cold reset, the BIOS begins executing instructions from the system ROM. Before using RAM, the BIOS must detect and initialize enough memory for code, data, and stack. Without RAM, algorithms during this portion of the BIOS must be fairly simple.

The BIOS detects memory by reading and writing a few strategic addresses. This is called probing. The BIOS first probes to determine if memory is populated across one or two memory carriers (Section Memory Port Detection). It tests and initializes 8 MB of memory for use during POST. If BIOS cannot find 8 MB of error-free memory, it issues a 1-3-3-1 beep code and halts POST. At this stage, the BIOS cannot distinguish between a missing memory carrier and a broken memory port. The BIOS checks for these types of errors later, when more resources are available for testing, logging, and alerting. The BIOS cannot display an error message on the video screen because the video option ROM requires memory. Likewise, the BIOS cannot log an error to the SEL because the error logging routines require memory.

After initializing this small amount of memory, the BIOS loads a module that checks memory timing requirements (Section Timing Optimization) and sizes the memory DIMMs (Section Memory Sizing). At first, the BIOS uses conservative memory timings that work with all supported DIMMs. This module examines the Serial Presence Detect (SPD) EEPROM on each DIMM to determine the actual timing requirements and updates the chip set accordingly. The module then probes each DIMM slot and configures the chip set for the memory it detected (up to 32 GB). As before, it cannot distinguish between a missing DIMM and a broken DIMM.

At this point in BIOS, the lower portion of memory is ready for use. As such, BIOS decompresses code and data from the flash ROM into system memory. The BIOS allocates PCI resources, installs the video option ROM, and initiates error logging. The BIOS then performs advanced tasks that were infeasible earlier in POST.

After assigning PCI resources, BIOS accounts for overlapping memory regions through a process called Memory Reclaiming (Section Memory Reclaiming). As the amount of installed memory grows toward 4 GB, system memory and memory-mapped resources such as PCI devices can overlap. Ordinarily, the system memory located in this overlapped region would be lost. However, the OCPRF100 MP server system BIOS attempts to remap the lost memory to a location above 4 GB.

The Extended Memory Test tests and initializes the remainder of memory. It displays the traditional memory counter on the video display. ECC is initialized as described in Section ECC Initial-

ization. If this test detects an error, BIOS reduces the size of the faulty DIMM to the nearest 1 MB. “Defective Memory Remapping” is described in Section Defective Memory Remapping of this document.

With memory properly configured and tested, BIOS configures the memory type range registers (MTRRs) to describe cacheable and uncacheable memory ranges. The MTRR algorithm is described in Section MTRR Initialization.

Finally, the BIOS validates the memory configuration by comparing the DIMM sizes programmed in the memory controller to the actual values found in the SPD of each DIMM. As mentioned previously, the early BIOS tests are unable to distinguish between missing and failed hardware. This final comparison provides a uniform method of collecting memory size adjustments from all of the algorithms mentioned previously.

Memory Port Detection

The OCPRF100 MP server system can operate with one or two OPRF100 memory carriers installed. Each memory carrier connects to one of the two memory ports of the Profusion PCIset.

When two memory ports are enabled, the chip set interleaves memory addresses between the ports. This is an architectural feature of the chip set that cannot be disabled by software. Interleaving occurs on a cache line basis. Odd cache lines proceed to one memory port; even cache lines proceed to the other port. The chip set pairs each DIMM site on the left memory carrier with the corresponding DIMM site on the right memory carrier. For this reason, the size and placement of DIMMs on both carriers must be identical as described in Section Supported Configurations.

Before sizing memory, the BIOS probes memory addresses to determine if memory is located in one or two memory carriers. While executing from ROM, the algorithm probes both memory ports. If it finds any pair of DIMM sites where both DIMMs are installed, the algorithm exits with both ports enabled. Otherwise, it enables one memory port and disables the other one.

At this stage of POST, the BIOS cannot diagnose and report error conditions. Video and error logging are not yet available. The lack of a stack limits the capabilities of ROM-based algorithms. As such, the memory port detection algorithm is designed to tolerate errors where possible so that later algorithms can report them.

Several error cases deserve elaboration. These cases can be caused by a number of problems including improper DIMM placement, DIMM failures, and memory port failures:

Mismatched Sizes. If a DIMM on one carrier is smaller than the corresponding DIMM on the other carrier, the memory port detection algorithm takes no special action. Instead, it enables both memory ports and allows the sizing routine to choose the smaller size as described in Section Memory Sizing.

Mismatched Placement with At Least One Pair Found. If a pair of DIMMs is found in at least one pair of DIMM sites, the algorithm takes no special action. Instead, it enables both memory ports and allows the sizing routine to ignore unmatched DIMMs as described in Section Memory Sizing.

Mismatched Placement with No Pairs Found. If DIMMs are placed on two memory carriers but not in pairs, the algorithm arbitrarily enables one port and disables the other one.

No Memory Found. If the BIOS does not find 8 MB of error-free memory, the algorithm terminates with a 1-3-3-1 beep code and halts POST.

Before booting the operating system, the BIOS validates the memory configuration as described in Section Configuration Validation.

Timing Optimization

The PC-100 DIMMs used on the system contain SPD EEPROMs that provide configuration information. The BIOS initially assumes conservative values for memory timings. The BIOS adjusts the chip set timing registers based on the information it retrieves from the SPD.

Memory Sizing

The system BIOS detects memory DIMMs by probing addresses. It determines the size of each DIMM and configures the chip set accordingly. When DIMMs are installed across two memory carriers, they must be installed in pairs as described in Section Supported Configurations. If a DIMM on one memory carrier is smaller than the corresponding DIMM on the other memory carrier, the sizing algorithm configures the pair as though each was the smaller size.

The algorithm operates in three steps. First, ROM-based code locates, tests, and initializes a small amount of memory (currently 8 MB) in which to install a protected mode module. If BIOS cannot find error-free memory, it issues a 1-3-3-1 beep code and halts POST. If it does find error-free memory, it initializes ECC in this region and then installs the protected mode module. The protected mode module then examines the SPD of each DIMM and adjusts the memory timing registers of the chip set. Next, the protected mode module probes each DIMM slot to determine how much memory is present. Finally, ROM-based code configures the chip set based on the results of the protected mode module.

Memory testing is further described in Section Defective Memory Remapping. ECC initialization is explained in Section ECC Initialization. Memory timing optimization is discussed in Section Timing Optimization.

ECC Initialization

ECC logic in the Profusion PCIset reduces exposure to single-bit errors. Before using memory, the BIOS must initialize ECC; ECC initialization cannot be disabled.

As indicated previously, the BIOS requires a small amount of memory (currently 8 MB) to execute POST. Shortly after video is enabled, the BIOS initializes the remainder of memory. The BIOS enters protected mode and fills system memory as part of the same POST task that tests extended memory. To improve the speed of the ECC fill, BIOS invokes multiple processors to perform the fill. Although the BIOS provides a hot key (Section Defective Memory Remapping) for terminating the extended memory test, it always performs the ECC fill before terminating the POST task.

The architecture of the chip set requires the initialization algorithm to use full-line writes. The BIOS accomplishes this by temporarily setting a variable-range MTRR to write-back (WB) cacheable when initializing ECC.

Memory Reclaiming

The region immediately below 4 GB traditionally has been used for ROMs, APICs, and other memory-mapped resources such as PCI devices. If enough system memory is installed, these memory-mapped resources may overlap system memory. The BIOS creates a “gap” in memory address space to accommodate these memory-mapped resources. This region is called the High Memory Gap (HMG). The minimum HMG supported by the Profusion PCIset is 256 MB.

Rather than losing the system memory located in the gap, the OCPRF100 MP server system BIOS enables the “reclaiming” feature of the Profusion PCIset. The chip set adjusts the effective address before sending the cycle to physical memory. Reclaiming is transparent to system software; the value retrieved by int 15h, E820h properly accounts for reclaiming.

Figure 9-1: Effect of Reclaiming on the System Memory Map shows the effect of reclaiming on the system memory map. In this example, the system contains 8 GB of memory with a 256 MB gap just below 4 GB. Beginning at the gap, the BIOS shifts the physical mapping upward by the size of the gap. The top of system memory is shifted upward by the size of the gap.

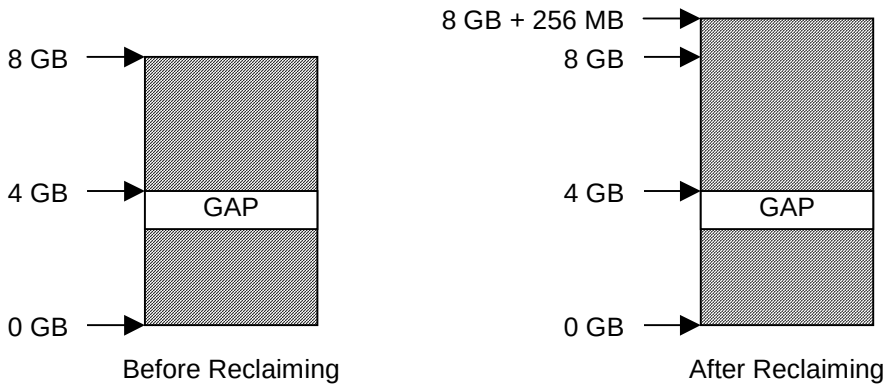

Figure 9-1: Effect of Reclaiming on the System Memory Map

The Profusion PCIset address space is limited to 32 GB. Thus, if 32 GB of system memory is installed, the gap cannot be reclaimed and memory in this gap is lost. For such a large memory configuration, the loss is negligible.

Configuration Validation

As a final check before booting the operating system, the BIOS reads the SPD EEPROMs provided by the PC-100 DIMMs and compares the actual size to the size configured in the chip set. If a mismatch is found, the BIOS displays a message on the screen and logs an error to the SEL.

9.3.1.2 Processor Initialization

The BIOS detects and configures eight processors. For each processor, the BIOS:

- examines the BIST results,
- detects the stepping,
- loads the BIOS update for that stepping,
- enables processor bus ECC,
- sets the MSRs,
- sets the MTRRs, and
- initializes system management mode.

The BIOS supports mixed processor steppings; the flash ROM provides space for BIOS updates for eight steppings. Processors must have the same size second-level cache.[1] The hardware design ensures that all processors operate at the same frequency. The number of processors and the measured speed is displayed on the video screen and the front panel LCD.

9.3.1.2.1 BSP Selection

Bootstrap processor (BSP) selection is performed by a hardware mechanism. On reset, all processors compete to become the BSP. Other processors are called application processors (APs). The BSP executes POST, invoking the APs as needed to initialize the machine.

This hardware mechanism generally selects the processor with the highest APIC ID to be the bootstrap processor, although other processors can win on rare occasions. The APIC ID for a processor is defined by its physical location as indicated in the table below. The Profusion PCIset contains a register that allows BIOS to modify the upper two bits of the APIC ID on subsequent resets. The BIOS always sets this register in such a way that the values shown in the table below are maintained.

Table 9-1: APIC ID Assignments

Board	Processor	APIC ID
Left Processor Mezzanine Board	Processor 1	4
Left Processor Mezzanine Board	Processor 2	5
Left Processor Mezzanine Board	Processor 3	6
Left Processor Mezzanine Board	Processor 4	7
Right Processor Mezzanine Board	Processor 1	0
Right Processor Mezzanine Board	Processor 2	1
Right Processor Mezzanine Board	Processor 3	2

1. Although BIOS supports mixed steppings, uncharacterized errata may exist. The OCPRF100 MP server system BIOS does not support combinations that have known errata. Refer to the processor specification update for further information about mixing processor steppings.

Table 9-1: APIC ID Assignments (Continued)

Right Processor Mezzanine Board	Processor 4	3

BSP selection is normally a hardware function. BIOS or server management firmware may override this selection in three situations:

- The Fault Resilient Booting feature may disable a failed processor as described in Section Fault Resilient Booting (FRB).
- BSP failsafe code may halt a processor if hardware selects two processors as BSP. In theory, a known hardware issue can allow each processor bus to elect its own BSP. If this occurs, BIOS halts the processor with the lower APIC ID before entering POST. The halted processor remains available to the operating system.[1]
- The lowest-feature processor algorithm requires BIOS to boot the operating system using the "least-featured" processor. At post code 93h, BIOS examines the feature flags and the stepping of each processor. BIOS executes the remainder of POST using the least-featured processor.[2]

9.3.1.2.2 Processor Startup

The BIOS wakes each processor as needed to check BIST results, set MSRs, initialize the L2 cache, and install the BIOS update. If a processor fails BIST, the BIOS disables it as described in Section Fault Resilient Booting (FRB). The BIOS enables the SMM facility of the processor and installs code for handling system events. This code is stored in a protected area of RAM that is accessible only by processors executing in this mode. After initialization of an AP is complete, the BIOS halts it using an "hlt" instruction.

When POST completes, the APs remain halted with their caches enabled. The BSP alone is enabled to receive local interrupts. The APs can respond to interprocessor interrupts (IPIs) but they are disabled from receiving local interrupts.

9.3.1.2.3 MTRR Initialization

The processor provides memory type range registers (MTRRs) to describe the cacheability attribute of various regions of memory. The BIOS marks all of system memory, except for shadow memory, as write-back cacheable (WB). It marks all other regions, including PCI space and video memory, as uncacheable.

The BIOS sets the MTRRs after PCI resources have been assigned and system memory has been tested. The BIOS uses the fixed range MTRRs to describe regions below 1 MB, and variable range MTRRs to describe the rest of memory space. The processor contains eight variable

1. This issue is documented as "Documentation Change D11" in the *Pentium® II Xeon™ Processor Specification Update.*
2. The Lowest-feature processor algorithm is described in *Extension to Pentium® Pro Processor BIOS Writer's Guide*, Revision 3.4.

range MTRRs, of which two must be left free for use by the operating system. Thus, BIOS can use only six variable range MTRRs.

The processor permits MTRR ranges to overlap in specific cases. If a fixed range MTRR and a variable range MTRR refer to the same region of memory, the processor honors the fixed range MTRR. If two variable range MTRRs overlap, uncacheable and write protect (WP) supercede WB. Other types of overlap produce undocumented results.

The length of a region of memory described by a variable range MTRR must be a power of two. The region must start on a boundary that is a multiple of its length. For example, a single register may describe a 4-MB block but not a 6-MB block. That 4-MB block can start at 104 MB or 108 MB, but not 106 MB. Other sizes require multiple MTRRs. To describe a 3.5-GB system, BIOS programs a 2-GB block, a 1-GB block, and a 512-MB block. Such a configuration consumes three MTRRs. MTRR programming becomes more complicated when system memory grows large enough to overlap PCI resources. The BIOS programs MTRRs that describe system memory plus an additional MTRR that describes the overlap. Due to the reclaiming feature described in Section Memory Reclaiming, the top of memory is adjusted to account for the remapped memory. Figure 9-1: Effect of Reclaiming on the System Memory Map describes an example system with 8 GB of memory and a 256-MB HMG. Due to reclaiming, the top of memory in that example is not 8 GB but 8 GB + 256 MB. For such a system, the BIOS programs the MTRRs as follows:

- One MTRR describes a 256-MB HMG from 0_F000_0000h to 0_FFFF_FFFFh as uncacheable. This range takes precedence over the WB range it overlaps. One MTRR describes an 8-GB block of system memory from 0_0000_0000h to 1_FFFF_FFFFh as WB. Note that the fixed range MTRRs take precedence in the lower 1 MB of this region.
- One MTRR describes a 256-MB block of system memory from 2_0000_0000h to 2_0FFF_FFFFh as WB.

If this method consumes more MTRRs than the six that BIOS is allowed to use, BIOS uses an alternate method. In the alternate method, BIOS uses one MTRR to describe a block that is larger than the actual amount of cacheable memory. It then uses the remaining MTRRs to trim away uncacheable addresses. Consider a system with 7 GB, 640 MB of system memory and a 256-MB HMG. After reclaiming the gap, the top of memory becomes 7 GB, 896 MB. By the original method, it would take one MTRR to describe the gap and six MTRRs to describe system memory (4 GB + 2 GB + 1 GB + 512 MB + 256 MB + 128 MB). Since BIOS is not allowed to use more than six MTRRs, this configuration is infeasible. However, the alternate algorithm can describe such a system using only three MTRRs:

- One MTRR describes a 256-MB HMG from 0_F000_0000h to 0_FFFF_FFFFh as uncacheable. This range takes precedence over the WB range it overlaps.
- One MTRR describes an 8-GB block of system memory from 0_0000_0000h to 1_FFFF_FFFFh as WB. As before, the fixed range MTRRs take precedence in the lower 1 MB of this region.
- One MTRR describes a 128-MB block of system memory from 1_F800_0000h to 1_FFFF_FFFFh as uncacheable. This range takes precedence over the WB range it overlaps.

Together, these two methods properly describe all possible configurations using the supported DIMM sizes on OPRF100 memory carriers with any combination of PCI cards.

Memory failures can create situations where small blocks cannot be described properly as cacheable memory. This occurs because the granularity of the Extended Memory Test is 1 MB. Describing memory to this level of granularity can consume more MTRRs than are available. The small amount of leftover memory is left uncacheable. Although the OCPRF100 MP server system continues to operate properly, failing DIMMs should be replaced at the earliest convenient time.

9.3.1.3 Resource Assignment

BIOS Plug and Play code assigns bus numbers, memory space, I/O space, PIC-mode IRQs, direct memory access (DMA) channels, and OPROM space.

Resource assignment occurs in two parts. First, the BIOS scans the PCI buses and assigns bus numbers to them. While scanning the buses, it collects the resource requirements of each device. After identifying the requirements, BIOS assigns the actual resources.

Scan Order. The OCPRF100 MP server system BIOS assigns PCI bus numbers in accordance with PCI specifications. The BIOS scans resources in PCI Function Address order, starting with device 00h on bus 00h and continuing through device 1Fh on the highest-numbered PCI bus.

The OPRF100 I/O carrier contains four peer PCI segments labeled A through D. When no PCI-to-PCI bridges are installed, these segments are numbered 0 through 3. If a bridge is inserted in a PCI bus, all subsequent PCI numbers are increased by one. For example, a bridge inserted into segment B would alter the bus numbers assigned to segments C and D. In this example, segments A and B would be numbered 0 and 1. The bus behind the bridge would be numbered bus 2. Segments C and D would be numbered 3 and 4. Refer to the PCI specifications for additional information about bus numbering.

The table below shows the scan order when no PCI-to-PCI bridges are installed. By default, BIOS boots from the first bootable device encountered. Section Boot Device Selection explains how to select a different boot device without physically moving the devices.

Table 9-2: Default Boot Device Scan Order

Device	Segment	Device Number
Primary IDE	-	-
PCI Slot 1	A	04h
PCI Slot 2	A	05h
Embedded LVDS	A	0Ah
PCI Slot 3	B	04h
PCI Slot 4	B	05h

Table 9-2: Default Boot Device Scan Order (Continued)

PCI Slot 5	B	06h
PCI Slot 6	B	07h
PCI Slot 7	C	04h
PCI Slot 8	C	05h
PCI Slot 9	D	04h
PCI Slot 10	D	05h

Resource Allocation. After the requirements have been identified, the BIOS assigns resources to devices. With the elimination of ISA slots, non-PCI devices compete with PCI devices for surprisingly few resources as shown in the table below. In addition, the embedded PCI VGA controller claims traditional VGA resources.

Table 9-3: Competition for Resources

	Non-PCI Devices	**PCI Devices**
Memory Space	No	Yes
I/O Space	Yes, traditional ports < 2000h	Yes, 2000h-FFFFh
DMA Channels	Yes	None
PIC-mode Interrupts	Yes	Yes
OPROM Space	None	Yes

As the table shows, PCI devices compete with non-PCI devices for PIC-interrupt lines only. However, the non-PCI devices leave at least one interrupt available for PCI. Because PCI devices can share interrupts, all devices are guaranteed to receive an interrupt. The sharing of PIC-mode interrupt lines does not diminish performance because most operating systems use the I/O APIC for interrupt delivery.

Option ROM space is limited to a small region by conventions established at the beginning of the PC architecture. Large systems such as the OCPRF100 MP server system were not envisioned at that time. The embedded VGA, embedded SCSI, and add-in PCI devices compete with each other for the space between C0000h and DFFFFh. In addition, user binary and console redirection code may also reside in this region.

Because of the large number of PCI slots supported by this system, some configurations may contain more option ROMs than can fit in the available space. The BIOS prints a warning message about each option ROM which fails to shadow. For proper operation, the VGA OPROM and

the boot device OPROM (if any) must shadow successfully. The boot device should be placed near the beginning of the scan order to ensure that its option ROM shadows successfully.

Appendix A shows the OCPRF100 MP server system resource maps.

Hot Plug Resource Padding. Although the OCPRF100 BIOS does not yet support hot-add, it does generate the Hot-plug Resource Table (HPRT) when enabled in BIOS Setup.

If the HPRT is enabled, BIOS can reserve resources for adapters that may be added later. Another BIOS Setup option specifies the level of resources allocated. The three modes are Disabled, Minimum, and Maximum.

When set to Disabled, BIOS reserves no resources. When set to Minimum or Maximum, BIOS allocates a range of memory addresses, I/O addresses, and bus numbers for each of the four bus segments.

Table 9-4: PCI Resource Allocation with Hot-plug Resource Table Enabled

	Maximum Allocation Mode (Per Slot)	**Minimum Allocation Mode (Per Slot)**
Nonprefetchable Memory	8 MB	16 MB
Prefetchable Memory	32 MB	128 MB
I/O	4 KB	4 KB
Bus Numbers	1	1

If the HPRT is enabled, BIOS routes all PCI interrupts to PIC-mode interrupt lines. Once the operating system enables the I/O APIC for SMP mode, this routing is no longer used.

ISA Aliasing. Some adapters on traditional ISA machines incompletely decoded address space. Conceivably, some software may have been written that depends upon this fact. Thus, the BIOS supports ISA Aliasing mode. This mode can be enabled through BIOS Setup.

For strict compatibility with such software, the BIOS observes these aliasing restrictions when assigning resources to PCI devices. The BIOS restricts PCI I/O space assignments to addresses where bits 8 and 9 equal zero. In other words, 1C00h is a legal PCI address but 1D00h is not. Other addresses are diverted to the embedded ISA bus.

Unfortunately, this compatibility restriction reduces available I/O space by approximately 75%. While this does not limit most configurations, systems with several PCI-to-PCI bridges with four or more devices behind each bridge may exhaust the available I/O space.

Configuration Storage. The extended system configuration data (ESCD) contain system information as well as data records created by the SSU; they are stored in the flash component instead of battery-backed NVRAM. Software should not attempt to access the ESCD directly; instead, it should use the standard BIOS calls.

Large PCI machines such as the OCPRF100 MP server system quickly exceed the 48 “virtual slot” limit imposed by the *ESCD Specification*. For this reason, PCI configuration information is stored in a special data structure.

The BIOS stores configuration information for internal non-PCI peripheral devices in CMOS configuration RAM along with most other BIOS Setup options.

Compatibility Devices. The OPRF100 board set contains several embedded devices that map into I/O locations below 1000h. In addition, the video buffer for the embedded PCI VGA controller maps into the traditional memory range from A0000h to BFFFFh. In accordance with the *PCI to PCI Bridge Specification*, these devices are located on PCI segment A or on the embedded ISA bus which attaches to segment A. If a PCI plug-in card replaces one of these embedded devices, that card must reside in PCI segment A.

Restrictions. Some resource requests permitted by the PCI specification are not supported by OCPRF100 BIOS.

The PCI specification permits adapters to request memory blocks below 1 MB. 128KB of this region is reserved for video memory. The remainder is occupied by system memory, including shadowed PCI expansion ROMs. As such, the OCPRF100 BIOS does not permit memory-mapped resources to be allocated in this region.

The PCI specification also permits adapters to request huge blocks of memory space for memory mapped resources. For 32-bit adapters, the allocation method supports requests as large as 2 GB. For 64-bit adapters, the allocation method supports requests that exceed the address width of the processor. OCPRF100 BIOS does not honor requests for 1 GB or more of memory space.

In practice, these restrictions should not affect the vast majority of PCI adapters, if any at all. At this time, the risk associated with changing the PCI resource allocation routines is deemed to be larger than any benefit derived from the changes.

9.3.1.4 PCI Speed Determination

PCI bus segments C and D (slots 7 through 10) support 33 MHz and 66 MHz PCI adapters. Prior to starting POST, the BIOS determines if 33 MHz cards are located in these bus segments. If a bus segment is empty, BIOS sets the frequency based on an option in BIOS Setup. The default for this BIOS setup option is to set these buses to run at 33 MHz. Otherwise, BIOS sets the bus segment to the highest frequency supported by the installed cards. The clock speeds of segments C and D are set independently of each other; one bus can run at 33 MHz while the other runs at 66 MHz. Segments A and B are always set to 33 MHz.

9.3.1.5 POST Memory Manager

The *POST Memory Manager Specification* allows external clients such as option ROMs or OEM code to request memory buffers during initialization and to release them later. Without the POST

Memory Manager (PMM), external clients can destroy buffers used by the system BIOS or another client.

See the *POST Memory Manager Specification* for more information.

9.3.1.6 Boot Device Selection

By default, the BIOS boots from the first bootable device encountered. The system BIOS allows the user to specify the boot device without physically rearranging the hardware. By adhering to the *BIOS Boot Specification*, the system BIOS allows the user to select a different boot device through on-screen menus. Without this feature, users would have to physically move the devices in order to chose a different boot device.

Changing the Boot Order. The boot menu in BIOS Setup allows the user to specify the boot order. The menu presents the first eight bootable devices encountered during the device scan. BIOS Setup saves the new boot order in CMOS configuration RAM.

Temporarily Selecting a New Boot Device. The user can temporarily select a new boot device by pressing the ESC key when the “Press <F2> key to enter Setup” message appears at the bottom of the screen. A pop-up menu presents a list of bootable devices. If the selected boot device fails to load the operating system, the BIOS reverts back to the sequence specified in BIOS Setup. Subsequent boots revert back to the order specified in BIOS Setup.

Restrictions. Legacy devices that do not conform to the *BIOS Boot Specification* cannot be selected in this manner. Devices must identify themselves as initial program load (IPL) devices to be included in the boot menu. Furthermore, devices that hook interrupt 19h bypass the Boot Device Selection feature and cannot be disabled.

The current implementation of the *BIOS Boot Specification* supports a maximum of eight devices. If more than eight devices are present, the user should disable the Multiboot option in BIOS Setup.

9.3.1.7 Mouse and Keyboard Port Swapping

The OCPRF100 MP server system BIOS allows users to plug the keyboard or PS/2 mouse connectors into either port on the machine. It detects and initializes the keyboard and mouse accordingly. This simplifies installation.

9.3.1.8 LCD Messages

The front panel LCD displays informative messages during POST. These include:

- POST status.
- BIOS revision.
- Error codes.

The table below shows the POST status messages that the BIOS displays on the LCD:

Table 9-5: POST Status Messages on the LCD

LCD Message	Corresponding POST Code
CMOS TEST	09h
CACHE TEST	0Bh
IDE LOCAL BUS	0Fh
KB CONTROLLER	22h
MEMORY TEST	2Ch, 2Eh
CPU BUS CLOCK	32h
PCI SCAN	49h
VIDEO TEST	4Ah
SERIAL TEST	82h
PARALLEL TEST	84h
PCI ROM SCAN	98h
SYSTEM BOOT	B2h

Immediately prior to booting the operating system, the BIOS displays one of the following messages:

- Number of processors and their speed.
- Custom string.

The custom string can be defined by either the system vendor or the OEM. This string is 32 characters in length, displayed as two lines of 16 characters each.

System software may write to the LCD by sending messages over the IPMB. The BIOS provides a real-mode interface for accessing the LCD. This interface is described in the appendices at the end of this document.

9.3.2 Reliability, Availability, Serviceability

9.3.2.1 Hot-plug Replacement of PCI Devices

A PCI adapter can be replaced with an identical adapter without shutting down the system. This is called “like-for-like replacement.” The addition of new cards to a running system (hot add/upgrade) is not supported by the initial release of the system.

The system BIOS supports like-for-like replacement by initializing the PCI hot-plug controller contained within each PB64. Because the new device consumes the same resources as the old device, no other BIOS support is required.

The initial release of OCPRF100 MP server system BIOS does not produce the Hot-plug Resource Table required for hot plug support under Unixware*.

9.3.2.2 Fault Resilient Booting (FRB)

The system BIOS attempts to boot the system, even if one or more processors fail. The BMC provides two watchdog timers that guard the POST sequence.

The system supports all three levels of FRB.

Level 3 – BSP Reset Failures. The FRB-3 timer safeguards BSP selection. It starts counting when the system comes out of hard reset. The BSP indicates its health by disabling this timer at the beginning of POST. If the timer expires because the BSP failed to disable it, the BMC resets the system and disables the failed processor. The duration of the FRB-3 timer is 10 seconds.

Level 2 – BSP POST Failures. The FRB-2 timer safeguards the POST sequence. BIOS enables this timer early in POST and disables it only after a significant portion of POST has completed. If BIOS does not reach this point, the BMC generates an asynchronous system reset (ASR), but it does not disable the processor. The duration of the FRB-2 timer is 12 minutes.

BIOS enables the FRB-2 timer before disabling the FRB-3 timer. This ensures proper coverage of boot failures.

Level 1 – BSP BIST Failures. Since hardware selects the BSP, a processor that has failed BIST may become the BSP. BIOS detects this situation and selects a good processor to be the BSP. If no other processor is available, BIOS boots from the failed processor, displaying an error message to notify the user.

If an AP fails BIST or fails to complete BIST, BIOS considers the AP to have failed. Failed processors are not listed in the multiprocessor (MP) table.

For each type of failure, BIOS displays an error message on the subsequent reboot and records the failure in the system event log.

9.3.2.3 Defective Memory Remapping

The OCPRF100 MP server system BIOS tests memory during POST and reconfigures memory such that any failing locations are no longer accessible.

This test occurs in two parts. The Base Memory Test tests the minimum amount of memory required to execute POST. The Extended Memory Test tests the remainder of memory.

To improve the speed of the Extended Memory Test, the system BIOS invokes all available processors to perform the test. Furthermore, a BIOS Setup option allows users to specify the coverage of the Extended Memory Test. If “1 MB” is selected, BIOS tests each 1-MB boundary. If “1KB” is selected, BIOS tests each 1-KB boundary. If “Every location” is selected, BIOS tests

every byte. The BIOS is configured at the factory to terminate the Extended Memory Test with either the ESC key or the space bar.

For the sake of system reliability, single-bit error correction is not enabled until after these tests are complete. Although single-bit errors in system memory are recoverable, the Base and Extended Memory Tests treat them as failures. If BIOS were to allow a hard single-bit error to pass the test, protection against spurious single-bit errors would be lost because a subsequent single-bit error would produce a multi-bit error. Running a memory test with error correction turned on is not an accurate test.

9.3.2.3.1 Base Memory Test

The system BIOS requires a small amount of memory (currently 8 MB) to execute POST as described in Section Memory Configuration Algorithms. It uses this memory for code, data, and stack.

BIOS locates and configures this memory by testing DIMM sites until it locates 8 MB of working memory. At this point in POST, BIOS lacks the resources to distinguish between an absent DIMM and a failed one. Since display and logging facilities are not yet available, BIOS simply skips any absent or failed DIMMs. BIOS cannot display an error message on the video screen because the video option ROM requires memory. Likewise, BIOS cannot log an error to the SEL because the error logging routines require memory. Later in POST, BIOS checks the SPD EEPROMs to determine if any DIMMs were skipped (Section Configuration Validation).

If BIOS cannot find 8 MB of error-free memory, it issues a 1-3-3-1 beep code and halts POST.

9.3.2.3.2 Extended Memory Test

The Extended Memory Test examines memory above base memory. It executes shortly after video has been enabled, providing the traditional memory counter that displays the status of the test.

Because the system supports 32 GB of memory, BIOS enters protected mode to perform the test. While in protected mode, BIOS dispatches portions of the test to all available processors. This improves the speed of the test. If the test detects an error, it reduces the size of the DIMM (or DIMM pair) so that the failing cell is no longer available. The granularity of this algorithm is 1 MB. If the failing location is in the first megabyte of the DIMM pair, the entire pair is lost. If the failing location is in the second megabyte, the first megabyte remains usable but the rest of the pair is lost.

Errors are displayed on the LCD and the video screen. The error messages indicate the location of the failing components and the amount of memory that is being deconfigured. Errors also are recorded in the SEL. Appendix C shows the format of the error log entries.

9.3.2.4 Coherency Filter Testing

The Profusion PCIset uses coherency filters to maintain cache coherency. These filters are required whenever both processor buses are enabled. If all processors are installed on a single processor bus, the filters are optional.

BIOS sizes and tests the coherency filters. If part of the coherency filters fail, BIOS attempts to resize the filter to a small supported size. If BIOS is unable to configure any portion of the filter, it restarts the machine with only one processor bus enabled. Thus, an eight-processor machine with a failed coherency filter can still operate with four processors.

The filters must be installed as a matched pair. If the sizes are not equal due to a hardware failure or configuration error, BIOS configures the system for the smaller size and issues an error message during POST.

9.3.2.5 Critical Event Logging

The system follows a consistent strategy for the handling of errors and other interesting system events. Events such as ECC errors, fan failures, or voltage problems are logged in the SEL. The SEL provides 8KB of nonvolatile storage for recording system events. System processors access the SEL by sending messages over the IPMB. Server management cards and other IPMB agents also can access the SEL, even when the system processors are not running.

The BMC manages the SEL. It receives messages from agents wishing to read or modify the log. The BMC also manages “sensors,” which monitor the status of system resources, logging events in the SEL when required. The BMC serializes all requests before accessing the SEL.

BIOS logs POST-time errors and run-time events. If a POST task encounters a failure or other noteworthy situation, BIOS records it in the SEL. For run-time events, BIOS provides an error handler that processes errors, which occur while the operating system is running. BIOS installs this run-time handler in SMRAM, a special area of RAM that can be accessed only by processors executing in SMM. Processors enter SMM in response to a system management interrupt (SMI).

9.3.2.5.1 Event Types

Events are classified as critical and noncritical events. Critical events compromise data integrity, requiring prompt attention from the operating system. In most cases, the operating system shuts down to prevent further propagation of the error. Examples of critical events include bus errors, PCI system errors, and uncorrectable ECC errors. A critical event is indicated to the operating system by a nonmaskable interrupt (NMI). Noncritical events simply generate an SMI and are handled by the SMM code without intervention by the operating system. (The BMC handles its own set of noncritical events without involving BIOS.)

Operating systems generally support the NMI sources that have a standard register interface across products from many different vendors. They do not support the unique error sources of an individual product. Thus, a typical operating system can process a PCI bus error but it cannot recognize a product-specific error source such as a coherency tag RAM failure. To ensure that the operating system recognizes such events, the system routes certain hardware-specific signals to a standard NMI source such as parity error (port 61h). The SMM code identifies the true error source by examining device registers.

9.3.2.5.2 Interrupts

Error processing involves one or more of the following event handlers.

BIOS SMI Handler. All system errors are preprocessed by the SMI handler. The SMI handler logs events, as required, by sending commands to the BMC. Events which normally generate an NMI are intercepted by the SMI handler for processing prior to the invocation of the NMI handler. The SMI handler presents platform-specific errors as one of the standard bus errors such as parity error.

OS NMI Handler. The OS NMI handler processes standard bus errors. It executes after the SMI handler completes. To allow the OS to take appropriate action in response to platform-specific errors, the BIOS SMI handler presents platform-specific errors as one of the standard bus errors.

BIOS NMI Handler. The system BIOS provides a real-mode NMI handler that is invoked if an NMI occurs during POST. To maintain DOS compatibility, the BIOS NMI handler processes standard errors only. It displays an error message, issues a beep signal, and halts. If an unknown or spurious NMI occurs, the BIOS NMI handler disables the NMI signal using bit 7 of I/O port 70h (real-time clock (RTC) Index Port). This can cause unusual side effects because it allows a spurious NMI to block a subsequent valid NMI.

9.3.2.5.3 Error Signals

The OCPRF100 MP server system supports a number of error reporting signals. Most of these signals eventually propagate to SMI, allowing the BIOS SMI handler to process the event and log an entry. If the BIOS SMI handler determines that the event is critical, it asserts NMI to allow the operating system to take appropriate action. Figure 9-2: Error Reporting Paths shows how these signals lead to an SMI.

Memory Errors. If the memory controller detects an uncorrectable memory error, it asserts IOBERR. If it detects a correctable memory error, it asserts SBCERR.

Coherency Filter Parity Errors. If the memory controller detects a parity error in the Left or Right Coherency Filter, it asserts BINIT and the system resets. BIOS logs the error on the next reboot.

PCI Errors. PCI defines two error signals: SERR and PERR. SERR indicates a fatal error. PERR is intended to be recoverable, although the system can be configured to treat it as a fatal error.

System Bus Errors. The system supports three system buses named the Left, Right, and I/O buses. The processor specification defines three error signals on each bus: AERR, BERR, and BINIT.

The memory controller checks ECC for data it receives across the system bus. If it detects an uncorrectable error, it asserts BERR. If it detects a correctable error, it asserts SBCERR.

Each PB64 checks ECC for data it receives across the system bus. If a PB64 detects an uncorrectable error, it asserts BERR. If a PB64 detects a correctable error, it silently corrects the error but does not generate an error signal. Thus, single-bit errors detected solely by a PB64 are not logged.

AERR and BINIT events do not propagate to SMI. Instead, they force an immediate reset. The error status registers retain their information through the reset, allowing BIOS to log the errors after the reset.

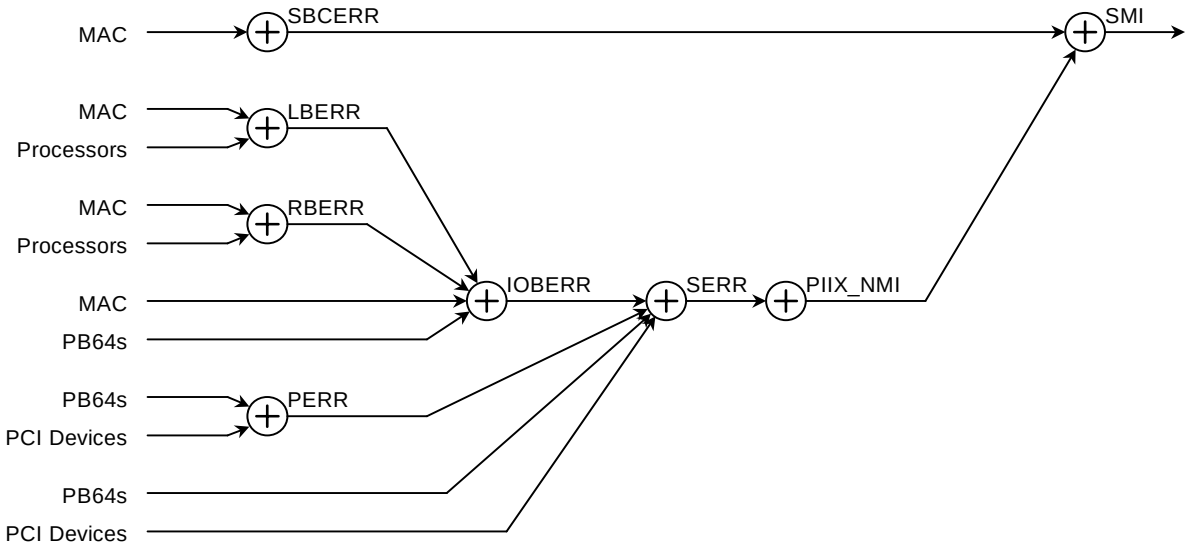

Figure 9-2: Error Reporting Paths

The system BIOS logs events in accordance with the *Intelligent Platform Management Interface Specification*. In keeping with that architecture, each event is treated as a sensor. The event-specific portion of each error consists of six data bytes. The first three bytes describe the sensor. The last three bytes describe the event itself.

In keeping with Table 3-2 of the *IPMI Specification v0.9*, the OCPRF100 BIOS defines several System Software Ids for events generated by BIOS, the User Binary, and the SMI Handler. The table below defines these platform-specific IDs.

Table 9-6: System Software IDs for OCPRF100 BIOS

BIOS Area	System Software ID
POST, System BIOS	00h
POST, User-Binary	01h
SMM, System BIOS	10h
SMM, User-Binary	11h

The table below shows the errors recorded in the SEL by the BIOS. See the individual component specifications for information about the specific error conditions detected by each device.

Table 9-7: Run-time Errors Handled by the OCPRF100 MP Server System BIOS

Error Type	Detected By	Reporting Signal	SEL Entry	NMI?
ECC Memory Errors				
Correctable	MAC	SBCERR	0Ch 01h E7h 40h [a] [b]	No
Uncorrectable	MAC	BERR	0Ch 01h E7h 41h [a] [b]	Yes
Event Logging Disabled				
Correctable Memory Errors Disabled	MAC	SBCERR	0Ch 02h E7h 00h FFh FFh	No
Correctable Bus Errors Disabled	MAC	SBCERR	0Ch 02h E7h 41h 00h 00h	No
Coherency Filter Errors				
Coherency Filter Parity Error	MAC	SBCERR	19h 05h 07h 42h 00h [c]	No†
Cache Protocol Error	MAC	BINIT	19h 05h 07h 42h 01h FFh	No†
System Bus Errors				
Address Parity Error	MAC	AERR/BINIT	13h 04h E7h 48h 09h [d]	No†
Address Parity Error	PB64	AERR/BINIT	13h 04h E7h 48h 09h [e]	No†
Request Parity Error	MAC	AERR/BINIT	13h 04h E7h 48h 01h FFh	No†
Request Parity Error	PB64	AERR/BINIT	13h 04h E7h 48h 01h FFh	No†
BINIT, driven by processor	MAC	BINIT	13h 04h E7h 48h 0Ah [d]	No†
BERR, driven by processor	MAC	BERR	13h 04h E7h 48h 0Ah [d]	Yes
Protocol Violation	MAC	BINIT	13h 04h E7h 48h 0Ch [d]	No†

Table 9-7: Run-time Errors Handled by the OCPRF100 MP Server System BIOS (Continued)

Protocol Violation	PB64	BINIT	13h 04h E7h 48h 0Ch [e]	No†
Response Parity Error	PB64	AERR/BINIT	13h 04h E7h 48h 0Eh [e]	No†
Correctable Data Error	MAC	SBCERR	13h 04h E7h 47h 00h FFh	No
Uncorrectable Data Error	MAC	BERR	13h 04h E7h 48h 0Fh [d]	Yes
Uncorrectable Data Error	PB64	BERR	13h 04h E7h 48h 0Fh [e]	Yes
PCI Bus Errors				
Data Parity Error on Transmit Cycle	PB64	PERR	13h 06h E7h 48h 15h [e]	Yes††
Data Parity Error on Receive Cycle	PB64	PERR	13h 06h E7h 48h 16h [e]	Yes††
Nonspecific Data Parity Error Reported, all other cases	PB64	PERR	13h 06h E7h 44h 03h [e]	Yes††
Address Parity Error	PB64	SERR	13h 06h E7h 48h 17h [e]	Yes
Inbound Timeout Error	PB64	SERR	13h 06h E7h 48h 04h [e]	Yes
Target Abort	PB64	SERR	13h 06h E7h 48h 05h [e]	Yes
Nonspecific Data Parity Reported, PB64 as master	PB64	PERR	13h 06h E7h 04h 00h [e]	Yes††
Unknown System Error signaled	PB64	SERR	13h 06h E7h 05h 00h [e]	Yes
Other Errors				
I/O Channel Check NMI detected	PIIX4	PIIX_NMI	13h 03h E7h 02h FFh FFh	Yes
POST Error	None	None	0Fh 4Eh E7h 41h [f] [g]	No
Other Events				
System Boot Event	None	None	12h 08h E7h 01h FFh FFh	No

[a] 00h for Left Memory Carrier, 01h for Right Memory Carrier

[b] Reference designator or “J-number” of Memory DIMM in binary. For example, 0Dh indicates J13.

[c] 00h for Left Coherency Filter, 01h for Right Coherency Filter

[d] 00h for Left P6 Bus, 01h for Right P6 Bus, 02h for P6 I/O Bus

[e] C8h for Segment A, D0h for Segment B, D8h for Segment C, C0h for Segment D

[f] LSB of four-digit POST error number

[g] MSB of four-digit POST error number..

Table 9-7: Run-time Errors Handled by the OCPRF100 MP Server System BIOS (Continued)

†	Because these errors cause a reset, BIOS logs them on the reboot.
††	PERR is recoverable according to the PCI specification. Logging is controlled by BIOS Setup.

9.3.2.5.4 Throttling Prevention

The system detects, corrects, and logs correctable errors as indicated in the table above. As long as these errors occur infrequently, the system should continue to operate without a problem.

Occasionally, correctable errors are caused by a persistent failure of a single component. For example, a broken data line on a DIMM would exhibit repeated errors until replaced. Although these errors are correctable, continual calls to the error logger can throttle the system, preventing any further useful work.

For this reason, the system counts certain types of correctable errors and disables reporting if they occur too frequently. Correction remains enabled but calls to the error handler are disabled. This allows the system to continue running, despite a persistent correctable failure. BIOS adds an entry to the event log to indicate that logging for that type of error has been disabled. Such an entry indicates a serious hardware problem that must be repaired at the earliest possible time.

The system BIOS implements this feature for two types of errors detected by the MAC: correctable memory errors and correctable bus errors. If ten errors occur in a single hour, the corresponding error handler disables further reporting of that type of error. A unique counter is used for each type of error; i.e., an overrun of memory errors does not affect bus error reporting.

Each one-hour period is measured from 0 minutes, 0 seconds to 59 minutes, 59 seconds. When an error is reported, the error handler reads the month, day, year, and hour from the real-time clock. If these fields do not match the timestamp of the previous error, BIOS resets the count for a new hour. This measurement method avoids the arcane details of calendar arithmetic without compromising protection against throttling.

9.3.2.6 CMOS Default Override

The system provides a method to revert back to configuration defaults in hardware, without relying on the ability to boot BIOS Setup or the SSU. The OPRF100 board set contains a configuration jumper on the I/O carrier. If set to “Clear CMOS” prior to reset, BIOS discards the current configuration settings and installs default settings.

Early in POST, BIOS checks the jumper. If set, BIOS restores CMOS configuration RAM, the ESCD, SCSI NVRAM, and the PCI IRQ tables to the default state. Password settings are not affected.

BIOS also may decide to clear the ESCD if its checksum fails or if the “Reset SCD” switch is set to “Yes” in BIOS Setup.

9.3.2.7 BIOS Recovery

If the system fails to complete POST and boot an operating system, it may be necessary to run the BIOS recovery procedure.

By moving a jumper on the OPRF100 I/O carrier, BIOS executes the recovery BIOS (also known as the boot block) instead of the normal BIOS. The recovery BIOS is a self-contained image that exists solely as a fail-safe mechanism for installing a new BIOS image. The recovery BIOS boots from a floppy diskette only. It does not display anything on the video screen during the recovery process.

Section Performing BIOS Recovery explains the recovery procedure.

9.3.3 Manageability

9.3.3.1 Console Redirection

BIOS supports redirection of both video and keyboard via a serial link (COM 1 or COM 2). When console redirection is enabled, local (host server) keyboard input and video output are passed both to the local keyboard and video connections, and to the remote console via the serial link. Keyboard inputs from both sources are considered valid and video is displayed to both outputs. Optionally, the system can be operated without a host keyboard or monitor attached to the system and run entirely via the remote console. Only text-based programs such as BIOS Setup can be accessed via console redirection.

9.3.3.1.1 Operation

When redirecting through a modem (as opposed to a Null modem cable), the modem needs to be configured with the following:

- Auto-answer (e.g., ATS0=2 to answer after 2 rings).
- Modem reaction to DTR set to return to command state (e.g., AT&D1).

Failure to provide #2 above causes the modem to either drop the link when the server reboots (as in AT&D0), or makes the modem unresponsive to server baud rate changes (as in AT&D2).

The BIOS Setup option for handshaking must be set to CTS/RTS + CD. The CD refers to carrier detect. This prevents the server from sending video updates to a modem that is not connected to a remote modem. If this is not selected, video update data being sent to the modem will inhibit many modems from answering an incoming call.

If console redirection is enabled, redirection code is loaded into memory and activated during POST. While redirection cannot be unshadowed without rebooting, it can be inhibited and restarted. When inhibited, the serial port is released by redirection and may be used by another application. Restarting reclaims the serial port and continues redirection. Inhibiting/restarting is accomplished through the following interrupt 16h mechanism. The standard interrupt 16h (keyboard handler) function AH=05h places a keystroke in the key buffer, just as if an actual key had been pressed. Keystrokes so buffered are examined by redirection, and if a valid command string has been sent, it is executed. The following commands are supported in this fashion:

```
Esc C D Z 0 - Inhibit Console Redirection.
Esc C D Z 1 - Restart Console Redirection.
```

In order to inhibit redirection, the software must call interrupt 16h, function ah=05h five times to place the five keys in the key buffer. Keystrokes sent to the interrupt 16h buffers are buffered and should be removed via the normal interrupt 16h calls to prevent these keystrokes from being passed on to another application.

9.3.3.1.2 Keystroke Mappings

During console redirection, the remote terminal (which may be a dumb terminal or a system with a modem running a communication program, such as ProComm*) sends keystrokes to the local server. The local server passes video back over this same link.

For keys that have an ASCII mapping, such as A and Ctrl+A, the remote simply sends the ASCII character. For keys that do not have an ASCII mapping, such as F1 and Alt+A, the remote must send a string of characters, as defined in the tables below. The strings are based on the ANSI terminal standard. Since the ANSI terminal standard does not define all the keys on the standard 101-key U.S. keyboard, mappings for these keys were created, such as F5 – F12, Page Up, and Page Down.

Alt key combinations are created by sending the combination `^[}` followed by the character to be Alt-modified. Once the Alt key combination is sent, the next keystroke is translated into its Alt-key mapping. For example, the sequence `^[}a` sends an `Alt-a` to the server. Unusual combinations outside of the ANSI mapping and not listed in the table below, are not supported (e.g., Ctrl+F1).

Table 9-8: Non-ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
ESC	^[	NS	NS	NS
F1	^[OP	NS	NS	NS
F2	^[OQ	NS	NS	NS
F3	^[OR	NS	NS	NS
F4	^[OS	NS	NS	NS
F5	^[OT	NS	NS	NS
F6	^[OU	NS	NS	NS
F7	^[OV	NS	NS	NS
F8	^[OW	NS	NS	NS
F9	^[OX	NS	NS	NS
F10	^[OY	NS	NS	NS
F11	^[OZ	NS	NS	NS

Table 9-8: Non-ASCII Key Mappings

F12	^[O1	NS	NS	NS
Print Screen	NS	NS	NS	NS
Scroll Lock	NS	NS	NS	NS
Pause	NS	NS	NS	NS
Insert	^[[L	NS	NS	NS
Delete	(7Fh)	NS	NS	NS
Home	^[[H	NS	NS	NS
End	^[[K	NS	NS	NS
Pg Up	^[[M	NS	NS	NS
Pg Down	^[[2J	NS	NS	NS
Up Arrow	^[[A	NS	NS	NS
Down Arrow	^[[B	NS	NS	NS
Right Arrow	^[[C	NS	NS	NS
Left Arrow	^[[D	NS	NS	NS
Tab	(09h)	NS	NS	NS

NOTES: NS = Not supported, (xxh) = ASCII character xx.

Table 9-9: ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
backspace	(08h)	(08h)	(7Fh)	^[}(08h)
(accent) ‘	‘	(tilde) ~	NS	^[}‘
1	1	!	NS	^[}1
2	2	@	NS	^[}2
3	3	#	NS	^[}3
4	4	$	NS	^[}4
5	5	%	NS	^[}5
6	6	^	NS	^[}6
7	7	&	NS	^[}7
8	8	*	NS	^[}8

Table 9-9: ASCII Key Mappings (Continued)

9	9	(	NS	^[}9
0	0	)	NS	^[}0
(dash) -	-	(under) _	(1Fh)	^[}-
=	=	+	NS	^[}=
a to z	a to z	A to Z	(01h) to (1Ah)	^[}a to ^[}z
[	[	{	(1Bh)	^[}[
]	]	}	(1Dh)	^[}]
\	\	|	(1Ch)	^[}\
(semi-colon) ;	;	(colon) :	NS	^[};
(apostrophe) ’	‘	(quote) "	NS	^[}'
(comma) ,	,	<	NS	^[},
(period) .	.	>	NS	^[}.
/	/	?	NS	^[}/
(space)	(20h)	(20h)	(20h)	^[}(20h)

NOTES: NS = not supported, (xxh) = ASCII character xx.

9.3.3.1.3 Limitations

Console redirection is a real-mode BIOS extension, and does not operate outside of real-mode. Console redirection will not work once the operating system or a driver like EMM386 takes the processor into protected mode. If an application takes the processor in and out of protected mode, it should inhibit redirection before entering protected mode and restart it once back into real mode. Video is redirected by scanning and sending changes in text video memory. Although console redirection supports text-based (ANSI) graphics characters, it does not support graphical VGA modes. Because keyboard redirection relies on the BIOS interrupt 16h handler, software bypassing this handler does not receive redirected keystrokes.

9.3.3.1.4 Interface to Server Management

If BIOS determines that console redirection is enabled, it will read the current baud rate from CMOS and pass this value to the front panel controller via the IPMB.

9.3.3.2 DMI/SMBIOS Support

The DMI and SMBIOS interface provides a method of managing computers in an enterprise. The main component of DMI is the management information format (MIF) database. This database

contains all the information about the computing system and its components. Using DMI, a system administrator can obtain the types, capabilities, operational status, installation date, and other information about the system components.

The system BIOS complies with revision 2.1 of the *SMBIOS Specification*, implementing all of the mandatory function calls. It follows the system device node model used by Plug and Play, and uses Plug and Play BIOS functions to access DMI information. Plug and Play functions 50h-5Fh are assigned for the SMBIOS interface. Each of the SMBIOS Plug and Play functions is available both in real mode and 16-bit protected mode.

BIOS constructs a table in shadow memory containing DMI information, so that it is available to the drivers that require this information but that cannot perform BIOS calls. The table contains two parts:

- SMBIOS entry point header structure.
- SMBIOS structure table.

The SMBIOS structure entry point can be found in the F0000h to FFFFFh physical address area of memory and is paragraph (16 byte) aligned. The table below shows the DMI BIOS header structure.

Table 9-10: DMI BIOS Header Structure

Element	Length	Description
Header	5 Bytes	_DMI_
Checksum	1 Byte	Checksum of SMBIOS header structure.
Length	2 Bytes	Total length of SMBIOS structure table.
BIOS Structure Table Address	4 Bytes	32-bit physical address of beginning of byte aligned DMI structure table.
NumStructures	1 Byte	Total number of structures within the structure table.
DmiBIOSRevision	1 Byte	Revision of the SMBIOS extensions.

The SMBIOS structure table contains all of the SMBIOS structures fully packed together. The data is in the exact format returned by calling function 51h, GetDmiStructure. This table is static. BIOS creates this table before passing control to the operating system and does not update it while the operating system is running, even if there are configuration changes.

The system BIOS supports the following SMBIOS types:

- Type 0 – System BIOS
- Type 0 – Video BIOS

- Type 0 – SCSI BIOS
- Types 1 through 13
- Type 16
- Type 17

The BIOS supports general purpose nonvolatile (GPNV) storage as described by the SMBIOS specification. Programs should call function 55h, GetGPNVInfo, to determine the size and availability of GPNV areas. The table below lists the handles supported by the BIOS.

Table 9-11: SMBIOS GPNV Handles

Handle	Size	Use
0	-	Intel Reserved
1	-	Intel Reserved
2	-	Intel Reserved
3	-	Embedded Symbios* Parameters
4	100h	OEM Use
5	800h	OEM Use

Flashing a new version of BIOS does not clear OEM GPNV areas.

9.3.4 Security

The OCPRF100 MP server system BIOS provides a number of security features. This section describes the security features and operating model. Some of these events, such as entering secure mode via hot key, cannot take place unless the keyboard is connected to the keyboard controller, and are not supported when the keyboard is connected to a USB port.

9.3.4.1 Operating Model

The table below summarizes the operation of security features supported by the system BIOS.

Table 9-12: Security Features Operating Model

Mode	Entry Method/ Event	Entry Criteria/Qualifier	Behavior	Exit Criteria	After Exit
Secure mode	Keyboard Inactivity Timer, Secure Mode Button, Programming of Keyboard Controller Hot Key	User Password/ keyboard controller inactivity timer (set by BIOS Setup)	Screen goes blank (if enabled in Setup). Floppy writes are disabled (if selected in Setup). Power and reset switches on the front panel are disabled. No mouse or keyboard input is accepted.	User password	Video is restored. Floppy writes are enabled. Power and reset switches are enabled. Keyboard and mouse inputs are accepted.
Secure boot	Power On/Reset	User password/ secure boot enabled in BIOS Setup	Boots drive C, if drive A is empty. Prompts for password, if not empty. Video is blanked (if enabled in Setup). Floppy writes are disabled (if programmed in Setup). Power and reset switches on the front panel are disabled. No mouse or keyboard input is accepted; however, the mouse driver can be allowed to load before a password is required.	User password	Floppy writes are enabled. Power and reset switches are enabled. Keyboard and mouse inputs are accepted. System attempts to boot from drive A.
User password boot (AT style)	Power On/Reset	User password/ secure boot disabled in BIOS Setup	System halts for user password before booting. Video is blanked (if enabled in Setup). Power and reset switches on the front panel are disabled. No mouse or keyboard input is accepted.	User password	Power and reset-switches are enabled. Keyboard and mouse inputs are accepted. Boot sequence is determined by Setup options.
Power and reset switch lockout	Same as “Secure Mode” above	User-programmed bit (using BIOS Setup)	Power and reset buttons are disabled on front panel.	User clears the bit	Power and reset switches enabled.

9.3.4.2 Password Protection

BIOS supports passwords to reduce the risk of tampering with the system. A user and administrator password can be set in BIOS Setup.

If only the user password is set, BIOS accepts the user password to boot the machine, exit secure mode, or run BIOS Setup. If both passwords are enabled, BIOS accepts either password to boot the machine, exit secure mode, or enable the mouse; however, it requests an administrator password before changing the system configuration through BIOS Setup.

The administrator password controls access to basic system configuration, independently from other access controls. For example, an administrator can modify the system hardware configuration while others can access the machine's file system.

Once set, a password can be disabled by changing it to a null string or by setting the "Clear Password" jumper on the OPRF100 I/O carrier.

9.3.4.2.1 Inactivity Timer

If the inactivity timer function is enabled, and no keyboard or mouse actions have occurred for the specified time-out period, the following occurs until the user password is entered:

- Keyboard and mouse input is inhibited.
- Video is blanked (if enabled).
- Floppy drive is write protected (if enabled).
- Front panel buttons are locked out (if enabled).

The user may specify a time-out period of 1 to 120 minutes.

9.3.4.2.2 Hot Key Activation

A hot key can activate secure mode immediately, without waiting for the inactivity time-out to expire. BIOS Setup allows the user to select the hot key.

9.3.4.2.3 Clear Password Jumper

BIOS reads the "Clear Password" jumper (located on the OPRF100 I/O carrier) to determine if it is set. If set, any passwords are cleared from CMOS and password protection is disabled.

9.3.4.2.4 Boot Without Keyboard

The system can boot with or without a keyboard. The presence of the keyboard is detected automatically during POST, and the keyboard is tested if present. There is no Setup option for enabling and disabling the keyboard.

9.3.4.2.5 Floppy Write Protection

If enabled in BIOS Setup, floppy disk writes are disabled when the system is in secure mode. Floppy write protection is in effect only while the system is in secure mode. Otherwise, write protection is disabled.

9.3.4.3 Front Panel Lock

If enabled in BIOS Setup, the front panel, power switch, and reset button are disabled when in secure mode.

9.3.4.4 Secure Boot Mode

Secure boot mode lets the system boot and run the OS, but no mouse or keyboard input is accepted until the user password is entered. In secure boot mode, if the BIOS detects a floppy disk in the A drive at boot time, it prompts the user for a password. When the password is entered, the system can boot from the floppy and secure mode is disabled. Any one of the secure mode triggers, as described in the previous table, causes the system to return to secure mode. If there is no disk in drive A, the system boots from the C drive and is placed in secure mode automatically. All of the secure mode features (that are enabled) go into effect at boot time.

Secure boot mode can be enabled through the BIOS Setup.

9.3.4.5 Video Blanking

If enabled in BIOS Setup, the video display is blanked out when the system is in secure mode. Exiting secure mode enables the video display.

9.3.4.6 Emergency Management Port (EMP)

The emergency management port (EMP) feature of server management allows the front panel controller to communicate via serial port even if the system power is off. This could be used for remote power cycling of the system, for example. This feature can be enabled by an administrator through BIOS Setup.

The administrator can set or change the password through BIOS Setup. The BIOS installs the EMP password by sending the appropriate commands over the IPMB. Because BIOS Setup supports an administrator password, the EMP password can be changed without entering the current EMP password.

The EMP password can be cleared through BIOS Setup or by setting the “Clear Password” jumper on the OPRF100 I/O carrier.

9.3.5 Customization

System OEMs can differentiate their products by customizing the BIOS. The extent of customization is limited to what is stated in this section.

The user binary capability of the system BIOS allows system vendors to change the look and feel of BIOS and to manage OEM-specific hardware by executing custom code during POST. Custom code should not hook critical interrupts, reprogram the chip set, or take any other action that affects the correct functioning of system BIOS.

9.3.5.1 User Binary

System customers can supply up to 16 KB of code and data for use during POST and at run-time. User binary code is executed at several defined hook points within POST. An additional hook point is defined within the SMM handler.

The user binary code is stored in the system flash. If no run-time code is added, BIOS temporarily allocates a code buffer according to the *POST Memory Manager Specification*. If run-time code is present, BIOS shadows the entire 16 KB block as though it were an option ROM. BIOS leaves this region writeable to allow the user binary to update any data structures it defines. System software can locate a run-time user binary by searching for it like an option ROM, checking each 2KB boundary from C0000h to EFFFFh. The system vendor can place a signature within the user binary to distinguish it from other option ROMs.

The BIOS detects a user binary by examining the structure in the table below. When shadowed, this structure is compatible with the standard option ROM header.

Table 9-13: User Binary Header

Offset	Value	Description
00h	AA55h	ROM Signature
02h	20h	Length (16 KB)
03h	CBh	Opcode for RET FAR
04h	varies	Mask Byte
05h	JMP CS:IP	CS:IP is User SMM Code
0Ah	JMP CS:IP	CS:IP is User Code for After Video Initialization
0Fh	JMP CS:IP	CS:IP is User Code for Before Video Initialization
14h	JMP CS:IP	CS:IP is User Code for POST Errors
19h	JMP CS:IP	CS:IP is User Code for Before Int19h
1Eh	JMP CS:IP	CS:IP is User Code for Before ROM Scan
23h	JMP CS:IP	CS:IP is User Code for After ROM Scan

BIOS examines bytes 0 through 3 of the header. If they do not match, BIOS ignores the user binary.

Bit 0 of byte 4 indicates whether the code is disposable or not. If bit 0 is 1, BIOS assumes the code only executes during POST and that no code is intended for run-time. If bit 0 is 0, BIOS assumes the runtime code is present and that the entire user binary must persist after the operating system is booted.

Bits 7 through 1 of byte 4 indicate which user hooks should be executed. The table below describes these hooks.

Table 9-14: User Binary Hook Points

Scan Point	Mask	RAM/Stack/BDA	Video/Keyboard
Disposable flag	01h	Not applicable.	Not applicable.
This scan occurs only as a result of an SMI. For security reasons, the OCPRF100 MP server system BIOS copies the SMM user code to SMRAM and executes it from SMRAM. SMM code cannot make far calls.	02h	A stack is assured.	Video memory and INT 10h services are not accessible since SMRAM is mapped over the top of where video RAM usually is. Keyboard services are not available through BIOS, although port accesses to the keyboard are possible. All the restrictions that are placed on SMM code apply.
This scan occurs immediately **after** video initialization.	04h	Yes	Yes
This scan occurs immediately **before** video initialization.	08h	Yes	No
This scan occurs on POST error. On entry, BX contains the number of the POST error.	10h	Yes	Yes
This is the final scan. It occurs immediately **prior** to the INT 19 for normal boot and allows user code to completely circumvent the normal INT 19 boot, if desired.	20h	Yes	Yes
This scan occurs immediately **before** the normal external ROM scan.	40h	Yes	Yes
This scan occurs immediately **following** the normal external ROM scan.	80h	Yes	Yes

The user SMM code executes near the end of the SMI handler, after BIOS has processed the SMI event. As such, the user code cannot circumvent the standard handling of the event. It cannot be used to prevent logging or to prevent the assertion of NMI. However, it can be used to create additional error records and to assert NMI, if desired.

The following code fragment demonstrates a user binary.

```
;
; The SCAN_MASK determines which user binaries are used
; and whether the user binary is disposable or persists
; after POST.
;
FLAG_DISPOSABLE         EQU   00000001b
```

```
FLAG_SMM                EQU   00000010b
FLAG_POST_VIDEO         EQU   00000100b
FLAG_PRE_VIDEO          EQU   00001000b
FLAG_POST_ERROR         EQU   00010000b
FLAG_INT19              EQU   00100000b
FLAG_PRE_ROM_SCAN       EQU   01000000b
FLAG_POST_ROM_SCAN      EQU   10000000b

SCAN_MASK   EQU    FLAG_SMM              \
                 + FLAG_POST_VIDEO       \
                 + FLAG_PRE_VIDEO        \
                 + FLAG_POST_ERROR       \
                 + FLAG_INT19            \
                 + FLAG_PRE_ROM_SCAN     \
                 + FLAG_POST_ROM_SCAN    \
                 + FLAG_DISPOSABLE

cseg SEGMENT USE16 PUBLIC 'CODE'

;
; Define the Entry Points of the user binary
;
EntryPoints PROC FAR                ; MUST be a far procedure
      db    055h
      db    0AAh
      db    020h              ; 16K USER Area
      retf
      db   SCAN_MASK          ; Scan mask
      retf
entryReserved:
      dw    0
      dw    0
entrySMM:
      jmp   NEAR PTR userSMM
      dw    0
entryPostVideo:
      jmp   NEAR PTR userPostVideo
      dw    0
entryPreVideo:
      jmp   NEAR PTR userPreVideo
      dw    0
entryPostError:
      jmp   NEAR PTR userPostError
      dw    0
entryInt19:
      jmp   NEAR PTR userInt19
      dw    0
```

```
entryPreRomScan:
      jmp   NEAR PTR userPreRomScan
      dw    0
entryPostRomScan:
      jmp   NEAR PTR userPostRomScan
      dw    0
userReturn::                      ; common exit point
      retf
EntryPoints ENDP


userSmm PROC NEAR
      jmp   userReturn
userSmm ENDP

userPostVideo PROC NEAR
      jmp   userReturn
userPostVideo ENDP

userPreVideo PROC NEAR
      jmp   userReturn
userPreVideo ENDP

userPostError PROC NEAR
      jmp   userReturn
userPostError ENDP

userInt19PROC NEAR
      jmp   userReturn
userInt19ENDP

userPreRomScan PROC NEAR
      jmp   userReturn
userPreRomScan ENDP

userPostRomScan PROC NEAR
      jmp   userReturn
userPostRomScan ENDP

;pad  equ   1000h-($-EntryPoints)     ; 4K USER Area
;pad  equ   2000h-($-EntryPoints)     ; 8K USER Area
pad   equ   4000h-($-EntryPoints)     ; 16K USER Area

    db   pad dup(0)       ; Pad to proper size

cseg  ends              ; End of CSEG segment
```

```
END
```

A user binary can be created and installed as follows:

Assemble and link the file using MASM* or other suitable assembler. This will create `mybinary.exe`.

Convert the EXE to a HEX file by executing `EXE2HEX mybinary`.

Convert the HEX file into a flashable USR file by executing `MAKEUSER mybinary.hex /s16`. The argument indicates that the size of the user binary should be 16KB.

Copy `mybinary.usr` and `iflash.exe` to a floppy disk. Insert the floppy, execute `iflash.exe`, and select `mybinary.usr` as the file to flash.

Reboot the system when prompted. The user binary should execute during POST.

Additional information about iFLASH is located in Chapter Flash Utility.

9.3.5.2 Language

The system BIOS supports five languages at a time. iFLASH is used to load language support that replaces the text strings for POST and general error messages with text strings translated into a particular language.

Intel provides specifications for all BIOS text strings, so that any OEM can have them translated and prepared for updating with iFLASH. By default, the system BIOS provides translations for English, Spanish, French, German, and Italian. The language can be selected using BIOS Setup.

9.3.5.3 Server Management Interface

The BIOS communicates with the IPMB by reading and writing the SMIC using three registers in I/O space. BIOS provides a real-mode interface to the IPMB using extensions to interrupt 15h function calls.

The BIOS provides several methods for exchanging data with OEM code as described in the following sections.

9.3.5.3.1 Echo Feature

The echo feature reroutes system event messages to system BIOS via the SMIC interface. The BIOS provides a user binary hook that allows custom code to acknowledge a critical event and to query the event log record. User binary or user system software is responsible for enabling this feature in the BMC interrupt flag register; if enabled, the BMC generates an SMI interrupt. The SMM handler is invoked; it retrieves this log record from the firmware subsystem, and stores this record in the OEM ELOG buffer, which resides in SMRAM. Just before exiting, the SMM handler passes control to the user binary for further processing. The user binary is responsible for managing this buffer; it must clean and reinitialize the buffer after processing the data.

9.3.5.3.2 SMM Messaging

SMM messaging is similar to the echo feature in that a user binary or system software can enable SMM messaging by setting the BMC interrupt flag register to allow all SMM messages to be passed from the IPMB to the system BIOS. Again, this feature is established with an SMI interrupt. These messages are passed into the OEM SMM buffer in SMRAM for processing. The BIOS is responsible for the IPMB protocols that transmit and receive data over the SMIC interface. The user binary is responsible for validating the data. The user binary is also responsible for managing this buffer; it must clean and reinitialize the buffer after processing the data.

9.3.5.3.3 SMS Messaging

This feature is similar to the SMM messaging feature except that a different bit is set in the BMC interrupt flag register. The data stream is stored in OEM SMS buffers.

9.3.5.3.4 ELOG Messaging

Before logging an event to the SEL, the SMM handler stores the event in the OEM ELOG buffer, a 16-byte buffer in SMRAM. Only events that are monitored and reported by the BIOS SMM handler are copied into this buffer.

The first byte of the buffer indicates the length of the record. The remaining bytes contain the event record as specified in Appendix C.

9.3.5.3.5 Buffer Allocation

The system BIOS allocates five buffers in SMRAM as shown in the table below.

Table 9-15: User Buffers Allocated for IPMB Interfaces

Buffer Types	Length	Usage
OEM User Area	128 bytes	Free for use by OEM
OEM SMM Buffer	64 bytes	Stores SMM messages
OEM EMSG Buffer	64 bytes	Stores event messages from IPMB
OEM SMS Buffer	64 bytes	Stores SMS messages
OEM ELOG Buffer	16 bytes	Stores system event log record

User binary code can locate the buffers by examining the structure shown in the table below. The structure is located in SMRAM at offset 0006h. User binary code must examine the revision before using the data in the structure.

Table 9-16: Pointers to User Buffers

Offset	Bytes	Name
0006h	4	Revision – “2.00”
000Ah	2	SMM Data Segment
000Ch	2	OEM User Area
000Eh	2	OEM SMM Buffer
0010h	2	OEM Event Message Buffer
0012h	2	OEM SMS Buffer

NOTES: This structure may be altered after system reset.

9.4 BIOS Setup Utility

The OCPRF100 MP server system BIOS automatically configures system resources. BIOS Setup allows the user to set preferences about system operation. It stores these preferences in CMOS configuration RAM. Because BIOS Setup resides in flash ROM, the user can invoke it without booting an operating system.

During POST, BIOS prompts the user to enter BIOS Setup with the following message:

```
Press <F2> to enter Setup
```

After the user presses F2, a few seconds may pass while BIOS completes its test and initialization tasks.

BIOS Setup supports security passwords, which reduces the risk of unauthorized modifications. If enabled, BIOS Setup requests an administrator password before allowing modifications.

Screen Format. The BIOS Setup screen is divided into four functional areas.

Table 9-17: BIOS Setup Screen Functional Areas

Menu Selection Bar	Located at the top of the screen, the Menu Selection Bar allows the user to select the top level menus. These are the Main Menu, Advanced Menu, Security Menu, Server Menu, and Boot Menu.
Menu Area	Located at the center of the screen, the Menu Area displays options and information. Some items have submenus.

Table 9-17: BIOS Setup Screen Functional Areas (Continued)

Item Specific Help	Located at the right side of the screen, this area supplies help messages for the menu items.
Keyboard Command Bar	Located at the bottom of the screen, the Keyboard Command Bar displays keyboard commands for modifying settings and for navigating through the menus and submenus.

Keyboard Commands. BIOS Setup supports the following keystroke commands.

Table 9-18: Keystroke Commands

F1	**Help**	Pressing F1 on any menu invokes the general help window.
ESC	**Exit**	The Escape key allows the user to back out of any field. When the Escape key is pressed while editing a field, the edit of that field is terminated. When the Escape key is pressed in a submenu, the parent menu is re-entered. When it is pressed in a top-level menu, the Exit Menu appears.
¦	**Select Item**	The up arrow selects the previous value in an option list.
Ø	**Select Item**	The down arrow selects the next value in an option list.
´	**Select Menu**	The left and right arrow keys move between top level menus.
-	**Change Value**	The minus key changes the value of an item to the previous value in the list.
+	**Change Value**	The plus key changes the value of an item to the next value in the list. Pressing the space bar performs the same function.
Enter	**Execute Command**	The Enter key activates submenus, selects options, and changes an item's value.
F9	**Setup Defaults**	The F9 key restores the default values for configuration options. A pop-up menu confirms the choice before modifying the values.
F10	**Save and Exit**	The F10 key saves the settings and reboots the system. A pop-up menu confirms the choice before saving the values.

9.4.1 Main Menu

The tables below describe the Main Menu and its submenus.

Table 9-19: Main Menu

Feature	Option	Description
System Time	HH:MM:SS	Sets the system time.
System Date	MM/DD/YYYY	Sets the system date.
Legacy Diskette A:	Disabled 360Kb, 5 ¼” 1.2Mb, 5 ¼” 720Kb, 3 ½” 1.44/1.25Mb, 3 ½”† 2.88Mb, 3 ½”	Selects the floppy diskette type for drive A.
Legacy Diskette B:	Disabled† 360Kb, 5 ¼” 1.2Mb, 5 ¼” 720Kb, 3 ½” 1.44/1.25Mb, 3 ½” 2.88Mb, 3 ½”	Selects the floppy diskette type for drive B.
Primary Master		Selects IDE submenu.
Primary Slave		Selects IDE submenu.
Processor Information		Selects Processor Information submenu.
Keyboard Features		Selects Keyboard Features submenu.
Language	English (US)† French German Italian Spanish	Selects language used by BIOS.

NOTES: Default values are marked with the "†" symbol.

Table 9-20: IDE Submenu

Feature	Option	Description
Autotype Fixed Disk		Pressing the Enter key instructs BIOS Setup to detect the type of fixed disk. If successful, the remaining value fields on this menu are automatically filled in.

Table 9-20: IDE Submenu (Continued)

Type	None CD-ROM IDE Removable ATAPI Removable User Auto†	If “Auto” is selected, BIOS determines the parameters during POST. If “User” is selected, BIOS Setup prompts the user to fill in the drive parameters. Drive types 1 through 39 are predetermined drive types.
Cylinders		Displays the number of cylinders.
Heads		Displays the number of read/write heads.
Sectors		Displays the number of sectors per track.
Maximum Capacity		Displays the capacity of the drive.
Multisector Transfers	Disabled 2 Sectors 4 Sectors 8 Sectors 16 Sectors	Displays status of multisector transfers. Autotyped by BIOS.
LBA Mode Control	Disabled Enabled	Displays status of Logical Block Access. Autotyped by BIOS.
32 Bit I/O	Disabled† Enabled	Enables 32-bit IDE data transfers.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4	Selects the method for transferring data to/from the drive. Auto-typed by BIOS.
Ultra-DMA Mode	Disabled Mode 0 Mode 1 Mode 2	Selects the Ultra-DMA mode used for transferring data to/from the drive. Autotyped by BIOS.

NOTES: Default values are marked with the "†" symbol.

Table 9-21: Processor Information Submenu

Feature	Option	Description
Left Processor 1 Stepping ID		Displays the stepping of the processor.
Left Processor 1 L2 Cache Size		Displays the size of the L2 cache.
Left Processor 2 Stepping ID		Displays the stepping of the processor.
Left Processor 2 L2 Cache Size		Displays the size of the L2 cache.

Table 9-21: Processor Information Submenu (Continued)

Left Processor 3 Stepping ID		Displays the stepping of the processor.
Left Processor 3 L2 Cache Size		Displays the size of the L2 cache.
Left Processor 4 Stepping ID		Displays the stepping of the processor.
Left Processor 4 L2 Cache Size		Displays the size of the L2 cache.
Right Processor 1 Stepping ID		Displays the stepping of the processor.
Right Processor 1 L2 Cache Size		Displays the size of the L2 cache.
Right Processor 2 Stepping ID		Displays the stepping of the processor.
Right Processor 2 L2 Cache Size		Displays the size of the L2 cache.
Right Processor 3 Stepping ID		Displays the stepping of the processor.
Right Processor 3 L2 Cache Size		Displays the size of the L2 cache.
Right Processor 4 Stepping ID		Displays the stepping of the processor.
Right Processor 4 L2 Cache Size		Displays the size of the L2 cache.

Table 9-22: Keyboard Features Submenu

Feature	Option	Description
Numlock	Auto† On Off	Selects the power-on state of the Num Lock key.
Key Click	Disabled† Enabled	Enables key click.
Keyboard auto-repeat rate	30/sec† 26.7/sec 21.8/sec 18.5/sec 13.3/sec 10/sec 6/sec 2/sec	Selects key repeat rate.
Keyboard auto-repeat delay	¼ sec ½ sec† ¾ sec 1 sec	Selects delay before key repeat.

NOTES: Default values are marked with the "†" symbol.

9.4.2 Advanced Menu

The tables below describe the Advanced Menu and submenus.

Warning: Setting items on this menu to incorrect values may cause the system to malfunction.

Table 9-23: Advanced Menu

Feature	Option	Description
Processor Serial Number	Disabled Enabled†	Enables or disables the Processor Serial Number feature of the Pentium® III Xeon™ processor.
Reset Configuration Data	No† Yes	If “Yes” is selected, BIOS clears System Configuration Data during the next boot. The field is automatically reset to “No” in next boot.
System Wakeup Feature	Disabled† Enabled	Enables Wake on LAN* for operating systems that do not support ACPI. If the operating system enables ACPI, this mode has no effect.
Use Multiprocessor Specification	1.1 1.4†	Selects the version of MP spec to use. Some operating systems require version 1.1 for compatibility reasons.
Large Disk Access Mode	CHS LBA†	Select the drive access method for IDE drives. Most operating systems use LBA or "Logical Block Addressing." Some operating systems, however, may use the CHS or "Cylinder-Head-Sector" method.Consult your operating system documentation for more information.
Pause Before Boot	Disabled† Enabled	If enabled, BIOS pauses for five seconds before booting the operating system.
Hot-plug PCI Master Control	Disabled† Enabled	Set this to “Enable” to create the Hot-plug PCI Resource Table and to reserve resources for each hot-plug PCI slot.
Hot-plug PCI Allocation Level	Disabled: Min. † Max.	Set amount of resources to allocate to empty hot-plug PCI slots
PCI Configuration		Selects PCI Configuration submenu.
I/O Device Configuration		Selects I/O Device Configuration submenu.
Advanced Chip Set Control		Selects Advanced Chip Set Control submenu.

NOTES: Default values are marked with the "†" symbol.

Table 9-24: PCI Configuration Submenu

Feature	Option	Description
Processor Bus	100 MHz	Displays the clock speed of the Processor Bus.
PCI Slots 1-2	33 MHz	Displays the clock speed of PCI Segment A.
PCI Slots 3-6	33 MHz	Displays the clock speed of PCI Segment B.
PCI Slots 7-8	33 MHz 66 MHz	Displays the clock speed of PCI Segment C.
PCI Slots 9-10	33 MHz 66 MHz	Displays the clock speed of PCI Segment D.
PCI Bus Speed Default	33 MHz† 66 MHz	If no cards are present behind a 66 MHz capable PCI bus, this selects the speed (33 or 66 MHz) of that empty bus. If cards are present, this option is ignored and the slot speed is automatically determined.
PCI Device, Embedded SCSI		Selects PCI Mode Submenu for the embedded LVDS controller.
PCI Slot 1		Selects PCI Mode Submenu for this PCI slot.
PCI Slot 2		Selects PCI Mode Submenu for this PCI slot.
PCI Slot 3		Selects PCI Mode Submenu for this PCI slot.
PCI Slot 4		Selects PCI Mode Submenu for this PCI slot.
PCI Slot 5		Selects PCI Mode Submenu for this PCI slot.
PCI Slot 6		Selects PCI Mode Submenu for this PCI slot.
PCI Slot 7		Selects PCI Mode Submenu for this PCI slot.
PCI Slot 8		Selects PCI Mode Submenu for this PCI slot.
PCI Slot 9		Selects PCI Mode Submenu for this PCI slot.
PCI Slot 10		Selects PCI Mode Submenu for this PCI slot.

Table 9-25: PCI Mode Submenu

Feature	Option	Description
Option ROM Scan	Disabled Enabled†	Enables option ROM scan.
Enable Master	Disabled Enabled†	Enables device(s) as a PCI bus master.

Table 9-25: PCI Mode Submenu (Continued)

Latency Timer	Default 0020h 0040h 0060h 0080h† 00A0h 00C0h 00E0h	Specifies the minimum guaranteed number of PCI bus clocks that a device can master on a PCI bus during one transaction.

NOTES: Default values are marked with the "†" symbol.

Table 9-26: I/O Device Configuration Submenu

Feature	Option	Description
Serial Port A	Disabled Enabled† Auto	If set to “Auto,” BIOS configures the port.
Base I/O Address	3F8h† 2F8h 3E8h 2E8h	Selects the base I/O address for COM port A.
Interrupt	IRQ 3 IRQ 4†	Selects the IRQ for COM port A.
Serial Port B	Disabled Enabled† Auto	If set to “Auto,” BIOS configures the port.
Base I/O Address	3F8h 2F8h† 3E8h 2E8h	Selects the base I/O address for COM port B.
Interrupt	IRQ 3† IRQ 4	Selects the IRQ for COM port B.
Parallel Port	Disabled Enabled† Auto	If set to “Auto,” BIOS configures the port.
Mode	Output only Bidirectional† EPP ECP	Selects the mode of the LPT port.

Table 9-26: I/O Device Configuration Submenu (Continued)

Base I/O Address	378h† 278h 178h 3BCh	Selects the base I/O address for LPT port. 178h is only available when the LPT port is in EPP mode. Otherwise, 3BCh is available.
Interrupt	IRQ 5 IRQ 7†	Selects the IRQ for LPT port.
DMA channel	DMA 1 DMA 3†	Selects the DMA channel for LPT port when configured for ECP mode.
Floppy disk controller	Disabled Enabled† Auto	Enables embedded floppy disk controller.

NOTES: Default values are marked with the "†" symbol.

Table 9-27: Advanced Chip Set Control Submenu

Feature	Option	Description
Extended RAM Step	1 MB† 1 KB Every location	Selects the thoroughness of the extended memory. If “1 MB” is selected, BIOS tests each 1 MB boundary. If “1KB” is selected, BIOS tests each 1KB boundary. If “Every location” is selected, BIOS tests every byte. BIOS defaults to the fastest test.
L2 Cache	Disabled Enabled†	Enables the second level cache. The second level cache should be disabled only for diagnostic purposes.
Multiboot Support	Disabled† Enabled	Enables Boot Device Selection as described in Section .
Override PHP Switches	Disabled† Enabled	If enabled, the individual slot switches cannot power down the slots. If disabled, the power to each slot can be removed by the individual slot switches.

NOTES: Default values are marked with the "†" symbol.

9.4.3 Security Menu

The table below describes the Security Menu.

Table 9-28: Security Menu

Feature	Option	Description
User Password is	Set Clear†	Status only. Administrator password must be enabled before user password can be enabled. User password is enabled by entering a user password and disabled by entering a null user password.
Administrator Password is	Set Clear†	Status only. Enabled by entering an administrator password and disabled by entering a null administrator password.
Set User Password	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort.
Set Administrator Password	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort.
Password on boot	Disabled† Enabled	Requires password entry on boot. System remains in Secure Mode until password is entered. Password On Boot takes precedence over Secure Mode Boot.
Secure Mode Timer	Disabled† 1 min 2 min 5 min 10 min 20 min 1 hr 2 hr	Sets the period of key/PS2 mouse inactivity specified before Secure Mode activates. A password is required for Secure Mode to function.
Secure Mode Hot Key (Ctrl-Alt-?)	Disabled† [A, B, ..., Z]	Assigns a hot key that invokes Secure Mode.
Secure Mode Boot	Disabled† Enabled	System will boot in Secure Mode. The user must enter a password to unlock the system.
Video Blanking	Disabled† Enabled	Blank video when Secure Mode is activated. A password is required to unlock the system.
Floppy Write Protect	Disabled† Enabled	When Secure Mode is activated, the floppy drive is write protected. A password is required to re-enable floppy writes.
Front Panel Lockout	Disabled† Enabled	When Secure Mode is activated, the Reset and Power switches are locked. A password is required to unlock the system.

NOTES: Default values are marked with the "†" symbol.

9.4.4 Server Menu

The tables below describe the Server Menu and submenus.

Table 9-29: Server Menu

Feature	Option	Description
System Management		Selects System Management submenu.
Console Redirection		Selects Console Redirection submenu.
Processor Retest	No† Yes	Select “Yes” to clear historical processor status and retest all processors on the next boot.
EMP Password Switch	Disabled† Enabled	Enables the EMP password.
EMP Password		Selects the EMP password.
EMP ESC Sequence		This field is updated from the Front Panel Controller firmware.
EMP Hangup Line String		This field is updated from the Front Panel Controller firmware.
Modem Initialization String		This field is updated from the Front Panel Controller firmware.
High Modem Initialization String		This field is updated from the Front Panel Controller firmware.
EMP Access Mode	Pre-Boot Only Always Active Disabled†	Selected when the EMP is enabled. If “Always Active,” the EMP is always enabled. If “Pre-Boot Only,” the EMP is enabled during power down or POST only. If “Disabled,” the EMP is disabled.
EMP Restricted Mode Access	Disabled† Enabled	Enables Restricted Mode. In Restricted Mode, Power Down, Front Panel NMI, and Reset Control via EMP are disabled.
EMP Direct Connect/ Modem Mode	Direct Connect† Modem Mode	Allows the user to connect to a local machine without using a modem.

NOTES: Default values are marked with the "†" symbol.

Table 9-30: System Management Submenu

Feature	Option	Description
Firmware SMIs	Disabled Enabled†	Enables SMI generation by agents on the Intelligent Platform Management Bus (IPMB). Because BIOS requires SMIs for various tasks, setting this field to disabled does not disable all sources of SMIs.
System Event Logging	Disabled Enabled†	Enables logging of critical events.

Table 9-30: System Management Submenu (Continued)

Clear Event Log	Disabled† Enabled	Clears the System Event Log (SEL). This option is reset to Disabled on each boot.
Memory Scrubbing	Disabled Enabled†	Enables memory scrubbing by the Profusion* chip set.
AERR Enable	Disabled Enabled†	Enables AERR to be asserted on the processor host buses.
Assert NMI on BERR	Disabled Enabled†	Enables BERR to be reported as a critical event via NMI. Requires SERR to be enabled as well.
Assert NMI on PERR	Disabled Enabled†	Enables PERR to be reported as a critical event via NMI. Requires SERR to be enabled as well.
Assert NMI on SERR	Disabled Enabled†	Enables SERR to be reported as a critical event via NMI.
Enable Host Bus Error	Disabled Enabled†	Enables ECC checking on the processor buses
FPC Error Check	Disabled† Enabled	Enables Front Panel Controller (FPC) checking. If enabled, BIOS verifies that it can communicate with the FPC.
HSC Error Check	Disabled† Enabled	Enables Hot-swap Controller (HSC) checking. If enabled, BIOS verifies that it can communicate with the HSC.
Server Management Info		Selects Server Management Information submenu.

NOTES: Default values are marked with the "†" symbol.

Table 9-31: Server Management Information Submenu

Feature	**Description**
Board Part Number	Displays Board Part Number.
Board Serial Number	Displays Board Serial Number.
System Part Number	Displays System Part Number.
System Serial Number	Displays System Serial Number.
Chassis Part Number	Displays Chassis Part Number.
Chassis Serial Number	Displays Chassis Serial Number.
BMC Revision	Displays Baseboard Management Controller Revision.
FPC Revision	Displays Front Panel Controller Revision.
HSC Revision	Displays Hot-swap Controller Revision.

Table 9-32: Console Redirection Submenu

Feature	Option	Description
COM Port Address	Disabled† 3F8 2F8 3E8	When enabled, use the I/O port specified.
IRQ #	3† 4	When enabled, use the IRQ specified.
COM Port Baud Rate	9600† 19.2K 38.4K 115.2K	When enabled, use the baud rate specified. The maximum baud rate supported by the Emergency Management Port is 19.2K.
Flow Control	No Flow Control CTS/RTS XON/XOFF CTS/RTS + CD†	When enabled, use the flow control type specified.

NOTES: Default values are marked with the "†" symbol.

9.4.5 Boot Menu

The table below describes the Boot Menu.

Boot Menu options allow the user to select the boot device. The table below shows an example list of devices ordered in priority of the boot invocation. Items can be reprioritized by using the UP and DOWN arrow keys to select the device. Once the device is selected, use the + (plus) key to move the device higher in the boot priority list. Use the - (minus) key to move the device lower in the boot priority list.

Table 9-33: Boot Menu

Feature	Option	Description
Floppy Check	Disabled† Enabled	If Enabled, system will verify floppy type on boot. “Disabled” will result in a faster boot.
Boot Device Priority		Selects the Boot Device Priority submenu.
Hard Drive		Selects the Hard Drive submenu.
Removable Devices		Selects the Removable Devices submenu.

Table 9-33: Boot Menu (Continued)

Removable Format		Selects the Removable Format submenu.
Maximum Number of I_2O Drives	1† 4	Selects the maximum number of I_2O (Intelligent I/O) drives that will be assigned a DOS drive.
Message Timeout Multiplier	1† 2 4 8 10 50 100 1000	All I_2O message timeout values are multiplied by this number.
Pause During POST	Disabled† Enabled	Use this to start the IRTOS (I_2O Real-time Operating System) manually. When POST has stopped, it issues three beeps. Pressing any key continues POST.

NOTES: Default values are marked with the "†" symbol.

9.4.6 Exit Menu

The table below describes the Exit Menu.

Table 9-34: Exit Menu

Option	Description
Exit Saving Changes	Exit Setup and save changes.
Exit Discarding Changes	Exit Setup without saving changes.
Load Setup Defaults	Load default values for all Setup items.
Load Custom Defaults	Load settings from Custom Defaults.
Save Custom Defaults	Save changes as Custom Defaults. If CMOS fails, BIOS uses Custom Defaults if available. If not, it uses the factory defaults.
Discard Changes	Load previous values of all Setup items.
Save Changes	Save all changes.

9.5 Flash Utility

The Flash Memory Update utility (iFLASH) updates the flash ROM with new system software. The loaded code and data include the following:

- System BIOS
- Embedded video BIOS and SCSI BIOS
- BIOS Setup utility
- OEM-supplied user binary area
- Language file

iFLASH communicates with the existing BIOS to provide security mechanisms which reduce the risk of tampering. It also communicates with BIOS to verify that the new BIOS image is compatible with the existing image. This helps to prevent an incorrect BIOS from being placed into flash memory.

iFLASH operates in three modes: interactive mode, command line mode, and recovery mode. Interactive mode and command line mode are used in normal situations. In these modes, the user boots DOS and then executes the iFLASH utility. The keyboard and video monitor are available for issuing commands, locating files, and displaying progress. If iFLASH is interrupted by a power failure or by user intervention, the flash ROM may contain an incomplete BIOS. Recovery mode provides a method to install the BIOS when the flash ROM has been corrupted.

For best results, iFLASH should run under DOS with no extended memory managers loaded. The flash utility does not support DPMI environments such as Windows*, Windows 95, or Windows NT*. Because the utility is written for DOS, it does not run under any other operating system.

9.5.1 Interactive Mode

Interactive mode provides a menu that allows the user to update a particular area of the flash ROM or display the header of a flash file.

For interactive mode, the user invokes iFLASH on the DOS command line with no options. Subsequent menus allow the user to update the flash ROM or display the header of a BIOS file.

The utility assumes the following suffixes:

First System BIOS File `.BIO`

Logo/User Binary File `.USR`

Language File `.LNG`

After a file is selected, the utility prompts the user to confirm the action. It displays a BIOS Image Title, Time Stamp, BIOS Version, and BIOS ID. The user should check these fields before continuing.

System BIOS. Normally, iFLASH updates the entire flash ROM except for the recovery boot block. Custom language files and user binaries are removed. They must be flashed separately. Flashing the system BIOS does not clear CMOS configuration RAM. Furthermore, it does not clear the Vital Product Data area accessed by SMBIOS GPNV calls.

The update takes three to five minutes to complete. During this time, the user must not reset or power-down the system. Otherwise, the user must boot in recovery mode to install the BIOS. When iFLASH completes the update, it prompts the user to reboot.

The system BIOS is delivered as a series of binary files. The files are named as follows:

```
biosname.BIO
biosname.BI1
biosname.BI2
etc.
```

In this example, `biosname` is a unique name for each OCPRF100 MP server system BIOS release. The binary files should not be renamed. Each file contains a link to the next file in the sequence. iFLASH checks these links before modifying the flash ROM.

User Binary. The BIOS reserves a 16KB area in flash for custom user binary code. The user binary area is updated separately. Only one file is needed; its filename extension must be .USR.

Language Block. The BIOS supports a custom language block that allows system vendors to provide strings in other languages. (Intel provides strings in English, French, Italian, German, and Spanish.) The custom language block is updated separately from the rest of BIOS. The filename extension of the language files must be .LNG.

9.5.2 Command Line Mode

The command line mode produces the same result as interactive mode but without the interactive user interface. The user invokes iFLASH at the command line as follows:

- iFLASH /P filename- Program the device from the named file.
- iFLASH /X filename- Examine the header of the named file.
- iFLASH /H- Print Help.

Because iFLASH supports multiple Intel products, other options presented in the help screen may not be supported on this product.

After the command is invoked, iFLASH proceeds as described in Section Interactive Mode.

9.5.3 Recovery Mode

Recovery mode should be used only when your system BIOS is corrupted such that it will not boot. Recovery mode requires at least 4 MB of RAM. Drive A must be a 3.5” 1.44-MB floppy drive.

The recovery diskette should be created before it is needed and saved for later use.

9.5.3.1 Creating a Bootable Recovery Diskette

The recovery diskette should contain the same files as the normal flash diskette. Do not include a CONFIG.SYS file on this disk.

Test the disk by booting to it in normal mode. If correctly configured, it should invoke iFLASH.

9.5.3.2 Performing BIOS Recovery

The follow procedure boots the recovery BIOS and flashes the normal BIOS:

- Turn system power off.
- Move the BIOS recovery jumper to the recovery state.
- Insert the BIOS recovery diskette containing the new BIOS image files.
- Turn system power on.

At this point, the recover BIOS boots from the DOS-bootable recovery diskette. BIOS emits one beep when it passes control to DOS. DOS then executes a special AUTOEXEC.BAT that contains “iFLASH” on the first line. iFLASH reads the flash image and programs the necessary blocks. It emits one beep to indicate the beginning of the flash operation. After a period of time, BIOS emits two beeps to indicate that the flash procedure completed successfully. If the flash procedure fails, BIOS emits a continuous series of beeps.

When the flash update completes:

- Turn system power off.
- Remove the recovery diskette.
- Restore the jumper to its original position.
- Turn system power on.
- Flash any custom blocks such as user binary or language blocks.

The system should now boot normally using the updated system BIOS.

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Appendix A: BIOS Resource Maps

Appendix A shows the resource maps for the initial release of the OCPRF100 MP server system. These maps are subject to change with each release of the system BIOS.

The table below shows the system memory map. For PCI devices, BIOS allocates memory space just below the APICs. This region grows downward to accommodate the specific devices installed in the system.

The system does not support memory gaps from 512KB to 640KB and from 15 MB to 16 MB. These regions are treated as normal system memory.

Table 1: Memory Space Assignments

Start	End	Assignments
1_0000_0000h	Varies	System memory above 4 GB.
0_FFF0_0000h	0_FFFF_FFFFh	Flash ROM window.
0_FEE0_0000h	0_FEE0_FFFFh	Processor local APIC.
0_FEC0_0000h	0_FEC0_FFFFh	I/O APIC.
Varies	0_FEBF_FFFFh	PCI devices.
0_0010_0000h	Varies	System memory.
0_000C_0000h	0_000F_FFFFh	Shadow ROM space.
0_000A_0000h	0_000B_FFFFh	Video buffer/SMRAM.
0_0000_0000h	0_0009_FFFFh	System memory.

The table below shows the memory space from C0000h to FFFFFh in more detail. The embedded VGA OPROM occupies 32 KB. OPROMs for plug-in VGA controllers may vary in size.

Table 2: Shadow ROM Assignments

Start	End	Assignments
E0000h	FFFFFh	BIOS.
DC000h	DFFFFh	Option ROMs or Console Redirection.
D8000h	DBFFFh	Option ROMs or User Binary Run-time Code.

Table 2: Shadow ROM Assignments (Continued)

C8000h	D7FFFh	Option ROMs.
C0000h	C7FFFh	VGA BIOS.

The 2 MB flash component is accessed through a 1 MB window located at FFF00000h (4095 MB). A General Purpose Output port (GPO28) from the PIIX4E selects which half of the device is being accessed. Setting GPO28 to a 0 selects the OEM portion of the flash ROM; setting it to a 1 selects the Intel portion. The flash ROM layout is shown in the table below and is subject to change with each release.

Table 3: Flash Map Summary

GPO28	Start	End	Assignments
1	FFFF_0000h	FFFF_FFFFh	BIOS block.
1	FFFE_C000h	FFFE_FFFFh	Recovery boot block.
1	FFFE_0000h	FFFE_BFFFh	Reserved for Intel expansion.
1	FFFD_0000h	FFFD_FFFFh	BIOS block.
1	FFFC_4000h	FFFC_FFFFh	BIOS block.
1	FFFC_0000h	FFFC_3FFFh	Console redirection binary.
1	FFFB_2000h	FFFB_FFFFh	BIOS block.
1	FFFA_0000h	FFFB_1FFFh	Language block.
1	FFF9_C000h	FFF9_FFFFh	BIOS block.
1	FFF9_8000h	FFF9_BFFFh	User binary.
1	FFF9_0000h	FFF9_7FFFh	SMM binary.
1	FFF8_0000h	FFF8_FFFFh	ESCD, VPD, and SCSI NVRAM.
1	FFF2_0000h	FFF7_FFFFh	Reserved for Intel expansion.
1	FFF0_0000h	FFF1_FFFFh	Protected mode module.
0	FFF0_0000h	FFFF_FFFFh	Reserved for system vendors.

The table below shows the system I/O map. When BIOS allocates I/O space to PCI devices, it starts at 2000h and continues upward. Addresses below 2000h are reserved for embedded devices.

For compatibility with software that supports EISA buses, addresses xC80h-xC83h are reserved for EISA IDs. If ISA Aliasing is enabled, PCI devices are restricted to addresses where bits 8 and 9 are zero.

Table 4: I/O Space Assignments

Start	End	Assignments
2000h	FFFFh	PCI devices
0000h	1FFFh	Embedded devices

Before booting the operating system, BIOS configures the interrupts to use two AT-compatible PIC devices. These PICs support a total of 16 interrupt lines as shown in the table below. Most operating systems switch out of PIC mode and use the I/O APIC to process interrupts.

Table 5: PIC-Mode IRQ Assignments

IRQ	Assignments
0	System timer
1	Keyboard
2	Cascade
3	Serial port or PCI devices
4	Serial port or PCI devices
5	Parallel port or PCI devices
6	Floppy disk controller
7	Parallel port or PCI devices
8	Real-time clock
9	SCI and SMBus
10	PCI devices
11	PCI devices
12	Mouse
13	None

Table 5: PIC-Mode IRQ Assignments

14	Primary IDE or PCI devices
15	PCI devices

Appendix B: BIOS POST Codes

BIOS issues POST codes to I/O port 80h to indicate the start of a POST task or to indicate an error condition. If a POST task fails before video resources are initialized, BIOS may emit a “beep code.” A beep code is a series of individual beeps on the PC speaker, each of equal length.

The table below describes the POST codes and beep codes used by the OCPRF100 MP server system BIOS. Note that BIOS enables the hot-plug controller before starting POST, but that the controller takes approximately 1.5 seconds to power-on a slot. Therefore, POST codes issued in the first 1.5 seconds may not be displayed.

Table 6: Port-80h POST Codes

POST Code	Beep Code	POST Task
02		Verify real mode
03		Disable NMI
04		Get processor type
06		Initialize system hardware
08		Initialize chip set registers with initial POST values
09		Set in POST flag
0A		Initialize processor registers
0B		Enable processor cache
0C		Initialize caches to initial POST values
0E		Initialize I/O
0F		Initialize the local bus IDE
10		Initialize power management
11		Load alternate registers with initial POST values new
12		Restore processor control word during warm boot
13		Reset PCI bus masters
14		Initialize keyboard controller
16	1-2-2-3	BIOS ROM checksum
17		Prepare to size RAM
18		8254 timer initialization
1A		8237 DMA controller initialization

Table 6: Port-80h POST Codes (Continued)

1C		Reset programmable interrupt controller
20	1-3-1-1	Test DRAM refresh
22	1-3-1-3	Test 8742 keyboard controller
24		Set ES segment register to 4 GB
28	1-3-3-1	Autosize DRAM
29	1-3-3-2	Initialize or call POST memory manager
2A	1-3-3-3	Clear 512KB base RAM and verify the coherency filter configuration
2C	1-3-4-1	RAM failure on address line xxxx
2E	1-3-4-3	RAM failure on data bits xxxx of low byte of memory bus
2F		Prepare to shadow system BIOS
30	1-4-1-1	RAM failure on data bits xxxx of high byte of memory bus
32		Test processor bus-clock frequency
33		Initialize the POST dispatch manager
34	1-4-2-1	Test CMOS
35		RAM Initialize alternate chip set registers
36		Warm start shut down
37		Reinitialize the chip set (MB only)
38		Shadow system BIOS ROM
39		Reinitialize the cache (MB only)
3A	1-4-3-3	Autosize cache
3C		Configure advanced chip set registers
3D		Load alternate registers with CMOS values new
40		Set initial processor speed new
42		Initialize interrupt vectors
44		Initialize BIOS interrupts
45		Initialize run-time devices
46		Check ROM copyright notice
47		Initialize manager for PCI option ROMs
48		Check video configuration against CMOS
49		Initialize PCI bus and devices
4A		Initialize all video adapters in system
4B		Display QuietBoot screen

Table 6: Port-80h POST Codes (Continued)

4C		Shadow video BIOS ROM
4E		Display copyright notice
50		Display processor type and speed
52		Test keyboard
54		Set key click if enabled
56		Enable keyboard
58	2-2-3-1	Test for unexpected interrupts
59		Initialize POST display service
5A		Display prompt "Press F2 to enter SETUP"
5B		Disable cache
5C		Test RAM between 512KB and 640KB
60		Test extended memory
62		Test extended memory address lines
64		Jump to UserPatch1
66		Configure advanced cache registers
67		Initialize processors
68		Enable external and processor caches
69		Setup power management
6A		Display external cache size
6B		Load custom defaults
6C		Display shadow message
6E		Display nondisposable segments
70		Display error messages
72		Check for configuration errors
74		Test real-time clock
76		Check for keyboard errors
7A		Test for key lock on
7C		Set up hardware interrupt vectors
7E		Test coprocessor if present
80		Detect and install external RS232 ports
81		Initialize run-time devices
82		Detect and install external parallel ports

Table 6: Port-80h POST Codes (Continued)

83		Configure IDE controller
84		Initialize parallel port
85		Initialize PC-compatible PnP ISA devices
86		Re-initialize embedded I/O ports
87		Initialize embedded configurable devices
88		Initialize BIOS data area
89		Enable NMI
8A		Initialize extended BIOS data area
8B		Initialize mouse
8C		Initialize floppy controller
8F		Preinitialize local-bus hard-disk controller
90	3-2-1-1	Initialize hard-disk controller or failure during Multiboot Allocation
91		Initialize local-bus hard-disk controller
92		Jump to UserPatch2
93		Build MPTABLE
94		Disable A20 address line
95		Install CD-ROM for boot
96		Clear huge ES segment register
97		Fixup MPTABLE
98	1-2	Search for option ROMs. One long, two short beeps on checksum failure.
9A		Shadow option ROMs
9C		Set up power management
9D		Initialize security
9E		Enable hardware interrupts
9F		Initialize local-bus hard-disk controller
A0		Set time of day
A2		Check key lock
A4		Initialize typematic rate
A8		Erase F2 prompt
AA		Scan for F2 key stroke
AC		Enter SETUP
AE		Clear in-POST flag

Table 6: Port-80h POST Codes (Continued)

B0		Check for errors
B2		POST done – prepare to boot operating system
B4	1	One short beep before boot
B5		Display multiboot menu
B6		Check password (optional)
B7		Initialize ACPI
B8		Clear global descriptor table
B9		Prepare to boot
BA		Initialize DMI
BC		Clear parity checkers
BD		Invoke boot menu
BE		Clear screen (optional)
BF		Check virus and backup reminders
C0	4-1-1-1	Try to boot with INT 19 (beep code if disabling A20 fails)
C1		Initialize the POST error manager
C2		Log POST errors
C3		Display POST errors
CC	4-1-4-1	Memory sizing error
CF	4-1-4-4	Coherency filter sizing error
D0		Interrupt handler error
D2		Unknown interrupt error
D4		Pending interrupt error
D6		Initialize option ROM error
D8		Shutdown error
DA		Extended block move
DC		Shutdown 10 error
DE		Keyboard controller error
DF	4-2-4-4	A20 error
FB		FRB in progress

Table 6: Port-80h POST Codes (Continued)

FC		Five second wait for BMC to initialize
FD		FRB-2 watchdog timer failed; reset will occur in five seconds.

Table 7: Recovery Mode Port-80h POST Codes

POST Code	Beep Code	POST Task
E0		Initialize chip set
E1		Initialize bridge
E2		Initialize processor
E3		Initialize timer
E4		Initialize system I/O
E5		Check forced recovery boot
E6		Validate checksum
E7		Go to BIOS
E8		Initialize processors
E9		Set 4 GB segment limits
EA		Perform platform initialization
EB		Initialize PIC and DMA
EC		Initialize memory type
ED		Initialize memory size
EE		Shadow boot block
EF		Test system memory
F0		Initialize interrupt services
F1		Initialize real-time clock
F2		Initialize video
F3		Initialize beeper
F4		Initialize boot
F5		Restore segment limits to 64KB

Table 7: Recovery Mode Port-80h POST Codes (Continued)

F6		Boot mini DOS
F7		Boot full DOS

Table 8: Port-80h Flashing/Debug Codes

Code 1	**Code 2**	**Error**
0F	0B	Firmware failed on FRB initiation
2D	00	Firmware failed to report processor status
02	00	Firmware failed to process error logging
2A	00	Firmware failed to reset processor sensor status
22	00	Firmware failed to kick-start watchdog timer
24	00	Firmware failed to initialize watchdog timer
25	00	Firmware failed to report watchdog timer status
32	00	Firmware failed to process enable/disable processor

Appendix C: BIOS Error Codes

The traditional single-byte error codes do not provide sufficient granularity for larger servers. Four-digit error codes provide greater insight into the actual failure. The table below shows the error codes listed on the VGA, on the LCD, and in the system event log.

Table 9: POST Error Codes

Code	Error Message
0200	Failure fixed disk
0210	Stuck key
0211	Keyboard error
0213	Keyboard locked - Unlock key switch
0230	System RAM failed at offset:
0231	Shadow Ram failed at offset:
0232	Extended RAM failed at offset:
0250	System battery is dead - Replace and run SETUP
0251	System CMOS checksum bad - Default configuration used
0260	System timer error
0270	Real-time clock error
0271	Check date and time settings
0280	Previous boot incomplete - Default configuration used
0281	Memory size found by POST differed from EISA CMOS
0297	Base memory error
0297	Extended memory error
02B0	Diskette drive A error
02B1	Diskette drive B error
02B2	Incorrect Drive A type - Run SETUP
02B3	Incorrect Drive B type - Run SETUP
02D0	System cache error - Cache disabled
02F0	CPU ID
02F4	EISA CMOS not writeable
02F5	DMA test failed

Table 9: POST Error Codes (Continued)

02F6	Software NMI failed
02F7	Fail-safe timer NMI failed
8108	Watchdog timer failed on last boot
8110	Server management Interface failed to function
814B	BMC in update mode
8150	NVRAM cleared by jumper
8152	ESCD data cleared
8153	Password cleared by jumper
8154	Sensor Data Record empty
8155	System Event Logging is full
8160	Unable to apply BIOS update for Right Processor 4
8161	Unable to apply BIOS Update for Right Processor 3
8162	Unable to apply BIOS Update for Right Processor 2
8163	Unable to apply BIOS Update for Right Processor 1
8164	Unable to apply BIOS Update for Left Processor 4
8165	Unable to apply BIOS Update for Left Processor 3
8166	Unable to apply BIOS Update for Left Processor 2
8167	Unable to apply BIOS Update for Left Processor 1
8168	Right Processor 4 L2 cache failed
8169	Right Processor 3 L2 cache failed
816A	Right Processor 2 L2 cache failed
816B	Right Processor 1 L2 cache failed
816C	Left Processor 4 L2 cache failed
816D	Left Processor 3 L2 cache failed
816E	Left Processor 2 L2 cache failed
816F	Left Processor 1 L2 cache failed
8170	BIOS does not support current stepping for Right Processor 4
8171	BIOS does not support current stepping for Right Processor 3
8172	BIOS does not support current stepping for Right Processor 2
8173	BIOS does not support current stepping for Right Processor 1
8174	BIOS does not support current stepping for Left Processor 4
8175	BIOS does not support current stepping for Left Processor 3

Table 9: POST Error Codes (Continued)

8176	BIOS does not support current stepping for Left Processor 2
8177	BIOS does not support current stepping for Left Processor 1
8180	PB64 failed to respond
8181	CPUID, processor steppings are different
8182	L2 cache size mismatch
8186	Processor families are different
8200	Baseboard management controller failed to function
8201	Front panel controller failed to function
8202	Power share controller failed to function
8205	Hot-swap controller failed to function
8210	Right Processor 4 failed BIST
8211	Right Processor 3 failed BIST
8212	Right Processor 2 failed BIST
8213	Right Processor 1 failed BIST
8214	Left Processor 4 failed BIST
8215	Left Processor 3 failed BIST
8216	Left Processor 2 failed BIST
8217	Left Processor 1 failed BIST
8220	Right Processor 4 internal error (IERR) failure
8221	Right Processor 3 internal error (IERR) failure
8222	Right Processor 2 internal error (IERR) failure
8223	Right Processor 1 internal error (IERR) failure
8224	Left Processor 4 internal error (IERR) failure
8225	Left Processor 3 internal error (IERR) failure
8226	Left Processor 2 internal error (IERR) failure
8227	Left Processor 1 internal error (IERR) failure
8230	Right Processor 4 thermal trip failure
8231	Right Processor 3 thermal trip failure
8232	Right Processor 2 thermal trip failure
8233	Right Processor 1 thermal trip failure
8234	Left Processor 4 thermal trip failure
8235	Left Processor 3 thermal trip failure

Table 9: POST Error Codes (Continued)

8236	Left Processor 2 thermal trip failure
8237	Left Processor 1 thermal trip failure
8240	Right Processor 4 disabled
8241	Right Processor 3 disabled
8242	Right Processor 2 disabled
8243	Right Processor 1 disabled
8244	Left Processor 4 disabled
8245	Left Processor 3 disabled
8246	Left Processor 2 disabled
8247	Left Processor 1 disabled
8250	Right Processor 4 failed FRB Level 3 timer
8251	Right Processor 3 failed FRB Level 3 timer
8252	Right Processor 2 failed FRB Level 3 timer
8253	Right Processor 1 failed FRB Level 3 timer
8254	Left Processor 4 failed FRB Level 3 timer
8255	Left Processor 3 failed FRB Level 3 timer
8256	Left Processor 2 failed FRB Level 3 timer
8257	Left Processor 1 failed FRB Level 3 timer
8260	Right Processor 4 failed initialization
8261	Right Processor 3 failed initialization
8262	Right Processor 2 failed initialization
8263	Right Processor 1 failed initialization
8264	Left Processor 4 failed initialization
8265	Left Processor 3 failed initialization
8266	Left Processor 2 failed initialization
8267	Left Processor 1 failed initialization
8270	Left memory carrier failed
8271	Right memory carrier failed
8272	DIMM not fully configured – Left Jx
8273	DIMM not fully configured – Right Jx
8274	Memory error detected in DIMM Left Jx
8275	Memory error detected in DIMM Right Jx

Table 9: POST Error Codes (Continued)

8276	DIMM size mismatch
8280	Coherency filter failed left data test
8281	Coherency filter failed right data test
8290	Coherency filter failed left address test
8291	Coherency filter failed right address test
8293	Coherency filter size mismatch
8294	Coherency filter data miscompare
8295	Unsupported DIMM SPD found
8296	I^2C Bus error
8297	Unexpected interrupt occurred
8298	Left Processor did not boot
8299	Right Processor did not boot
8300	Bad ECC DIMM found at left memory port
8301	Bad ECC DIMM found at right memory port
8302	Internal error occurred
8303	Bad or missing Coherency Filters, bus and processor(s) disabled
8304	Bad or missing Coherency Filters, bus disabled
8305	Too many errors, memory test aborted
8400	Switch fault on PCI hot-plug slot Px
8401	Hot-plug switches overridden by jumper or setup
8402	Hot-plug power-up sequence did not complete

Appendix D: Int15h BIOS Extensions

Intel has extended the software interrupt 15h interface to provide additional real-mode services as shown in the table below.

Table 10: Interrupt 15h Extensions

Function (AX)	Description
DA00h	Speaker services
DA08h	Front panel LCD services
DA12h	Cache services
DA15h	Intel ID string
DA20h	Update CMOS CRC/Checksum (BL = 83h)
DA20h	IPMB services (BL = 99h, 9Ah, 9Bh)
DA8Ch	Version information
DA92h	Processor information

Speaker Services. These functions enable or disable the speaker.

Table 11: Speaker Services

```
Call With    AH = DAh
               AL = 00h
               CL = 00h Disable Speaker
               = 01h Enable Speaker
               = 02h Read Speaker Status

Returns          AH = 00h Speaker Disabled
                 = 01h Speaker Enabled
             CF = 0 Success, or
               = 1 Invalid parameters, or
               = 1 Function Not Supported
             (If AH=86h)
```

Front Panel LCD Services. The LCD displays two lines of 16 characters. Permissible X coordinates are 0 to 15. Permissible Y coordinates are 0 to 1.

Table 12: Front Panel LCD Services

Call With AH = DAh
AL = 08h
BH = Subfunction # (See Table D-2)

Returns CF = 0 Success
= 1 Subfunction could not be performed.

Table 13: Front Panel LCD Subfunctions (AX=DA08h)

BH	Subfunction	Description
00h	Clear and home cursor	Disables the front panel LCD, or alternately enables and clears the LCD. Input: none. Output: none.
07h	Turn-on LCD	Enables the front panel LCD. Input: none. Output: none.
08h	Turn-off LCD	Disables the front panel LCD. Input: none. Output: none.
09h	Get LCD display info	Retrieves the information about the front panel LCD. Input: ES:DI points to user buffer of 5 bytes. Output: ES:DI Offset 0 = number of rows Offset 1 = number of columns Offset 2 = character cell width Offset 3 = character cell height Offset 4 = number of available character generator
0Ah	LCD read ASCII	Read displayed characters from the LCD. Input: ES:DI Offset 0 = number of characters to read Offset 1 = row number Offset 2 = column number Output: ES:DI Offset 0 = number of characters read Offset 1…n = characters

Table 13: Front Panel LCD Subfunctions (AX=DA08h) (Continued)

0Bh	LCD Write ASCII	Write characters to the LCD. Input: ES:DI Offset 0 = number of characters to write Offset 1 = row number Offset 2 = column number Offset 3…n = characters to write

Cache Services. Sets the state of the processor caches.

Table 14: Cache Services

```
Call With    AH = DAh
              AL = 12h
              CL = 0 Disable cache
              = 1 Enable cache
              = 2 Read cache status
              = 3 Set Writeback Mode
              = 4 Set Write-through Mode

Returns        AH, bit 0
              = 0  Cache Disabled
              = 1  Cache Enabled
              AH, bit 1
              = 0  Write-through Mode
              = 1  Writeback Mode
              CX, bit 15
              = 0  Size information is invalid
              = 1 Size information is valid
              CX, bits 14:0 Size of L2 cache in 32KB blocks
              CF = 0  Success
              = 1 Function not support (if AH = 86h)
```

Cache services are intended for diagnostic purposes only. The OCPRF100 MP server system does not support switching from writeback to write-through modes.

Intel ID String. Gets the Intel ID string for the BIOS. The string may look something like

```
SABR0.86B.0001.P01.121498
```

Table 15: Intel ID String

Call With	AH = Dah AL = 15h ES:DI = Points to 32-byte buffer to store results
Returns	CF = 0 Success = 1 Function not support (if AH = 86h) The 32-byte ID is formatted as follows: 5 byte board ID, “SABER” 1 byte board revision, starting from ‘0’ 3 byte OEM ID, ‘86B’ for standard BIOS 4 byte build number 1-3 byte describing build type (D for development, A for Alpha, B for Beta, Pxx for production version xx) 6 byte build date in mmddyy format 8 bytes reserved for future use

Update CMOS CRC/Checksum. Software can compute and store a new CRC/Checksum based on the current contents of CMOS.

Table 16: Update CMOS/CRC Checksum

Call With	AH = DAh AL = 20h BL = 83h Update CMOS CRC/Checksum
Returns	CF = 0 Success = 1 Function not support (if AH = 86h)

IPMB Services. The system BIOS provides real-mode calls to Read, Write, and Master Read/Write the IPMB. The Read and Write functions are used for all master/slave I^2C* devices on all buses. The Master Read/Write function performs the access using IPMB command 52h. It is typically used to “dump” I^2C devices.

IPMB Services have the following characteristics:

- They are 16-bit real-mode (EMM386 cannot be running).
- They can be used for all IPMB commands.
- They can be used to communicate with any I^2C controller.
- If the carry flag is set, the interface has broken or timed-out.
- The caller is responsible for providing proper inputs. No sanity check is provided.
- The caller is responsible for checking completion code.

Table 17: IPMB Services

Call With	AH = DAh AL = 20h BH = IPMB Command BL = 99h Read Device = 9Ah Write Device = 9Bh Master Read/Write Device CH, bits 2:0 = Bus indication CL = Number of input bytes (excluding command byte) DH = I^2C Controller ID DL = NetFn / LUN ES:DI = Points to data buffer Offset 0 is the first data byte to be sent. Offset n is the last data byte. Offset n+1 must be 0. This is the termination byte. It is not counted as a data byte.
Returns	CF = 0 Success = 1 Function not support (if AH = 86h) If successful, ES:DI = Points to the response data buffer Offset 0 contains the number of bytes returned. Offset 1 is the NetFn/LUN. Offset 2 is the command for which this is the response. Offset 3 is the completion code. Offset 4…n is the returned data.

The IPMB functions return the following generic completion codes:

```
00h = Command completed normally
C0h = Node busy or resources are temporarily unavailable
C1h = Invalid command
C2h = Command invalid for given LUN
C3h = Time-out while processing command or response unavailable
C4h = Out of space
C5h = Reservation canceled or invalid reservation ID
C6h = Request data truncated
C7h = Request data length invalid
C8h = Request data field length limit exceeded
C9h = Parameter out of range
CAh = Returned data (read) truncated
CBh = Request sensor, data or record not found
CCh = Invalid data field in request
CDh = Illegal command for specified sensor or record type
CEh = Command response could not be provided
FFh = Unspecified error
```

Version Information. Returns the BIOS version.

Table 18: Version Information

Call With	AH = Dah AL = 8Ch CL = 00h Get BIOS Version ES:DI = Points to a 12-byte data buffer
Returns	CF = 0 Success = 1 Function not support (if AH = 86h)

Processor Information. Returns information about the system processors.

Table 19: Processor Information

Call With	AH = Dah AL = 92h CL = Processor number (0…7)

Table 19: Processor Information (Continued)

Returns

```
AL  = Stepping ID
 AH  = Model
 BL  = Family
 BH  = Number of processors supported
   by platform
 CX  = Processor bus speed in BCD (MHz)
 DX  = Processor core speed in BCD (MHz)

 CF = 0 Success, or
   = 1 Processor not present, or
   = 1 Function not supported
 (If AH=86h)
 If processor not present, (CF)=1
 If function not supported, (AH)=86h, (CF)=1
```

Note: The processor number that is passed in (CL) as input refers to the physical position of the processor.

Appendix E: Processor Support

The Enterprise Server Group (ESG) supports the Performance Microprocessor Division's (PMD) position on mixed steppings in MP systems, however please note that you cannot mix processors with cache steppings requiring different voltages in the same system. The OPRF100 Board Set architecture implements one VRM to supply the same voltage to the cache core of two processors.

The table below indicates which steppings of the Pentium® III Xeon™ processor can be mixed within the same system. An "X" denotes which steppings can be mixed, and a blank indicates the OPRF100 MP Server Board Set does not support the given BIOS/stepping combination. NS indicates that processors with that S-Spec number are not supported in the OPRF100 Board Set.

Table 20: Supported Pentium® III Xeon™ Processor/BIOS Combinations

Processor Stepping	B0	B0	B0	B0	B0	B0	C0	C0	C0	C0	C0	C0	C0	C0	C0
Frequency	500MHz	500MHz	500MHz	500MHz	500MHz	500MHz	500MHz	500MHz	500MHz	500MHz	500MHz	500MHz	550MHz	550MHz	550MHz
Cache Size	512K	512K	1M	1M	2M	2M	512K	1M	2M	512K	1M	2M	512K	1M	2M
Stepping ID	0672H	0672H	0672H	0672H	0672H	0672H	0673H	0673H	0673H	0673H	0673H	0673H	0673H	0673H	0673H
S-SPEC	SL2XU	SL3C9	SL2XV	SL3CA	SL2XW	SL3CB	SL3D9	SL3DA	SL3DB	SL385	SL386	SL387	SL3AJ	SL3CE	SL3CF
SL2XU	x	x					x								
SL3C9	x	x					x								
SL2XV			x	x				x							
SL3CA			x	x				x							
SL2XW					x	x			x						
SL3CB					x	x			x						
SL3D9	x	x					x			x					
SL3DA			x	x				x			x				
SL3DB					x	x			x			x			
SL385							x			x					
SL386								x			x				
SL387									x			x			x
SL3AJ													x		
SL3CE														x	
SL3CF												x			x
BIOS															
Production Release 6	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Production Release 7	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

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