SC450NX MP Server System Specification Update

Release Date: May,1999

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The SC450NX MP Server may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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REVISION HISTORY

Date of Revision	Description
July , 1998	Preliminary Specification Update for the SC450NX MP Server System.
September , 1998	Updated with recent information.
October , 1998	Release version of Specification Update.
December , 1998	Updated with recent information.
January , 1999	Updated with recent information, cleaned up document.
February , 1999	No new information in this revision.
March , 1999	Errata 1-19 have been moved to the SC450NX TPS Appendix 20 Errata 20 Added Document Change #1 was included in the SC450NX TPS.
April , 1999	Updated errata 20 Added Pentium® III Xeon™ Processor Supported table
May , 1999	No updates.

PREFACE

This document is an update to the specifications contained in the *SC450NX MP Server System Technical Product Specification* (*243785-002*). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Specification Clarifications, Errata, and Document Changes.

Refer to the *Pentiumâ II Xeon Processor Specification Update* (243337-018) for specification updates concerning the Pentium II Xeon processor. Items contained in the Pentium II Xeon Processor Specification Update that either do not apply to the SC450NX MP Server system or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Refer to the *Intel 450NX PCIset Specification Update* (Order Number 243771-005) for specification updates concerning the Intel 82450NX PCIset. Items contained in these Specification Updates that either do not apply to the SC450NX MP Server system or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications for the SC450NX MP Server System. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Erratum are design defects or errors. Errata may cause the SC450NX's behavior to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.

Specification Update for the SC450NX MP Server System

GENERAL INFORMATION

Identification Information

Below are the specific boards, BIOS and components covered by this Specification Update. See the Board & Silicon Identification sections to determine the exact board(s), processor(s) and chipset(s) you have.

Baseboard Fab #	Baseboard PBA #	BIOS	SSU	Pentium® II Xeon™ Processor Stepping Supported	Pentium® III Xeon™ Processor Stepping Supported	82450NX MIOC/PX B Stepping
Fab 4	688264-403	Release 1	Release 2	B0/B1		B1 / B1
Fab 4	688264-406	Release 2	Release 2	B0/B1		B1 / B1
Fab 4	688264-415	Release 3	Release 3	B0/B1	BIOS Upgrade Necessary	B1 / B1
Fab 4	688264-420	Release 8	Release 3	B0/B1	B0	B1 / B1

Summary Table of Changes

The following tables indicate the Errata and the Document Changes that apply to the SC450NX MP Server System. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Table

Doc:	Intel intends to update the appropriate documentation in a future revision.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	Plans	ERRATA
20	Fix	Intel® Server Control reports L2 Cache Voltage threshold crossing events on SC450NX.

ERRATA

20. Intel® Server Control reports L2 Cache Voltage threshold crossing events on SC450NX.

PROBLEM: Unwarranted L2 Cache Upper Critical threshold crossing events may be reported on server systems after upgrading the Pentium® II Xeon™ processor from 400MHz to 450MHz. These events are seen only on systems running Intel Server Control (ISC) management software. No events will occur or be logged into the System Event Log (SEL) on server systems not running ISC.

The L2 cache voltage requirements have changed between the Pentium® II Xeon™ 400MHz processor and the Pentium® II Xeon™ 450MHz processor. The 400MHz processor L2 cache has a nominal voltage of 2.5v while the 450MHz processor has a nominal voltage of 2.7v. The L2 Cache Upper Critical threshold value monitored by ISC does not change to accommodate the difference in nominal voltages. The default Upper Critical L2 cache threshold for 400MHz processors is ~2.75v. On a system that has been upgraded to a 450MHz processor, ISC correctly show the nominal voltage at ~2.7v but the L2 Cache Upper Critical threshold remains unchanged at ~2.75v. Small fluctuations in voltage may generate threshold-crossing events that do not correctly indicate a system malfunction. Future processors with other voltage requirements may experience similar problems.

IMPLICATION: When installing new higher speed processors into the S450NX baseboard customers may get over-voltage warnings.

WORKAROUND: The SDRs for SC450NX are being modified to prevent the Intel Server Control management software from overwriting the correct BMC threshold values. This SDR modification will allow any future changes to L2 cache voltage requirements to be read and updated by the BMC and events reported correctly by ISC. The modification to the SDR will also apply to the Processor Voltage thresholds monitored by ISC.

Customer must download the latest version of the S450NX SDR's from Intel's website (https://support.intel.com) and flash into their system using the FRU/SDR load utility (also available on the website). Customers should check the website for "SDR_Readme.txt" to help match the correct SDR file for each processor.

Until the updated SDR files are available it is possible for the user to modify the L2 Cache thresholds by using Intel Server Control. The L2 Cache thresholds do not need to be changed on systems with 400MHz processors installed. On systems with 450MHz processors installed the user may change the Upper Critical threshold to ~2.9v and the Lower Critical threshold to ~2.5v. On systems with 500Mhz processors installed, the nominal L2 cache voltage is ~2.0v. The user may change the Upper Critical threshold to ~2.2v and the Lower Critical threshold to ~1.8v. The user must wait for a minimum of 10 minutes after making these changes before powering off or rebooting the system. This allows the new thresholds to be permanently saved by ISC and used after a power cycle or system reboot. There is no requirement, at this time, to modify the processor voltage threshold.

STATUS: Fixed in SDR Load Utility version 3.4.3 with SDR 9N