SR870BH2 Mainboard

Technical Product Specification

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Enterprise Platforms and Services Marketing

Revision History

Date	Revision Number	Modifications
10/08/2003	1.0	Initial release.

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1. Introduction to SR870BH2 Mainboard

1.1 Purpose of this Document

The purpose of this document is to describe the architecture, features, and hardware parameters of the SR870BH2 Mainboard.

1.2 Introduction

SR870BH2 Mainboard is the heart of a Itanium 2 processor system designed for a 2U chassis supporting one to two processors. The North Bridge system controller is an Intel® 870 SNC-M chip that interfaces with the Itanium 2 processor system bus, Double Data Rate (DDR) memory via Rambus interface, and I/O subsystem via the scalability port. The Low Pin Count (LPC) interface allows for localized Firmware Hub (FWH) support. Hub Link interface from PCI Riser board drives the P64H2 which has a dual channel SCSI controller and Dual channel GbENET controller both at PCI-X 133MHz. A second Hub Link interface from the PCI Riser board drives the ICH4 that interfaces with Video, IDE, USB, and LPC bus. The ICH4 LPC bus connects the south bridge FWH's, BMC, and SIO. Two fine-pitch BGA programmable logic devices control various logic such as power sequencing, reset, error handling, NMI/SDINT, PMI, and PME.

The SR870BH2 Mainboard design is partitioned according to the following functional blocks:

1. 1 or 2 Itanium 2, or future Socket K Processors
2. 870 Scalable Node Controller – Itanium 2 (SNC-M) chip for the Itanium 2 system bus, memory, and scalability port interface
3. 870 Memory Repeater Hub – DDR (MRH-D) Rambus memory interface and 8 X 2GB DDR Dual-in-Line Memory Module 1.7" capable (DIMM) sockets
4. VHDM interface to PCI Riser board
5. 870 P64H2 PCI-X bridge controller
6. Dual Channel LSI53C1030 Ultra320 controller
7. Dual Channel 82546EB GbENET controller
8. 870 I/O Control Hub 4 (ICH4) for interface with video, Universal Serial Bus (USB), IDE, Serial Port, and the Server Management Controller
9. Clock distribution
10. Voltage regulators and Processor power pod
11. PLD logic control
12. Processor/system reset
13. Server management
14. Flex Cable interface to Front Panel board
15. ITP Debug port

The figure below shows a photograph of the Mainboard without as it come from the board factory.

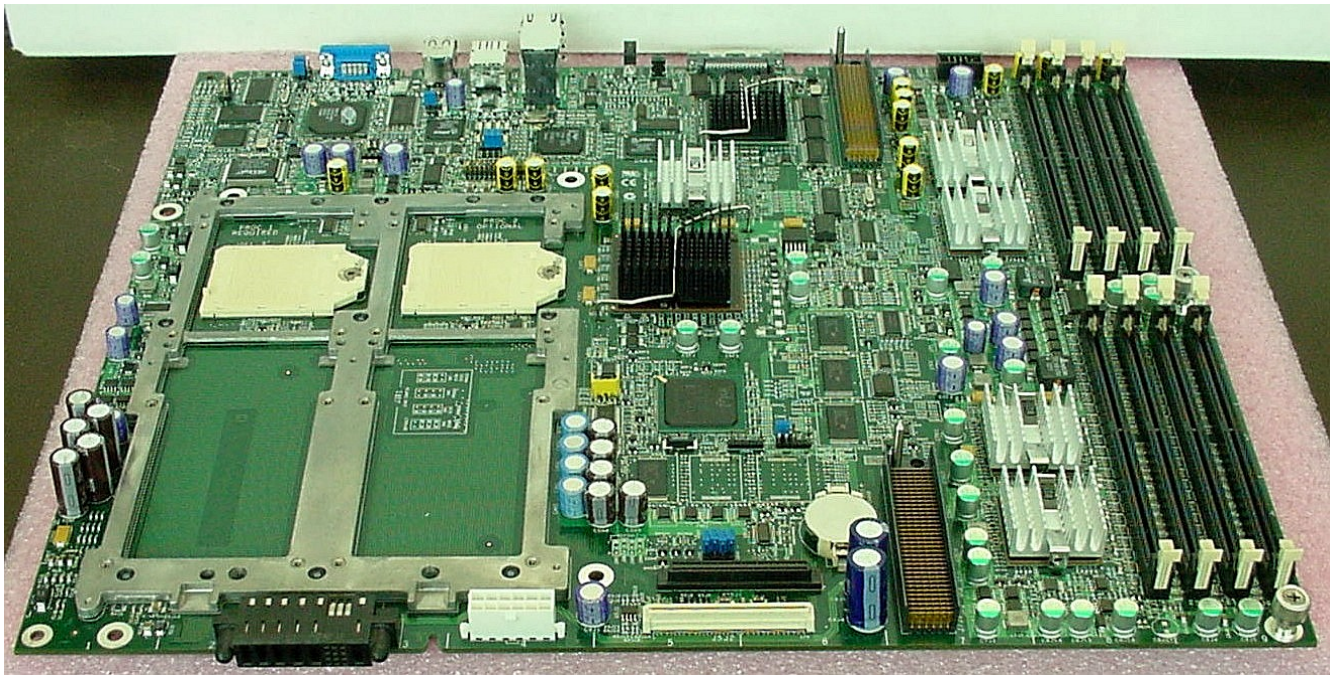


Figure 1. SR870BH2 Mainboard Top View

1.2.1 Block Diagram

The figure below illustrates the general architecture of the SR870BH2 Mainboard. The SIOH and P64H2-2 with its three PCI-X connectors are located on the PCI Riser Board.

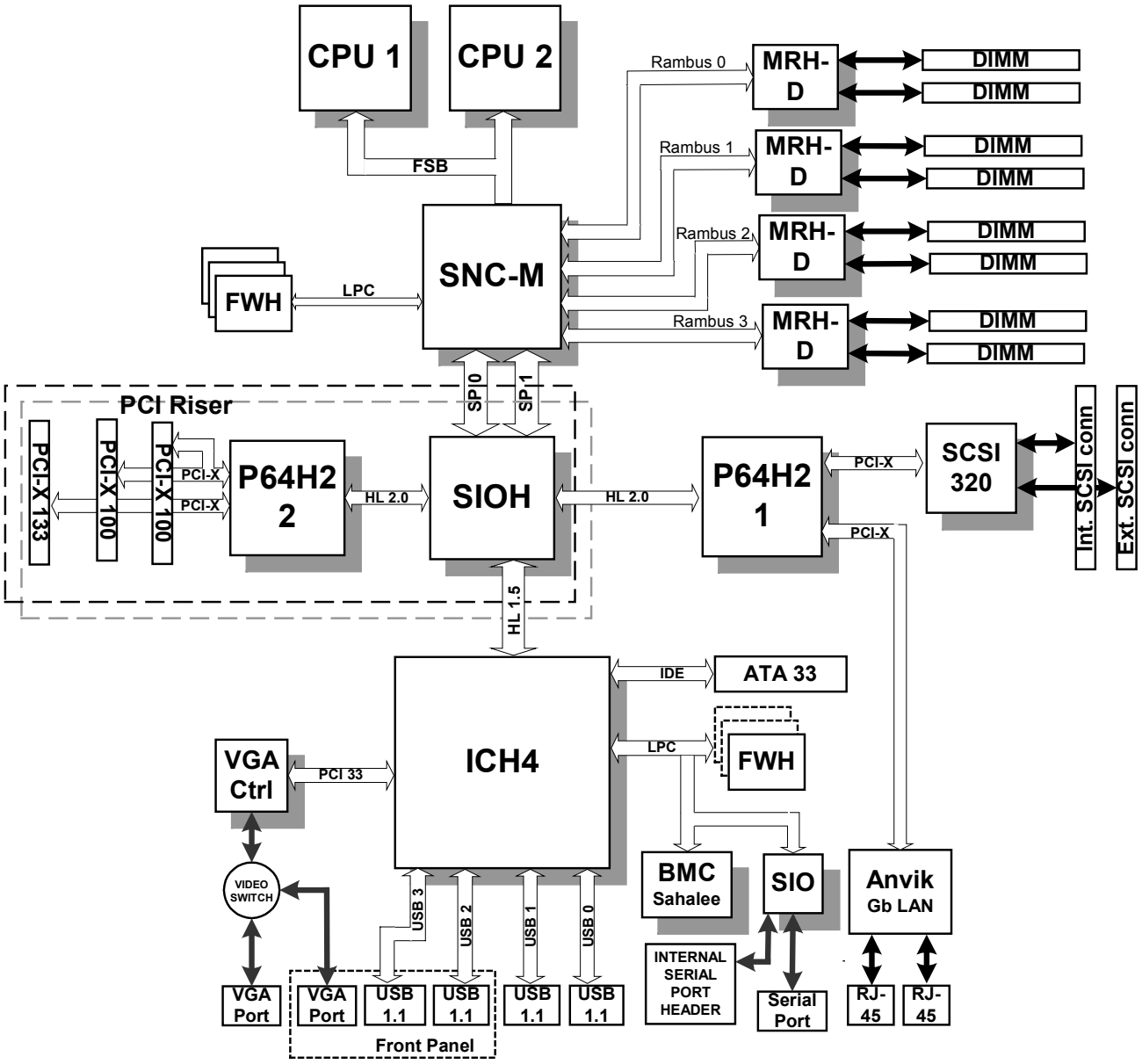


Figure 2. Mainboard Block Diagram

1.2.2 Placement Diagram

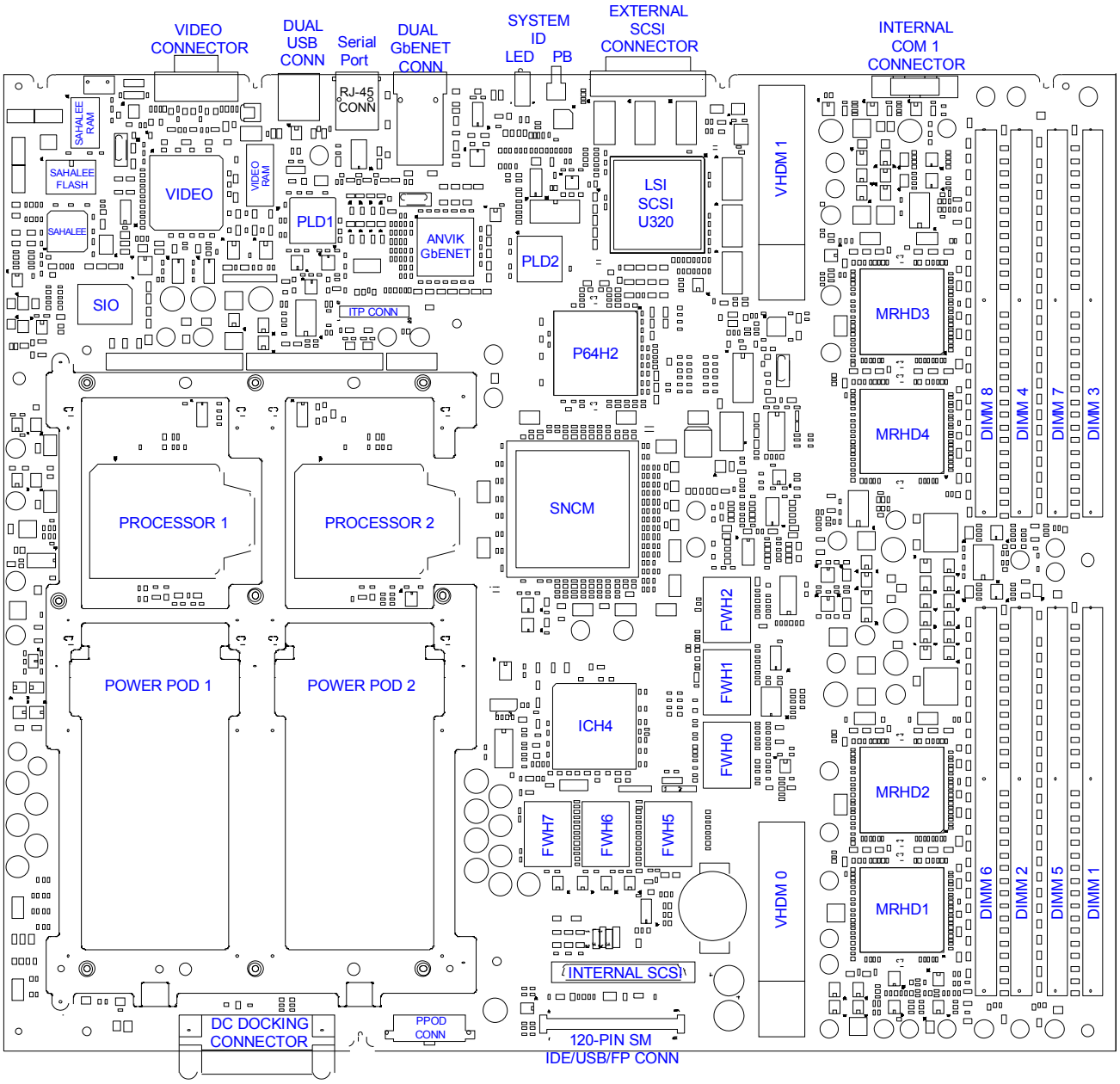


Figure 3. Mainboard Component Location (Primary Side)

2. SR870BH2 Mainboard

This chapter describes the architecture of the SR870BH2 Mainboard.

2.1 Features

The SR870BH2 Mainboard has the following features:

1. Two Itanium 2, or future Socket K Processors
2. SNC-M Scalable Node Controller bridging processor front side bus (FSB) to system memory, system I/O buses, and three of the six FWH's
3. Four MRH-D's for DDR memory interface
4. Eight 2GB DDR DIMM sockets
5. VHDM interface to PCI Riser board
6. Clock generation for all on-board and PCI Riser Board functions
7. 12-V DC-to-DC (D2D) converter power pod for each Processor
8. Embedded Regulators
   - 12 V to 1.8 V @ 17 A D2D
   - 12 V to 2.5 V @ 52 A D2D
   - 5 V to 1.2 V @ 12 A D2D
   - 5 V to 1.5 V @ 23 A D2D
   - 5 V Standby or 5 V to 3.3 V Standby D2D
   - 3.3 V Standby to 2.5 V Standby Regulator
   - 2.5 V Standby to 1.5 V Standby Regulator
   - 2.5 V to 1.25 V @ 12 A D2D
   - 1.8 V to 1.3 V @ 0.8 A Regulator
8. Six Firmware Hubs (FWH) for BIOS and system configuration utility (SCU) software
9. P64H2 PCI-X bridge for embedded SCSI and LAN controllers on 133MHz PCI-X buses
10. SCSI-320 Dual Channel Controller for Internal and External Ultra SCSI 320 channels.
11. 82546EB Gigabit Ethernet LAN Controller for two channels with RJ-45 connectors
12. ICH4 I/O Control Hub for interface with video, Universal Serial Bus (USB), IDE, Serial Port, three of the FWH's, and the Server Management Controller
13. RAGE128VR2X Video Controller on PCI 33MHz bus
14. Four USB ports with two USB connectors on board
15. LPC47B27X Super I/O (SIO) with control for two serial ports, one with on-board RJ-45 connector
16. Baseboard Management Controller (BMC) for server management functions
17. Six I^2C* system management buses
18. Debug port for use with an In-Target Probe (ITP)

2.2 Functional Architecture

This section provides a more detailed architectural description of the Mainboard functional blocks.

2.2.1 Itanium 2 Front Side Bus (FSB)

Both Itanium 2 processor sockets are connected to the 870/SNC-M through the system (Front Side) bus. The system bus consists of a 44-bit address bus and a 128-bit data bus. The address and control signals have parity protection. The data bus has Error Correcting Code (ECC) protection on each 64-bit half of the 128-bit data bus. The bus signals use Assisted Gunning Transceiver Logic (AGTL+) technology and are functionally compatible with the Intel® Itanium™ processor bus. The system bus strobes data on both the rising and falling edges of the 200 MHz clock to achieve an effective source synchronous transfer rate of 400 MT/s. The system bus signals are daisy chained with on-die termination (ODT) at both ends of the bus (the SNC-M and Processor 1). Processor 1 must be populated for the system to power up and operate normally as this Processor is hardwired on the Mainboard for ODT.

The features of the system bus are:

1. Full support for 2-way multiprocessing
2. 200 MHz with 2x strobes for equivalent 400 MHz operation
3. 6.4 GB/s peak bandwidth
4. 128-bit data bus
5. 128-byte cache line size
6. Utilization of 44 bits of the 50-bit processor address bus
7. Parity protection on address and control signals; ECC protection on the data signals
8. AGTL+ bus driver technology
9. Enhanced defer feature for out-of-order data delivery
10. System bus interrupt delivery (SAPIC architecture)
11. Supports Itanium 2 special cycles
12. Supports Future Socket K compatible Itanium Processors Family Processors

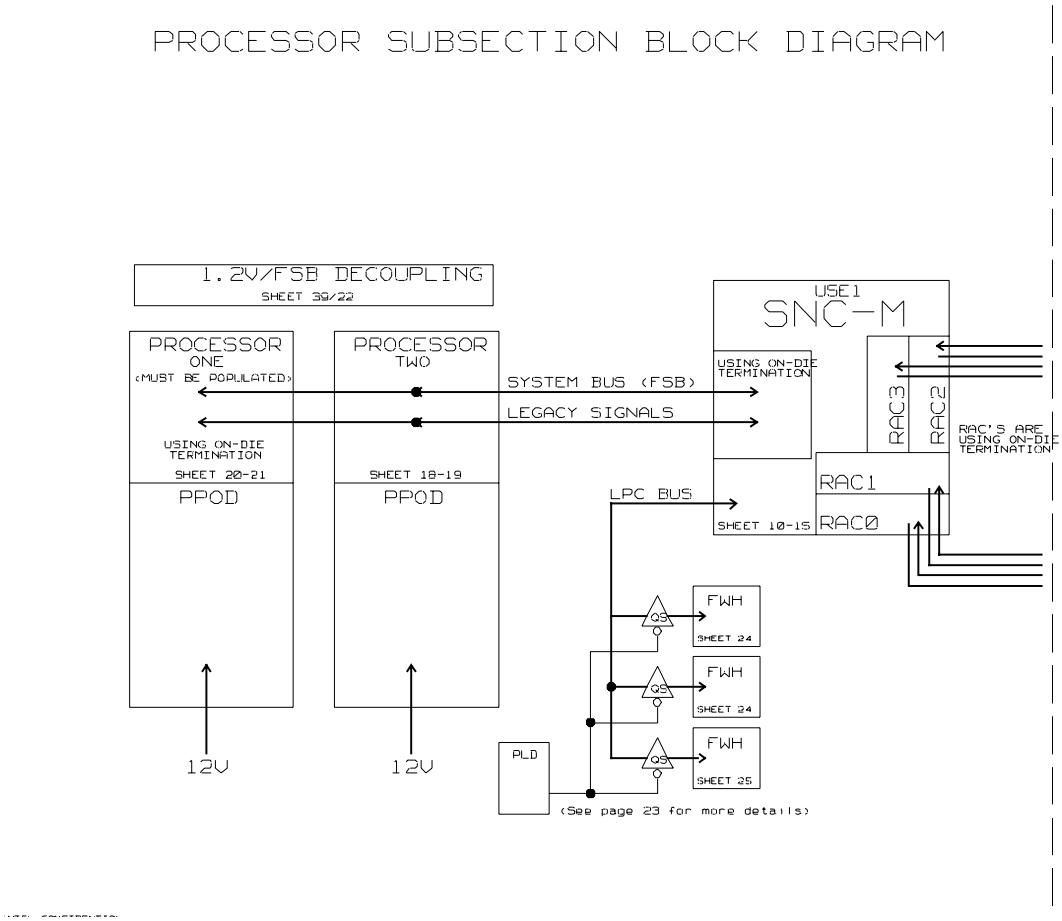


Figure 4. Processor Subsection Block Diagram

2.2.2 Memory Interface

The Itanium 2/870 memory subsystem consists of four memory repeater (MRH-D) chips, one per RDRAM channel of the SNC-M, which support up to two 72-bit wide DDR full-height 1.7” DIMM modules. The MRH-D translates Rambus memory transactions to SDRAM DDR. The DIMM modules can be 64, 128, 256, 512 MB, 1 and 2 GB technologies, supporting up to 16 GB of system memory.

Note: The DIMM’s off each MRH-D must be symmetrical with the DIMM’s of all the other MRH-Ds. That is, each MRH-D must hold the same type of DIMM on MRH-D 1, 2, 3, and 4. The memory upgrade granularity is the row of four DIMM’s that collectively provide a cache line.

The SNC-M and MRH-D incorporate a 400 MHz Rambus interface. Data is transferred on each edge of the clock giving an equivalent 800 MHz bus, 16-bit data and 2-bit ECC running at 1.6 GT/s per port. Each of the four Rambus ports on the SNC-M is connected to an MRH-D.

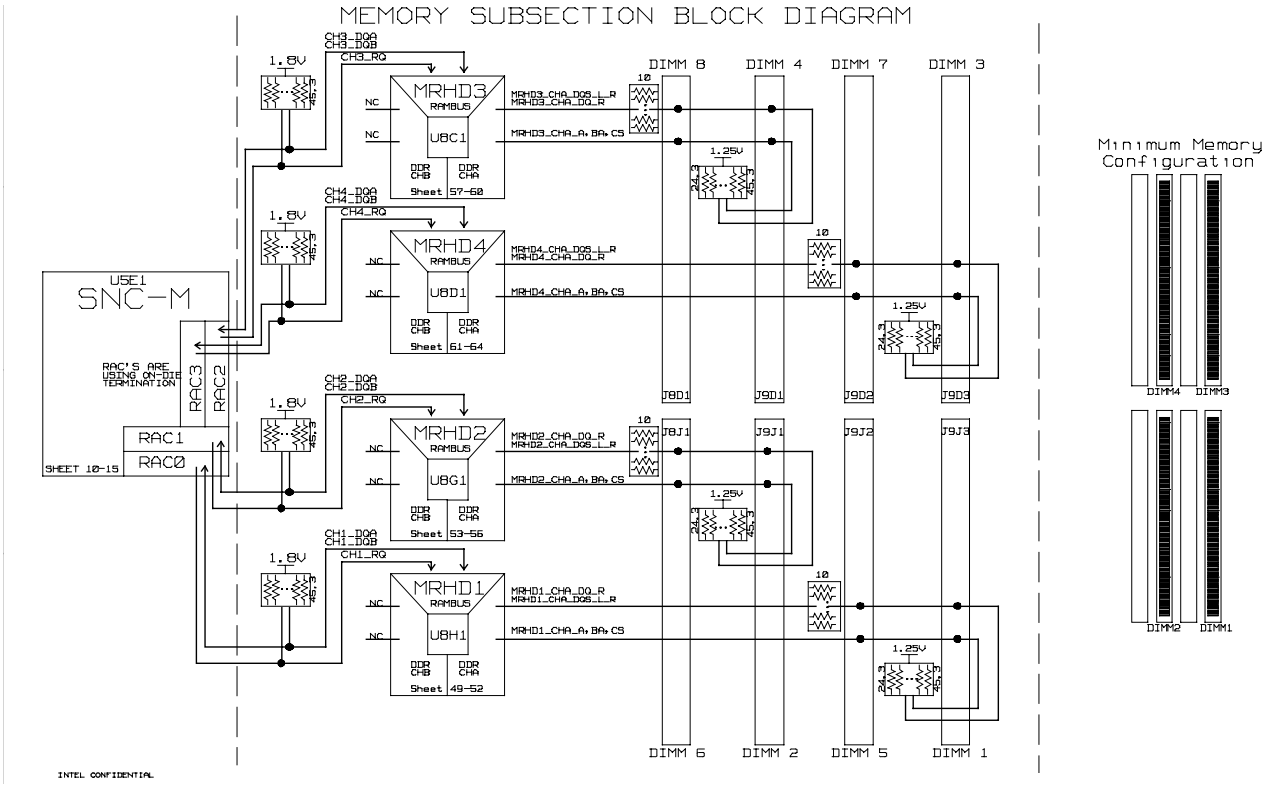


Figure 5. Memory Subsection Block Diagram

2.2.3 DDR Memory Array

The memory array consists of eight DIMM sockets. Four SNC-M Rambus memory channels are translated into four DDR channels using the MRH-D devices. Each channel consists of two DIMM sockets. Each SNC-M channel has a maximum bandwidth of 1.6 GB/s, for a total of 6.4 GB/s for the system.

2.2.3.1 Memory Configurations

This board will support the following DDR DRAM technologies and DIMM sizes *(all combinations not yet known).* A subset of these will be validated. Pease refer to the *SR870BH2 Memory Validation Test Plan* for details on supported and tested configurations.

Table 2-1. Available Memory Configurations

Device Technology	DIMMs				Node Cap (MB)	
					Min	Max
Mb	# devices	Org	MB x72	MB	4	8
64	9	2Mx8	8	64	256	512
	18	2Mx8 stk 4Mx4	16	128	512	1024
	36	4Mx4stk	32	256	1024	2048
128	9	4Mx8	16	128	512	1024
	18	4Mx8stk 8Mx4	32	256	1024	2048
	36	8Mx4stk	64	512	2048	4096
256	9	8Mx8	32	256	1024	2048
	18	8Mx8 stk 16Mx4	64	512	2048	4096
	36	16Mx4stk	128	1024	4096	8192
512	9	16Mx8	64	512	2048	4096
	18	16Mx8 stk 32Mx4	128	1024	4096	8192
	36	32Mx4stk	256	2048	8192	16384
1024	9	32Mx8	128	1024	4096	8192
	18	32Mx8 stk 64Mx4	256	2048	8192	16384

2.2.3.2 DIMM Population Rules

The DIMM's off each MRH-D must be symmetrical with the DIMM's off all the other MRH-Ds. That is DIMM's 1, 2, 3, and 4 must have the same DIMM's. The DIMM's in slots 5, 6, 7, and 8 may be unpopulated or a different type of DIMM, as long as they are the same as one another.

2.2.4 MRH-D

The MRH-D component provides the ability to support two DDR "branch channels" on one SNC-M Rambus expansion channel. It acts as a translator for turning Rambus accesses into DDR accesses and vice versa.

2.2.5 North Bridge Port 80 Connector

A connector is provided for Port 80 output of Power On Self Test (POST) codes. J6G1 is a five-pin header with pin 4 missing as a key pin.

2.2.6 VHDMs

The SR870BH2 Mainboard and PCI Riser board connect through two VHDM (6 row x 35 columns or 210 pins) connectors. These are stripline connectors with the right angle receptacle version on the PCI Riser board and the header version on the Mainboard. The VHDM connector has a ground shield between each row of signals. Therefore in a 6 x 35 configuration there are 35 ground shields reducing crosstalk and other unwanted effects on high-speed signals. VHDM0 contains the Scalability Port I/O bus interface. VHMD1 contains Hub Link 2.0, Hub Link 1.5, Power, and Misc. signals. The Mainboard and PCI Riser are shown below in Figure 1, with pin-out orientation specific information.

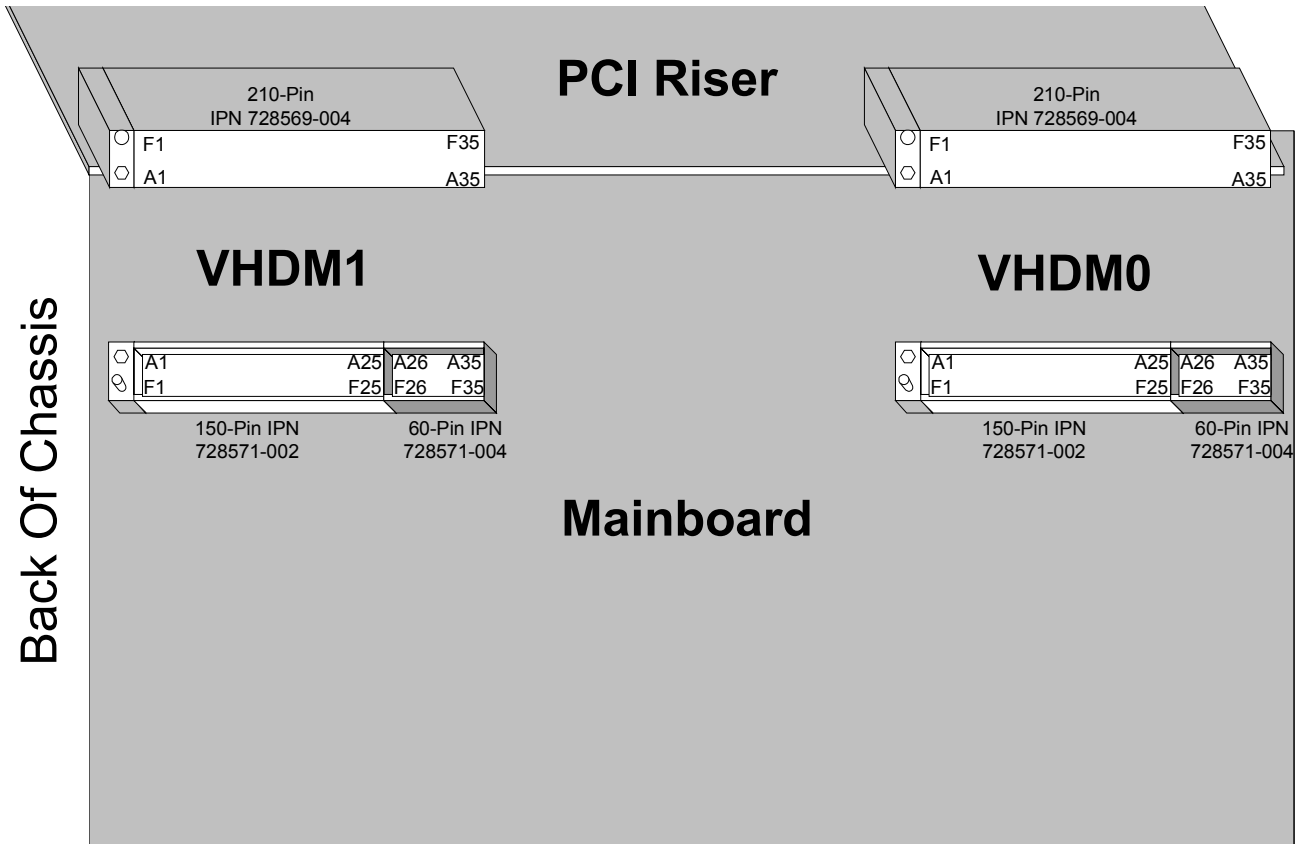


Figure 6: VHDM0 and VHDM1 Connector Orientation

2.2.6.1 Scalability Port I/O Bus Interface

The primary interface between the Mainboard SNC-M and the PCI Riser Board SIOH is the scalability port (SP) bus. The scalability port is a simultaneous bi-directional (SBD) tri-level bus, which provides a high-speed point-to-point link between the processor system and the I/O system.

Each port is a 4 byte, quad-pumped (4x) 200-MHz bus. This gives a raw throughput of 3.2 GB/s per direction for each bus off the SNC-M. The SNC-M has two SP ports that combined have a total bandwidth of 6.4 GB/s per direction, or a total bi-directional bandwidth of 12.8 GB/s.

2.2.7 P64H2

The P64H2 component is the PCI bridge controller component of the 870 chipset. It connects to the system through the HL2 bus coming from the SIOH component located on the PCI Riser Board. The P64H2 has two independent PCI-X bus interfaces capable of supporting to 133-MHz PCI-X bus devices.

See the P64H2 *Electrical Design Specification* for more details on the chip's functionality.

2.2.7.1 Power and Thermal Requirements

The P64H2 requires 1.8 V and 3.3 V for its operation. 1.8 V is used by the component's core and HL2 port termination. 3.3 V is used by the PCI ports termination. The P64H2 in this application requires a heat sink for proper thermal operation. For more information see the P64H2 Thermal Design Guide.

2.2.7.2 PCI Bus A

The P64H2 uses its PCI Bus A to control the Intel 82546 Dual-GbENET Controller. This is a PCI-X 133 MHz compliant bus.

2.2.7.3 PCI Bus B

The P64H2 uses its PCI Bus B to control the LSI52C1030 SCSI Controller. This is a PCI-X 133 MHz compliant bus.

2.2.8 SCSI Interface

A single LSI 53C1030 Ultra 320 LVDS controller provides the integrated SCSI interfaces. The controller resides on PCI Bus Segment B. The controller communicates as a 64-bit PCI-X device for optimum performance. The controller's PCI-X interface operated at a bus speed of 133 MHz. The configuration registers define PCI-related parameters for the LSI53C1030 device. The LSI53C1030 supports all mandatory registers in the PCI configuration space header including the Vendor ID, Device ID, Class Code, Revision ID, Header Type, and Command and Status fields.

The LSI53C1030 supports two Ultra 320 LVDS channels. One is intended for control of internal drives, and the other is intended for high-speed connection to an external SCSI device. SCSI port 'B' of the LSI53C1030 controls the internal SCSI channel. The internal channel is routed to the SR870BH2 SCSI board via a SCSI U320 cable. The internal channel has been validated only for LVDS operation. SCSI port 'A', of the LSI53C1030, controls the external SCSI channel. The external channel connector is located near the LSI53C1030 chip where it can be cabled to the system chassis bulkhead connector. The external channel can be operated with LVDS or SE signaling, provided the external cabling supports the required signaling.

A PCI-X 'RAID' adapter is supported by unplugging the internal SCSI 'B' channel cable on the Mainboard and SCSI board then utilizing the cable routing channel for the 'RAID' cable.

The LSI53C1030 supports Imbedded Mirroring via NVSRAM and PLD logic. IM allows the user to stripe information to the SCSI drives on the SCSI board.

The LSI53C1030 operates on 1.8 V and 3.3 V. 1.8 V powers the LSI53C1030's core and 3.3 V powers the PCI-X and SCSI interfaces.

The LSI53C1030 uses an 80-MHz crystal to clock the SCSI interface.

Refer to the LSI 53C1030 data sheets at http://www.lsilogic.com for more details on the SCSI controller operation.

2.2.9 82546EB Dual Port Gigabit Ethernet Controller

82546EB Dual Port Gigabit Ethernet Controller is a single component with two full Gigabit Ethernet MAC and PHY layer functions to provide two standard IEEE 802.3 Ethernet interfaces for 1000Base-T, 100Base-TX, and 10Base-T applications (802.3, 802.3u, 802.3ab).

1. Capable of transmitting and receiving two channels of data at up to 1000 Megabits per second
2. Provides a single, direct PCI 2.2 and PCI-X 1.0a compliant bus operating as a single multifunction device at clock frequencies up to 133 MHz
3. SMBus port enables network manageability implementations required by IT personnel for remote control and alerting via the LAN
4. Caches up to 64 packet descriptors in a single burst for efficient PCI bandwidth usage
5. 64-KB on-chip packet buffer
6. Does not require a heat sink in this Application

The 82546EB accesses a 64 register by 16-bit serial EEPROM device, AT93C66, automatically after reset for pre-boot configuration data before it is accessed by host software. The MAC address, serial number, and additional configuration information stored in the EEPROM is available to software

2.2.9.1 Dual RJ45 Ethernet Connector

The board provides a dual-RJ45 connector (JA4A1) for Ethernet connection.

Below are definitions of the speed/status LED's.

1. Speed LED: Yellow On, 1000-Mbps Ethernet
2. Speed LED: Green On, 100-Mbps Ethernet
3. Speed LED: Off, 10-Mbps Ethernet
4. Status LED: Green On, Ethernet link detected
5. Status LED: Off, Ethernet link not found
6. Status LED: Green Flashing, Ethernet data activity

2.2.10 ICH4

The ICH4 is a 421-pin Enhanced Ball Grid Array (EBGA), Intel 82801DA chip. The ICH4 provides the following features:

1. PCI Bus Interface

- Supports PCI at 33 MHz, 32 bit
- Supports PCI Specification, Revision 2.2

2. Integrated IDE Controller
   - Independent timing of up to two drives
   - Ultra* ATA 100 (SR870BH2 supports ATA 33)
   - Implements Write Ping-Pong Buffer for fast write performance
3. USB
   - Two USB host controller with total four ports
   - USB 2.0 compliant (SR870BH2 supports 4 x USB 1.1)
   - Supports wake-up from sleeping state
4. Interrupt Controller
   - Support up to eight PCI interrupt pins
   - Two cascade 82C59
   - Integrated I/O APIC capability
   - 15 interrupts supported in 8259 mode; 24 supported in I/O APIC mode
   - Support serial interrupt protocol
   - Support Front-Side bus (FSB) interrupt delivery
5. 1.5-V core with 3.3-V I/O
   - 5-V tolerant buffers on IDE, PCI, USB Over Current (OC) and legacy signals
6. Hublink 1.5 Interface
7. Firmware HUB interface (mux with LPC bus pins)
   - Supports BIOS memory size up to 8 MBs, 6MB in this application
8. LPC Bus
   - Allows connect of legacy chip such as Super I/O, FWH's, and BMC
   - Support two master / Direct Memory Access (DMA) devices
9. SM Bus
   - Supports host interface; allow delivery POST80 code
   - Supports slave interface (not used in this application)
10. Real-Time Clock (RTC)
    - 256-byte battery-backed CMOS RAM
    - Hardware implementation to indicate century rollover

Table 2-2. ICH4 Strap Option

Part	Default	Description
R6G25	Install	No boot option for ICH4.
R5E6	Not installed	Test for ICH4's GPIO16 (Integrated PU resistor).

2.2.11 South Bridge Port 80 Connector

Table 2-17 shows the pin-out for the Port 80 connector (J5G1) connecting to the ICH4. Pin 4 is missing as an orientation key.

Table 2-3. South Bridge Port 80 Connector Pin-out

Signal Name	J5G1 Pin
+12V	1
SMBDATA	2
SMBCLK	3
GND	5

2.2.12 Rear USB Connectors

J3A1 is a single connector housing with two integral USB receptacles. The connector is shown in Table 2-18.

Table 2-4. Rear USB Connector Pin-out

Signal Name	J3A1 Pin
+5V (fused & filtered)	1
USB_P1_M_CONN	2
USB_P1_P_CONN	3
GND (thru ferrite)	4
+5V (fused & filtered)	5
USB_P0_M_CONN	6
USB_P0 _P_CONN	7
GND (thru ferrite)	8
GND	9
GND	10
GND	11
GND	12

2.2.13 Video

The SR870BH2 Mainboard utilizes an ATI Rage XL video chip. Its core processors run at 2.5 V, while its I/O has a 3.3 V interface. The video circuit has 8-MB SDRAM support. The video chip sits on the PCI bus from the ICH4 with IDSEL = AD17. It does not use the PCI IRQ line.

On the Beta revision, provision is made for a Front Panel video connector. Whenever a video monitor is plugged into the Front Panel video jack, the VID_FRNT_PRES_L line is pulled low. This signal enables circuits that divert the video monitor signals from the rear video jack to the Front Panel video jack through the 120-pin flex cable connector. The goal of the signal quality out the front is such that the platform will support resolutions up to and including 800x600. Due to design constraints, resolutions higher than this are not supported due to signal degradation.

2.2.14 120-Pin Flex Cable

The IDE bus originates from SR870BH2 Mainboard ICH4 south bridge controller and is passed to the Front Panel board through the 120-Pin Flex Cable. This permits interfacing to internal devices in the disk bay such as CDROM, DVDROM, DVDRAM, or LS240 floppy devices. That is to say all IDE ATA-33 compliant devices are supported, but actual device shipped with product may very depending on qualified components.

2.2.14.1 IDE Signal Descriptions

Refer to *Table 2-5* for a summary of the IDE interface connector signal pins that pass to the Front Panel Board, including the signal mnemonic, name, and brief description.

Table 2-5. IDE Signal Descriptions

Signal	Name and Description
IDE_CS1_L	Select Command Register Block.
IDE_CS3_L	Select Control Register Block.
IDE_DA[2:0]	Register Select Address (from ISA address bus).
IDE_DACK_L	Direct Memory Access (DMA) Acknowledge.
IDE_DD[15:0]	ISA Data.
IDE_DIOR_L	Read Request. Handshake request for read operations.
IDE_DIOW_L	Write Request. Handshake request for write operations.
IDE_DREQ	Direct Memory Access (DMA) request.
IDE_IORDY	Ready. Optional. Device ready for operation (high).
IDE_IRQ	IRQ14 Interrupt Request.
RST_PCIRST_L	Reset. Forces drivers on the ISA bus to initialize.

2.2.15 BMC

The BMC component connects to the ICH4 via the LPC bus and is the main engine of the systems server management. The BMC supports IPMB and EMP ports. It has six general I^2C buses and eight A2D pins for power monitoring. General Purpose I/Os (GPIOs) are used to support system functionality such as power up and reset sequence, front panel access, and in-system programming (ISP) / JTAG programming.

The BMC ASIC contains an ARM7TDMI core and associated peripherals. It is designed for use as the central server management controller in a server system. The BMC contains the logic needed for executing firmware, controlling the system, monitoring sensors, and communicating with other systems and devices via various interfaces.

In this implementation, the BMC is running at 40 MHz from an external oscillator. This chip and whole server management circuit is supplied with standby power. The BMC has a parallel bus that is used to connect SRAM and boot flash. A Programmable Logic Device (PLD) is connected to the BMC and designed to route additional server management signals and expand the BMC's I/O ports.

The BMC is used to support the following features on the SR870BH2 Platform:

1. ARM7TDMI processor core with JTAG connection for In-Circuit Emulation (ICE).

2. 32 KB of internal program/data RAM.

3. External parallel bus interfaces: Supports 512 KB SRAM and 1 MB Flash. The parallel bus is also routed to PLD1 for BMC expansion port.

4. 32-input interrupt controller supporting internal peripherals and eight external interrupts.

5. Two 16550-compatible serial Universal Asynchronous Receiver/Transmitters (UARTs) with integrated baud rate generators. One is used as the EMP port and another UART is not used.

6. Real-Time Operating System (RTOS) timer.

7. Watchdog timer.

8. RTC synchronization clock divider. A 32-kHz clock is provided from ICH4.

9. Eight 10-bit A/D converter channels used to monitor some of the power voltages

   - 5 V Standby
   - 3.3 V Standby
   - 2.5 V Standby
   - 1.5 V Standby
   - 3.3 V
   - 2.5 V
   - 1.3 V
   - 1.2 V
   - Other powers are monitored at the ADM1026.

10. LPC interface supporting the following features:

    - Slave interfaces: three 8042 Keyboard Controller Style (KCS) interfaces
    - Snoop Interface: specific I/O write cycle data snooping
    - Master Interface

11. Two master/slave, four master-only I^2C interfaces. This includes I^2C for IPMB, PCI, LAN, SYS, SMB and I/O.

12. Many pins usable as general purpose I/O.

13. Four LED drivers to support Power On, General Fault, Fan Fault, and Power Fault LED.

14. Parallel bus interface with PLDs to provide BMC expansion ports.

15. Support ISP chain PLD update utility via BMC's expansion port.

16. 40 MHz clock from external oscillator.

17. 156-pin Ball Grid Array (BGA) package.

Table 2-6. BMC Pins and Signals Group Description

Signal Group / Name	Description
SMM_A[22:0]	Output, BMC memory address. Routed to SRAM, BMC Flash and PLD1.
SMM_D[15:0]	Bi-direction, BMC data bus. Routed to SRAM, BMC Flash and PLD1.
BMC_RST_R_L	Input, BMC reset line. Generated from P3_3VSTBY_GD and hardware validation jumper.
BMC_40MHZ_OSC	BMC clock input, 40-MHz from oscillator (45/55 Duty cycle required).
LPC_BMC_LDRQ1_L	LPC bus master channel one, routed to ICH4 LDRQ1.
BMC_SCI_L	BMC server management interrupt. Routed to ICH4's RI_L pin, which is able to generate system configure interrupt (SCI).
BMC_LRST_PCIRST_L	PCI Reset line. Resets BMC LPC bus.
BUS_ISOLATE_L	When Voltage Controlled Current (VCC) power is not present, this signal will isolate BMC from LPC bus.
LPC_ICH_LAD[3:0], LPC_ICH_LFRAME_L	Five-wire LPC bus interface. Connects to ICH4, SIO, FWH.
XINT[7..0]	BMC IRQs. Connects to miscellaneous server management signals.
PMI_L	Platform Management Interrupt (PMI) IRQ line from CPLD.
BMC Serial Port 0	Used as EMP port.
BMC Serial Port 1	Not used
BMC I2C Buses	Six I^2C* buses, routed to I/O board, processor board, memory, etc.
BMC_SPKR_PLD2	Output, speaker output signal. Routed to CPLD where AND-ed with ICH4 speaker out signal. The AND-ed output signal routed to front panel.
PIRQE	Input to BMC, active high interrupt. Inverted from PIRQE_L of ICH4.
A2D[7..0]	BMC AD converter input pins. Monitor power voltages.
BMC_VREF	Voltage reference for A2D converter. Uses 2.5 V input from shunt regulator U1B2.
BMC_PLD_RST_L	Output from BMC, resets PLD2.
BMC_D2D_EN	D2D enable, routed to PLD1.
BMC_PS_ON_L	Output from BMC, power switch on signal routed to PLD1. PLD sends this signal to ICH4.
SM_PWRBTN_L	Power button signal, routed to PLD. PLD sends this signal out to ICH4.
PWR_BTN_DBNC_L	Debounced Power On switch input to BMC. Signal comes from front panel.
RST_BTN_DBNC_L	Debounced Reset switch input to BMC. Signal comes from front panel.
SDINT_ BTN_DBNC_L	Debounced SDINT switch input to BMC. Signal comes from front panel.
BMC_WE_L	BMC write enable. Routed to SRAM, Flash, PLD.
BMC_OE_L	BMC output enable. Routed to SRAM, Flash, PLD.
BMC_FLASH_CE_L	BMC chip select output for FLASH memory.
BMC_SRAM_CE_L	BMC chip select output for Static Random Access Memory (SRAM).
BMC_FRC_UPDATE_L	BMC update request, connected to DIP switch.

2.2.16 Firmware Hub (FHW)

The Mainboard contains a total of four firmware hub flash parts (2MB TSOP40 package). Three of the FWH's are off the North Bridge (SNC-M) and one is off the South Bridge (ICH4). Currently ID0 and ID2 off the North Bridge can be swappable via an onboard jumper or SMFW GPIO. The intent here is to support a BIOS recovery if the lower 2MB of the FW becomes corrupted. ID 5 and 6 off of the South Bridge are not currently populated, but the footprint sites are available. FWH's to the SNC-M stay on the same LPC bus with quick switch isolation. This is also the case for the ICH4 FWH's. This isolation is utilized for quick parallel programming during In-Circuit Test (ICT) for throughput optimization. The FWH off of the ICH4 has a dedicated 33 MHz clock.

The 3.3 V power is connected to VPP pins of the FWH's through FETs. For normal FWH write access, the 3.3 V power is always on the VPP pin. For manufacture programming, an ICT machine call will pull low transistors' gate (pin 1), thus isolating the 3.3 V from VPP. At the same time, the ICT machine can inject 12 V power on VPP. This speeds up the programming process, lowering the overall programming time for the Mainboard.

Each FWH has five general input pins, giving a total of 20 General Purpose Inputs (GPIs). The lower 4 bits of FWH ID0 and ID2 define the PCB version. For example, the third fabrication of the board is set to 0011. GPI of the FWH ID1 off of the SNC-M and the upper GPI for ID0 and ID2 are not used. FWHs ID5 and ID7 off of the ICH4 have their GPIs tied to jumpers for CMOS clearing, Password Clearing, and Recovery boot operations, respectively.

* Configurations and quantity of FWH's may change in future for additional BIOS features.

2.2.17 Super I/O

The SMCS Super I/O is used to provide two serial ports. The chip also on the ICH4 LPC bus and has AMI* BIOS inside. The serial port address setting is at 0x2E as the default. For details on these I/O ports, see the SMSC LPC47B27 Super I/O Controller with LPC Interface for Consumer Applications Specification. Signals for both serial ports are routed to PLD2 where COM2 is then routed to the rear serial port connector. COM1 is routed to the internal 2x5 header, J8A1 located on the rear of the Mainboard behind the memory section, for WHQL compliance.

2.2.18 Rear Serial Port through RJ-45 Connector

The SR870BH2 Mainboard is equipped with an external RJ-45 connector located at J3A2 on the back of the chassis. It will support any standard serial device, as well as providing support for serial port concentrators.

Although the RJ-45 serial port is capable of supporting all standard serial signals with only eight pins, it can only be configured to support either a DSR or DCD signal at a given time. The Jumper J1A1 controls signal RSRL_MODE0_L to PLD2. PLD2 then configures pin 7 of the Serial port to DSR if in factory default position 1-2 or DCD if moved to pin 2-3. A typical DCD device would be a Modem.

Adapters or Dongles from the RJ-45 are configured as DSR-Peripherals or DCD-Modem. The adapter you choose to use must match the configuration of the serial port Jumper settings. DSR-peripherals is the factory default setting of 1-2 on jumper J1A1. The MM number for these adapters is 838996. Note that the documentation associated with this part number is for a different Intel server design and this documentation will supercede any provided document with 838996.

2.2.19 Internal COM1 Header

The SR870BH2 Mainboard is equipped with an internal COM1 connector. It will support any standard serial device, as well as providing support for serial port concentrators. COM1 is routed to the internal 2x5 header, J8A1 located on the rear of the Mainboard behind the memory section, for WHQL compliance.

2.2.20 Voltage Distribution

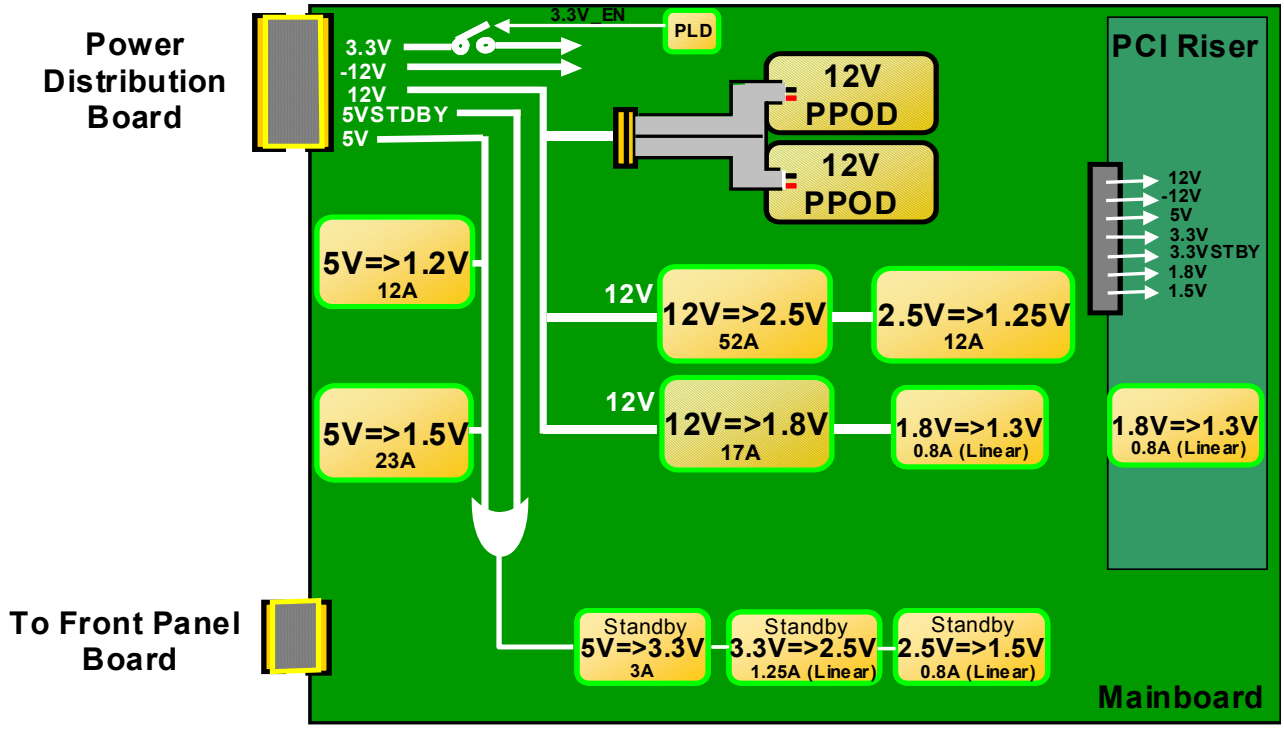


Figure 7: Voltage Distribution

2.2.20.1 Voltage Regulators

The power supply bay docking connector on the Mainboard receives various voltage rails from the Power Supply Bay. They are 12 V, -12 V, 5 V, 5 V Standby, and 3.3 V. The 3.3 V is switched off at a point between the connector and loads until enabled by the power sequencing logic. This is to meet the power sequencing requirements for various chipset components as well as the LSI 53C1030 SCSI ASIC.

Each installed processor has a power pod powered by 12 V through a cable between the Mainboard and the power pods.

5V and 3.3V rails are used for miscellaneous components and are passed to the PCI Riser for PCI Power as is -12V.

The Mainboard board has six embedded D2D regulators and three linear regulators to supply other required voltages.

Table 2-7. Voltage Regulator Table

Output Voltage	Current Capacity	Regulator Type	Regulator Drive Voltage	Where Used
2.5 V	52 A	D2D	12 V	Video controller, DIMM power, and drive for 1.25 V regulator
1.8 V	17 A	D2D	12 V	MRH-D, P64H2, SIOH, SNC-M, 1.8V to 1.3V regulators
1.5 V	23 A	D2D	5 V	SNC-M, SIOH, ICH4
1.2 V	12 A	D2D	5 V	AGTL+ FSB Terminators, SNC-M, and ICH4
3.3 V Standby	4 A	D2D	5 V when available, or 5 V Standby	Drive for 2.5 V Standby regulator, GENET, ICH4, BMC, Server Management components
1.25 V	12 A	D2D	2.5 V	DDR DRAM terminations
1.3 V	0.8 A	Linear	1.8 V	SNC-M, SIOH SP bus logic
2.5 V Standby	1.25 A	Linear	3.3 V Standby	GbENET Controller and RJ45 connectors with magnetics.
1.5 V Standby	0.8 A	Linear	2.5 V Standby	GbENET, ICH4

2.2.20.2 Embedded Regulator Voltage Controller

The table below points out the VID bit setting for the appropriate voltage output of the HIP6311 Multi-phase buck PWM controller.

2.2.20.3 Processor Power Pod

A power pod supplies the voltage for each of the two processors independently. Each power pod will provide the processor and cache with the voltages they require from the +12 V power rail provided to it from the processor board. The 12 volts will be supplied to the processor power pods via a Y-cable from a 12-pin connector on the Mainboard to each power pod.

The following list shows the features of the power pod regulator:

1. 12 V input @ 27 A +/- 10%
2. 12 V ground return
3. Output: 0.95 V to 1.70 V @ 130 W
4. Efficiency at 130 W greater than 80%

2.2.20.4 +2.5 V Embedded Regulator

The 2.5 V voltage regulator circuit utilizes a HIP6311A controller, which provides accurate, high drive, programmable supply voltage. The 2.5 V regulator on the Mainboard provides power for the DIMM interface pins of the MRH-D, 1.25 V regulator, and DDR DRAMs.

1. 0 A to 52 A maximum output current
2. 85% efficiency at maximum load
3. Active-High PWRGD open-collector output
4. Active-Low output disable input
5. Short circuit protection

Table 2-8. 12V to 2.5V Typical Voltage and Tolerance

Voltage	Description	Min	Typical	Max	Tolerance
12 V	Input voltage	10.8V	12 V	13.2V	+/-10%
2.5 V	DIMM interface Power, Video	2.375V	2.5	2.625 V	+/- 5%

2.2.20.5 +1.2 V Embedded Regulator

The 1.2 V voltage regulator circuit utilizes a HIP4006E controller, which provides an accurate, high drive programmable supply voltage to the processor bus. The following list shows the features of the onboard +1.2V regulator.

1. 0 A to 16 A maximum output current
2. 85% efficiency at maximum load
3. Active-High PWRGD open-collector output
4. Active-Low output disable input
5. Short circuit protection

Table 2-9. 5V to 1.2 V Typical Voltage and Tolerance

Voltage	Description	Min	Type	Max	Tolerance
5 V	Input voltage	4.75 V	5 V	5.25 V	5%
1.2 V	Output buffer and termination voltage for FSB AGTL+ drivers on Processors and SNC	1.182 V	1.2 V	1.218 V	+/-*1.5%

*DC variation only.

2.2.20.6 +1.5 V Embedded Regulator

The 1.5 V voltage regulator circuit utilizes a HIP6311A controller, which provides accurate, high drive, programmable supply voltage to the Intel 870 SNC-M, SIOH, and ICH4. The following list shows the features of the onboard VCC 1.5 voltage regulator.

1. 0 A to 25 A maximum output current
2. 85% efficiency at maximum load
3. Active-High PWRGD open-collector output
4. Active-Low output disable input
5. Short circuit protection

Table 2-10. 5V to 1.5V Typical Voltage and Tolerance

Voltage	Description	Min	Type	Max	Tolerance
5 V	Input voltage	4.75 V	5 V	5.25 V	+/-5%
1.5 V	Provides core voltage to Intel® 870 SNC-M, SIOH and ICH4 components	1.425 V	1.5 V	1.575 V	+/-5%

*SIOH is located on the PCI Riser board

2.2.20.7 +1.8 V Embedded Regulator

The 1.8 V voltage regulator circuit utilizes a HIP6311A controller, which provides accurate, high drive, programmable supply voltage to the Intel 870 SNC-M, P64H2's and MRH-D components, and defines the RSL logic. The following list shows the features of the onboard VCC 1.8 voltage regulator.

1. 0 A to 17 A maximum output current
2. 85% efficiency at maximum load
3. Active-High PWRGD open-collector output
4. Active-Low output disable input
5. Short circuit protection

Table 2-11. 1.8 V Tolerance

Voltage	Description	Min	Type	Max	Tolerance
12V	Input voltage	10.8V	12 V	13.2V	+/-10%
1.8 V	Provides core voltage to MRH-D component	1.71 V	1.8 V	1.89 V	+/-5%

2.2.20.8 +1.3V Linear Regulator

The 1.3 V voltage regulator circuit utilizes an EZ1581 linear regulator, which provides accurate voltage to the Intel 870 SNC-M SP bus drivers. The following list shows the features of the onboard 1.3 V voltage regulator.

1. 2.0 A MAX output current
2. 70% efficiency at maximum load
3. Thermal shutdown short circuit protection
4. Active-High output disable input (3.3 V enables circuit, 0 V disables output)
5. Output protection Schottky to input

Table 2-12. 1.3 V Tolerance

Voltage	Description	Min	Type	Max	Tolerance
1.8 V	Input Voltage	1.71 V	1.8 V	1.89 V	+/-5%
1.3 V	SP bus voltage	1.235 V	1.3 V	1.365 V	+/-5%

2.2.20.9 +1.25V Embedded Regulator

The 2.5-V to 1.25-V D2D provides the DDR termination voltage. Per Dynamic Data Read (DDR) specification, the converter output is required to track DC fluctuations in the 2.5-V input. The following list shows the features of the +1.25V regulator:

1. 0 A to 12 A maximum output current
2. 85% efficiency at maximum load
3. Active-High PWRGD open-collector output
4. Active-High output enable input
5. Over-current protection
6. Over-voltage protection

Table 2-13. 1.25 V Tolerance

Voltage	Description	Min	Type	Max	Tolerance
2.5 V	Input voltage reference	2.375V	2.5	2.625 V	+/- 5%
1.25 V	Output voltage for DIMM terminators	1.188 V	1.25 V	1.312 V	+/-5%

2.2.20.10 Embedded +5V Standby or +5V to +3.3V Standby Regulator

+3.3V Standby is provided through a switching regulator that is powered by +5V Standby until the PWOK_ORED signal is asserted when one or more power supply modules is powered on and within regulation. When PWOK_ORED is driving high, the current source for the regulator is switched from +5V Standby to +5V. This is achieved via a TPS2815 dual high speed MOSFET driver with external P-Channet Fet drivers. The following list shows the other features of the +3.3V Standby regulator:

1. 0 A to 4 A maximum output current
2. 85% efficiency at maximum load
3. Active-High power good output signal

Table 2-14. 3.3 V Standby Tolerance

Voltage	Description	Min	Type	Max	Tolerance
5 V	Input voltage	4.75 V	5 V	5.25 V	+/-5%
5 V Standby	Input voltage	4.75 V	5 V	5.25 V	+/-5%
3.3 V Standby	Output voltage	3.135 V	3.3 V	3.465 V	+/-5%

2.2.20.11 Embedded +2.5V Standby Linear Regulator

The +2.5V Standby is regulated down from +3.3V Standby through a linear regulator IC for use by the GbENET controller.

Table 2-15. 2.5 V Standby Tolerance

Voltage	Description	Min	Typical	Max	Tolerance
3.3 V Standby	Input voltage	3.135 V	3.3 V	3.465 V	+/-5%
2.5 V Standby	GbENET controller standby power	2.375V	2.5	2.625 V	+/- 5%

2.2.20.12 Embedded +1.5V Standby Linear Regulator

The +1.5V Standby is regulated down from +2.5V Standby through a linear regulator IC for use by the ICH4 and GbENET.

Table 2-16. 1.5 V Standby Tolerance

Voltage	Description	Min	Typical	Max	Tolerance
2.5 V Standby	Input voltage	2.375V	2.5	2.625 V	+/- 5%
1.5 V Standby	ICH4 standby power and GbENET	1.425 V	1.5 V	1.575 V	+/-5%

2.2.21 Programmable Logic Devices

There are two programmable logic devices (PLD) on the Mainboard. The first PLD is the Power Good/Reset/BMC Expansion port PLD. This device's primary responsibility is managing the power sequencing described in above. However, the PLD also provides logic that performs reset, NMI/SDINT, PMI, PME, server management, and ISP functions. See diagrams below for more information on the specific functions of PLD1.

The second PLD is supports COM/EMP port routing, Error event handling, PME, and SCSI Integrated Mirroring NVSRAM interface. As an additional feature, this PLD also controls firmware hub initialization. See diagrams below for more information on the specific functions of PLD2.

2.2.22 Power-Up Sequence

Tiger2 Power Sequencing Diagram (In reference to PLD1 on the Mainboard)

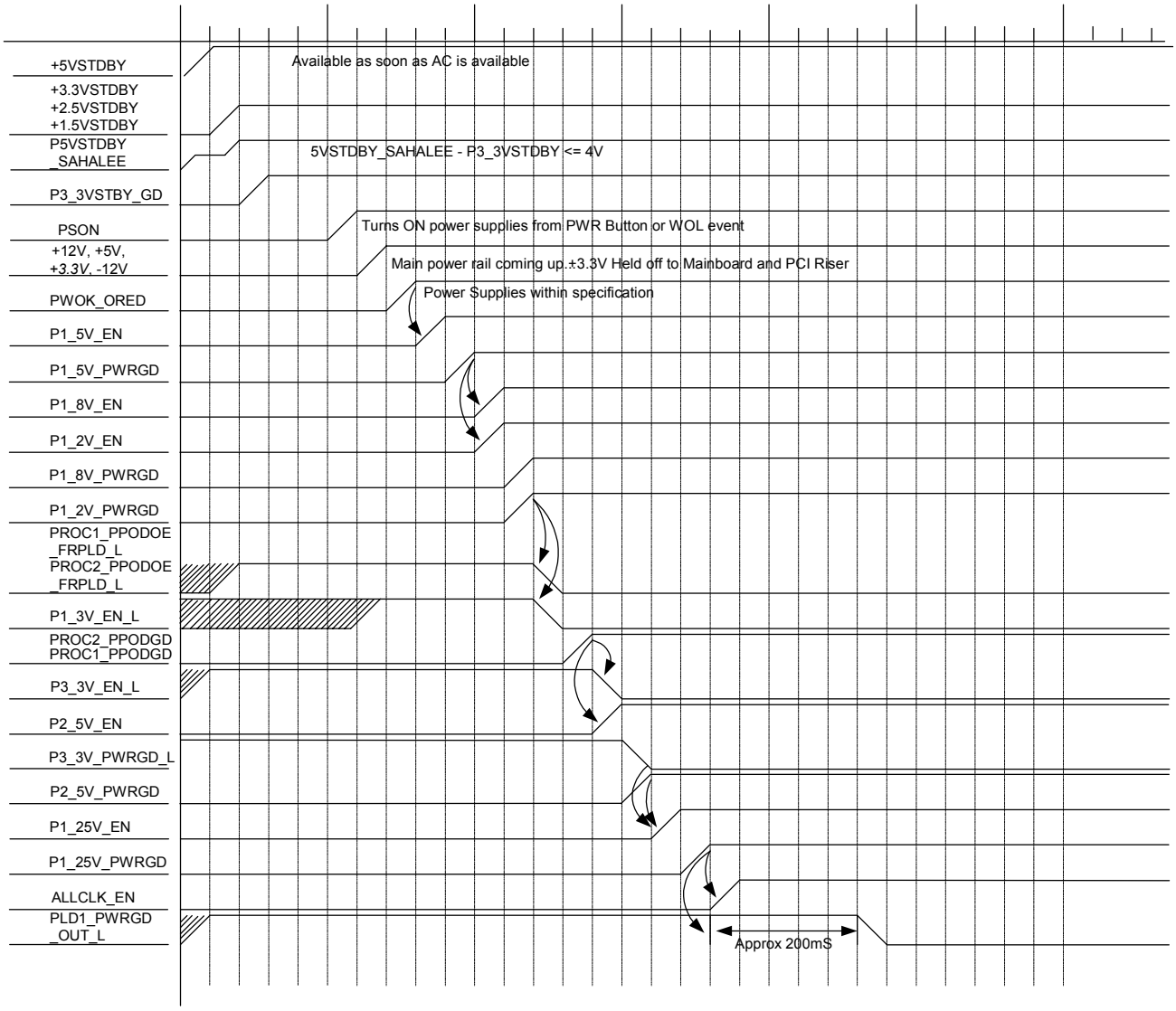


Figure 8. SR870BH2 Power Sequencing Diagram

1. With no +3.3VSTDBY available, a 3 V, 500 mAh battery powers the nonvolatile memory in the SCSI circuit, and also the 32KHz clock oscillator and the Real Time Clock (RTC) functions of the ICH4.
2. When one or more of the power supplies is installed and the AC power is provided, 5VSTDBY is supplied to the Mainboard from the Power Bay Board.
3. Initially, +5VSTDBY powers the +3.3VSTDBY D2D. (Later PWOK_ORED the logic switches the power source to non-standby 5V to reduce loading on the 5VSTDBY bus as the total current on the Standby rail can exceed the 2A maximum of the power supply.
4. The BMC requires that its +5VSTDBY supply must never be more than 4 V greater than its +3.3VSTDBY supply. For this reason, a sequencing circuit clamps the +5VSTDBY pins of the

BMC to a maximum of 3.8 V above the +3.3VSTDBY supply. This is the P5VSTDBY_SAHALEE power net.

5. +3.3VSTDBY powers the +2.5VSTDBY and the +1.5VSTDBY linear regulators.
6. Four conditions are required before the system can be awakened from the sleep state (standby power).
   - CPU #1 must be present and properly seated.
   - CPU #2 must not be installed without CPU1.
   - The PCI Riser Board must be present.
   - The Front Panel Board must be present.
   - The SCSI Board must be present.
7. The system power on begins when the system power button is pressed or on a Wake-On-LAN (WOL) event occurs. The BMC asserts BMC_PS_ON_L to the power sequencing PLD. If processor one is sensed by the PLD as present as well as the above conditions qualified through INTERLOCK_L signals, the PLD asserts the PSON_L signal going to the main power supplies, ordering them to power up +12V, -12V, +5V, and +3.3V_IN rails.
8. The power supply +3.3V_IN is blocked on the Mainboard from its +3.3V bus by a switch circuit until P3_3V_EN_L is asserted later by the power sequencing logic PLD. This is necessary due to SNC, SIOH, and LSI53C1030 requirements of having their core voltage 1.5V and 1.8V up before the IO voltage of 3.3V.
9. When power from +12V, -12V, +5V, and +3.3V_IN rails are within specification of the main power supplies, the Power Bay Board asserts PWOK_ORED to the power sequencing PLD.
10. The PLD then enables the +1.5V D2D and upon the PWOK_ORED signal and also switches the drive of +3.3VSTDBY from +5VSTDBY to +5V to prevent overloading of the +5VSTDBY supply.
11. When the +1.5V D2D asserts P1_5V_PWRGD, the PLD enables the +1.2 V and +1.8 V D2Ds.
12. When both P1_2V_PWRGD and P1_8V_PWRGD are asserted by the D2Ds, the PLD enables the processor power pods and the +1.3V.
13. Each processor that is present must assert its PPODGD signal, indicating power is ready, before the sequencing proceeds.
14. The PLD next asserts P2_5V_EN to enable the +2.5 V D2D, and P3_3V_EN_L to turn on the switch between P3_3V_IN and the +3.3 V power bus for the Mainboard and PCI Riser Board.
15. When the +2.5 V D2D and +3.3V switch asserts their power-goods, the PLD enables the +1.25 V D2D.
16. When the +1.25 V D2D asserts P1_25V_PWRGD, the PLD asserts ALLCLK_EN to enable system clocks.
17. About 200 ms later, PLD1_PWRGD_OUT_L is asserted to the BMC indicating that the power sequencing is complete.

2.2.23 Reset

There are six types of system resets supported. These resets are described in Table 2-17.

Table 2-17. Different Resets Supported

Reset Type	Description
Power-Good Reset	Occurs when the system power logic causes a power good assertion. This resets the SNC-M configuration registers and transaction states, as well as the processors.

	Whenever the system is powered on, it goes through a power good reset.
Hard Reset	A system reset caused by the assertion of RESETI_L. As a result of a hard reset, the processors, SNC-M, memory bus, and IO subsystem are reset to a known state.
Processor-Only Hard Reset	A system reset that only resets the processors. Setting the SAVCFG, SAVMEM, and SNC-M RESET command bits in the SNC-M System Reset register (SYRE) can trigger this reset.
SNC-M Local Hard Reset	This is a type of warm reset that resets only the processors, MRH-D, and North Bridge LPC-related components. Setting the SNCReset configuration bit in the SNC-M System Reset Register (SYRE) can perform this reset.
Processor Bus BINIT_L	This reset only resets the SNC-M. The reset occurs when the processor bus drives BINIT_L low. Only local memory will be accessible after BINIT_L has been driven low.
Soft Reset	This reset forces the processors to begin executing code at the boot vector. Soft resets are triggered when INIT_L is driven on the processor bus. INIT_L can be driven by either the SNC-M (when the SoftReset configuration bit is set in the System Reset Register [SYRE]) or the ICH4 (as a result of an I/O event).

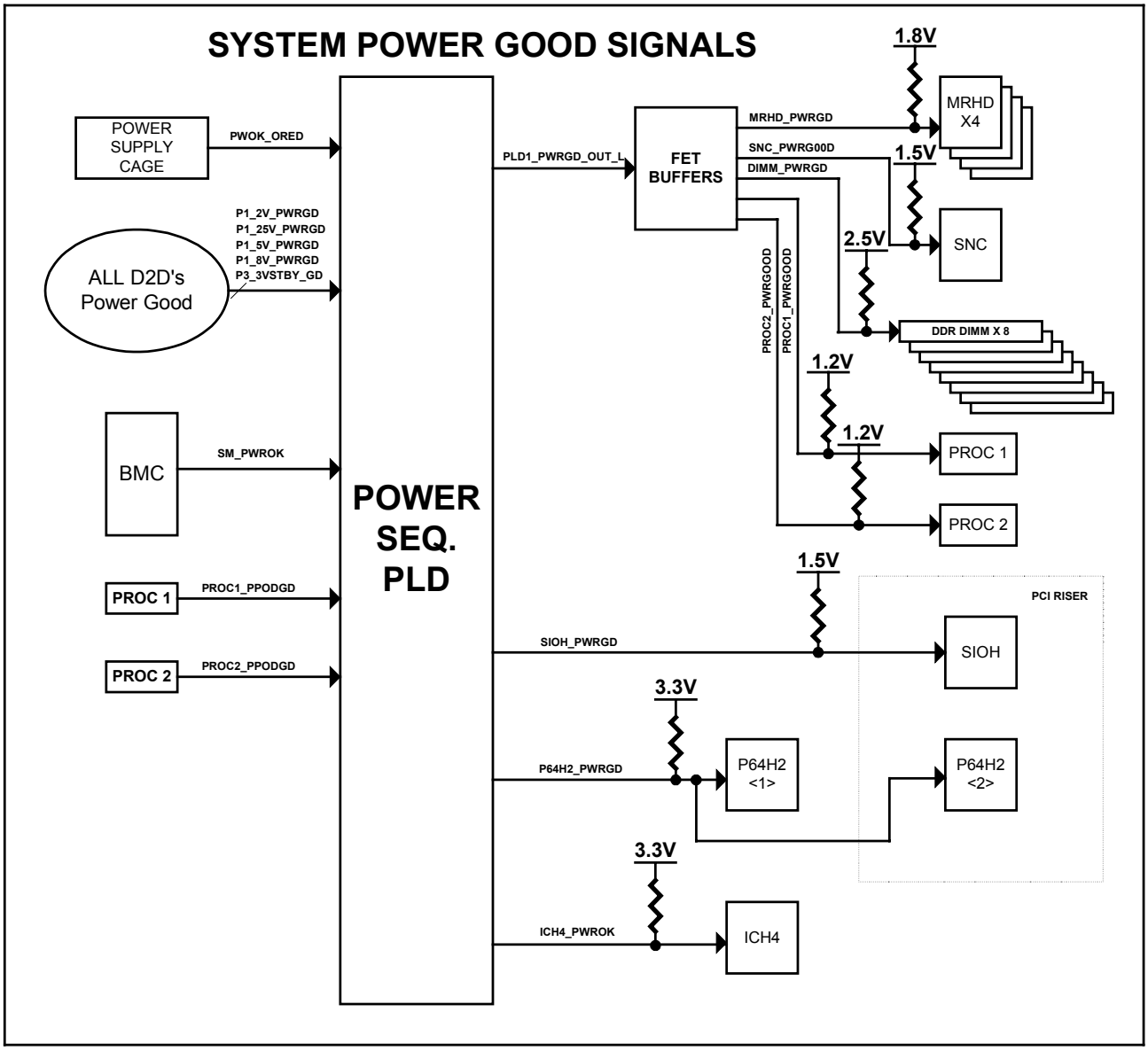


Figure 9. System Power Good

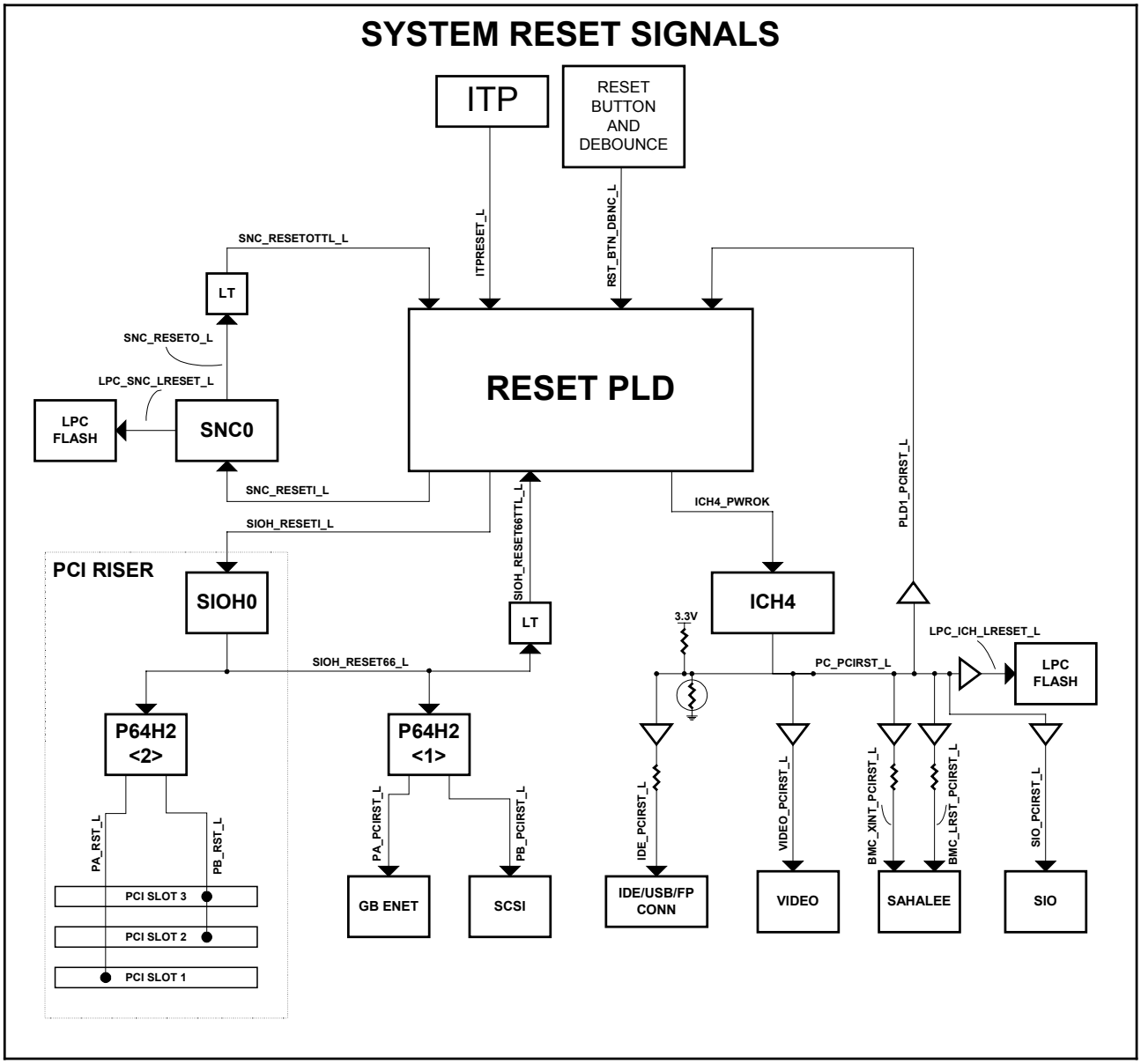
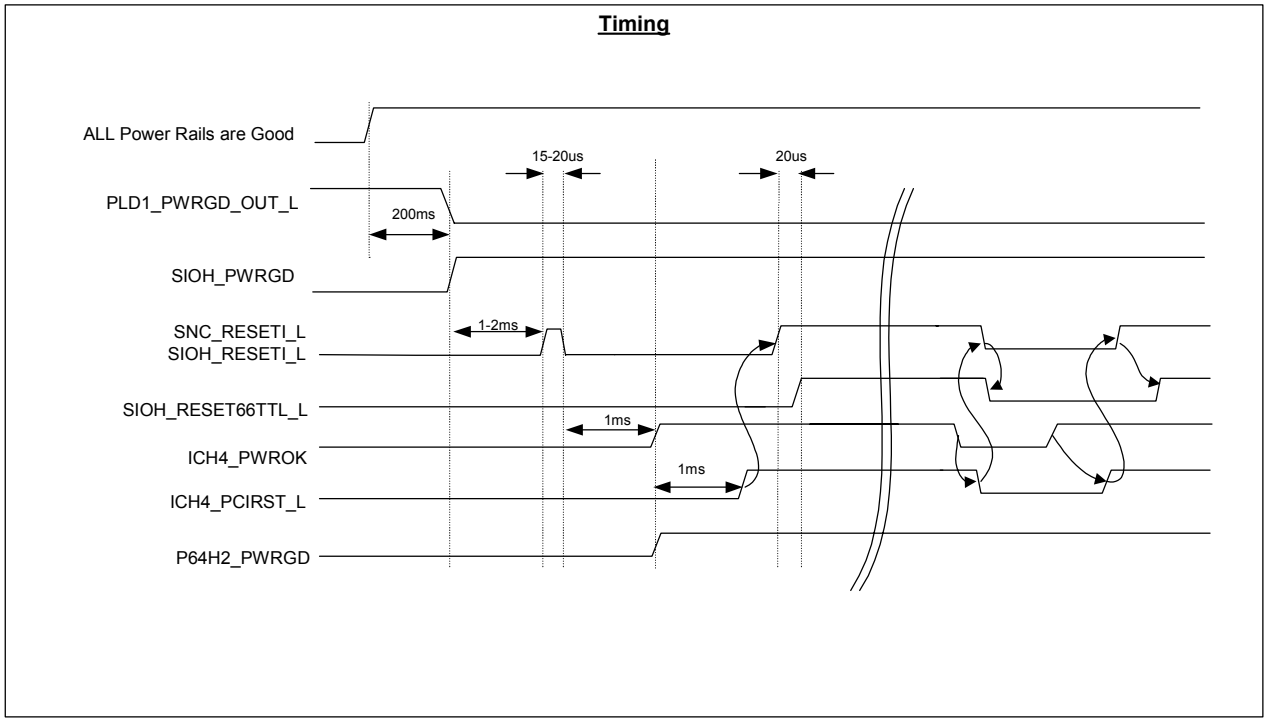


Figure 10. System Reset

Deterministic Reset Sequencer



Notes:

* All reset sources are tied to the ICH4_PWROK signal inside the PLD.
* The sources of hard reset in Tiger2: ITPRESET_L, RST_BTN_DBNC_L, SNC_RESETOTTL_L.
* Timings shown above are not to scale.

Figure 11. System Reset

NMI / SDINT(IA64)

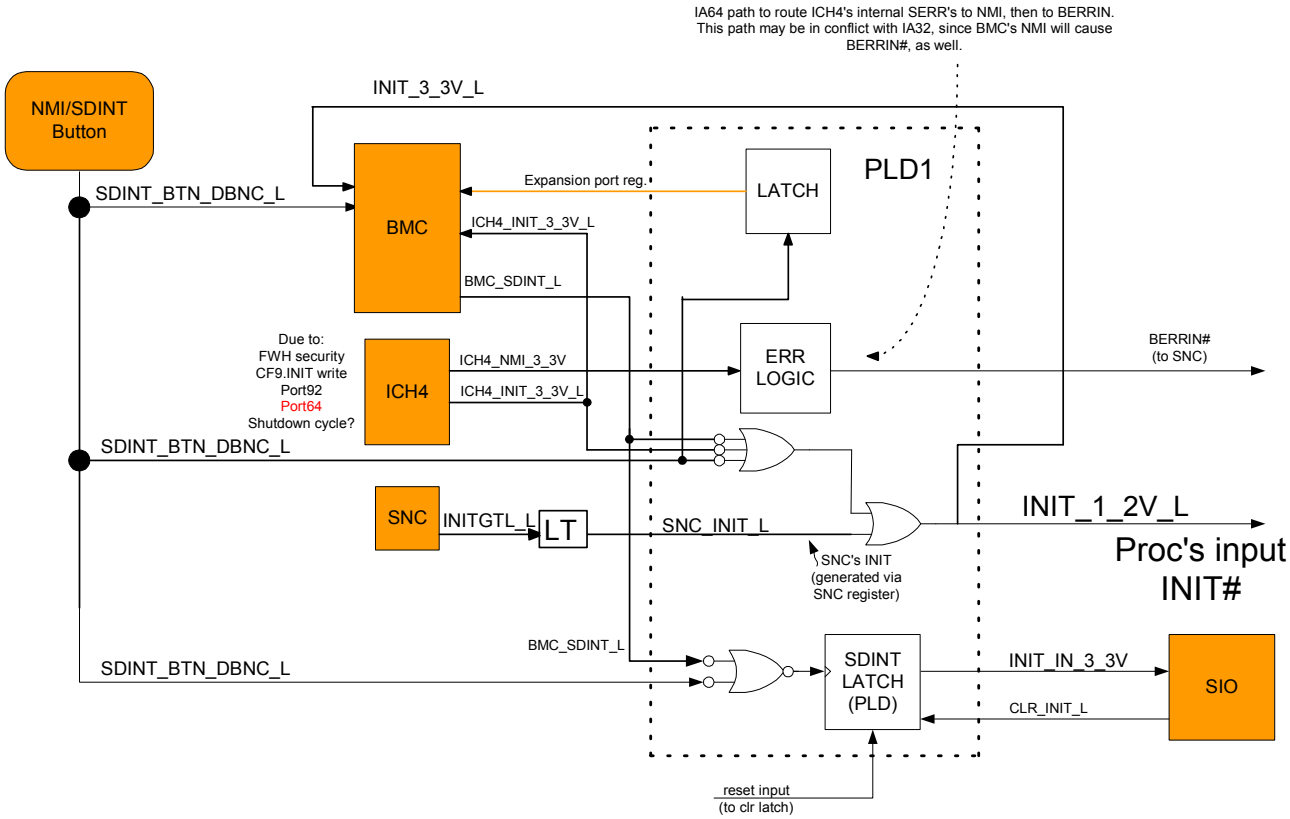


Figure 12. NMI / SDINT

PMI# (SMI#)

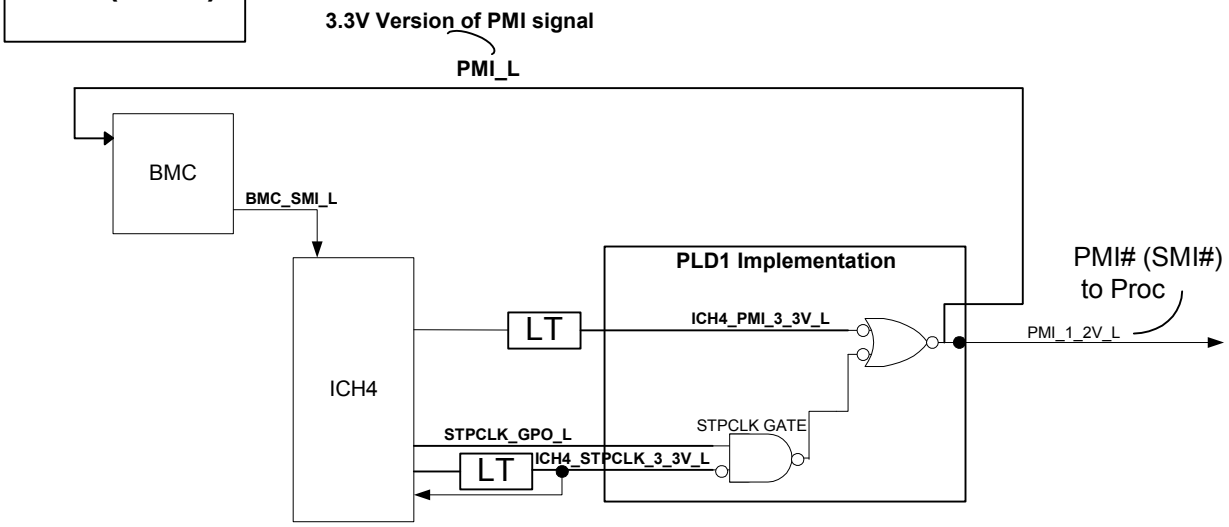


Figure 13. PMI

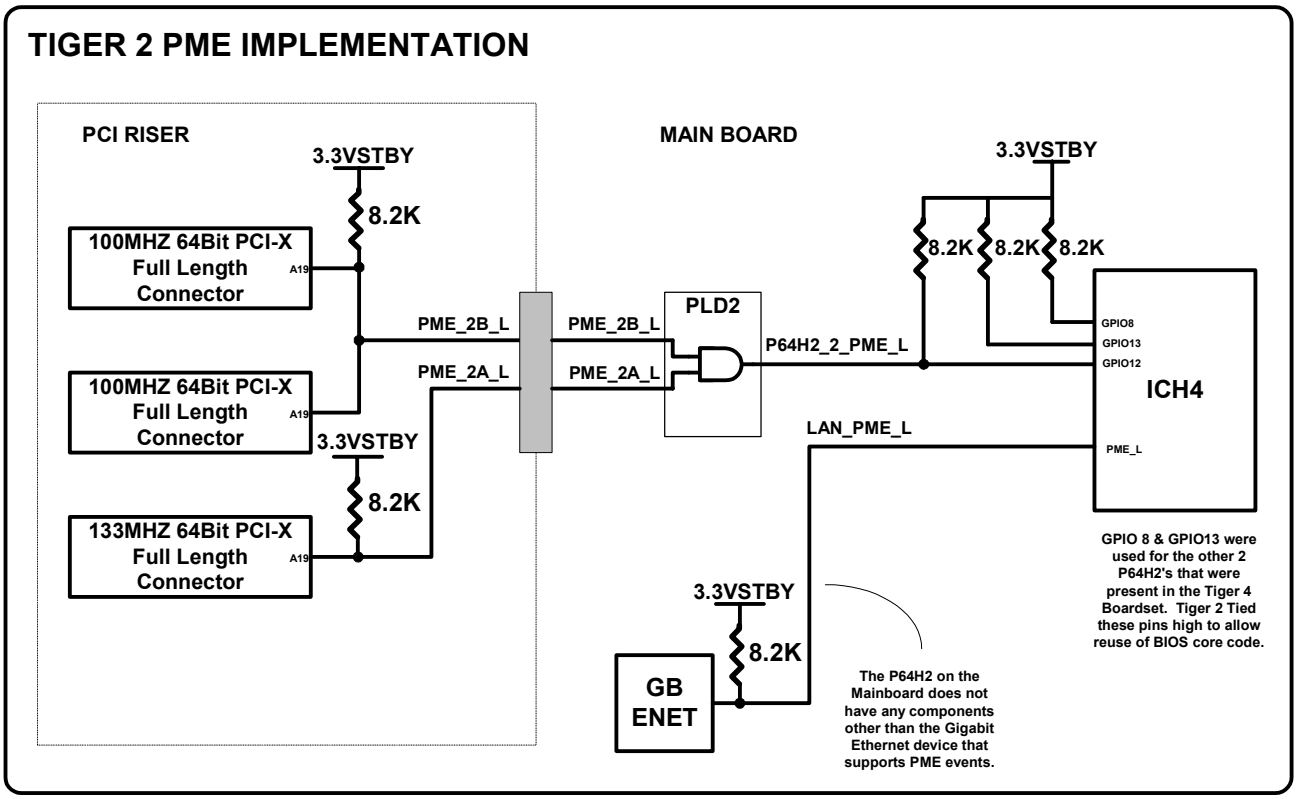


Figure 14. PME Implementation

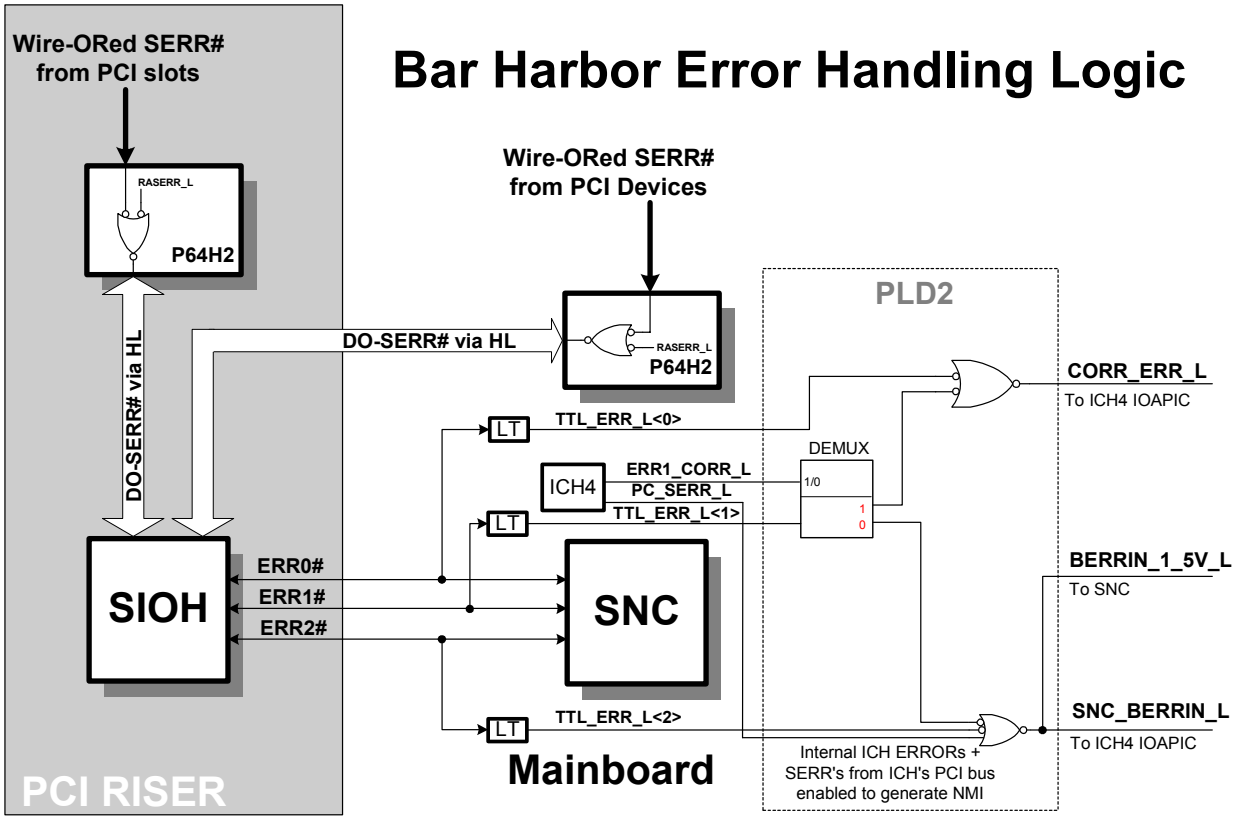


Figure 15. Error Handling Implementation

2.2.24 Configuring Baseboard Jumpers

There are four jumper blocks on the Mainboard. The primary functions of these jumper blocks are as follows:

Table 2-18. Miscellaneous Jumper Definitions

Connector	Signals	Function	Jumper Options	
J1A1	RSRL_MODE0_L	Use to set Serial Port mode J1A1 1-2 -> DSR devices J1A1 2-3 -> DCD devices (Like modem)	1-2	DSR Devices: RJ45 pin 7 to DSR, DCD = 1 (Default)
			2-3	DCD Devices: RJ45 pin 7 to DCD, DSR = 1
J1A2	RSRL_MODE1_L	NOT USED	1-2	Default
J3B1	(various)	Determines the JTAG signal chain	3-4	SNC, SIOH, PROC2, PROC1 (Default)
			5-6	
			7-8	
			1-3	SNC, SCSI, PROC2, PROC1
			5-7	
			3-5	SNC, PROC2, PROC1
			1-3	SNC, SIOH, SCSI, PROC2, PROC1
			2-4	
			5-6	
J3A3	SMM_BB_UNPROT_L	BMC Boot Block protection	1-2	Protected (Default)
			2-3	Unprotected, programmable
J5H1	RECV_BOOT_L	Reload BIOS from external	1-2	Protected (Default)
			2-3	Reload
J5H2	CLR_PASS_L	Clear password	1-2	Protected (Default)
			2-3	Clear Password
J5H3	CLR_CMOS_L	Clear CMOS memory	1-2	Protected (Default)
			2-3	Clear CMOS memory
J5H4	BMC_FRC_UPDATE_L	Place BMC in firmware update mode	1-2	Protected (Default)
			2-3	Update mode
J6G2	FWH20_ID1_SWAP_L	Swaps North Bridge FWH ID0 and ID2	1-2	Normal (Default)
			2-3	Swap ID0 with ID2

Note:

J3A3 must be set from 1-2 to 2-3, unprotected, for the PLD Update Utility to update PLD2 on the Mainboard and PLD3 on the SCSI board. This is an intended security feature.

Server Management Block

The figure below shows the system management logic for the SR870BH2 System. The Mainboard has six system management buses connecting all server management devices as well as the 870-chipset components, memory, and the two Itanium 2 processors. These buses are used to gather different types of information (such as voltage, temperature, and device info) from the various devices and are accessed through the Baseboard Management Controller (BMC) via server management software such as Intel® Server Controls (ISC). See BMC section for more information specific to the BMC. For more information see the SR870BH2 Server Management EAS.

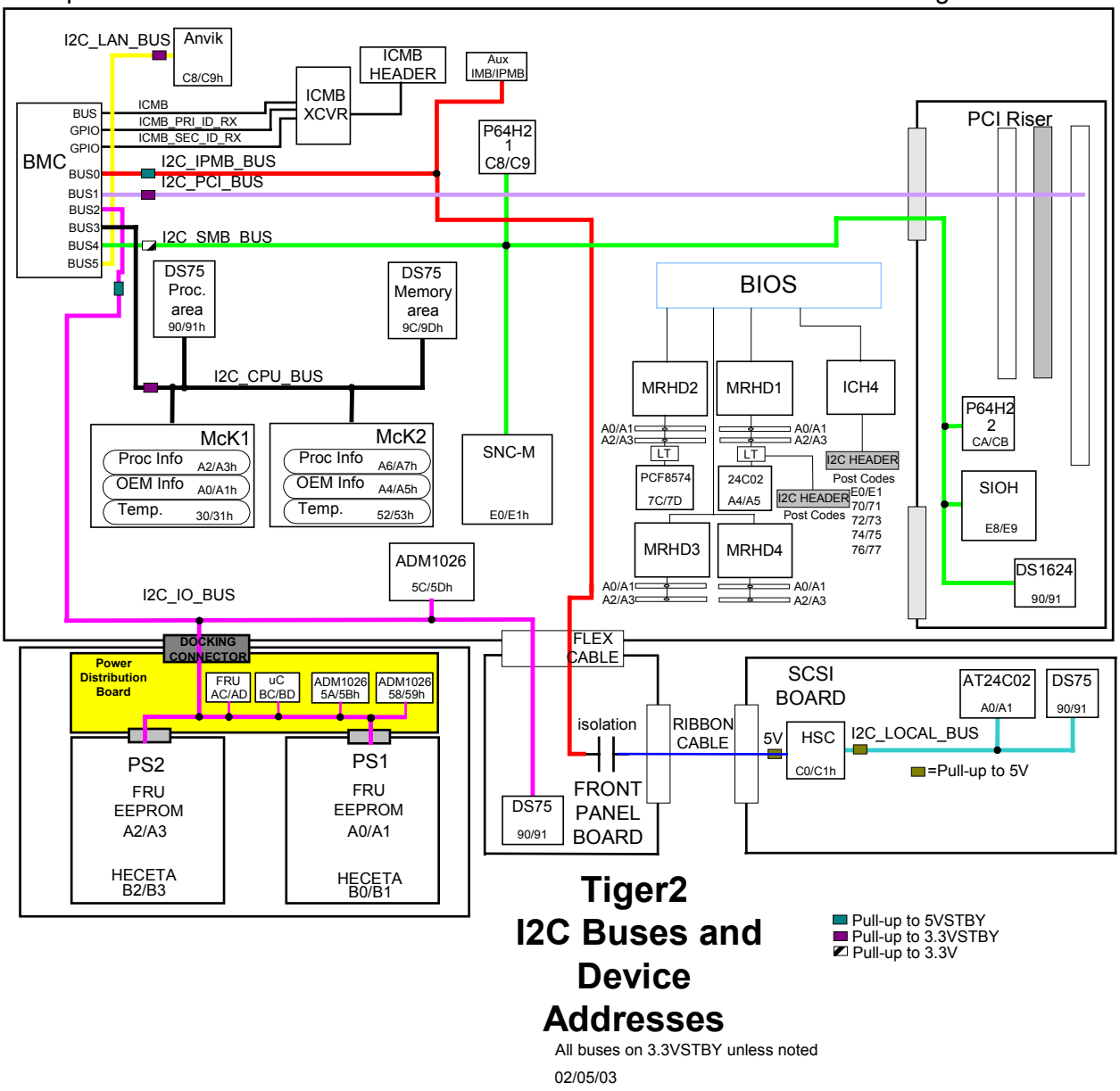


Figure 16. Server Management Diagram

2.2.25 I²C* Address Map

Table 2-19. Device list on System I²C Buses*

Board	Device	Function	BMC I²C Bus	I²C Address	Supply Voltage
Main	IMB/IPMB Header	IMB/IPMB external access	Bus 0, IPMB	Not determined	+5 V Standby
SCSI	GEM359	SCSI Hot-Swap Controller	Bus 0, IPMB	C0/C1h	+5 V
PCI Riser	PCI connectors	Not determined	Bus 1, PCI	Not determined	+3.3V
Power Bay	ADM1026	Voltage monitor and General Purpose IO	Bus 2, IO	58/59h	+5 V Standby
Power Bay	ADM1026	Voltage monitor and General Purpose IO	Bus 2, IO	5A/5Bh	+5 V Standby
Main	ADM1026	Voltage monitor and General Purpose IO	Bus 2, IO	5C/5Dh	+5 V Standby
Front Panel	DS75	Temperature (Front Panel)	Bus 2, IO	90/91h	+5 V Standby
Power Bay	FRU	Power Bay Board Identity	Bus 2, IO	AC/ADh	+5 V Standby
Power Bay	PS1-FRU	PS1 Module Identity	Bus 2, IO	A0/A1h	+5 V Standby
Power Bay	PS1-HECETA	Function Monitor	Bus 2, IO	B0/B1h	+5 V Standby
Power Bay	PS2-FRU	PS2 Module Identity	Bus 2, IO	A2/A3h	+5 V Standby
Power Bay	PS2-HECETA	Function Monitor	Bus 2, IO	B2/B3h	+5 V Standby
Power Bay	Microcontroller	Power Supply Control	Bus 2, IO	BC/BDh	+5 V Standby
Main	Proc1 Socket	Processor 1 Proc Info	Bus 3, CPU	A2/A3h	+3.3 V Standby
Main	Proc1 Socket	Processor 1 OEM Info	Bus 3, CPU	A0/A1h	+3.3 V Standby
Main	Proc1 Socket	Processor 1 Temperature	Bus 3, CPU	30/31h	+3.3 V Standby
Main	Proc2 Socket	Processor 2 Proc Info	Bus 3, CPU	A6/A7h	+3.3 V Standby
Main	Proc2 Socket	Processor 2 OEM Info	Bus 3, CPU	A4/A5h	+3.3 V Standby
Main	Proc2 Socket	Processor 2 Temperature	Bus 3, CPU	52/53h	+3.3 V Standby
Main	DS75	Temperature (Proc area)	Bus 3, CPU	90/91h	+3.3 V Standby
Main	DS75	Temperature (Memory area)	Bus 3, CPU	9C/9Dh	+3.3 V Standby
Main	SNC-M	Scalable Node Controller	Bus 4, SMB	E0/E1h	+3.3V
Main	P64H2	PCI Bridge	Bus 4, SMB	C8/C9h	+3.3V
PCI Riser	P64H2	PCI Bridge	Bus 4, SMB	CA/CBh	+3.3V
PCI Riser	SIOH	System I/O Hub	Bus 4, SMB	E8/D9h	+3.3V
PCI Riser	DS1624	FRU Info & Temperature	Bus 4, SMB	90/91h	+3.3V
Main	82546EB	GbENET Controller	Bus 5, LAN	C8/C9h	+3.3 V Standby

Note: 1. The SNC-M SMBus device ID is set through NODEID[3:0].

2.2.26 DS75 Temperature Sensor and FRU Information

The DS75, when accessed via the I²C bus, will provide the temperature of the at that location on the Mainboard. The temperature data is a 9-bit value, which gives a range of –55C to +125C in 0.5C increments. There are two DS75 on the SR870BH2 Mainboard, one located by the SM120-Pin connector for pre-heat air and the second by the 1.5V converter for Memory/Vreg/PCI temperature.

2.2.27 ADM1026* Hardware Monitor and FRU

The ADM1026* is a system hardware monitor providing voltage and temperature measurement and limit comparison of various system parameters. There are 13 voltage-sensing inputs, two pairs of temperature-sensing diode inputs, and ten digital signal inputs that are monitored using the ADM1026*. *Table 2-22* shows the voltage sensors, temperature sensors, and data signals configured with the ADM1026. The ADM1026 holds the Mainboard FRU information in its 8 kbytes on-chip E²PROM. The ADM1026 resides on the BMC's I2C_IO bus.

Table 2-20. ADM1026 EEPROM Programming Areas

Area	Size	Description
Common Header	8 bytes	Programming offsets to the other areas below.
Internal Use	48 bytes	This area is reserved for general-purpose use by the Intel® Server Management Firmware/Controllers.
Board Info	80 bytes	Contains the board FRU information listed in Table 1-15.
Product Info	120 bytes	Available for OEM use. †

† The Intel-provided FRU and SDR load utility allows OEMs to program any of the FRU SEEPROM on the SR870BH2 board set. Refer to *FRU & SDR Load Utility EPS* for more details.

Table 2-21. Example of Subset of FRU Information

Information	Description	Example	Notes
Mfg. Date/Time	Time and date of board manufacture (value programmed (in hex) is the number of minutes after 0:00 hrs 1/1/96	01ff593h (Date and time translation shown below) f593 = 2094483 min = 3 yr 358 Days & 1116 min = Dec 23, 1999, 6:36 pm	2
Manufacturer	Board Manufacturer	Intel	1
Board Product Name	Board Name/Description	SR870BH2 Mainboard	2
Board Serial Number	Intel® Board Serial Number	INBR42385906	2
Board Part Number	Intel Board Part Number	A67194-320	2

Notes: 1. Actual Value programmed into the board
2. Example value. Actual value to be determined at the time the board is manufactured.

*Table 2-22. Signals Monitored by the ADM1026**

Signal	I^2C* Interface	Comments/Description
+3.3V	Input	Voltage monitor
+5V	Input	Voltage monitor
-12V	Input	Voltage monitor
+12V	Input	Voltage monitor
+1.8V	Input	Voltage sensor
+1.5V	Input	Voltage sensor
+1.25V	Input	Voltage sensor
SNC_TDIOCATHODE	Input	Voltage sensor for SNC-M temperature-sensing diode
SNC_TDIOANODE	Input	Voltage sensor for SNC-M temperature-sensing diode
TDIO_CATHODE	Input	Voltage sensor for SIOH temperature-sensing diode
TDIO_ANODE	Input	Voltage sensor for SIOH temperature-sensing diode
SCSI_A_VREF0	Input	Voltage sensor
SCSI_A_VREF1	Input	Voltage sensor
SCSI_A_VREF2	Input	Voltage sensor
SCSI_B_VREF0	Input	Voltage sensor
SCSI_B_VREF1	Input	Voltage sensor

Signal	I^2C* Interface	Comments/Description
SCSI_B_VREF2	Input	Voltage sensor
THERMTRIP1_L	Input	Processor 1 Thermal Trip
THERMTRIP2_L	Input	Processor 2 Thermal Trip
SCSIA_SE	Input	SCSI mode single-ended
SM_PROC1_PPODOE	Output	Proc1 Power Pod Enable
SM_PROC2_PPODOE	Output	Proc2 Power Pod Enable
PROC1_PPODGD	Input	Proc 1 Power Pod Good
PROC2_PPODGD	Input	Proc 2 Power Pod Good
PROC1_PRES_L	Input	Proc 1 Power Pod Present
PROC2_PRES_L	Input	Proc 2 Power Pod Present
INTRUSION_L	Input	Chassis intrusion

2.2.28 Chassis Intrusion

The 120-pin flex cable connector J5J2 and two-pin connector J1A8 provide connection to two parallel, normally-open intrusion switches yielding the signal INTRUSION_L. A switch closure for this signal is differentiated through an RC connection to remove DC drain on the battery, and the isolated side of the RC network is pulled up to battery, VCC_RTC. This signal is buffered to the ADM1026 where it may be state detected, and to the ICH4 intruder pin.

2.2.29 ID Button and LED

The ID button S5A1 is connected in parallel with the Front Panel ID pushbutton. The ID LED is controlled by PLD1 and may be activated by the BMC. The LED is disconnected by plugging a connector into the integral jack.

2.2.30 Intel® 870 Chipset I^2C* Interface

The SNC-M component of the Intel® 870 set includes an I^2C slave port to accept commands from a server management controller. This I^2C slave port interfaces with the SNC-M configuration unit, which gives a server management controller visibility into all configuration registers in the chip set.

2.2.31 Itanium 2 Processor Server Management Features

The Itanium 2 processor cartridge includes a system management bus interface, which allows access to several processor features. The system management components on the cartridge include two memory components (EEPROM's) and a thermal sensing device (digital thermometer). The processor information EEPROM provides information about the processor cartridge. This information is permanently write-protected. The other EEPROM is a scratch EEPROM that is available for other data at the system vendor's discretion.

The thermal sensing device is connected to the on-die thermal diode. TH_TRIP_L is a signal that is asserted when processor thermal failure has occurred.

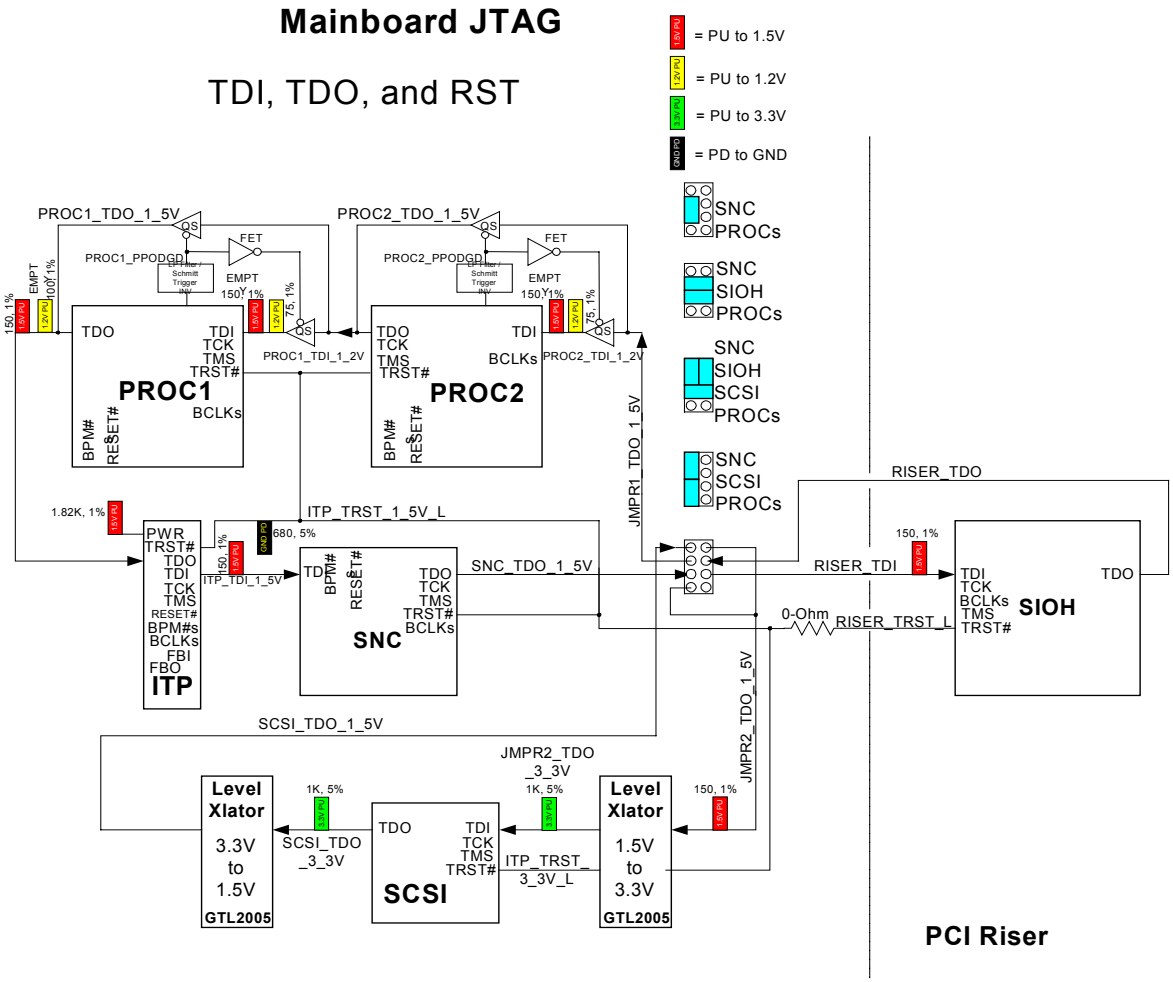
For more information, please refer to the *Itanium 2 Electrical, Mechanical and Thermal Specification (EMTS)*.

2.2.32 Debug Port/In-Target Probe (ITP)

This ITP port provides an interface for system and component level debug. During system test and debug, all events and commands use the JTAG (Joint Test Action Group) protocol to access registers and memory.

In system debug, this port is controlled by the ITP, which is a PCI card driven by an application running on a PC. JTAG runs asynchronous to the system clocks at no more than 1/12.5 of the bus clock frequency or 16 MHz.

Figure 17. Implementation of JTAG, 1 of 4



Mainboard JTAG

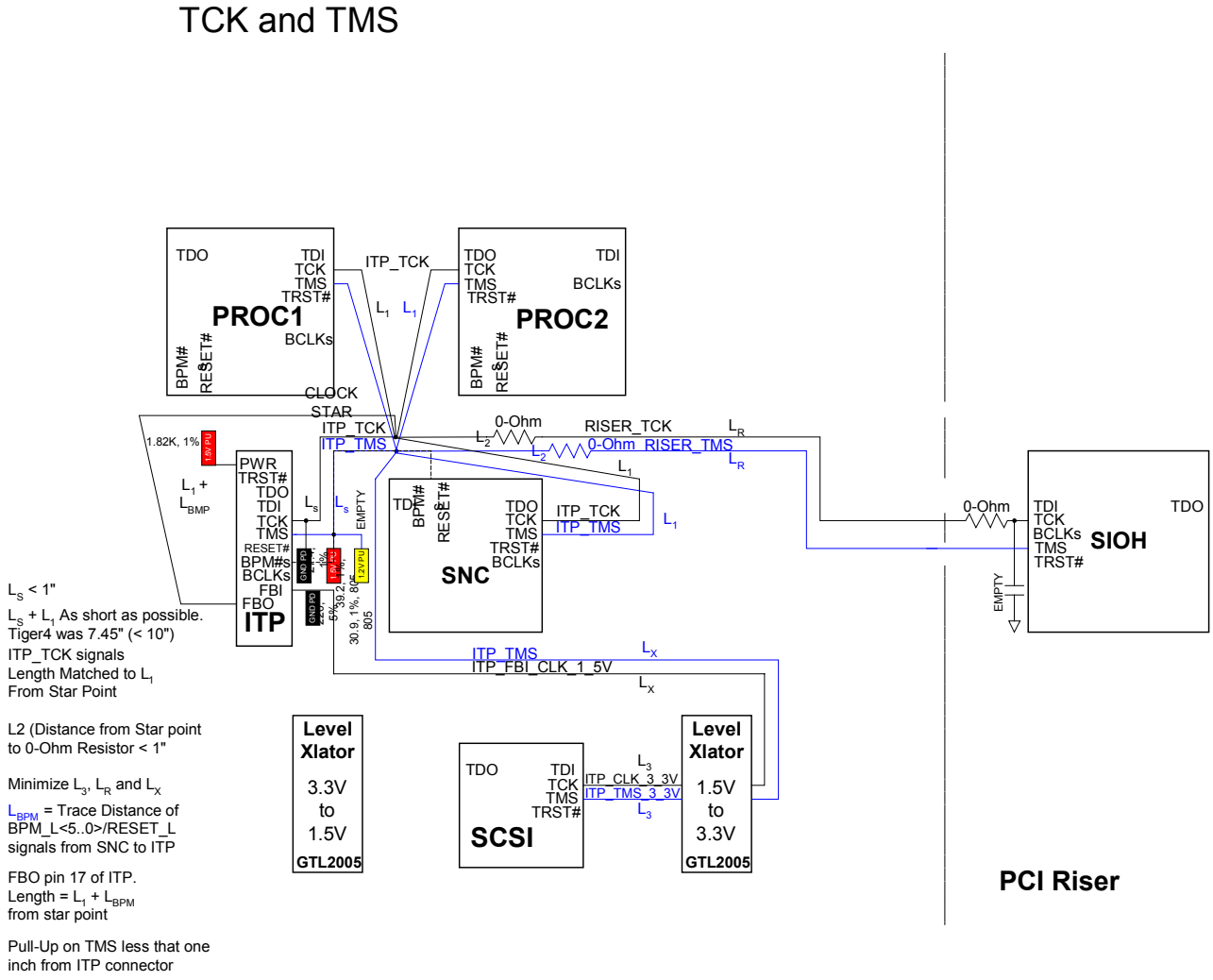


Figure 18. Implementation of JTAG, 2 of 4

Mainboard JTAG

200MHz Clocks

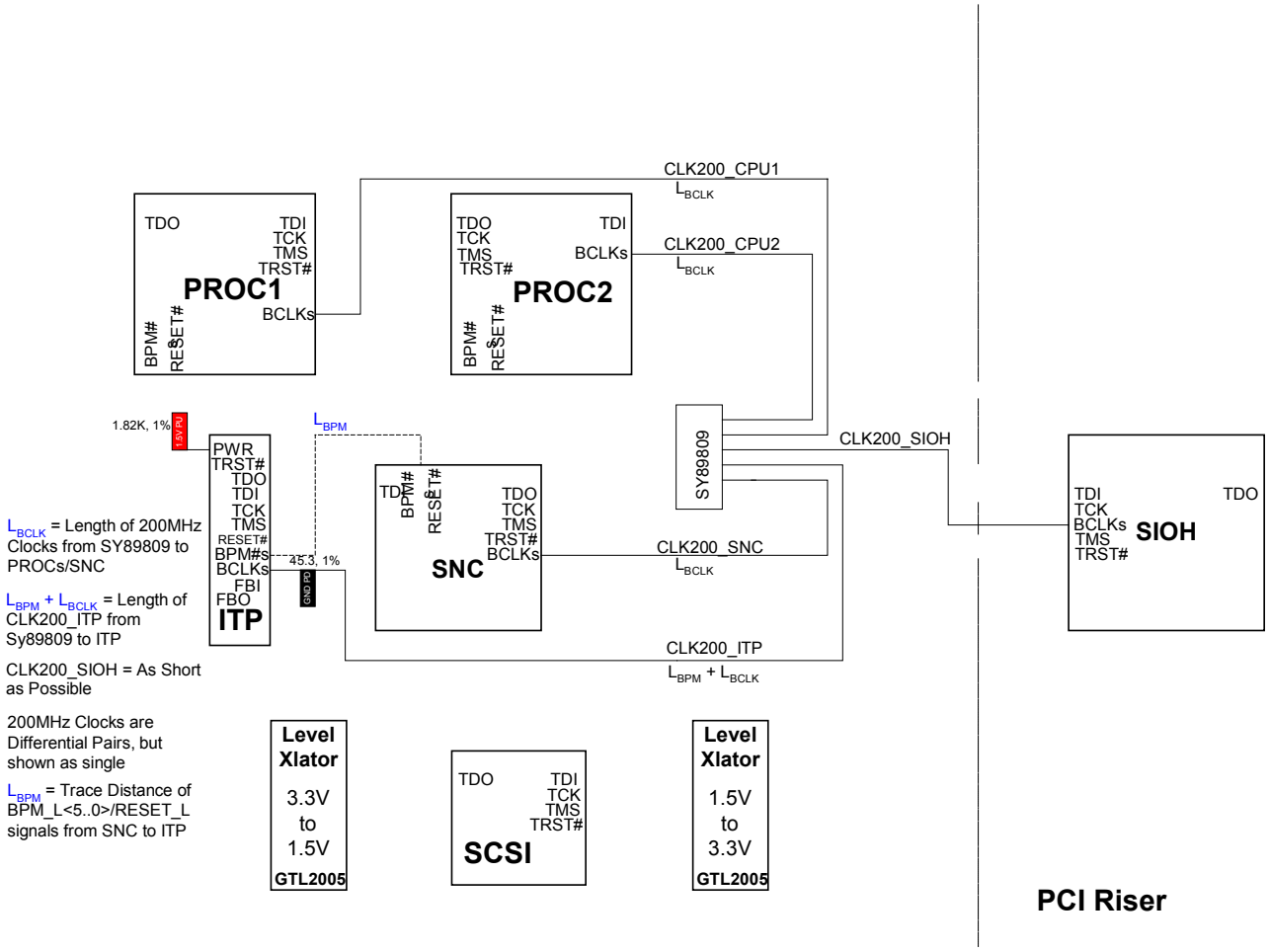
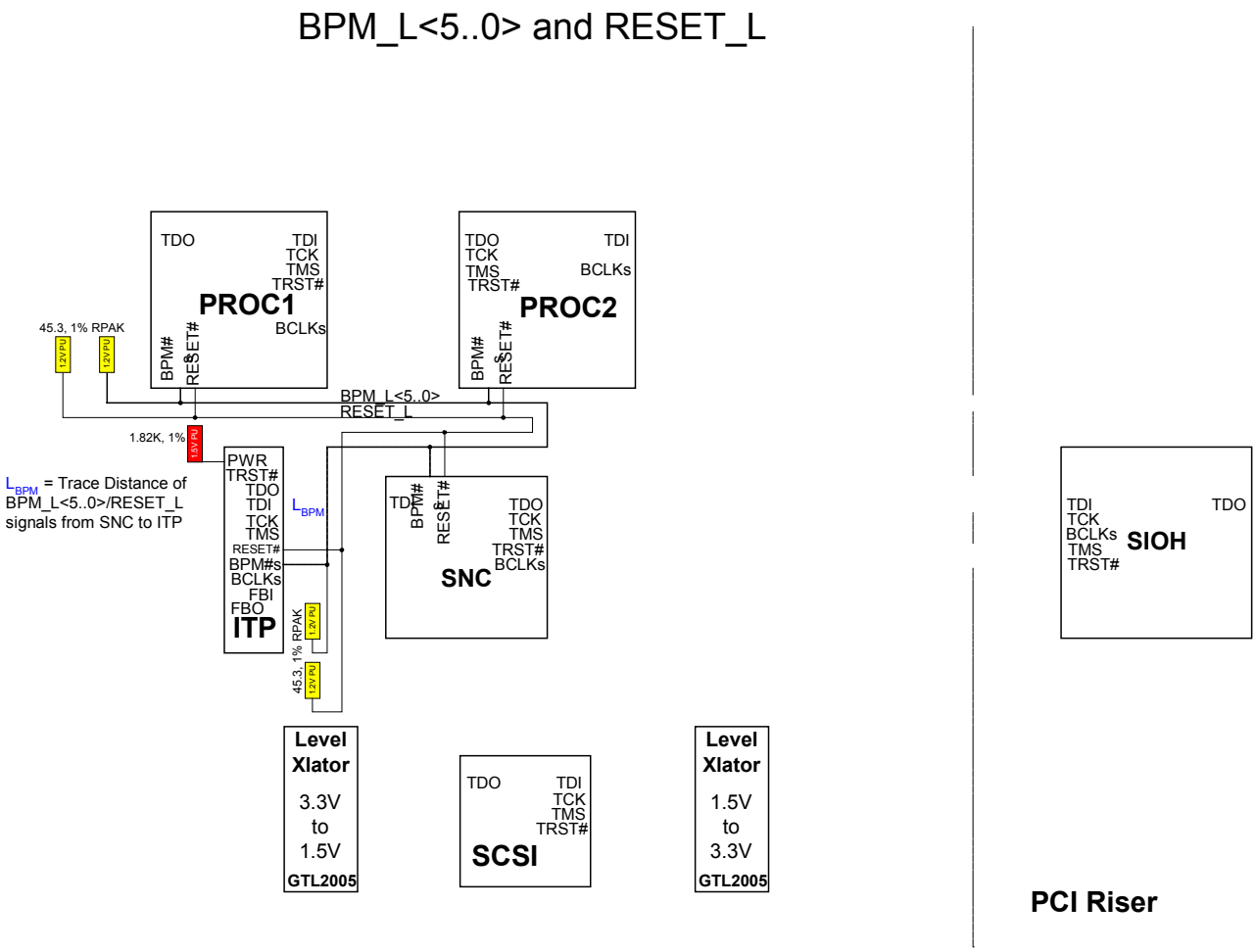


Figure 19. Implementation of JTAG, 3 of 4

Mainboard JTAG



2.2.33 ISP Interface

The ISP interface allows programming of the system Programmable Logic Devices (PLD). Through the 1x8 header on the on the Mainboard all three system PLDs are accessable. If the Flex cable is not installed, the PLD chain will be downsizes

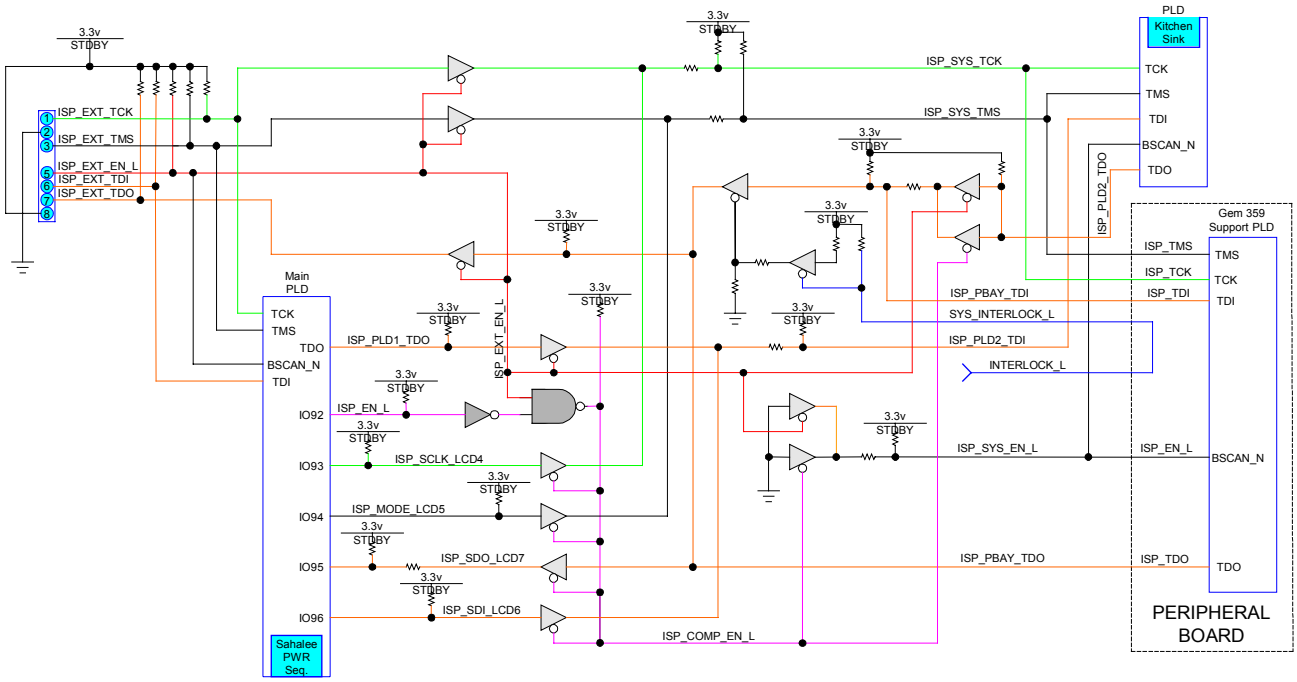


Figure 20. ISP Programming Diagram

2.2.34 Power Connection

The Mainboard receives power through the Power Bay Docking Connector (J3J1). The connector also carries power control and the I^{2}C IO server management bus. Table 3.1 describes the connector signals.

Table 2-23. Mainboard Power Connection (J3J1)

Signal	Current	Pin #	# of Pins
+12V	36 A	P1A1 - P1D2	1 blade
+5V	36A	P2A1 - P2D2	1 blade
P3_3V_IN	36A	P2A1 - P2D2	1 blade
GND	70 A	P4A1 - P4D2, P5A1 - P5D2, P6A1 - P6D2, B2, D2	3 blades & 2 pins
+5VSTDBY	2 A	A3, B3	2 pins
-12V	1 A	A1	1 pin
P5V_SENSE	1 A	B1	1 pin
P3_3V_SENSE	1 A	C1	1 pin
SENSE_RTN	1 A	C2	1 pin
I2C_IO_SCL	1 A	A2	1 pin
I2C_IO_SDA	1 A	C3	1 pin
PSON_L	1 A	D1	1 pin
BUF_PWOK_ORED	1 A	D3	1 pin

2.2.35 Itanium 2 Processor Socket Pin-out

A detailed description of the Itanium 2 processor signals and their pin-outs are described in the Itanium 2 *EMTS*.

2.2.36 Mechanical Specifications

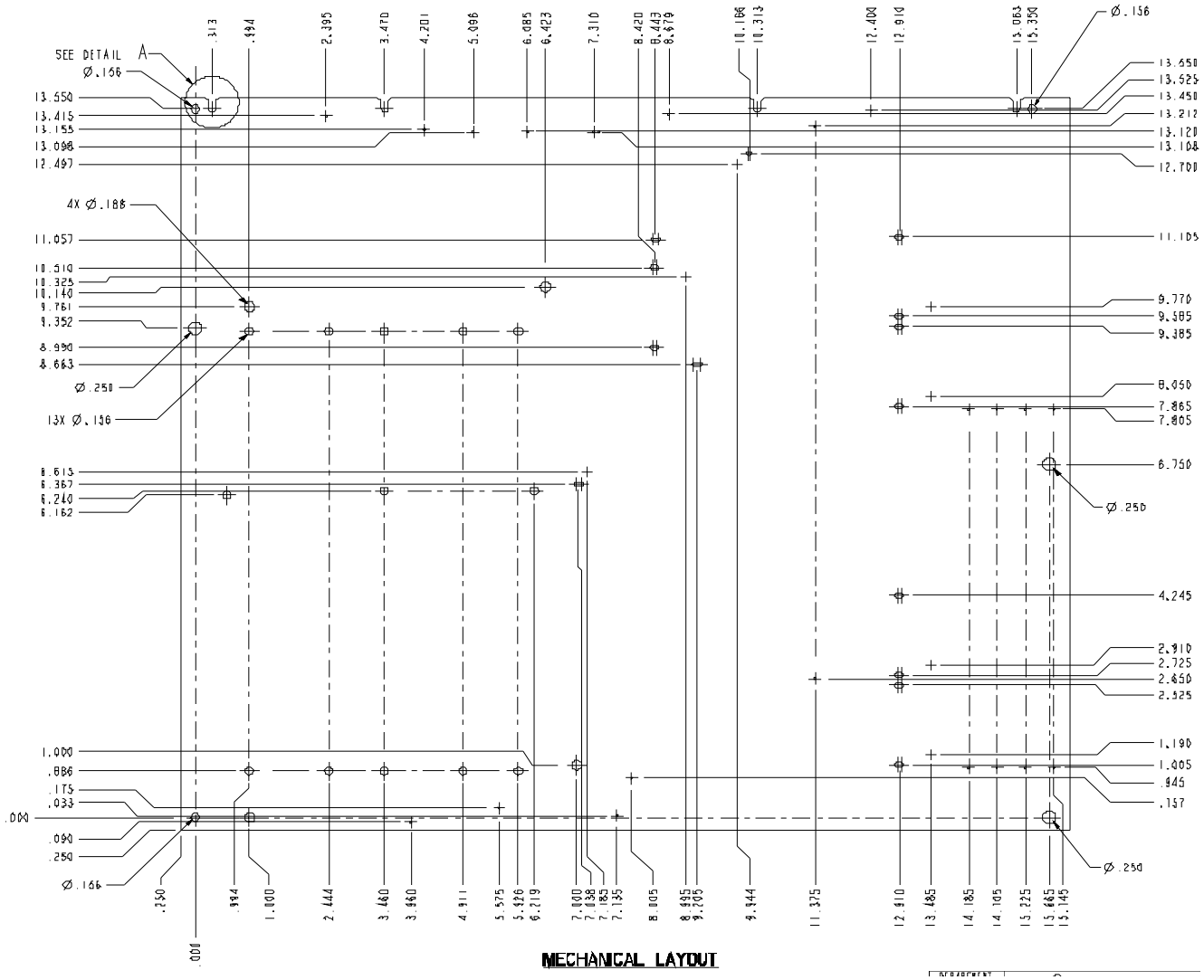


Figure 21. Mechanical Layout

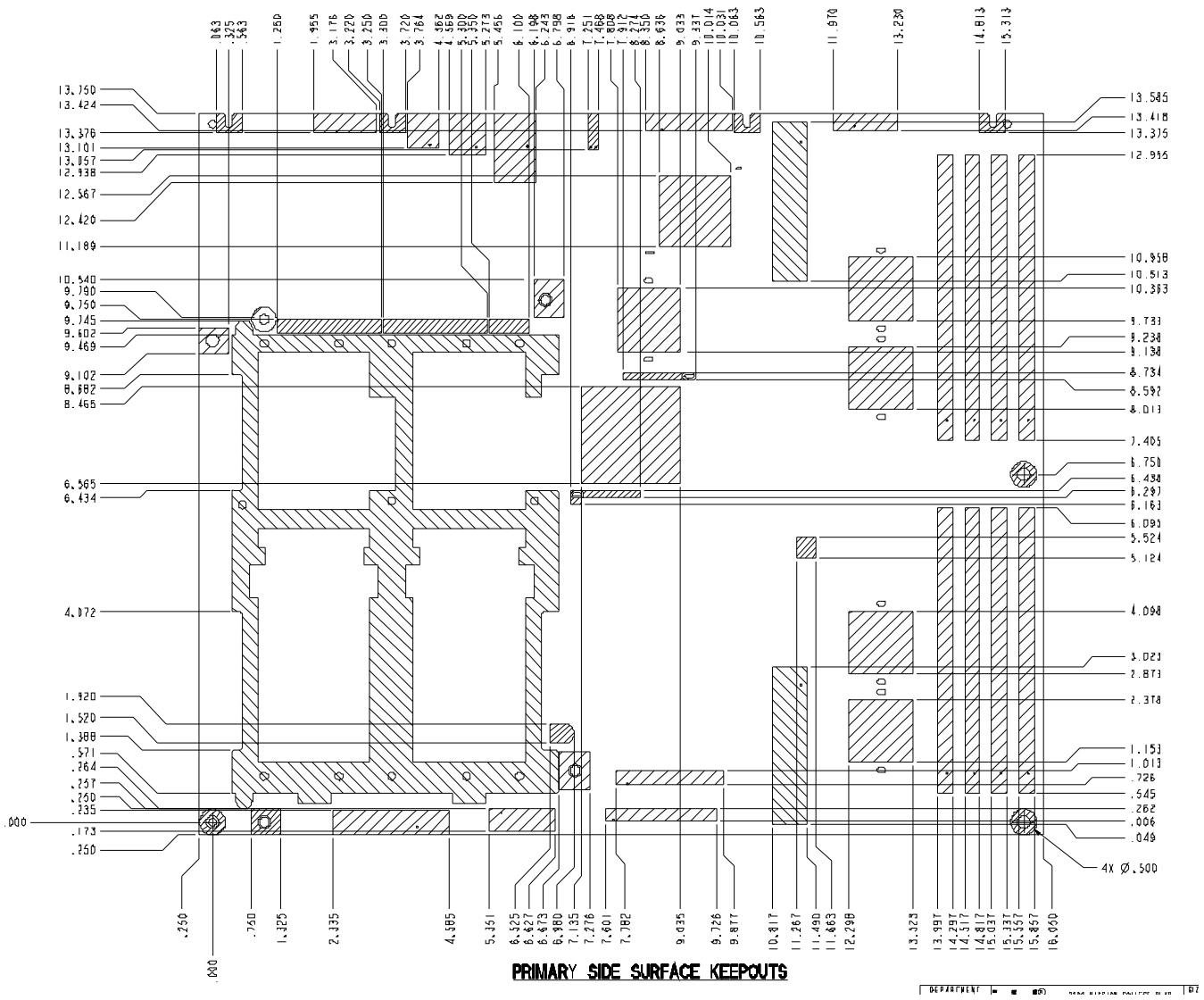


Figure 22. Primary Side Surface Keep-outs

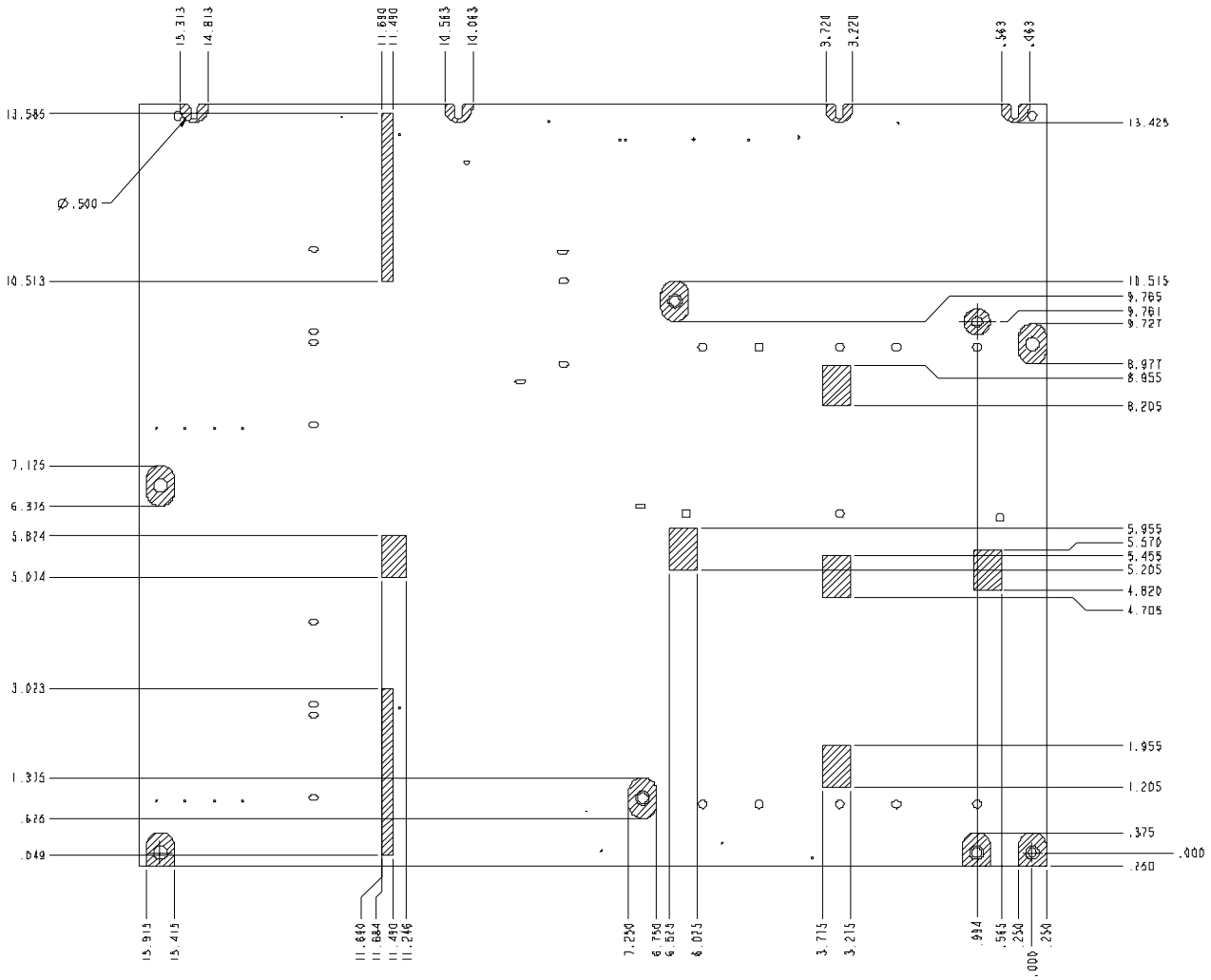


Figure 23. Secondary Side Surface Keep-outs

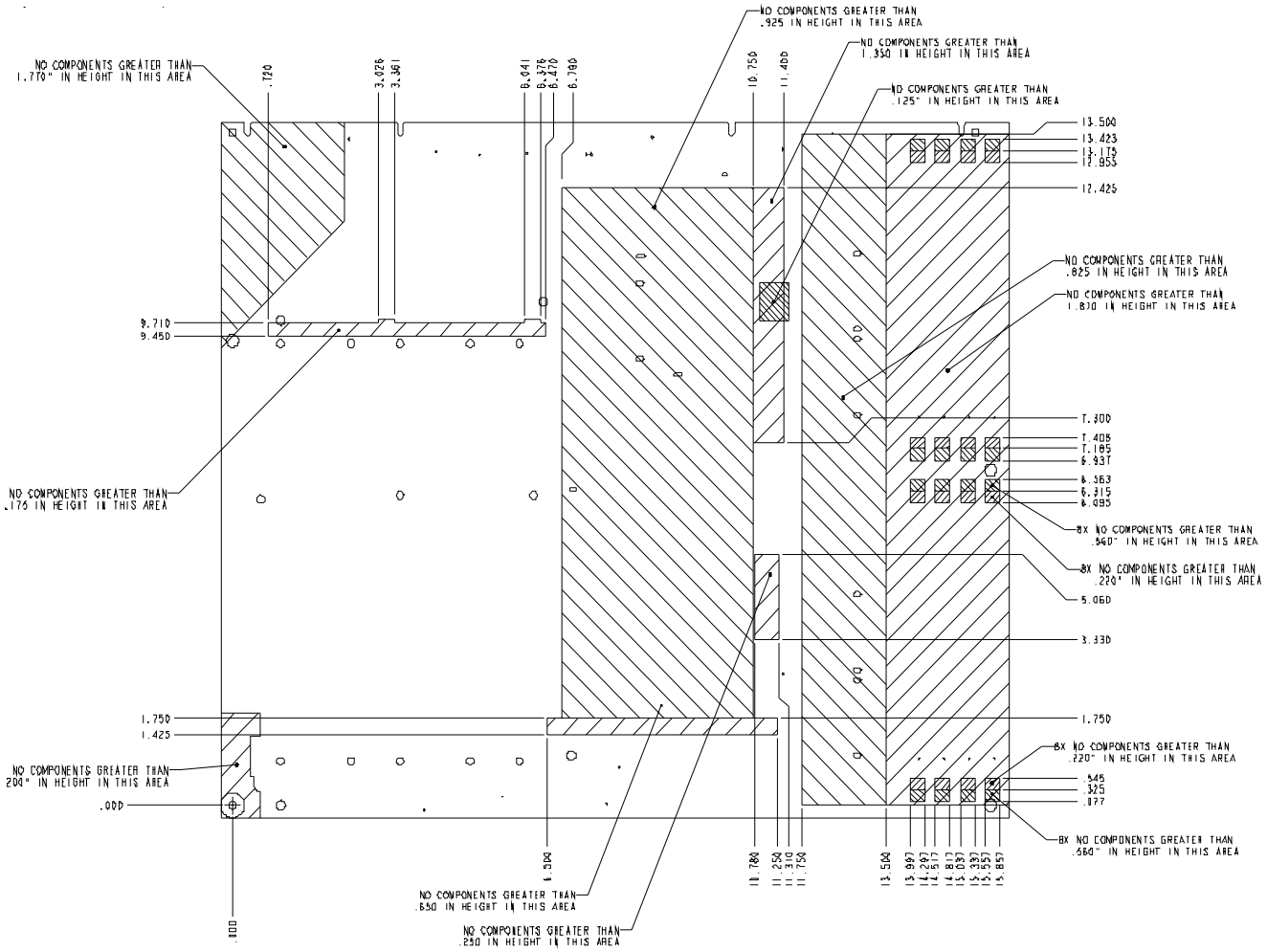


Figure 24. Primary Side 3D Keep-outs

2.2.37 Processor Retention Mechanism

The processor retention mechanism is shown in below. There is one used for the Mainboard to support the two processors on the primary side. The primary purpose for the retention mechanism is to provide a secure base to fasten the processor and power pod assembly to the processor board.

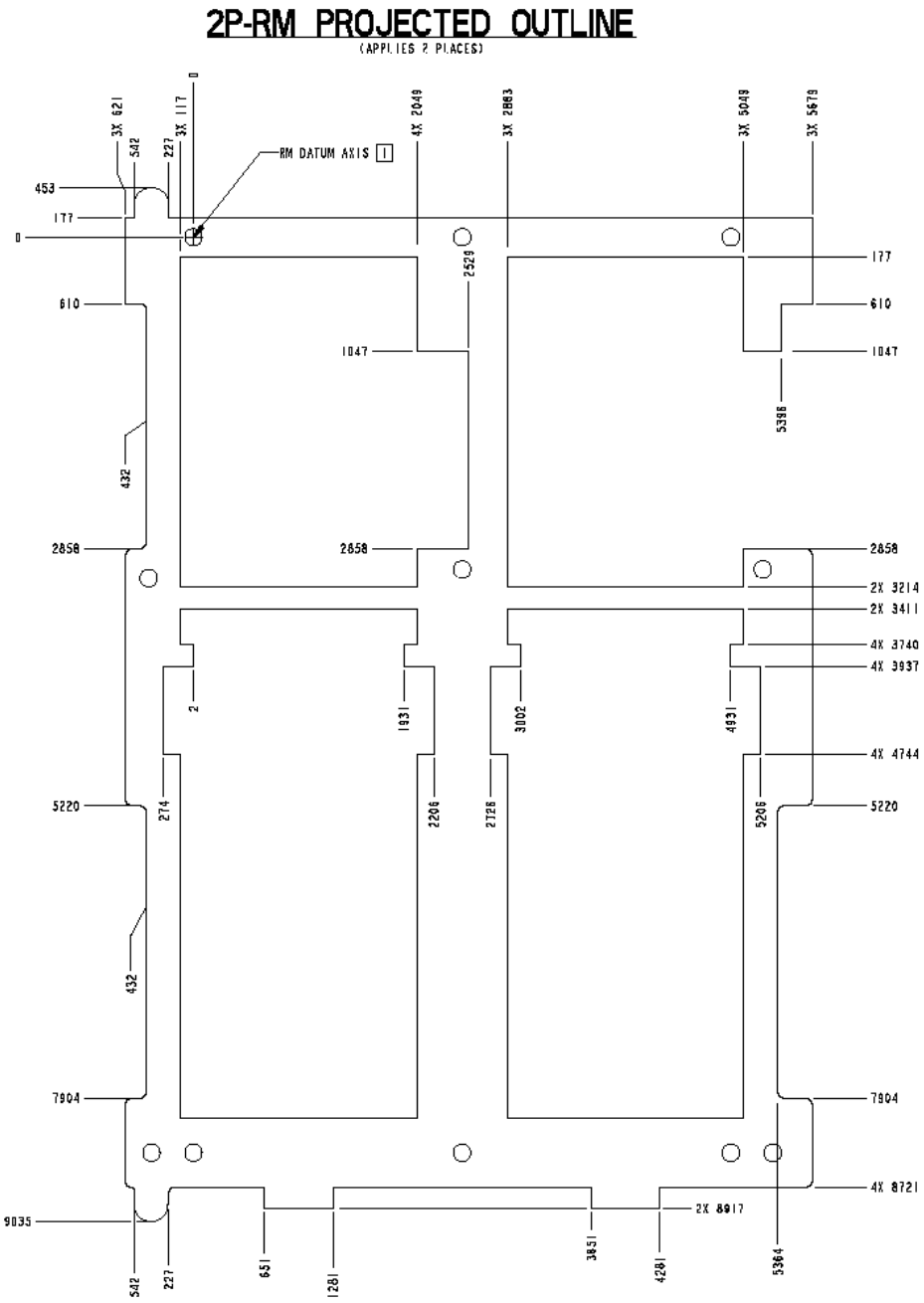


Figure 25. Processor Retention Mechanism

2.2.38 Thermal Requirements

Components requiring forced convection cooling are shown in the table below. Refer to the listed reference documents for specific temperature and airflow requirements. The Processor enabled heat sinks require tightly ducted, dedicated flow to meet thermal requirements. Careful attention to specifications and reference documents will ensure that cooling requirements for these components can be met. Maximum board operating temperatures are dependent on system layout and airflow. Board components not listed in the table will be adequately cooled if the cooling requirements for

the listed components are met. For more information please see the System Integration System EPS.

Table 2-24. Critical Mainboard Components

Component	Airflow (lfm)	Air Temp °C	Heat Sink Required
Mainboard	200	50	N/A
Processor			Yes
Power Pod			Yes
SNC-M	200	50	Yes
P64H2	200	50	Yes
SCSI	200	50	Yes
MRH-D	200	50	Yes
ICH4	200	50	No
DIMM'S	200	50	N/A

2.2.39 Quality and Reliability Target

The quality and reliability targets are outlined in the *25-GS3000 Specification* and *Environmental Standards Handbook (Intel document# 662394-05).*

Quality goals outlined for the Mainboard are:

1. Intel Board Factory Line fall out maximum 3000 DPM
2. Board-level VCLF (Verified Customer Line Fallout) < 5000 DPM at FLQ (Full Qual Level)

Reliability goals outlined for the Mainboard are:

1. Board MTBF (Mean Time Between Failure) goal > 250,000 hours at 35°C operating temperature.

Appendix A: Glossary

This appendix contains important acronyms and terms used in the preceding chapters.

Term	Description
A, Amp	Ampere
AGTL+	assisted gunning transceiver logic+
BMC	baseboard management controller
C	Centigrade
CMOS	complementary metal-oxide semiconductor
CPU	Central processing unit
D2D	DC-to-DC
DDR	Double data rate
DIMM	dual inline memory module
DMA	direct memory access
DRAM	dynamic random access memory
ECC	error correcting code
EDS	external design specification
EMTS	electrical, mechanical, and thermal specification
EPS	external product specification
FET	field effect transistor
FRB	fault resilient boot
FRU	field replaceable unit
FSB	front-side bus
FWH	firmware hub
GB	gigabyte – 1024 MB
GB/s	gigabytes per second
Gbit	Gigabit
Hz	hertz (frequency of measurement = 1 cycle/second)
I/O	input/output
I^2C*	inter-integrated circuit
ID	Identification
ISP	in-system programming
ITP	in-target probe
JTAG	Joint Test Action Group
LPC	low pin count
M	mega or million
m	Milli
mA	Milliamps
MB	megabyte – 1,024KB
MB/s	megabytes per second
Mbit	Megabit
Mbit/s	megabits per second
MHz	Megahertz
MP	Multiprocessor
MRH-D	memory repeater hub DRR

Term	Description
MRH-S	memory repeater hub (for SDRAM)
MT/s	megatransfer per second
PCB	printed circuit board
PCI	peripheral component interconnect
PID	programmable interrupt device
PLD	programmable logic device
PPOD	power pod
PROC	processor/memory complex
RAC	Rambus ASIC Cell
RAM	random access memory
RDRAM	RAMbus DRAM
RSL	Rambus signal level
SAPIC	streamlined APIC
SCSI	small computer systems interface
SCU	System Configuration Utility
SDRAM	synchronous dynamic RAM (DRAM type)
SM	server management
SMBus	I^2C server management bus
SMI	server management interrupt
SNC	scalable node controller
SNC-M	870 scalable node controller-Itanium 2
SP	scalability port
SRAM	static random access memory
SSTL	stub series terminated logic
STBY	Standby
U	rack unit (1.75”)
USB	Universal Serial Bus
V	Volt
VA	voltage ampere
Vac	alternating current (AC) voltage
Vdc	volts of direct current
VHDM	very high density module
VID	voltage identifier (ID)
VRM	voltage regulator module
Vstby	volts standby
Vtt	termination voltage
W	Watt

Glossary

This appendix contains important terms used in the preceding chapters.

Word / Acronym	Definition
E8870	The chipset used in the SR870BH2
ACPI	Advanced Configuration and Power Interface
ADC	Analog to Digital Converter.
AP	Application Processor.
API	Application Programming Interface.
APIC	Intel Advanced Programmable Interrupt Controller for Symmetric Multi-processor (SMP) systems.
Etc.	