Technical Information Manual

IntelliStation M Pro Type 6868
Professional Workstation

Note

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First Edition (December 1999)

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Preface

This *Technical Information Manual* provides information for the IBM® IntelliStation® M Pro Type 6868. The manual is intended for developers who want to provide hardware and software products to operate with this IBM computer and provides an in-depth view of how this IBM computer works. Users of this publication should have an understanding of computer architecture and programming concepts.

Related publications

In addition to this manual, the following IBM publications provide information related to the operation of the IBM IntelliStation M Pro:

- *IntelliStation M Pro User Guide*
  This hardcopy publication, also available on the *Software Selections CD*, contains information about setting up your computer, configuring your hardware and software, operating and maintaining your computer, and installing options. Also included are warranty information, instructions for diagnosing and solving problems, and information on how to obtain help and service.
- *Understanding Your Computer*
  This online publication is provided on the *Software Selections CD* that comes with your computer. If your computer has IBM-preinstalled software, this document is also available using Access IBM. It includes general information about using personal computers and in-depth information about the specific features of your computer.
- *Hardware Maintenance Manual*
  This publication contains information for trained service technicians. It is available at http://www.ibm.com/pc/support on the World Wide Web, and it can also be ordered from IBM. To purchase a copy, see the "Getting Help, Service, and Information" section in *IntelliStation M Pro User Guide*.
- *Adaptec SCSI Documentation*
  This documentation, which is provided on the *Software Selections CD* that comes with IntelliStation M Pro computers, includes information on the SCSI interface, including instructions for installing and configuring SCSI devices.

Terminology usage

Attention: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

In this manual, some signals are represented in a small, all-capital-letter format (-ACK). A minus sign in front of the signal indicates that the signal is active low. No sign in front of the signal indicates that the signal is active high.

The use of the term *hex* indicates a hexadecimal number.

When numerical modifiers such as K, M, and G are used, they typically indicate powers of 2, not powers of 10. For example, 1 KB equals 1 024 bytes (2^{10}), 1 MB equals 1 048 576 bytes (2^{20}), and 1 GB equals 1 073 741 824 bytes (2^{30}).

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When expressing storage capacity, MB equals 1 000 KB (1 024 000). The value is determined by counting the number of sectors and assuming that every two sectors equals 1 KB.

Note: Depending on the operating system and other system requirements, the storage capacity available to the user might vary.

Chapter 1. System overview

IntelliStation M Pro Type 6868 computer systems provide state-of-the-art computing power with room for future growth.

Major features

The major features are:

- An Intel® Pentium® III microprocessor with MMX™ technology, streaming single-instruction multiple data (SIMD) extensions, and 256 KB L2 cache
- Up to 2 GB of RAMBUS system memory
- Dual microprocessor support
- Integrated IDE bus master controller, Ultra DMA/66 capable
- SCSI hard disk drive
- System management
  - Wake on LAN® support
  - Desktop Management Interface (DMI) BIOS and DMI software
  - Integrated network protocols
  - Enablement for remote administration
  - Wake on Ring support
- IDE CD-ROM drive, standard
- Asset security
  - Security settings provided by the Configuration/Setup Utility program
    - Power-on and administrator password protection
    - Startup sequence control
    - Hard disk drive and diskette drive access control
    - I/O port control
  - Cover key lock
  - U-bolt and security cabling (optional)
  - Operating system security
  - Diskette write-protection
  - Alert on LAN® support
  - Tamper-detection switch on the chassis
- Accelerated graphics port (AGP)
- Integrated 16-bit stereo audio controller and built-in high-quality speaker in some models (supports AC-97 Audio, SoundBlaster, and Microsoft® sound system applications)
- Networking
  - IBM 10/100 megabits-per-second (Mbps) Ethernet with Wake on LAN support

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- Expansion
  - Four drive bays
  - Five PCI expansion slots
- PCI I/O bus compatibility
- 3.5-inch, 1.44 MB diskette drive
- Input/output features
  - One 25-pin, parallel port with Extended Capabilities Port (ECP)/Extended Parallel Port (EPP) support
  - One 9-pin, universal asynchronous receiver/transmitter (UART) serial port
  - Two 4-pin, Universal Serial Bus ports
  - One 6-pin, keyboard port
  - One 6-pin, mouse port
  - One 15-pin, DDC2B-compliant monitor port on the AGP adapter
  - Three 3.5-mm audio jacks (line out/headphone, line in, microphone)

Other features

The IntelliStation M Pro supports the following features.

Network support

IntelliStation M Pro computers are enabled to support management over a network. The following is a list of supported functions:

- CMOS Save/Restore utility program
- CMOS setup over LAN
- Selectable primary startup sequence
- POST/BIOS update from network:
- Selectable automatic power on startup sequence
- Wake on LAN
- Wake on Ring for serial port

Wake on LAN

The power supply of the computer supports the Wake on LAN feature. With the Wake on LAN feature, the computer can be turned on when a specific LAN frame is passed to the computer over the LAN. You can find the menu for setting the Wake on LAN feature in the Configuration/Setup Utility program.

Wake on Ring

All models can be configured to turn on the computer after a ring is detected from an external or internal modem. The menu for setting the Wake on Ring feature is in the Configuration/Setup Utility program. One option controls this feature:

- **Serial Ring Detect:** Use this option if the computer has an external modem connected to the serial port. if the computer has an internal modem.

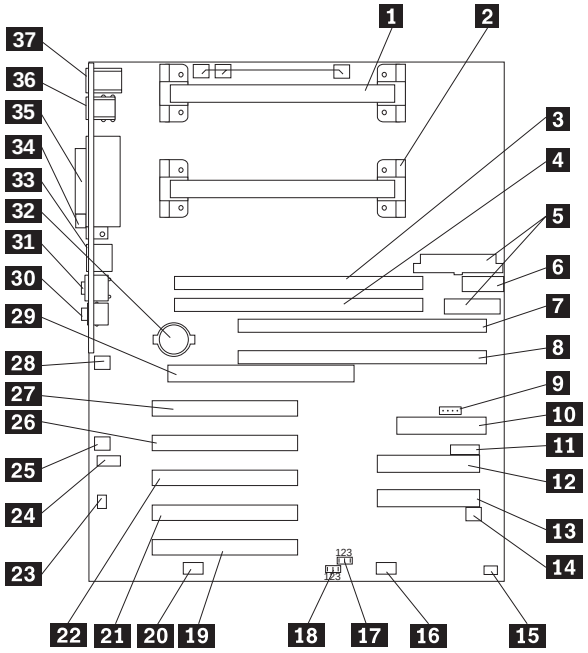
Chapter 2. System board features

This section includes information about system board features.

System board layout

The system board might look slightly different from the one shown.

Note: A diagram of the system board, including switch and jumper settings, is attached to the underside of the computer cover.



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2 Secondary microprocessor
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4 RIMM connector 2 (Channel A)
5 Power connectors
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7 RIMM connector 3 (Channel B)
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Pentium III microprocessor with MMX technology

IntelliStation M Pro Type 6868 comes with an Intel Pentium III microprocessor. The microprocessor, which has an attached heat sink, plugs directly into a connector on the system board.

Features

The features of this microprocessor are as follows:

- Optimization for 32-bit software
- 64-bit microprocessor data bus
- 133 MHz front-side bus (FSB)
- 256 KB L2 cache integrated into the microprocessor
- 32-bit microprocessor address bus
- Math coprocessor
- MMX technology, which boosts the processing of graphic, video, and audio data
- Cache speed is full processor core speed
  - 4-way set associative
  - Nonblocking

Chip set control

The Intel 840 chip set is the interface between the microprocessor and the following:

- Memory subsystem
- PCI bus
- IDE bus master connection
- USB ports
- SMBus
- Enhanced DMA controller
- Real-time clock (RTC)

System memory

The system memory interface is controlled by the Intel 840 chip set. Rambus dynamic random access memory (RDRAM) is standard.

The maximum amount of addressable system memory is 2 GB. For memory expansion, the system board provides four Rambus inline memory module (RIMM) connectors. Rambus memory is divided into two channels, A and B.

The system board supports PC600 memory and PC800 memory RIMMs in sizes of 64 MB, 128 MB, 256 MB, and 512 MB. Channels A and B must contain equal amounts of memory. The amount of preinstalled memory varies by model.

The following information applies to system memory:

- ECC (error checking and correction) RDRAM is standard.
- The maximum height of memory modules is 6.35 cm (2.5 in.).
- Install only ECC RIMMs to enable ECC.
- RIMM connectors do not support dual inline memory modules (DIMMs).
- Any connector that does not have a RIMM installed must have a *continuity RIMM* (C-RIMM), a module that looks like a RIMM but has no memory on it. A continuity RIMM continues the connection on a RIMM connector that does not have memory installed in it.

- Use PC600 or PC800 RIMMs only.
- Maximum system memory can be auto-detected and auto-configured using serial presence detect and configuration interface (BIOS specific).

  The following table shows the possible configuration of RIMMs and continuity RIMMs that can be used in the IntelliStation M Pro.

Figure 1. Memory configurations

Channel A		**Channel B**		**Functions as**
RIMM 1	**RIMM 2**	**RIMM 3**	**RIMM** 4	
PC600	PC600	PC600	PC600	PC600
PC800	PC800	PC800	PC800	PC800
PC600	PC600	PC600	PC800	PC600
PC600	PC600	PC800	PC600	PC600
PC600	PC800	PC600	PC600	PC600
PC800	PC600	PC600	PC600	PC600
PC800	PC600	PC800	PC600	PC600
PC600	PC800	PC600	PC800	PC600
PC800	PC800	PC800	PC600	PC600
PC600	C-RIMM	PC600	C-RIMM	PC600
C-RIMM	PC600	C-RIMM	PC600	PC600
PC800	C-RIMM	PC800	C-RIMM	PC800
C-RIMM	PC800	C-RIMM	PC800	PC800
PC600	C-RIMM	PC800	C-RIMM	PC600
C-RIMM	PC600	C-RIMM	PC800	PC600
PC800	C-RIMM	PC600	C-RIMM	PC600
C-RIMM	PC800	C-RIMM	PC600	PC600

Note:

- PC600 RIMM runs at 300 MHz
- PC800 RIMM runs at 400 MHz

For information on the pin assignments for the memory-module connectors, see “Memory connectors” on page 23.

PCI bus

The fully synchronous 33 MHz PCI bus originates in the chip set. Features of the PCI bus are:

- Integrated arbiter with multitransaction PCI arbitration acceleration hooks
- Zero-wait-state, microprocessor-to-PCI write interface for high-performance graphics
- Built-in PCI bus arbiter with support for up to six 32-bit PCI devices
- Microprocessor-to-PCI memory write posting
- Conversion of back-to-back, sequential, microprocessor-to-PCI memory write to PCI burst write
- PCI-to-DRAM up to 100+ megabytes per second (MBps) speed
- Multitransaction timer to support multiple, short PCI transactions within one PCI arbitration cycle
- PCI 2.2 compliant
- Delayed transaction
- PCI parity checking and generation support

IDE bus master interface

The system board incorporates a PCI-to-IDE interface that complies with the *AT Attachment Interface with Extensions* standard.

The bus master for the IDE interface is integrated into the I/O hub of the Intel 840 chip set. The chip set is PCI 2.2 compliant. It connects directly to the PCI bus and is designed to allow concurrent operations on the PCI bus and IDE bus. The chip set is capable of supporting PIO mode 0–4 devices and IDE DMA mode 0–3 devices, and ATA 66 transfers of up to 66 MBps.

The IDE devices receive their power through a four-position power cable containing +5dc, +12dc, and ground voltage. When devices are added to the IDE interface, one device is designated as the master device and another is designated as the slave or subordinate device. These designations are determined by switches or jumpers on each device. There are two IDE ports, one designated Primary and the other Secondary, allowing for up to four devices to be attached. The total number of physical IDE devices is determined by the mechanical package.

For the IDE interface, no resource assignments are given in the system memory or the direct memory access (DMA) channels. For information on the resource assignments, see “Input/output address map” on page 32 and Figure 34 on page 36 (for IRQ assignments).

Two connectors are provided on the system board for the IDE interface. For information on the connector pin assignments, see “IDE connectors” on page 26.

USB interface

Universal Serial Bus (USB) technology is a standard feature of the computer. The system board provides the USB interface with two connectors integrated into the ICH1 (I/O hub) in the chip set. A USB-enabled device can attach to a connector, and if that device is a hub, multiple peripheral devices can attach to the hub and be used by the system. The USB connectors use Plug and Play technology for installed devices. The speed of the USB is up to 12 MBps with a maximum of 127 peripheral devices. The USB is compliant with *Universal Host Controller Interface Guide 1.0*.

Features provided by USB technology include:

- Support for hot-pluggable devices
- Support for concurrent operation of multiple devices
- Suitability for different device speeds
- Support for up to five meters' (16 ft 4.9 in) cable length from host to hub or from hub to hub
- Guaranteed speeds and low latencies appropriate for specific devices
- Wide range of packet sizes
- Limited power to hubs

For information on the connector pin assignments for the USB interface, see “USB port connectors” on page 29.

Low pin-count bus

The low pin-count (LPC) bus is a new design that enables device connections to the Super I/O without ISA or X-Bus. The IntelliStation M Pro uses the National Semiconductor PC87363 Super I/O chip. The PC87363 chip runs at 33 MHz and includes the following:

- Diskette drive controller
- Keyboard and mouse controller
- IEEE 1284 parallel port
- One UART serial port

- General purpose input/output (GPIO) ports
- compliance
- ACPI compliance

A setting in the Configuration/Setup Utility program enables or disables diskette write protection.

Video subsystem

The IntelliStation M Pro comes with one of the following graphics solutions:

- Matrox Millennium G400 accelerated graphics port (AGP) adapter
- IBM Fire GL1 AGP adapter
- Appian Gemini AGP adapter
- Intense3D 4110 AGP adapter

Features of the Matrox Millennium G400 AGP adapter

The Matrox Millennium G400 AGP adapter is a 2D/3D video solution that includes the Matrox MGA G400 video chip, 16 MB of 166 MHz SGRAM, a 300 MHz random access memory and digital-to-analog converter (RAMDAC), an EEPROM module with video POST and BIOS code, video support for various hardware multimedia upgrades,and a DDC2B monitor connector.

The Matrox MGA G400 video chip is 100% compatible with VGA function, supports all video modes, and contains the following advanced features:

- Integrated video subsystem on the chip including 2D, 3D, and a video port
- 66 MHz AGP 4x system bus interface with sideband address support and a request queue depth of 32
- Command list bus-mastering support for fast 2D performance
- 128-bit, 166 MHz SGRAM interface with block write and write-per-bit support
- 256-bit internal data bus
- OpenGL MCD and Direct3D optimized 3D engine
- High-resolution support up to 2048 x 1536
- 300 MHz, internal RAMDAC that supports up to 75 Hz refresh rate at 1920 x 1440 resolution
- Second display output port capable of running at 136 MHz (1280 x 1024 at 75 Hz), which can support a TV, a second monitor, or a flat-panel display
- Multiple monitor and adapter support (up to 4) in one computer
- Compliance with the following standards:
  - PC98 (along with PC99, a Microsoft hardware requirement)
  - Accelerated Graphics Port (AGP) 2.0,
  - VESA VBE V2.0,
  - DDC2B
- Advanced power-management support
- Complete Plug and Play support

Features of the IBM Fire GL1 AGP adapter

The IBM Fire GL1 AGP adapter includes the IBM Oasis video chip, 32 MB of 100/124 MHz SGRAM, an EEPROM module that contains the video POST and BIOS code, and a DDC2B monitor connector.

The IBM Oasis chip uses CMOS technology and is 100% compatible with VGA function and supports all VGA modes. The IBM Oasis chip also
contains the following hardware features:

- Integrated video subsystem on a chip including 2D engine, 3D engine, and a RAMDAC
- 66 MHz AGP 2x capable system bus interface with sideband address support and a request queue depth of 9
- 256-bit, 2-way interleaved 100 MHz SGRAM interface with block write and write-per-bit support
- Dual DMA units used to move data between system memory and the video memory
- Pixel cache used for BitBLITs, rendering operations, and texture operations
- Overlay support on a per-window basis
- OpenGL MCD and Direct3D optimized 3D engine
- Pentium III single instruction, multiple data (SIMD) and multiprocessor optimization in the OpenGL ICD
- Video processor that includes color space conversion and hardware scaling with X and Y interpolation for high quality video playback.
- 250 MHz, internal RAMDAC that supports up to 85 Hz refresh rate at 1600 x 1200 or 75 Hz at 1920 x 1200
- Multiple monitor and adapter support (up to 4) in one computer
- Complete Plug and Play support, including the monitor

Features of the Appian Gemini AGP adapter

The Appian Gemini AGP adapter is a single-slot, dual-monitor graphics solution featuring a high-speed AGP 2X interface, 16 MB of on-board SGRAM running at 110 MHz and full VGA and SVGA compatibility. The Appian Gemini AGP adapter has two display channels and is designed to support multiple monitor configurations under Windows 98, Windows NT 4.0 Workstation, and Windows 2000.

The Appian Gemini AGP adapter uses a single Savage/MX graphics accelerator from S3 for dual monitor output. The Savage/MX features a 270 MHz RAMDAC for accelerated 2D and 3D graphics. The Appian Gemini AGP adapter card includes high-resolution display, plug and play compliance, support for video input/output, DVD motion compensation, support for DirectX 6 with hardware texture compression, and dual outputs.

The Appian Gemini also features the powerful and easy-to-use Appian HydraVision multiple monitor display management software for Windows 98, Windows NT 4.0 Workstation, and Windows 2000. HydraVision software enables user-defined placement of windows and dialog boxes within the multiple monitor display space and provides a variety of productivity tools designed specifically for multiple monitor management, including the following:

- S3 Savage/MX
- 270 MHz RAMDAC
- 1280 x 1024 x 24 bits per pixel (bpp) at 85 Hz on two channels
- AGP 2X interface with sideband addressing

- 16 MB 105 MHz SGRAM (shared frame buffer)
- Support for 8, 16, and 32 bits per pixel (bpp)
- Support for display power management signaling (DPMS) and Advanced Configuration and Power Interface (ACPI) management
- Display data channel (DDC) support
- Driver support
- Direct3D and OpenGL
- Support for video signal conversion between:
  - Phase Alternate Line (PAL)
  - National Television Systems Committee (NTSC)
  - Sequential Couleur Avec Memoire (SECAM, sequential color with memory)
- Appian TV Tuner support
- PC98 and PC99 compliance

Features of the Intense3D 4110 AGP adapter

The Intense 3D 4110 is a 2D/3D video solution with 128 MB 66.6 MHz SGRAM that includes:

- AGP 2x DMA transfer rates
- AGP 2x Fast write transfers from host microprocessor
- 8 MB SDRAM DirectBurst memory
- 64 MB frame buffer supporting SuperScene, full-scene, multisampled antialiasing
- Onboard texture memory with full bitmapped trilinear interpolated texture processing
- Maximum resolution of 1280 x 1024, 75 Hz vertical refresh for Windows NT (VGA) startup.
- 2 video lookup tables
- 16- and 32-bit color depths
- 10-bit gamma correction
- Sterioscopic views support - interlaced or frame sequential
- DDC monitor support
- DVI-I Digital flat-panel display support
- Synchronizing, or genlocking, of the video data to an external video source (requires optional plug on adapter module)
- Multiview functionality, which enables frame locking and rate locking of multiple workstations (requires optional plug on adapter module)
- Advanced power-management support
- Complete Plug and Play support

Video resources

The video subsystem supports all video graphics array (VGA) modes and is compliant with super video graphics array (SVGA) modes and the *Video Electronics Standards Association (VESA) 1.2*.

The graphics memory controller supports the VESA DDC standard 1.1 and uses DDC1 and DDC2B to determine optimal values during automatic monitor detection.

The video subsystem has the following resource assignments.

Figure 2. Video subsystem resources

Resource	Assignment
ROM	Hex C0000–C7FFF (32 KB)
RAM	Hex A0000–BFFFF
I/O (hex)	VGA registers: Attributes 0–14, CRT controller 0–18/22/24/26, CRTC Extension 0-6, DACSTAT, FEAT, GCTL 0-8, INSTS0-1, MISC, Sequencer 0-4, DAC
IRQ	PCI interrupt 1 (automatically assigned to IRQ 0BH by POST or can be disabled in the Configuration/Setup Utility)
DMA	None

For further information on resource assignments, see Appendix B, “System address maps” on page 32 and Appendix C, “IRQ and DMA channel assignments” on page 36.

The IntelliStation M Pro supports the following video subsystem modes.

Figure 3. Supported VGA video modes

Mode (hex)	Display mode	Screen resolution	Colors	Buffer start (hex)	Dot clock (MHz)	Sweep rate (kHz)	Refresh rate (Hz)
00	Text	40 x 25 characters	B/W	B8000	28.322	31.5	70
01	Text	40 x 25 characters	16	B8000	28.322	31.5	70
02	Text	80 x 25 characters	B/W	B8000	28.322	31.5	70
03	Text	80 x 25 characters	16	B8000	28.322	31.5	70
04	Graphics	320 x 200 pixels	4	B8000	25.175	31.5	70
05	Graphics	320 x 200 pixels	4	B8000	25.175	31.5	70
06	Text	640 x 200 pixels	2	B8000	25.175	31.5	70
07	Text	80 x 25 characters	Mono	B0000	28.322	31.5	70
0D	Graphics	320 x 200 pixels	16	A0000	25.175	31.5	70
0E	Graphics	640 x 200 pixels	16	A0000	25.175	31.5	70
0F	Graphics	640 x 350 pixels	Mono	A0000	25.175	31.5	70
10	Graphics	640 x 350 pixels	16	A0000	25.175	31.5	70
11	Graphics	640 x 480 pixels	2	A0000	25.175	31.5	70
12	Graphics	640 x 480 pixels	16	A0000	25.175	31.5	60
13	Graphics	320 x 200 pixels	256	A0000	25.175	31.5	70

Monitor support

The video subsystem provides a 15-pin monitor connector on the preinstalled graphics adapter. For information on connector pin assignments, see Appendix A, “Connector pin assignments” on page 23.

Audio subsystem

The IntelliStation M Pro comes with an integrated audio controller. These models are capable of playing and recording sounds and support SoundBlaster, Adlib, and Microsoft Windows Sound System applications.

The device drivers are on the hard disk and are also available on the *Product Recovery CD* or *Device Driver and IBM Enhanced Diagnostics CD* that comes with the computer.

If you connect an optional device to the audio connectors, follow the instructions provided by the manufacturer. (Note that device drivers might be required. If necessary, contact the manufacturer for information on these device drivers.)

The following connectors are available on the integrated audio controller:

- *Line/headphone out* port for connecting powered speakers. To hear audio from the adapter you must connect a set of speakers to the Line out port. These speakers must be powered with a built-in amplifier. In general, any powered speakers designed for use with personal computers can be used with the audio subsystem. These speakers are available with a wide range of features and power outputs.
- *Line in* port for connecting musical devices, such as a portable CD player or stereo system.
- *Microphone* for connecting a microphone.

Super input/output controller

Control of the integrated input/output (I/O) and diskette drive controllers is provided by a single module. This module, which supports Plug and Play, controls the following features:

- Diskette drive interface
- Serial port
- Parallel port
- Keyboard and mouse ports
- General-purpose I/O ports

Diskette drive interface

The IntelliStation M Pro diskette drive subsystem supports the following devices:

- 1.44 MB, 3.5-inch diskette drive
- 1.44 MB, 3.5-inch, 3-mode drive for Japan (no BIOS support for 3-mode drive)
- 1.2 MB, 5.25-inch diskette drive
- 1 Mpbs, 500 Kbps, or 250 Kbps internal tape drive

Note: A 2.88 MB, 3.5-inch diskette drive is not supported.

One 34-pin connector is provided on the system board for diskette drive support. For information on the connector pin assignments, see “Diskette drive connector” on page 27.

Serial port

One universal asynchronous receiver/transmitter (UART) serial port is integrated into the system board. The serial port includes 16-byte data, first-in first-out (FIFO) buffers and has a programmable baud rate generator. The serial port is NS16450 and PC16550A compatible.

For information on the connector pin assignments, see “Serial port connector” on page 30.

Note: Current loop interface is not supported.

The following figure shows the serial port assignments in the configuration.

Figure 4. Serial port assignments

Port assignment	Address range (hex)	IRQ level
Serial A	03F8–03FF	IRQ4

The default setting for the serial port is COM1.

Parallel port

Integrated in the system board is support for extended capabilities port (ECP), enhanced parallel port (EPP), and standard parallel port (SPP) modes. The modes of operation are selected through the Configuration/Setup Utility program with the default mode set to SPP. The ECP and EPP modes are compliant with IEEE 1284.

The following figure shows the parallel port assignments used in the configuration.

Figure 5. Parallel port assignments

Port assignment	Address range (hex)	IRQ level
Parallel 1	03BC–03BE	IRQ7
Parallel 2	0378–037F	IRQ5
Parallel 3	0278–027F	IRQ5

The default setting for the parallel port is Parallel 1.

The system board has one connector for the parallel port. For information on the connector pin assignments, see “Parallel port connector” on page 31.

Keyboard and mouse ports

The keyboard and mouse subsystem is controlled by a general purpose 8-bit microcontroller; it is compatible with 8042AH and PC87911. The controller consists of 256 bytes of data memory and 2 KB of read-only memory (ROM).

The controller has two logical devices: one controls the keyboard and the other controls the mouse. The keyboard has two fixed I/O addresses and a fixed IRQ line and can operate without the mouse. The mouse cannot operate without the keyboard because, although it has a fixed IRQ line, the mouse relies on the addresses of the keyboard for operation. For the keyboard and mouse interfaces, no resource assignments are given in the system memory addresses or DMA channels. For information on the resource assignments, see “Input/output address map” on page 32 and Figure 34 on page 36 (for IRQ assignments).

The system board has one connector for the keyboard port and one connector for the mouse port. For information on the connector pin assignments, see “Mouse and keyboard port connectors” on page 30.

Network connection

IntelliStation M Pro models have an integrated Ethernet controller, with the following features:

- Operates in shared 10BASE-T or 100BASE-TX environment
- Transmits and receives data at 10 Mbps or 100 Mbps
- Has a RJ-45 connector for LAN attachment
- Operates in symmetrical multiprocessing (SMP) environments
- Supports Wake on LAN
- Supports Alert on LAN
- Supports Remote Program Load (RPL) and Dynamic Host Configuration Protocol (DHCP)

Cabling requirements for Wake on LAN adapters

The IntelliStation M Pro has a 3-pin connector on the system board that provides the auxiliary 5 volts (AUX5) and wake-up signal connections.

Real-time clock and CMOS

The real-time clock is a low-power clock that provides a time-of-day clock and a calendar. The clock settings are maintained by an external battery source of +3 V dc.

The system uses 242 bytes of complementary metal-oxide semiconductor (CMOS) memory to store data. The CMOS memory is erased if the recovery jumper on the system board is moved.

To locate the battery, see “System board layout” on page 3.

Flash EEPROM

The system board uses 8 megabits (Mb) of flash electrically erasable, programmable, read-only memory (EEPROM) to store the basic input/output system (BIOS), video BIOS, IBM logo, Configuration/Setup Utility, and Plug and Play data.

If necessary, the EEPROM can be easily updated using a stand-alone utility program that is available on a 3.5-inch diskette.

Expansion adapters

Each PCI-expansion connector is a 32-bit slot. PCI-expansion connectors support the 32-bit +5 V dc, local-bus signaling environment that is defined in *PCI Local Bus Specification 2.1*.

The IntelliStation M Pro has five PCI slots to support the addition of adapters. For information on installing adapters, see the *IntelliStation M Pro User Guide*.

For information on the connector pin assignments, see “PCI connectors” on page 25.

Recovery jumper

The recovery jumper on the system board is used to reset CMOS default vaues. For the location of the recovery jumper, see the “System board layout” on page 3.

Figure 6. Recovery jumper

Pins	Description
1 and 2	Normal (factory default)
2 and 3	Clear CMOS/password, boot block recovery

Cable connectors

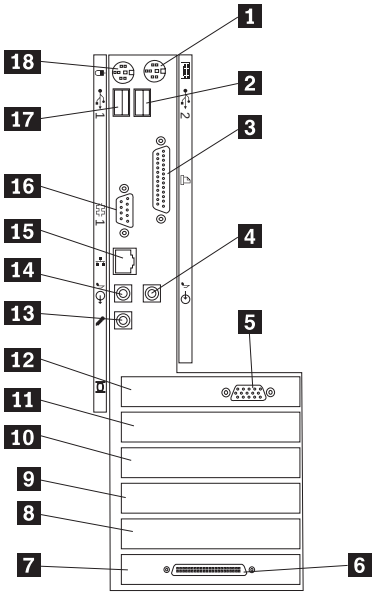
Connections for attaching devices are provided on the back of the computer. The connectors are:

- USB (2)
- Mouse
- Keyboard
- Serial
- Parallel
- Monitor (SVGA or DVI)
- Audio connectors for line in, line/headphone out, and microphone

Connector panel

Connectors for features integrated into the system board can be identified by an icon directly below each connector. A connector located on an adapter might not have an identifying icon.

For pin-out details on connectors, see Appendix A, “Connector pin assignments” on page 23. The following illustration shows the connector panel for the IntelliStation M Pro:



1 Keyboard connector
2 USB-2 connector
3 Parallel connector
4 Audio line in
5 Monitor connector
6 SCSI connector
7 PCI slot 5
8 PCI slot 4
9 PCI slot 3
10 PCI slot 2
11 PCI slot 1
12 AGP slot
13 Microphone connector
14 Audio line out connector
15 Ethernet connector
16 Serial connector
17 USB-1 connector
18 Mouse connector

Chapter 3. Physical specifications

This section lists the physical specifications for the IntelliStation M Pro Type 6868. The IntelliStation M Pro has five expansion slots and four drive bays.

Note: This computer is classified as a Class A digital device. Please see the *IntelliStation M Pro User Guide* for further information about this classification.

Dimensions

- Height: 492 mm (19.4 in.)
- Width: 200 mm (7.9 in.)
- Depth: 460 mm (18.1 in.)

Weight

- Minimum configuration as shipped: 18.1 kg (40 lb)
- Maximum configuration: 20.4 kg (45 lb)

Environment

- Air temperature:
  - System on: 10° to 35°C (50° to 95°F)
  - System off: 10° to 43°C (50° to 110°F)
  - Maximum altitude: 2134 m (7000 ft)

  Note: The maximum altitude, 2133.6 m (7000 ft.), is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.
- Humidity:
  - System on: 8% to 80%
  - System off: 8% to 80%

Electrical input

- Input voltage:
  - Low range:
    - Minimum: 90 V ac
    - Maximum: 137 V ac
    - Input frequency range: 57–63 Hz
    - Voltage switch setting: 115 V ac
  - High range:
    - Minimum: 180 V ac
    - Maximum: 265 V ac
    - Input frequency range: 47–53 Hz
    - Voltage switch setting: 230 V ac
  - Input kilovolt-amperes (kVA) (approximate):
    - Minimum configuration as shipped: 0.08 kVA
    - Maximum configuration: 0.28 kVA

Note: Power consumption and heat output vary depending on the number and type of optional features installed and the power management optional features in use.

Heat output

- Approximate heat output in British thermal units (Btu) per hour:
  - Minimum configuration: 245 Btu/hr (70 watts)
  - Maximum configuration: 700 Btu/hr (204 watts)

Airflow

- Approximately 0.56 cubic meter per minute (20 cubic feet per minute) maximum

Acoustical noise-emission values

- Average sound-pressure levels:
  - At operator position:
    - Idle: 37 dBA
    - Operating: 43 dBA
  - At bystander position–1 meter (3.3 ft):
    - Idle: 32 dBA
    - Operating: 36 dBA
- Declared (upper limit) sound-power levels:
  - Idle: 4.7 bels
  - Operating: 5.1 bels

Note: These levels were measured in controlled acoustical environments according to procedures specified by the American National Standards Institute (ANSI) S12.10 and ISO 7779 and are reported in accordance with ISO 9296. Actual sound-pressure levels in a given location might exceed the average values stated because of room reflections and other nearby noise sources. The declared sound-power levels indicate an upper limit, below which a large number of computers will operate.

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Chapter 4. Power supply

The IntelliStation M Pro uses a 330-watt power supply. This power supply provides +3.3-volt power for the Pentium microprocessor and core chip set and +5-volt power for PCI adapters. Also included is an auxiliary 5-volt (AUX 5) supply to provide power to power-management circuitry and the Wake on LAN feature. The power supply converts the ac input voltage into four dc output voltages and provides power for the following:

- System board
- Adapters
- Internal drives
- Keyboard and auxiliary devices
- USB devices

A logic signal on the power connector controls the power supply; the front panel switch is not directly connected to the power supply.

The power supply connects to the system board with a 2-pin by 10-pin connector.

Power input

The following figure shows the power-input specifications. The power supply automatically selects the correct input voltage.

Figure 7. Power-input requirements

Specification	Measurements
Input voltage, low range	100 (min) to 127 (max) V ac
Input voltage, high range	200 (min) to 240 (max) V ac
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz

Power output

The power supply outputs shown in the following figure includes the current-supply capability of all the connectors, including system board, DASD, PCI, and auxiliary outputs.

Figure 8. Power-output (330 watts)

Output voltage	Regulation	Minimum current	Maximum current
+5 volts	+5% to –4%	1.5 A	32.0 A
+12 volts	+5% to –5%	0.2 A	8.5 A
–12 volts	+10% to –9%	0.0 A	0.7 A
+3.3 volts	±5%	0.0 A	25.0 A
–5 volts	±10%	0.0 A	0.4 A
+5 volt (auxiliary)	+5% to –5%	0.005 A	0.75 A

Note: The total combined 3.3 V and 5 V power must not exceed 217 watts.

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Component outputs

The power supply provides separate voltage sources for the system board and internal storage devices. The following figures show the approximate power that is provided for specific system components. Many components draw less current than the maximum shown.

Figure 9. System board

Supply voltage	Maximum current	Regulation limits
+3.3 V dc	3000 mA	+5.0% to –5.0%
+5.0 V dc	4000 mA	+5.0% to –4.0%
+12.0 V dc	25.0 mA	+5.0% to –5.0%
–12.0 V dc	25.0 mA	+10.0% to –9.0%

Figure 10. Keyboard port

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	275 mA	+5.0% to –4.0%

Figure 11. PCI-bus adapters (per slot)

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	2000 mA	+5.0% to –4.0%
+3.3 V dc	3030 mA	+5.0% to –4.0%

Note: For each PCI connector, the maximum power consumption is rated at 10 watts for +5 V dc and +3.3 V dc combined. Typical power budget assumptions use 7.5 watts per adapter. If maximum power is used, the overall system configuration will be limit ed in performance.

Figure 12. USB port

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	500 mA	+5.0% to –4.0%

Figure 13. Internal DASD

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	1400 mA	+5.0% to –5.0%
+12.0 V dc	1500 mA at startup, 400 mA when active	+5.0% to –5.0%

Note: Some adapters and hard disk drives draw more current than the recommended limits. These adapters and drives can be installed in the system; however, the power supply will shut down if the total power used exceeds the maximum power that is available.

Output protection

The power supply protects against output overcurrent, overvoltage, and short circuits. See the power supply specifications on the previous pages for details.

A short circuit that is placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply. If this shutdown

state occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

If an overvoltage fault occurs (in the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

Connector description

The power supply for the IntelliStation M Pro has four 4-pin connectors for internal devices. The total power used by the connectors must not exceed the amount shown in “Component outputs” on page 17. For connector pin assignments, see Appendix A, “Connector pin assignments” on page 23.

Chapter 5. System software

This section briefly describes some of the system software included with the computer.

BIOS

The computer uses the IBM basic input/output system (BIOS), which is stored in flash electrically erasable programmable read-only memory (EEPROM). Some features of the BIOS are:

- PCI support in accordance with *PCI BIOS Specification 2.2*
- Microsoft PCI IRQ Routing Table
- Plug and Play support in accordance with *Plug and Play BIOS Specification 1.1a*
- Advanced Power Management (APM) support according to *APM BIOS Interface Specification 1.2*
- Wake on LAN support
- Wake on Ring support
- Alert on LAN support
- Remote program load (RPL) and Dynamic Host Configuration Protocol (DHCP)
- Startable CD-ROM support
- Flash-over-LAN support
- Alternate startup sequence
- IBM look and feel, such as screen arrangements
- *ACPI (Advanced Configuration and Power Interfaces) 1.0b*
- IDE logical block addressing (LBA) support
- LSA 2.0 support
- LS120 support
- *DM BIOS 2.1* (DMI 2.0 compliant)
- PC99 compliance

Plug and Play

Support for Plug and Play conforms to the following:

- *Plug and Play BIOS Specification 1.1a and 1.0*
- *Plug and Play BIOS Extension Design Guide 1.0*
- *Plug and Play BIOS Specification, Errata, and Clarifications 1.0*
- *Guide to Integrating the Plug and Play BIOS Extensions with system BIOS 1.2*
- Plug and Play Kit for DOS and Windows

POST

IBM power-on self-test (POST) code is used. Also, initialization code is included for the on-board system devices and controllers.

POST error codes include text messages for determining the cause of an error. For more information, see Appendix D, “Error codes” on page 37.

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Configuration/Setup Utility program

The Configuration/Setup Utility program provides menus for selecting options for devices, I/O ports, date and time, system security, start options, advanced setup, and power management.

More information on using the Configuration/Setup Utility program is provided in *IntelliStation M Pro User Guide*.

Advanced Power Management (APM)

The IntelliStation M Pro computers come with built-in energy-saving capabilities. Advanced Power Management (APM) is a feature that reduces the power consumption of systems when they are not being used. When enabled, APM initiates reduced-power modes for the monitor, microprocessor, and hard disk drive after a specified period of inactivity.

The BIOS supports APM 1.2. This enables the system to enter a power-managed state, which reduces the power drawn from the ac electrical outlet. Advanced Power Management is enabled through the Configuration/Setup Utility program and is controlled by the individual operating system.

For more information on APM, see *IntelliStation M Pro User Guide*.

Advanced Configuration and Power Interface (ACPI)

Advanced Configuration and Power Interface (ACPI) BIOS mode enables the operating system to control the power-management features of the computer. Not all operating systems support ACPI BIOS mode. See the operating system documentation to determine if ACPI is supported.

Flash update utility program

The flash update utility program is a stand-alone program to support flash updates. This utility program updates the BIOS code and can change the machine readable information (MRI) to different languages.

The flash update utility program is available on the World Wide Web at http://www.ibm.com/pc/us/intellistation. Look for the Downloadable Files link on this page.

Diagnostic program

The diagnostic program that comes with the IntelliStation M Pro computer is provided on the *Device Driver and IBM Enhanced Diagnostics CD*. It runs independently of the operating system. You can use IBM Enhanced Diagnostics to diagnose and repair problems with the computer. You can download the latest version from http://www.ibm.com/pc/support/desktop/desktop_support.html on the World Wide Web. For more information on this diagnostic program, see *IntelliStation M Pro User Guide*.

Chapter 6. System compatibility

This chapter discusses some of the hardware, software, and BIOS compatibility issues for the computer.

Hardware compatibility

This section discusses hardware, software, and BIOS compatibility issues that must be considered when designing application programs.

The functional interfaces are compatible with the following interfaces:

- Intel 8259 interrupt controllers (edge-triggered mode)
- National Semiconductor NS16450 and NS16550A serial communication controllers
- Motorola MC146818 Time of Day Clock command and status (CMOS reorganized)
- Intel 8254 timer, driven from a 1.193 MHz clock (channels 0, 1, and 2)
- Intel 8237 DMA controller, except for the Command and Request registers and the Rotate and Mask functions; the Mode register is partially supported
- Intel 8272 or 82077 diskette drive controllers
- Intel 8042 keyboard controller at addresses hex 0060 and hex 0064
- All video standards using VGA, EGA, CGA, MDA, and Hercules modes
- Parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode

Use this information to develop application programs. Whenever possible, use the BIOS as a hardware interface for maximum compatibility and portability of applications.

Hardware interrupts

Hardware interrupts are level-sensitive for PCI interrupts. The interrupt controller clears its in-service register bit when the interrupt routine sends an End-of-Interrupt (EOI) command to the controller. The EOI command is sent regardless of whether the incoming interrupt request to the controller is active or inactive.

The interrupt-in-progress latch is readable at an I/O-address bit position. This latch is read during the interrupt service routine and might be reset by the read operation or it might require an explicit reset.

Note: For performance and latency considerations, designers might want to limit the number of devices sharing an interrupt level.

With level-sensitive interrupts, the interrupt controller requires that the interrupt request be inactive at the time the EOI command is sent; otherwise, a new interrupt request will be detected. To avoid this, a level-sensitive interrupt handler must clear the interrupt condition (usually by a read or write operation to an I/O port on the device causing the interrupt). After processing the interrupt, the interrupt handler:

1. Clears the interrupt
2. Waits one I/O delay
3. Sends the EOI
4. Waits one I/O delay
5. Enables the interrupt through the Set Interrupt Enable Flag command

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Hardware interrupt IRQ9 is defined as the replacement interrupt level for the cascade level IRQ2. Program interrupt sharing is implemented on IRQ2, interrupt hex 0A. The following processing occurs to maintain compatibility with the IRQ2 used by IBM Personal Computer products:

1. A device drives the interrupt request active on IRQ2 of the channel.
2. This interrupt request is mapped in hardware to IRQ9 input on the second interrupt controller.
3. When the interrupt occurs, the system microprocessor passes control to the IRQ9 (interrupt hex 71) interrupt handler.
4. This interrupt handler performs an EOI command to the second interrupt controller and passes control to the IRQ2 (interrupt hex 0A) interrupt handler.
5. This IRQ2 interrupt handler, when handling the interrupt, causes the device to reset the interrupt request before performing an EOI command to the master interrupt controller that finishes servicing the IRQ2 request.

Hard disk drives and controller

Reading from and writing to the hard disk is initiated in the same way as in IBM Personal Computer products; however, new functions are supported.

Software compatibility

To maintain software compatibility, the interrupt polling mechanism that is used by IBM Personal Computer products is retained. Software that interfaces with the reset port for the IBM Personal Computer positive-edge interrupt sharing (hex address 02F*x* or 06F*x*, where *x* is the interrupt level) does not create interference.

Software interrupts

With the advent of software interrupt sharing, software interrupt routines must daisy chain interrupts. Each routine must check the function value, and if it is not in the range of function calls for that routine, it must transfer control to the next routine in the chain. Because software interrupts are initially pointed to address 0:0 before daisy chaining, check for this case. If the next routine is pointed to address 0:0 and the function call is out of range, the appropriate action is to set the carry flag and do a RET 2 to indicate an error condition.

Machine-sensitive programs

Programs can select machine-specific features, but they must first identify the machine and model type. IBM has defined methods for uniquely determining the specific machine type. The machine model byte can be found through Interrupt 15H, Return System Configuration Parameters function (AH)=(C0H).

Appendix A. Connector pin assignments

The following figures show the pin assignments for various system board connectors.

Monitor connector

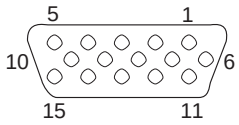

Figure 14. Monitor port connector pin assignments—SVGA

Pin	Signal	I/O	Pin	Signal	I/O
1	Red	O	2	Green	O
3	Blue	O	4	Monitor ID 2 - Not used	I
5	Ground		6	Red ground	
7	Green ground		8	Blue ground	
9	+5 V, used by DDC2B		10	Ground	
11	Monitor ID 0 - Not used	I	12	DDC2B serial data	I/O
13	Horizontal sync	O	14	Vertical sync	O
15	DDC2B clock	I/O			

Memory connectors

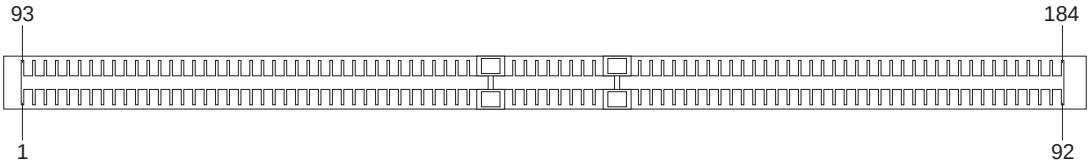

Figure 15 (Page 1 of 2). System memory connector pin assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Gnd	93	Gnd	47	NC	139	NC
2	LDQA8	94	LDQA7	48	NC	140	NC
3	Gnd	95	Gnd	49	NC	141	NC
4	LDQA6	96	LDQA5	50	NC	142	NC
5	Gnd	97	Gnd	51	Vref	143	Vref
6	LDQA4	98	LDQA3	52	Gnd	144	Gnd
7	Gnd	99	Gnd	53	SCL	145	SA0
8	LDQA2	100	LDQA1	54	Vdd	146	Vdd
9	Gnd	101	Gnd	55	SDA	147	SA1
10	LDQA0	102	LCFM	56	SVdd	148	SVdd
11	Gnd	103	Gnd	57	SWP	149	SA2
12	LCTMN	104	LCFMN	58	Vdd	150	Vdd

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Figure 15 (Page 2 of 2). System memory connector pin assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
13	Gnd	105	Gnd	59	RSCK	151	RCMD
14	LCTM	106	NC	60	Gnd	152	Gnd
15	Gnd	107	Gnd	61	RDQB7	153	RDQB8
16	NC	108	LROW2	62	Gnd	154	Gnd
17	Gnd	109	Gnd	63	RDQB5	155	RDQB6
18	LROW1	110	LROW0	64	Gnd	156	Gnd
19	Gnd	111	Gnd	65	RDQB3	157	RDQB4
20	LCOL4	112	LCOL3	66	Gnd	158	Gnd
21	Gnd	113	Gnd	67	RDQB1	159	RDQB2
22	LCOL2	114	LCOL1	68	Gnd	160	Gnd
23	Gnd	115	Gnd	69	RCOL0	161	RDQB0
24	LCOL0	116	LDQB0	70	Gnd	162	Gnd
25	Gnd	117	Gnd	71	RCOL2	163	RCOL1
26	LDQB1	118	LDQB2	72	Gnd	164	Gnd
27	Gnd	119	Gnd	73	RCOL4	165	RCOL3
28	LDQB3	120	LDQB4	74	Gnd	166	Gnd
29	Gnd	121	Gnd	75	RROW1	167	RROW0
30	LDQB5	122	LDQB6	76	Gnd	168	Gnd
31	Gnd	123	Gnd	77	NC	169	RROW2
32	LDQB7	124	LDQB8	78	Gnd	170	Gnd
33	Gnd	125	Gnd	79	RCTM	171	NC
34	LSCK	126	LCMD	80	Gnd	172	Gnd
3	Vcmos	127	Vcmos	81	RCTMN	173	RCFMN
36	SOUT	128	SIN	82	Gnd	174	Gnd
37	Vcmos	129	Vcmos	83	RDQA0	175	RCFM
38	NC	130	NC	84	Gnd	176	Gnd
39	Gnd	131	Gnd	85	RDQA2	177	RDQA1
40	NC	132	NC	86	Gnd	178	Gnd
41	Vdd	133	Vdd	87	RDQA4	179	RDQA3
42	Vdd	134	Vdd	88	Gnd	180	Gnd
43	NC	135	NC	89	RDQA6	181	RDQA5
44	NC	136	NC	90	Gnd	182	Gnd
45	NC	137	NC	91	RDQA8	183	RDQA7
46	NC	138	NC	92	Gnd	184	Gnd

PCI connectors

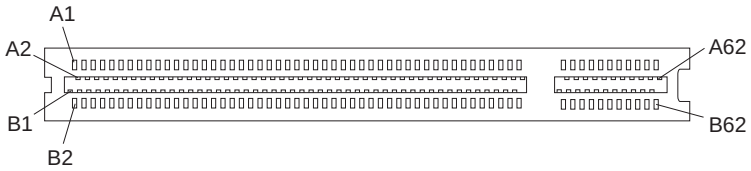

Figure 16 (Page 1 of 2). PCI connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
A1	TRST#	O	B1	–12 V dc	
A2	+12 V dc		B2	TCK	O
A3	TMS	O	B3	Ground	
A4	TDI	O	B4	TDO	I
A5	+5 V dc		B5	+5 V dc	
A6	INTA#	I	B6	+5 V dc	
A7	INTC#	I	B7	INTB#	I
A8	+5 V dc		B8	INTD#	I
A9	Reserved		B9	PRSNT1#	I
A10	+5 V dc		B10	Reserved	
A11	Reserved		B11	PRSNT2#	I
A12	Ground		B12	Ground	
A13	Ground		B13	Ground	
A14	3.3 V AUX		B14	3.3 V AUX	
A15	RST#	O	B15	Ground	
A16	+5 V dc (I/O)		B16	CLK	O
A17	GNT#	O	B17	Ground	
A18	Ground		B18	REQ#	I
A19	PCI		B19	+5 V dc	
A20	Address/data 30	I/O	B20	Address/data 31	I/O
A21	+3.3 V dc		B21	Address/data 29	I/O
A22	Address/data 28	I/O	B22	Ground	
A23	Address/data 26	I/O	B23	Address/data 27	I/O
A24	Ground	I/O	B24	Address/data 25	
A25	Address/data 24	I/O	B25	+3.3 V dc	
A26	IDSEL	O	B26	C/BE 3#	I/O
A27	+3.3 V dc		B27	Address/data 23	I/O
A28	Address/data 22	I/O	B28	Ground	
A29	Address/data 20	I/O	B29	Address/data 21	I/O
A30	Ground	I/O	B30	Address/data 19	
A31	Address/data 18	I/O	B31	+3.3 V dc	
A32	Address/data 16	I/O	B32	Address/data 17	I/O
A33	+3.3 V dc		B33	C/BE 2#	I/O
A34	FRAME#	I/O	B34	Ground	
A35	Ground		B35	IRDY#	I/O
A36	TRDY#	I/O	B36	+3.3 V dc	

Figure 16 (Page 2 of 2). PCI connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
A37	Ground		B37	DEVSEL#	I/O
A38	STOP#	I/O	B38	Ground	
A39	+3.3 V dc		B39	LOCK#	I/O
A40	SMBCLK[1]	I/O	B40	PERR#	I/O
A41	SMBDATA[1]	I/O	B41	+3.3 V dc	
A42	Ground		B42	SERR#	I/O
A43	PAR		B43	+3.3 V dc	
A44	Address/data 15	I/O	B44	C/BE 1#	I/O
A45	+3.3 V dc	I/O	B45	Address/data 14	I/O
A46	Address/data 13		B46	Ground	
A47	Address/data 11	I/O	B47	Address/data 12	I/O
A48	Ground	I/O	B48	Address/data 10	I/O
A49	Address/data 9		B49	Ground	
A50	Key		B50	Key	
A51	Key		B51	Key	
A52	C/BE(0)#	I/O	B52	Address/data 8	I/O
A53	+3.3 V dc	I/O	B53	Address/data 7	I/O
A54	Address/data 6		B54	+3.3 V dc	
A55	Address/data 4	I/O	B55	Address/data 5	I/O
A56	Ground	I/O	B56	Address/data 3	I/O
A57	Address/data 2		B57	Ground	
A58	Address/data 0	I/O	B58	Address/data 1	I/O
A59	+5 V dc		B59	+5 V dc	
A60	ACK64#	I/O	B60	ACK64#	I/O
A61	+5 V dc		B61	+5 V dc	
A62	+5 V dc		B62	+5 V dc	

.

IDE connectors

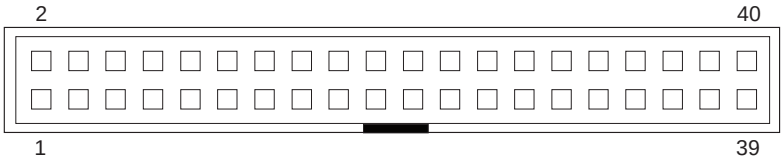

Figure 17 (Page 1 of 2). IDE connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	RESET	O	21	NC	

[1] These assignments are for PCI connector slot one only; for all other slots, the signal for pin A40 is SDONE and for pin A41 is SBO#

Figure 17 (Page 2 of 2). IDE connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
2	Ground		22	Ground	
3	Data bus bit 7	I/O	23	I/O write	O
4	Data bus bit 8	I/O	24	NC	
5	Data bus bit 6	I/O	25	I/O read	O
6	Data bus bit 9	I/O	26	Ground	
7	Data bus bit 5	I/O	27	I/O channel ready	I
8	Data bus bit 10	I/O	28	ALE	O
9	Data bus bit 4	I/O	29	NC	
10	Data bus bit 11	I/O	30	Ground	
11	Data bus bit 3	I/O	31	IRQ	I
12	Data bus bit 12	I/O	32	CS16#	I
13	Data bus bit 2	I/O	33	SA1	O
14	Data bus bit 13	I/O	34	PDIAG#	I
15	Data bus bit 1	I/O	35	SA0	O
16	Data bus bit 14	I/O	36	SA2	O
17	Data bus bit 0	I/O	37	CS0#	O
18	Data bus bit 15	I/O	38	CS1	O
19	Ground		39	Active#	I
20	Key (Reserved)		40	Ground	

Diskette drive connector

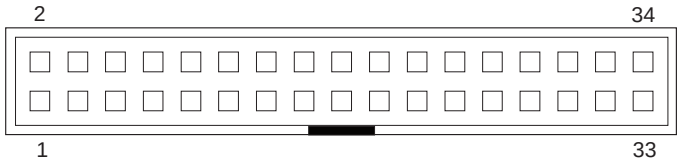

Figure 18 (Page 1 of 2). Diskette drive connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Drive 2 installed #	I	2	High density select	O
3	Not connected		4	Not connected	
5	Ground		6	Data rate 0	
7	Ground		8	Index#	I
9	Reserved		10	Motor enable 0#	O
11	Ground		12	Drive select 1#	O
13	Ground		14	Drive select 0#	O
15	Ground		16	Motor enable 1#	O
17	MSEN1	I	18	Direction in#	O
19	Ground		20	Step#	O
21	Ground		22	Write data#	O
23	Ground		24	Write enable#	O
25	Ground		26	Track0#	I
27	MSEN0	I	28	Write protect#	I

Figure 18 (Page 2 of 2). Diskette drive connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
29	Ground		30	Read data#	I
31	Ground		32	Head 1 select#	O
33	Data rate 1		34	Diskette change#	I

Power supply connector

Figure 19. Power supply connector pin assignments

Pin	Signal name	Pin	Signal name
1	+3.3 V dc	11	+3.3 V dc
2	+3.3 V dc	12	–12 V dc
3	Ground	13	Ground
4	+5 V dc	14	ON/OFF
5	Ground	15	Ground
6	+5 V dc	16	Ground
7	Ground	17	Ground
8	PWR GOOD	18	–5 V dc
9	+5 V dc standby	19	+5 V dc
10	+12 V dc	20	+5 V dc

Wake on LAN connectors

Figure 20. Wake on LAN connector pin assignments

Pin	Description
1	+5 V dc standby
2	Ground
3	Wake on LAN

Alert on LAN connectors

Figure 21. Alert on LAN connector pin assignments

Pin	Description
1	SMB Data
2	SMB Clock
3	Intrusion

Tamper detection switch

Figure 22 (Page 1 of 2). Tamper switch pin assignments

Pin	Description
1	Ground

Figure 22 (Page 2 of 2). Tamper switch pin assignments	
Pin	**Description**
2	Tamper switch

Radio frequency ID

Figure 23. Radio frequency identification (RFID) pin assignments	
Pin	**Description**
1	RFID Ant 1
2	Key
3	Ground
4	RFID Ant 2

SCSI high frequency LED connectors

Figure 24. SCSI high frequency LED connector pin assignments	
Pin	**Description**
1	Not connected
2	to LED
3	to LED
4	Not connected

CD audio connector

Figure 25. CD audio connector pin assignments	
Pin	**Description**
1	CD-in left
2	CD-in Ground
3	CD-in Ground
4	CD-in right

USB port connectors

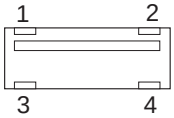

Figure 26 (Page 1 of 2). USB port connector pin assignments	
Pin	**Signal**
1	VCC
2	-Data
3	+Data

Figure 26 (Page 2 of 2). USB port connector pin assignments	
Pin	**Signal**
4	Ground

Mouse and keyboard port connectors

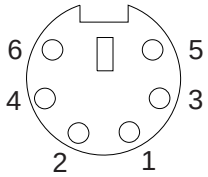

Figure 27. Mouse port connector pin assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Data	I/O	2	Reserved	I/O
3	Ground		4	+5 V dc	
5	Clock	I/O	6	Reserved	

Figure 28. Keyboard port connector pin assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Keyboard data	I/O	2	Mouse data	I/O
3	Ground		4	+5 V dc	
5	Keyboard clock	I/O	6	Mouse clock	I/O

Serial port connector

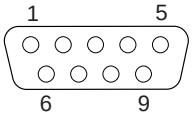

Figure 29. Serial port connector pin assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Data carrier detect	I	2	Receive data#	I
3	Transmit data#	O	4	Data terminal read	O
5	Ground		6	Data set ready	I
7	Request to send	O	8	Clear to send	I
9	Ring indicator	I			

Parallel port connector

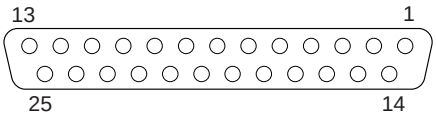

Figure 30. Parallel port connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	STROBE#	I/O	2	Data bit 0	I/O
3	Data bit 1	I/O	4	Data bit 2	I/O
5	Data bit 3	I/O	6	Data bit 4	I/O
7	Data bit 5	I/O	8	Data bit 6	I/O
9	Data bit 7	I/O	10	ACK#	I
11	BUSY	I	12	PE	I
13	SLCT	I	14	AUTO FD XT#	O
15	ERROR#	I	16	INIT#	O
17	SLCT IN#	O	18	Ground	
19	Ground		20	Ground	
21	Ground		22	Ground	
23	Ground		24	Ground	
25	Ground				

Appendix B. System address maps

The following charts represent how the hard disk stores different types of information. Address ranges and byte sizes are approx imate.

System memory map

The first 640 KB of system board RAM is mapped starting at address hex 0000000. A 256 byte area and a 1 KB area of this RAM are reserved for BIOS data. Memory can be mapped differently if POST detects an error.

Figure 31. System memory map

Address range (decimal)	Address range (hex)	Size	Description
0 K – 512 K	00000–7FFFF	512 KB	Conventional
512 K – 639 K	80000–9FBFF	127 KB	Extended conventional
639 K – 640 K	9FC00–9FFFF	1 KB	Extended BIOS data
640 K – 767 K	A0000–BFFFF	128 KB	Dynamic video memory display cache
768 K – 800 K	C0000 to C7FFF	32 KB	Video ROM BIOS (shadowed)
800 K – 896 K	C8000–DFFFF	96 KB	PCI space, available to adapter ROMs
896 K – 1 MB	E0000–FFFFF	128 KB	System ROM BIOS (main memory shadowed)
1 MB – 16 MB	100000–FFFFFF	15 MB	PCI space
16 MB – 4096 MB	1000000–FFDFFFF	4080 MB	PCI space (positive decode)
4096 – 4120 MB	FFFE0000 – FFFFFFFF	128 KB	System ROM BIOS

Input/output address map

The following figure lists resource assignments for the I/O address map. Any addresses that are not shown are reserved.

Figure 32 (Page 1 of 3). I/O address map

Address (Hex)	Size (bytes)	Description
0000–000F	16	DMA 1
0010–001F	16	General I/O locations, available to PCI bus
0020–0021	2	Interrupt controller 1
0022–003F	30	General I/0 locations, available to PCI bus
0040–0043	4	Counter/timer 1
0044–00FF	28	General I/0 locations, available to PCI bus
0060	1	Keyboard controller byte, reset IRQ
0061	1	PIIX4, system port B
0064	1	Keyboard controller, CMD/STAT byte
0070, bit 7	1 bit	Enable NMI
0070, bits 6:0	1 bit	Real-time clock, address
0071	1	Real-time clock, data

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Figure 32 (Page 2 of 3). I/O address map

Address (Hex)	Size (bytes)	Description
0072–007F	14	General I/O locations, available to PCI bus
0080	1	POST checkpoint register during POST only
008F	1	Refresh page register
0080–008F	16	ICH1, DMA page registers
0090–0091	15	General I/O locations, available to PCI bus
0092	1	PS/2 keyboard controller registers
0093–009F	15	General I/O locations
00A0–00A1	2	Interrupt controller 2
00A2–00BF	30	APM control
00C0–00DF	31	DMA 2
00E0–00EF	16	General I/O locations, available to PCI bus
00F0	1	BX, Coprocessor Error register
00F1–016F	127	General I/O locations, available to PCI bus
0170–0177	8	Secondary IDE channel
01F0–01F7	8	Primary IDE channel
0200–0207	8	Available
0220–0227	8	SMC 37C673, Serial port 3 or 4
0228–0277	80	General I/O locations, available to PCI bus
0278–027F	8	SMC 27C673, LPT3
0280–02E7	102	Available
02E8–02EF	8	SMC PC37C673, Serial port 3 or 4
02F8–02FF	8	COM2
0338–033F	8	SMC PC37C673, serial port 3 or 4
0340–036F	48	Available
0370–0371	2	SMC SIO system board Plug and Play index,data registers
0372–0375	4	Available
0376–0377	2	IDE channel 1 command
0378–037F	8	LPT2
0380–03B3	52	Available
03B4–03B7	4	Video
03BA	1	Video
03BC–03BE	16	LPT1
03C0–03CF	16	Video
03D4–03D7	4	Video
03DA	1	Video
03D0–03DF	11	Available
03E0–03E7	8	Available
03E8–03EF	8	COM3 or COM4
03F0–03F5	6	Diskette channel 1
03F6	1	Primary IDE channel command port
03F7 (Write)	1	Diskette channel 1 command
03F7, bit 7	1 bit	Diskette disk change channel
03F7, bits 6:0	7 bits	Primary IDE channel status port

Figure 32 (Page 3 of 3). I/O address map

Address (Hex)	Size (bytes)	Description
03F8–03FF	8	COM1
0400–047F	128	Available
0480–048F	16	DMA channel high page registers
0490–0CF7	1912	Available
0CF8–0CFB	4	PCI Configuration address register
0CFC–0CFF	4	PCI Configuration data register
LPT*n* + 400h	8	ECP port, LPT*n* base address + hex 400
0CF9	1	Turbo and reset control register
0D00–FFFF	62207	Available

DMA I/O address map

The following figure lists resource assignments for the DMA address map. Any addresses that are not shown are reserved.

Figure 33 (Page 1 of 2). DMA I/O address map

Address (hex)	Description	Bits	Byte pointer
0000	Channel 0, Memory Address register	00–15	Yes
0001	Channel 0, Transfer Count register	00–15	Yes
0002	Channel 1, Memory Address register	00–15	Yes
0003	Channel 1, Transfer Count register	00–15	Yes
0004	Channel 2, Memory Address register	00–15	Yes
0005	Channel 2, Transfer Count register	00–15	Yes
0006	Channel 3, Memory Address register	00–15	Yes
0007	Channel 3, Transfer Count register	00–15	Yes
0008	Channels 0–3, Read Status/Write Command register	00–07	
0009	Channels 0–3, Write Request register	00–02	
000A	Channels 0–3, Write Single Mask register bits	00–02	
000B	Channels 0–3, Mode register (write)	00–07	
000C	Channels 0–3, Clear byte pointer (write)	A	
000D	Channels 0–3, Master clear (write)/temp (read)	00–07	
000E	Channels 0–3, Clear Mask register (write)	00–03	
000F	Channels 0–3, Write All Mask register bits	00–03	
0081	Channel 2, Page Table Address register [2]	00–07	
0082	Channel 3, Page Table Address register [2]	00–07	
0083	Channel 1, Page Table Address register [2]	00–07	
0087	Channel 0, Page Table Address register [2]	00–07	
0089	Channel 6, Page Table Address register [2]	00–07	
008A	Channel 7, Page Table Address register [2]	00–07	
008B	Channel 5, Page Table Address register [2]	00–07	
008F	Channel 4, Page Table Address/Refresh register	00–07	
00C0	Channel 4, Memory Address register	00–15	Yes
00C2	Channel 4, Transfer Count register	00–15	Yes

Figure 33 (Page 2 of 2). DMA I/O address map

Address (hex)	Description	Bits	Byte pointer
00C4	Channel 5, Memory Address register	00–15	Yes
00C6	Channel 5, Transfer Count register	00–15	Yes
00C8	Channel 6, Memory Address register	00–15	Yes
00CA	Channel 6, Transfer Count register	00–15	Yes
00CC	Channel 7, Memory Address register	00–15	Yes
00CE	Channel 7, Transfer Count register	00–15	Yes-
00D0	Channels 4–7, Read Status/Write Command register	00–07	
00D2	Channels 4–7, Write Request register	00–02	
00D4	Channels 4–7, Write Single Mask register bit	00–02	
00D6	Channels 4–7, Mode register (write)	00–07	
00D8	Channels 4–7, Clear byte pointer (write)		
00DA	Channels 4–7, Master clear (write)/temp (read)	00–07	
00DC	Channels 4–7, Clear Mask register (write)	00–03	
00DE	Channels 4–7, Write All Mask register bits	00–03	
00DF	Channels 5–7, 8- or 16-bit mode select	00–07	

PCI configuration space map

The following figures list the PCI allocations.

Bus number (hex)	Device number (hex)	Function number (hex)	Description
00	00	00	Intel 84440BX (host bridge)
00	01	00	Intel 84440BX (PCI/AGP)
00	1E	0	Intel 82371AB Hub interface to PCI bridge registers
00	1F	01	Intel 82371AB IDE bus master
00	1F	02	Intel 82371AB USB
00	1F	0	Intel 82371AB Interface bridge registers
00	1F	5	AC '97 audio controller
02	X	00	PCI connectors

[2] Upper byte of memory address register.

Appendix C. IRQ and DMA channel assignments

The following figures list the interrupt request (IRQ) and direct memory access (DMA) channel assignments.

Figure 34. IRQ channel assignments

IRQ	System resource
NMI	Critical system error
SMI	System management interrupt for power management
0	Reserved (interval timer)
1	Reserved (keyboard)
2	Reserved, cascade interrupt from slave PIC
3	COM2 [3]
4	COM1 [3]
5	LPT2/audio (if present)
6	Diskette controller
7	LPT1 [3]
8	Real-time clock
9	Video
10	Available to user
11	Available to user
12	Mouse port
13	Reserved (math coprocessor)
14	Primary IDE (if present)
15	Secondary IDE (if present)

Figure 35. DMA channel assignments

DMA channel	Data width	System resource
0	8 bits	Open
1	8 bits	Open
2	8 bits	Diskette drive
3	8 bits	Parallel port (for ECP or EPP)
4		Reserved (cascade channel)
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

[3] Default, can be changed to another IRQ.

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Appendix D. Error codes

The *IntelliStation M Pro User Guide* and the *Hardware Maintenance Manual* provide complete lists of error and beep codes.

POST error codes

POST error messages appear when, during startup, POST finds problems with the hardware or a change in the hardware configuration. POST error messages are 3-, 4-, 5-, 8-, or 12-character alphanumeric messages.

Beep codes

Beep codes are a series of tones in sets of two or three that sound when there are POST errors. The beep pattern represents numeric v alues and provide further information about the location of a potential problem.

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