Table 2-1.
Glossary of Symbols

Symbol	Definition
EA	Effective operand address; the address from which the operand will be obtained. This is determined only after all selection of sectors, indexing, and indirect addressing required have been performed.
n	Specified number of shifts to be performed.
N	Two's complement of the number of shifts to be performed.
ADB	Address Bus
INB	Input Bus
OTB	Output Bus
PMI	Previous Mode Indicator - associated with Extended Addressing Model 516-05, 06
DP Mode	Double Precision Mode associated with Model 516-11
A	A-Register (16-bits)
P	Program Counter (16-bits) -
B	B-Register (16-bits)
E	E-Register (16-bits)
X	Index Register (16-bits)
M	M-Register (16 bits)
C	C-bit (1 bit)
$\longrightarrow$	Replaces
$\rightleftharpoons$	Is exchanged with
$\longrightarrow\!\!\!\!\!\!\downarrow$	Is discarded
$\wedge$	Logical AND
$\vee$	Logical OR
$\not\vee$	Exclusive OR
+	Algebraic Addition
( )	Contents of a hardware register (e. g., (A) = contents of A-Register)
[ ]	Contents of core location specified by (e. g. [EA] = contents of core location specified by EA)
T	Tag Bit (bit 2 of instruction word)
MR	Memory Reference Instruction
G	Generic Instruction
SH	Shift Instruction
IO	Input-Output Instruction

Table 2-2.
DDP-516 Instruction Repertoire

Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
Load and Store						
CRA	G	140040	Clear A	O → (A)	1	0.96
IAB	G	000201	Interchange A and B	(A) ⇆ (B)	1	0.96
IMA	MR	13	Interchange Memory and A	(A) ⇆ [EA]	3	2.88
INK	G	000043	Input Keys	(C) → $(A)_1$ (DP Mode) → $(A)_2$ (PMI) → $(A)_3$ O → $(A)_{4-11}$ Shift Count → $(A)_{12-16}$	1	0.96
LDA	MR	02	Load A	[EA] → (A)	2	1.92
LDX	MR	15 T = 1	Load X	[EA] → (X) [EA] → [00000]	3	2.88
			NOTE This instruction cannot be indexed. However, if indirect addressing is called for, the indirect address can be indexed in the usual manner.			
OTK	G	171020	Output Keys	$(A)_1$ → (C) $(A)_2$ → (DP Mode) $(A)_3$ → (PMI) $(A)_{12-16}$ → Shift Count	2	1.92
STA	MR	04	Store A	(A) → [EA]	2	1.92
STX	MR	15 T = 0	Store X	(X) → [EA]	2	1.92
			NOTE This instruction cannot be indexed. However, if indirect addressing is called for, the indirect address can be indexed in the usual manner.			
Arithmetic						
ACA	G	141216	Add C to A	(A) + (C) → (A) Overflow status → (C)	1	0.96
ADD	MR	06	Add	(A) + [EA] → (A) Overflow status → (C)	2	1.92
AOA	G	141206	Add One to A	(A) + 1 → (A) Overflow status → (C)	1	0.96

Table 2-2. (Cont)
DDP-516 Instruction Repertoire

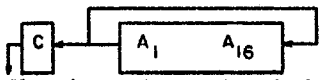
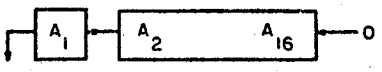
Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
SUB	MR	07	Subtract	(A) - [EA] → (A) Overflow status → C	2	1.92
TCA	G	141407	Two's Complement A	- (A) → (A)	1.5	1.44
Logical						
ANA	MR	03	AND to A	(A) ∧ [EA] → (A) EXAMPLE: (A) 0 1 0 1; [EA] 0 0 1 1; RESULT IN A 0 0 0 1	2	1.92
CSA	G	140320	Copy Sign and Set Sign Plus	$(A)_1 \rightarrow (C)$ $0 \rightarrow (A)_1$	1	0.96
CHS	G	140024	Complement A Sign	$\overline{(A)}_1 \rightarrow (A)_1$	1	0.96
CMA	G	140401	Complement A	$\overline{(A)} \rightarrow (A)$	1	0.96
ERA	MR	05	Exclusive OR to A	(A) ⊻ [EA] → (A) EXAMPLE: (A) 0 0 1 1; [EA] 0 1 0 1; RESULT IN A 0 1 1 0	2	1.92
SSM	G	140500	Set Sign Minus	$1 \rightarrow (A)_1$	1	0.96
SSP	G	140100	Set Sign Plus	$0 \rightarrow (A)_1$	1	0.96
Shift						
ALR	SH	0416N	Logical Left Rotate	 The A register is shifted left, end-around (n) positions. A_1 is shifted out to A_{16} and the C bit. The C bit takes the state of the last bit shifted into A_{16}.	1 + n/2	0.96 + 0.48n
ALS	SH	0415N	Arithmetic Left Shift	 Overflow status → (C) The A register is shifted left (n) positions. If shifting causes a change in the sign of A at any time during the instruction, the C bit is set. If the sign is not changed, the C bit is reset. After 16 or more shifts, the A register contains ZERO.	1 + n/2	0.96 + 0.48n

Table 2-2. (Cont)
DDP-516 Instruction Repertoire

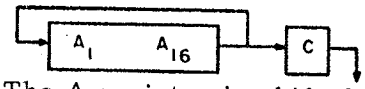
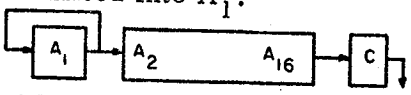
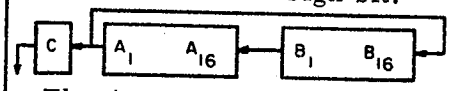
Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
ARR	SH	0406N	Logical Right Rotate	 The A register is shifted right, end around (n) positions. Bits shifted out of A_{16} enter A_1 and the C bit. The C bit takes the state of the last bit shifted into A_1.	1 + n/2	0.96 + 0.48n
ARS	SH	0405N	Arithmetic Right Shift	 The A register is shifted right (n) positions. The sign bit (A_1) does not change; it is shifted into vacated positions of the register. Bits shifted out of A_{16} enter the C bit. The C bit takes the state of the last bit shifted out of the register. If 15 or more shifts are specified, all stages of the A register will be the same as the sign bit.	1 + n/2	0.96 + 0.48n
LLR	SH	0412N	Long Left Rotate	 The A and B registers are treated as a single 32-bit register and shifted left, end around, (n) positions. Bits shifted out of B_1 enter A_{16}; bits shifted out of A_1 enter B_{16} and the C bit. Bits shifted out of C bit are discarded. The C bit takes the state of the last bit shifted into B_{16}.	1 + n/2	0.96 + 0.48n

Table 2-2. (Cont)
DDP-516 Instruction Repertoire

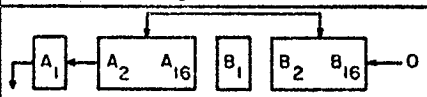
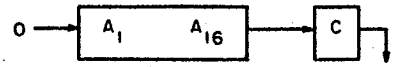
Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
LLS	SH	0411N	Long Arithmetic Left Shift	 Overflow Status → (C) The A and B registers are treated as a single 31-bit register (B_1 is not changed) and shifted left n positions. ZEROs are shifted into vacated positions through B_{16}. Bits shifted out of B_2 enter A_{16}. If at any time during the instruction the sign of the A register $(A)_1$ is changed, the C bit is set. If at the end of the instruction the sign has not been changed, the C bit is reset. If 31 or more shifts are specified, the A and B registers contain ZERO (except for B_1, which is unchanged).	1 + n/2	0.96 + 0.48n
LGL	SH	0414N	Logical Left Shift	 The A register is shifted left (n) positions. ZEROs fill in vacated bit positions. A_1 is shifted to the C bit. Bits shifted out of C are discarded. After 16 or more shifts, the A register contains ZERO. The C bit takes the state of the last bit shifted out of the register.	1 + n/2	0.96 + 0.48n
LGR	SH	0404N	Logical Right Shift	 The A register is shifted right (n) positions. ZEROs fill in vacated bit positions. A_{16} is shifted to the C bit. Bits shifted out of C are discarded. After 16 or more shifts, the A register contains ZERO. The C bit takes the state of the last bit shifted out of the register.	1 + n/2	0.96 + 0.48n

Table 2-2. (Cont)
DDP-516 Instruction Repertoire

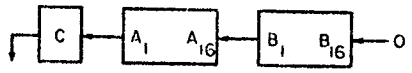
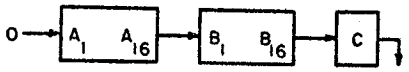
Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
LLL	SH	0410N	Long Left Logical Shift	 The A and B registers are treated as a single 32-bit register (A being the most significant) and shifted left n positions. Zeros are shifted into vacated positions of B. Bits are shifted from B_1 to A_{16}. Each bit shifted out of A_1 enters the C bit. Bits shifted out of the C bit are discarded. If 32 or more shifts are specified, the A and B registers will contain ZERO. The C bit takes the state of the last bit shifted out of the register.	1 + n/2	0.96 + 0.48n
LRL	SH	0400N	Long Right Logical Shift	 The A and B registers are treated as a single 32-bit register (A being the most significant) and shifted right n positions. Bits shifted out of A_1 enter B_1. Bits shifted out of B_{16} enter the C bit. Bits shifted out of C bit are discarded. ZEROs are shifted into vacated positions through A_1. The C bit takes the state of the last bit shifted out of the register. If 32 or more shifts are specified, the A and B registers will contain ZERO.	1 + n/2	0.96 + 0.48n

Table 2-2. (Cont)
DDP-516 Instruction Repertoire

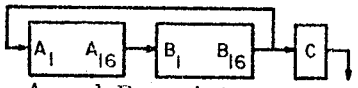
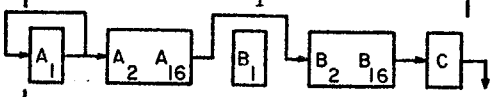
Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
LRR	SH	0402N	Long Right Rotate	 The A and B registers are treated as a single 32-bit register (A being the most significant) and shifted right, end-around (n) positions. Bits shifted out of A_{16} enter B_1. Bits shifted out of B_{16} enter A_1 and the C bit. Bits shifted out of C are discarded. The C bit takes the state of the last bit shifted into A_1.	1 + n/2	0.96 + 0.48n
LRS	SH	0401N	Long Arithmetic Right Shift	 The A and B registers are treated as a single 31-bit register (B_1 is not changed) and shifted right (n) positions. The sign bit, in A_1, is not unchanged; it is propagated into vacated positions of the register. Bits shifted out of A_{16} enter B_2. Bits shifted out of B_{16} enter the C bit. (Bits shifted out of the C bit are discarded.) After 30 or more shifts, both registers are filled with the sign of the A register, except for B_1 which is unchanged. The C bit takes the state of the last bit shifted out of the register.	1 + n/2	0.96 + 0.48n

Table 2-2. (Cont)
DDP-516 Instruction Repertoire

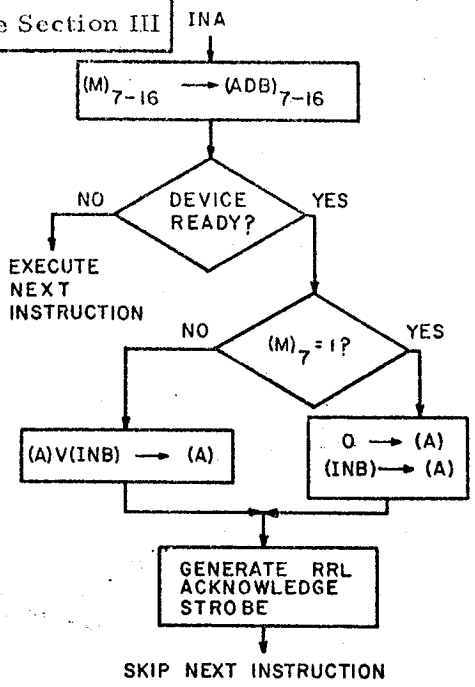
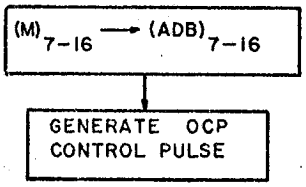
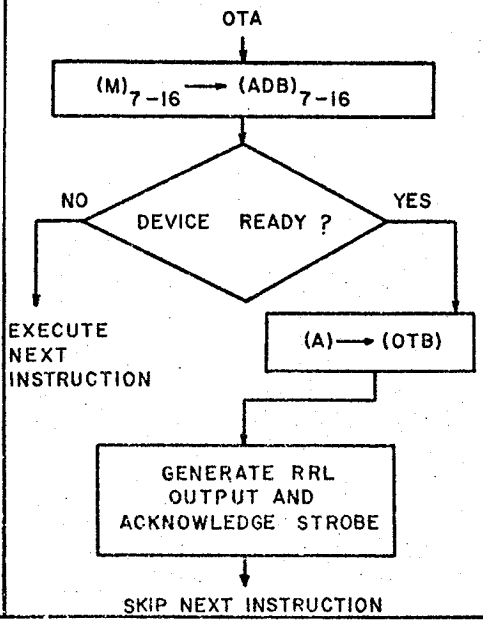
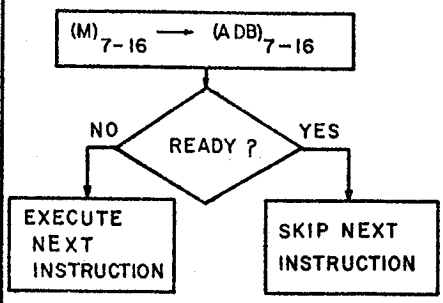
Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
Input-Output		For I/O Discussion see Section III				
INA	IO	54 For INA Codes see Appendix	Input to A		2	1.92
OCP	IO	14 For OCP codes see Appendix	Output Control Pulse		2	1.92
OTA	IO	74 For OTA codes see Appendix	Output from A		2	1.92

Table 2-2. (Cont)
DDP-516 Instruction Repertoire

Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
SMK	IO	74 For SMK codes see Appendix	Set Mask (Special OTA)	(A) → (OTB) Generate SMK pulse to transfer output bus to external device mask flip-flops. This instruction does not skip.	2	1.92
SKS	IO	34 For SKS codes see Appendix	Skip if Ready Line Set	$(M)_{7-16} \rightarrow (ADB)_{7-16}$ 	2	1.92
Control						

CAS	MR	11	Compare	Algebraically compare (A) and [EA]
				If (A) > [EA], execute next instruction
				If (A) = [EA], skip next instruction
				If (A) < [EA], skip two instructions
					3	2.88

ENB	G	000401	Enable Program Interrupt	Set machine status to permit interrupt. The permit interrupt status will not take effect until the instruction immediately following ENB is completed. (PI indicator lights.)	1	0.96
HLT	G	000000	Halt	Sets machine to halt mode. No further instructions or interrupts will be serviced until the console START button is pressed, at which time normal execution resumes.		
INH	G	001001	Inhibit Program Interrupt	Resets "permit interrupt status" to prohibit standard or priority interrupts. (PI indicator is extinguished.)	1	0.96

Table 2-2. (Cont)
DDP-516 Instruction Repertoire

Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
IRS	MR	12	Increment, replace and Skip	[EA] + 1 → [EA] If [EA] + 1 = 0, skip next instruction	3	2.88
JMP	MR	01	Unconditional Jump	EA → (P) Next instruction to be executed is at location EA.	1	0.96
JST	MR	10	Jump and Store Location	$(P_{3-16}) \rightarrow [EA_{3-16}]$ $[EA_{1,2}]$ not changed $EA_{3-16} + 1 \rightarrow (P_{3-16})$	3	2.88
NOP	G	101000	No Operation	Performs no operation. Computer proceeds to next instruction.	1	0.96
RCB	G	140200	Reset C Bit	O → (C)	1	0.96
SCB	G	140600	Set C Bit	1 → (C)	1	0.96
SKP	G	100000	Unconditional Skip	Skip next instruction	1	0.96
SLN	G	101100	Skip if (A_{16}) One	If $(A_{16}) = 1$: skip next instruction	1	0.96
SLZ	G	100100	Skip if (A_{16}) Zero	If $(A_{16}) = 0$: skip next instruction	1	0.96
SMI	G	101400	Skip if A Minus	If $(A_1) = 1$: skip next instruction	1	0.96
SNZ	G	101040	Skip if A Not Zero	If (A) ≠ 0: skip next instruction	1	0.96
SPL	G	100400	Skip if A Plus	If $(A_1) = 0$: skip next instruction	1	0.96
SR1	G	100020	Skip if Sense Switch 1 is Reset	If Sense Switch 1 is OFF: skip next instruction	1	0.96
SR2	G	100010	Skip if Sense Switch 2 is Reset	If Sense Switch 2 is OFF: skip next instruction	1	0.96
SR3	G	100004	Skip if Sense Switch 3 is Reset	If Sense Switch 3 is OFF: skip next instruction	1	0.96

Table 2-2. (Cont)

DDP-516 Instruction Repertoire

Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
SR4	G	100002	Skip if Sense Switch 4 is Reset	If Sense Switch 4 is OFF: skip next instruction	1	0.96
SRC	G	100001	Skip if C Reset	If (C) = 0: skip next instruction	1	0.96
SS1	G	101020	Skip if Sense Switch 1 is Set	If Sense Switch 1 is ON: skip next instruction	1	0.96
SS2	G	101010	Skip if Sense Switch 2 is Set	If Sense Switch 2 is ON: skip next instruction	1	0.96
SS3	G	101004	Skip if Sense Switch 3 is Set	If Sense Switch 3 is ON: skip next instruction	1	0.96
SS4	G	101002	Skip if Sense Switch 4 is Set	If Sense Switch 4 is ON: skip next instruction	1	0.96
SSC	G	101001	Skip if C Set	If (C) = 1: skip next instruction If Sense Switch 4 is ON: execute next instruction	1	0.96
SSR	G	100036	Skip if No Sense Switch Set	If no Sense Switches are ON: skip next instruction	1	0.96
SSS	G	101036	Skip if Any Sense Switch Set	If any Sense Switch is ON: skip next instruction	1	0.96
SZE	G	100040	Skip if A Zero	If (A) = 0: skip next instruction	1	0.96
Half-Word						
CAL	G	141050	Clear A, Left Half	$O \rightarrow (A_{1-8})$ (A_{9-16}) are unchanged	1	0.96
CAR	G	141044	Clear A, Right Half	$O \rightarrow (A_{9-16})$ (A_{1-8}) are unchanged	1	0.96
ICA	G	141340	Interchange Characters in A	$(A_{1-8}) \leftrightarrows (A_{9-16})$ A_1 is interchanged with A_9, A_2 with A_{10}, etc.	1	0.96

Table 2-2. (Cont)
DDP-516 Instruction Repertoire

Mnemonic	Type	Op Code	Definition	Description	No. of Cycles	Time (μsec)
ICL	G	141140	Interchange and Clear Left Half of A	$(A_{1-8}) \rightarrow (A_{9-16})$ $O \rightarrow (A_{1-8})$ Bits 9-16 of A are replaced with bits 1-8; bits 1-8 are cleared.	1	0.96
ICR	G	141240	Interchange and Clear Right Half of A	$(A_{9-16}) \rightarrow (A_{1-8})$ $O \rightarrow (A_{9-16})$ Bits 1-8 of A are replaced with bits 9-16; bits 9-16 are cleared.	1	0.96